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Polyphase Filter Design Methodology for Wireless communication Applications

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1. Introduction

The growing wireless communication market has generated increasing interest in highly integrated circuits. This has been a relentless pressure for low cost, low power and small size of transceivers. At the same time, the emergent mobile communications require high-speed data transmission and high data-rate systems. For instance, the IEEE 802.11a/g wireless standards, which incorporate OFDM (Orthogonal Frequency Division Multiplexing) modulation, are able to provide up to 54Mbps. This has led to many improvements in design and development of circuit components and transceiver architectures.

Progress in silicon integrated circuit technology and innovations in their design have enabled mobile products and services. In most current designs, the analog part of a receiver uses multiple integrated circuits which may have been implemented in Gallium Arsenide (GaAs), Silicon Germanium (SiGe) or bipolar processes. They offer the best performance in terms of speed, noise sensitivity and component matching. Implementing similar circuits in CMOS processes with the same performances is still challenging because of its low process tolerances, parasitic effects and low quality factor passive components. However, CMOS process offers high density of integration and low consumption making it a good candidate for wireless communications (Mikkelsen, 1998).

In radiofrequency (RF) receivers, frequency down-conversion is an essential operation. It consists on the translation of the incoming RF signal to a lower frequency called the intermediate frequency (IF). This is typically performed by mixing the amplified RF signal with the local oscillator (LO) signal. The IF is defined as

$$f_{IF} = |f_{RF} - f_{LO}| \quad (1)$$

However, this frequency translation provides a serious problem of frequency image rejection (Razavi (a), 1997). Hence, classical wireless receiver architectures have been commonly implemented using the superheterodyne topology, in which the image suppression is done by off-chip devices such as discrete components, ceramic or surface acoustic wave (SAW) filters (Razavi, 1996; Samavati et al, 2000; Macedo & Copeland, 1998). They have high quality factor and good linearity; however, their high cost and their non

integration make them less attractive to be used in the emerging integrated receivers (Razavi (a), 1997; Huang et al, 1999).

To overcome this drawback, zero-IF receiver architectures, in which the RF signal is transposed directly to baseband, have been proposed (Razavi (b), 1997; Behzad et al, 2003). Since the LO is at the same frequency as the RF input, this architecture removes the IF and the image rejection problem, which arises differently in the receiver chain and results from mismatches between the I (in-phase) and Q (quadrature) paths as well as amplitude mismatches. Although the direct conversion performs well image rejection, this architecture suffers from flicker noise, DC offsets and self-mixing at the inputs of the mixers, resulting in filter saturation and distortion.

To understand how the problem of frequency image arises, consider the process of down-conversion as represented in the Fig.1. When mixing the wanted signal band (at f_{RF}) with the LO, the obtained signal band is located at f_{IF}. But, since a simple analog multiplication does not preserve the polarity of the difference between the two mixed signals (i.e $\cos(\omega_1-\omega_2)t=\cos(\omega_2-\omega_1)t$), the signal band at f_{RF}-$2f_{IF}$ is also translated to the same IF after mixing with the LO. The signal at f_{RF}-$2f_{IF}$ is known as the image frequency. Therefore, any undesired signal located at the image frequency will be translated to the same IF along with the desired RF signal. And, this image signal may distort the wanted signal and lead to an improper system work. Thus, the image signal must be filtered before mixing.

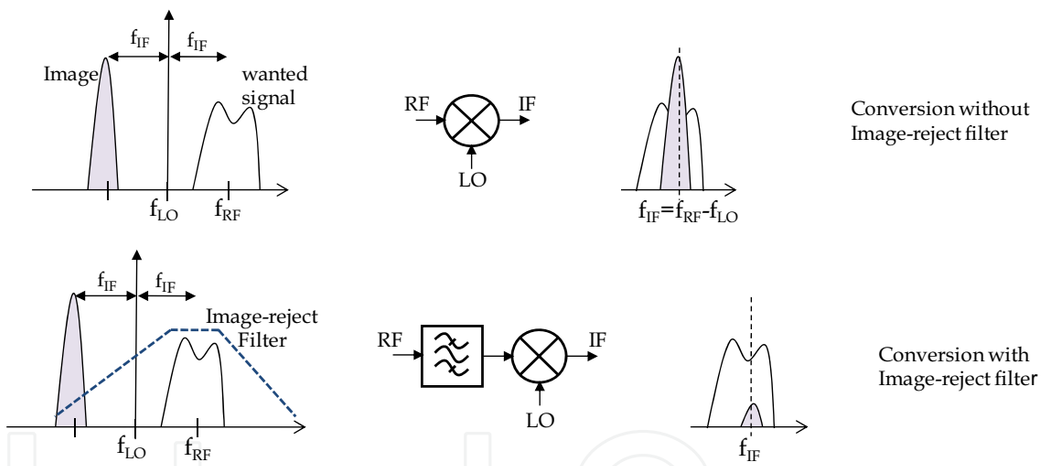


Fig. 1. Image rejection problem in RF receivers

An important specification to determine the performance of a receiver and to quantify its degree of image rejection is the image rejection ratio defined as the ratio of the magnitude in the attenuation band to that in the passband and can be given by

$$IRR = \frac{Desired\ Signal\ Level}{Image\ Signal\ Level} \tag{2}$$

The IRR required to ensure signal integrity and suitable bit-error-rate (BER) varies depending on the application. As an example, for short-range applications where low or moderate selectivity is required, an image suppression of 45dB is adequate, but is far less than that required in long-range heterodyne receivers. For example, DECT and DCS-1800

applications require 50dB and 60dB of image rejection respectively (Long, 1996). Method proposed ten years ago (Rudell et al, 1997), enforced external tuning or laser trimming and achieved image-rejection ratios, typically on the order of 35-50dB.
In this article, we will study first a state-of-the-art of the image rejection techniques as well as their implementation constraints inside wireless architectures. This study concerns essentially the image-reject architectures and focuses on complex polyphase filters. Then, we will propose a design methodology dedicated to passive polyphase filters (PPF) which includes in the design flow an analytical model allowing quantifying the impact of the mismatch of the components and the resulting signal in the IRR degradation. This methodology takes into account the non ideality of passive components (parasitic capacitances and resistors) together with the symmetry of the signal path during the layout design. Different techniques dedicated to layout matching combined with optimum component sizing from an experimental method are proposed so as to increase the IRR. Such a method gives a possibility to design PPFs operating from wide frequency range (1MHz to 5GHz) and allows attaining high performances in terms of IRR (about 60 dB). The proposed method has been validated with some test-cases in full CMOS technology.

2. Image rejection techniques

2.1 Image-reject architectures

Image-rejection architectures are the most known methods for implementing image rejection structures. They can typically be divided into half-complex and full-complex architectures (Crols et al, 1998; Steyaert et al, 2000) (Fig.2).

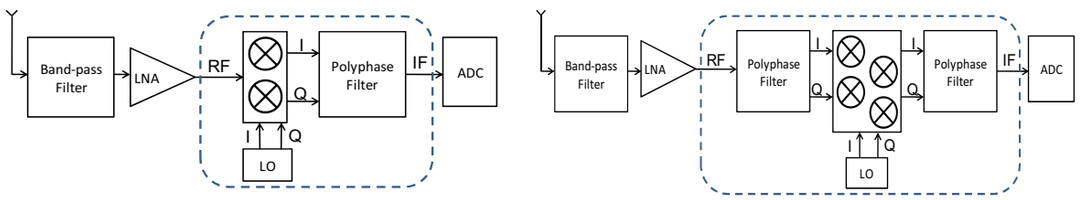


Fig. 2. Half-complex (a) and full-complex (b) receiver architectures, using polyphase filters

The half-complex architecture is based on the use of image-reject mixers combined with passive or active filters. As shown in Fig.2(a), a real RF signal is mixed with a LO complex signal to feed the IF polyphase filter. The quality of the image rejection inside such an architecture results mainly from three parameters: i) the balance between I and Q signals (phase and magnitude error), ii) the adequate matching of mixers iii) the polyphase filter performances.
There are two well-known architectures using such techniques: the Hartley and Weaver architectures, depicted in Fig.3 (Razavi (b), 1996; Xu et al, 2001). Generally, the Weaver topology is preferred to the Hartley architecture. In fact, the 90° phase shifter bloc (Fig.3(a)) comes with hard design constraints in terms of component matching which result to significant phase error especially at high frequencies. For instance, a change of 20% in resistors and capacitors (used to generate the quadrature), due to temperature and process variations, gives an IRR of only 20dB (Maligeorgos & Long, 2000).

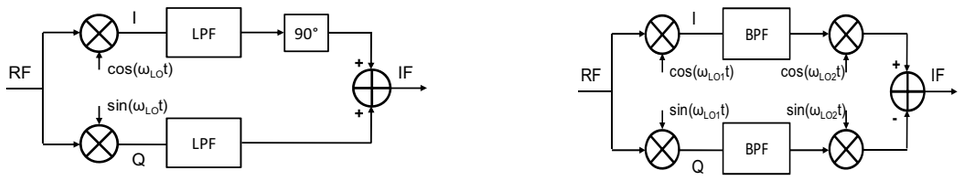


Fig. 3. Hartley (a) and Weaver (b) image-reject architectures

Basic Hartley and Weaver implementations proposed in the literature have typically IRRs in the range of 30-40dB (Carta et al, 2005). This is far below the 60dB required by wireless standards (Long & Maliepaard, 1999). In fact, phase mismatch between I and Q signals and gain mismatch between mixer signal paths result to much lower image rejection value. The IRR can be expressed as a function of the mismatches (Rudell et al, 1997)

$$IRR = \frac{1 + (1 + \Delta A)^2 + 2(1 + \Delta A)\cos(\varphi_1 + \varphi_2)}{1 + (1 + \Delta A)^2 - 2(1 + \Delta A)\cos(\varphi_1 + \varphi_2)} \tag{3}$$

where φ_1 and φ_2 represent the phase errors of LO_1 and LO_2 respectively, and ΔA is the gain error between I and Q paths. As shown in Fig.4, the IRR as a function of the total phase and gain mismatch. Thus, in order to provide an IRR of 60dB with a gain mismatch of 0.1%, the LO phase errors must be less than 0.1°.

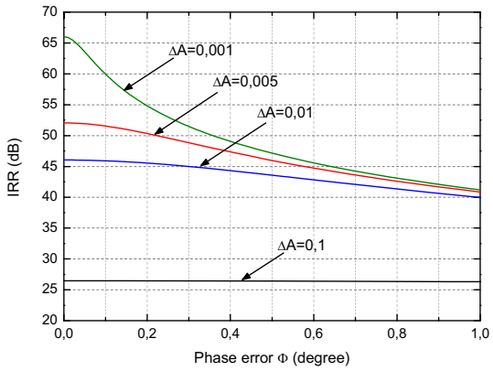


Fig. 4. Image rejection ratio (IRR) versus the phase mismatch for different gain mismatch quantities (Rudell et al., 1997)

The need for a monolithic solution for image-reject receiver which can perform gain and phase calibration is obvious. Various calibration techniques to correct the mismatch have been developed using analog or digital circuits. Digital calibration techniques have been implemented at the analog-to-digital converter (ADC) level inside the receiver chain (Valkama & Renfors, 2000; Sun et al, 2008) using either background digital correlation loops or commutated feedback capacitor switching to correct non-idealities in baseband components. Another technique is proposed in (Montemayor & Razavi, 2000) and consists on a self-calibrating architecture. It determines the phase and gain mismatches of a Weaver architecture and applies a feedback through gain and phase adjustment. A special dedicated tone at the image frequency is used and a periodic calibration with the external image tone is needed. This property restricts its application on systems using time division multiple access (TDMA). This method improves the image rejection with no penalty in linearity,

noise or gain, but increases the power consumption. Another technique consists on continuous calibration in a modified-image-reject-Weaver architecture (Elmala & Embabi, 2004). The phase and gain mismatches quantities are calibrated independently without the use of any external calibrating tones. This system generates two control signals using a variable delay gain circuit in two independent calibration loops. A further technique, based on the Weaver architecture, consists on simultaneous calibration by a sign-sign least mean square (SS-LMS) algorithm (Der & Razavi, 2003). The LMS adaptation circuit adjusts the phase and gain mismatches differentially to avoid systematic control. Digitally storing the calibration coefficients solves the problem of periodic refreshing, making it suitable for systems using code division multiple access (CDMA), but an external image tone is still needed in calibration procedure. Furthermore, a post-processing image rejection algorithm is proposed in (Lerstaveesin & Song, 2006) to reject the image in the baseband using an adaptive zero-forcing sign-sign feedback concept and does not require complicated digital processing. This algorithm can detect and correct I/Q imbalance continuously, but it alleviates the need for a high resolution ADC in the digital image rejection device.

Despite the difficulty to realize accurate phase shifters, (Chou & Lee, 2007) demonstrates that this is not essential in the Weaver architecture. The image rejection is performed by making the phase mismatch between I and Q signals of the first LO to be equal to that of the second LO. Thus the design constraints on phase matching are relaxed, and more attention can be placed on gain matching (Chou & Lee, 2007).

The full-complex architecture (also referred as double quadrature down-conversion) requires the use of complex polyphase filters. The complex polyphase filters are suitable for high frequency applications since they can meet the dynamic range and bandwidth requirement in RF frequencies (Wu & Chou, 2004). In this case, a notch frequency located at the image frequency is used to reject image signals rather than bandpass filtering. As shown in Fig.2(b), the RF signal is complex filtered (RF polyphase filter), then the RF and LO complex signals are multiplied together to feed the IF polyphase filter, to reach about 60dB of image suppression (Behbahani et al, 2001). The interest of this structure comes from the fact that the image rejection is supported in the RF domain by the RF polyphase filter and the quadrature LO, which is advantageous compared to the half-complex architecture. Thus, the design constraints in terms of image rejection are relaxed in the RF polyphase filter and the LO compared to the IF polyphase filter.

Summary of performances of numerous image-reject architectures reported above is given in table 1.

	Technology	*RF/IF (Hz)*	*IRR*	*IIP3*	*NF*	*Power consumption*
(Rudell et al., 1997)	0.6µm CMOS	1.9G / 200M	45dB	-7 dBm	14dB	92mW
(Carta et al., 2005)	BiCMOS	5 - 2.4 G/ 20M	33dB	-12 dBm	8.9dB	19mW
(Behbahani et al., 2001)	0.6µm CMOS	270M / 10M	60dB	-	-	62.7mW

	Technology	*RF/IF (Hz)*	*IRR*	*IIP3*	*NF*	*Power consumption*
(Crols & Steyaert, 1995)	0.7μm CMOS	900M /3M	46dB	27.9 dBm	24dB	500mW
(Wu & Razavi, 1998)	0.6μm CMOS	900M / 400M	40dB	-8 dBm	4.7dB	72mW
(Banu et al., 1997)	0.5μm BiCMOS	900M / 10.7M	50dB	-4.5 dBm	4.8dB	60mW
(Lee et al., 1998)	0.8μm CMOS	1G/ 100M	29dB	0.6 dBm	19dB	108mW
(Behbahani et al., 1999)	0.6μm CMOS	270M/ 10M	58.5 dB	-8 dBm	6.1dB	33mW
(Samavati et al., 2001)	0.24μm CMOS	5.2G	53dB	-7dBm	7.3dB	58.8mW
(Meng et al., 2005)	GaInP/ GaAs HBT	5.2G / 30M	40dB	-10dBm	-	150mW
(Wu & Chou, 2003)	0.18μm CMOS	5G / 20M	50.6dB	-13dBm	8.5dB	22.4mW
(Kim & Lee, 2006)	0.18μm CMOS	5.25G/1G	40dB	-8dBm	7.9dB	57.6mW
(Razavi, 2001)	0.25μm CMOS	5.25G/2.6G	62dB	-15dBm	6.4dB	29mW
(Lee et al., 2002)	0.25μm CMOS	5.25G/ 300M	51dB	-7dBm	7.2dB	21.6mW
(Chou & Wu, 2005)	0.25μm CMOS	6M - 30M	48dB	-8dBm	-	11mW

Table 1. Circuit performances using the Weaver and double quadrature conversion architectures

2.2 Complex polyphase filters

A Hilbert filter responds to the complex representation of a signal and is based on a shift transform, $s \mapsto (s + j\omega_0)$ (Khvedelidze, 2001). It translates the poles and transforms the lowpass response into a bandpass response centered at $\omega=\omega_0$, while preserving both amplitude and phase characteristics. Thus, owing to its asymmetric response to positive and negative frequencies, such a filter may be synthesized to suppress the image and pass the desired frequency; as the case of polyphase filters (Chou & Wu, 2005).

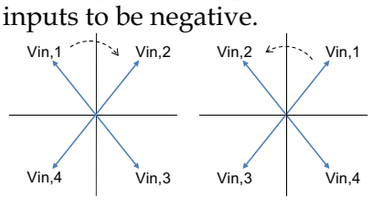
Invented by Gingell in 1971, polyphase filters were used to generate of quadrature signals in audio applications and were implemented first using discrete components (Gingell, 1971). This work has many limitations since working on such low frequency audio domain does not consider the influences of parasitic resistors and capacitors, moreover, components mismatch was not analyzed in the discrete components implementation (Tetsuo, 1995). Integrated PPFs were rediscovered in 1994 as an efficient RF quadrature generation technique in CMOS technology (Steyaert & Crols, 1994). The design of integrated CMOS PPF faces many challenges, so that many researches aim to analyze the sensitivity of the RF CMOS PPF in RF integrated transceivers (Galal & Tawfik, 1999) and their application in image rejection. This analysis allows understanding the PPF behavior, but it remains too theoretical for designers to get quantitative results about influences of process and mismatch variations on PPF performances.

A polyphase signal is a set of two or more vectors having the same frequency but different in phase (Galal et al, 2000). If its vectors have the same magnitude and are equally spaced in phase, it is considered symmetric. Hence, a symmetric two-phase signal consists of two vectors of equal magnitudes with the same frequency and being separated in phase by 180°. The phase order of the signal vectors determines the polarity of the polyphase signal sequence, i.e. a positive sequence has a clockwise phase order, while a negative sequence has an anticlockwise phase order. This introduces the concept of negative and positive frequencies (Fig.5). It should be noted that the phase order is different from the direction of rotation because all sequences, whether positive or negative, consist of vectors rotating anticlockwise. Since PPF networks have asymmetric responses to inputs of opposite polarities, they were described as *asymmetric* (Tetsuo, 1995).

The study of the PPF response can be performed by the way of vector analysis (Galal & Tawfik, 1999). Since the PPF phases are symmetric, the chain matrix of a single phase represents the chain matrix of the network. The PPF output is considered as the sum of the outputs cascaded by each symmetric input alone thanks to linear superposition rules. Fig.6 shows the structure of one phase generalized PPF, where admittance Y1 is connected between the input and the corresponding output, and Y2 is skewed between the input and output of adjacent phases. The chain matrix of a single phase can be written as (Galal & Tawfik, 1999)

$$\begin{bmatrix} Vin,k \\ Iin,k \end{bmatrix} = \frac{1}{Y1+e^{j\theta}Y2} \begin{bmatrix} Y1+Y2 & 1 \\ 2.Y1.Y2(1-cos\theta) & Y1+Y2 \end{bmatrix} \begin{bmatrix} Vout,k \\ Iout,k \end{bmatrix} \quad (4)$$

where θ represents the relative phase difference between V_{in} and the neighboring inputs, which in turn determines the polarity of the inputs. If θ<0, V_{in} will be leading $e^{j\theta}V_{in}$ in phase, which causes the inputs to be positive. On the other hand, if θ>0, V_{in} will be lagging, thus causing the inputs to be negative.



(a) (b)

Fig. 5. Two polyphase signals has a positive phase sequence (a) and a negative phase sequence (b)

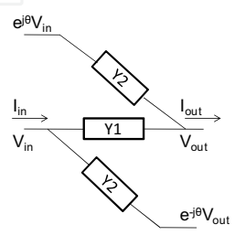


Fig. 6. A single phase of a generalized PPF network

Resistance-capacitance (RC) polyphase networks are a special case of sequence asymmetric polyphase networks. They represent a passive implementation of polyphase filters which makes them attractive for integrated high-frequency and low-power applications. The structure of a four-phase RC polyphase filter network, which composes one stage, is shown in Fig.7. One stage of an RC PPF contributes to one pole frequency, called a *notch*, around which the image is attenuated. It can be derived as

$$f_p = {}^{1}/_{2\pi RC} \tag{5}$$

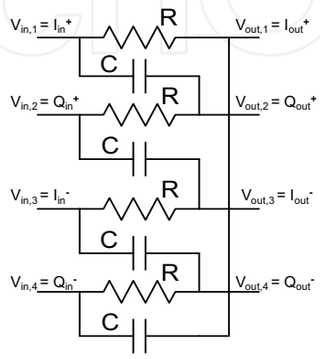


Fig. 7. One "four-phase" RC polyphase filter stage

3. Passive Polyphase Filter (PPF) Design

3.1 Case of a single-stage PPF

Let us now express the transfer function H(ω) of the PPF. Since the PPF is a complex filter, its transfer response can be represented as

$$H(\omega) = H_1(\omega) + j.H_2(\omega) \tag{6}$$

where $H_1(\omega)$ and $H_2(\omega)$ are the real and imaginary parts of the transfer function respectively. Let us note H(ω) the transfer function for any phase in a positive sequence, while H(-ω) that of negative one. Since complex polyphase filters discriminate positive and negative sequences, H(ω) ≠ H(-ω).

In the case of four-phase RC PPF shown in Fig.7, and substituting in (4) Y1, Y2 and θ for 1/R, sC and ±π/2 respectively, the open-circuit ($I_{out,k}$=0) voltage transfer function in a positive sequence can be written such as

$$H(\omega) = \frac{V_{out,k}}{V_{in,k}} = \frac{\omega_p - \omega}{\omega_p + j\omega} = A\frac{1 - \omega RC}{1 + j\omega RC} \tag{7}$$

while in a negative sequence, we yield

$$H(-\omega) = \frac{V_{out,k}}{V_{in,k}} = \frac{\omega_p + \omega}{\omega_p + j\omega} = A\frac{1 + \omega RC}{1 + j\omega RC} \tag{8}$$

where A is an amplification factor and ω_p is the pole frequency. The transfer curves of $|H(f)|_{dB}$ and $|H(-f)|_{dB}$ are shown in Fig.8 for f_p =2.4GHz. Note that the desired signal with positive frequency falls in the filter's passband while the image signal at negative frequency is attenuated. The IRR, previously defined in (2), can be expressed as following

$$IRR(\omega) = \frac{|H(\omega)|}{|H(-\omega)|} = \frac{\omega_p - \omega}{\omega_p + \omega} \tag{9}$$

Thus, according to (9), we can deduce that IRR (f_p) = 0 if $H_1(\omega)$ and $H_2(\omega)$ are perfectly matched. Nevertheless, this theoretical value is difficult to achieve due to intrinsic mismatch of the components and the non uniformity of the connection lines.
Now, let us generalize the transfer function considering gain and pole mismatches which can be expressed as

$$H_m(s) = \frac{A\omega_p\left(1-\frac{\Delta A}{2A}\right)\left(1-\frac{\Delta\omega_p}{2\omega_p}\right)}{s+\omega_p\left(1-\frac{\Delta\omega_p}{2\omega_p}\right)} + j\frac{A\left(1+\frac{\Delta A}{2A}\right)s}{s+\omega_p(1+\frac{\Delta\omega_p}{2\omega_p})} \quad (10)$$

where ΔA and $\Delta\omega_p$ are the mismatch quantities of the gain and the pole frequency, respectively.
Analytical modeling has been performed in order to quantify the impact of the mismatch on the IRR degradation and the notch frequency drift. Results are summarized in table 2 for some typical values of ΔA and $\Delta\omega_p$. The same effect has been reported on Fig.8. It can be noted (table 2) that pole mismatch of 2% leads to an IRR degradation higher than 20dB and gain mismatch greater than 10% cause bandwidth degradation higher than 200MHz. It depicts that the gain mismatch ΔA shifts the frequency, while the pole frequency mismatch $\Delta\omega_p$ changes the IRR.

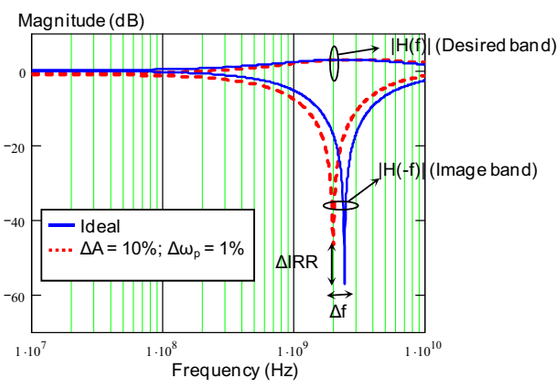


Fig. 8. Transfer responses of a PPF for a positive (|H(f)|) and negative (|H(-f)|) phase sequences

$\Delta\omega_p$(%)	ΔA (%)	Δf (MHz)	ΔIRR (dB)
1	20	500	10
1	10	200	10
1	5	50	10
2	5	50	20
3	5	50	23

Table 2. Gain and pole mismatch influence on the notch frequency and the IRR

This mismatch results essentially from components imbalance. Thus, considering a single RC PPF section, if the absolute values of R and C deviate such as R+ΔR and C+ΔC, the pole frequency differ from 1/(2πRC) and the residual voltage is given by

$$\delta_A = \frac{1 - \omega.\tau(1+\delta_\tau)}{\sqrt{1+(\omega.\tau(1+\delta_\tau))^2}} \tag{11}$$

where δ_τ is the time constant fractional deviation (Behbahani et al, 2001).
Since in the vicinity of the pole frequency, $\omega.\tau = 1$, we have

$$\delta_A \simeq \frac{-\delta_\tau}{\sqrt{2}} \tag{12}$$

Further, the matching of a parameter M is generally defined as a standard deviation of Gaussian distribution of relative ΔM/M between identically designed paired devices. Then, the IRR with consideration of R and C mismatches can be expressed in a normalized RMS quantity (Behbahani et al, 2001) and then given by

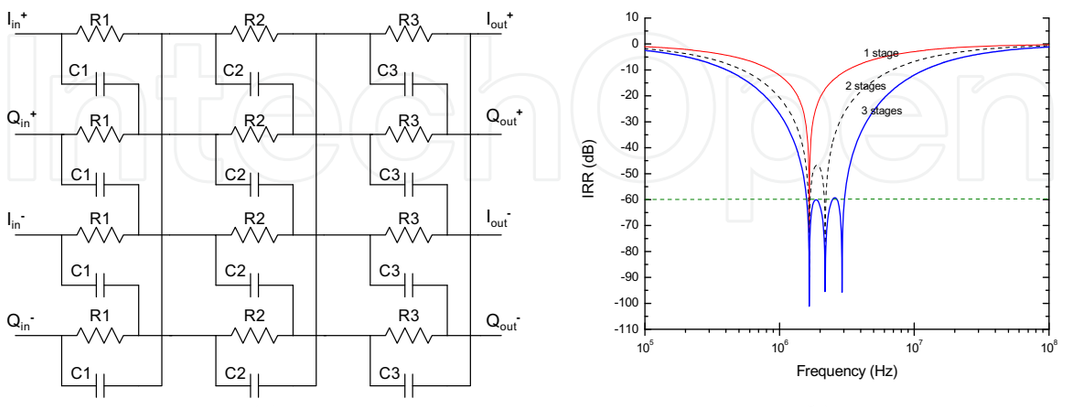
$$\frac{\sigma(image\ Out)}{Desired\ Out} = \frac{\sigma_\tau}{4} = \frac{1}{4}\sqrt{\left(\frac{\sigma_R}{R}\right)^2 + \left(\frac{\sigma_C}{C}\right)^2} \tag{13}$$

3.2 Case of a multi-stage PPF

Since a one-stage PPF suppresses the image only around the notch frequency, it supplies a narrow band rejection. By cascading several stages with different notches, a wide bandwidth can be achieved. These notches have to be placed at equal frequency ratios (Fang et al, 2005); i.e

$$\alpha = {f_{p2}}/{f_{p1}} = {f_{p3}}/{f_{p2}}, etc. \tag{14}$$

Figure 9 depicts the topology of cascaded stages of RC polyphase filter and their correspondent frequency responses. It shows the image rejection through multi-stage-RC PPFs, in which the notches are logarithmically spaced for equiripple response. The bandwidth to be covered and the desirable image rejection amount fix the number of stages needed for the polyphase filter.



(a) (b)

Fig. 9. A three-stage RC PPF topology (a); Cascade frequency responses of one-, two- and three-stage PPFs

In spite of its broadband, a multistage PPF presents gain losses because each stage loads the previous one. Thus, additional buffers should be included between the stages for loss compensation or impedance adaptation. The cost remains in the increased power consumption due to buffers. In addition, the pole location of the original RC PPF could be changed. Other structures of multistage RC polyphase filters are proposed in (Komoriyama et al, 2007) to overcome the problem of buffering and to ensure minimal element value-spread and equal-ripple gain.
In the case of a two-stage RC PPF, the transfer function can be obtained by multiplying the chain matrices, as given in (4), of each stage and evaluating the open-circuit ($I_{out,k}$=0) complex transfer function. We yield

$$H(\omega) = \frac{(1-\omega R_1 C_1)(1-\omega R_2 C_2)}{1-\omega^2(R_1 C_1 R_2 C_2) + j\omega(R_1 C_1 + R_2 C_2 + 2R_1 C_2)} \tag{15}$$

In the case of a three-stage RC PPF, the transfer function is given by

$$H(\omega) = \frac{(1-\omega R_1 C_1)(1-\omega R_2 C_2)(1-\omega R_3 C_3)}{D(\omega)} \tag{16}$$

where $D(\omega) = 1-\omega^2(R_1R_2C_1C_2 + R_1R_3C_1C_3 + R_2R_3C_2C_3 + 2R_1R_3C_2C_3 + 2R_1R_2C_1C_3 + 2R_1R_2C_2C_3) + j\omega(R_1C_1 + R_2C_2 + R_3C_3 + 2R_1C_2 + 2R_1C_3 + 2R_2C_3) - j\omega^3(R_1R_2R_3C_1C_2C_3)$

The resultant IRR_N of N cascaded stages can be derived by multiplying the IRR of each one-stage polyphase filter as

$$IRR_N(\omega) = \prod_{n=1}^{N} IRR_n(\omega) \tag{17}$$

4. Active Polyphase Filters

In CMOS wireless receiver design, multi-stage polyphase filters are widely used. One solution consists on substituting the passive resistive parts of the filter by active one, using transconductances (Behbahani et al, 2002; Andreani et al, 2000). This topology behaves in the same way as the regular structure if gm equals to 1/R with ideal source and load. The high input impedance of the transconductance reduces the loading of the preceding stage. The active polyphase filter combines isolation, gain and small chip area.
Many realizations of active resistor are based on the use of inverter-type transconductor, originally proposed by *Nauta* (Andreani & Mattison, 2002). The transconductor circuit proposed in (Behbahani et al, 2000) has many advantages including good linearity, low-noise, high-frequency capability and low-voltage; but at the same time it suffers from common-mode instability. Further RC-active polyphase filter implementations are based on the use of second generation current conveyors (CCIIs) (Ün (a), 2004) or on the use of conventional operational amplifiers (OPAMPs) and RC components (Ün (b), 2004). However, in high-frequency operation, opamp RC filters design is problematic because of the required gain-bandwidth, the power consumption and the swing limitations. Thus, the OPAMP can be replaced by an operational transconductance amplifier (OTA) (Tsividis, 1994). Even so, problems due to OTAs design with adequate gain and bandwidth in low-voltage CMOS process are preserved. Hence, techniques of feedback and feedforward

common-mode compensation are used with such structures allowing high dc gain and good phase margin even in low-voltage CMOS applications (Harrison, 2002; Thandri & Silva-Martinez, 2003). Another structure of active RC PPF proposed in (Tillman & Sjoland, 2005) is based on CMOS inverters, with dc feedback to stabilize the bias point. It is used to generate quadrature signals and combines high gain and good quadrature performance (quadrature error<0.8° in the tuning range [9.14, 10.58] GHz).
Furthermore, (Chian et al, 2007) proposes a novel design idea to implement polyphase filters based on replacing passive components by MOSFETs. This active device gives the same functions as the conventional passive polyphase filter with a significant reduction of the chip area; but it includes great effects of nonlinearity and parasitic components, making it difficult to handle in the experimental plan. They can be realized also by using gyrators, but, it is difficult to realize a gyrator using practical passive elements because of its reciprocity. Other complex filters are reported as part of the receiver design and, therefore, details about the filter performance were not given (Van Zeijl et al, 2002).
The active polyphase filter solutions, comparing to the passive ones, have smaller area, making them more adequate for low and intermediate frequency applications, but have at the same time more power consumption and lower linearity. Owing to the recent improvements on CMOS technology, passive components present better quality, in particular in the high frequency domain. Then, it is more convenient to use PPFs in the RF part, with certainly a special attention to the parasitics and the matching. The electrical model used in EDA (CAO) tools is no more sufficient or not enough accurate to underline the parasitic contributions as well as mismatch effects while designing the RF PPFs. Therefore, it is necessary to perform a PPF modeling to achieve the suitable performances of the future wireless communication standards.

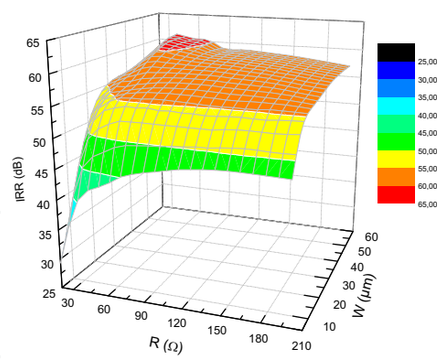
5. Mismatch analysis

While working with PPF, the image rejection depends on the ability of the designer to achieve sufficient matching on the resistors and capacitors which comes from many causes (Hastings, 2006) such as microscopic fluctuations in dimensions, process biases, diffusion interactions, thermoelectric effects, etc. The requirements from component matching are contradictory to that of minimization of noise coupling, signal loss and chip area. It is known from experimental studies (McNutt et al, 1994) that the variance of adjacent resistors and capacitors is inversely proportional to their area. Consequently, large component area is required to achieve high IRR, but, in the same time, large area increases the parasitic capacitances value of filter components. In fact, achieving high IRR with polyphase filter results from an optimal sizing of the filter components. In other terms, tradeoff between the chip area and IRR must to be considered. Furthermore, back-end design methodology including layout consideration is mandatory in order to optimize CMOS PPF.
Different simulations related to image rejection have been done to verify multi-stage RF PPFs for a given communication standard. In these experiments, let us consider image rejection in a low-IF receiver with RF PPFs working around 2.4GHz. First, the characteristics of the different stages and principally their notches frequencies are chosen. Once the notches frequencies are determined, values of resistors and capacitors can be selected. Small signal simulations with *SpectreRF* (*Cadence*®) have been considered to focus on the effect of the component variations on the IRR and consequently to calibrate judiciously the optimal sizes

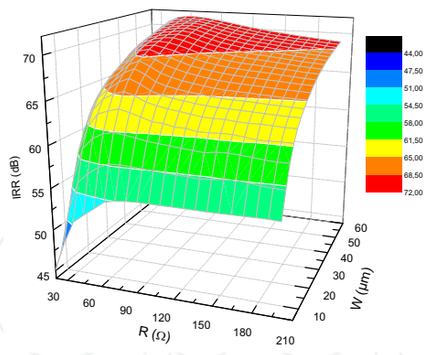
and values of resistors composing the filter allowing the required IRR. To investigate this further, Fig.10 shows the simulated IRR results for different polyphase networks with mismatch consideration. The IRR is illustrated in three-dimensional plot as a function of the resistor's electrical value (R) and resistor size, which for the current study corresponds to the width (W). In the X-axis, the parameter R is used to calibrate the first stage of the polyphase filter. The resistor values of the other stages are set to a fixed pole ratio α, as shown in (14). The capacitors are chosen to give the right pole frequency.

These three-dimensional plots show first that multiplying the number of stages gives a higher IRR. For example for the couple (R, W) equal to (70Ω, 10µm), the IRR increases from 52dB with three-stage polyphase design (Fig.10(a)), to 60dB with four stages (Fig.10(b)) and reaches 65dB with five stages (Fig.10(c)). However, having many stages in the polyphase network conducts to a growth of the components number and increases the silicon area, the power loss and the parasitic capacitances. Hence, according to the costumer need, designers should make a compromise between achieving a polyphase filter with high image rejection and low area and low silicon area cost.

Furthermore, Fig.10 illustrates that a high IRR is achieved if the value and the size of the resistor converge to the optimal values on each multi-stage polyphase filter. For about the different filter configurations, it shows that the IRR variation versus R corresponding to a given configuration is quasi-linear. For instance for a five-stage PPF, the IRR changes from 65dB, to 68dB and 70dB for resistor's width of 10µm, 20µm and 40µm respectively (Fig.10(c)). In this case, it can be noted that a gain of only 5dB in the IRR produces an expansion of the resistor size by almost 400% confirming the existence of an optimal component sizing for a specified IRR with each polyphase filter configuration. The possible reason is that large component area yields better matching on the circuit and presents optimal parasitic capacitances effect.



(a)



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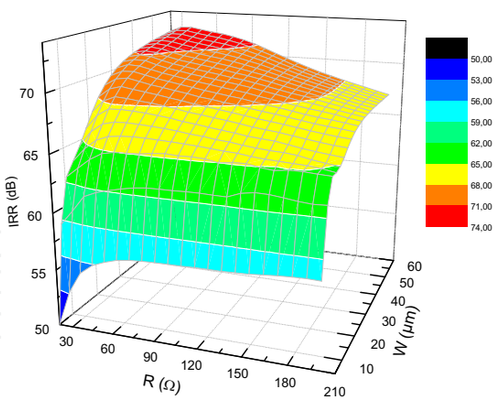
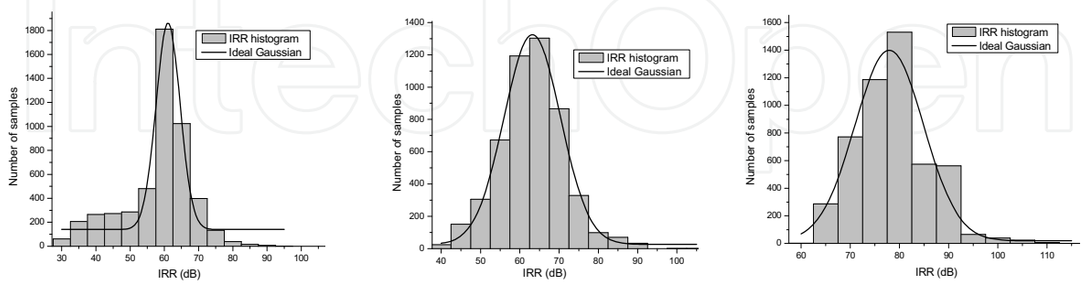


(c)

Fig. 10. IRR variation of (a) three, (b) four, and (c) five PPF versus resistor's sizes and values

A statistical representation is suitable to characterize the processes happening in probabilistic ways. In statistical simulations, sequences of random numbers with a certain probability distribution function are used to model the stochastic process. Usually, many statistical simulations runs are conducted and averaged to reach good accuracy of the simulation results. Process tolerances and component mismatch in integrated circuits are consequences of stochastic processes within a certain range, and they are usually available in CMOS process files derived by elaborate measurements. It is known that both process tolerances and component mismatch have truncated Gaussian probability distribution functions (Spence & Soin, 1997). In our application, Monte Carlo simulation can be applied to verify the statistical nature of the IRR with certain process tolerances and a resultant component mismatch, and to check the probability distribution of the gain mismatch. After optimal sizing and value calibrations of the PPF components as shown previously, three, four and five stages are simulated. The analysis concerns the process and mismatch variations of the PPF component corners (Polysilicon resistors and MIM (Metal-Insulator-Metal) capacitors for the current study) before parasitics extraction on the frequency band [2, 3] GHz. The Monte Carlo simulation results are expressed as frequency of occurrence histogram (5050 samples of RF PPFs) for different intervals of the IRR and shown in Fig. 11.



(a) (b) (c)

Fig. 11. Monte Carlo simulation results of (a) three, (b) four and (c) five stage RF PPF: IRR histogram (process and mismatch variations)

The impact of process and mismatch variations on the PPF response is summarized in table 3. It illustrates the worst case and mean value of IRR, as well as the notch position drift and the IRR distribution between 50dB and 90dB.

PPF stages number	*Mean value of the IRR*	*Worst case IRR*	*Notch drift*	*Standard deviation σ*	*IRR distribution between 50dB and 90dB*
3	62dB	51dB	405MHz	9.11	85%
4	72dB	57dB	306MHz	10.05	95%
5	87dB	64dB	317MHz	11.95	97%

Table 3. Monte Carlo simulation results of multi-stage RF PPFs: mean value and worst case IRR, notch position drift and IRR distribution between 50dB and 90dB

The obtained results confirm that increasing the stages number increases the mean value of the IRR on the desired bandwidth. It can be noted that the higher is the PPF stages number, the lower is the PPF immunity to mismatch effects, given that the distribution becomes wider and the standard deviation σ increases from 9.11 to 10.05 and 11.95 for three-stage, four-stage and five-stage RF PPFs respectively. This is due to the components and connections growth in the design, inducing, at the same time, an expansion of its area.
Let us consider a unit surface S_0 of a one-stage RF PPF. Since in the RF domain the size of our PPF components is almost identical, we can suppose that an n-stage PPF has a surface of $n.S_0$. Thus, a compromise can be made while designing PPFs depending on the system specifications. For example, a 60dB image rejection will cost $3.S_0$ with a standard deviation of 9, while a roughly 85dB image rejection will cost $5.S_0$ with a standard deviation of 12.

6. Parasitics analysis and line modeling

Since the implementation of RC polyphase filter on integrated circuit engenders parasitic capacitance to the substrate and at the output nodes, special attention must to be paid on the parasitic capacitance and loading capacitance effects. In Fig.12 we model a simplified equivalent circuit of a two-stage RC PPF with parasitic capacitance to substrate (Cp1, Cp2, Cp3) and load capacitance (a part of Cp3).

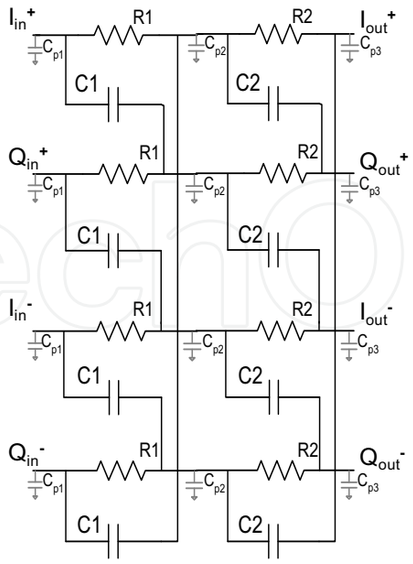


Fig. 12. Equivalent circuit of the two-stage RC PPF with parasitic capacitance

In this case, the transfer functions of one-stage and two-stage RC polyphase filter are given respectively as follows

$$H_{p1}(j\omega) = \frac{1 - \omega R_1 C_1}{1 + \omega R_1 (C_1 + C_{p2})} \tag{18}$$

$$H_{p2}(j\omega) = \frac{(1 - \omega R_1 C_1)(1 - \omega R_2 C_2)}{1 - \omega^2 R_1 R_2 \left[C_1 C_2 + C_1 C_{p2} + C_2 (C_{p2+} C_{p3}) + C_{p2} C_{p3}\right] + j\omega \left[R_1 (C_1 + 2C_2 + C_{p2} + C_{p3}) + R_2 (C_2 + C_{p3})\right]} \tag{19}$$

It can be noted from (18) and (19) that the parasitic capacitances do not change the zero positions $1/2\pi R_1 C_1$ and $1/2\pi R_2 C_2$ of $H_{p1}(j\omega)$ and $H_{p2}(j\omega)$. Simulation results of frequency response including parasitic capacitances depict that the gain drops for high frequency domain when the parasitic capacitance values increase (Yamaguchi et al, 2003).

Furthermore, properly arranging the components and optimally sizing the connections are necessary to guarantee an equilibrated parasitic repartition in the circuit, which can conserve the symmetrical structure of passive polyphase filter. The major loss and parasitic capacitance contributions in connections are considered in order to obtain better filter performance. In fact, loss in a conductor can be generally described by the following equation

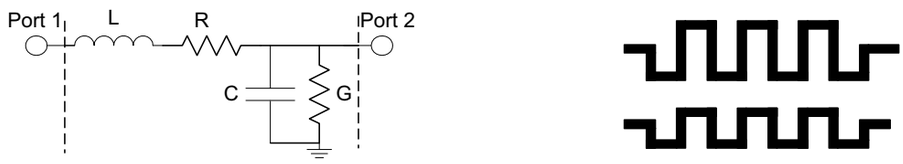
$$R = \frac{\rho_{film} . L}{t . W} \tag{20}$$

where ρ_{film} is the thin film resistivity of the metal, t is the metal thickness, and L and W are the trace length and width, respectively. Therefore, loss can be minimized by using metals with very low resistivity, increasing the cross sectional area of the trace ($t.W$), or reducing the overall trace length. Besides, the metal of connection is isolated from the semiconductor substrate (typically at ground potential) by one or more dielectric layers used to separate interconnect layers (inter-metal dielectrics). This creates a parasitic shunt capacitor that can be approximated by the following equation

$$C = \frac{A.\varepsilon}{d} \tag{21}$$

where A is the total area of the metal traces, ε is the permittivity, and d is the thickness of the dielectric. The parasitic capacitance decreases with high metals levels, but at the same time this will increase the parasitic resistance because of stacking the different "via" resistivities. Hence, designers must balance both the parasitic shunt capacitance and conductor loss when selecting a conductor dimensions and metals levels.

Characterization and modeling of the interconnection lines have been performed to improve their properties. The equivalent network line model between two ports used in this study is shown in Fig.13(a). First, the line parameters have been extracted with electromagnetic simulations (*HFSS™*). Then, the correspondent line models have been specified and inserted inside the polyphase filter design at the main sensitive points and simulated with the *Agilent ADS®* tool. Calibration of the additional parasitics allows their allocation symmetrically along the design, since their total elimination is not possible. This study has demonstrated that lines with different shapes give the same filter response (IRR and bandwidth) provided that the interconnect lengths in respectively I/Q paths are equalized. It is caused by the fact that this will balance the parasitic interconnect resistance in each branch. For example, serpentine and bus shapes could be used simultaneously for the parallel interconnections. By adjusting the height of serpentine, the wire length in the branches of the PPF may be equalized while keeping the same number of corners (Fig 13(b)).



(a) (b)

Fig. 13. (a) Equivalent network line model between different levels of interconnect. (b) Considerations of interconnect to balance parasitics in polyphase filter branches

Besides, the inaccuracy of resistors and capacitors, due to Si substrate parasitic effect, causes quadrature phase imbalance. To overcome this problem it is possible to make the polyphase filter tunable so as to compensate the phase imbalance. The tunable phase can be used to improve image rejection or moderate I/Q phase error in direct conversion or low-IF receivers. For instance, varactor-based tunable polyphase filters on Si have been implemented at 5GHz (Sanderson et al, 2004). Another technique to solve RC inaccuracy of PPF is to use InGa/GaAs heterojunction bipolar transistor which has a very good frequency response but which remains expensive (Meng et al, 2005). In addition, in the RF front-end receiver, the input large parasitic capacitances of the following double quadrature mixer degrade the loss of the RF polyphase filter. To overcome this problem, on-chip spiral inductors are inserted at the output of the RF PPF in (Kim & Lee, 2006) and then tune out the total input parasitic capacitances of the double quadrature mixer.

In our design, a new polyphase filter implementation (shown in Fig.14) is proposed to balance the bandwidth variation due to mismatches in a symmetrical structure. It consists on the RC basic passive polyphase network, adding up active resistors implemented with MOS transistors. It is known that the R_{on} of the MOS transistor is function of its dimensions

and of the grid voltage (VG). Thus, with an external tuning of VG, the value of R_{on}, and then the PPF resistor value and the notches, can be adjusted independently. Consequently, that gives a tuning characteristic to the filter bandwidth, and can be applied to synthesize multi-standards application filters. The MOS transistor dimensions are chosen to have the adequate calibration of the bandwidth dispersion. Using these MOS active resistors possibly adds nonlinearity to the PPF design, and then other active resistor realizations, such as parallel-MOS and double-MOS differential resistor, with better linearity performance, have been proposed (Allen & Holberg, 2002).

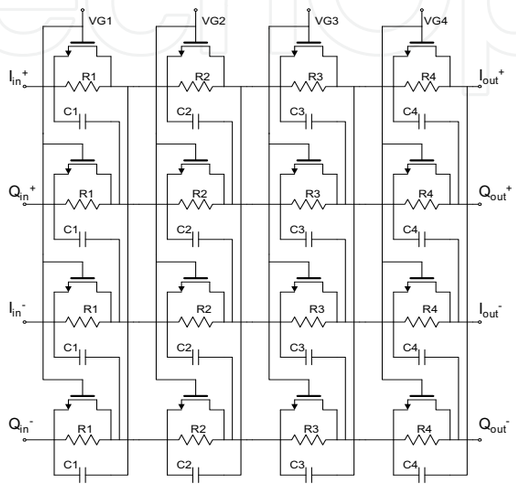


Fig. 14. Four-stage voltage tunable RC polyphase filter structure

7. Layout techniques

In addition, while components with large areas decrease the impact of mismatch, the parasitic capacitance and resistance can have a much larger effect on output imbalance. Minimization of these parasitics requires careful attention to layout symmetry. The parasitic extraction procedure, performed with the *Star-RCXT* tool of *Synopsys*, shows that most extracted parasitics are set in the interconnection network. Interconnects present electrical losses that need to be taken into account during layout and then during performances estimation. It is clear that, on the circuit, the inner traces see parasitic capacitance from the left and right, while the outer traces only see parasitic capacitance from one side. Hence, weaving the traces gives each path the same total distance spent as both an inner and an outer trace. To equalize the parasitic effect of overlapping traces, a grid of vertical and horizontal running interconnects has been laid out. Moreover, two parallel signal lines are placed far enough apart so that the interline capacitance is negligible.

Furthermore, a judicious choice of metal level and interconnection drawing is necessary. In fact, using high level of metallization engenders low parasitic capacitance but gives high parasitic resistance. Thus, depending on the device sensibility and on the required matched components, the metal level is chosen. For example, in low-loss applications, the metal 6 is the most suitable (in 0.13µm CMOS technology) since it is the thickest one and has less capacitance. The number of "vias" used for interconnects is also significant in leading to equilibrated parasitics, especially in the case of RF passive polyphase filters. These vias give

high contact resistance that can be almost equal to the filter resistance. Table 4 presents some extraction results of a line connection between a resistor and a capacitor having different metal levels with different vias number. It shows that increasing the number of vias does not change the parasitic capacitance, but decreases the parasitic resistance. It is due to putting the contact resistance of each via in parallel and then lowering the equivalent resistance. Therefore, connections in the radio frequency PPF have to use great number of vias to minimize their parasitic effect.

Metal level of the line	*Via number*	*Parasitic capacitance (fF)*	*Parasitic Resistance (Ω)*
Metal 2	1	14.5	19.11
	2	14.54	11
	3	14.56	7
Metal 3	1	14.13	19.11
	2	14.15	13.49
	3	14.18	10.82

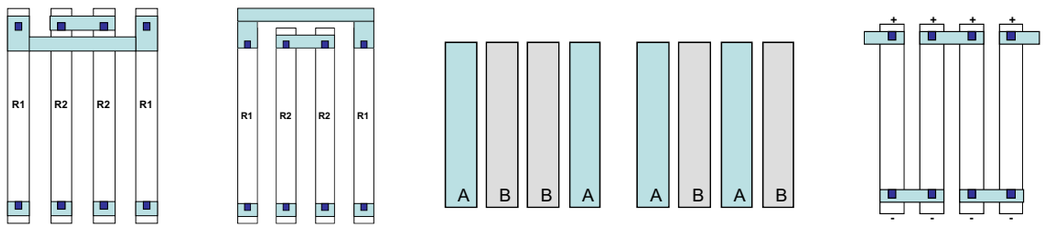
Table 4. Extraction results of a line connection (W=2.5-µm/L=5-µm) with different metal levels between a Polysilicon-resistor and a MIM-capacitor in 0.13µm CMOS technology

Total equilibrated interconnects drawing is hard to obtain in the case of PPF. However, owing to the symmetry of the PPF stages, the parasitic modelling and extraction procedures illustrate that ensuring the same drawings between I and Q paths is sufficient to guarantee same matching and same performances as in the case of an ideal structure (with same drawings for the four PPF paths), and then, that may loosen the constraints of design techniques.

In addition to designing a symmetrical circuit, further layout techniques have been used to assure highly matched devices, as shown below

- To reduce the sensitivity of the device to process biases, resistors are made same width and capacitors consider same area-to-periphery ratios.
- Dummy resistors are added to either border of an array of matched resistors to guarantee uniform etching. Dummies should be electrically connected to ground (or to other low-impedance node) to avoid electrostatic modulation and floating diffusions. Moreover, the metal overlapping the active area of resistors can lead to metallization-induced mismatches. Thus, the "folded-out" interconnection (Fig.15(a)) produces better matching than the "folded-in" interaction (Fig.15(b)).
- Stress has an impact upon silicon since it is piezoresistive. One of the most known techniques for reducing stress-induced mismatches is the *common-centroid layout*. It arranges segments of matched devices along one dimension. For example, if we consider two devices (A and B), each composed of two segments, the possible patterns are shown in Fig.15(c). The pattern ABBA has an axis of symmetry that divides it into two mirror-image halves (AB and BA). It requires dummies since segments of A occupy both ends of the array. The pattern ABAB, with interdigitated resistors, haven't common axis of symmetry and needs dummies as well as the ABBA pattern. Thus, the pattern ABAB lets stress-induced mismatches on devices and consequently it should be avoided (Hastings, 2006).

- Thermoelectric effects cannot be eliminated with the common-centroid layout in the case of an array of resistors, because they arise from differences in temperature between the ends of each resistor segment. The thermoelectric potentials of individual segments can be cancelled by reconnecting them as shown in Fig.15(d). The resistor should have an even number of segments, half connected in one direction and half connected in the other.
- Electrostatic interactions cause variations in resistors and capacitances. Thus, matched resistors with same values can belong to a common tank (or N-wells). If resistors have different values, they should be divided into segments of equal values, and each segment must reside in its own independently biased tank. In addition, wires that do not connect matched resistors should not cross them, because they may capacitively couple noise into the resistor and the electric field between the wire and the resistor can modulate the conductivity of the resistance material. The *electrostatic shielding* (or *Faraday shielding*) is a technique that can isolate a resistor from the influence of overlying leads and gives shielding against capacitive coupling (Hastings, 2006).
- To avoid electromigration between signals, I and Q paths are separated with a grounded bus.
- Size, orientation and temperature stress of MOS transistors influence their matching. A better matching is obtained when transistors are oriented along the same crystal axis in the same direction because of the stress-induced mobility variations. They should also be placed in close proximity even next to one another in order to facilitate common-centroid layout.



(a) (b) (c) (d)

Fig. 15. Resistor array interconnection in (a) "folded-in" and (b) "folded-out" styles. (c) Examples of common-centroid arrays. (d) Proper connection of resistor segments cancelling the thermoelectric

8. PPF Design methodology

As analyzed previously, component mismatch, process tolerances and parasitic effects must be considered in the design of CMOS PPFs to accomplish a robust design. We propose a design methodology dedicated to PPFs as shown in Fig.16. Such top-down design methodology is a structured approach to design PPFs operating from wide frequency range and which can satisfy high performances in terms of IRR (about 60dB) from wide frequency range (1MHz to 5GHz).

This PPF design methodology can be arranged into considerations first in the system requirements, then in the schematic design and next in the layout view. Thus, starting out from target specifications and constraints in terms of IRR, application bandwidth, cost and consumption, we can summarize the design flow as the guidelines below

- Accomplishing analytical calculations and modeling to quantify the component mismatch and parasitic elements effects and to focus on the resulting PPF response to phase and gain imbalances.
- Fixing the number of stages needed for the polyphase filter according to the bandwidth to be covered and the desirable image rejection amount.
- Equally placing the notches on the frequency domain with growing impedance while traversing the filter stages to lower losses and noise figure.

If the cascade filter loss is still too large, we move on changing the component type as well as calibrating its parameters, even as inserting inter-stage buffers to preserve signal dynamic range within the polyphase filter. After adjusting the losses into the PPF, we fulfill statistical simulations to longer analyze the component mismatch.

- Optimal sizing of the PPF components in terms of electrical value and dimensions. The matching quantities needed between resistors and capacitors determine the physical area of the filter.

If in the schematic simulation, the target specification cannot be met, we move on to the component resizing procedure and deduce the compliance with the required constraints. After completing the schematic design, we carry out the physical layout design.

- Modeling the interconnection lines and performing electromagnetic simulation to deduce their parameters; and then inserting them in the PPF design to maximize its immunity to the non idealities.
- Designing the layout taking into account the parasitic elements: the conductor loss of the interconnect metal creates parasitic resistance, and the dielectric between the traces and the substrate or between two overlapping traces creates parasitic capacitance. Layout which creates equal parasitics for each path through the polyphase is necessary to minimize the imbalance and maintain the symmetry.
- Using dummies around the matched components to reduce the boundary effects and on-chip shielding to isolate the PPF design from the unwanted substrate noise coupling. The electromigration is minimized with a ground separation between the I and Q signals. A judicious choice of the metal level and number of contacts or vias is also necessary.
- Post layout simulating the PPF with the extracted coefficients. In this extraction method, parasitics between neighboring components, wires and parasitics to the substrate are extracted. In this way, we can provide realistic simulation results before manufacturing the circuit.

If the target specifications required by the application are not yet satisfied, we go back to the parasitics minimization procedure and post-layout simulation (PLS) until assuring them. Then, we finish the design.

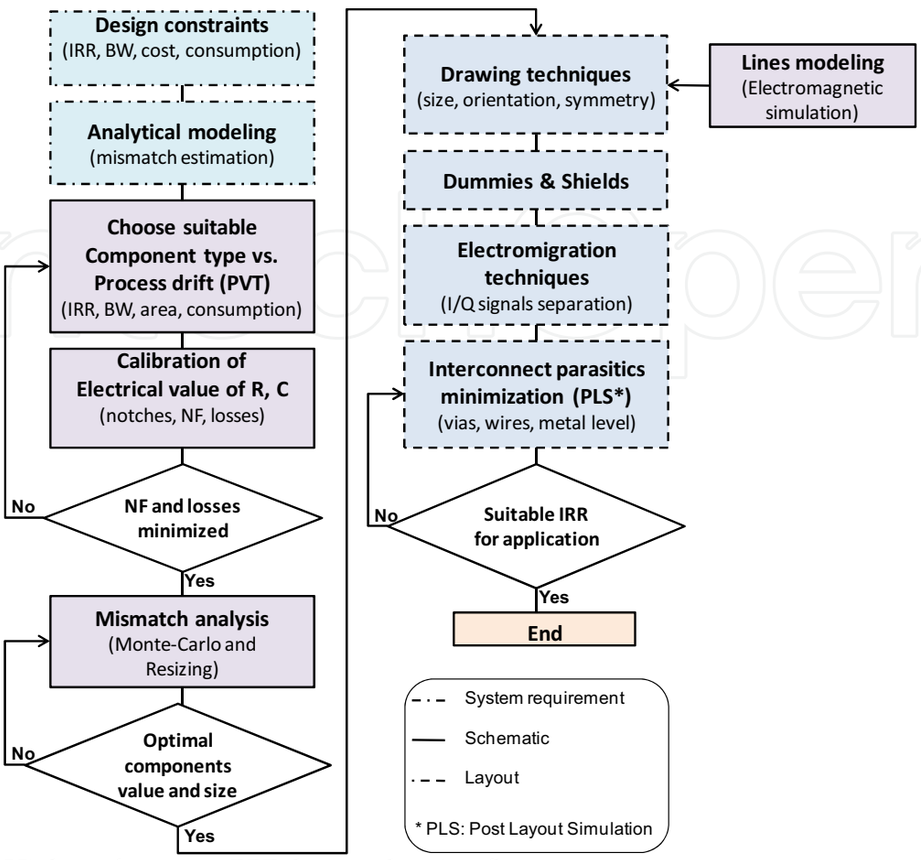


Fig. 16. High performance PPF design planning flow

9. PPF implementation

The proposed design methodology has been validated with some test-cases in full CMOS process. For instance, Fig.17 shows the layout of a four-stage RF tunable PPF (rf. Fig.14) designed to work around 5GHz, and fabricated in 0.13-µm CMOS technology. It occupies a die area of 310 x 83 µm² without test pads.

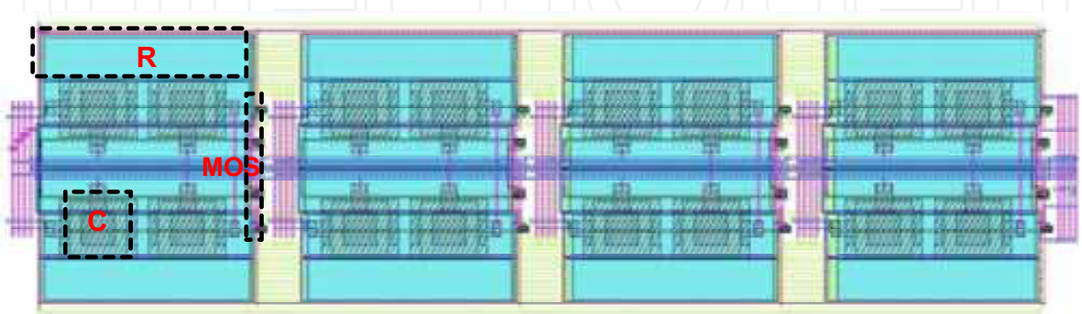


Fig. 17. Layout of the 5GHz four-stage tunable PPF: 310 x 83 µm² without test pads

The frequency response of the implemented 5GHz tunable PPF is depicted in Fig.18. It shows that the variation of the control grid voltage of MOS resistors enables the tuning of the PPF bandwidth by 1GHz while conserving an IRR almost steady around 75dB. Then, this proposed tuning characteristic can be applied to multi-standard applications, or used to compensate for the bandwidth drift due to mismatches.

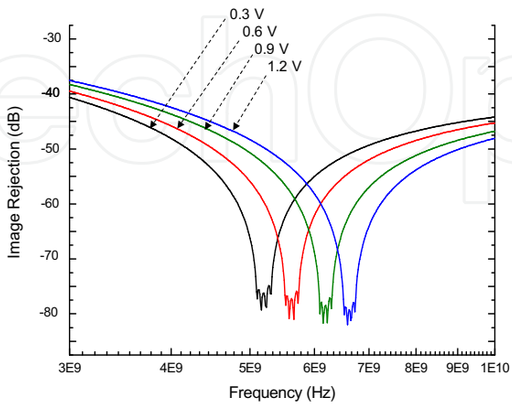


Fig. 18. Frequency responses of the 5GHz tunable polyphase filters using different control grid voltages

A chip photo of the fabricated chip is shown in Fig.19. It occupies 815 x 319 µm² with test pads. On-chip polysilicon resistors have been added to recombine the four outputs of the PPF in order to avoid the inaccuracy of the external hybrid couplers and to facilitate the measurement procedure. Thus, a differential output is obtained and can be measured easily with active probes.

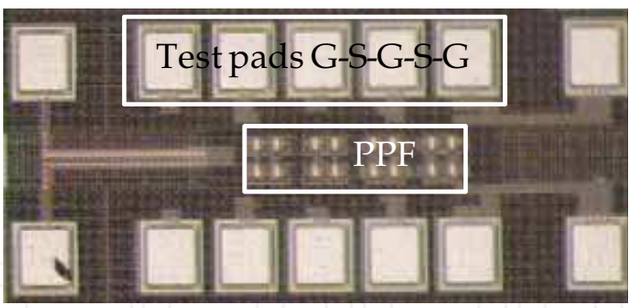


Fig. 19. Die micrograph of the fabricated PPF test chip in 0.13-µm CMOS technology

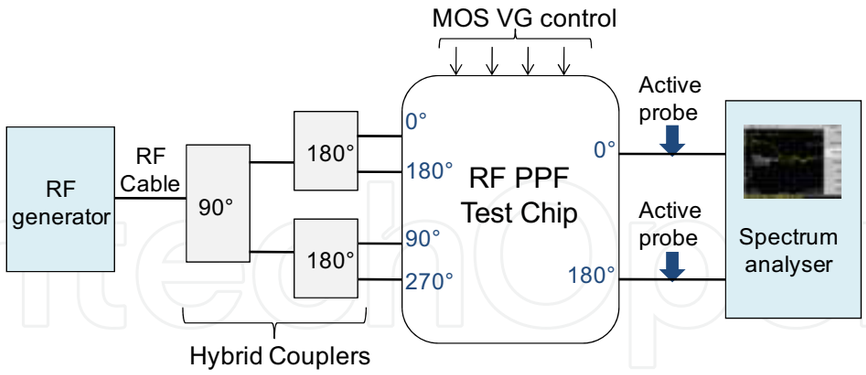


Fig. 20. Diagram of the PPF measurement setup

A diagram of the measurement setup for test of the CMOS PPF is illustrated in Fig.20. On-wafer RF measurements can be performed since balanced G-S-G-S-G pads (*G* for ground and *S* for signal) are used. The four input phases of the filter are generated by using a signal generator and wideband passive hybrid couplers. The measurement procedure is being processed to validate the obtained simulation results.

10. Conclusion

Wireless communication bands and services are proliferating, resulting in a great development of standards and in an enhanced need for integrated circuits. In this paper, it is demonstrated that techniques for image rejection have been constantly evolving in recent years because of this tremendous success of wireless products. Among the various techniques, the polyphase filters might become the choice for future image rejection scheme, thanks to its promising performances and to the semiconductor process advances. An analytical approach of RC polyphase filters as well as a study of components mismatch and non-ideality impact on the IRR degradation have been presented in this paper. That leads us to propose a design methodology dedicated to passive polyphase filters (PPFs), taking into account optimum component sizing, lines modeling and layout symmetry and matching. This method has been validated with some test-cases in full CMOS technology and allows attaining high image rejection (about 60dB) from wide frequency range (1MHz to 5GHz).
In addition, the wireless services have different carrier frequencies, channel bandwidths, modulation schemes, data rates, etc., which motivates the industry to look for multi-standard and multi-band devices. In this paper, a tunable polyphase filter structure has been proposed, which can be applied to synthesize multi-standard application filters. This tuning characteristic can be also used to compensate for the bandwidth drift due to mismatches.

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Mobile and wireless communications applications have a clear impact on improving the humanity wellbeing. From cell phones to wireless internet to home and office devices, most of the applications are converted from wired into wireless communication. Smart and advanced wireless communication environments represent the future technology and evolutionary development step in homes, hospitals, industrial, vehicular and transportation systems. A very appealing research area in these environments has been the wireless ad hoc, sensor and mesh networks. These networks rely on ultra low powered processing nodes that sense surrounding environment temperature, pressure, humidity, motion or chemical hazards, etc. Moreover, the radio frequency (RF) transceiver nodes of such networks require the design of transmitter and receiver equipped with high performance building blocks including antennas, power and low noise amplifiers, mixers and voltage controlled oscillators. Nowadays, the researchers are facing several challenges to design such building blocks while complying with ultra low power consumption, small area and high performance constraints. CMOS technology represents an excellent candidate to facilitate the integration of the whole transceiver on a single chip. However, several challenges have to be tackled while designing and using nanoscale CMOS technologies and require innovative idea from researchers and circuits designers. While major researchers and applications have been focusing on RF wireless communication, optical wireless communication based system has started to draw some attention from researchers for a terrestrial system as well as for aerial and satellite terminals. This renewed interested in optical wireless communications is driven by several advantages such as no licensing requirements policy, no RF radiation hazards, and no need to dig up roads besides its large bandwidth and low power consumption. This second part of the book, Mobile and Wireless Communications: Key Technologies and Future Applications, covers the recent development in ad hoc and sensor networks, the implementation of state of the art of wireless transceivers building blocks and recent development on optical wireless communication systems. We hope that this book will be useful for students, researchers and practitioners in their research studies.

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