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Virtual and Remote Laboratories for E-Learning Using EDA Tools

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1. Introduction

Distance learning has gained in popularity not only as a way to offer instruction in locations without local expertise, but also as a cost-effective method where limited enrolment at one location would not normally warrant offering the course. In engineering technology programs, where most courses have a lab component, distance learning offers many new challenges in course delivery (K.D Taylor et al., 1996) and (L. Peretto et al., 2008). Nowadays the challenge for engineering education is about the online education: the role of laboratory is very important in engineering studies. In the past two decades great efforts have been made in this direction and many proposals of virtual and remote labs have been presented (D. Bonatti et al., 2007). Recent advances in digital system design have had a huge impact on the learning situation for students enrolled in hardware design courses. Since the invention of the Internet, many academicians, educators, and researches have been searching for effectual virtual lab experiments, however, the very nature of real experimentation was not possible or missing (A. Abu-El Humos et al., 2005). Hardware Design Laboratory is one of the main concerns for e-learning courses in digital design area (W.M. El-Medany, 2007).
The use of Hardware Description Languages and Field Programmable Gate Arrays for digital design today changes the way of designing and testing the digital circuits. The students can use software tools to design and test their circuits, and then use a hardware tools "FPGA Boards" to implement their design in a real hardware implementation using FPGA chip, which is a programmable chip that can be configured with a custom digital design. Hardware design laboratory using VHDL and FPGA has been used for partial e-learning courses, where the students can do most of the work for their experiment at home using the free software tool available on the internet, that work include the simulation and implementation, then they come to the lab with a binary file that will be used for configuring the FPGA chip, and then they can test their design in a hardware level using the available FPGA development board (W.M. El-Medany, 2007). In this chapter we are going to describe the use of Hardware Description Languages (HDL) and Field Programmable Gate Arrays (FPGA) for delivering the digital design courses as partial and full E-learning courses. The most important part of the digital design courses is the hardware laboratory. We are introducing a virtual and remote laboratory for digital design that is suitable for partial and full e-learning courses in computer engineering hardware design. The virtual

and remote laboratory based on using Spartan 3E FPGA starter kits from Diligent that are connected to the lab PCs through the USB port, and by using a digital camera that are connected to the PC. The PCs are connected to the Local Area Network (LAN) in the campus. The students can remotely login to the lab PCs by using Microsoft remote desktop connection to program the FPGA chip with their design, and then test the design remotely through the parallel port of the lab PCs. For testing the hardware circuit through the PC parallel port a Graphical User Interface (GUI) has been built using Visual Basic to apply forces to the design input pines that are connected to parallel port of the PC, and then read the design output also through the parallel port.

2. Digital Design Laboratory

Normally in digital design laboratory, the students can do their experiments by bringing up the required components; start to connect the components together by wiring them on a breadboard; then test the circuit by giving some inputs and view the corresponding output on LEDs (Light Emitting Diodes) or 7-Segment display to verify the functionality of the circuit. This process takes longer time, especially if the student has some mistake in the wiring, or some faulty ICs. An example of the normal method in digital design laboratory is given in Figure 1.

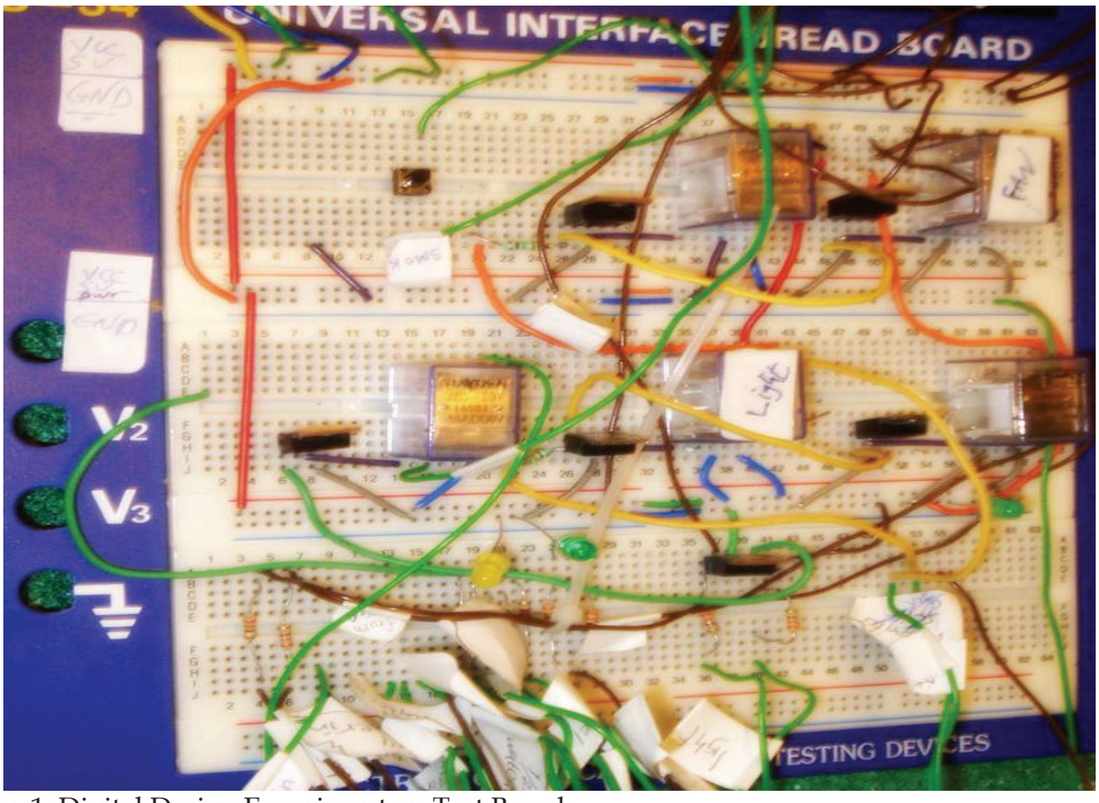

Fig. 1. Digital Design Experiment on Test Board

3. Modern Digital Design Laboratory Using EDA Tools

Nowadays, Hardware Description Languages (HDL) are being used for describing the design hardware, where the student can use EDA tools to enter his or her design and go through all design processes to finish and test the design, by going through all design process on the PC without using any hardware tools (Pastor, J.S.A, 2004) and (Fujii, N. , 2005). Then the design can be implemented in hardware using FPGA (Field Programmable Gate Array) with the aid of the hardware tools that is connected to the computer, which in this case is the downloading FPGA development board (Lockwood, J.W, 2001) and (Fujii, N. , 2003). Some of the available FPGA development boards have a number of switches and LEDs for testing the implemented design (Seinauskas, R, 1997) and (Fujii, N. , 2005). In our hardware design laboratory we are using VHDL language for describing the design and Xilinx tools for the hardware design implantation. Xilinx ISE 6.2i has been used for the design entry and synthesis process and ModelSim XE 5.6 has been used for the simulation process, where Xilinx Spartan 3 starter kit has been used for the hardware implementation. Students upload their design files on WebCt in the form of VHDL file, waveform file, and binary file for programming the FPGA, and then they can download the file on the PC that is attached to the FPGA development boards in the laboratory for testing their design (W.M. El-Medany, 2007). Figure 2, shows Xilinx Spartan 3 starter kit attached to a PC in the Laboratory, in which Xilinx software tools and WebCt are both running such that the design files already on Webct can be downloaded to Xilinx. This technique is useful for partial delivering of e-learning digital design courses.

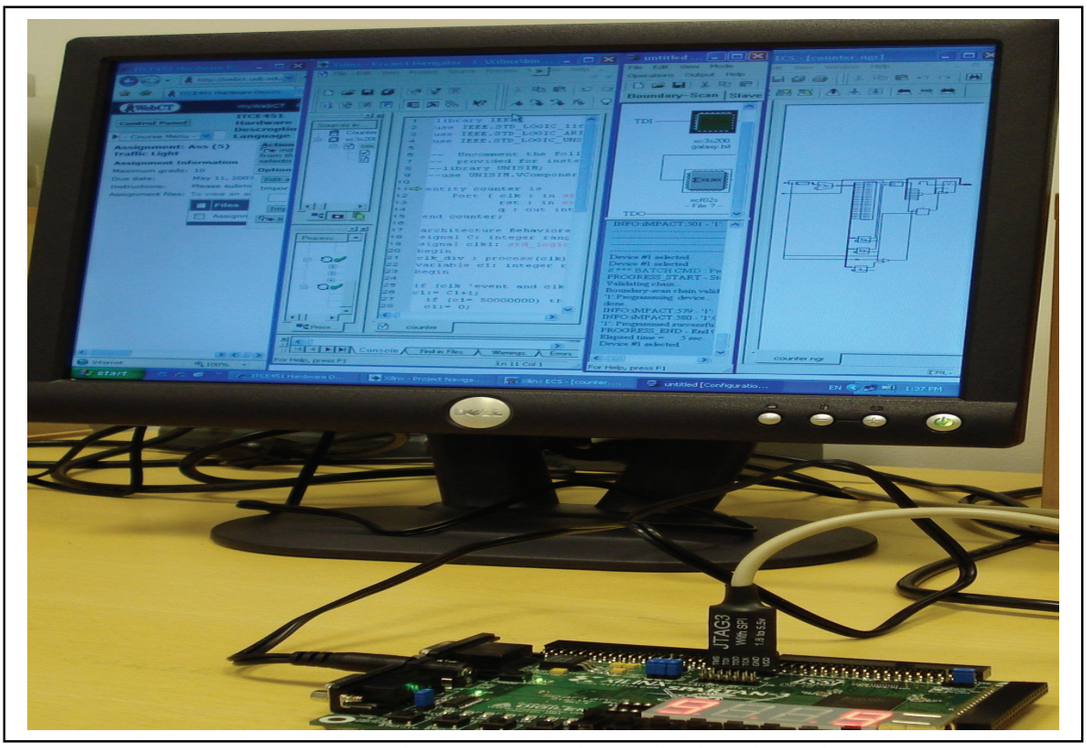

Fig. 2. Xilinx Spartan 3 FPGA Development Board Attached to the Lab PC

4. VHDL Design Steps

The design steps when using VHDL as a hardware description language, starts by writing a VHDL code that describes the required digital circuit, checking the code for syntax error, converting the code into gate level design using the available synthesis tools from Xilinx, assigning the pines for the target device, implementing the design, and then programming the device using the available FPGA development board. All of these steps can be done by the student at home; the last step which is programming the FPGA device is the only step that must be done in the laboratory for testing the design (W.M. El-Medany, 2007). Figure 3 shows a block diagram for the design steps as indicated above, the student also simulate the design using ModelSim to verify the correctness of the design. After finishing the first four steps as shown in Figure 3, the student uploads all the necessary files on his account to Webct, downloads these files on the PC in the Laboratory, and then do the last step for testing the design.

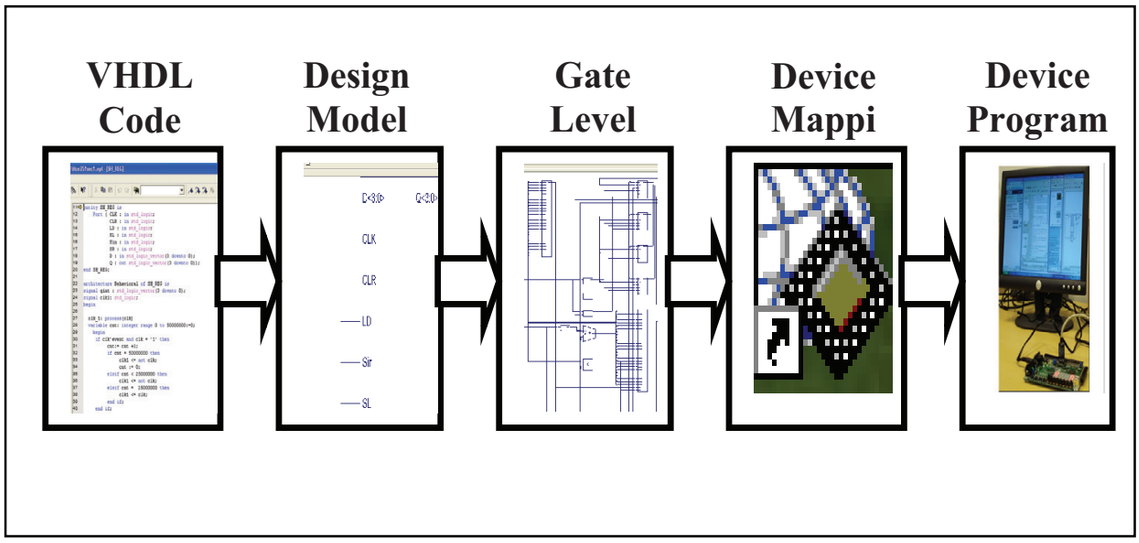

Fig. 3. Block Diagram for VHDL Design Steps

5. FPGA Design Methodology

The design methodology when using FPGA as the target hardware implementation can be described in a series of steps as shown in Figure 4. Where the design has to be specified and documented at the initial step. The second step is the design entry, which can be VHDL / Verilog or schematic entry. After checking the code or circuit, the design has to be simulated for the functionality of the design, if the function is not correct, then code or circuit has to be modified again and again until a correct function achieved, this is the third step. The design will be synthesized to build the gate circuit of the design; this step is valid only for the HDL entry, in which the code is converted to logic circuit. The implementation step is for mapping the design into the FPGA chip, in which place and rout tack place. Then the FPGA device will be configured with the design, for this step the FPGA development board has to be connected to the PC, in which the software tools is running. At the end after configuring the device, the design will be tested in a hardware level by assigning forces to the inputs

and testing the output for the given input. After checking the code or circuit, the design has to be simulated for the functionality of the design, if the function is not correct, then code or circuit has to be modified again and again until a correct function achieved, this is the third step, and it is shown in Figure 5, as an example, the simulation in the figure is for 4*1 multiplexer. To build the hardware circuit, the design will be synthesized to generate the gate level circuit of the design as shown in Figure 6, the top-level design in that figure is for a clock division design, in which the code is converted to logic circuit. The implementation step is for mapping the design into the FPGA chip. Then the FPGA device will be configured with the design. At the end after configuring the device, the design will be tested in a hardware level by assigning forces to the inputs and testing the corresponding outputs (WM El-Medany and A. Kamal, 2008).

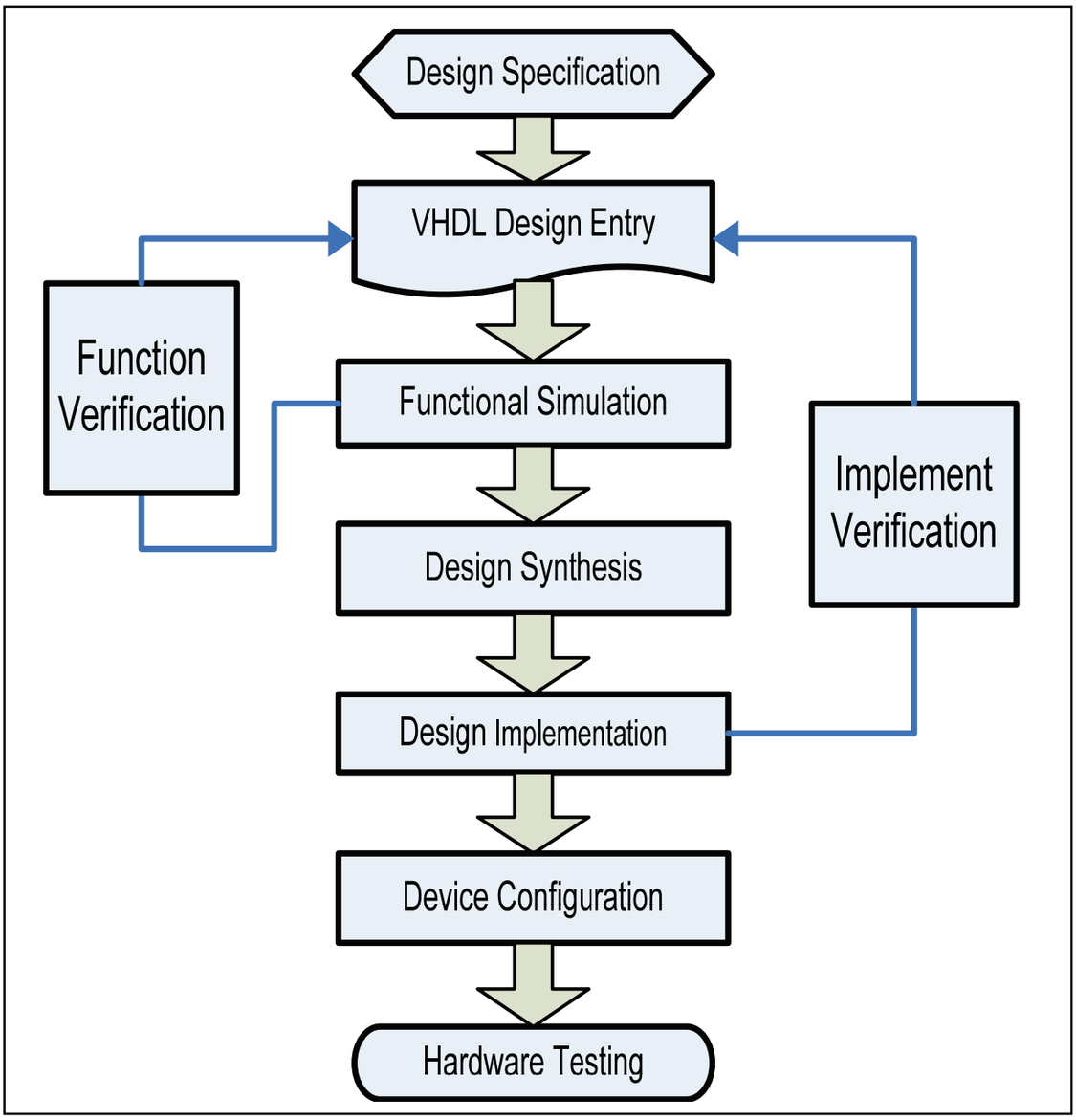

Fig. 4. FPGA Design Methodology

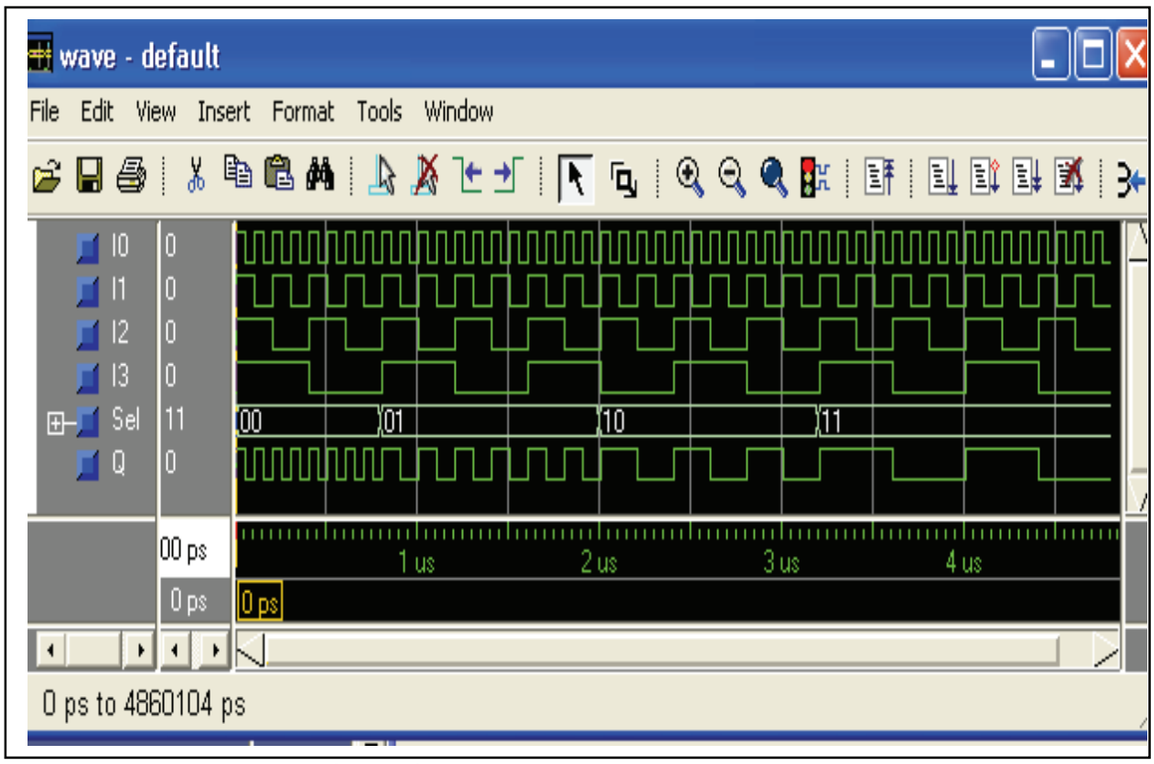

Fig. 5. VHDL Design Simulation for 4*1 MUX

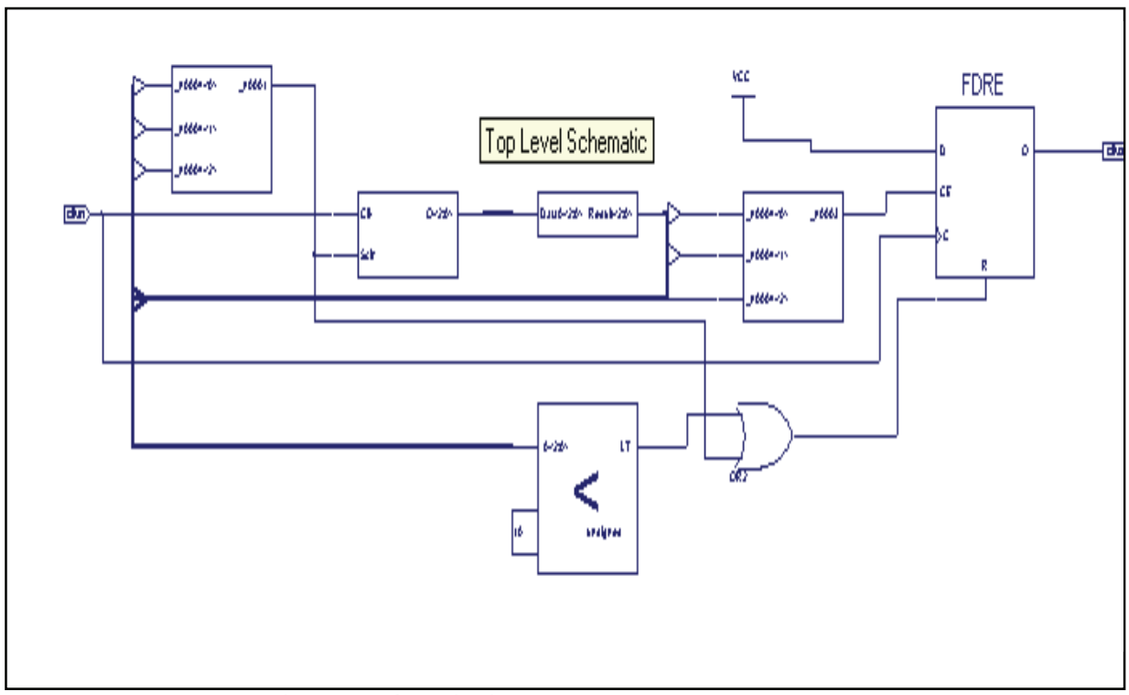

Fig. 6. VHDL Top-Level Design for Clock Division

6. FPGA Remote Laboratory

Remote laboratories have been used widely for software simulation tools, where the students can remotely login to the lab machine to access and run the software tools and do any required simulation or any software tasks. But the story for the hardware is different, where the students need to build and test their hardware physically. For these reasons the hardware courses are normally delivered as partial e-learning courses because the students can not do all the assignments without coming to the laboratory. The FPGA remote laboratory is a technique based on using the FPGA board with lab PC as remote laboratory for digital design. The FPGA remote laboratory is needed only for the last two steps of the VHDL design flow shown in Figure 4, where all the other steps can be done using the free available software tool from Xilinx. The students can also run the software tools on the lab PC and finish all the design steps including downloading the bit stream file into the FPGA, and then testing the circuit through the PC parallel port using Microsoft XP remote desktop that accesses the Lab PC from a remote machine. Figure 7 shows the parallel port pin assignments that have been used for sending and receiving data to the design for Verification.

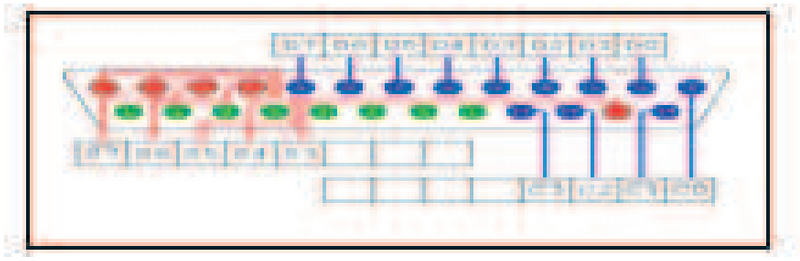

Fig. 7. Parallel Port Pin Assignments

Figure 8 shows the student access of the FPGA remote laboratory and the configuration of the FPGA chip from the student machine. In the botom right of Figure 8, you can see the FPGA development board that is connected to the PC parallel port, with the JTAG cable is connected through the USB port of the PC instead of the parallel port JTAG cable to make the parallel port available for the design testing. In the botom left of Figure 8, we can see the FPGA development board with the connection to the parallel port through the used bread board. A Graphical User Interface (GUI) has been designed using Visual Basic to simplify the process of applying forces to the design inputs, and then check the output. The GUI also simulate the switches and LEDs of the FPGA development board, through the GUI the student can just click the mouse to force the input, then he can see the output on his PC screen.

The system architecture of the remote laboratory is shown in Figure 9. The remote laboratory consists of 20 PCs; each PC is attached with one FPGA development board, with a total of 20 FPGA boards. All lab PCs are connected to the local area network of the campus. The students can use the free available webpack software from Xilinx to finish most of the design steps including the implementation and generation of the bit stream file that are required for programming the FPGA chip, then they can remotely login to the lab machine to access and run the Xilinx ISE software tools to configure the device, after that they can remotely test their design through the PC parallel port using Microsoft XP remote desktop that accesses the Lab PC from a remote machine.

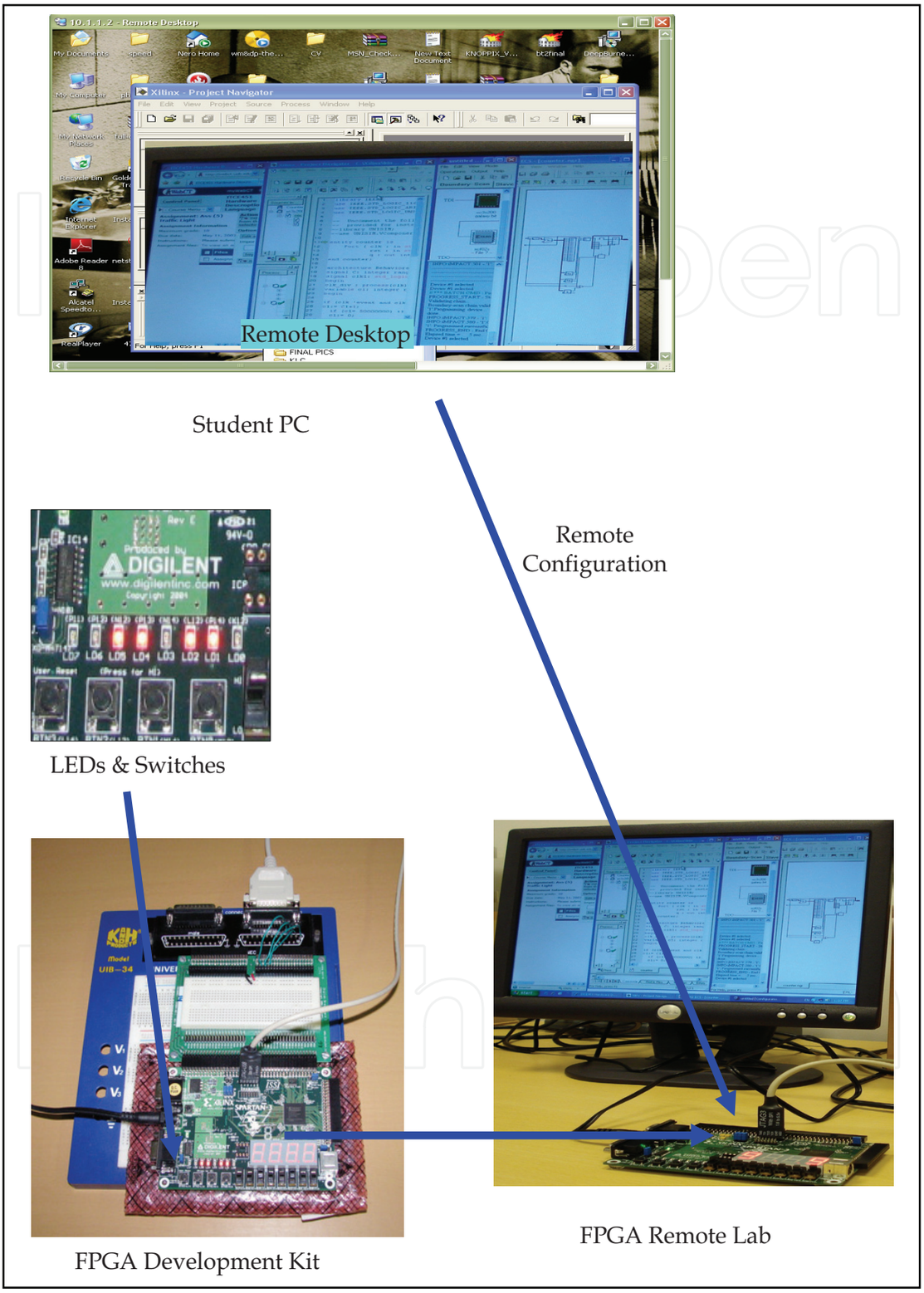

Fig. 8. FPGA Remote Laboratory

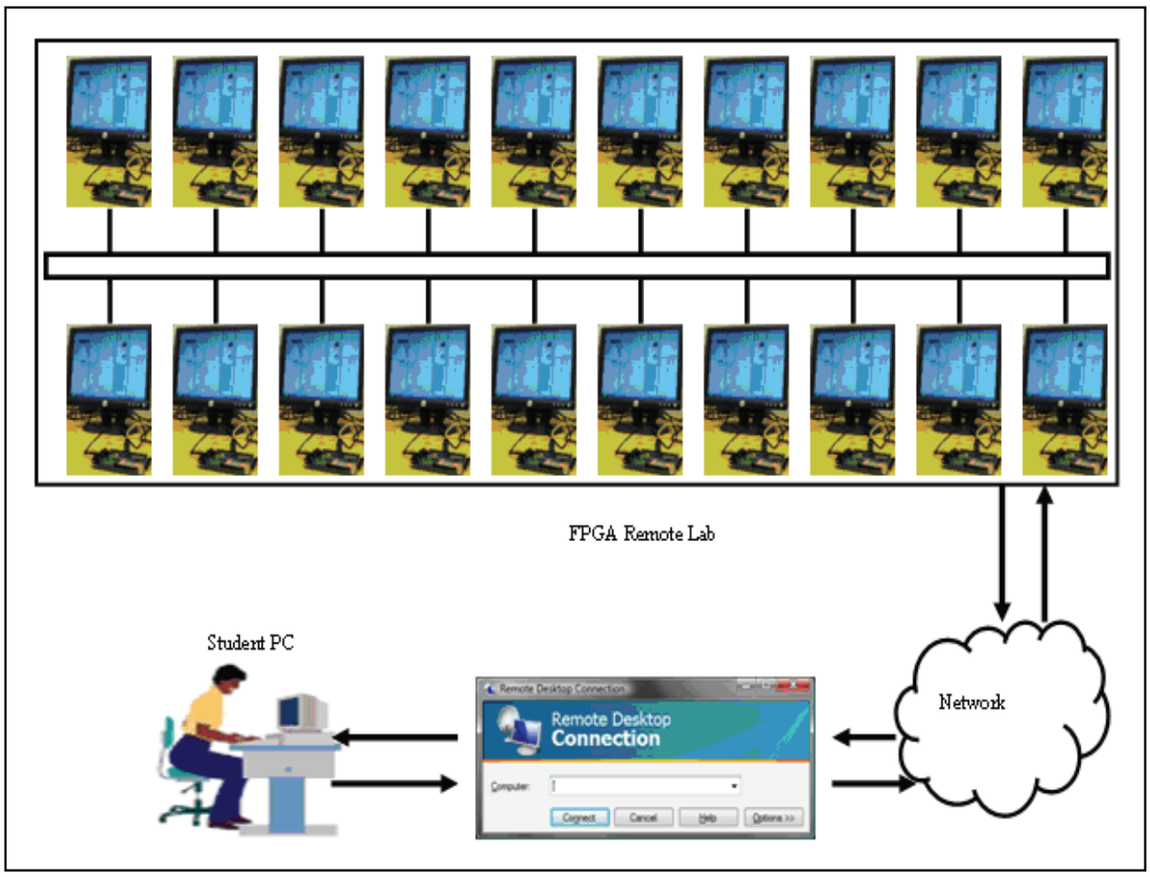

Fig. 9. System Architecture

7. Conclusion

FPGA remote laboratory has been introduced for hardware courses in area of computer engineering to be delivered as full e-learning courses. The FPGA remote laboratory consists of 20 PCs, each PC is connected to one FPGA development board, where FPGA Spartan 3E starter kit from Digilent has been used for programming the Spartan 3E FPGA chip. VHDL has been used as the design entry for the Xilinx ISE Foundation software tools for simulation and implementation. The laboratory has been tested for remote configuration of the FPGA chip through the USB port as well as remote testing of the design through the PC parallel port. GUI has been designed using Visual Basic by which the user can easily test the design remotely by applying forces to the design inputs, and then read the corresponding output. The remote access has been achieved by using Microsoft XP desktop remote connection. More developments are needed for the introduced FPGA remote laboratory. One of the developments is to use a webpage to remotely access the laboratory through the internet for programming or testing the FPGA. Another issue is to use a web camera with each FPGA development board, by which the user can monitor the FPGA board and see the output of the design on the available LEDs or 7-Segments.

8. References

K.D Taylor, J.W Honchell, W.E DeWitt, (1996). "Distance learning in courses with a laboratory", Frontiers in Education Conference, 26th Annual Conference, Proceedings of Volume 1, pp. 44 - 46, 6-9 Nov.

L. Peretto, S. Rapuano, M. Riccio, D. Bonatti, (2008). "Distance learning of electronic measurements by means of measurement set-up models", Measurement, pp. 274–283,.

D. Bonatti, G. Pasini, L. Peretto, E. Pivello, R. Tinarelli, (2007). "A Novel Approach for Laboratory Activities in E-Learning Courses", 2007 IEEE Instrumentation and Measurement Technology Conference, pp. 1-6.

A. Abu-El Humos, B Alhalabi, M.K. Hamzal, E. Shufro, W. Awada, (2005). "Remote labs environments (RLE): a constructivist online experimentation in science, engineering, and information technology", IECON 2005. 31st Annual Conference of IEEE, pp. 6-10.

WM El-Medany, (2007). "E-Learning for Hardware Design Laboratory Using VHDL and FPGA", Sixth International Internet Education Conference, ICT-Learn2007, Cairo, Egypt, pp. 285-289.

WM El-Medany, A. Kamal, (2008). "Development of Design Lab for Hardware e-Learning Courses in UOB" The second International Conference & Exhibition for Zain E-Learning, Bahrain.

WM El-Medany, (2008). "FPGA Remote Laboratory for Hardware E-Learning Courses", The IEEE REGION 8 SIBRCON 2008, International Conference on "Computational Technologies in Electrical and Electronics Engineering", Novosibirsk Scientific Centre, Novosibirsk, Russia.

M. Auer, A. Pester, D. Ursutiu, C. Samoila, (2003). "Distributed virtual and remote labs in engineering", 2003 IEEE International Conference on Industrial Technology, Volume 2, pp. 1208 - 1213Issue .

J. Hu, C. Meinel, (2004). "Tele-Lab ''IT-Security'' on CD: portable, reliable and safe IT security training", Computers & Security, Volume 23, pp. 282-289.

J. Lucca, (2004). "An assessment of e-Learning technologies to support telecommunications laboratory learning objectives", Proceedings of the 37th Annual Hawaii International Conference on System Science,.

P. Hai Lin, M. Lin, (2005). "Design and implementation of an Internet-based virtual lab system for e-learning support", ICALT. Fifth IEEE International Conference on Advanced Learning Technologies.

M.J. Callaghan, J. Harkin, E. McColgan, T.M. McGinnity, L.P. Maguire, (2007). "Client–server architecture for collaborative remote experimentation", Journal of Network and Computer Applications, Volume 30, pp. 1295–1308.

M. Guggisberg, P. Fornaro, T. Gyalog, H. Burkhart,(2003). "An interdisciplinary virtual laboratory on nanoscience", Future Generation Computer Systems volume 19, pp. 133–141.

Z. Nedic, J. Machotka, A. Nafalski, (2003). "Remote laboratories versus virtual and real laboratories", FIE 2003. 33rd Annual Frontiers in Education, Volume 1, pp. T3E-1 - T3E-6.

R. Hashemian, C. Pedapati, (2005). "Backboard-Based Digital Hardware Design Using FPGAs ", Proceedings of ASEE 2005 IL/IN Sectional Conference, pp. T3-4.

R. Hashemian, J. Riddley, "A Method to Design, Construct and Test Digital Hardware all in Classroom Environment", 37th ASEE/IEEE Frontiers in Education Conference, pp. T3G 1-6.

WM El-Medany, M. R. El-Sabry, (2008). "GSM-Based Remote Sensing and Control System Using FPGA", Proceedings of the International Conference on Computer and Communication Engineering, ICCCE'08, IEEE catalog number CFP0839D, V II, pp. 1093-1097.

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