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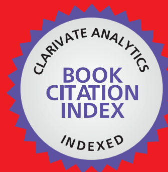

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Carbon Nanotube Interconnect Technologies for Future LSIs

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1. Introduction

Carbon nanotubes (CNTs) are attractive as nanosize structural elements from which devices can be constructed by bottom-up fabrication. A CNT is a macromolecule of carbon and is made by rolling a sheet of graphite into a cylindrical shape. CNTs exhibit excellent electrical properties that include current densities exceeding 10^9 A/cm^2 and ballistic transport along the tube. Because of these factors, with their large electro-migration tolerance and low electrical resistance, CNTs can be used as nano-size wiring materials, and are thus becoming potential candidates for future LSI interconnects. Much effort has been made to produce CNT vias, which use bundles of MWNTs (multi-walled carbon nanotubes), as vertical wiring materials as shown in Figure 1. Sato et al. demonstrated low-resistance CNT vias employing a novel metallization technology, which used preformed catalyst metal particles, to grow dense MWNT-bundles by thermal chemical vapor deposition (CVD).

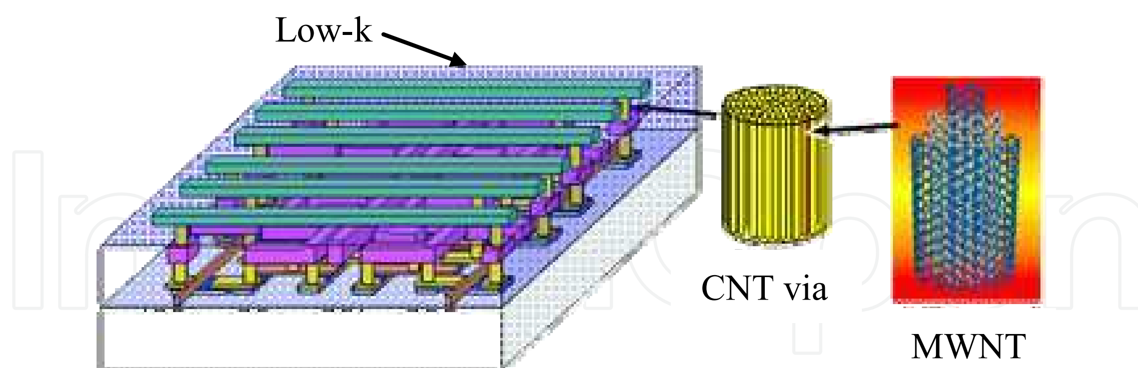

Fig. 1. Schematic of future LSI interconnects consisting of CNT vias and low-k materials.

The advantage of CNT-bundles is their low resistance, which may be the solution to the problem of high resistance in scaled-down vias. As shown in Fig. 2, we estimated the resistance of a 50-nm-diameter via depending on the filling rate of CNTs in the via area. In this estimation we assumed that CNTs have the quantum resistance $R_Q = h/4e^2 = 6.45$ kΩ (conductance $G_Q = 2G_{Q0} = 4e^2/h$, which reaches the maximum conductance limit for ballistic transport in two channels of a CNT), that current flows through each shell of MWNTs, and that there is no dependence of ballistic transport on CNT length. In order to lower the

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resistance of CNT vias, it is necessary to increase the nanotube's density, by decreasing its diameter. Regarding the electrical properties, CNTs consist of semiconductive CNTs as well as metallic types. Since the energy gap of a semiconductive CNT is inversely proportional to its diameter, smaller-diameter SWNTs may adversely influence the current conduction property. On the other hand, larger-diameter MWNTs seem to have a vanishing energy gap at room temperature. So, we are aiming at using metallic MWNTs with their ballistic transport properties as vias.

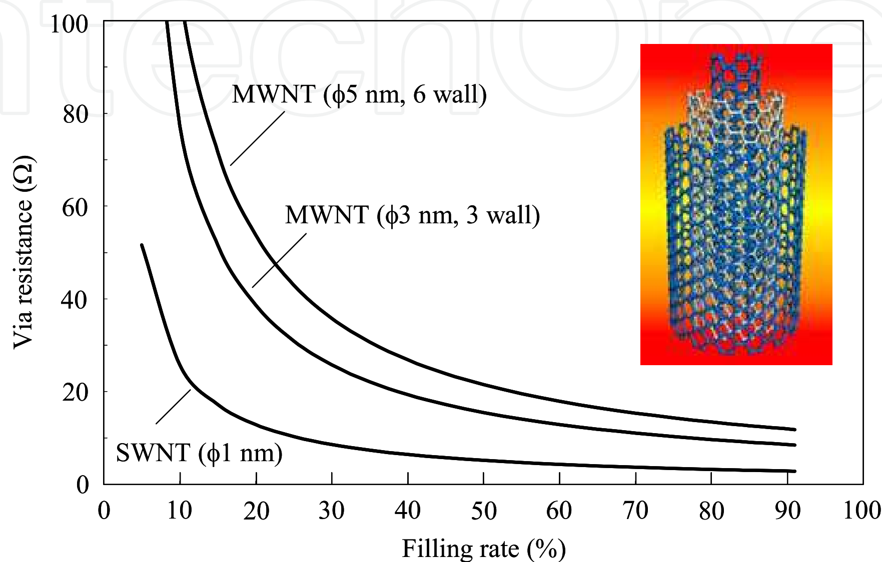


Fig. 2. Estimated resistance of 50-nm-diameter vias dependent on the filling rate of CNTs in a via hole for 1-nm-diameter SWNT, 3-nm-diameter 3-walled MWNT, and 5-nm-diameter 6-walled MWNT.

In this study, we demonstrated vertically scaled-down CNT via interconnects to clarify the current conduction properties of MWNT-bundles grown using thermal CVD. Based on our investigation, the carrier transport is expected to be ballistic for scaled-down vias. The excellent tolerance of CNT vias to a high current density was also demonstrated.

2. Experimental

As schematically shown in Fig. 3, we proposed CNT damascene processes to integrate scaled-down CNT vias with Cu interconnects. The processes were mostly compatible with conventional Cu interconnects. Briefly, a substrate with a Cu interconnect covered by a dielectric layer was first prepared. The dielectric layer was SiOC with k = 3.0 or k = 2.6. Via holes with a diameter of 160 nm were made using conventional photolithography followed by dry etching. A TaN/Ta barrier layer and a TiN contact layer were deposited by physical vapor deposition (PVD). Because CNTs do not need barrier layers, it is favourable to deposit these metals except the sidewall of the via hole. Size-controlled Co particles with an average diameter of about 4 nm were then deposited using a catalyst nano-particles deposition system. Previously we grew CNTs selectively in via holes, but all over the substrate in our new damascene process. For MWNT growth using the thermal CVD system, a mixture of C_2H_2 and Ar at 1 kPa was used as the source gas. The substrate temperature ranged from 400 ºC to 450 ºC. The chemical mechanical polishing (CMP) process we used is as follows:

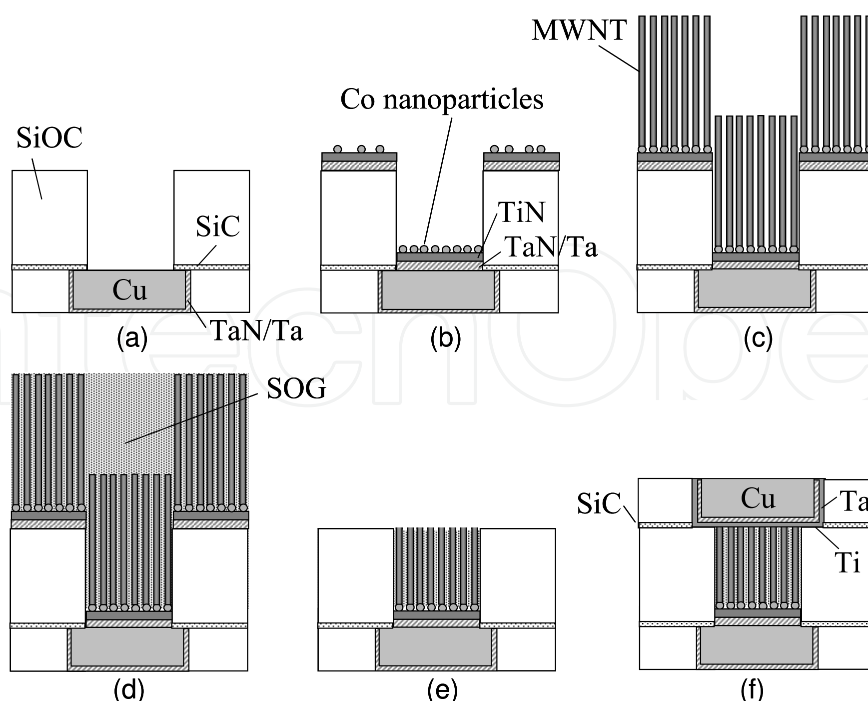


Fig. 3. CNT damascene via process: (a) Via hole formation on bottom Cu interconnect, (b) TaN/Ta barrier layer, TiN contact layer and Co catalyst nanoparticle formation, (c) MWNT growth, (d) SOG coating, (e) CMP Planarization, and (f) Top Cu interconnect formation.

the samples were coated with the spin-on glass (SOG) in order to hold the CNTs during the CMP process. CNTs were polished on the TiN layer on a SiOC layer with a conventional IC1000 pad and silica slurry under pressures of 2 psi (13.8 kPa) for 240 sec. Then, the TiN and TaN/Ta layers were polished with conventional barrier-metal CMP slurry. After polishing, the substrate was slightly wet-etched using buffered HF solution. Finally, the Ti top contact layer, Ta barrier layer and Cu wire were connected to CNT vias by PVD without subsequent annealing.

3. Results and discussion

Figures 4(a) and (b) are the cross-sectional scanning electron microscopy (SEM) images of CNT vias fabricated with growth temperatures of 450 ºC and 400 ºC. We can see in the images that CNTs grown at 400 ºC are a little less straight than those at 450 ºC, suggesting CNTs at 400 ºC are a little more defective.
To further investigate the quality of CNTs, we performed transmission electron microscopy (TEM) analyses, whose results are shown in Fig. 5. The TEM images indicate that CNTs grown at either temperature are of high quality. However, CNTs at 400 ºC appear to be a little more defective.
Figure 6(a) shows a cross-sectional SEM image of CNTs formed all over the substrate, having 160-nm diameter via holes, at the growth temperature of 450 ºC. We succeeded in growing vertically-aligned MWNTs with a diameter of 10 nm, a shell number of 7 and a density of $3x10^{11}$ cm^{-2}. Figure 6(b) shows a cross-sectional SEM image of CNT vias after CMP planarization. MWNT-bundles were successfully polished under pressures as low as those in the conventional Cu/low-k CMP process. Although SOG is filled well with MWNTs inside the 160-nm-diameter via hole, the filling factor of CNT in via is still low in this study.

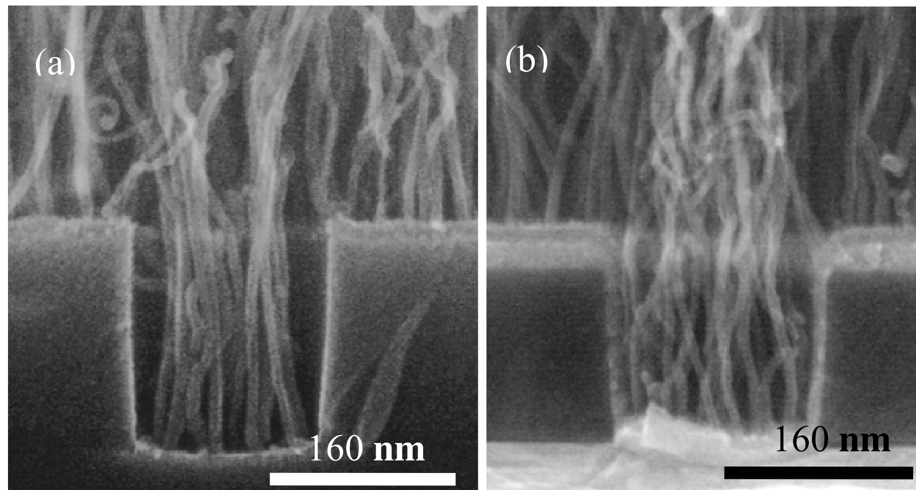


Fig. 4. Cross-sectional SEM image of the 160-nm-diameter CNT growth temperature (a) 450 °C and (b) 400 °C.

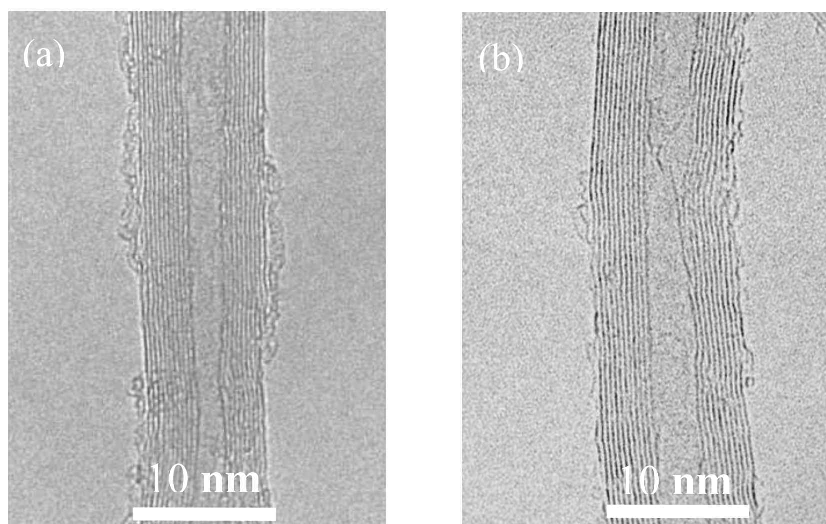


Fig. 5. TEM image of the CNT growth temperature (a) 450 °C and (b) 400 °C.

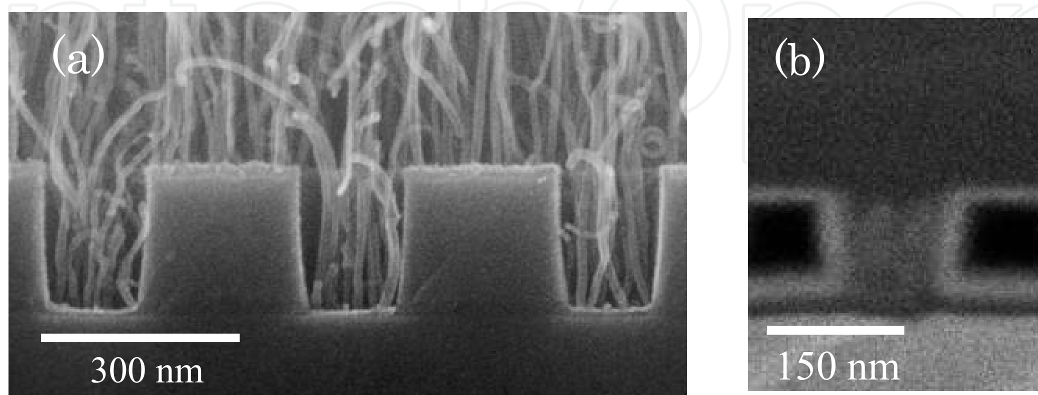


Fig. 6. Cross-sectional SEM image of (a) vertically aligned MWNTs formed all over the substrate, having 160-nm-diameter via holes, and (b) 160-nm-diameter CNT vias after CMP planarization.

We measured the via resistance of 2800-nm-diameter CNT vias with a four-point probe using Kelvin patterns. Figures 7(a) and (b) show the current-voltage characteristic on the low-bias region for the via height of 60 nm and 520 nm, respectively. For both cases, the current increased linearly depending on the voltage, and good ohmic contacts were achieved between the MWNT-bundle and the TiN contact layer. We summarized the electrical properties of 2800-nm-diameter CNT vias for a via height of 60 nm and 520 nm in Table I. The obtained resistance of 0.05 Ω for 60-nm-height 2800-nm-diameter vias is the lowest value ever reported. The most important point of the result is that the via resistance decreased by about 84% as the via height decreased by about 89%.

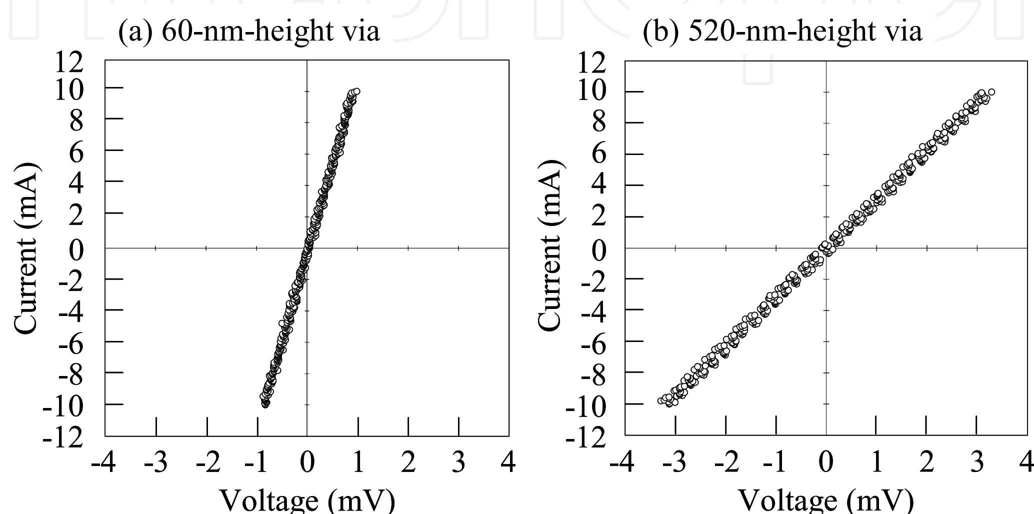


Fig. 7. Current-voltage characteristic of the 2800-nm-diameter CNT vias with a via height of (a) 60 nm and (b) 520 nm.

Sample	Diameter (nm)	Height (nm)	Resistance (Ω)	Resistivity (μΩcm)	Transport property
#1	2800	60	0.05	-	Ballistic
#2	2800	520	0.32	379	Ohmic

Table 1. Summary of electrical properties for CNT vias. The CNT density of $3x10^{11}$ cm^{-2} corresponds to the filling rate of 24%. The diameter and the shell number are 10 nm and 7, respectively. The shell number which contributes to the current conduction was estimated from the assumption of the quantum resistance.

Figure 8 shows via resistance distributions of the 2000-nm-diameter CNT vias with and without CMP planarization. The average via resistance of the sample with CMP decreased by about 25% compared with that without CMP. The scattering for the distribution of the sample with CMP is also smaller than that without CMP. We speculated that cutting the CNT bundles short by CMP could increase the number of electrical contacts between MWNT tips and the top metal electrode, because as-grown CNT bundles have an unfavorable worse uniformity in length.

We also measured the resistance of 160-nm-diameter CNT vias with a four-point probe using Kelvin patterns. Figure 9 shows the current-voltage characteristics on the low-bias region. It was found that the resistance depended on the growth temperature. The via

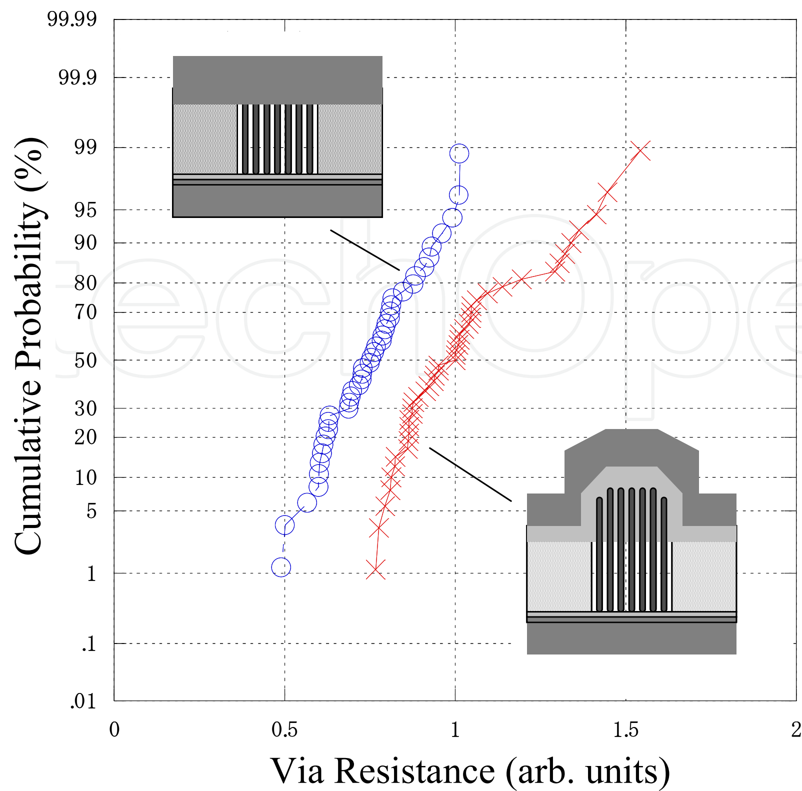


Fig. 8. Via resistance depending on the top metal contacts with and without CMP planarization.

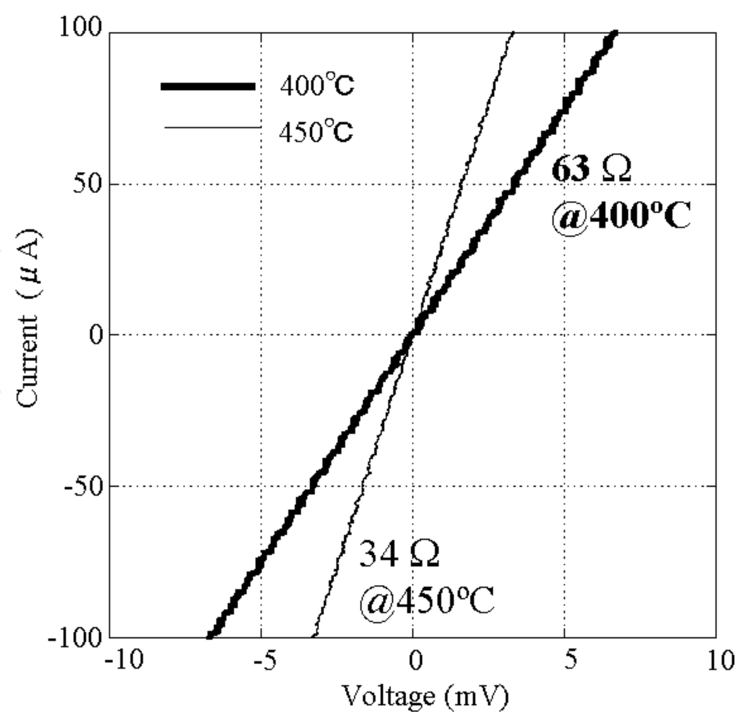


Fig. 9. Current-Voltage characteristics of the 160-nm-diameter CNT via grown at (a) 450 °C and (b) 400 °C.

resistance was 34 Ω for a growth temperature of 450 ºC, and 64 Ω for 400 ºC. Since the site density of the CNTs was similar for both temperatures, we speculate that the difference in resistance may have been caused by the difference in the CNT quality.

To investigate the transport mechanism, we measured the temperature dependence of the via resistance as shown in Fig. 10. The 520-nm-height vias shows the linear decrease of the resistance by decreasing the temperature. This characteristic is ohmic, which has been attributed to electron-phonon scattering. The corresponding resistivity of 379 μΩcm was obtained for 520-nm-height CNT vias, which are of the same order of magnitude as the value of CVD-tungsten (W) plugs (100-210 μΩcm). On the other hand, the resistance of 60-nm-height vias was independent of temperatures as high as 423 K, which suggests that the carrier transport is ballistic.

In order to estimate the electron mean free path λ_{CNT} of ballistic transport, we assumed the quantum resistance R_Q. The CNT via resistance R_{Via} is given by (1), where R_C is the imperfect metal-CNT contact resistance, n_{CNT} is the number of shells which contributed to the current conduction and H is the via height

$$R_{Via} = \frac{R_C + R_{CNT}}{n_{CNT}} \tag{1}$$

where

$$\begin{aligned} R_{CNT} = R_Q &= \frac{h}{4e^2} \;\ldots\; if\ H \ll \lambda_{CNT} \\ &= H \cdot \frac{R_Q}{\lambda_{CNT}} = H \cdot \left[\frac{h}{4e^2}\right] \cdot \frac{1}{\lambda_{CNT}} \;\ldots\; if\ H > \lambda_{CNT} \end{aligned}$$

Assuming the imperfect contact resistance R_C is as low as 0.5 kΩ, we estimated that the shell number of 7 contributed as a current conduction channel.

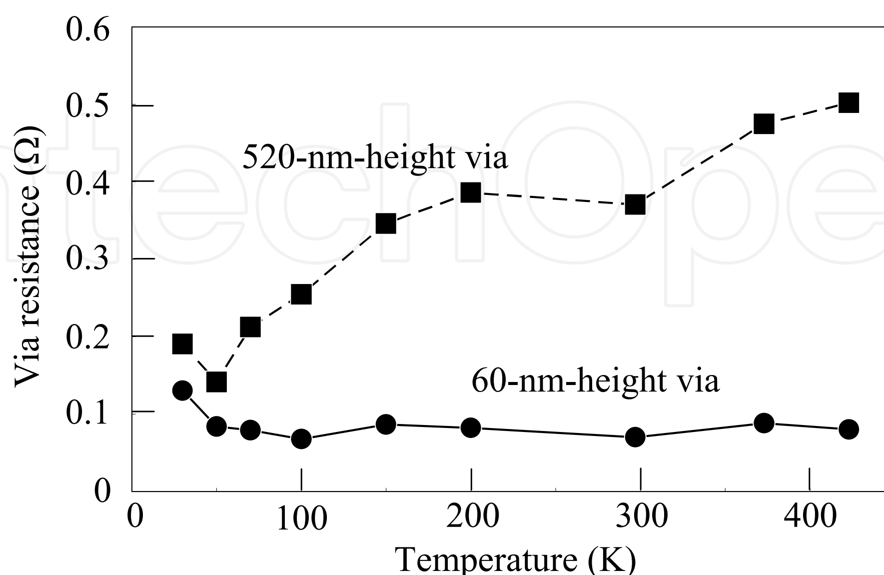


Fig. 10. Temperature dependence of the via resistance for the 60-nm and 520-nm-height CNT via.

Figure 11 shows the via resistance as a function of the via height. The filled circles show the previous results for 2800-nm-diameter vias with a growth temperature of 450 ºC. The solid lines indicate the via resistance calculated assuming various electron mean free paths. An solid rectangle or triangle indicates the current result normalized to a diameter of 2800 nm. As can be seen in the figure, the current result for 450 ºC falls on the line for an electron mean free path of 80 nm, the same as the previous data. This seems reasonable considering the growth temperature for the previous data was also 450 ºC. On the other hand, the resistance for 400 ºC falls on the line for an electron mean free path of 40 nm, which suggests the quality of CNTs grown at 400 ºC is not as high as that at 450 ºC, as also speculated from the SEM and TEM results. We therefore currently work on synthesizing higher-quality CNTs at 400 ºC or lower.

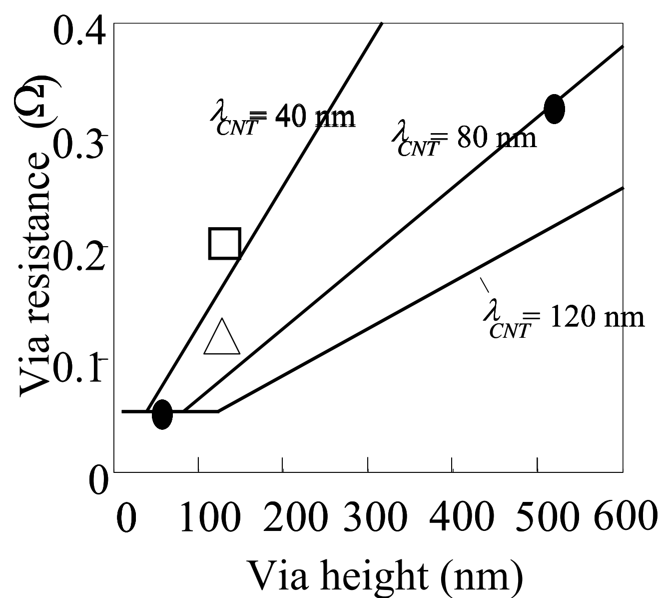
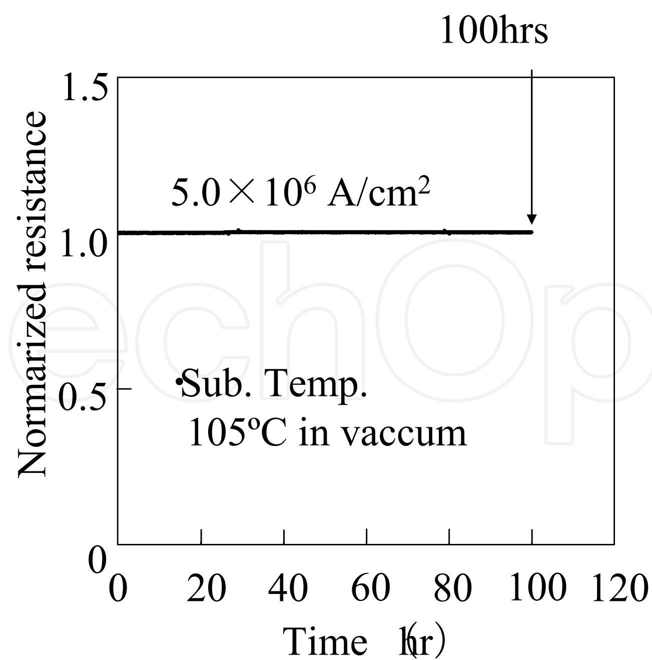
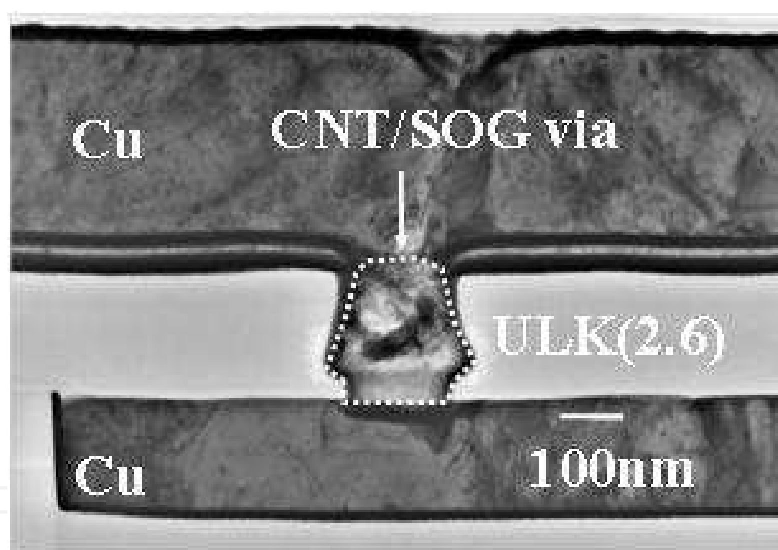


Fig. 11. Via resistance dependence as a function of the via height.
Solid line: the via resistance calculated assuming various electron mean free paths.
•: 2800-nm-diameter via 450 °C growth, △: 160-nm-diameter via 450 °C growth, □: 160-nm-diameter via 400 °C growth.

The stability of the via resistance under an electric current with a density of 5.0×10^6 A/cm^2 is shown in Fig. 12(a). The via diameter and growth temperature were 160 nm and 400 ºC, respectively. The dielectric layer was made of SiOC with k = 2.6. The measurement was performed at 105 ºC in a vacuum. The resistance remained stable even after running the electric current for 100 hrs. This indicates that the CNT via is robust over a high-density current as we expect. The cross-sectional TEM image of the via is shown in Fig. 12(b). The via shape looks deformed, but this was caused by high-energy electrons during the TEM observation.



(a)



(b)

Fig. 12. (a) EM characteristics at 105 ºC in a vacuum and (b) cross-sectional TEM image of the CNT via.

4. Conclusion

In this chapter, we report our trials of using bundles of CNTs with their ballistic transport properties as via interconnects of LSIs. We proposed CNT damascene processes to integrate scaled-down CNT vias with Cu interconnects. Moreover, we demonstrated vertically scaled-down MWNTs via interconnects to clarify the current conduction properties of MWNTs-bundles.

We fabricated a CNT via interconnect and evaluated its electrical properties and robustness over a high-density current. We found that the CNT via resistance was independent of temperatures, which suggests that the carrier transport is ballistic. From the via height dependence of the resistance, the electron mean free path was estimated to be about 80 nm, which is similar to the via height predicted for hp32-nm technology node. This indicates that it will be possible to realize CNT vias with ballistic conduction for hp32-nm technology node and beyond. It was also found that a CNT via was able to sustain a current density as high as 5.0×10^6 A/cm^2 at 105 ºC for 100 hours without any deterioration.

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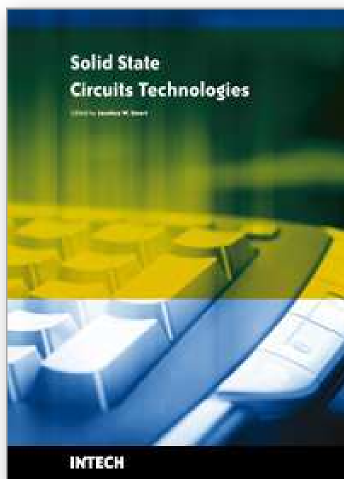

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The evolution of solid-state circuit technology has a long history within a relatively short period of time. This technology has lead to the modern information society that connects us and tools, a large market, and many types of products and applications. The solid-state circuit technology continuously evolves via breakthroughs and improvements every year. This book is devoted to review and present novel approaches for some of the main issues involved in this exciting and vigorous technology. The book is composed of 22 chapters, written by authors coming from 30 different institutions located in 12 different countries throughout the Americas, Asia and Europe. Thus, reflecting the wide international contribution to the book. The broad range of subjects presented in the book offers a general overview of the main issues in modern solid-state circuit technology. Furthermore, the book offers an in depth analysis on specific subjects for specialists. We believe the book is of great scientific and educational value for many readers. I am profoundly indebted to the support provided by all of those involved in the work. First and foremost I would like to acknowledge and thank the authors who worked hard and generously agreed to share their results and knowledge. Second I would like to express my gratitude to the Intech team that invited me to edit the book and give me their full support and a fruitful experience while working together to combine this book.

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