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Ultralow-power LSI Technology with Silicon on Thin Buried Oxide (SOTB) CMOSFET

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1. Introduction

For a variety of applications from mobile to high-performance computing, the power consumption of very-large-scale-integrated (VLSI) circuits is a serious issue. The scaling rule has been a paradigm for miniaturizing complementary metal-oxide-semiconductor (CMOS) field-effect-transistors (FETs) in VLSI circuits for a long period. In the ideal scaling rule, the supply voltage V_{dd} should decrease in proportion to the miniaturization of the transistor. This V_{dd} reduction has roughly been successful so far. In extremely scaled transistors such as those in the 45-nm logic node and beyond, however, it is very difficult to further decrease V_{dd}. Unless V_{dd} is reduced with the scaling rule, the power consumption of the LSI will increase significantly due to an increase in both operational and standby-leakage power (Sakurai, 2004; Chen, 2006). The primary cause of this difficulty is widely recognized as the increase in threshold voltage (V_{th}) variation of CMOSFETs, because V_{dd} should be set higher considering the margin to the increased V_{th} variation (Takeuchi et al., 1997).

Variation of transistor characteristics, primarily V_{th} variation, is increasing substantially in sub-100-nm technologies. This makes the V_{dd} reduction, required by the scaling rule, difficult, and significantly increases the power consumption of an LSI chip. Here, power consumption P of an inverter, which is the representative LSI unit circuit, is defined as

$$P = CV_{dd}^2 f + I_{leak} V_{dd} \tag{1}$$

where C, f, and I_{leak} are load capacitance, operation frequency, and leakage current, respectively. The first and second terms on the right-hand side represent operational and standby power, respectively. As the scaling proceeds, C and I_{leak} decrease due to the size reduction of transistors, and f increases. Since the miniaturization enables the number of circuits crammed onto a single chip to increase exponentially, it is extremely important to lower V_{dd} to maintain power consumption of an LSI chip (Moore, 1979). In the ITRS 2008 roadmap, the rate of V_{dd} reduction below 1 V is forecasted to be extremely small.

The origin of V_{th} variation is not only due to lithographic variations and layer thicknesses, but also due to line edge roughness (LER) and random dopant fluctuation (RDF) (Asenov et al., 2003; Mizuno et al., 1994). In particular, it has been pointed out that the V_{th} variation caused by the number and special distribution of impurities in the channel of transistors (RDF) becomes serious with the scaling. The magnitude of the V_{th} variation is described by

standard deviation σV_{th}, since the distribution of V_{th} usually shows a normal distribution. The V_{th} variation becomes small with the wider area of the gate because the impurity distribution should be random. This relationship is well known (Pelgrom et al., 1989) and is defined as

$$\sigma V_{th} = A_{Vt} / (L_g W_g)^{1/2} \qquad (2)$$

where L_g and W_g are the length and width of a gate, and the gradient A_{Vt} is called the Pelgrom coefficient. Moreover, in conventional bulk CMOSFETs, the following relationship exists

$$A_{Vt} \propto t_{ox} (N_{channel})^{1/4} \qquad (3)$$

where t_{ox} and $N_{channel}$ are the thickness of a gate oxide and a channel impurity density. Because $N_{channel}$ has increased to suppress the short channel effect (SCE), A_{Vt} has increased with scaling. Thus, it is understood that the present V_{th} variation problem is inevitably caused by the conventional bulk CMOSFETs' miniaturization.

To solve these problems, it is necessary to first decrease the V_{th} variation due to size variations by suppressing SCE, and secondly to decrease RDF by lowering the impurity densities of the channel. FinFETs, which have strong immunity from SCE without increasing the impurity density of the channel, are reported to have low V_{th} variation (Thean et al., 2006). On the other hand, to continue to both improve the speed and reduce the power from the system-LSI designer's viewpoint, it is necessary to set V_{th} and V_{dd} to the best value in every circuit block or set of transistors in LSI circuits. The multiple V_{th} design, such as that with two or three kinds of V_{th} setting, is already indispensable. Additionally, a technique that controls V_{dd} adaptively according to the state of operation has also been applied (Nakai et al., 2005). A technique to apply substrate bias V_{bb} to control V_{th} flexibly is used in some applications, also (Miyazaki et al., 2000). This V_{bb} control technique is a strong tool that can minimize the performance deviation due to temperature fluctuation as well as the variation of each chip. However, in present scaled bulk CMOSFETs, it is difficult to apply V_{bb} because of the increase in the junction leakage current between the source/drain and the substrate.

To solve the power consumption and V_{th} variation issues, we have proposed a fully depleted silicon-on-insulator (FD-SOI) CMOSFET with an ultrathin buried oxide (BOX), named "silicon on thin BOX (SOTB)". In this chapter, we will describe the features, process and characteristics of the SOTB CMOSFET. Its wide-range back-gate controllability, which enables the optimization of both performance and power after fabrication, will also be described. In addition, to solve some intrinsic problems with SOI technology such as poor electrostatic discharge (ESD) susceptibility and low breakdown voltage, an SOTB/bulk hybrid technology for system-on-chip (SoC) applications will be presented. In the later part of this chapter, we will show the variability reduction and back-gate bias control in the SOTB scheme and demonstrate its impact on the power reduction of VLSI circuits.

2. SOTB CMOSFET

2.1 Features of SOTB CMOSFET

To solve the V_{th} variation problem due to RDF and satisfy the demand from circuit designers, we have proposed the SOTB CMOSFET (Tsuchiya et al., 2004; Ishigaki et al., 2008; Morita et al., 2008). Figure 1 shows a schematic cross-section of the SOTB structure.

Ultrathin SOI and BOX layers make the transistor highly immune from SCE, and its intrinsic channel without halo implant suppresses the V_{th} variation due to RDF. The thin BOX and impurity doping in the substrate just beneath the thin BOX enables a multiple V_{th} design. This thin BOX and the doped region also enable the wide-range back-gate controllability which realizes optimization of both performance and power after fabrication.
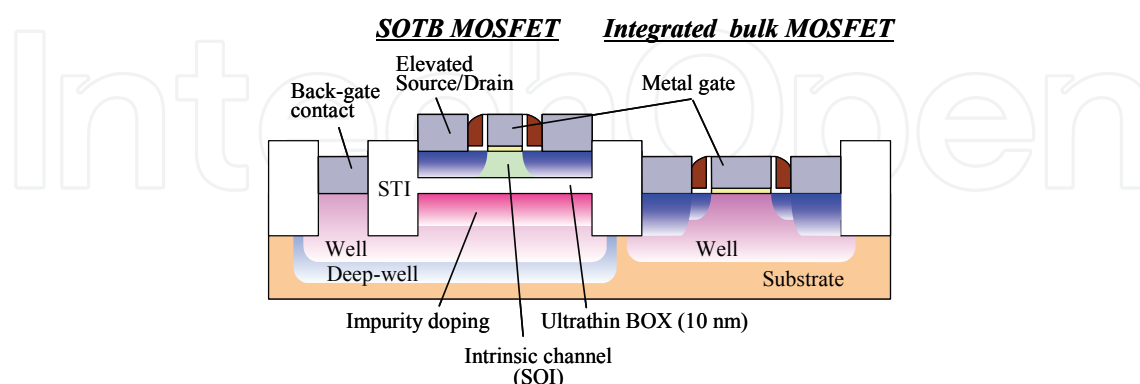

Fig. 1. Schematic cross-sectional view of hybrid SOTB/bulk CMOSFETs.

Some intrinsic problems with (FD-) SOI technology such as poor electrostatic discharge (ESD) susceptibility and low breakdown voltage are well known (Yoshimi et al., 1990). Such adverse effects can be easily avoided by combining bulk technology on the same wafer. The previous approach to integrating SOI and bulk technologies required the use of selective epitaxial growth to compensate for the height difference (Yang et al., 2003), which significantly increases process complexity. In this SOTB structure, bulk CMOSFETs for high-voltage I/O operation, ESD protection, and analog circuits can be easily integrated by removing the thin SOI/BOX layers. This simplified SOTB/bulk hybrid technology is preferable for SoC applications because no design change for the conventional peripheral circuits is required.

Regarding the isolation between transistors and back-gate contacts, this SOTB technology uses a conventional shallow-trench isolation (STI) process similar to the bulk technology. The slight change is that the trench is formed by dry etching three layers: the SOI, BOX, and substrate, as shown in Fig. 1. Consequently, the isolation between devices on the SOI and back-gate contacts is ensured by STI. The well region, acting as a back gate and ground plane, was formed beneath the BOX layer and connected to the region of the back-gate contact through the area underneath the STI. The back-gates for NMOS and PMOS are also isolated by STI. This back-gate contact structure in SOTB technology can be fabricated with the same mask layout as the conventional bulk CMOSFET. A triple-well structure is also adopted to prevent leakage for back-gate biasing.

2.2 Device design and fabrication

For low-standby power (LSTP) applications, a single mid-gap metal gate with an intrinsic channel is easily introduced in the fabrication process and is suitable for the desired V_{th} (Fenouillet-Beranger et al., 2008). However, unless the gate-induced drain leakage (GIDL) current is suppressed to less than the subthreshold leakage, off-current I_{off} cannot be reduced at the desired V_{th}. GIDL increases when gate bias V_g becomes negative (for NMOS, vice versa for PMOS). This is because of band-to-band tunneling in and around the drain junction below the gate edges. This leakage current is a source-to-drain current in SOI

structures because of the BOX layer, unlike the bulk transistor in which the GIDL current flows to the substrate. In the SOTB structures, the intrinsic channel is also effective to suppress GIDL because of low electric fields around the drain junction below the gate edges. Note that in an SOTB device, it is unnecessary to consider either the junction depth (because it is controlled only by SOI thickness) or the channel-impurity profile (because the SOTB device has an intrinsic channel with no halo implant). Therefore, the control of GIDL in an SOTB is simple. Only the gate overlap length L_{ov}, which is defined as the length of the overlapped region between gate and source/drain extensions, needs to be controlled.

Figure 2 plots the calculated GIDL with various L_{ov} values by using the ATLAS simulation (http://www.silvaco.com). The parameters used in this calculation are as follows: L_g, SOI thickness, BOX thickness, and gate oxide thickness are 65, 15, 10, and 2 nm at V_{dd} = 1.2 V, respectively. The inset shows the potential distribution with L_{ov} of 10 nm when V_g is -0.5 V and V_{dd} is 1.2 V. It is shown that the potential on the drain edge is steep due to the bias difference between the gate and drain. When L_{ov} is 10 nm, I_{off} (at V_g = 0 V) increases because of the subthreshold leakage and the GIDL since the large overlap enhances both the SCE and the GIDL. By decreasing L_{ov} to less than a few nm, GIDL can be reduced sufficiently. At the same time, however, on-state current I_{on} also decreases. Therefore, this indicates that L_{ov} should be carefully optimized for a target specification.
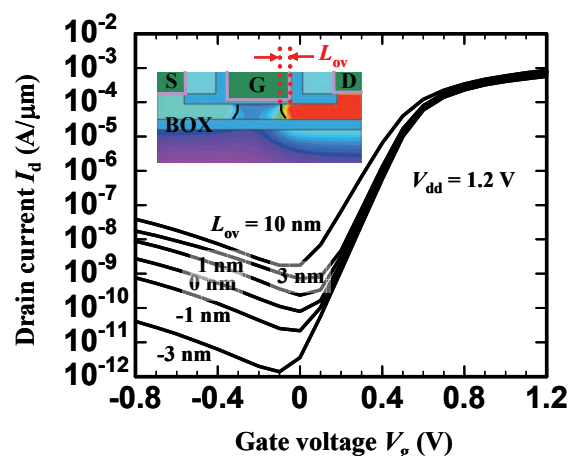

Fig. 2. Simulated NMOS I_d –V_g characteristics as a function of gate overlap length L_{ov} at V_{dd} = 1.2 V. The inset shows the potential distribution in SOTB structure at V_g = -0.5 V.

Figure 3 shows a process flow and a cross-sectional transmission electron microscope (TEM) image of an SOI/bulk hybrid structure. After the STI formation, the SOI layers (t_{SOI} ~ 12 nm) on both the well contact and bulk active regions were removed by dry etching using a BOX layer (t_{BOX} ~ 10 nm) as a stopper, followed by the removal of the BOX layer. Due to the small step height of 22 nm (t_{SOI} + t_{BOX}), gate patterning can easily be performed on both the SOI and bulk regions simultaneously. This process enables the SOTB/bulk hybrid structure to be fabricated without requiring epitaxial growth to compensate for the height difference. The SOI region is on the left side of the TEM image, and the integrated bulk region is on the right. Smooth gate patterning without voids on both the SOI and bulk regions was confirmed. These integrated hybrid bulk CMOSFETs with a 7.5-nm-thick gate dielectric were fabricated on the exposed surface of the silicon support wafer by removing SOI/BOX layers. The quality of the surface after the BOX removal is a concern in this process. Carrier mobilities as high as a universal curve and gate oxide interface trap density (D_{it}) as low as

10^{11} eV^{-1}cm^{-2} were confirmed with no sacrificial oxidation of the surface, indicating that little damage was caused by dry etching during the SOI-layer removal (Ishigaki et al., 2008). A sufficiently long time-dependent dielectric breakdown (TDDB) lifetime is ensured at V_g = 3.3 V, as shown in Fig. 4.
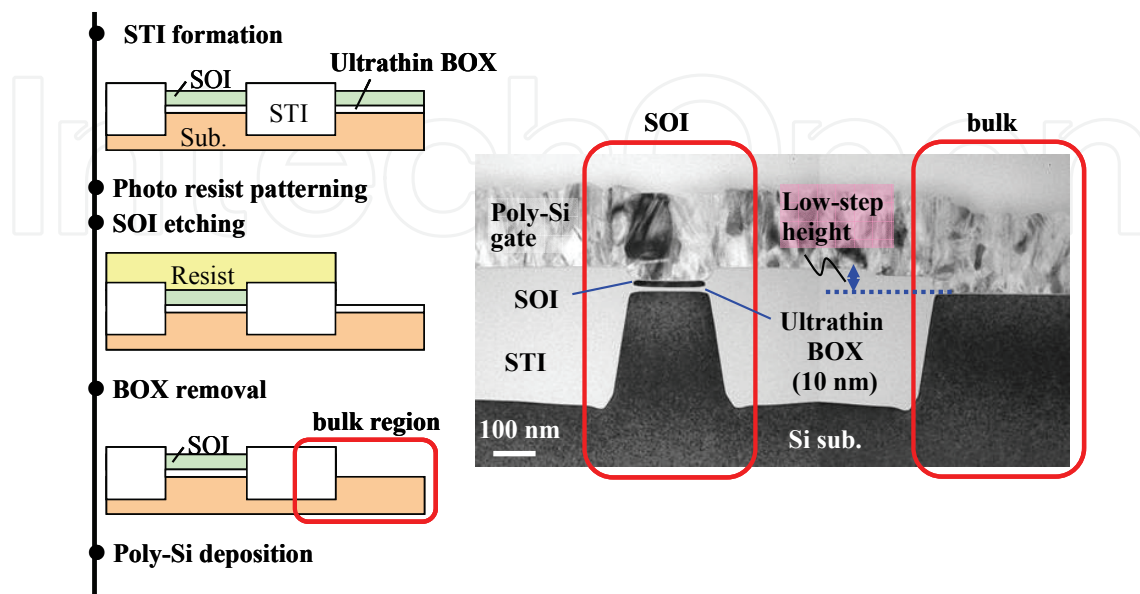

Fig. 3. Process flow of hybrid SOI/bulk fabrication and a cross-sectional TEM image of poly-Si gate on hybrid SOI/bulk regions.
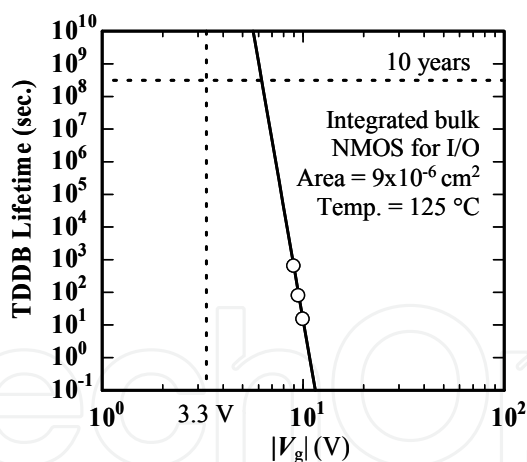

Fig. 4. TDDB lifetime of integrated bulk NMOS for I/O operation.

Figure 5 shows the following process steps as well as a cross-sectional TEM image of a fabricated 50-nm-gate-length SOTB MOSFET. In the dual oxidation process, SiON gate dielectrics were formed at an equivalent oxide thickness (EOT) of 1.9 nm for SOTB core CMOSFETs, and 7.5 nm for bulk I/O CMOSFETs. To precisely control L_{ov}, an additional SiN offset spacer was formed after the first SiO$_2$ spacer formation and before the source/drain extension implantation. After forming a sidewall, an elevated source/drain structure was formed by selective epitaxial growth to obtain low external resistance. To prevent recesses in the SOI, the conditions for gate- and sidewall- etching and precleaning before epitaxy were

carefully optimized, resulting in a low external resistance, as shown in Fig. 6. In low-power FD-SOIs with intrinsic channels, no dual metal technology between NMOS and PMOS gates, such as nickel silicide phase control (Veloso et al., 2006), is required when using nickel silicide as a gate electrode material. The gate poly-Si and the source/drain epitaxial Si were set to their optimal heights before gate-cap removal and fully silicided simultaneously in a single step without using chemical mechanical polishing (CMP). The metal inserted poly-silicon stack (MIPS) metal-gate structure is also applicable for SOTB CMOSFETs.

- Gate formation
- **Offset SiO$_2$ spacer & additional SiN spacer formation**
- SDE implantation
- Sidewall formation
- **Selective epitaxial growth**
- S/D and counter implantation
- Activation annealing
- **NiSi fully silicide formation**
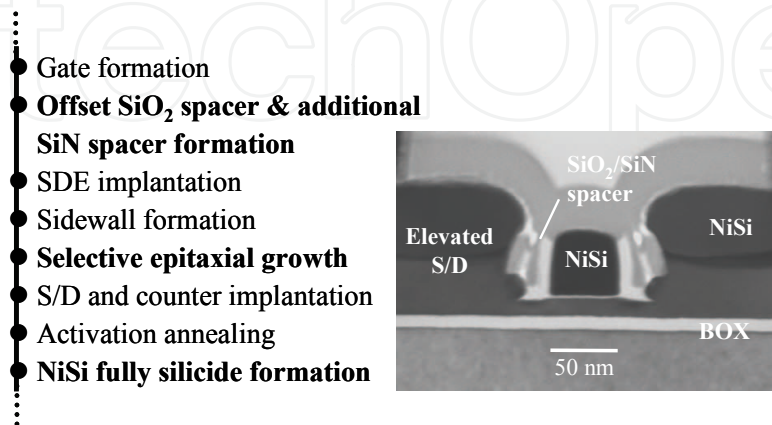
Fig. 5. Process steps and cross-sectional TEM image of 50-nm-gate-length SOTB MOSFET.
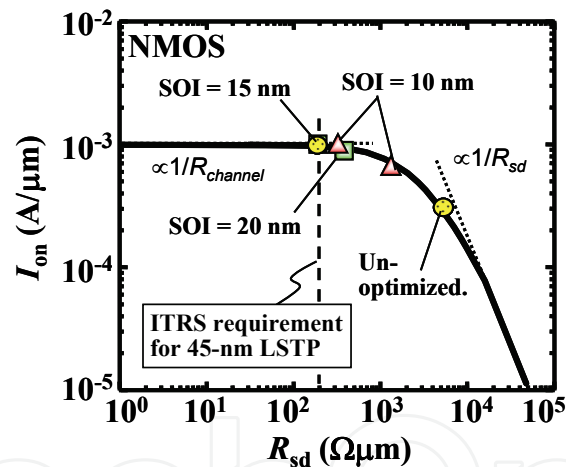
Fig. 6. Relationship between on-current I_{on} and external resistance R_{sd}.

3. Characteristics of SOTB CMOSFET

The typical subthreshold characteristics of the 50-nm-gate-length SOTB CMOSFETs at V_{dd} = 1.2 V are plotted in Fig. 7. The desired symmetrical characteristics were successfully obtained with a single Ni FUSI gate. The off-state drain currents were less than 20 pA/µm due to the reduction of GIDL with properly controlled L_{ov}. At the same time, comparable on-currents were obtained with the conventional bulk CMOSFETs. The I_{off} could be further reduced to 1 pA/µm by reducing L_{ov} (Ishigaki et al., 2009). These I_{on}/I_{off} values are in good agreement with the data based on bulk or FD-SOI technology for LSTP applications (Kimizuka et al., 2005). These SOTB CMOSFETs also suppressed the SCE even with the intrinsic channel because of the thin SOI and BOX layers. Figure 8 demonstrates that the

SOTB CMOSFET is free from the self-heating effect thanks to the thin BOX. That is, negative drain conductance (decreasing I_d with increasing V_d) was not observed.
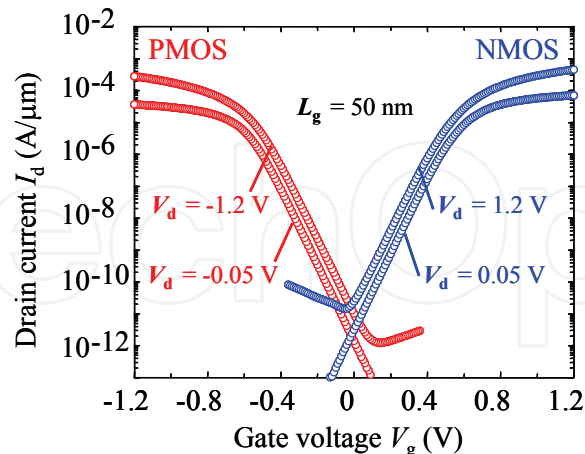

Fig. 7. Typical I_d-V_g characteristics of 50-nm-gate-length SOTB CMOSFET.
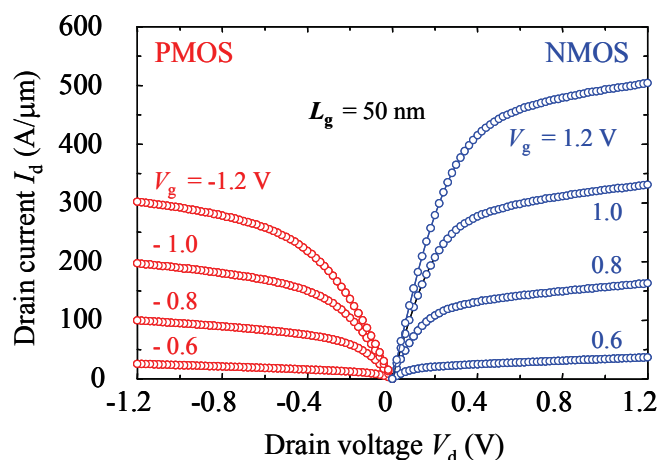

Fig. 8. I_d-V_d characteristics of 50-nm-gate-length SOTB CMOSFET. No self-heating is evident due to the thin BOX.

In the SOTB scheme, time-to-time or area-to-area (including die-to-die or wafer-to-wafer) device characteristics can be widely controlled using the back-gate bias V_{bb}. In particular, forward back-gate bias can be effectively used because there is no substrate leakage. Note that a forward bias higher than 0.6 V can never be applied in conventional bulk CMOSFETs owing to the significant increase in p-n junction leakage current from source to substrate. The dependences of V_{th} and the subthreshold slope (*SS*) of a 50-nm-gate-length SOTB CMOSFET on V_{bb} at V_{dd} = 1.2 V are shown in Fig. 9. By applying a reverse V_{bb}, V_{th} increased to above 0.6 V, and the *SS* decreased to less than 80 mV/decade. In contrast, by applying a forward back-gate bias of 1.2 V, V_{th} can be lowered by more than 0.3 V while keeping the *SS* small. In such a high forward bias, there is no increase in the substrate leakage currents.

As for conventional bulk structures, reverse biasing can be used to reduce the standby leakage after fabrication. However, this is less effective because both V_{th} variation and GIDL increases (Yasuda et al., 2007). In the SOTB scheme, GIDL is sufficiently suppressed by the intrinsic channel and the controlled L_{ov}, and forward V_{bb} is also effective in adjusting the V_{th} variation. The die-to-die compensation for the V_{th} of each chip is demonstrated in Fig. 10.
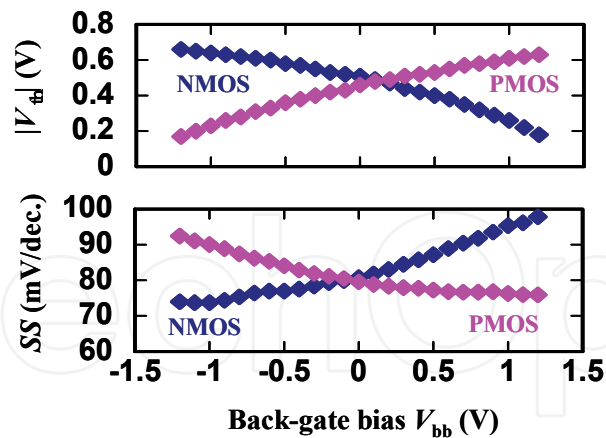
Fig. 9. Dependences of V_{th} and SS for a 50-nm-gate-length SOTB CMOSFET as a function of back-gate bias V_{bb} at V_{dd} = 1.2 V.

Each circle represents a 50-nm-gate-length NMOS of a chip. The open circles indicate the V_{th} distribution without V_{bb} control, and the closed circles indicate the distribution with V_{bb} control, that is, when the V_{bb} was adjusted for each transistor to approach the target V_{th}. The V_{bb} values range from -1.2 to 1.2 V, in 0.2-V increments. Without V_{bb} control, the range of V_{th} distributions is about 0.1 V due to size (gate length or layer thicknesses such as SOI) variations or channel dose fluctuations. The standard deviation σV_{th} with V_{bb} control was suppressed to 1/4 (case A) even with such a wide V_{bb} step. In addition, the typical V_{th} can be set arbitrarily within a range of 0.18 V (cases B and C), which is larger than the 0.1 V of the original V_{th} distribution, while keeping the variation suppressed. It is assumed, for instance, that setting the optimum V_{bb} according to the speed and the power of the chip will improve the yield.
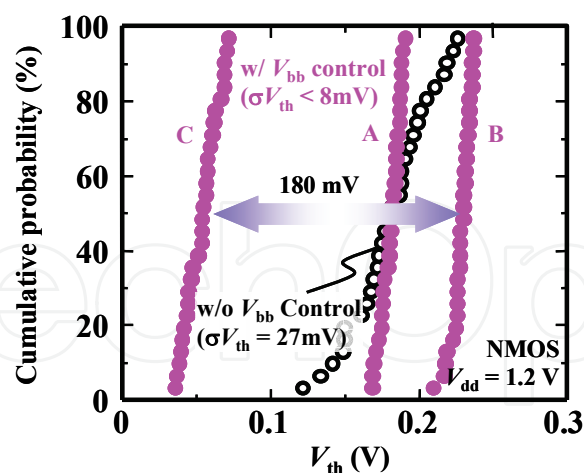

Fig. 10. V_{th} shift and variation reduction of Poly-Si gate SOTB NMOS using back-gate bias V_{bb} (V_{bb}: -1.2 < V_{bb} < 1.2 V, increments = 0.2 V).

4. Reduction of power consumption

The nominal V_{th} cumulative probability plot (not shown) of SOTB CMOSFETs indicates that the distribution is random and SCE is suppressed even down to 50 nm (Morita et al., 2008).

The Pelgrom plot is shown in Fig. 11. The slope of the plot, the Pelgrom coefficient A_{vt}, is 1.8 and 1.5 mVμm for NMOS and PMOS, respectively. These values are about half those of conventional bulk CMOSFETs of the same technology generation due to the intrinsic channel without halo implant. Impurities below the BOX layer have a small impact on the variability. The local component of variation is also plotted. To extract the local variation of V_{th}, the difference between the forward and the reverse measurement by exchanging the source and drain was used (Tanaka et al., 2000). It has already been confirmed that this method simply represents the local variation of adjusting pair transistors (Sugii et al., 2008). These results suggest the SOTB CMOSFET is robust in terms of variability.
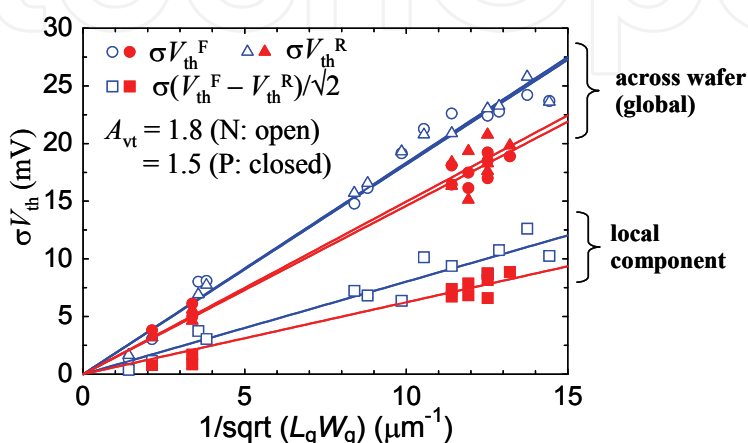

Fig. 11. Pelgrom plot of SOTB CMOSFETs for both global and local components.

Because static random access memory (SRAM) has been integrated in recent VLSI circuits with large capacities occupying large areas, reducing the power consumption of SRAMs is becoming increasingly important. Moreover, since the SRAM circuit is most sensitive to the local V_{th} variation, it is assumed that achieving low V_{dd} is most difficult with SRAM. Figure 12 plots the characteristics of 6T-SOTB SRAM cells 0.99 μm² in size. The static noise margins (SNM) of 0.357 V at V_{dd} = 1.2 V and 0.142 V at V_{dd} = 0.6 V indicate a much more stable operation in comparison with conventional bulk ones. The fail bit count (FBC) analysis indicated that the SOTB-SRAM can operate as low as 0.6 V, whereas the bulk SRAM with the same cell size operates at 1.1 V (Tsuchiya et al., 2009).
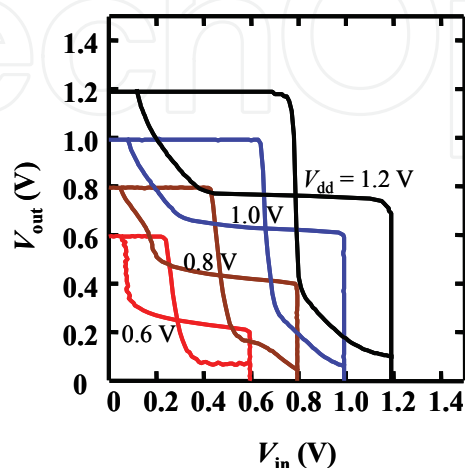

Fig. 12. Measured butterfly curves of 50-nm-gate-length SOTB SRAM cell.

The variability of SOTB CMOSFETs has a significant impact on standby power consumption. The total standby leakage of a conventional 6T-SRAM cell is roughly expressed as

$$I_{\text{standby}} = 3I_{\text{off}} + 2I_{\text{gate}} \tag{4}$$

where I_{gate} is the gate leakage when the gate node of a transistor is high. We calculated the standby leakage of an SRAM between SOTB and bulk devices, taking variability into account. When V_{th} decreases from a typical value (ideally at the minimum I_{d} point determined both by subthreshold and GIDL currents), I_{off} increases on the subthreshold slope of 80 mV/decade. On the other hand, I_{off} also increases with larger V_{th} because of the GIDL with a slope of 400 mV/decade. The summation of off-currents taking V_{th} distribution into account is expressed as

$$\Sigma I_{\text{off}} = \int P\,(\Delta V_{\text{th}}) \times I_{\text{off}}\,(\Delta V_{\text{th}}) \tag{5}$$

where P is a probability of V_{th} in the distribution, and ΔV_{th} is the deviation from the typical V_{th}. The σV_{th} of SOTB and bulk devices is 27 and 54 mV, respectively. I_{gate} is calculated as a constant without taking variability into account because its value is much smaller for LSTP applications, where J_{g} is 2×10^{-3} A/cm2. The integrated standby leakage of 1-Mbit SRAM is shown in Fig. 13. One typical I_{off} of SOTB devices is calculated as 10 pA/μm compared with bulk devices. The other typical I_{off} value of SOTB devices is 1 pA/μm. When the typical I_{off} = 10 pA/μm, the standby leakage of the SOTB device is 44% that of the bulk ones. This result indicates that reducing σV_{th} by half also reduces the standby leakage by half. Moreover, when the typical I_{off} of an SOTB device = 1 pA/μm, the standby leakage can be further reduced to 6%. In the case of I_{off} = 1 pA/μm, which indicates a lower on-state current, the driving performance can be boosted by using back-gate biasing in the SOTB technology.
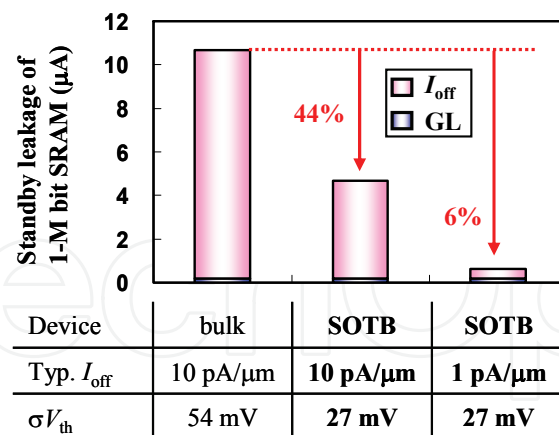
Device	bulk	SOTB	SOTB
Typ. I_{off}	10 pA/μm	10 pA/μm	1 pA/μm
σV_{th}	54 mV	27 mV	27 mV

Fig. 13. Estimated standby leakage of 1-Mbit SRAM taking V_{th} variability into account.

5. Conclusion

Recently, the scalability of CMOSFETs has become a topic of utmost importance. In SOTB technology, scalability can be pursued by reducing the SOI and BOX thicknesses. The minimum SOI thickness is considered to be 6 nm, after which the influence of the quantum effect or mobility degradation appears (Uchida et al., 2001). Given this value and

considering the thickness variation, the minimum gate length of the SOTB CMOSFET is expected to be about 20 nm while maintaining a small V_{th} variation (Sugii et al., 2009). In addition, the applicability of back-gate biasing is important. Even if the uniformity of transistors is not maintained, the characteristic variation can be eased by correcting V_{bb}.

In this chapter, it was shown that both operating voltage and standby power can be substantially reduced due to the low variability of the SOTB CMOSFET. This indicates that the power consumption of VLSI circuits can be drastically reduced. Moreover, when combined with V_{bb} control, it is possible to obtain the optimum power efficiency by flexibly changing V_{dd} and V_{th} to the operation situation. It is hoped that these flexible voltage controls will be applied to VLSI circuits in the future to meet the increasingly complex application demands.

6. Acknowledgements

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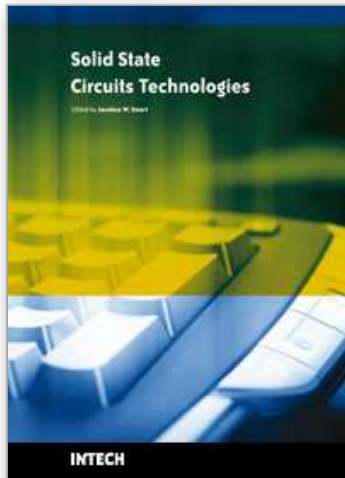
Solid State Circuits Technologies

Edited by Jacobus W. Swart

The evolution of solid-state circuit technology has a long history within a relatively short period of time. This technology has lead to the modern information society that connects us and tools, a large market, and many types of products and applications. The solid-state circuit technology continuously evolves via breakthroughs and improvements every year. This book is devoted to review and present novel approaches for some of the main issues involved in this exciting and vigorous technology. The book is composed of 22 chapters, written by authors coming from 30 different institutions located in 12 different countries throughout the Americas, Asia and Europe. Thus, reflecting the wide international contribution to the book. The broad range of subjects presented in the book offers a general overview of the main issues in modern solid-state circuit technology. Furthermore, the book offers an in depth analysis on specific subjects for specialists. We believe the book is of great scientific and educational value for many readers. I am profoundly indebted to the support provided by all of those involved in the work. First and foremost I would like to acknowledge and thank the authors who worked hard and generously agreed to share their results and knowledge. Second I would like to express my gratitude to the Intech team that invited me to edit the book and give me their full support and a fruitful experience while working together to combine this book.

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