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Statistical Prediction of Circuit Aging under Process Variations

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1. Introduction

With relentless scaling of CMOS technology, circuit timing uncertainty due to temporal degradation and static process variations poses a dramatic challenge to IC design (*International Technology Roadmap for Semiconductors*, 2008; Reddy et al., 2002; Nassif, 2001; Lin et al., 1998). The deterioration of circuit performance over time, i.e., aging, is usually caused by several physical mechanisms such as channel-hot-carrier (CHC), negative-bias-temperature-instability (NBTI), and time-dependent-dielectric-breakdown (TDDB) (Schroder & Babcock, 2003; Alam & Mahapatra, 2005; Wang et al., 2007; Vattikonda et al., 2006; Ogawa et al., 2003). Among these effects, NBTI is the leading mechanism that is responsible for the majority part of circuit aging (Kimizuka et al., 1999; Wang et al., 2007). In (Wang et al., 2007), the authors show that for 65nm technology, CHC degradation is much smaller than NBTI degradation, almost one order lower in the degradation magnitude. NBTI primarily increases the threshold voltage (V_{th}) of PMOS devices. Such parameters shift significantly affects circuit lifetime and performance (e.g., power, speed and failure rate), and in the worst case, may even result in a complete parametric failure of a system (Borkar, 2006; Alam & Mahapatra, 2005; Wang et al., 2007; Vattikonda et al., 2006; Bhardwaj et al., 2006; Kumar et al., 2006; Paul et al., 2006). To cope with this threat and guarantee circuit lifetime, it is critical to include NBTI into circuit analysis and adaptively develop design techniques to effectively mitigate its negative impact on performance.

For a VLSI design, an accurate prediction of circuit performance degradation under NBTI remains as a tremendous challenge. As shown in (Wang et al., 2007), NBTI has a strong dependence on dynamic operation conditions, such as supply voltage (V_{dd}), temperature (T) and input signal probability (α_s). Usually these parameters are not spatially or temporally uniform, but vary significantly from gate to gate and from time to time. Similar to the burn-in process, we may use high voltage and high temperature to guardband the worst case condition. However, the search for the worst case α_s is computationally inhibitive due to the extremely large space of signal probabilities for each input node. A practical method is proposed to predict the upper bound of each gate under all possible input α_ss (Agarwal et al., 2008).

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Besides these uncertainties, static process variation poses another challenge that leads to the variance of circuit aging. Fig. 1 illustrates an example that shows the statistical measurement of switching frequency and the leakage (*IDDQ*) of ring oscillators (ROs) before the reliability test. In this 65nm technology, more than 3X and 25% variability are observed in circuit leakage and the speed, respectively. These variabilities are attributed to statistical distributions of device parameters that are caused by the manufacturing process (Nassif, 2001). Examples include dopant concentration, channel length (L), oxide thickness (t_{ox}), etc. Their impact on device and circuit performance is usually investigated through a reduced set of device parameters – V_{th} is the most important one among them, as the interface between process and electrical studies. In (Liu et al., 2007), we have identified that the leading variation sources are L, V_{th} and carrier mobility (μ). By including the extracted variations of these three sources in the nominal model file, we are able to accurately predict the change of IV characteristics in all regions. Other variations, such as that in t_{ox}, are included into these variations (e.g., V_{th} is a function of t_{ox}) and indirectly affect device performance.

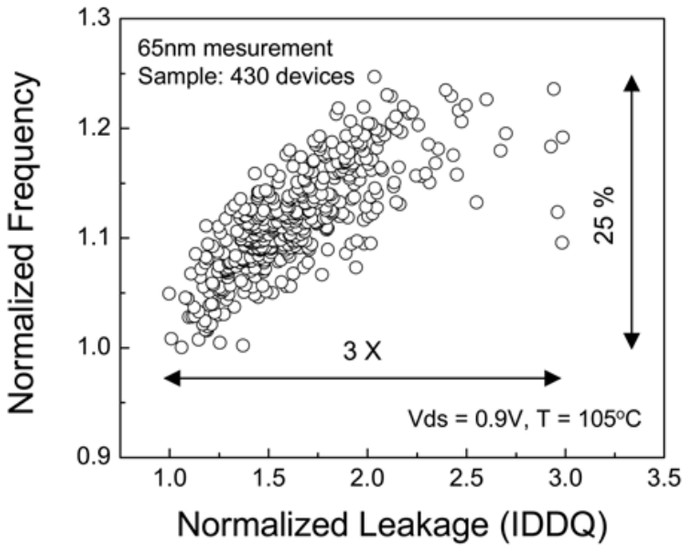

Fig. 1. Measured RO leakage and frequency variations before the stress.

Since NBTI effect has an exponential dependence of V_{th} (Wang et al., 2007; Alam & Mahapatra, 2005; Wang et al., 2007), circuit aging strongly interacts with process variations, significantly shifting both the mean and the variance of the circuit performance. By focusing on this primary variation source – V_{th}, we are therefore able to gain key insights and project the first-order trend. Other secondary process sources are neglected in this work. With the availability of more detailed data in the future, we will incorporate more sources. Fig. 2 shows the measured speed degradation from the same set of ROs as those in Fig. 1. Circuit performance and its variability not only depend on static process variations, but also change over the period of dynamic operation because of the effect of circuit aging (Schroder & Babcock, 2003; Wang et al., 2007). Therefore, accurate prediction of circuit performance distribution during its life time should consider the impact of static variations, primary reliability mechanisms, and more importantly, their interactions. This prediction is essential for designers to safely guardband the circuit for a sufficient life time. Otherwise, we have to either use an overly pessimistic bound, or resort to expensive stress tests in order to collect enough statistical information.

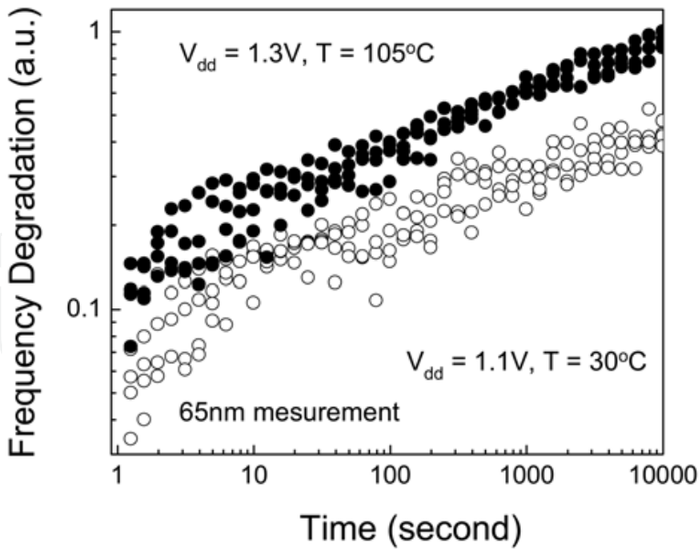

Fig. 2. Measured frequency degradation of a 11-stage ring oscillator under different stress conditions (four selected samples each condition).

A few works have been published in the literature to estimate the statistical variations in temporal NBTI degradation (Rauch, 2002; 2007; Rosa et al., 2006; Kang et al., 2007). Their assumption is the number of broken bonds in the channel is a Poisson random variable, and correspondingly V_{th} follows the Poisson distribution. With technology scaling, additional V_{th} variations, such as random dopant fluctuation and short channel effects, need to be considered. The measurement data show that the distribution of V_{th} variations follows the Gaussian distribution (Liu et al., 2007). In addition, the correlations between process variation and NBTI are ignored in previous work. In this work, we begin with the assumption that process variation induced V_{th} change is Gaussian random variable. We leverage compact models of transistor degradation and circuit performance to achieve accurate and efficient reliability prediction. Dynamic NBTI effect is incorporated into the analytical framework to account for the aging of circuit speed and the leakage (Schroder & Babcock, 2003; Wang et al., 2007). Based on our initial observation with the available data, the specific contributions and conclusions of this work include:

- A statistical predictive methodology of circuit aging is proposed. In this analytical approach, only five model parameters need to be extracted from fresh data (i.e., before the stress). With the initial information of the transistor and circuit topology, these models provide accurate prediction of circuit performance degradation and the variability.
- The degradation rate of circuit speed and its standard deviation follows a power law of 1/6. While the mean of circuit timing goes up with the stress time, the variance actually declines due to the interaction between NBTI effect and process variations. The degradation rate of both values is independent on the amount and the type of variations in the circuit.
- The mean and the standard deviation of logarithmic *IDDQ* reduce with the stress time as $t^{1/6}$, with the variance more sensitive to global variations.
- A hierarchical statistical aging analysis methodology is proposed to efficiently predict circuit aging under both process variations and operation uncertainties.

The outline of the paper is as follows: In Section 2, the statistical modeling for both transistor and circuit performance degradation is described, and the proposed models are comprehensively verified with silicon data from industrial 65nm technology, as well as SPICE simulation results. Section 3 presents a hierarchical statistical aging analysis methodology for circuit performance prediction. Finally Section 4 concludes this work.

2. Statistical modeling of circuit aging

NBTI is the dominant effect of circuit aging in advanced CMOS technology (Schroder & Babcock, 2003; Kimizuka et al., 1999). We propose a hierarchical solution to bridge the underlying device physics with efficient circuit analysis. Based on the reaction-diffusion mechanism, we developed the model of *Vth* shift under NBTI effect. In the presence of process variations and aging, using Gradual Change Approximation (GCA), this model is further expanded as a linear function of *Vth* shift to efficiently predict the performance degradation.

To characterize the change of circuit performance under the stress, the Alpha-power law based delay model and the leakage model are calibrated for a given gate. Under the condition that the amount of NBTI-induced V_{th} shift is much smaller than the nominal value of V_{th}, both models are simplified to extract the dependence of circuit performance to V_{th} change.

Finally, the gate-level models are integrated into various circuit paths to analytically predict the aging of path timing and the leakage. Both the mean value and the variance of these important metrics are derived as a function of static performance variability, the nominal sensitivity of circuit performance, and other operation conditions, such as supply voltage and temperature.

2.1 Gradual change approximation

NBTI manifests itself in a gradual increase in the magnitude of PMOS threshold voltage, resulting in the degradation of circuit performance over time. A set of publications have shown that NBTI is only pronounced in a long term, i.e., the performance degradation of transistors and circuits is a gradual aging process (Kumar et al., 2006; Wang et al., 2007). ΔV_{th} in different devices due to variation and NBTI is still a relative small portion compared to the nominal V_{th} value. Thus, when we derive the statistical degradation model, the first order Taylor expansion (i.e., linear expression) is applicable to transistor and circuit metrics, such as Equations (1) and (2), as well as gate delay and leakage analysis. This is the Gradual Change Approximation (GCA), which can be applied to simplify the following model derivations.

$$e^x = \sum_{n=0}^{\infty} \frac{x^n}{n!} = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \cdots \qquad \text{for all } x \tag{1}$$

$$(1+x)^p = \sum_{n=0}^{\infty} \binom{p}{n} x^n \qquad \text{for all } |x| < 1, \text{ and all complex } p \tag{2}$$

2.2 Transistor degradation model

NBTI occurs when a negative gate bias is applied to the PMOS devices and it has two phases: stress and recovery (Alam & Mahapatra, 2005; Wang et al., 2007). In stress phase, the

holes in the channel weaken the Si-H bonds, which results in the generation of the positive interface charges and hydrogen species. During recovery phase, the interface traps are annealed by the hydrogen species and thus, V_{th} degradation ($\Delta V_{th-nbti}$) is partially recovered.
Two main theories are proposed to interpret NBTI degradation: Reaction-Diffusion (RD) (Alam & Mahapatra, 2005; Alam et al., 2007; Krishnan et al., 2005) and hole Trapping/ Detrapping (T/DT) (Shen et al., 2006; Parthasarathy et al., 2006; Huard et al., 2006). R-D model naturally explains the long-term power law time exponent of NBTI (n ~1/6) (Alam et al., 2007; Wang et al., 2007; Bhardwaj et al., 2006). However, the experimental data obtained by using on-the-fly (OTF) measurement (Parthasarathy et al., 2006; Rangan et al., 2003), or ultra-fast (UF) measurement (Reisinger et al., 2006) show that the power law dependence with a time exponent of $n > 1/6$. R-D model cannot explain well the fast transient in the beginning of recovery of NBTI. Thus, we introduce an experimental term to capture the behavior of the fast response in recovery (Bhardwaj et al., 2006; Wang et al., 2007), and the long-term $\Delta V_{th-nbti}$ is given by,

$$\Delta V_{th-nbti} = \left(\sqrt{K_v^2 \cdot T_{clk} \cdot \alpha_s}/\left(1-\beta_t^{1/2n}\right)\right)^{2n} \tag{3}$$

$$\text{where} \qquad \beta_t = 1 - \frac{2\xi_1 \cdot t_e + \sqrt{\xi_2 \cdot C \cdot (1-\alpha_s) \cdot T_{clk}}}{2t_{ox} + \sqrt{C \cdot t}} \tag{4}$$

$$K_v = \left(\frac{q t_{ox}}{\epsilon_{ox}}\right)^3 K^2 C_{ox}(V_{gs} - V_{th})\sqrt{C} exp\left(\frac{2E_{ox}}{E_0}\right) \tag{5}$$

where T_{clk}, α_s, and n are clock period, input signal probability, and time exponential constant (1/6), respectively. K, ξ_1, ξ_2 and E_0 are fitting parameters. K_v describes the dependence of the bias voltage, T, t_{ox} and other technology parameters associated with NBTI degradation (Bhardwaj et al., 2006; Wang et al., 2007). For more details about the meaning and value of the parameters, please refer to (Bhardwaj et al., 2006; Wang et al., 2007). The dependence of NBTI effect on V_{th} (which is a parameter lumping many process details) is still under the debate. For instance, reference (Alam & Mahapatra, 2005) has discussed several possibilities. A general observation is that NBTI is strongly affected by the electric field. Under the stress condition, this field is proportional to $(V_{gs} - V_t)/t_{ox}$, which leads to our model. By so far, this model matches data from 180nm down to 45nm, making it a generic model to describe NBTI effect in technology scaling. We are further collecting data from multi-V_{th} technology at the same technology node, with the target to verify it with more process details. Fig. 3 verifies this model with one set of experimental data under different stress conditions. Besides this long term prediction model, both static and real time dynamic models are also available in (Bhardwaj et al., 2006; Wang et al., 2007). The models well capture NBTI recovery effect (Agarwal et al., 2008).
This model assumes nominal degradation without considering the statistical process variations. If there are global and local process variations, V_{th} in Equation (5) should be expressed as:

$$V_{th} = V_{th0} + \Delta V_{th-g} + \Delta V_{th-l} \tag{6}$$

where V_{th0} is the nominal threshold voltage, ΔV_{th-g} and ΔV_{th-l} represent the change of threshold voltage due to global and local variations, respectively. Equation (6) shows that

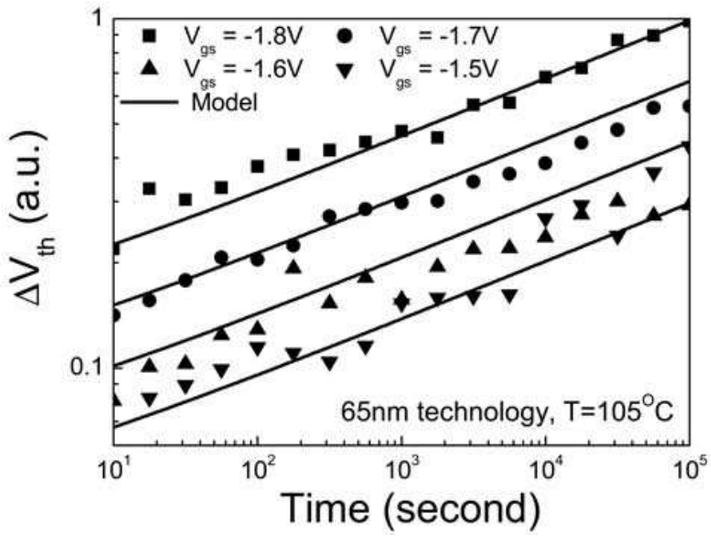

Fig. 3. Threshold voltage degradation under different stress conditions.

positive variation results in V_{th} increase, which correspondingly leads to smaller V_{th} degradation (according to Equations (3) and (5)), while negative variation results in larger V_{th} degradation. Fig. 4 shows V_{th} degradation over time for three different transistors. Due to process variations, Device 1 starts with a larger V_{th} and Device 3 starts with a smaller V_{th}. Substitute their fresh V_{th} to Equations (3) - (5), ΔV_{th} for these three devices is shown as Fig. 4. At the beginning, the difference in V_{th} degradation between Device 1 and Device 3 is 20.97%. With the increase of stress time, the difference becomes smaller and smaller. After 10^5s stress, it decreases to 15.57%. Such a compensation between process variations and aging is well captured by our model.

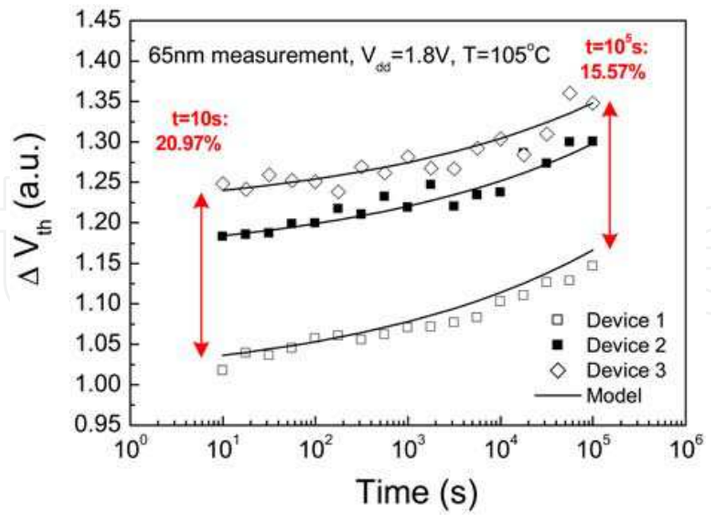

Fig. 4. Threshold voltage degradation over time for different devices

Since the degradation rate of different circuit paths is pronouncedly different due to different switching activities and circuit topologies (Wang et al., 2007), in (Agarwal et al., 2008), we introduce a Maximum Dynamic Stress (MDS) simulation technique with α_s

approaching to 1, which gives a simple and realistic estimation of the upper limit of gate delay degradation under dynamic NBTI. By using GCA and MDS described in (Agarwal et al., 2008), the long term prediction model is further simplified as a variation dependent model, i.e.,

$$\Delta V_{th-nbti} = A\left(1 - S_v(\Delta V_{th-g} + \Delta V_{th-l})\right)t^n \tag{7}$$

where the value of A depends on both technology parameters and operating conditions; S_v is the nominal sensitivity of NBTI degradation to V_{th} shift. In this work, $A = 2.5 \times 10^{-3} V/s^{1/6}$ and $S_v = 7V^{-1}$. Fig. 5 validates this simplified model (Equation (7)) with the long term predictive model (Equations (3) - (5)) under different process variations. Within $\pm 30mV$, it provides accurate prediction of V_{th} degradation.

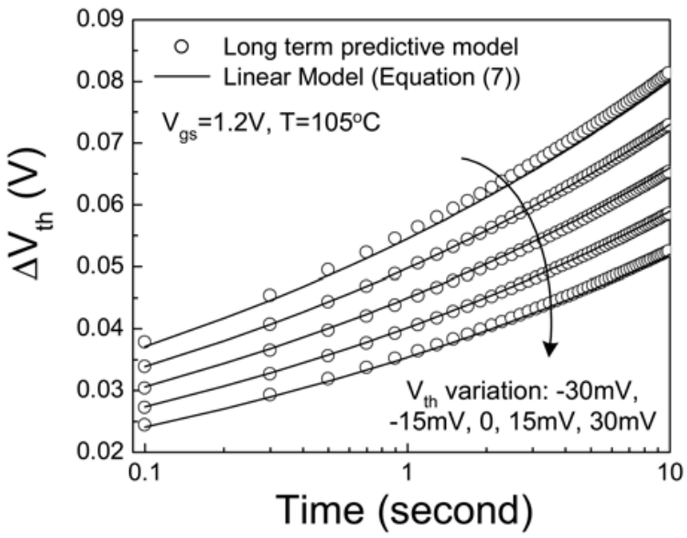

Fig. 5. Verification of process variation dependent NBTI model.

Besides V_{th} change, carrier mobility also degrades with increasing stress time (Wang et al., 2007). According to the universal effective mobility model, the dominant components of carrier scattering are phonon scattering, surface roughness scattering, and coulomb scattering. Aging effects induced interface charges result in stronger column scattering, which affects the carrier mobility mostly in low V_{gs} region. Because of this reason, mobility degradation is more important for analog circuit aging, but not for digital circuits. This behavior has been confirmed by the 65nm data (Wang et al., 2007). Thus, in this work, since the analysis is focused on digital circuit in which the devices operate at saturation region, the mobility degradation is ignored.

2.3 Gate delay degradation model

A widely used gate delay (T_{di}) model is based on the Alpha-power law that was proposed in (Sakurai & Newton, 1990),

$$T_{di} = (C_{li} V_{dd}) / (\beta_i (V_{dd} - V_{thi})^{\alpha}) \tag{8}$$

where C_{li} is the effective load capacitance of the gate; β_i is a parameter depending on gate size. Under both process variations and NBTI effect, V_{thi} of PMOS is given by

$$V_{thi} = V_{th0} + \Delta V_{thi} \tag{9}$$

$$\Delta V_{thi} = \Delta V_{thi-g} + \Delta V_{thi-l} + \Delta V_{thi-nbti} \tag{10}$$

Substituting V_{thi} into Equation (8) and using the GCA of $1/(1-x)_p \approx 1+ p \cdot x$ (for $x \ll 1$), we obtain:

$$T_{di} = \frac{C_{li}V_{dd}}{\beta_i(V_{dd} - V_{th0} - \Delta V_{thi})^{\alpha}} \approx \frac{C_{li}V_{dd}}{\beta_i(V_{dd} - V_{th0})^{\alpha}}\left(1 + \frac{\alpha \Delta V_{thi}}{(V_{dd} - V_{th0})}\right) \tag{11}$$

We define $T_{d0i} = (C_{li}V_{dd})/(\beta_i(V_{dd} - V_{th0})^{\alpha})$, which is the gate delay without process variations and NBTI degradation ($\Delta V_{thi} = 0$), and $S_{ti} = \alpha/(V_{dd} - V_{th0})$, which is the nominal sensitivity of gate delay to PMOS V_{th} shift. These two parameters rely on the process technology and the circuit structure. They can be conveniently extracted from SPICE simulation at the nominal condition. Thus, Equation (11) becomes:

$$T_{di} = T_{d0i}(1 + S_{ti}\Delta V_{thi}) \tag{12}$$

Substitute Equations (7) and (10) into (12),

$$T_{di} = T_{d0}(1 + S_{ti}(At^n + (1 - AS_v t^n)\Delta V_{thi-g} + (1 - AS_v t^n)\Delta V_{thi-l})) \tag{13}$$

Since 65nm measurement data show that the distribution of V_{th} variation is Gaussian distribution (Nassif, 2001; Liu et al., 2007), in this work, we assume ΔV_{thi-g} and ΔV_{thi-l} are Gaussian random variables. Their mean (μ_g and μ_l) are 0 and their standard deviations (σ_g and σ_l) depend on the manufacturing process (Borkar et al., 2003). Since gate delay is linearly proportional to the threshold voltage change, the probability distribution function (PDF) of gate delay also follows the normal distribution $N \sim (\mu_{T_{di}}, \sigma^2_{T_{di}})$.

At t = 0, $\Delta V_{th-nbti}$ = 0. Assuming global and local variations are uncorrelated random variables (Boning & Nassif, 2001), $\mu_{T_{di}}(0)$ and $\sigma^2_{T_{di}}(0)$ are given by:

$$\mu_{T_{di}}(0) = T_{d0i}, \quad \sigma_{T_{di}}(0) = T_{d0i}S_{ti}\sqrt{\sigma_g^2 + \sigma_l^2} \tag{14}$$

At $t > 0$, from Equation (13), we get

$$\mu_{T_{di}}(t) = \mu_{T_{di}}(0)(1 + AS_{ti}t^n), \quad \sigma_{T_{di}}(t) = \sigma_{T_{di}}(0)(1 - AS_v t^n) \tag{15}$$

Given the initial conditions of the process and timing information for the transistor and the gate, Equation (15) predicts the mean and standard deviation with increasing time. From these equations, we have four observations:

1. The mean of gate delay increases with the stress time, while the variance decreases. Since a lower-V_{th} transistor has a faster degradation rate and thus, larger V_{th} increase, this phenomenon compensates static process variations and reduces the variance during the stress period.
2. As the stress time increases, the aging of both mean and standard deviation follows the same power law of $t^{1/6}$.
3. The degradation rate of gate delay and its variance are independent of the amount and the type of variations.

4. The degradation rate is determined by the sensitivities to V_{th} shift. Process variations only affect the fresh variability, but not the degradation rate.

2.4 Circuit performance degradation model

2.4.1 Path timing

The PDF of a path comprising n gates corresponds to the linear combination of the n PDFs of gate delays. The mean and the variance of the path delay (T_d) are given by

$$\mu_{T_d} = \sum_{i}^{n} \mu_{T_{di}}, \quad \sigma_{T_d}^2 = \sum_{i}^{n}\sum_{j}^{n} \sigma_{T_{di}} \cdot \rho_{ij} \cdot \sigma_{T_{dj}} \tag{16}$$

where ρ_{ij} is the correlation coefficient between two gates. For the simplicity of the demonstration, we assume the inter-gate correlation is the same for all the gates, i.e., $\rho_{ij} = \rho$, while this methodology is general enough for all statistical conditions. Thus, the variance of path delay is derived as

$$\sigma_{T_d}^2 = \sum_{i}^{n}\sum_{j}^{n} \sigma_{T_{di}} \cdot \rho \cdot \sigma_{T_{dj}} + \sum_{i}^{n}(1-\rho) \cdot \sigma_{T_{di}}^2 \tag{17}$$

In the case of local variations, $\rho = 0$, i.e., the variations between two gates are uncorrelated. The case of $\rho = 1$ describes global variations, i.e., the variations between two gates are correlated. With both local and global variations, $\sigma_{T_d}^2$ is given by the linear combination of the variance of the local and global variations. Fig. 6 shows the delay distribution of ROs due to circuit aging. The distribution of gate delay becomes increasingly narrower under the stress as indicated by Equation (15).

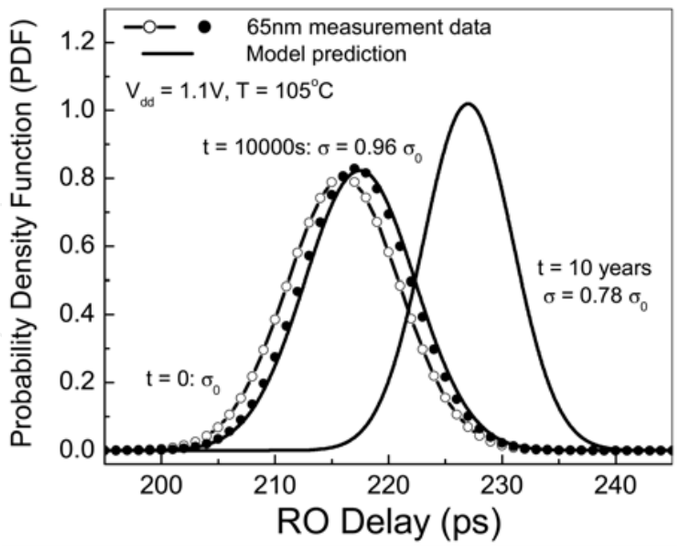

Fig. 6. The PDF's of 65nm RO delay during aging.

The proposed predictive methodology is generated for a path consisting of various types of gates. Fig. 7 shows such a circuit example. By stressing the path for different years, Fig. 8 compares the model prediction with SPICE simulation results of gate delay. Under different

types and amount of variations, the model provides accurate prediction of the mean and standard deviation.

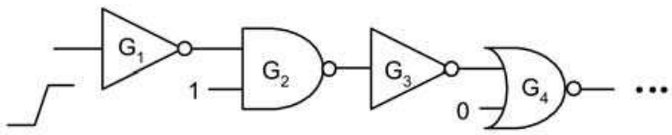

Fig. 7. Circuit example for path timing analysis.

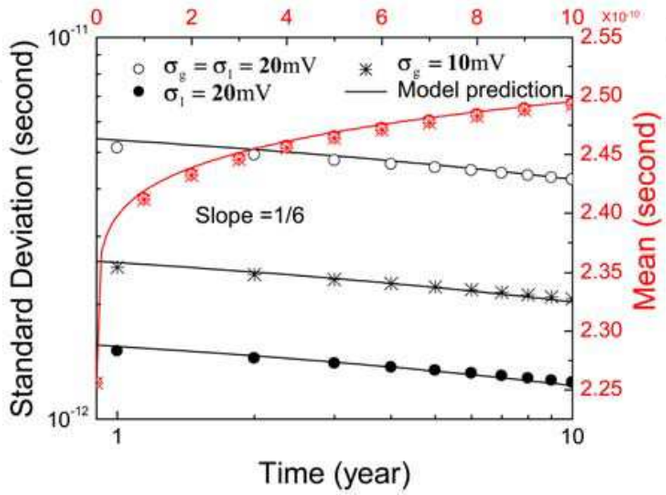

Fig. 8. The temporal increase of the mean and standard deviation of circuit speed (path is shown in Fig. 7).

2.4.2 Leakage

IDDQ of a circuit is defined as the total amount of leakage current at the standby. It has an exponential dependence on V_{th}:

$$IDDQ = \sum_{i}^{n} I_{0i} \cdot e^{-\frac{V_{thi}}{mv_T}} = \sum_{i}^{n} I_{0i} \cdot e^{-\frac{(V_{th0i}+\Delta V_{thi})}{mv_T}} \tag{18}$$

where $I_{0i} = \beta_i (m-1)(1-e^{-V_{ds}/v_T})$, m is the body effect coefficient and v_T is the thermal voltage (kT/q). Substitute Equation (10) into (18), we get

$$IDDQ = \sum_{i}^{n} I_{0i} e^{-\frac{V_{th0i}}{mv_T}} e^{-\frac{\Delta V_{thi-g}+\Delta V_{thi-l}+\Delta V_{thi-nbti}}{mv_T}}$$

$$= \sum_{i}^{n} IDDQi(0) e^{-\frac{\Delta V_{thi-g}+\Delta V_{thi-l}+\Delta V_{thi-nbti}}{mv_T}} \tag{19}$$

$IDDQi(0)$ is the gate leakage at t = 0, i.e., $\Delta V_{thi-g} = \Delta V_{thi-l} = \Delta V_{thi-nbti} = 0$. Taking the natural logarithms on both sides of Equation (19), we have

$$Ln(IDDQ) = Ln\left(\sum_{i}^{n} IDDQi(0) e^{-\frac{\Delta V_{thi-g}+\Delta V_{thi-l}+\Delta V_{thi-nbti}}{mv_T}} \right) \tag{20}$$

Under global variations, using Equation (7), Equation (20) becomes the following

$$Ln(IDDQ) = -\frac{At^n + (1 - AS_v t^n)\Delta V_{thi-g}}{mv_T} + Ln\left(\sum_i^n IDDQi(0)\right) \tag{21}$$

The mean and standard deviation of circuit leakage are

$$\mu_{Ln(IDDQ)}(t) = \mu_{Ln(IDDQ)}(0) - A \cdot t^n / (mv_T) \tag{22}$$

$$\sigma_{Ln(IDDQ)}(t) = (1 - AS_v t^n)/(mv_T) \cdot \sigma_g \tag{23}$$

where $\mu_{Ln(IDDQ)}(0) = Ln\left(\sum_i^n IDDQi(0)\right)$

Under local variations, Equation (20) is approximated as

$$\begin{aligned} Ln(IDDQ) &\approx Ln\left(e^{-\frac{At^n}{mv_T}} e^{-\frac{(1-AS_v t^n)\Delta V_{thi-l}}{(mv_T)\cdot\eta}} \sum_i^n IDDQi(0)\right) \\ &= -\frac{At^n}{mv_T} + \frac{(1 - AS_v t^n)\Delta V_{thi-l}}{(mv_T)\cdot\eta} + Ln\left(\sum_i^n IDDQi(0)\right) \end{aligned} \tag{24}$$

where η has the value between 0 and 1, depending on the circuit structure. The mean and standard deviation of circuit leakage are

$$\mu_{Ln(IDDQ)}(t) = \mu_{Ln(IDDQ)}(0) - A \cdot t^n / (mv_T) \tag{25}$$

$$\sigma_{Ln(IDDQ)}(t) = (1 - AS_v t^n)/(mv_T) \cdot (\sigma_l / \eta) \tag{26}$$

Akin to path timing, logarithmic *IDDQ* has the same time dependence under either global or local variation. Their impact is only different by a factor of η, which is derived from the circuit structure. Fig. 9 shows that the logarithmic mean and the standard deviation degradation of leakage current follow the power law of $t^{1/6}$. The mean is relatively independent of the type of variations, while standard deviation is more sensitive to the global variation.

3. Statistical aging analysis

The analysis above generates the statistics of each gate under the aging effect. In reality, the distributions of logic gates in a circuit are correlated depending on their statistical properties. To obtain the information of path timing degradation, we can incorporate statistical timing analysis techniques to handle the correlation. In this section, we propose a hierarchical method to extract related model parameters and prepare the framework for the integration.

3.1 Statistical static timing analysis flow

Fig. 10 shows the statistical circuit performance analysis flow which is used to predict the circuit performance. This flow incorporates conventional static timing analysis with the statistical properties of the circuit and the process technology. The primary components include:

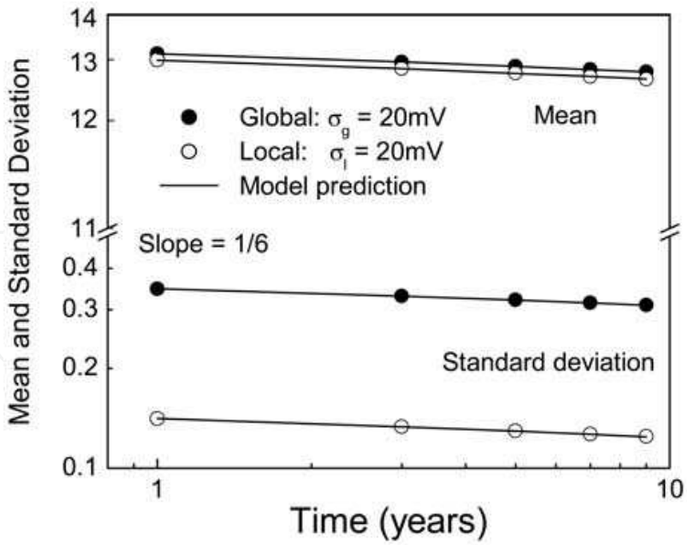

Fig. 9. The mean and standard deviation degradation of leakage.

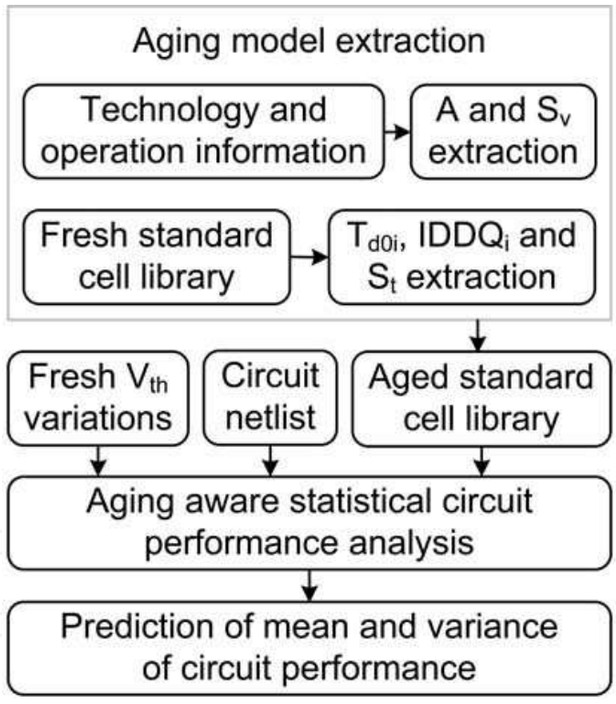

Fig. 10. Statistical circuit performance analysis flow.

1. Model parameter extraction. Given technology and operating condition information, A and S_v are extracted. Given standard cell performance library, T_{d0i}, $IDDQ_i$ and S_t are extracted. For more details about parameter extraction, please refer to (Wang et al., 2007) and Section 3.2.1.
2. Substituting all the parameters into Equations (13), (21) and (24), we obtain the aged standard cell performance library. The cell timing and leakage are functions of transistor global and local V_{th} variations and stress time.

3. Generating two statistical distribution of transistor fresh V_{th} variations, one is for global variation and the other is for local variation. Their means are 0, and standard deviations are determined by the manufacturing process.
4. Given circuit netlist, random assign V_{th} variations from the generated distribution to each transistor. With specified V_{th} variations, the cell timing and leakage of the aged standard cell library are only function of stress time.
5. Given stress time, using circuit performance analyzer with the aged standard cell library, we get the circuit performance degradation. For example, we want to do timing analysis for given circuit. Since the aged library provides each cell timing information, the path timing is obtained by adding up all the individual cell timings in the path. We can do leakage analysis in the same way.
6. For circuit performance distribution prediction, given initial V_{th} variation distribution, Equations (16), (17), (22), (23), (25), (26) directly give the mean and standard derivation of circuit performance distribution.

3.2 Model prediction and silicon validation

3.2.1 Model parameter extraction

In order to accurately predict the circuit performance degradation, there are five parameters need to be characterized at $t = 0$, including: A, S_v, S_t, T_{d0i} and $IDDQi$.

A: Parameter of long term V_{th} degradation under nominal conditions. Its value is extracted from Equations (3) - (5), with the dependence of temperatures, V_{dd}, and switching activity.

S_v: the sensitivity of NBTI-induced transistor degradation to the nominal value of V_{th}.

S_t: the sensitivity of gate delay to PMOS V_{th} shift.

T_{d0i}: nominal gate delay, without V_{th} variation and aging.

$IDDQi$: nominal gate leakage, without V_{th} variation and aging.

Note these parameters are all extracted from the nominal condition, but not affected by process variations. Variations only change the distribution of T_d and $IDDQ$, which can be obtained from the statistics at $t = 0$ (i.e., before the stress). During the stress, the interaction between variability and reliability follows the prediction of our new models. These statistical reliability models improve the predictability in the design stage, avoiding expensive reliability test at the circuit level.

3.2.2 Test chip and measurement

To validate the statistical models for the circuit performance, an inverter ring oscillator was designed as the prototype circuit (Reddy et al., 2002). Fig. 11 shows the simplified schematic of the ring oscillator. The channel length of the transistors in the ring oscillator is drawn at the minimum design rule. There is a NAND gate that allows the RO oscillation enable/disable (OE pin). When the oscillation is disabled, i.e., OE = 0V, IDDQ is measured through V_{RING}.

When the oscillation is enabled, i.e., OE = V_{dd}, the RO oscillates at full speed (several GHz) and Ring Oscillator Frequency (Fosc) is measured periodically without any interruptions. Similar as the on-the-fly measurement at the device level, this dynamic stress measurement is nonstop. In this work, the ROs are stressed under various supply voltage and temperature conditions. The temperature was the same for both stress and measurement and no electrical stress was applied until the temperature was at the proper value.

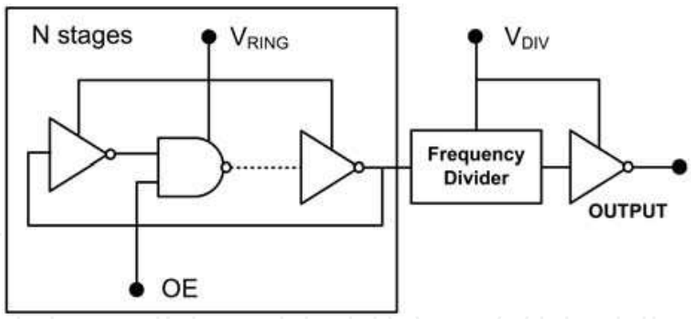

Fig. 11. Simplified schematic of inverter ring oscillator circuit. Oscillation is disabled by grounding the Oscillation Enable (OE) pin.

3.2.3 Model validation with silicon data

The proposed statistical model is verified by 65nm technology available silicon data under a few operating conditions. Fig. 12 shows the delay degradation of ROs. The dots present the mean changes; the error bars are scaled delay distribution of the sample circuits; and the lines are the model predictions. While the mean value increases as $t^{1/6}$, as a signature of the dominance of NBTI effect in circuit aging, the distribution declines with stress time. Fig. 13 evaluates the change of both the active current (*IDDA*), and the leakage current (*IDDQ*). Since $IDDA \approx CV/f$, for given switching frequency, *IDDA* is easily extracted. Our predictive models only require the sensitivities of transistor and circuit aging, as well as the statistics before the stress. Then the degradation of circuit performance is fully predicted toward the end of the life time.

3.3 Simulation setup of circuit benchmarks

The statistical aging analysis has been implemented in C to predict the circuit performance degradation of ISCAS85, 89 and ITC99 benchmark circuits (, n.d.; *ITC99 Benchmark*, n.d.). We

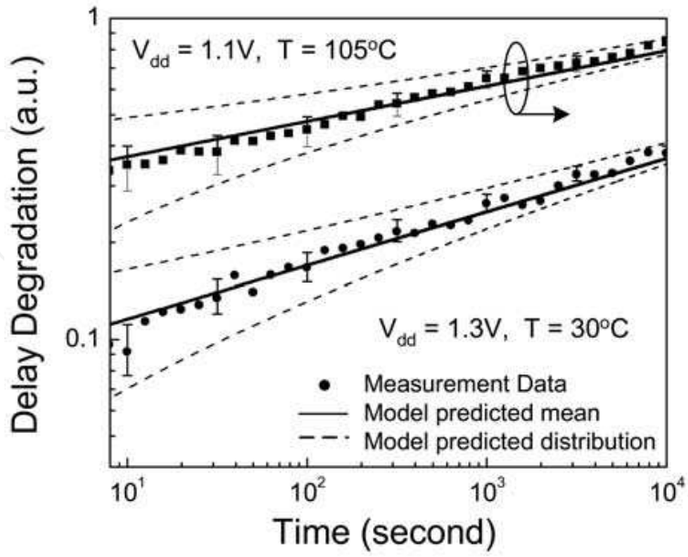

Fig. 12. Delay degradation of ROs under various stress conditions (four selected samples each condition).

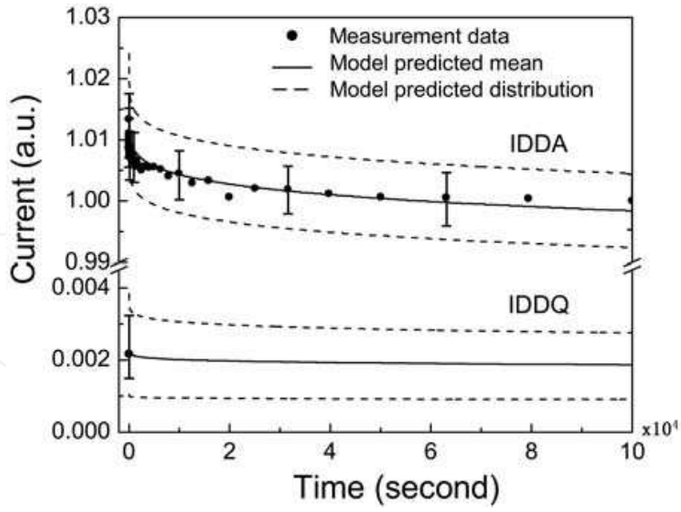

Fig. 13. The prediction of *IDDA* and *IDDQ* degradation.

obtain an aging aware library by running SPICE simulation using PTM 65nm technology (Zhao & Cao, 2006). This library consists of 5 different cells: INVERTER, 2 input NAND, 3 input NAND, 2 input NOR, 3 input NOR. The benchmark circuits in the BLIF format are synthesized by SIS (E. M. Sentovich, K. J. Singh, L. Lavagno, C. Moon, R. Murgai, A. Saldanha, H. Savoj, P. R. Stephan, and R. K. Brayton & Sangiovanni-Vincentelli, 1992) using this standard library. Random local and global variations are generated from a Gaussian distribution with mean 0 and standard deviation which is determined by the manufacturing process. The delay of each gate is calculated at time = 0 (with the variations) and after 10 years (with variations and NBTI degradation) using the aging aware library. Timing analysis is then performed, and the path delay for each path is calculated as the sum of the individual gate delays. After the run, the path with the maximum delay is identified as the critical path in the design.

3.4 Results and discussions

Figures 14 and 15 show the path delay distribution under both NBTI effect and process variation with time increasing. From these two figures, it can be seen that the mean of the path delay increases, while the standard deviation of the path delay decreases. Both of them follows the power law dependence of $t^{1/6}$. As shown in the figure, at t = 0, the delay difference between maximum and minimum is 10.18%, while after 10 years stress, it reduces to 5.29%. The Path delay degradation caused by NBTI effect for 10 years stress is 14.06%, which is more than the delay difference caused by process variations at t = 0. Thus, for the circuit designers, it is critical to consider both NBTI effect and process variation at the early design stage.

Table 1 further shows the simulation results for different benchmark circuits at *Time* = 0 and *Time* = 10 years. For a given circuit, *Path* represents the number of the total path in the circuit. T_{d0} and T_{d10} are the critical path delay of the circuit without process variations at *Time* =0 and *Time* = 10 years, respectively. The *Max*, *Mean* and *Min* columns correspond to the maximum, mean and minimum of the sets of the critical path delay under different simulation iteration. Δ is the delay difference between maximum and minimum. Δ_{nbti} is the NBTI-induce path delay degradation. *m* indicates the margin need to be add during the circuit design stage.

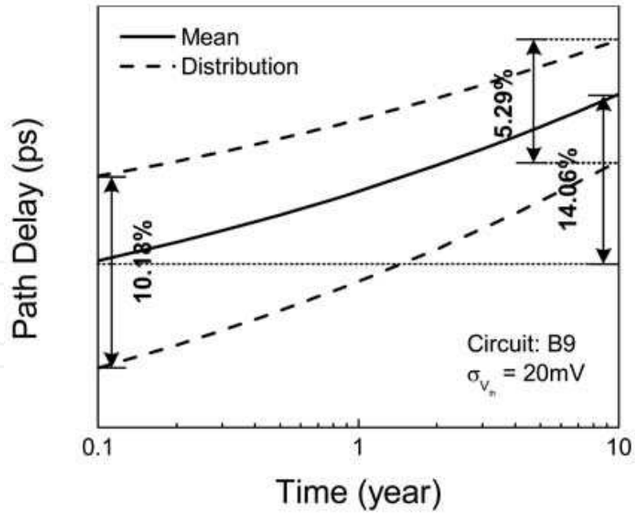

Fig. 14. Path delay mean change under both NBTI effect and process variations.

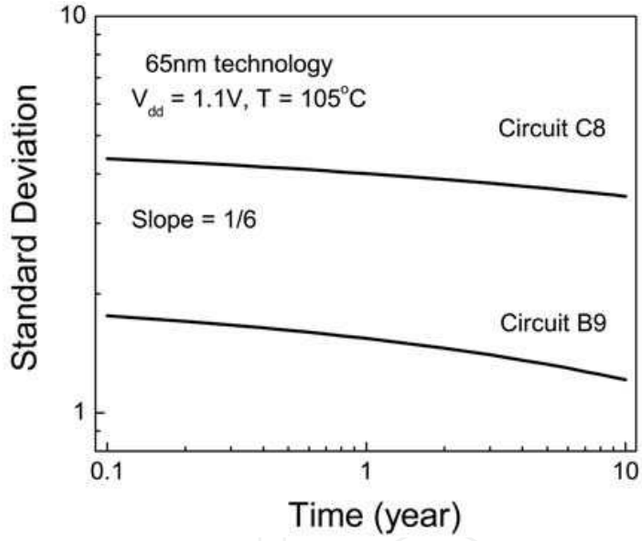

Fig. 15. Path delay standard deviation change under both NBTI effect and process variations.

Based on the simulation results of Table 1, we have three observations.

1. For most circuits, NBTI-induced delay degradation is comparable or larger than the process variations-induced delay difference. For example, circuit K2, after 10 years stress, NBTI-induced delay degradation is 15.65%, while the delay difference caused by process variation at *Time* = 0 is 13.22%. Thus, for circuit designers, it is necessary to add a guardband for NBTI in addition to guardband for process variations.
2. The impact of process variations on circuit delay strongly depends on the circuit structure. For instance, at *Time* = 0, process variation-induced delay difference for circuit Frg2 is 33.09%, while it is 4.97% for circuit Apex6. This effect is seen at *Time* = 10 years also.
3. The mean of the circuit delay increases with time, while the standard deviation decreases. Both of them follow the NBTI power law of $t^{1/6}$ and are independent of process variations (Fig. 14 and Fig. 15).

Circuit	Path	$Time = 0(ps)$					$Time = 10years(ps)$					$\Delta_{nbti}(\%)$	$m(\%)$
		$\sigma_l = 0$	$\sigma_l = 20mV$				$\sigma_l = 0$	$\sigma_l = 20mV$					
		T_{d0}	Max	$Mean$	Min	$\Delta(\%)$	T_{d10}	Max	$Mean$	Min	$\Delta(\%)$		
k2	10404	44458.02	47136.9	44435.39	41261.71	13.22	51416.18	52806.87	51404.44	49756.88	6.86	15.65	18.78
des	99845	34743.06	36887.09	34850.87	33244.59	10.48	39558.86	40568.06	39552.43	38624.65	5.59	13.86	16.77
b9	206	144.61	152.49	145.45	137.76	10.18	164.94	169.03	165.29	161.39	5.29	14.06	16.89
c8	201	227.79	240.24	227.78	216.57	10.39	263.04	269.48	263.02	256.75	5.59	15.47	18.30
comp	2016	4349.09	4452.62	4347.67	4326.27	2.91	4960.90	5014.65	4960.15	4902.26	2.58	14.07	15.30
frg2	4792	1438.80	1859.83	1588.31	1383.74	33.09	1652.40	2006.68	1897.89	1661.26	24.01	14.85	39.47
term1	649	1710.81	1786.63	1712.73	1630.49	9.13	1968.15	2007.51	1968.98	1926.45	4.74	15.04	17.34
apex6	1499	991.08	1016.69	991.31	967.41	4.97	1136.71	1150.01	1136.82	1124.43	2.58	14.69	16.04
count	368	827.46	855.96	827.62	799.14	6.87	948.16	962.96	948.25	933.46	3.56	14.59	16.38
example2	1307	443.47	467.57	445.37	428.27	8.86	505.71	518.22	506.62	497.83	4.60	14.04	16.86
f51m	174	342.17	359.84	342.11	324.35	10.37	391.52	400.69	391.49	382.26	5.38	14.42	17.10
frg1	127	785.78	805.38	786.00	763.64	5.31	900.42	910.59	900.50	888.93	2.76	14.59	15.89
lal	188	160.47	176.76	160.92	149.43	17.03	185.74	194.19	185.80	178.34	9.88	15.74	21.01
ldd	447	619.40	638.88	620.29	598.31	6.55	709.44	719.53	709.90	698.49	3.40	14.54	16.17
mux	189	1074.41	1112.05	1075.01	1033.14	7.34	1236.53	1256.07	1236.84	1215.11	3.81	15.09	16.91

Table 1. Simulation results for ISCAS and ITC99 circuit benchmark

By integrating the gate-based dynamic stress bound and process variation prediction model into circuit timing analysis, we verify that our hierarchical method provide a safe and tight bound of circuit timing degradation. Fig. 16 is the netlist of benchmark circuit C17. Fig. 17 shows the delay distribution of circuit C17 under various input vectors and process variations. As shown in the figure, the proposed method provides a safe and tight bound in the estimation of the circuit timing degradation, which helps to improve design predictability and avoid pessimistic guardbanding under NBTI effect.

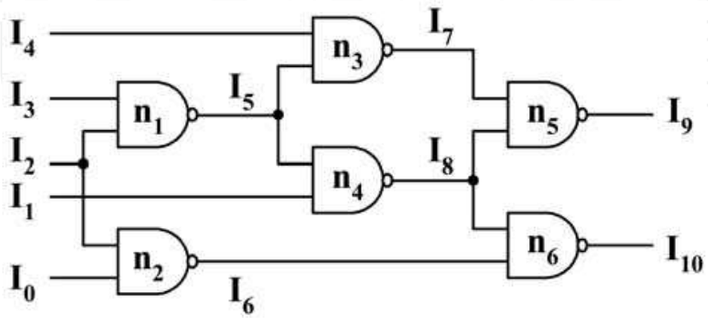

Fig. 16. Circuit C17 netlist.

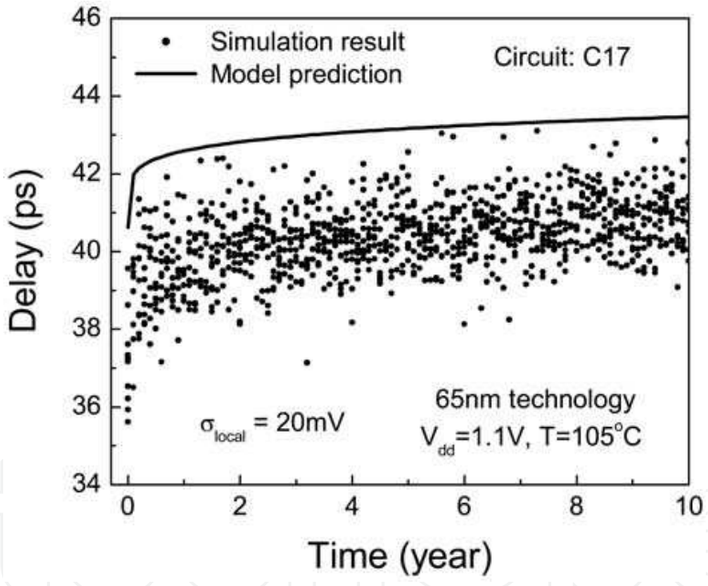

Fig. 17. Delay distribution of circuit C17 with various input vectors and process variations.

3.5 Impact of statistical variations on SRAM

The six transistor SRAM (6T SRAM) design is highly sensitive to process variations, especially local random variations. The mismatch between neighboring transistors reduces the cell Static Noise Margin (SNM) (Krishnan et al., 2006; Lin et al., 2006; Rosa et al., 2006). The impact of statistical variations on SRAM SNM is mainly divided into Read, Write, and Hold stability. Under the NBTI effect, a weaker PMOS transistor increases Read failures, but improves the Write operation (Krishnan et al., 2006; Lin et al., 2006). Fig. 18 shows the PDF of 6T SRAM Read noise margin during the aging. In the SRAM cell, only one side of PMOS

is stressed (i.e., with the gate biased at the ground), and the PMOS in the other side remains in the recovery. The mismatch in the stress mode reduces Read noise margin on one side, with no impact on the other side. As shown in Fig. 18, the mean value of Read noise margin decreases with longer aging time. Since Read SNM is determined only by the stressed PMOS side, NBTI induced SNM degradation is not cancelled out between stressed PMOS side and unstressed PMOS side. Therefore, the tail of Read SNM is determined by the stressed PMOS side. This behavior is different from the aging effect in a logic path, where random variability in each stage is averaged in the path timing. Further studies on statistical aging modeling are needed to predict the nonlinear behavior in SRAM.

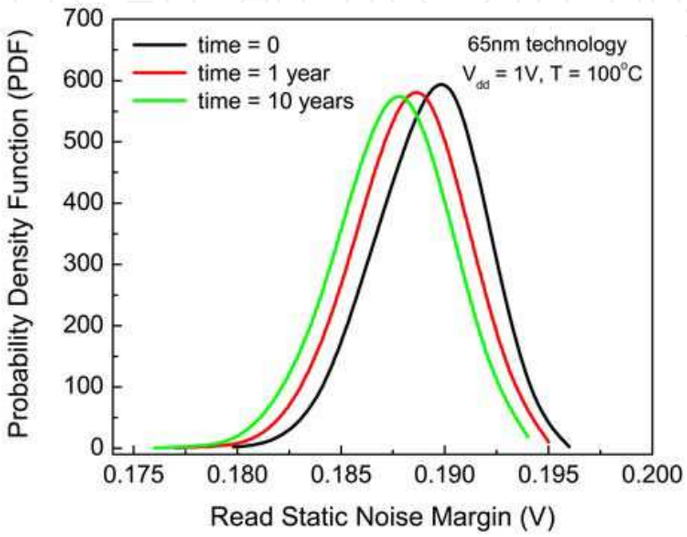

Fig. 18. The probability density function of SRAM read noise margin during aging.

4. Conclusions

In this work, a statistical methodology is developed to predict circuit performance degradation under both NBTI effect and process variations. These analytical solutions reveal that the degradation rate and its standard deviation are independent on the type and the amount of process variations. In order to predict the mean and the variance of circuit aging, only the characteristics of transistor degradation and circuit performance sensitivity to aged parameters are required. The aging of circuit speed and *IDDQ* shows a power law dependence on the stress time, as an evidence of the dominance of NBTI effect. The proposed method is implemented into SPICE simulation and timing analysis tools. With verification with 65nm silicon data, it supports statistical aging analysis in standard design flow, improving design predictability and helping avoid pessimistic guardbanding under the increasingly severe aging effect. We are collecting a larger volume of statistical data to further verify these conclusions.

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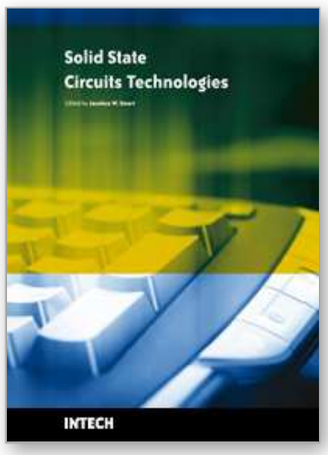

Solid State Circuits Technologies

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The evolution of solid-state circuit technology has a long history within a relatively short period of time. This technology has lead to the modern information society that connects us and tools, a large market, and many types of products and applications. The solid-state circuit technology continuously evolves via breakthroughs and improvements every year. This book is devoted to review and present novel approaches for some of the main issues involved in this exciting and vigorous technology. The book is composed of 22 chapters, written by authors coming from 30 different institutions located in 12 different countries throughout the Americas, Asia and Europe. Thus, reflecting the wide international contribution to the book. The broad range of subjects presented in the book offers a general overview of the main issues in modern solid-state circuit technology. Furthermore, the book offers an in depth analysis on specific subjects for specialists. We believe the book is of great scientific and educational value for many readers. I am profoundly indebted to the support provided by all of those involved in the work. First and foremost I would like to acknowledge and thank the authors who worked hard and generously agreed to share their results and knowledge. Second I would like to express my gratitude to the Intech team that invited me to edit the book and give me their full support and a fruitful experience while working together to combine this book.

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