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Advances in RFID Components Design: Integrated Circuits

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1. Introduction

Many RFID Components are either discrete components or integrated circuits components. With high demand and huge RFID market in supply and chain management, more RFID systems will employ integrated circuit components. This is due to cost competitiveness in using integrated circuit components. Understanding of these advanced components is therefore essential for the development of advanced RFID system.

This chapter emphasizes on the practical design of advanced RFID components namely the tag and the reader. This chapter discusses the design methodology of integrated circuit. The technology such as Silicon Bipolar and Silicon CMOS are studied in this chapter; the focus is on understanding the advantages and disadvantages of using these technologies for the design of advanced RFID components. The architecture or circuit topology of reader and tag are also thoroughly discussed; the integration of features which normally reduces the number of discrete components is the focus of this topic. The circuit technique in designing the tag and reader is studied and analyzed. The current research trend in RFID integrated circuit is more on reader than tag. SiGe BiCMOS (Chiu et al., 2007), 0.18 μm CMOS (Wang et al., 2007, Khannur et al., 2008) are amoung technologies used in the latest reader resarch and product. The measurement methodology of advanced RFID components is also discussed in the last topic. Overall this chapter provides basic knowledge to the readers for further research in RFID integrated circuits.

The understanding in advances of RFID components design, namely the technology, design techniques and test enables one to pursue in effective design of the state of the art RFID systems.

2. Design methodology of integrated circuit

RFID System consists of two main hardware components, RFID tags or transponder and RFID readers or receiver. Both components have analog and digital circuitry. The reader would have more complex digital circuitry than tag. Fig. 1 shows integrated circuit (IC) design flow which can be used in designing both components.

Specification: In all IC designs, the first step is to identify the specification or requirement. Price or cost is normally considered at this stage as well.
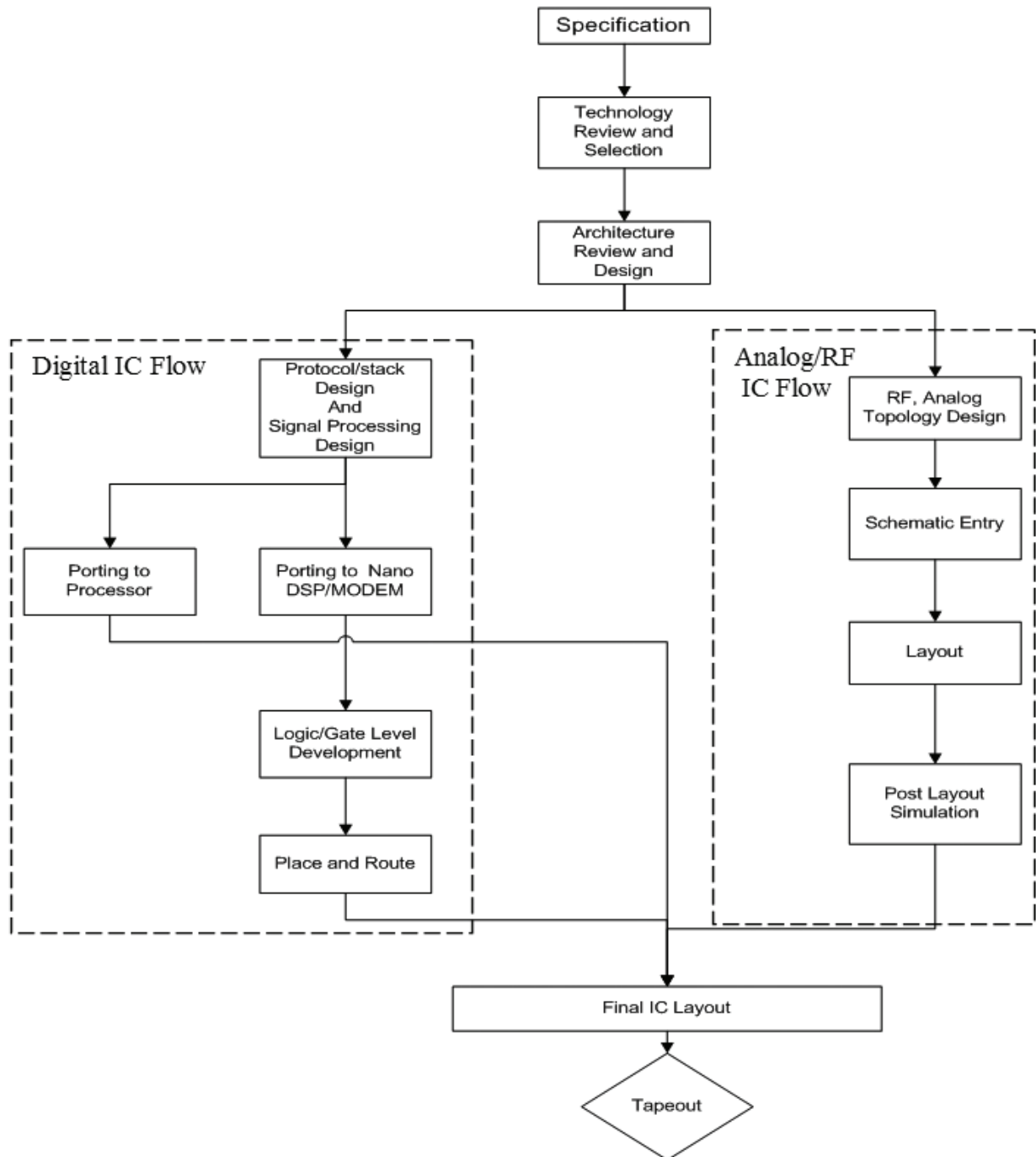
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Fig. 1. IC design flow

Technology Review and Selection: Silicon, GaAs or Silicon on Insulator (SOI) is decided based on its capability to meet the requirement and specification.

Architecture Review and Design: To review the suitable design architecture which can meet both selected technology and specification.

Protocol/stack Design and Signal Processing Design: Flow of state diagram development, Signal processing architecture design, Matlab simulation.

Porting to Processor: Port the program to processor/microcontroller such as ARM (for Reader), to Finite State Machine or simple general purpose process, 6502 compatible (for Tag) (De Vita & Iannaccone, 2004).

Porting to Nano DSP/MODEM: Conversion of Numerical model or state diagram to hardware language. The hardware language such as Verilog or VHDL is normally used at this stage.

Logic/Gate Level Development: Conversion of the hardware language to logic level (standard cell) by using EDA tools such as design compiler. Behavioural language such as Verilog or VHDL is normally used at this stage.

Place and Route: Conversion of standard cell to layout. A synthesizer is used at this stage.

RF, Analog topology Design: Topologies of RF and analog circuits are decided and designed.

Schematic Entry: Applying the schematic design using EDA tools and simulation or verification is made to verify the performance against the specification.

Layout: To design the mask for Analog and RF IC.

Post Layout Simulation: Simulation is done together with parasitic components which are extracted from the layout.

Final IC layout: To design or combine masks for both Analog, RF and digital IC

Tapeout: The mask design is sent to mask shop and later wafer fab or foundry for IC fabrication.

3. Technology

There are at least two main figure of merit parameters which characterize technology. They are transconductance, g_m and transition frequency, f_T. Equation (1) is basic transconductance formula, (2) is f_T of NPN Bipolar Transistor.

g_m is proportional to the voltage gain, high voltage gain is required for amplifier block, which is an important block for RF and analog circuit. For CMOS device, current has to be increased in order to increase g_m. f_T is the frequency where current gain is unity, high frequency RFID IC requires high f_T device which is normally ten times of the operational frequency.

$$g_m = \frac{I_{OUT}}{V_{IN}} \tag{1}$$

Where I_{OUT} is output current of device, V_{IN} is input voltage to the device.

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)} \tag{2}$$

Where C_π is parasitic capacitance between base and emitter, C_μ is parasitic capacitance between collector and base.

3.1 Bipolar

From Fig. 2, NPN Bipolar transistor, is not a symmetrical device, this can been seen from the difference of doping level of emitter and collector. Buried layer is used to reduce the collector resistance. This will make RFID IC design more complex, where collector and emitter cannot be swapped. The scaling of Bipolar technology is not aggresive as CMOS technology (Semiconductor Industry Association, 1997). These factors have hindered the use of Bipolar technology for RFID tag where simple design is normally chosen.
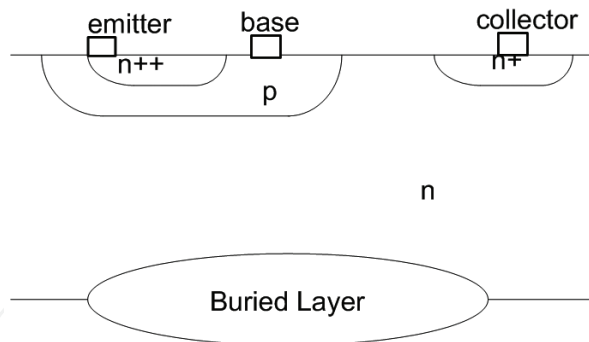
Fig. 2. Cross Section of NPN Bipolar Transistor

$$I_{OUT} = I_s \exp(\frac{V_{BE}}{V_T}) \qquad (3)$$

Equation (3) shows current equation of NPN Bipolar transistor, where I_S is saturation current, V_T is thermal voltage and V_{BE} is voltage between base and emitter . By replacing (3) into (1), Transconductance of NPN Bipolar transistor is therefore,

$$g_m = \frac{I_{out}}{V_T} \qquad (4)$$

Where $V_T = \frac{kT}{q}$, k is Boltzmann's constant and T is temperature in Kelvin and q is a unit electron charge. At room temperature, V_T = 25 mV. Replace (4) into (2) yields $f_T = \frac{I_{OUT}}{V_T 2\pi(C_\pi + C_\mu)}$.

3.2 CMOS
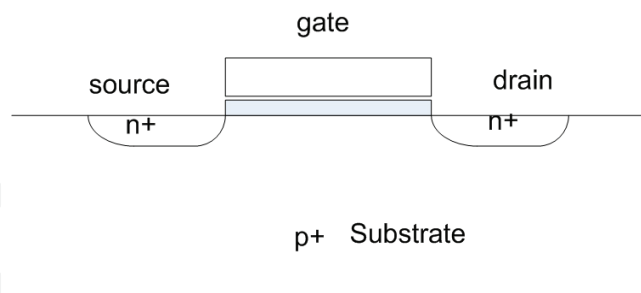
Fig. 3. NMOS Cross Section

From Fig. 3, NMOS device is a symmetrical device, this will ensure easier design and integration. The scaling of CMOS technology is aggressive and straight forward (Semiconductor Industry Association, 1997).

$$I_d = k'\frac{W}{2L}(V_{gs} - V_T)^2 \qquad (5)$$

Equation (5) is drain current equation of NMOS device, where W is channel width, L is channel length, V_T is threshold voltage and k' is transconductance parameter. Transconductance for NMOS is

$$g_m = \frac{2I_d}{V_{gs} - V_T} \tag{6}$$

V_{gs}-V_T is normally in the range of hundreds millivolt.

From (6) and (4), bipolar devices tend to have higher g_m and f_T. Smaller dimension of CMOS technology would have almost similar f_T as Bipolar technology. Smaller dimension of CMOS technology is usually more expensive than Bipolar technology. Equation (7) is f_T of CMOS transistor.

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{7}$$

Where C_{gs} is parasitic capacitance between gate and source, C_{gd} is parasitic capacitance between gate and drain.

3.3 BiCMOS

BiCMOS is the technology where Bipolar and CMOS devices are in the same substrate. Designer can employ high g_m devices for RF and analog circuit, at the same time high integration of analog and digital circuit by using CMOS devices. This process/technology could provide a quick and cost effective solution to the design.

4. RFID Reader IC

Complete Reader IC for UHF application is still new, the motivation behind the development is because of high demand in portable RFID Reader for supply chain management application.

Fig. 4 shows block level of reader IC. Passive UHF RFID system is usually half duplex system. Interface block in RFID Reader IC is normally composed of serial to parallel (SPI), Inter-Integrated circuit (I2C) and Universal Asynchronous Receiver/Transmitter (UART) type. Digital baseband modem is normally some form of Digital Signal Processing (DSP). Standards or protocols are determined or configured by the DSP. Digital to Analog Converter (DAC) receives digital data from DSP and convert it to analog signal. The signal is then later converted to RF by the RF transmitter or modulator. Frequency sythesizer is used to provide accurate high frequency resolution, especially for very high accuracy application. Directional Coupler provides one way direction of signal. Demodulator receives signal which is downconverted by downconverter to lower frequency. This lower frequency signal is later converted to digital signal by Analog to Digital Converter (ADC) for further processing in Digital Baseband Modem. Memory unit such as Read Only Memory (ROM) and Randon Access Memory (RAM) are employed in the whole design. Micro-Processor Unit (MPU) is used to receive command from the Interface and control Digital Baseband Modem. Like other ICs, RFID Reader IC also requires biasing circuitry.

4.1 RFID reader analog and RF receiver section

Receiver section is normally a direct conversion receiver (DCR). This topology will reduce the number of components in the receiver design.
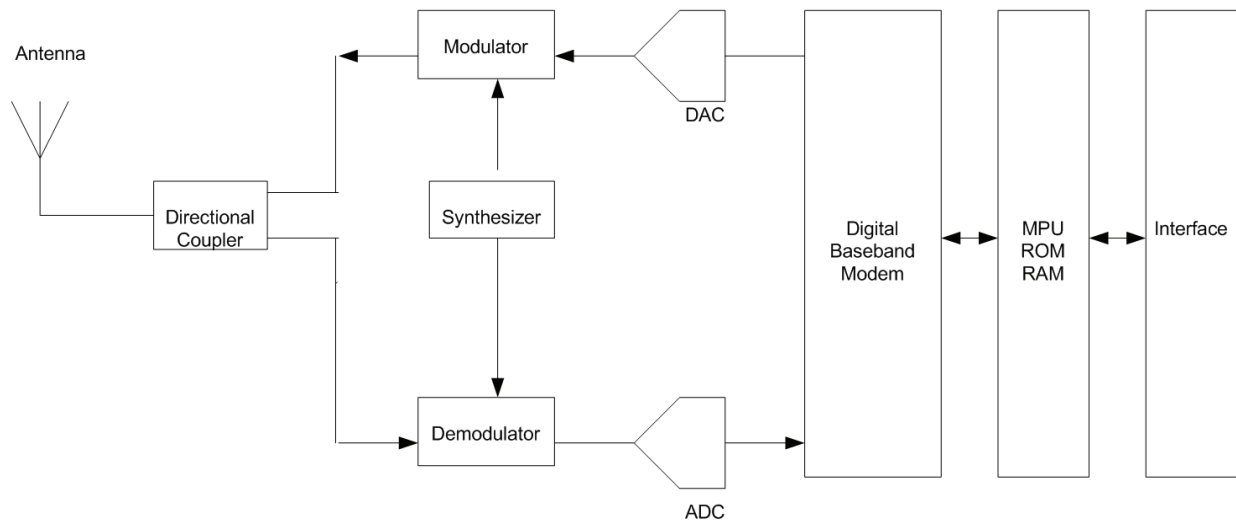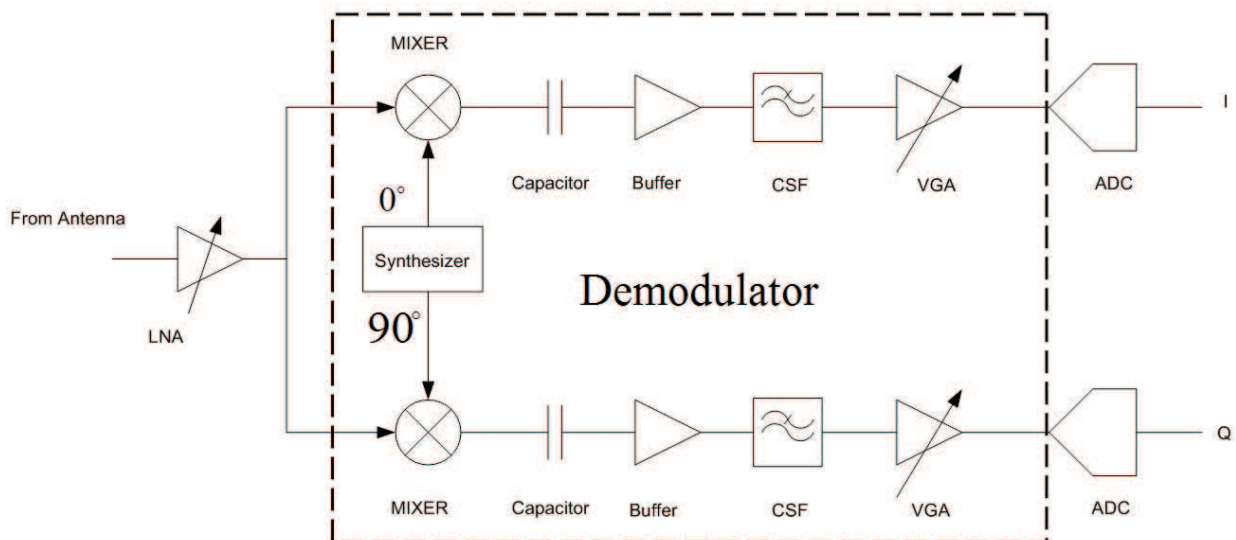
Fig. 4. RFID Reader IC block kevel

Fig. 5. Receiver section

Demodulator block discussed in Fig.4 is now clearly shown in Fig. 5. It consists of I/Q Mixer and Analog Baseband Circuit (Buffer, Channel Select Filter (CSF) and Variable Gain Ampifier (VGA)), Synthesizer is a separate block and not part of Demodulator. Self jammer is a problem to receiver, this is when a continuous wave (CW) signal is sent to a tag, a leakage of this transmit signal at receiver input leads to saturation of receiver block and degradation of sensitivity. For direct conversion architecture, the leakage to the receiver is directly down converted to DC. To deal with self jammer, two antennas sometimes are suggested to maximize the isolation between receiver and transmitter (Wang et al., 2007).

4.1.1 Low noise amplifier

The purpose of Low Noise Amplifier (LNA) as shown in Fig. 5 is to amplify weak received signal without adding too much noise to the signal. In the receiver chain, LNA determines the sensitivity. Fig. 6 shows 2-stage single ended input and differential output LNA. The fist stage is cascode LNA amplifier with capacitor, C_{ext} for Power-Constrained Simultaneous Noise and Input Matching (PCSNIM) (Nguyen et al., 2004). With the capacitance, the circuit

can achieve low noise, high gain at an optimum low current consumption. Second stage is a differential amplifier with inductive degeneration, L_{S2}. L_g, C_{ext} and L_S are used to achieve PCSNIM. L_d and C_c is for output matching of the first stage. R_B is used to bias transistor M4. I_s set DC current for this stage. R_O is load for the second stage. This topology can achieve high linearity with low noise peformance. High linearity is required to tolerate self-jamming signal.

For some LNA's output matching, capacitive transformer is sometimes used. The capacitive transformer is implemented using MOS capacitors. These capacitors achieve high Q-factors and are compatible with standard CMOS technology (Marzuki & David, 2006).
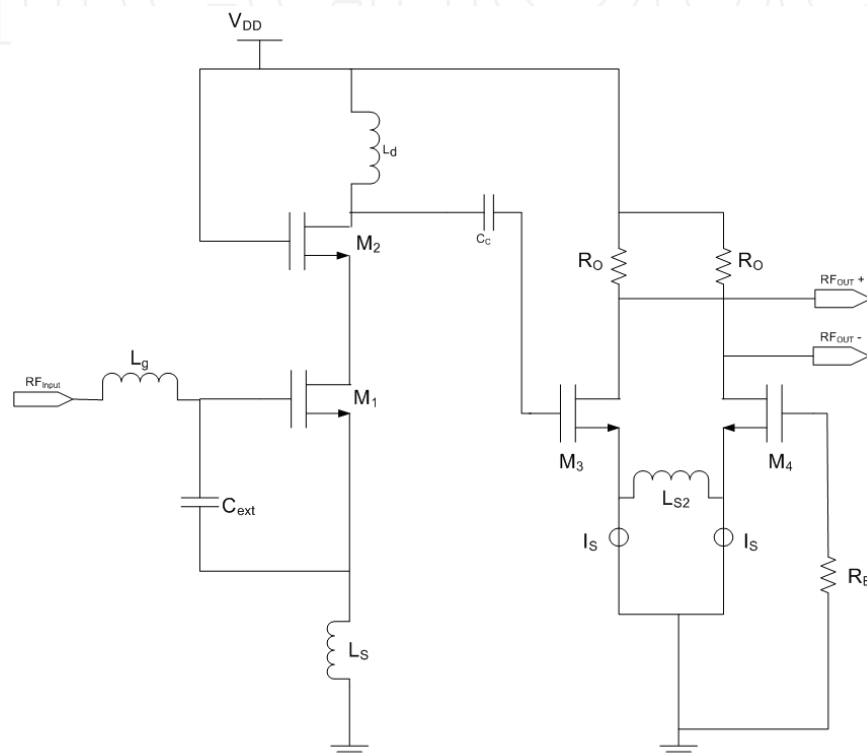
Fig. 6. Low Noise Amplifirer Circuit

4.1.2 I/Q mixer

I/Q Mixer is used to convert RF frequency signal to Intermediate Frequency (IF) frequency signal Passive mixer as in Fig. 7 has high linearity compared to conventional gilbert-cell mixer (Lee, 1998). The high linearity of the mixer due to linearity of NMOS switches (low impedance and no g_m non linearity). The passive switching mixer has very low $1/f$ noise because there is no DC current through the switching stage (Zhou & Chang, 2005). Local Oscillator (LO) signal is provided by synthesizer block. R_b is used to bias the drain of NMOS switches.

The output of the mixer are AC coupled to block DC offset. The DC blocking capacitor value is chosen depending on the data rate of tag.

4.1.3 Analog baseband circuit

The purpose of this block is to process the analog IF signal to digital singal. Analog Baseband Circuit composes Variable Gain Amplifier (VGA), filter and ADC. For DCR, transmitter carrier leakage at the receiver input is down converted to DC. It can also be further removed by a DC offset cancellation circuit in the baseband section.
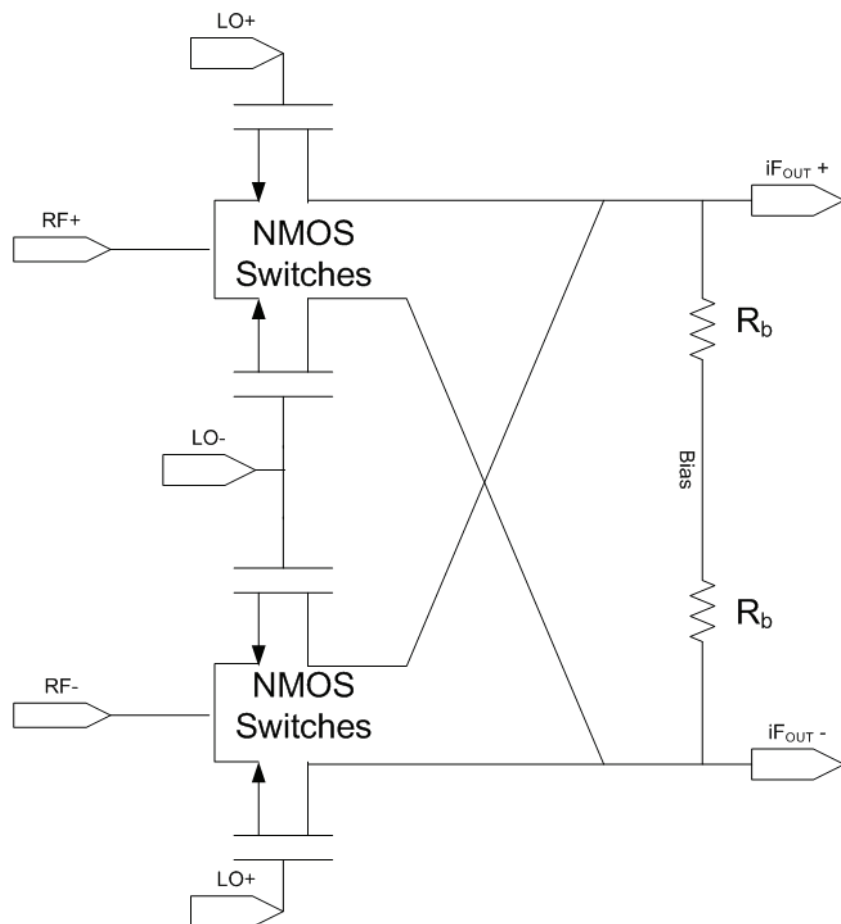
Fig. 7. Passive Mixer

For Class 1 and ISO 1800-6C, channel select filter is configured as low pass filter with zero IF. Example of the filter is 3 rd order, chebychev filter using Output Transconductance Amplifier (OTA) is shown Fig. 8.
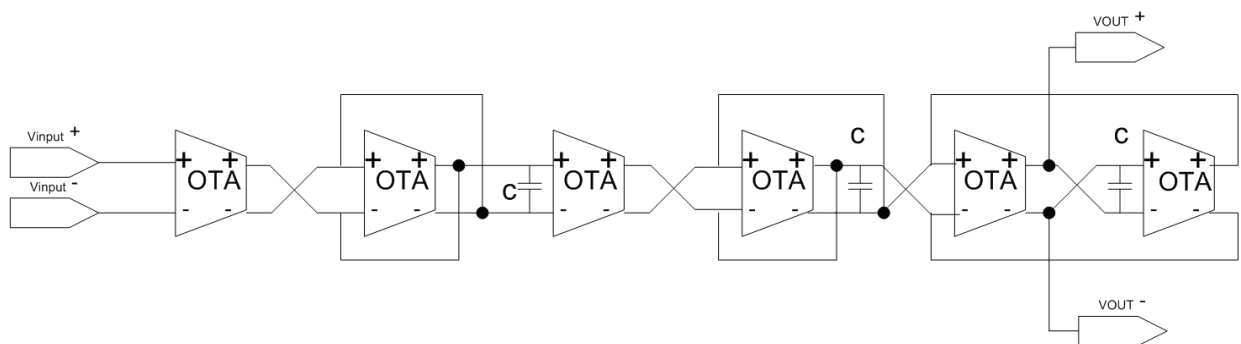

Fig. 8. 3rd Order Chebychev filter

A Simple OTA is shown in Fig. 9. This OTA uses 6 inverters.

Opamp-based programmable gain amplifiers are normally used as VGA for the excellent linearity performance. The resolution is 1 dB with large control range can be achieved. The amplifier is used to increase the signal voltage for easier analog to digital conversion. 10 bit pipe-lined ADC is used to convert analog signal to digital signal (Khannur et al., 2008).
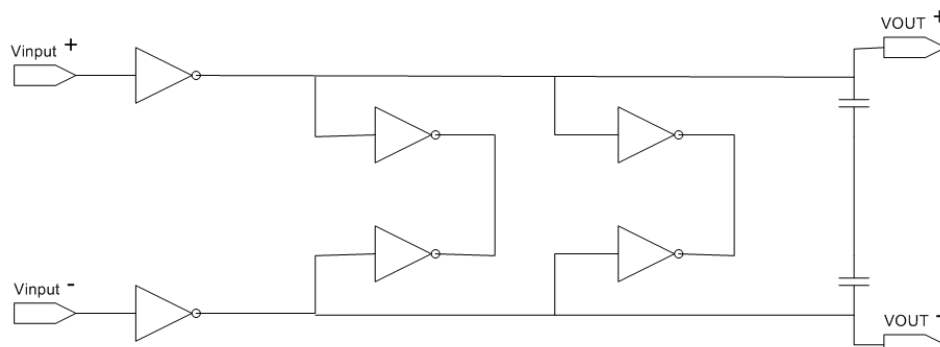
Fig. 9. Inverter-Based OTA

4.2 Receiver digital baseband demodulator

Fig. 10 shows receiver digital baseband demodualtor or modem. Digital Filter block provides a bandpass digital filtering to preserve the information contents of the in-band signal whilst alttenuating out-of-band noise and interference.
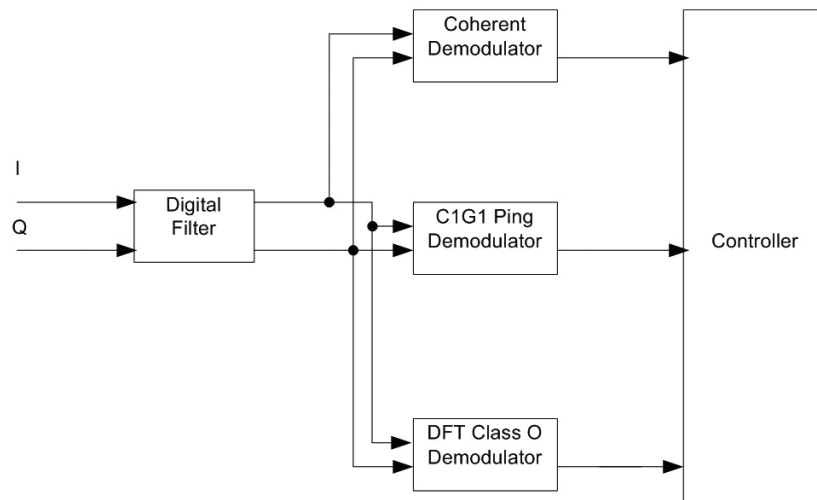

Fig. 10. Receiver Digital Baseband Demodulator

Class 0 Demodulator computes 16-bin DFT and compares the peak power in the data-1 bins. The soft decision is passed to bit slicing. Ping demodulator (Class 1 Gen 1) uses Zero crossing detector followed by matched filter for all 32 possible combination of a ping reply. This signal is with out preambles or synchronization
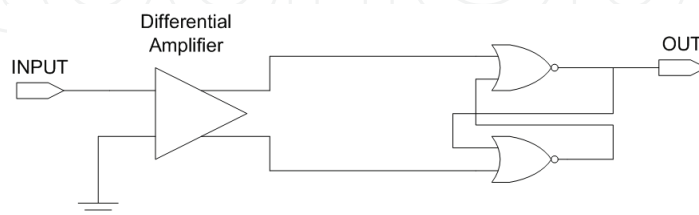
Fig. 11. Zero Crossing Detector

Fig. 11 shows a differential amplifier and a flip-flop as zero crossing detector. Coherent Demodulator uses a correlator and estimator to measure the incoming tag data rate utilizing the pilot tone as the preamble. Controller block will process digital data for application or host processor.
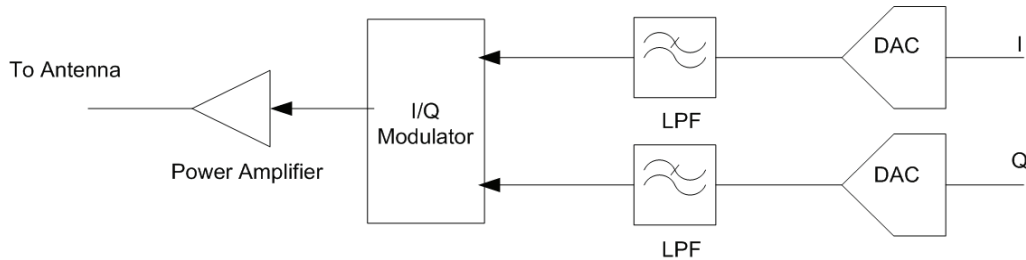
4.3 RFID reader analog and RF transmitter section

Fig. 12. RFID Reader Analog and RF Transmitter Section

Fig. 12 shows Analog and RF Transmitter of RFID Reader. The purpose of this block is to convert digital I and Q data to RF signal. Current steering 10 bit DAC (Khannur et al., 2008) are used to convert digital signal to analog signal. The low pass filter (LPF) is used to eliminate spectral spur and to ensure the transmit spectrum fits well into transmit mask. I/Q modulator is used to convert low frequency signal to 900 MHz band. Class A PA is used to produce to maximum 30 dBm output signal.

4.3.1 Power amplifier

Cascode topology (Khannur et al., 2008) is normally used for Power Amplifier (PA). Attenuator is used to control the gain or output power of PA. Matching circuit is needed to match for optimum power transfer between input and transistor gate. Biasing of the transistor is done through RF choke. L_d and capacitor tune the circuit to the UHF frequency. PA circuit is shown in Fig. 13
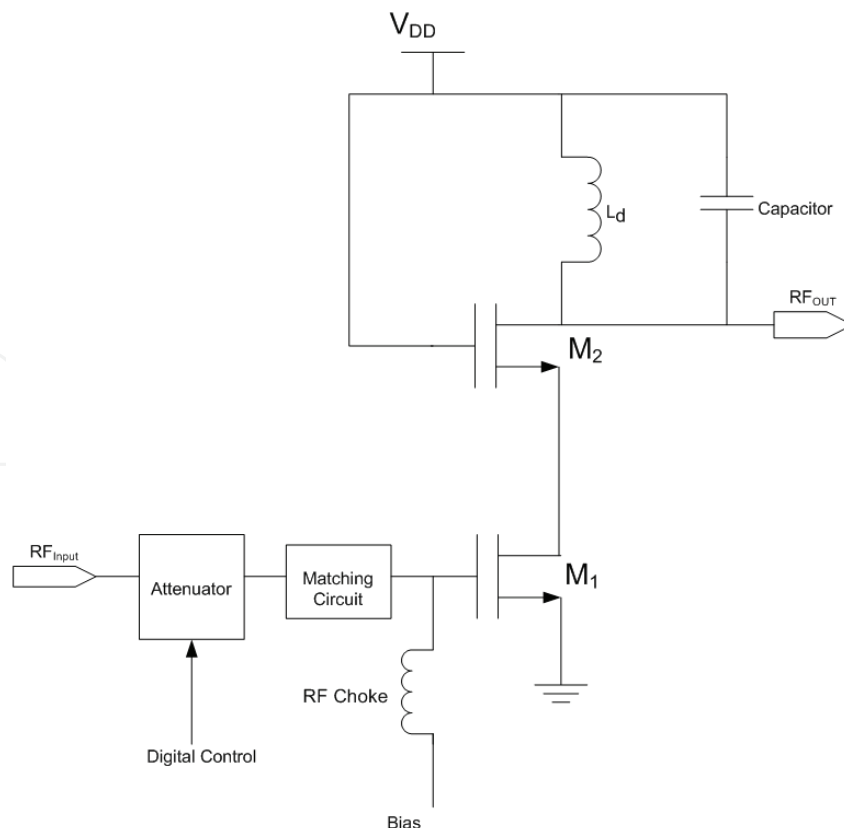
Fig. 13. Variable Power Amplifier

4.3.2 I/Q modulator

Gilber Cell mixers are used for I/Q mixer. Both I and Q sections are used for generating SSB –ASK Modulation. Input I/Q signal is from Digital to Analog Converters.

I/Q Modulator is shown in Fig. 14. Source degeneration, R_E is needed to increase the linearity to satisfy transmitter spectrum mask. Local oscillator (LO) signal is provided by the synthesizer block. I_s is used to set DC current for the modulator.
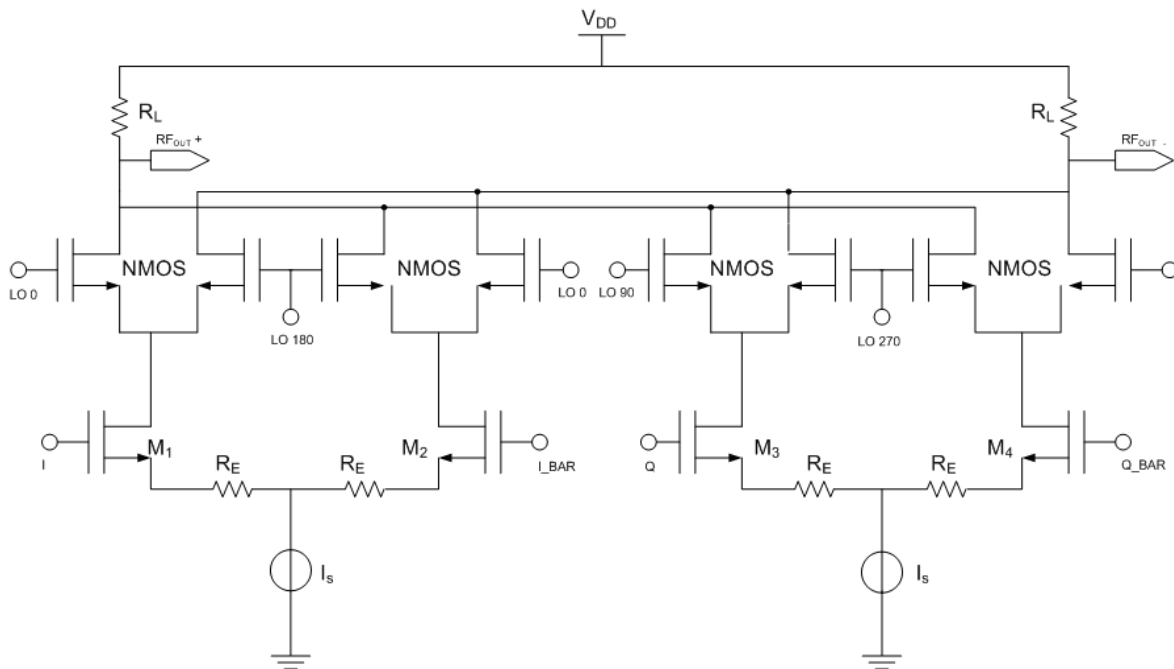
Fig. 14. I/Q Modulator

4.4 Transmitter digital baseband modulator

Fig. 15 shows Transmitter Digital Baseband Modulator. Hilbert Transform filter and cordic frequency shifter are used to provide real modulation or complex modulation. This is to support different modulation schemes such as ASK, SSB ASK or PR ASK. Predistorion block is needed to cope with the nonlinearities by PA when supply modulation is used. Controller is a programmable microcode sequencer. It receives non-real time commands from a protocol processor which is preambles and frame sync.
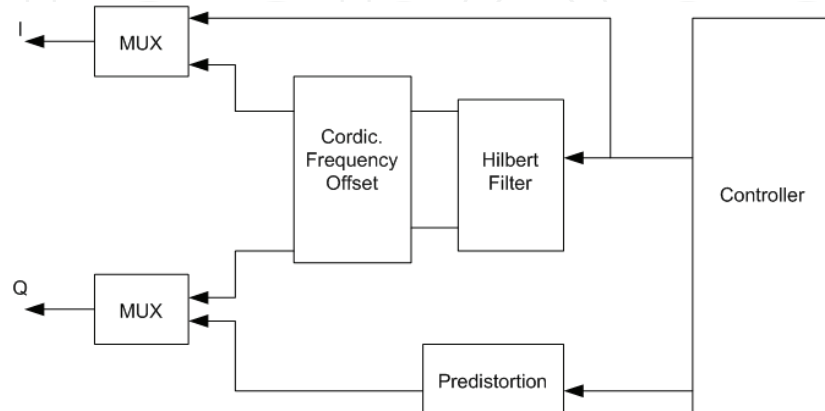
Fig. 15. Digital Transmit Modulator

Output I and Q are connected to DAC for analog and RF processing.

4.5 Synthesizer

Synthesizer provides LO signal for both receiver and transmitter. Dual loop PLL Synthesizer can achieve good phase noise and low spurious level with good frequency resolution (Razavi, 1997). Integer-N PLL with a divide-by- 2/3 with external loop filter can also meet the requirement (Chiu et al., 2007). This type of synthesizer is small, and this leaves space for more complex digital block to be implemented in reader IC.

4.6 Biasing circuitry

One important requirement in integrated circuit is constant performance across temperature. This is especially critical for analog integrated circuits such as radio frequency integrated circuits (RFIC). One way to control the performance is to control the current consumption.

A typical RFIC circuit employs a circuit which provides stable voltage or current source across temperature. A Popular circuit is bandgap circuit which provides stable voltage reference to RFIC circuit. The bandgap circuit employs diodes as internal reference, the diode array tends to increase the size of the layout and model accuracy is scarce.

A circuit called Voltage for current source (VCS) circuit provides voltage for the current source in all RF IC circuits. The circuit is shown in Fig. 16. VCS circuit employs three transistos. IPTAT is current proportional to absolute temperature and I_s is the required current. Equation (8) shows that I_s can be designed to be constant, proportional or complimentary across temperature variation.
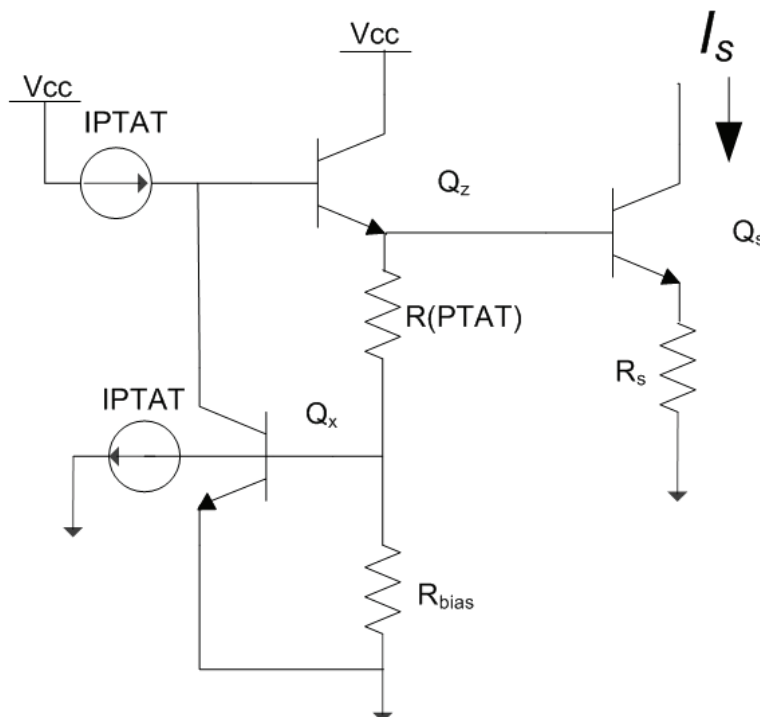

Fig. 16. Simplified VCS with Current Source (Marzuki et al., 2008)

$$I_S = \frac{(IPTAT \times R(PTAT) + V_{BE}(Q_x) - V_{BE}(Q_S)) + V_{BE}(Q_x) \times \dfrac{R(PTAT)}{R_{bias}}}{R_s} \tag{8}$$

5. RFID Tag IC

Unlike reader IC, tag IC development is already mature. The focus on the tag IC development is on reducing the cost. Fig. 17 shows RFID Tag block main diagram. A rectifier is employed to establish supply voltage to the rest of the circuits. The supply voltage is regulated using protection and voltage regulation circuit. Demodulator receives signal or information from the RFID reader, while modulator is used to convert digital data to higher frequency signal. Clock recovery and divider circuit accurately produce 50-50 duty cycle clock which is generated from RFID reader. Digital block is normally composed of MPU and memory block. Information identification is normally stored in memory block.
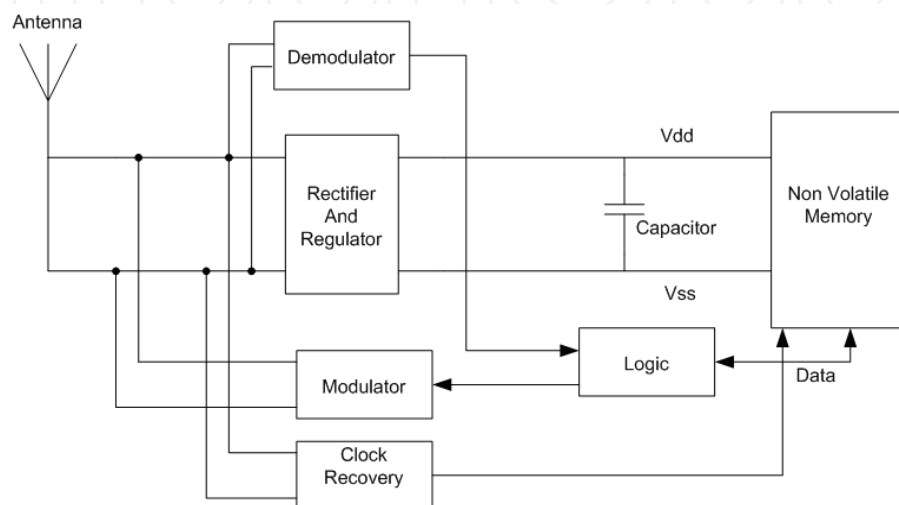

Fig. 17. RFID Tag

The design of UHF tag IC is normally targetted for long distance application. This proves to be a challenge. Design tradeoff must be made and some techniques must be done to accomodate the requirement. For UHF RFID tag, only (dipole) antenna is external component, while the rest of the blocks are in one IC.

5.1 Rectifier

The received signal, sent by an interrogator device, generates a sinusoidal voltage which is then rectified, filtered and multiplied if necesary to generate a DC voltage that can be used to supply and activate internal circuitry.

The concept of rectifier is to transfer the charge from C_{in} to C_{hold} during the cycles of incoming strong signal. The basic circuit of single stage rectifier is shown in Fig. 18

Low V_{th} PMOS (Fig. 18 (c)) is used to get low voltage drop of around 150 mV on each diode-connected transistor.

5.1.1 Efficiency

Efficiency is very important, high effeciency indicates that less power will be wasted, and longer detection range can be achieved. Basic efficiency (Kocer & Flynn, 2005) equation

$$Efficiency = \frac{DCV_{OUT}}{V_{INPEAK} \times n} \tag{9}$$

Where DCV_{out} is the generated output voltage. V_{INPEAK} is the peak incident RF amplitude, n is number of stages.
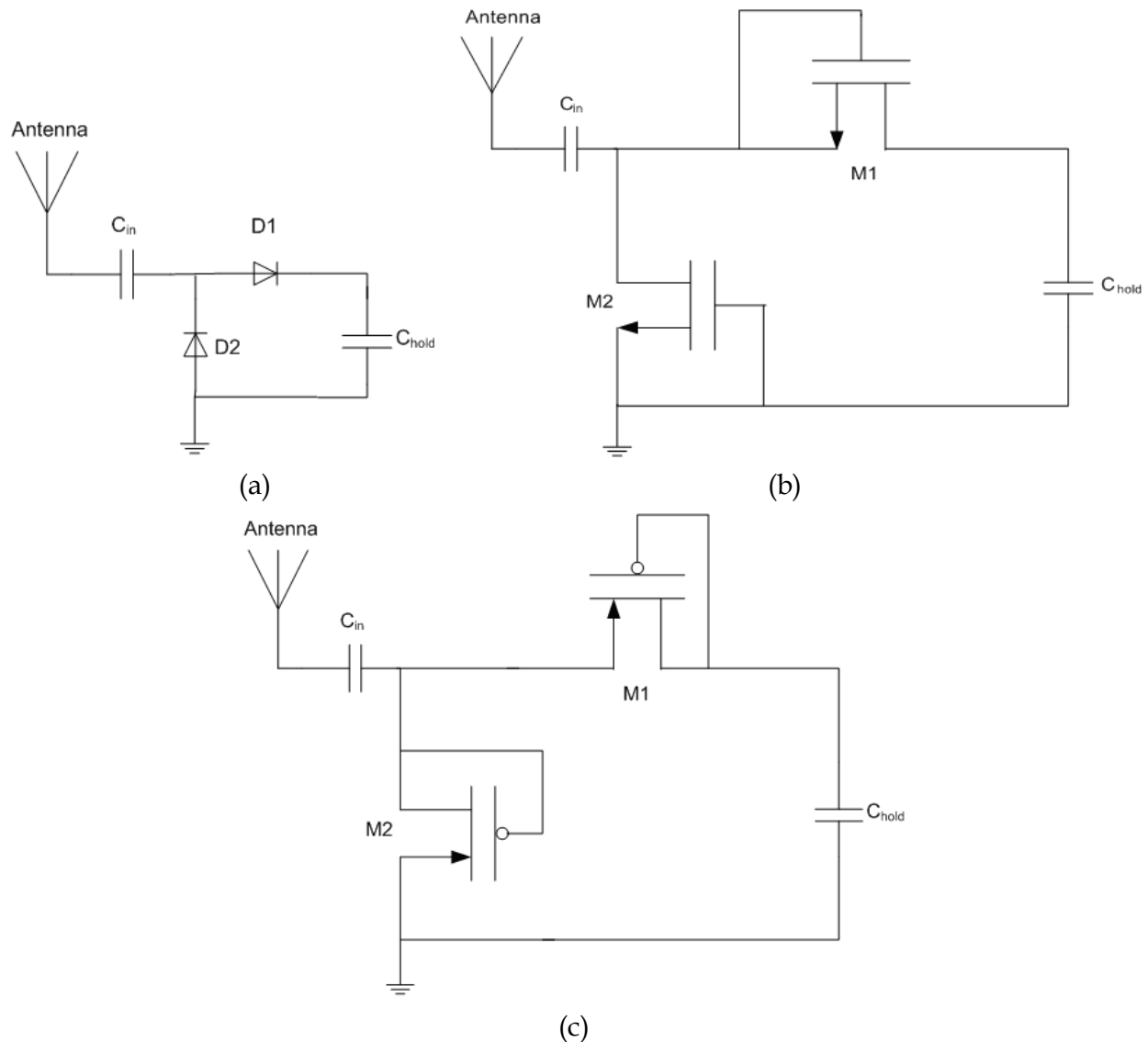
Fig. 18 (a). Rectifier using diode (b). Rectifier using NMOS (c) Rectifier using PMOS

One of the loss factors is the threshold voltage, which is associated with the diode-connected MOS. The specially designed Schottky diodes with low resistance allow for a high-efficiency conversion of RF energy to DC supply voltage, but not many IC technologies come with this diode. For standard CMOS technology, to reduce or eliminate the threshold voltage, an external voltage must be applied between gate and source. An example of the concept is shown in Fig. 19.

V_{bth} is external voltage source. The storage capacitor stores the V_{th} voltage for the MOS diode.

5.1.2 Full wave rectifier

Fig. 20 shows a single stage mirror-stacked stucture of two CMOS half-difference rectifier circuits, this can optimize power efficiency due to eliminating of parasitic capacitances a the input terminal IN -. This is due to IN – is AC ground. The circuit multiply the input voltage.
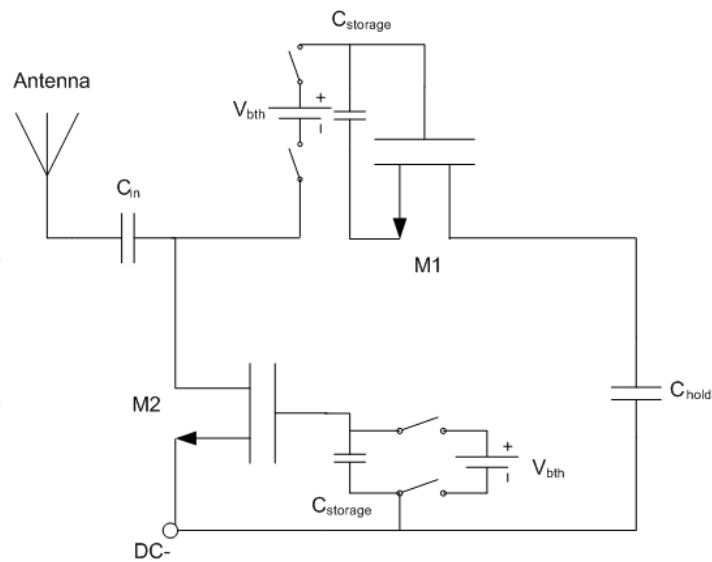
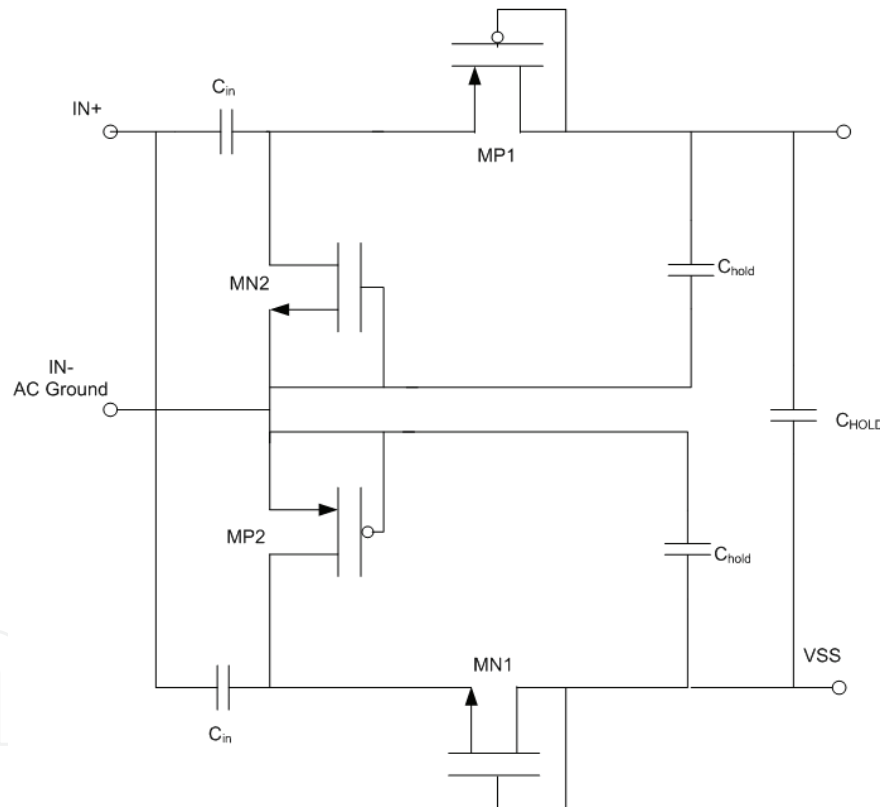Fig. 19 Rectifier circuit with External Voltage Source (Nakamoto et al., 2007)

Fig. 20. Full Wave Rectifier (Nakamoto et al., 2007)

5.1.3 Power matching

At RF frequency, power matching is important for optimum power transfer between antenna and input of rectifier. If mismatch occur, smaller DC power is converted by the rectifier. The equivalent input impedance of the rectifier might be represented, as a zero-order approximation, by the parallel of a resistance and a capacitance. In the high frequency analysis of the rectifier, all the capacitances of the rectifier can be considered as short-

circuited and so all diodes can be considered in parallel or anti-parallel with the input. As a consequence, at the input of the rectifier, the capacitances of all diodes are in parallel. The equivalent input resistance, R_{eq}, of the rectifier is the resistance calculated from power consumption. Using an LC power matching network, the L= QR_A/ω_o, and C = Q /$R_{eq} \omega_o$, (Razavi, 1997), where, R_A is the resistance of the antenna and Q is the quality factor of the LC network $Q = \sqrt{R_{eq}/R_A - 1}$. An inductance L', in parallel with the input of rectifier, can be used to compensate the equivalent input capacitance of the rectifier.   Fig. 21 shows the matching network.
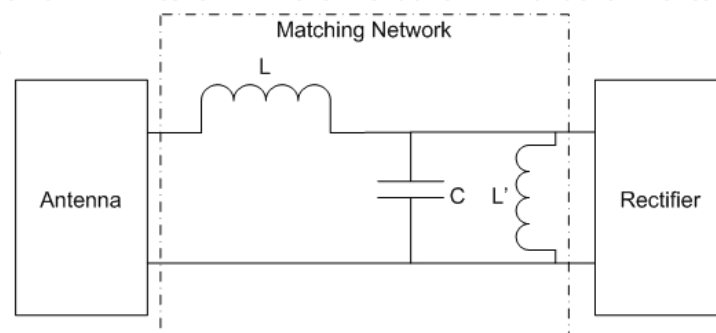

Fig. 21. Matching Network (De Vita & Iannaccone, 2004)

5.2 Modulator

Backscatter modulator is normally used for tag IC. The modulated backscattered signal happen when IC input impedance changing upon receiving CW carrier with small notches for data transfer from the reader. A design trade-off must be made in order to ensure a larger power still availabe for (rectifier) power supply. Fig. 22 shows PSK modulator circuit.
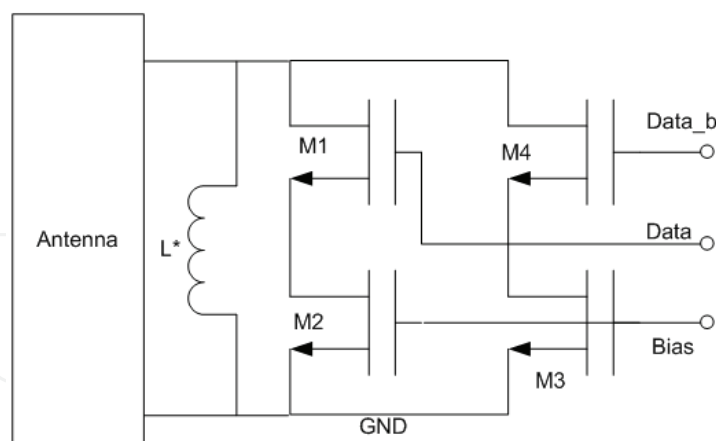

Fig. 22. PSK Modulator (De Vita & Iannaccone, 2004)

Depending on the data signal level, either MI or M4 conducts leading to a different output capacitance, since the two transistors have different sizes. The inductor **L*** makes the variation of the imaginary part of the impedance seen by the antenna symmetric with respect to zero. Transistors M2 and M3 allow us to obtain an output resistance of the modulator much larger than the antenna resistance so that only a negligible fraction of the power at the antenna goes to the modulator. The condition for ASK modulation is explained in (Finkenzeller, 2003), where input impedance must be in resistance.

5.3 Demodulator

The demodulator detects the ASK modulated signal from Reader. Fig. 23 shows basic circuit of ASK demodulator.
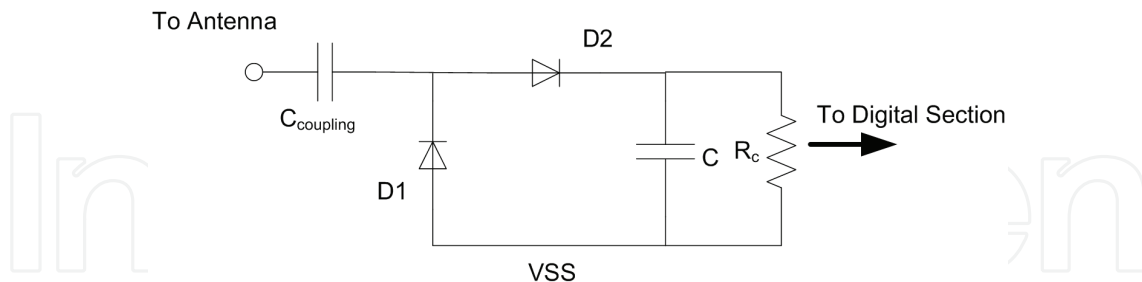

Fig. 23. ASK demodulator (De Vita & Iannaccone, 2004)

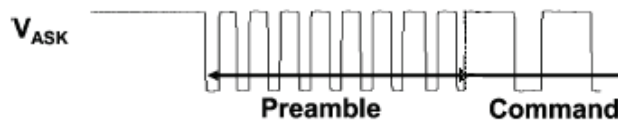D1 and D2 can be replaced by diode connected MOS transistor.

Fig. 24. Demodulated ASK (Nakamoto et al., 2007)

Fig. 24 shows an example of demodulated signal, output of demoulator. The first serial signal is preamble signal, the second serial signal is the command from reader.

6. Measurement methodology

For RFID Reader, the output of transmit after filter carrier phase noise is important. The receiver sensitivity to the noise due to leakage from the transmit signal is normally measured. While power efficiency measurement is crucial for tag IC.

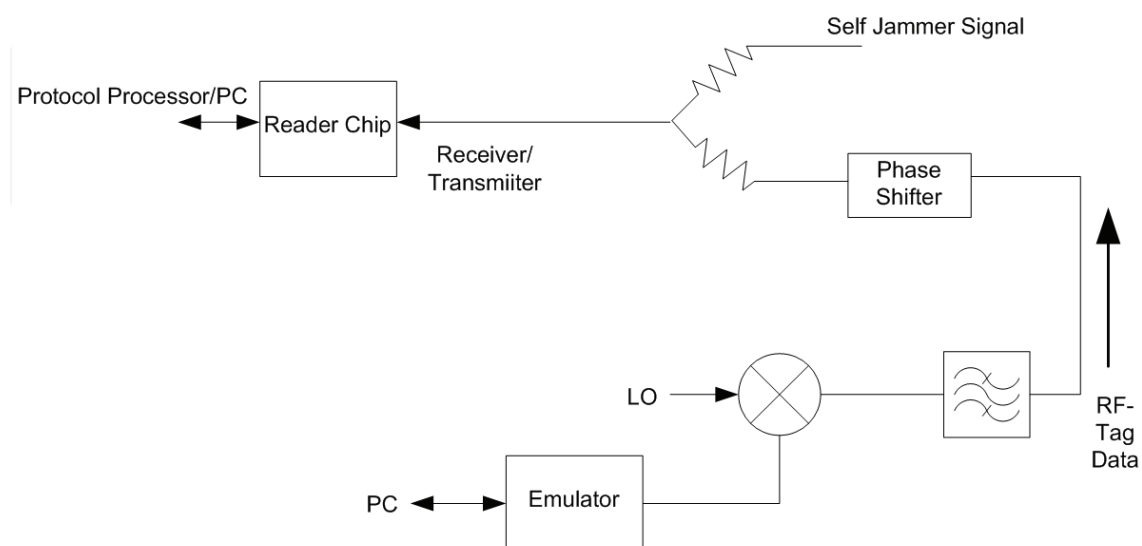### 6.1 RFID reader receiver sensitivity measurement

Fig. 25. Reader Receiver Sensitivity

Fig. 25 shows test bench measurement for reader IC. Emulator such as FPGA can be used to imitate RFID tag data. Phase Shifter is used to change phase of tag data.

Example measurement result is shown in Fig. 26. This is example of receiver sensitivity measurement with different incoming tag phase. The tag phase is orthogonal to the jammer noise is the best case phase.
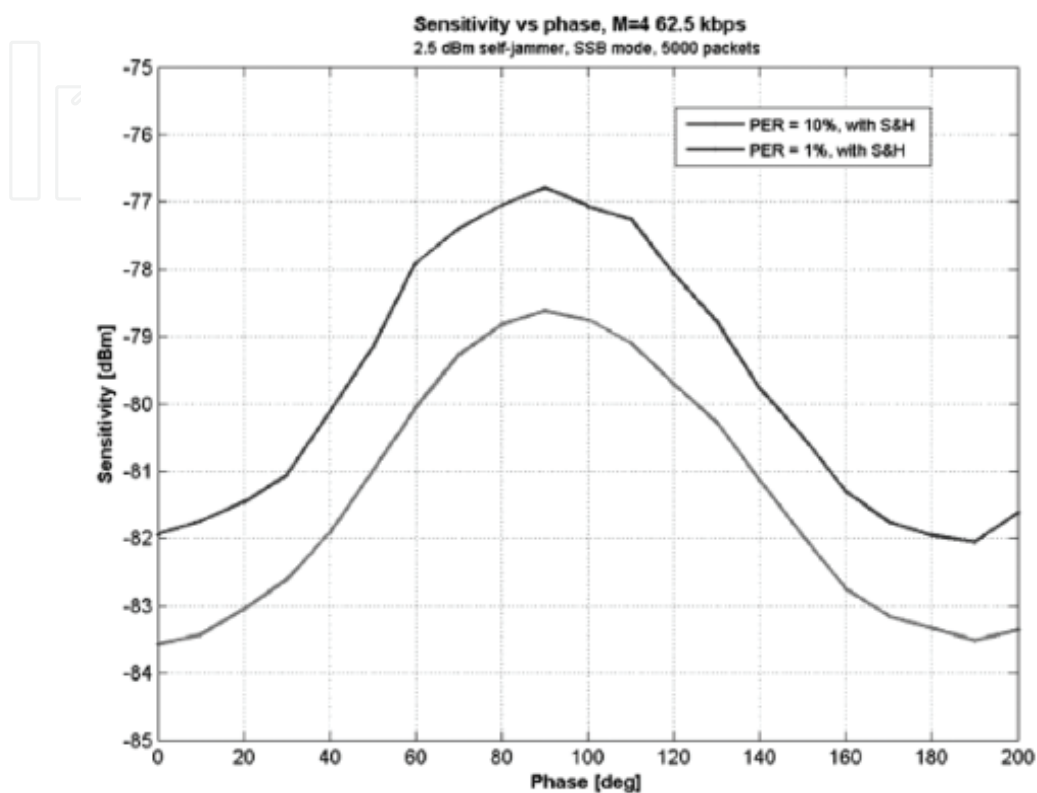

Fig. 26. Measured Packet Error Rate (PER) vs tag phase

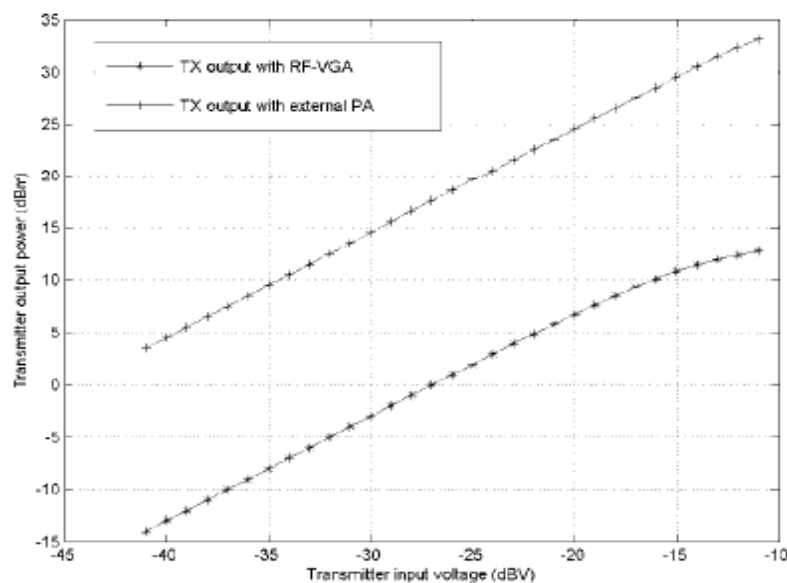## 6.2 RFID reader transmitter measurement
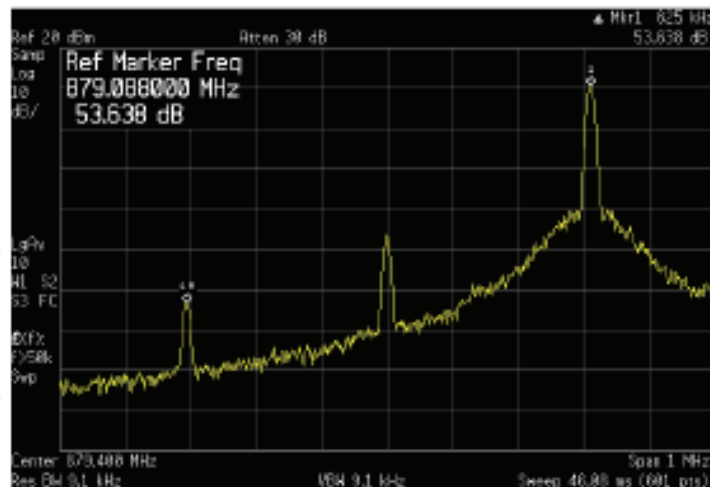

Fig. 27. P1dB Measurement.

Fig. 28. Sideband Measurement

Fig. 27, 28 and 29 are transmitter measurement results. The transmitter output (Fig. 25) is normally connected to a spectrum analyzer. P1dB measurement shows measurement with and without PA. P1dB is when the power gain is decreased by 1 dB. Obviously from the measurement result, TX output with PA has higher linearity than TX output without PA. Sideband measurement shows sideband rejection ration of ~ 54 dB.
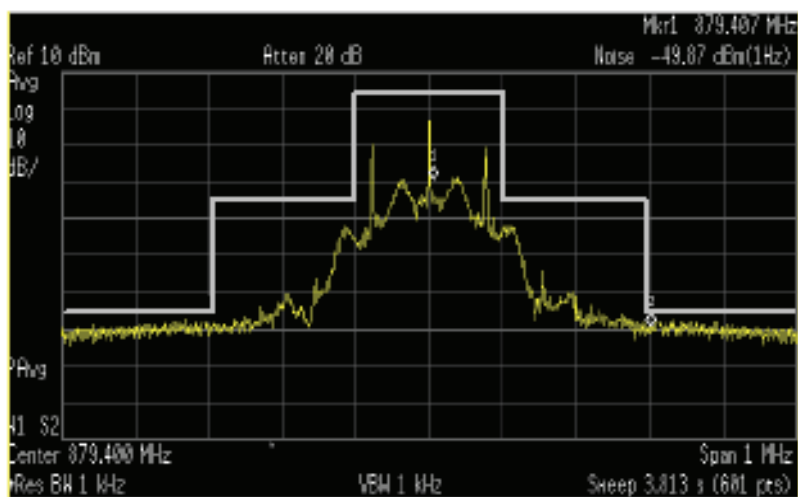

Fig. 29. Spectrum Mask

Fig. 29 shows the measured transmitter output spectrum for DSB-ASK and the requirement mask. The center frequency is 879.4 MHz.

6.3 RFID tag IC measurement

Unlike RFID Reader IC, RFID Tag measurement is tedious and difficult because of several factors namely the die area is small which prohibits test pads. This has required IC designers to endeavour to design and support custom test equipment and dramatically lengthening IC development.

On wafer measurement is a chosen method if anechoic chamber is not available, where antenna loss is not present and mismatch can be eliminated.

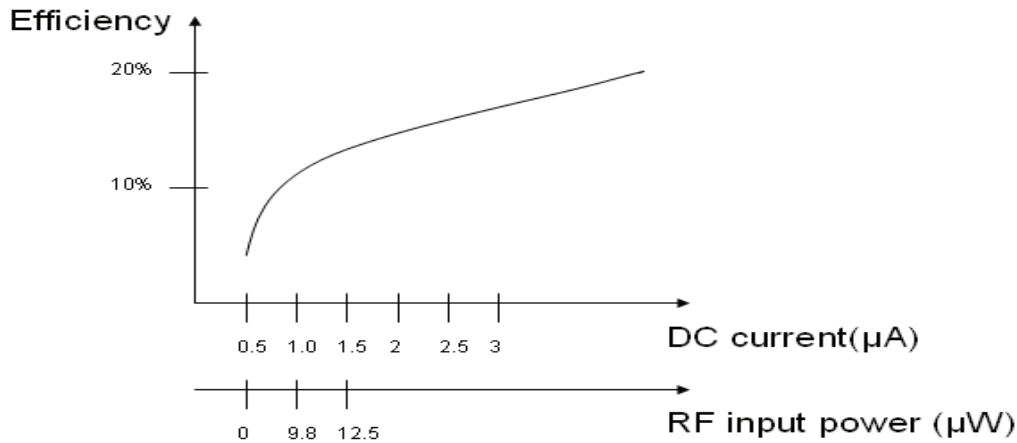Example of power efficiency measurement is shown in Fig. 30.

Fig. 30. Efficiency vs Tag DC current consumption

Say Fig. 30 shows an example of RFID tag measurement, say by design 1.5µA is total current consumption for tag IC in Read mode therefore the required RF input power is 12.5 µW. The power required to Write tag (EEPROM) is normally twice compared to Read mode (Karthaus & Fischer, 2003). Average RF input power (Karthaus & Fischer, 2003) to the tag,

$$P_{RF} = (1 - m^2).P_{available} \tag{10}$$

Where m is modulation index, $P_{available}$ is available power to the tag. Assuming $m = 0.5$, calculated $P_{available}$ is 16.7 µW. The difference between P_{RF} and $P_{available}$ is utilized as backscattered modulated power.

Reader with 500 mW Effective Radiated Power (ERP), more than 4.5m reading distance can be achieved with $P_{available}$ of 16.7 µW (Karthaus & Fischer, 2003).

6.3.1 More challenges with RFID tag IC testing for mass production (Murfett, 2004)

RFID Tag IC test measurement is a challenge due to its high volume and low cost requirement. Below are two main challenges.

6.3.1.1 Test visibility and digital logic

Due to the critical size constraints, dies may only contain the two bond pads for connection to the antenna. Addition of other pads for testing will cause a rapid expansion of the die size. Thus it is can often be difficult to find room for post-rectifier Vdd and Vss test points, let alone the pads required for conventional boundary scan chain type testing. Furthermore, the logic complexities of the IC's are often quite small. Function control is implemented via state machine logic, and never by something as complex as the most basic micro-controller.

6.3.1.2 Non-volatile memory issues

EEPROM memories must be properly initialised at wafer level. It must be possible to stress the memory to its performance limits to test endurance and data retention. It must be possible to adjust the operating state of the memory to set it to sensitive states. It also must be possible to perform write and erase all, or write and erase of odd or even pages, to

perform memory initialisation cycling and cross-talk checkerboard tests. All of these commands add significant overhead to the command set of the IC. Furthermore, baking tests for data retention may last up to hours, which adds a significant time and hence cost to the overall testing of these dies.

7. Future research on RFID reader IC

In order to increase the function and application of RFID system, multiband tag IC has been developed. The tag can be operated for many application and places. An example of tag IC which can communicate from 13.56 MHz to 2.45 GHz (http://www.toppanforms.com /eng/news/mmchip.asp) is open for all applications. Once the demand is high for this multiband tag IC, new form of multiband RFID Reader IC need to be developed. Fig. 31 shows IC layout of dual band RFID Reader IC.
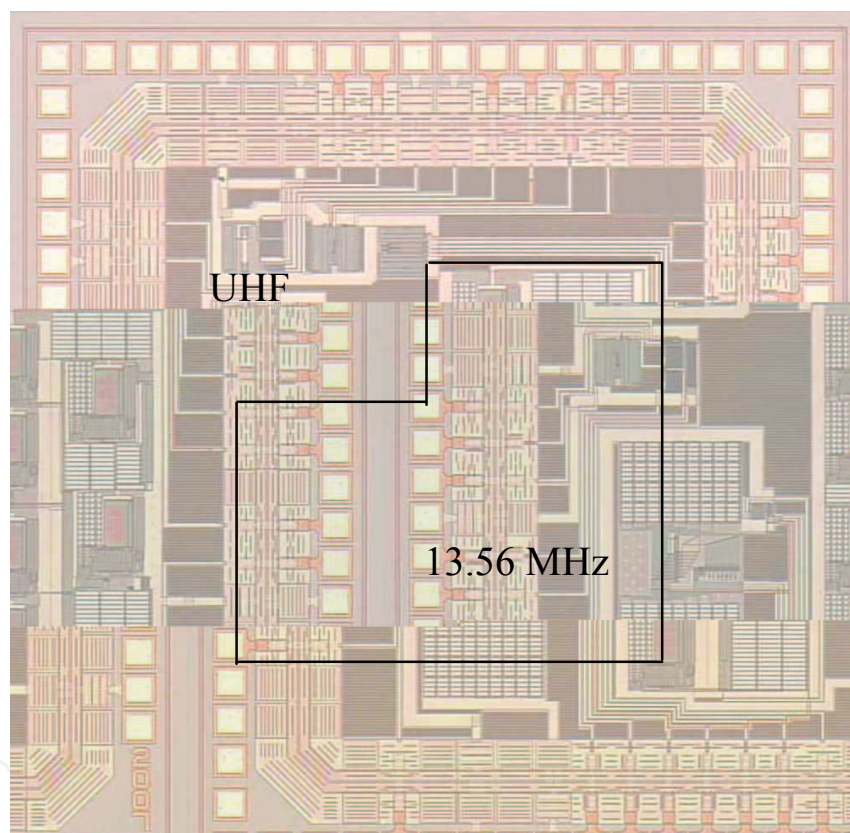

Fig. 31. Dual Band RFID Reader IC (Courtesy of C-RAD Technologies and SHRDC)

The Reader IC is fabricated in MIMOS using 0.35 µm CMOS technology.

8. Conclusion

This chapter has discussed the design methodology of integrated circuit. The technology such as Silicon Bipolar and Silicon CMOS are also studied in this chapter. The architecture or circuit topology of reader and tag are also thoroughly discussed. The circuit technique in designing the tag and reader is studied and analyzed. Digital circuit is not throughly discussed in tag due to its simplicity in nature. The main problem in tag IC development is only at Analog/RF front-end. The measurement methodology of advanced RFID

components is also discussed. Challenges of high volume testing is explained for future improvement development. Finally, a new type of reader IC, i.e. dual band is presented.

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Development and Implementation of RFID Technology

Edited by Cristina Turcu

The book generously covers a wide range of aspects and issues related to RFID systems, namely the design of RFID antennas, RFID readers and the variety of tags (e.g. UHF tags for sensing applications, surface acoustic wave RFID tags, smart RFID tags), complex RFID systems, security and privacy issues in RFID applications, as well as the selection of encryption algorithms. The book offers new insights, solutions and ideas for the design of efficient RFID architectures and applications. While not pretending to be comprehensive, its wide coverage may be appropriate not only for RFID novices but also for experienced technical professionals and RFID aficionados.

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