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Analog front-end for pixel sensors in a 3D CMOS technology for the SuperB Layer0

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Summary. — This work is concerned with the design of two different analog channels for hybrid and monolithic pixels readout in view of applications to the SVT at the SuperB Factory. The circuits have been designed in a 130 nm CMOS, vertically integrated technology, which, among others, may provide some advantages in terms of functional density and electrical isolation between the analog and the digital sections of the front-end.

PACS 85.40.-e – Microelectronics: LSI, VLSI, ULSI; integrated circuit fabrication technology.
PACS 29.40.-n – Radiation detectors.

1. – Introduction

In the SuperB Factory, a high-luminosity e^+-e^- collider intended for heavy flavour physics studies, the silicon vertex tracker (SVT), will have the role of providing precise information on both the position and direction of charged particles emerging from the interaction point. The SuperB SVT (very similar to the 5 layer BaBar SVT) is supplemented by a new innermost Layer0. In this work two different solutions are proposed for the Layer0: CMOS monolithic active pixel sensors (MAPS) with a deep N-well (DNW) acting as collecting electrode [1] and hybrid pixel sensors. CMOS MAPS can meet the stringent material budget requirements set by SuperB-Layer0, as their substrate can be thinned down to a few tens of microns with no significant signal loss. The most critical point of DNW MAPS is the low signal provided by the sensor and the relatively low degree of radiation hardness. Hybrid pixel detectors are comprised of two chips, one containing the sensor array and the other including the readout electronics, back-to-back connected generally by means of bump bonding techniques. Hybrid pixels can provide high signal-to-noise ratio and high radiation tolerance and they can work at high hit rates. Hybrid pixels are a well-established technology but have a limitation in their relatively large material budget increasing the probability of multiple scattering phenomena.

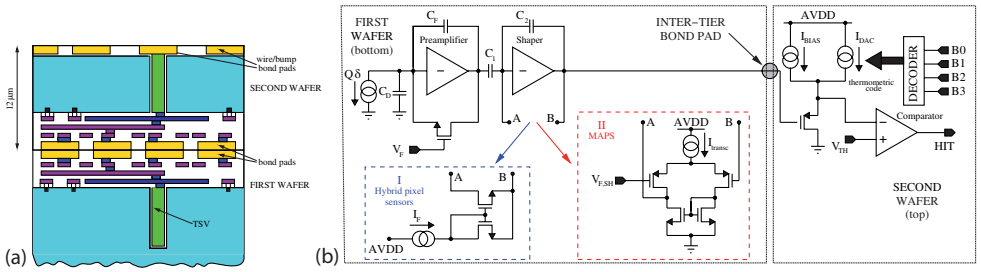

Fig. 1. – Cross-sectional view of a double-layer 3D process (a). Block diagram of the analog front-end circuit for CMOS MAPS and hybrid pixel sensors (b).

2. – Vertical Integration Technologies

The front-end circuits presented in this work have been designed in the Tezzaron/Globalfoundries process (fig. 1(a)) [2], which is a monolithic, wafer level 3D integration technology. Vertical integrated circuit manufacturing involves the independent fabrication of two or more planar circuits on different wafers, which are subsequently bonded together after precise alignment and thinning, therefore providing higher integration density. 3D technologies allow the designer to cope with the increasing spatial resolution requirements set by the experiments at the next generation colliders and, at the same time, provide the opportunity of developing a more complex in-pixel logic, also strongly reducing cross-talk issues in mixed-signal circuits. In the particular case of MAPS, further benefits derive from the improved electrical isolation between the sensor and digital sections in addition to the possibility of placing competitive N-well area on a different layer from the sensor, resulting in a better collection efficiency.

3. – MAPS and hybrid pixels analog processor schemes

To meet the resolution requirements set by the experiments at the SuperB Factory, the mixed signal front-end circuits have been laid out in a 50 μm square cell. Both the front-end processors for MAPS and hybrid pixel sensors, whose main features are shown in table I, include a charge preamplifier (PA) and a shaper stage (see fig. 1). The signal at the shaper output is compared to a chip-wide threshold V_{TH} by means of a discriminator. The in-pixel logic stores the hit in a flip-flop and takes care of communicating with the peripheral blocks for fast data retrieval. The C_F capacitor in the PA is continuously discharged by an NMOS transistor biased in deep subthreshold through the gate voltage V_F. Different solutions are employed for the shaping filter. In the MAPS analog channel a continuous time, RC-CR shaper follows the charge preamplifier. The capacitance C_2 in the shaper is discharged by means of a transconductor. The choice of a transconductor in the feedback network (fig. 1(b)) of the shaper was actually made for the purpose of reducing the effects of voltage drop on the channel-to-channel dispersion of the DC voltage at the shaper output (V_{bl}). By using a transconductor, it is possible to set V_{bl} to a given (chip wide) value by means of a voltage reference placed at the periphery of the chip, which is not affected by voltage drop issues [3]. Besides monolithic sensors, also a hybrid pixel approach is being investigated for the SuperB Layer0. In this readout scheme the charge preamplifier is followed by a shaper stage which is decoupled from the PA by means of the capacitance C_1. An NMOS current mirror structure

TABLE I. – *Main features and simulation results for MAPS and hybrid pixel front-end (FE).*

	MAPS FE	Hybrid pixel FE
Charge sensitivity (mV/fC)	850	50
Peaking time (ns)	360	260
Input dynamic range (e^- rms)	3000	60000
ENC (e^- rms)	35	130
Threshold dispersion (bef./aft. corr.) (e^- rms)	100/12	560/65
Pixel power dissipation (μW)	33	10
Detector parasitic capacitance (fF)	300	150

(fig. 1(b)) is used to continuously reset the shaper feedback capacitor C_2. Since C_2 is discharged by a constant current, proportional to the mirror reference current I_F, the recovery time increases linearly with the signal amplitude. It is worth observing that the front-end power consumption is significantly smaller here than in MAPS, therefore limiting the extent of the voltage drop issue on the power and ground lines. For this reason, the transconductor, whose property of stabilising the DC shaper output is no longer needed, has been replaced by the current mirror stage, which features better noise performance. Use of two CMOS layers, interconnected with a vertical integration technology, provides a large amount of functionalities in each pixel cell, including circuits for further system performance improvement. In particular, a threshold correction DAC has been implemented in both readout channels. The DC voltage at the output of the shaper, which is DC-coupled to a comparator, can differ from channel to channel due to random parameter mismatch [1]. In order to limit the effects of the threshold dispersion σ_{th}, a source follower is placed between the shaper stage and the discriminator and is biased by means of the I_{BIAS} current source. The current value of the I_{DAC} source is set by a 4-bit current steering DAC in each channel. The DAC block contains 15 unity current sources selected through a thermometric code. A decoder is used to convert a 4-bit word to the thermometric code used by the DAC.

4. – Conclusion and perspectives

Two different analog processors for hybrid pixels and monolithic sensors have been designed in view of applications to the SVT Layer0 of the SuperB Factory. They will be fabricated in a 3D, 130 nm CMOS technology, whose properties have been exploited to increase the functional density of the mixed-signal front-end and to improve the immunity of the analog section (and of the sensor in MAPS devices) from digital signals. After fabrication, characterization of the prototypes, besides laboratory tests, will require measuring the sensor detection efficiency through tests on a particle accelerator beam.

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