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Epitaxial hybrid pixel with triggerless readout in 130 nm Cmos technology for the Micro Vertex Detector of the $\overline{P}$anda experiment

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Summary. — The Micro Vertex Detector (MVD) is the innermost one of the $\overline{P}$anda experiment, sitting around the beam pipe. The sensors are arranged in a barrel section with two pixel and two strip layers, and 6 forward disks with mixed pixel and microstrip sensors. For the pixel detector part, a hybrid solution with thinned epitaxial sensors was chosen. The main requirements for the readout include: a pixel size of $100 \cdot 100\,\mu\text{m}^2$, an input charge measurement with 12 b that implies an amplitude resolution of 1 part out of 4096, a working frequency of 155.5 MHz, and a triggerless acquisition. The readout of the pixel detector is based on a front end chip, named Topix, that is under development. The Asic will provide the time position with a resolution of 6.43 ns and a charge measurement with a Time Over Threshold (TOT) technique; it features a matrix of $116 \cdot 110$ pixel cell channels and 311 Mb/s serializers as output ports. A 130 nm Cmos technology has been used to reduce the circuit size and to provide tolerance for the total dose, besides techniques against single event upset have been implemented. A Topix prototype with the full cell has been completely tested for radiation damage before and after irradiation, and a new release has been submitted to build an hybrid assembly. The stringent requirements in terms of space for the MVD lead to an architecture based on optical links. The GigaBit Transceiver (GBT) from CERN has been chosen as the baseline solution for the interface to the data acquisition. Low mass cables based on aluminium on polyimide are under development for the interconnections.

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1. – Introduction to the Micro Vertex Detector

The antiProton ANnihilation at DArmstadt ($\overline{P}$ANDA) is one of the main experiments that will be carried out in the Facility for Antiproton and Ion Research (FAIR) that is an international infrastructure for study in fundamental physics [1]. It is developed from the existing GSI laboratory, and it will host several activities from fundamental research to ion beam radiotherapy. Recently the ring, necessary for the $\overline{P}$anda experiment, has been funded.

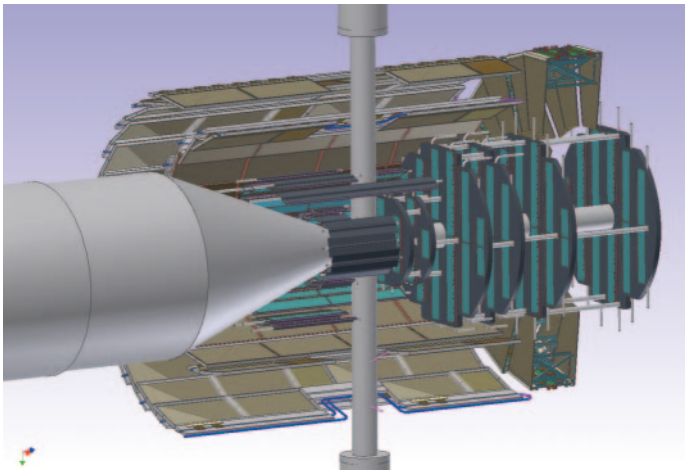

Fig. 1. – The internal view for the mechanical structure of the MVD showing barrels and disks.

$\overline{P}$anda is a fixed-target experiment with his multipurpose detector divided in a target spectrometer with a cylindrical symmetry and a forward spectrometer for particles with a solid angle below 10°. Antiproton-proton and antiproton-nucleus annihilations will be studied, exploiting targets with hydrogen pellets and gold-wire targets. The Micro Vertex Detector (MVD) is the innermost one and it is made by a barrel structure covering the interaction point and a set of forward disks around the beam pipe. There are 4 layers on the barrel region: to manage the high density of tracks, the two internal ones are based on hybrid pixel detectors, while the two external ones are composed by double-sided microstrip detectors. All the disks plan pixel detectors, with the last two completed by a microstrip ring. Summarizing the whole MVD system will have roughly 11 Mch for the pixel sensors, and about 200 kch for the strip sensors.

2. – The mechanical structure

The 4 disks composed only by pixel sensors will be placed inside the barrel making every interconnection with the system very complex (fig. 1). The whole detector is contained into the MVD frame, made of carbon fiber, that is designed for being split in two parts along the vertical plane to allow the assembly of the system around the beam and target pipes [2].

The pixel barrel is supported by a truncated cone structure that follows the beam pipe shape, and the sensors modules set are attached in cantilever mode. The group of pixel disks are brought together by some spacers, and they are mechanically independent from the barrel.

3. – The readout architecture

The major parameters driving the electronics design for the pixels are the continuous readout due to the triggerless architecture, and the high annihilation rate that in average is about $2 \cdot 10^7$ annihilation/s with an antiproton momentum of 15 GeV/c producing a particle flux of $6.1 \cdot 10^6$ particle/$(\mathrm{s} \cdot \mathrm{cm}^2)$.

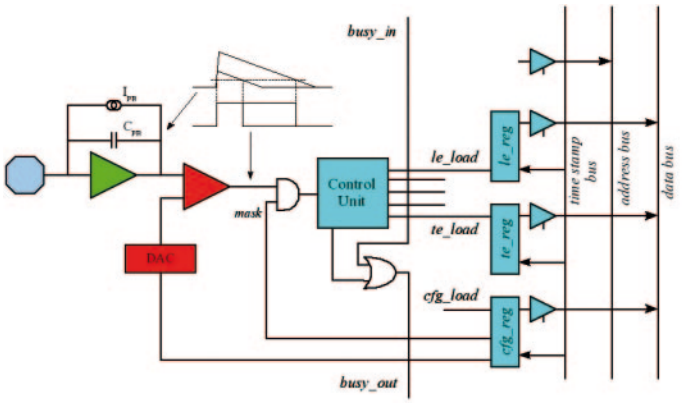

Fig. 2. – The Topix readout circuit implemented in each cell $100 \cdot 100\,\mu\mathrm{m}^2$ wide.

3˙1. *The hybrid pixel sensor.* – The hybrid pixels are built with a basic module composed by a stack of the readout chips at the bottom, the pixel sensor in the middle and the multilayer bus on the top; the chips are then glued on a carbon foam layer embedding a cooling pipe.

The pixel sensor is produced starting from an epitaxial wafer, made by a Czochralski substrate with low resistivity ($\sim 0.01\,\Omega \cdot \mathrm{cm}$) on which a $100\,\mu$m epitaxial layer with high resistivity (2–$4\,\mathrm{k}\Omega \cdot \mathrm{cm}$) is grown [3]. After the production the patterned wafer is thinned with a grinding process to remove the most of the Czochralski substrate to an overall thickness of $120\,\mu$m, with a depletion voltage less than 10 V. To complete the hybrid assembly, a final bump bonding is performed to match the readout with the sensor.

3˙2. *The Topix readout chip.* – The readout chip is called Topix and it is implemented by a 130 nm Cmos technology with the requirements of a pixel size of $100 \cdot 100\,\mu\mathrm{m}^2$, the $\mathrm{d}E/\mathrm{d}x$ measurement by the Time Over Threshold (TOT) technique with 12 b resolution, a system clock of 155.5 MHz, a particle flux of roughly $\sim 6 \cdot 10^6\,\mathrm{hit}/(\mathrm{s} \cdot \mathrm{cm}^2)$ and an input range with a large dynamic of 1–50 fC. Considering an architecture with serial output to minimize the number of connections, the dimension of the event word and the possible line encoding, an average data rate of about 500 Mb/s per chip is expected in the hottest region of the detector.

3˙3. *The Topix readout cell.* – The first block is a charge-sensitive amplifier with its feedback capacitor discharged by a constant current generator, thus producing a triangular signal (fig. 2). The amplifier feeds a comparator where the leading edge indicates the time of the particle hit, and it is used to latch the time stamp. The comparator trailing edge is used to latch the new time stamp in a second register, and the difference represents the Time Over Threshold (TOT) that is proportional to the energy loss [4].

The time stamps are provided simultaneously to all the cells by a Gray counter, changing one bit at a time. The comparator threshold is globally set by a common signal to the whole chip but, to reduce the actual dispersion, it is possible to tune the value individually by a 5 b DAC.

3˙4. *The end of column circuit.* – The pixel cells are arranged in columns, while the columns are organized in pairs so that the same buses for data can serve both the right

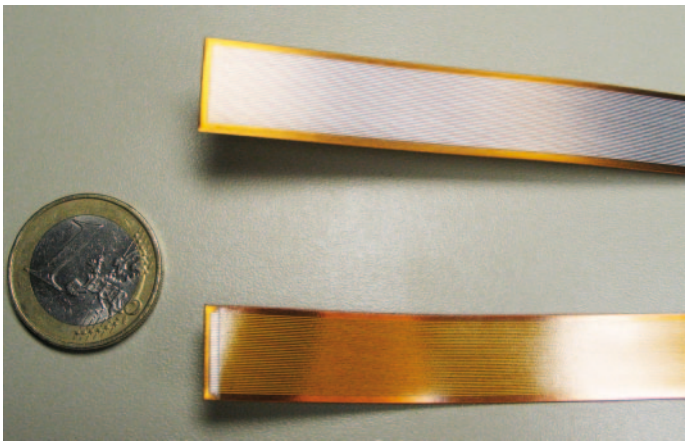

Fig. 3. – A couple of aluminium cable prototypes 1 m long with 18 differential microstrips.

and left sides. Through these buses the information gets the end of column area, where the circuits managing all the cells are placed. In this zone there are the sense amplifiers, the Gray counter, the FIFO buffers and the serializer. The data is written in the FIFO buffers after the Hamming encoding to implement the single error correction. The serial data coming out from Topix are organized in words 40b long, and the information relative to the same event is gathered in a frame. Each word has the following fields: the header (2 b), the unambiguous pixel address (14 b), the leading edge time (12 b) and the trailing edge time (12 b). Every frame can contain up to 64 K words and begins by a header with the frame counter and the error-correcting code, while ends by a trailer with cyclic redundancy check.

At present the module architecture foresees a direct connection from several Topix to the optical transceiver, otherwise a module controller featuring a single serial link could be a solution with the price of added cost and complexity. A possible candidate for the electrical optical conversion is the Giga Bit Transceiver (GBT), which is a major project developed at CERN. The GBT consists of a chipset, including the actual transceiver and the laser driver, produced in a standard technology but with radiation hardening techniques [5].

4. – The prototype results

Topix has been produced as a prototype in a reduced scale, with just 320 pixel cells distributed in 4 columns. The cell has the final size and presents the complete functionality, while it features a simplified end of column logic with a simple parallel output instead of the future serial ports. The tests returned good results with a TOT gain of 152 ns/fC ($\sigma = 6$ ns/fC), with a good linearity up to 100 fC and a small threshold dispersion, around 400 μV, after the tuning of the DAC in every cell. The test for the Total Ionizing Dose (TID) has been performed up to 50 Mrad of integrated dose. For the analogue part the baseline variation was within 3%, the noise changed less than 4% and the average gain value increased by nearly a factor two. The test for the Single Event Upset (SEU) has been performed to evaluate the behaviour of the cross section and energy threshold for the chip. Considering the $\overline{P}$anda flux the measured parameters indicate a final rate of

about 2–3 SEU/(chip · h), that is too much and has to be reduced. These tests have provided the information to drive the design of the Topix new prototype, that has been just received from the foundry and is ready for the functional test. For these reasons all the registers in the new cell have been protected with the triple redundancy, and an error correction has been implemented at the end of column.

Due to the main request for a low material budget, the interconnections inside the volume of the detector have to be made in aluminium rather than in copper. Up to now two technologies were investigated: a laminated metal over a polyimide film and a deposition on top of the insulator. Several prototypes with one single microstrip were manufactured, exploiting either one of the techniques, to evaluate the performances with a folded layout. Even though both of the solutions work properly for data rate beyond 1 Gb/s, the first technology has been chosen since it displays a larger robustness and capability for wire bonding with an increased strength measured by the pull test. At present the prototypes under study are 1 m long in a straight layout implementing a bus of 18 differential pairs, that means 36 lines, with different width and spacing of 100 μm + 100 μm and 150 μm + 150 μm, respectively (fig. 3). These prototypes have been tested with the final transceivers, designed at CERN to implement the Scalable Low Voltage Signaling (SLVS) electrical standard. For this purpose a batch of roughly 200 devices has been tested, to select circuits working at the nominal rate of 320 Mb/s. Due to the interstrip stray capacitance, these cables work well up to a speed of around 700 Mb/s that is above the requirements.

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