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The Design, Fabrication, Installation & Evaluation of the Balance Probe Monitor for Large Centrifuges at a National Laboratory Facility

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The Design, Fabrication, Installation & Evaluation of the Balance Probe Monitor for Large Centrifuges at a National Laboratory Facility

by

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Report

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Dedication

This work is dedicated to all those individuals who have inspired me to be the best version of myself, aim for the stars, and accomplish all of my dreams in the world. You are not forgotten.

Acknowledgements

I would like to thank my advisor, Professor Michael Becker, for his excellent classroom instruction and mentorship at the University of Texas including inputs on this project.

I am grateful to have worked with such talented staff at Sandia National Laboratory: my project mentor William Evans who has truly helped shape me into the engineer that I am today; other members of the Centrifuge Team who developed my skills and abilities to successfully accomplish this project and many other projects; as well as, my managers John Lorio and Todd Sterk for giving me endless resources to ensure my professional development.

I would also like to express my gratitude towards Sandia's Critical Skills Master's Program (CSMP) in conjunction with the GEM Consortium for sponsoring and funding me to expand on my passions in Electrical Engineering at the University of Texas. Without all of you, none of this would have been possible. I am honored to have had the opportunity to cross all of your paths on my journey.

Abstract

The Design, Fabrication, Installation & Evaluation of the Balance Probe Monitor for Large Centrifuges at a National Laboratory Facility

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The University of Texas at Austin, 2016

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Balance Probe Monitors were designed, fabricated, installed, and evaluated at Sandia National Laboratories (SNL) for the 22,600 g kg (50,000 g lb) direct drive electromotor driven large centrifuges. These centrifuges provide a high onset/decay rate g environment. The Balance Probe Monitor is physically located near a centrifuge's Capacitance Probe, a crucial sensor for the centrifuge's sustainability. The Balance Probe Monitor will validate operability of the centrifuge. Most importantly, it is used for triggering a kill switch under the condition that the centrifuge displacement value exceeds allowed tolerances. During operational conditions, the Capacitance Probe continuously detects the structural displacement of the centrifuge and an adjoining AccuMeasure 9000 translates this displacement into an output voltage. [1]

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Chapter 1: Introduction

Motivation for the Balance Probe Monitor

Sandia National Labs maintains large centrifuges that have been in operation since the late 1960's, and 1982 respectively. Updates, intended as a preventative measure to insure continued safe operations, longevity and graceful aging were implemented. Fundamentally, the Balance Probe Monitor serves as an automated kill switch option for large centrifuges. Several key design considerations were employed.

Key Design Considerations for Continuous Monitoring System

1. Reliability – Continuously monitor the centrifuge to ensure balance compliance.
2. Safety – Kill Switch to maximize centrifuge longevity and protect the surrounding facility and human operators.
3. Performance – Successfully kill power to the centrifuge if tolerance conditions were exceeded.

Continuous Monitoring System

For the system to continuously monitor the centrifuge, the system relies upon a Commercial Off-The Shelf (COTS) Capacitance Probe attached to an AccuMeasure 9000. As a centrifuge spins at a operator designated RPM, an AC signal can be detected with a frequency equivalent to RPM/60 (see the Appendix for more information). However, as the centrifuge becomes unbalanced, runout begins to be seen in the waveform as it is no longer a perfect AC signal due to the centrifuge being off-center. To

test for this displacement, a Capacitance Probe attached to the AccuMeasure 9000 Capacitance Sensor Amplifier monitors displacement at the base of the centrifuge.

The AccuMeasure System operates on the principle of parallel plate capacitor measurement. The electrical capacitance formed between an AccuMeasure (capacitance) Probe and a target surface varies as a function of the distance (gap) between these two surfaces. The concept of measurement is depicted below in Figure 1.

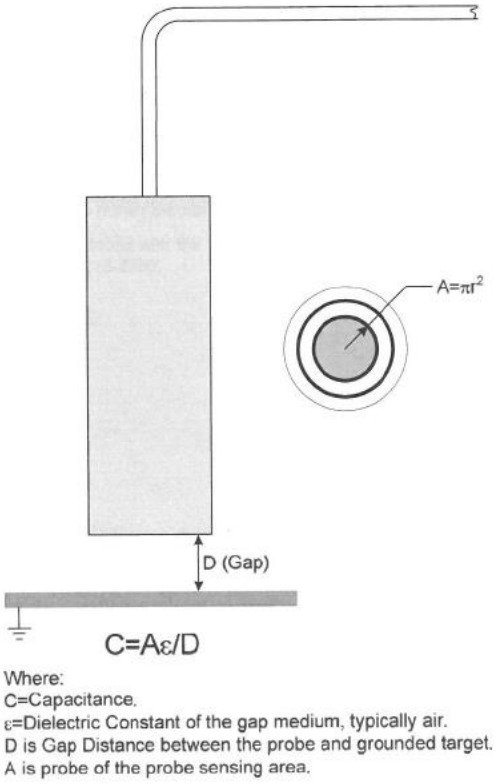


Figure 1: Capacitance Probe Physics

From there, the AccuMeasure System measures the electrical impedance of the capacitance between a sensing electrode in the probe and a ground referenced point. The magnitude of the impedance is directly proportional to the reciprocal of the capacitance

value: $Z_C = 1/\omega C$. Omega (ω) is proportional to the measured frequency at the Capacitance Probe. Simplifying from the previous equation gives us $Z_C = D/\omega \epsilon A$. The AccuMeasure Probe amplifier then produces a DC voltage that is linearly proportional to the average value of the probe gap impedance, as well as an AC voltage variation from the DC voltage that is directly proportional to the amplitude of the centrifuge vibration. The AccuMeasure 9000 circuitry eliminates the effects of both the probe cable capacitance and the stray capacitance at the edge of the probe sensing area that could cause non-linearity of the gap and vibration measurements. The standard full scale gap probes from 25um to 5mm (0.001 to 0.200 inches).

The measurement data from MTI Instruments (the manufacturer of the AccuMeasure9000) can be seen below in Figure 2.

Measurement Data:

Noise Level: .05 (mV RMS) **Sensitivity:** 20.0 (mV/µm)

Point Number	X µm	Y Volts
1	50.	1.000
2	100.	2.000
3	150.	3.000
4	200.	4.000
5	250.	5.000
6	300.	6.000
7	350.	6.999
8	400.	7.999
9	450.	8.999
10	500.	10.000

Uncertainty: .05%

Figure 2: Measurement Data (50um = 1 Mil peak to peak = 1 Volt)

The data collected from the Capacitance Probe is used to validate that the centrifuge operates within its environmental envelope. Most importantly, it is used for triggering a kill switch under the condition that the centrifuge displacement value exceeds allowed tolerances. During centrifuge operation, the Capacitance Probe continuously detects the structural displacement of the centrifuge and translates this displacement into an output voltage at the AccuMeasure.

The AccuMeasure then sends the output voltage to the Balance Probe Monitor to validate that the Capacitance Probe is working and both maintains the desired DC voltage signal necessary for power on and validates that the displacement balance is maintained within a desired operating threshold. The key function of the Balance Probe Monitor is to provide for a kill switch in the condition that the centrifuge is unbalanced during operations; this switch not only limits wear and tear but also prevents catastrophic structural failure, and eliminates the potential for operator injury. At any point when the Capacitance Probe signal exceeds the desired operating threshold, the monitor will open an interlock and automatically remove power, shutting off the centrifuge. When the Balance Probe Monitor detects an input signal within the desired operating threshold the centrifuge will function as intended.

Chapter 2: The Centrifuge Balance Sensor System

The centrifuges are shown below in Figure 3, as well as a set up of the laboratory. A closer look at one of the two large centrifuges can be seen in Figure 4.

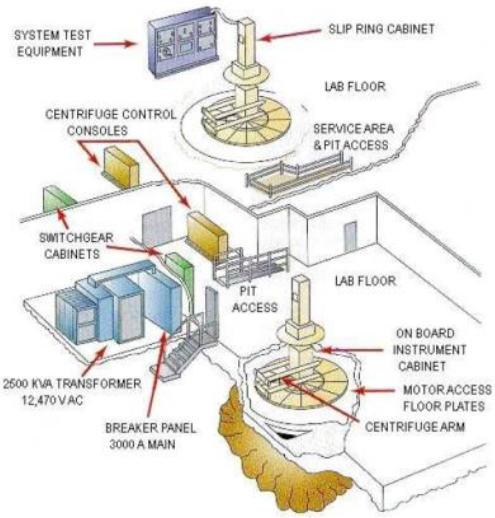


Figure 3: Large centrifuge facility at Sandia. [1]

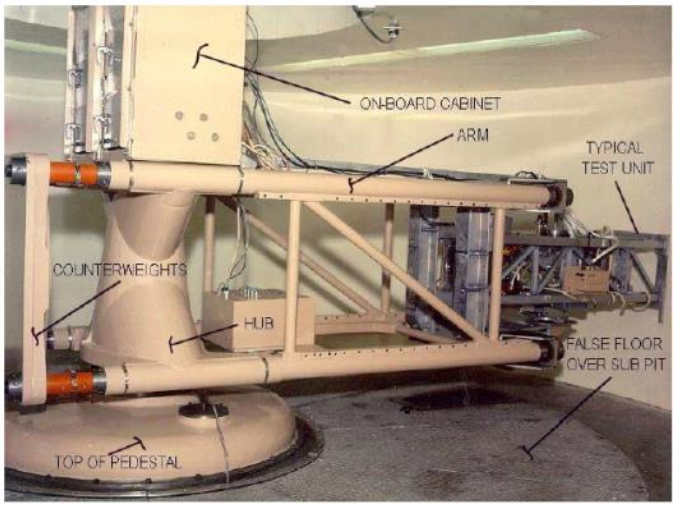


Figure 4: Motor-driven centrifuges. [1]

CENTRIFUGE & BALANCE PROBE CONFIGURATION

A centrifuge is constructed of a rotating Centrifuge Arm mounted and cantilevered from the core structure of the centrifuge. The Capacitance Probe is positioned beneath a floor at the base of the centrifuge's structure at the ground level.

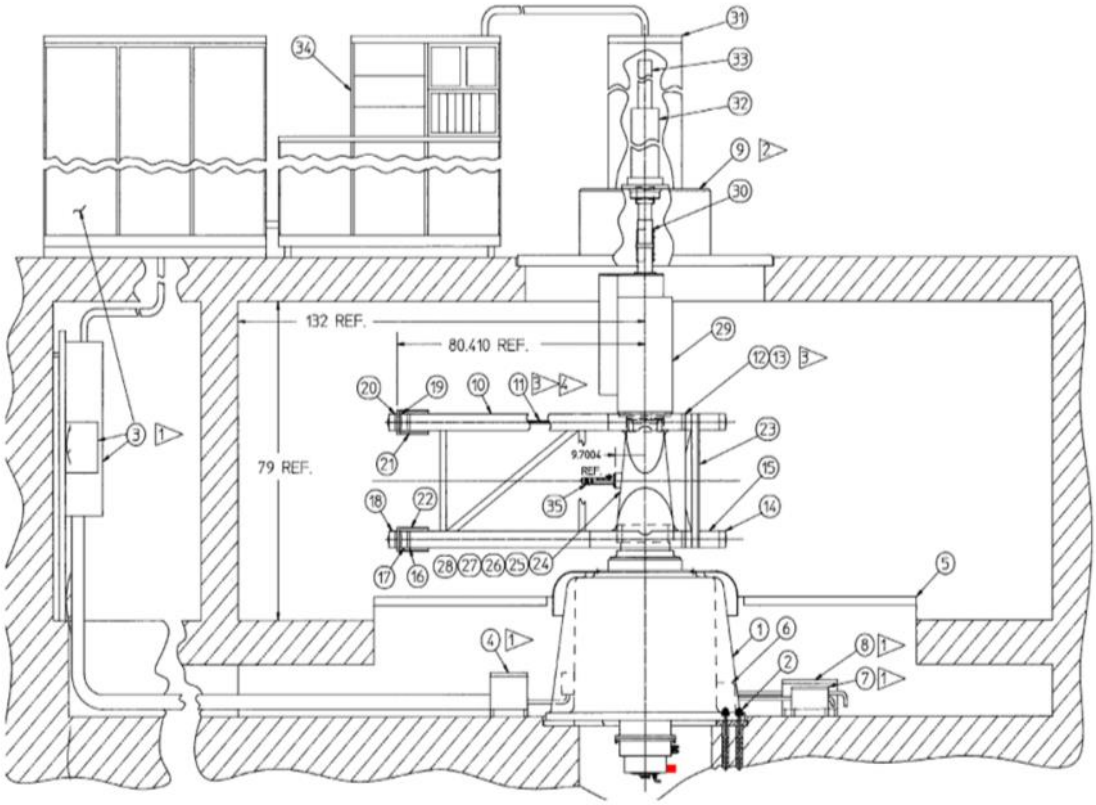


Figure 5: The Capacitance Probe is attached to the bottom of the centrifuge as shown in red.

The centrifuge's Capacitance Probe serves as a crucial sensor for insuring the centrifuge's sustainability. A Balance Probe Monitor (BPM) is adjoined with the Capacitance Probe but located at the Centrifuge Control Console. As previously stated, the BPM utilizes the measured displacement superimposed with the DC offset voltage to

both validate operability of the Capacitance Probe as well as to trigger a kill switch in the condition where operating tolerances are exceeded. The centrifuge and Capacitance Probe configuration are shown in Figure 5.

During operational conditions, the Capacitance Probe continuously detects the structural displacement of the centrifuge and the detection system translates this displacement into an output voltage.

BALANCE PROBE MONITOR DESIGN REQUIREMENTS

The functional and performance requirements of the Balance Probe Monitor (BPM) are specified as follows:

1. In the power on condition, the BPM shall detect a constant voltage difference of 1 V_{DC} from the Balance Probe to validate operability of the Probe.
2. In the operational condition, the BPM shall separate the AC displacement signal from the DC voltage for the purpose of evaluating displacement tolerances.
3. The BPM shall be capable of monitoring displacements in the range of 0.5 mil – 2 mil to allow for a range of user selected displacement thresholds that correlate to specific test conditions.
4. The BPM shall provide a kill switch (power off) when safe operating limits are exceeded.
5. The BPM shall have a momentary off switch allowing for the operator to reset the system as required.
6. The BPM shall operate between 0 – 5 Hz.

CONCEPTUALIZATION

The amount of displacement measured by the Capacitance Probe is expected to fluctuate based upon the RPM setting and other factors central to the operation of the centrifuge. The two input feeds to the input stage of the BPM are the Capacitance Probe signal and the Capacitance Probe return signal. The return signal includes any anticipated additive noise component. By design, the net DC voltage between the Capacitance Probe and the return is 1 V_{DC}. By utilizing a Differential Amplifier with a gain of 1, a 1 V_{DC} offset voltage is established (See Figure 6).

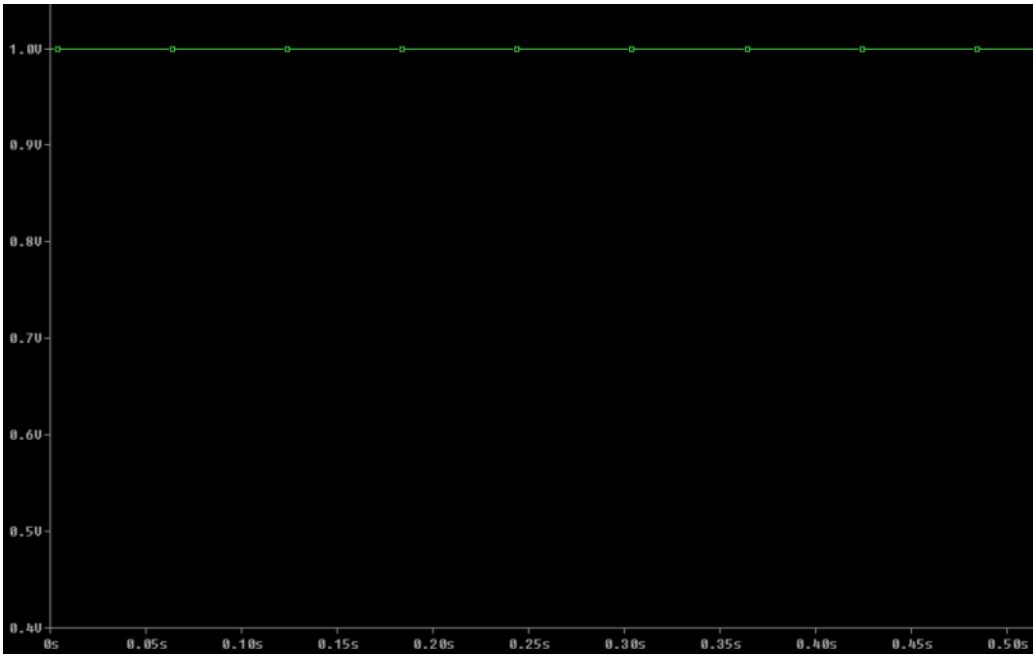


Figure 6: 1 V_{DC} offset voltage required for the power on condition.

In order to limit wear and tear on the centrifuge and more importantly to prevent catastrophic structural failure, a threshold voltage limit is established. Once operations exceed the threshold voltage, an automated kill switch is triggered. The acceptable range

of operation is between 0.5 mil – 2mil (50 μm = 1 Mil = 0.5 V_{DC}) which translates to 0.5 V_{DC} – 2 V_{DC} peak-to-peak. These are represented below in Figures 7 and 8 respectively.

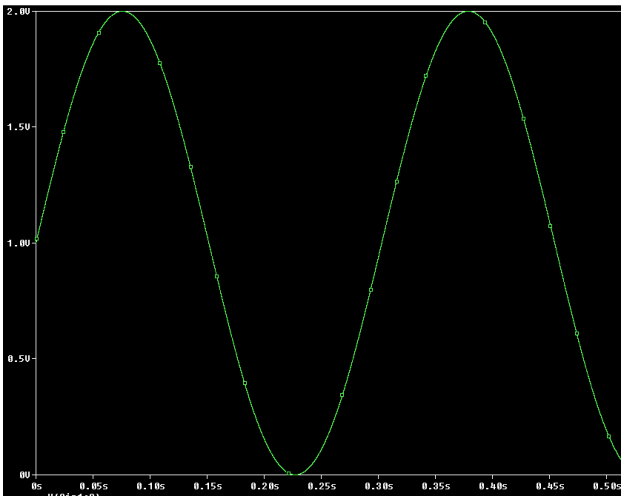


Figure 7: 2 V_{DC} Peak-to-Peak with 1 V_{DC} offset (2 mil threshold).

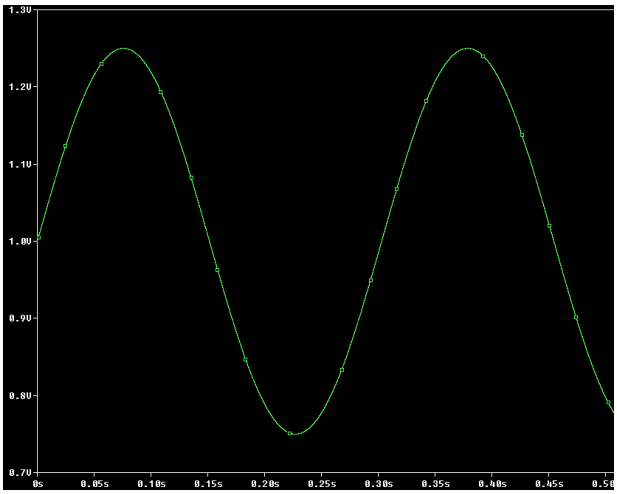


Figure 8: .5 V_{DC} Peak-to-Peak with 1 V_{DC} offset (0.5 mil threshold) .

The AC signal is generated as the Capacitance Probe continuously detects displacement on the centrifuge structure during the centrifuge operation. The maximum allowable displacement is no greater than 2 Mils and is equivalent to 1 V_{DC}. The signal measured by the BPM is representative of both the AC and DC components of the signal.

As previously stated, a Differential Amplifier may be used to amplify the difference of two signals as shown in the configuration in Figure 9, where $V_{out} = A (V_2 – V_1)$ and $A = R_3/R_1$ when $R_1=R_2$ and $R_3=R_4$. In terms of the electrical circuit design, this desired offset is being achieved by utilizing a Differential Amplifier with a gain of 1. As shown in Figure 9, this difference in voltage is determined between the voltage input of the Balance Probe System (BPS) connected at V_2 and the BPS return value, V_1 to the inverting terminal. When the Capacitance Probe is within range, this configuration will deliver a $1V_{DC}$ offset at V_{out} (Refer to Figure 6).

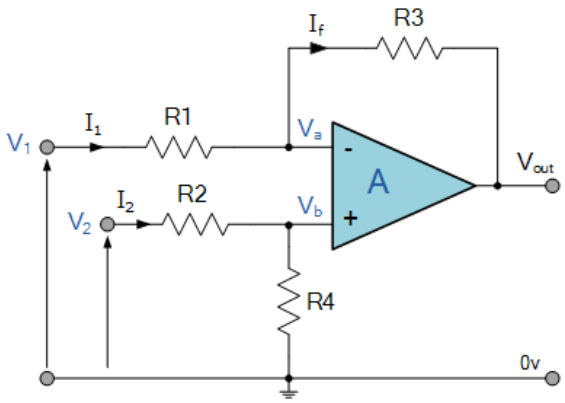


Figure 9: Differential Amplifier. [2]

In the event that the threshold limit ever exceeds the desired operating voltage (i.e. the AC voltage is unstable and becomes larger than the allowable threshold limit) the Balance Probe Monitor will open an interlock that will remove power to the device initiating a kill switch. This prevents the centrifuge's structure from becoming damaged due to an unbalanced condition. As previously stated, the unbalanced condition will be detected by the Capacitance Probe. The time varying displacement of the centrifuge's structure is measured in mils. The sensor outputs the displacement in terms of an AC

voltage signal as shown below in Figure 10. The centrifuge operates under the condition that the centrifuge is balanced within an acceptable threshold and the required Balance Probe Monitor input voltage is satisfied.

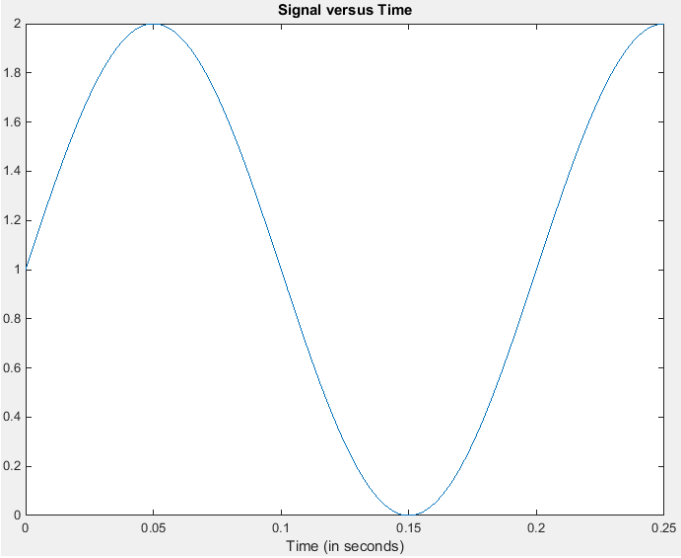


Figure 10: AC displacement shown as an output Signal (Voltage) versus Time.

When both conditions are met, i.e. the 1 V_{DC} and the V_{PP} voltage threshold conditions are met, the AND logic gate will detect a high signal from both the Comparator and Inverse Comparator with Hysteresis indicating an “operate” condition for the centrifuge.

The Inverting Comparator with Hysteresis is where the threshold can be user adjusted by altering a potentiometer. In the case where the Kill Switch is triggered, the operator will have to press a momentary off switch to reset power to the centrifuge.

The momentary off switch ensures that the operator cannot leave the switch on following a fault; the momentary off switch is a critical design component that avoids the potential to block triggering the kill switch with the detection of future faults. The

momentary off switch minimizes the possibility of human error. A SR Latch has been utilized to allow for the system to be analyzed if power is killed in response to an imbalance of the system preventing running the centrifuge without resetting the switch mentioned above – meaning an operator has acknowledged an imbalance in the system. Power can only be provided to one of the two circuit loops at a time. The switch is used to reset the SR latch to its initial condition after each detected threshold exceedance or detection of no offset voltage. For example, given a 2 mil threshold setting, power will be cut to the centrifuge once the SR Latch is triggered when the threshold voltage is exceeded.

Chapter 3: Balance Probe Monitor Preliminary Design

Preliminary Design

Now that our requirements have been laid out with a basic conceptualization, a preliminary circuit design responsive to the requirements can be established. The BPM circuit design must interface to both the centrifuge and AccuMeasure 9000/Capacitance probe (also known as BPS). This interrelationship is shown in Figure 11.

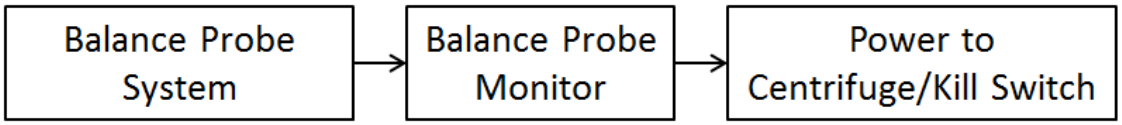


Figure 11: Interrelationship between BPS, BPM and Centrifuge Power.

Balance Probe Monitor

A further component breakdown of the BPM design can be seen in Figure 12.

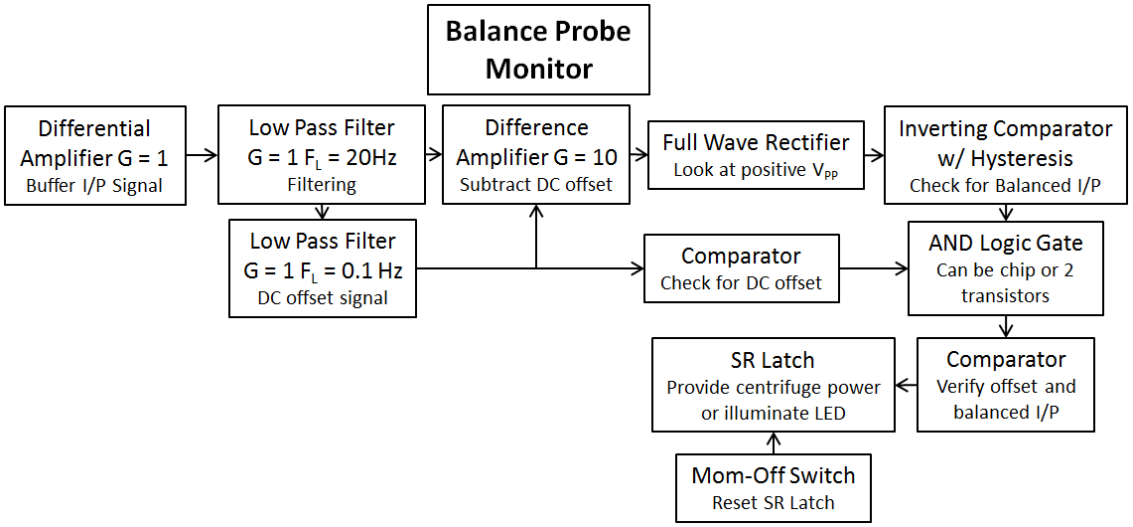


Figure 12: BPM component breakdown.

SUBSYSTEMS

Input Buffer – Differential Amplifier

The Capacitance Probe measures the displacement of the Centrifuge. The Differential Amplifier box shown below in Figure 13 represents the first input stage into the BPM. The output of the Capacitance Probe provides the input into the BPM from the AccuMeasure. The initial signals are sent into a Differential Amplifier with a gain of 1.

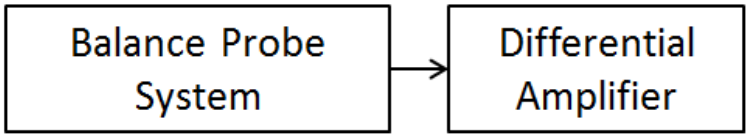


Figure 13: Signal sent from the Centrifuge and Capacitance Probe (BPS) into the 1st component of the BPM.

The output signal of the BPS, is buffered into the BPM through the Differential Amplifier. A net 1 V_{DC} signal is detected from the Differential Amplifier (Figure 9) by subtracting the signals from the BPS signal (non-inverting terminal) and the BPS return signal (inverting terminal). The user is able to change the offset voltage as needed (Figure 2) by setting the Capacitance Probe at different distances from the base of the centrifuge as shown above in Figure 5. When the BPS is within range correlating to an offset voltage (50um from the zeroed AccuMeasure reference), this configuration will deliver a 1 V_{DC} offset at V_{out} (refer to Figure 6).

The signal generated by measurements of the centrifuge displacement is superimposed onto the 1 V_{DC} offset voltage. This displacement signal is generated from the centrifuge as it spins. The mechanical structure holding the arm of the centrifuge begins to get displaced as the centrifuge spins at greater speeds. This displacement is

measured by the BPS which detects the structural displacement in mils. Our design specifications have limited our displacement threshold to .5 – 2 mils or .25 – 2 V_{DC} Peak to Peak (It should be noted 1 mil = .5 V_{DC}). This structural displacement in turn creates an AC signal that is also fed into the BPM. The 2 signals, when combined create a waveform as seen in Figure 6. The 1 V_{DC} signal sent from the BPS acts as an offset voltage; the AC signal then fluctuates between 0 and 2 volts (2 V_{PP}) when the displacement is at 2 mils due to the offset. The AC signal will have larger or smaller V_{PP} the faster or slower the Centrifuge spins.

Implications of Offset Voltage

The logic seen below in Figure 14 will be an AND logic gate and enable or disable the operation of the centrifuge. The balance (under threshold value) will need to send a '1' indicating the structural displacement is within spec. In addition, the BPS will need to send a '1' indicating that the probe monitor signal is present (offset voltage). The BPS accomplishes this by outputting an offset of 1V_{DC} telling the user that the probe is on and correctly taking measurements. The AND logic gate indicates both conditions must be met for the centrifuge to run. See Table 1 and Figure 14.

Balanced (B)	Probe Monitor Signal (S)	Run
0	0	0
0	1	0
1	0	0
1	1	1

Table 1: BPM AND Logic. B = under threshold value, S = offset voltage.

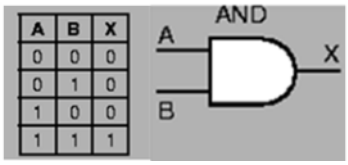


Figure 14: AND logic gate and logic table.

Noise Reduction, Separation of AC/DC Signal

Our next steps are to separate our superimposed AC and DC signals from the output of the Differential Amplifier signal seen in Figure 10. These signals are separated to allow the validation each condition (balanced and probe monitor signal) is met. This will require two separate operations. To isolate these signals we first need to calculate the frequency that we are operating at in Hertz. We can reference data from the balance probe signals seen in Figure 15 below to calculate this.

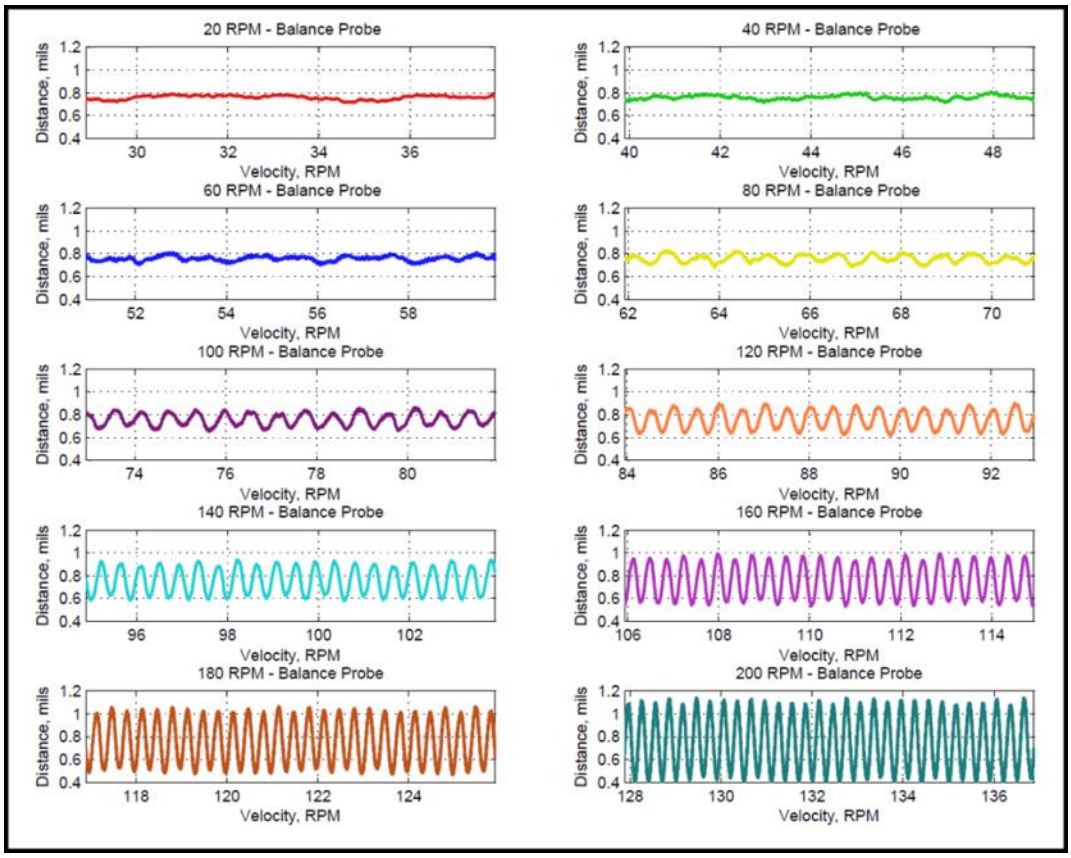


Figure 15: Centrifuge displacement for changing velocity (RPM) to mils.

To calculate Hertz we must recall the relationship between Hertz and RPM is Frequency = Hertz = RPM/60s. Figure 15 shows us that the maximum measured RPM the centrifuge runs at is 200. F = 200/60 = 3.33 Hertz (we can now see we are dealing with VERY small frequencies). With this information we need to bring two factors into consideration: 1 for the AC portion and 1 for the DC portion. For the AC component of the signal we want to ensure we eliminate noise and jitter to ensure accurate measurements and readings. For the DC component we want to eliminate the AC signal all together. We also need to consider that we might raise our RPM at a later date. Knowing this information we want two separate paths for the signal to follow to get two

different outputs to compare at the end (AND logic gate). To ensure that the AC signal path attenuates the out-of-band noise while factoring in a margin of error on the RPM rates as well as to allow greater RPM rates as needed at a later date we will use a 20 Hz Low Pass Filter (LPF with f_c = 20 Hz). This design, set the cutoff frequency to be greater than twice of the measured frequency to be compliant with the Nyquist criterion.

Recall that we are checking that the system is balanced (AC signal) and that the Capacitance Probe is properly connected and working (DC offset signal). Using the 20 Hz Low Pass Filter we are eliminating unwanted AC signals along one of the two output paths. However, the DC signal is still present here and thus will need to be eliminated later along this path. On the other output path we want to eliminate the AC signal to check that the BPS DC signal is present. To isolate the DC signal we want to eliminate the AC signal which can be accomplished by utilizing a second Low Pass Filter. We will use a 0.1 Hertz Low Pass Filter (LPF with fc = 0.1 Hz). In order for any AC signal to get through the 0.1 LPF the RPM rate would thus have to be less than 6 RPM (RPM = 0.1*60) which is negligible due to the fact the system will not be run at this setting. A representation of these Low Pass Filters can be seen in Figure 16.

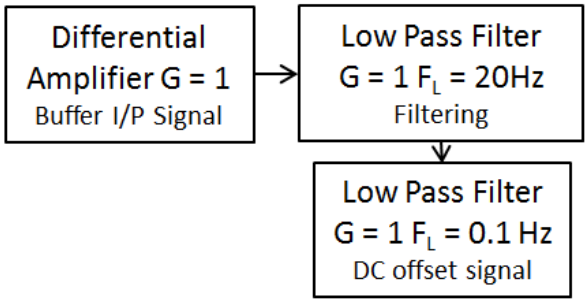


Figure 16: Differential Amplifier passing signals through the Low Pass Filters.

Following the 20 Hertz Low Pass Filter the output waveform should be a representation of Figure 7 above and the 0.1 Hertz Low Pass Filter should have an output waveform represented by Figure 6. Figure 7 shows that the 20 Hertz LPF only allows the desired AC signal to pass (still containing the DC offset) while Figure 6 only displays the DC voltage component as the AC component has been filtered out.

From the two previous LPF we need to progress the signals down the line to test the now separate AC and DC signals. Utilizing the 20 Hz LPF we removed any noise and jitter that was present but did not remove the DC voltage yet. To do this, we used a Difference Amplifier (as seen in Figure 17) by subtracting and cancelling the DC voltage in the 20 Hz LPF from the DC voltage in the 0.1 Hz LPF which leaves us with 0 V_{DC} since the two DC voltages from the two separate paths are identical. This will in turn shift the AC voltage down to fluctuate at the origin once the signal has passed through the Difference Amplifier. The Difference Amplifier will be configured to have a gain of 10.

Offset Voltage Validation

Referencing back to the DC voltage from the 0.1 Hz LPF we will send the voltage to a comparator (as seen in Figure 17). The voltage is being sent to a comparator to test if the expected input offset voltage from the BPS is present. If the voltage is not high enough the comparator will not trigger a favorable output and the centrifuge will not be able to run. The input voltage from the 0.1 Hz LPF will be 1 volt DC. The input from the LPF will be called V_+ and the lower value will be V_- and go into the inverting input of the Op-Amp. The comparator works similar to a logic gate. If $V_+ > V_-$ the comparator outputs a '1' or whatever the top rail value is (if the DC offset is present). If $V_- > V_+$ the

comparator outputs a '0' or whatever the bottom rail value is. Because we only want the device to work if $V_+ > V_-$ we know that the offset voltage must be larger than the voltage created from the current divider at the inverting input (V_-) of the Op-Amp. For this device we are using a uA741 Op-Amp that has a 15V and -15V rail reference. So if $V_- > V_+$ is true -15 volts will be output from the comparator. The logic aspect of this design will be addressed at the AND logic gate section below.

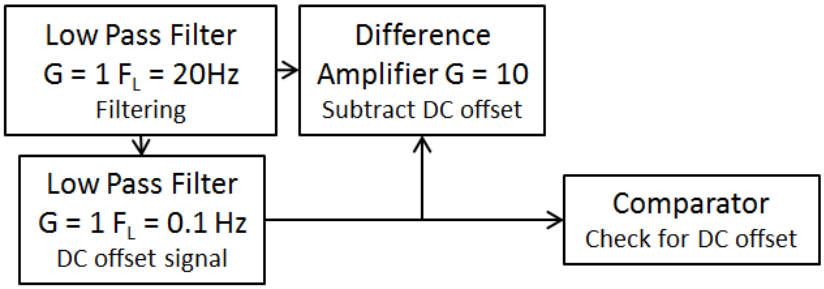


Figure 17: The two LPF signals output an AC only signal from the Differential Amplifier. Meanwhile the comparator has a DC input and outputs a DC signal based on the $V_+ > V_-$ or $V_- > V_+$ orientation.

Amplification and Signal Conditioning

As previously mentioned, the Difference Amplifier is only outputting an AC signal (the DC signal subtracted itself out from the two input signals) with a gain of 10 that is now at the origin instead of offset by 1 V_{DC}. However, this AC signal is oscillating between -10 and 10V and we want to only have positive voltage for when we compare at a logic gate as well as convert it to a "DC like" signal for use at a comparator. In order to convert the voltage to a fully positive voltage as well as have a "DC like" output we want to use a Full Wave Rectifier as seen in Figure 18. The output will be used to measure against the max allowed displacement with the comparator.

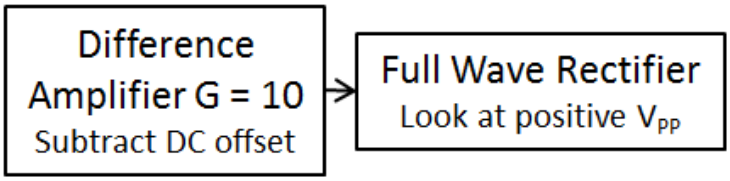


Figure 18: Differential Amplifier is converting the AC signal to a fully positive signal.

Centrifuge Balance Validation

The next step, prior to the AND logic gate is to test if the balance signal is a '1' (balanced) or '0' (not balanced). To do this we will need to compare the Full Wave Rectifier output signal (with the gain of 10 from the Difference Amplifier) and compare it with a DC voltage on the non-inverting input of an Inverting Comparator with a hysteresis Op-Amp. We can alter the voltage on the non-inverting op-amp input by creating a voltage divider. As the tolerance standards change for this device a potentiometer can be altered in the voltage divider to reflect the allowed structural displacement of the centrifuge. To ensure the centrifuge balance and oscillation never grows beyond the allowed tolerance we have to set V_+ input on the comparator to be the highest allowable voltage (displacement) so that if the input signal from the centrifuge is beyond that value the centrifuge will not be able to operate. In order to accomplish this we will utilize an inverting comparator. This means if the input signal (V_-) is below the threshold it will run because $V_+ > V_-$ still and '1' can then be output. In the case that V_- is greater than V_+ a '0' will be output. This block diagram can be seen in Figure 19.

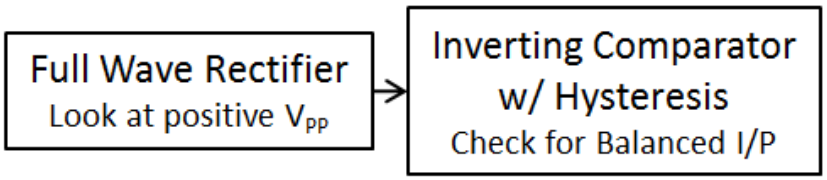
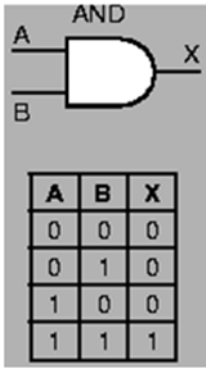


Figure 19: FWR signal is being compared at an inverting comparator to see if the centrifuge displacement is within tolerance.

Authenticate Operational Status – AND Logic Gate

In order to authenticate operational status, the output of the two comparators (Comparator and Inverting Comparator with hysteresis) will be evaluated. The power-on condition is indicated when both comparators simultaneously output a "1". Consequently, an AND logic gate as shown in the truth table in Figure 20 below, serves the purpose of our design requirements.



A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

Figure 20: List of the logic gate. Referencing the table we want, an AND logic gate.

Referencing Figure 20, an AND logic gate is incorporated into the Preliminary Design as one of the final stages of the BPM. The Inverting Comparator will signify the Balanced Centrifuge (B) and the Comparator signal will signify the Balance Probe Signal (S), these two together are the inputs for the AND logic gate (Figure 21). Testing the truth table, the AND gate will either allow or not allow the centrifuge to run contingent

upon the required conditions being met. If the conditions are not met, the AND gate will prevent the ability to power the centrifuge. If the conditions are met the AND gate sends a positive signal to the final comparator that verifies that the offset voltage is present and the centrifuge is balanced and will then send 5 Volts to the SR Latch ensuring that the centrifuge can run.

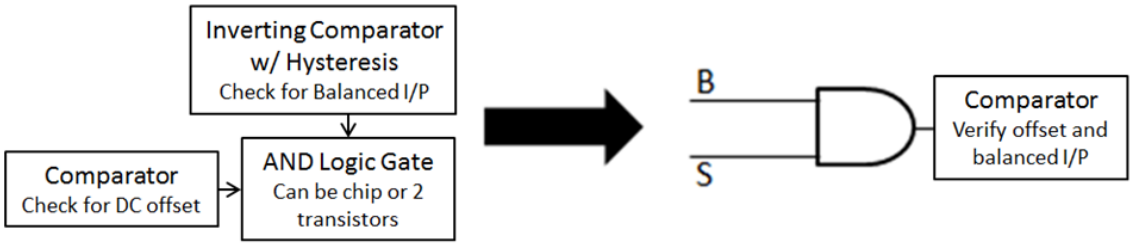


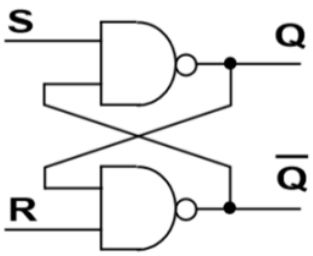
Figure 21: AND logic gate checking the Balance (B) and Signal (S) for '1's and '0's.

To apply our AND logic gate we will use 2 BJT transistors as each of our B and S inputs. We know that if a '0' is output from either of the comparators the output is -15 volts from uA741 Op-Amp. We also know that $V_{BE(on)}$ is approximately 0.7 Volts. Meaning in the case that -15 volts are output from either of the comparators, there will not be enough voltage to allow for current to flow over the BJT transistors. Alternatively, if the output is '1' the uA741 Op-Amp comparators will each output 15 volts which will turn on the BJTs and allow current to flow. However, if the balance comes out of spec or the Capacitance Probe loses signal the values will switch to '0' and immediately cause the SR Latch to kill power and safeguard the centrifuge.

Manual Reset Switch

The SR Latch causes the value to "latch" (remain constant) which is the value it brings to our design. If the system becomes out of balance, power will be killed until it is

manually reset by applying a voltage to one of the inputs. It uses the logic seen below in Figure 22 to accomplish this. The cycle will then repeat over and over again to provide power and kill power through the use of set and reset voltages. The applied voltage will come by pressing a switch that remains in the off state until it is activated by an operator. Pressing the switch completes a circuit loop sending 5V or a '1' to the SR Latch at S allowing for a reset. The final comparator sends its signal on R.



S	R	Q^+	$\overline{Q}^+$	Function
0	0	1-?	1-?	Indeterminate State
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	$\overline{Q}$	Storage State

Figure 22: SR logic.

The working design concept can be seen below in full in Figure 23.

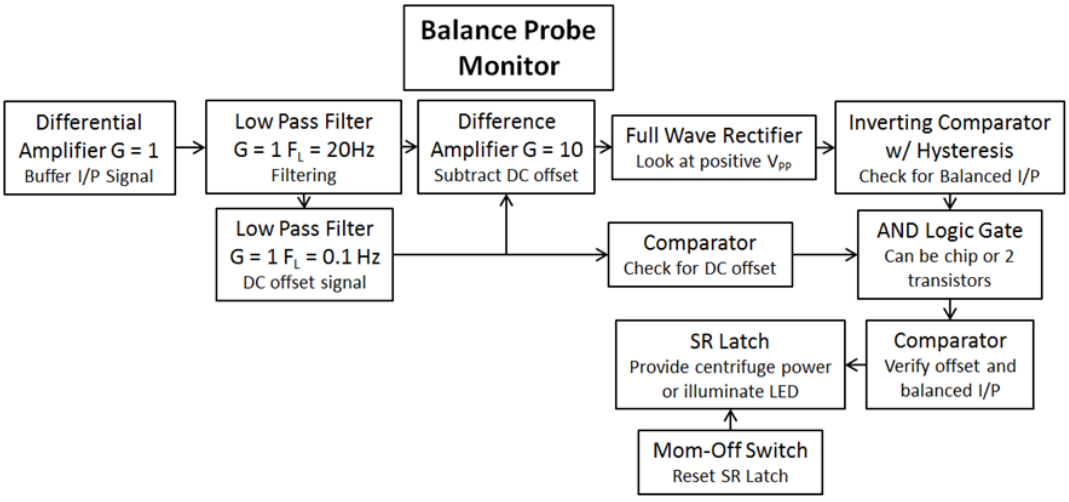


Figure 23: Full design concept.

The actual circuit is shown and displayed in the simulation section – Chapter 6.

Chapter 4: Power Supply

The final crucial component to our design is what power supply we will use. For this project we used a COTS power supply. The Astrodyne MTCC-0311 which supplies power levels of +/- 15V as well as +5V and has a ground connection. This power supply was supplied by Sandia National Laboratories for this project and that was the reason that it was used. All components were designed to meet the supply voltages.

POWER SUPPLY PRELIMINARY DESIGN

Another option besides using a COTS power supply would be to design a power supply. The following section will discuss how one could design and create their own power supply for the BPM if a COTS power supply was not available. For this option we will design two from scratch to accomplish our tasks. After working through our block diagrams above we will need a rail to rail voltage power supply (+V/-V) to supply some of our op-amps as well as a rail to ground power supply ($+V_1$/0V). This will require two separate designs to accomplish this. For this task we will follow the standard design laid out in Professor John Pearce's Design Casebook [2]. This block diagram for the AC to DC converter can be seen below in Figure 24.

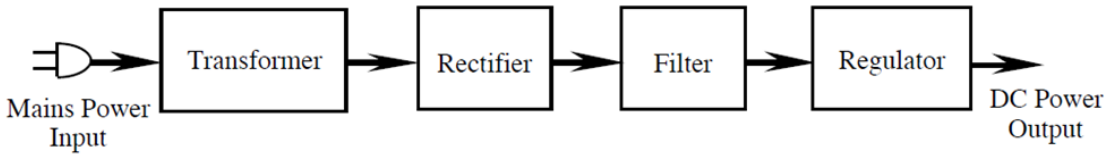


Figure 24: Block diagram of a standard analog DC power supply.

The transformer will follow having a set number of n windings on the primary and secondary. The primary and secondary sides will each have their grounding attached to their separate ground nodes respectively. This is seen below in Figure 25.

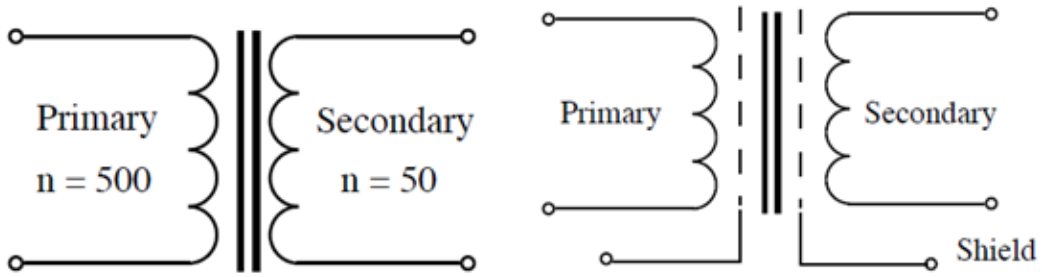


Figure 25: The primary and secondary are separately shielded and each have n windings.

Going through the transformer we will use a full wave bridge to achieve full rectification followed by filtering with capacitors to smooth out the rectified signal to a smooth DC like signal (note: as the load requires more current the smooth DC like signal will get loaded down and become less smooth). The capacitor values will be calculated at a later time when the voltages and current load is known. Then it will follow $\Delta V=I/(2fC)$ to derive the values. The rectification and filtering designs for the 2 power supplies of interest discussed previously will be designed to follow Figure 26 below.

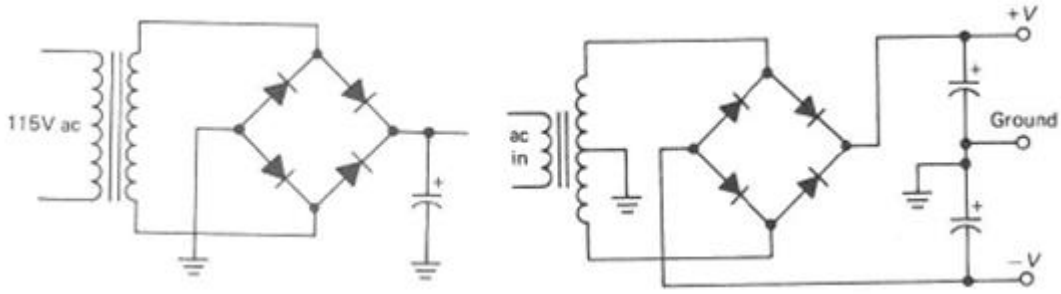


Figure 26: Power supply design set ups used to build our 2 power supply sources.

From the outputs seen in Figure 26 we will do the final step and use voltage regulators for voltage stability. Popular voltage regulators to consider are the LM317 and LM137 due to their high voltage input allowance and large range of voltage output. This allows great flexibility in the design. Each output voltage (+V,-V, and $+V_1$) will get a voltage regulator.

This will be the basis that will be followed to design the power supplies to provide power to the circuit laid out in Chapter 3. The actual circuit is shown and displayed in the simulation section – Chapter 6.

Chapter 5: Parts Selection (COTS)

This section will discuss all of the parts selected for this project and go into detail why certain parts were selected. Figure 27 shows all of the parts in the Bill of Materials (BOM).

1	BOM			
2	Part #	Quantity	Description	
3				
4	Op-Amps			
5	uA741CP	7	Rail to Rail -18/18V	
6	MCP6021-I/P	1	Ground to Rail 0/5V	
7				
8	Resistors			
9	RLR07C1200GSB14	1	120	1/4W Axial 1% tolerance, low noise, low failure
10	RNC60H2400FMB14	2	240	1/4W Axial 1% tolerance, low noise, low failure
11	RLR07C7150FSR36	2	715	1/4W Axial 1% tolerance, low noise, low failure
12	RLR07C1001FSB14	6	1k	1/4W Axial 1% tolerance, low noise, low failure
13	RLR07C1331FPR36	1	1.33k	1/4W Axial 1% tolerance, low noise, low failure
14	RLR07C2611FSR36	1	2.61k	1/4W Axial 1% tolerance, low noise, low failure
15	RLR07C1002FSB14	16	10k	1/4W Axial 1% tolerance, low noise, low failure
16	3005P-1-203	1	20k Pot	Trimmer Potentiometer, 3005 Series, 20kohm 1W PC PIN
17	RLR07C2002FSB14	2	20k	1/4W Axial 1% tolerance, low noise, low failure
18	RLR07C5602GSR36	1	56k	1/4W Axial 2% tolerance, low noise, low failure
19	RLR07C8202GMR36	2	82k	1/4W Axial 2% tolerance, low noise, low failure
20	RLR07C1003FSB14	3	100k	1/4W Axial 1% tolerance, low noise, low failure
21	RLR07C1603GSR36	3	160k	1/4W Axial 2% tolerance, low noise, low failure
22				20k pot
23	Capacitors			
24	M39003/01-2338/TR	4	0.1uF	CAP TANT 0.1UF 10% 50V AXIAL
25	M39003/01-3076	4	1uF	CAP TANT 1.0UF 10% 50V AXIAL
26	M39003/01-2374	2	10uF	CAP TANT 10UF 10% 50V AXIA
27	ST450-50L2KI	2	450uF	CAP TANT 450UF 50V 10% AXIAL
28	ST950-30L2MI	1	950uF	CAP TANT 950UF 30V 10%
29				
30	Diodes			
31	1N-4001	8	Power Diode for rectifier bride	
32	1N914BTR	2	Diode for full wave rectifier	
33				
34	Transistors			
35	2N3904BU	2	General Purpose Amplifier, NPN	
36	TIP31C	1	Power Amplifier, NPN	
37				
38	Misc			
39	LM317	2	Positive Voltage Regulator	
40	LM137	1	Negative Voltage Regulator	
41	G6CK-2114P-US-DC5	1	SR Latch	
42	41-421.038	1	Mom-Off Switch	
43				
44	Transformers			
45	165V10	1	Single Secondary, 115V Primary, 10V Secondary	
46	MPI-200-40	1	Duel Secondary, 115V Primary, 40V Secondary	

Figure 27: Bill of Materials

PARTS:

After having designed the circuit schematic, all of the parts were broken up into multiple sections that are listed above. They are Op-Amps, Resistors, Capacitors, Diodes, Transistors, Transformers, and Miscellaneous. All parts selected were through-hole parts.

Op-Amps:

uA741CP – The uA741 is a general purpose op-amp that can be used for multiple applications. It has a rail to rail voltage of -18/18V which met the -15/15V requirement of the given power supply. The system was designed to have an input signal of $1V_{PP}$ and then have a gain of 10 so the system needed to have a minimum of +/- 10V swing. 15V was arbitrarily set to ensure that the signal never had to deal with saturating on the op amps. When designing a system it is best to always build in tolerance to the system thus +/-15V met that requirement. This op-amp can also be used for all of the configurations needed (LPF, Differential Amplifier, Full Wave Rectifier, Comparator and the Voltage Follower) except for the final comparator which needed to output +5V or 0V for the G6CK-2114-US-DC5 Latching Relay to be able to read the signal of '1' or '0'.

MCP6021-I/P – As mentioned previously, the MCP6021-I/P was selected to be used as the final comparator. The G6CK-2114-US-DC5 Latching Relay can only read a +5 or 0 V signal, as such the uA741CP Op-Amp could not be used here. This system is a rail to ground system that operates off of a ground reference and a 5V rail signal. As the output just needed to output a high (5V) or low (0V) to turn on the $0.7V_{BE(on)}$ NPN TIP31C transistor and be read by the latching relay, this device was selected.

Resistors:

RLR07/RNC60/RN60 Series – All 3 of these resistors are Vishay resistors that are all built to military specifications. These are great resistors to use due to being low noise resistors and having VERY low failure rates which is desirable for a kill switch that would not allow a centrifuge to operate if a part failed. All of the selected resistors were 1/4W which is standard for low power circuits. The system designed is not dissipating significant power so these three resistor series are sufficient. Before final resistor values were chosen simulations were run in OrCad Cadence and a power analysis was looked at on the resistors in the simulation software. The highest power dissipation for a resistor was 8.553mW, well below the 1/4W part ratings.

3005P-1-203 – This 20k potentiometer was selected due to its ease of use. Also due to its physical design it could be built into a machine to have the multiturn portion accessible to the exterior of a metal holding chassis that the centrifuge would be in. This would give the advantage of allowing engineers to calibrate and adjust the total system displacement without taking apart the entire machine to make adjusts of the .5-2 mil tolerances stated above.

Capacitors:

M39003/01 Series – These capacitors are all heavy duty tantalum capacitors. They are designed for 50V which would cover the +/-15V fluctuation range that is supplied from the Astrodyne MTCC-0311. In addition, the 50V rating would give a significant safety margin.

ST Series – These capacitors were selected for having high voltages (50V and 30V respectively) in addition to their high capacitance values for the AC to DC converter. The large values will ensure that the bridge rectifier at the AC to DC converter does not ripple and we have clean power. The system was designed to have 1A of current draw which is well over the circuit requirement. The idea was to keep the ripple down by having large capacitors to meet the requirements for high current draw that will never occur. This series was also one of the few that had high breakdown voltage ratings. The 50V threshold capacitors will be used for the +/-20V fluctuation (40V total) and the 30V was used to cover the 10V transformer while still having 20V tolerance in case there is a surge of more voltage for whatever reason.

Diodes:

1N4001 – This is a power diode and was selected because they are commonly used for rectifier bridges. They are rated for 50V and thus will be sufficient to also handle the 20V total output on the higher range transformer with over a 100% safety margin. These diodes can also handle 1A of average current (which the power supply system was designed for) as well as has a 30A rating for the surge current so there is no worry that the diodes would blow up when the system initially powered up.

1N914BTR – This is just a generic diode that can be used for the full wave rectifier. A Schottky diode could also be used to get better performance near the zero crossings due to a low forward voltage drop and a fast switching action compared to a silicon diode.

Transistors:

2N3904BU – This is just a generic NPN transistor. Its only purpose was to be able to turn on when 5V is present and remain off when 0V is applied. They will not see much current and as such they are not power transistors (in which case the TIP31C would be used because it can easily handle 1.5A which would meet the other system requirements).

Tip31C – Another genereric NPN transistor. Its purpose is used to act as a power transistor to handle more current (1.5A). To ensure there components do not burn up during operation.

Miscellaneous Parts:

LM137 – This is a negative Voltage Regulator. They allow for engineers to easily select any output voltage between -1.2 to -37V by using different resistor values to set the gain. It would be used to create the -15V rail power output if a non COTS power supply solution were required. Because it sees -20V it is able to produce the desired -15V output easily. It also has can output 1.5A which meets the 1A current requirement from the other parts selected. Its sister unit the LM317 covers the positive voltage. It was also noted that it had 77dB Ripple Rejection.

LM317 – This is the positive voltage regulator stated above. It has an output range of 1.25V to 37V. So this voltage regulator could be used for both the +15V and +5V outputs needed to power the circuit if a non COTS power supply solution were required. It also provided the 1.5A to cover the 1A of the system. It was also noted that it had 80dB Ripple Rejection.

G6CK-2114P-US-DC5 – This is a SR Latching Relay. The latching relay was chosen because it maintains it's state after actuation, is asynchronous and the outputs can change as soon as the inputs do. Its digital logic is simulated by seeing 5V or 0V (high/low). This component was used due to access to a 5V DC power and ground. It also would turn the power off and keep it off when the latching state changed as it has 2 channels. So 1 is always on and the other is always off. It can also handle $250V_{AC}$ and $125V_{DC}$ so it can easily handle 24 V_{DC} of the centrifuge that this system is being designed to regulate.

41-421.038 – A generic switch that can handle 5V to switch the Latching Relay states manually. It allows the centrifuge operator the capability to reset the centrifuge when power has been killed to the system. It is a momentary off switch so that it is only temporarily on when pressed and the operator cannot leave it on forever thus always applying a 5V (high) signal. This is more to protect from user error. It is a button so that it can easily fit on the physical structure of the centrifuge and easily be pressed to reset the centrifuge.

Transformers:

165V10 – This transformer is a single primary to single secondary transformer. It has a laminated core to reduce the eddy currents and keep them to a minimum from interfering with the efficient transfer of energy from the primary coil to the secondary one. It also has a dual bobbin design so that no electrostatic shield is required. Its input is $115V_{AC}$ at 60Hz and gives $2000V_{rms}$ voltage isolation. It also has wire leads for easy use with other parts.

MPI-200-40 – This is a dual primary to dual secondary transformer. It can be used as a single primary to dual secondary transformer though which is how it has been designed for following the design above in the Power Supply Design section. It provides 40V at the secondary which meet the +20/-20V needed for the design I was created from a single $115V_{AC}$ input. It also has a laminated core which is desirable (see 165V10). It has an electrostatic shield – solid copper full width foil, this grounded shield equalizes the electrical stress around the conductor and diverts any leakage current to ground. This shield acts as a Faraday cage to reduce electrical noise from affecting the signals, and to reduce electromagnetic radiation. This shield also minimizes capacitively coupled noise. As such this system gives $4000V_{rms}$ voltage isolation with less than 100uA of leakage current.

NOTE: $115V_{AC}$ comes from the design side, equipment is normally designed to run on 115V +/- 10%. $120V_{AC}$ comes from the supply side, under standard conditions electrical utilities deliver electricity at 120V +/- 5%. So $115V_{AC}$ will work for this application.

Chapter 6: Simulation Results

Balanced (B)	Probe Monitor Signal (S)	Run
0	0	0
0	1	0
1	0	0
1	1	1

Table 2: AND Gate System Logic

To understand the table the signal meanings have been laid out below.

- S (1) = $1V_{DC}$ Offset Present
- S (0) = $0V_{DC}$ Present (Offset not present)
- B (1) = AC signal is below threshold
- B (0) = AC signal is above threshold

Reference Figure 23, the Full Design Concept, to follow the waveform progression in the following figures. All waveforms were generated with Cadence PSpice. The full circuit can be seen below in Figure 28, with zoomed in portions below in Figures 29-32 correlating to labels A-D.

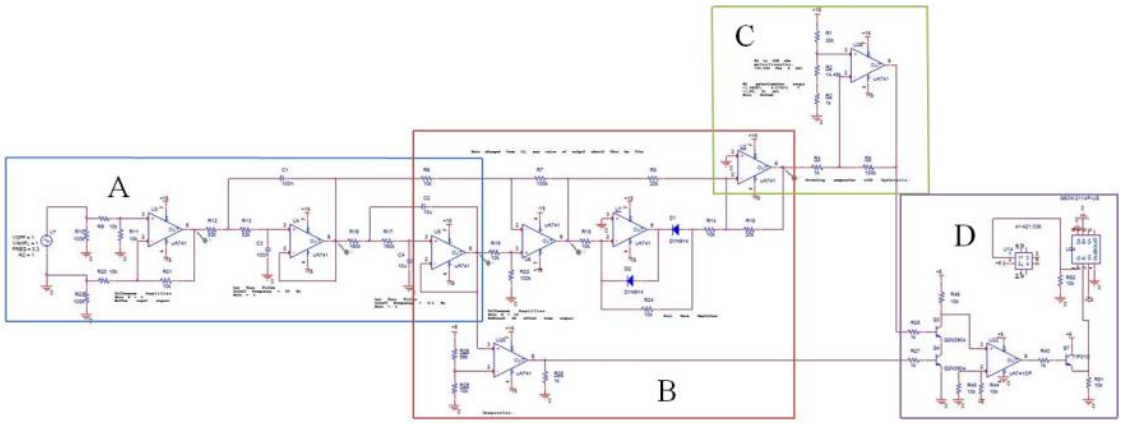


Figure 28: Final Circuit

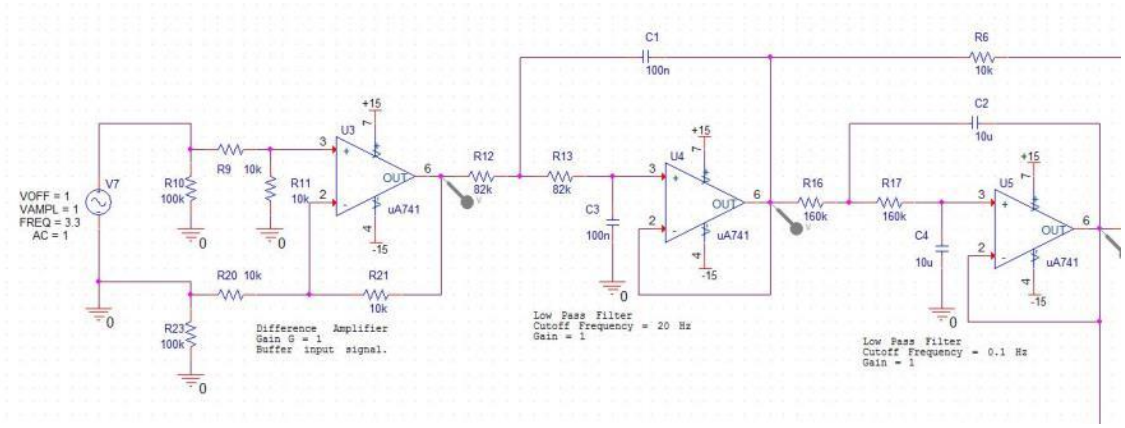


Figure 29: Label A of Figure 28.

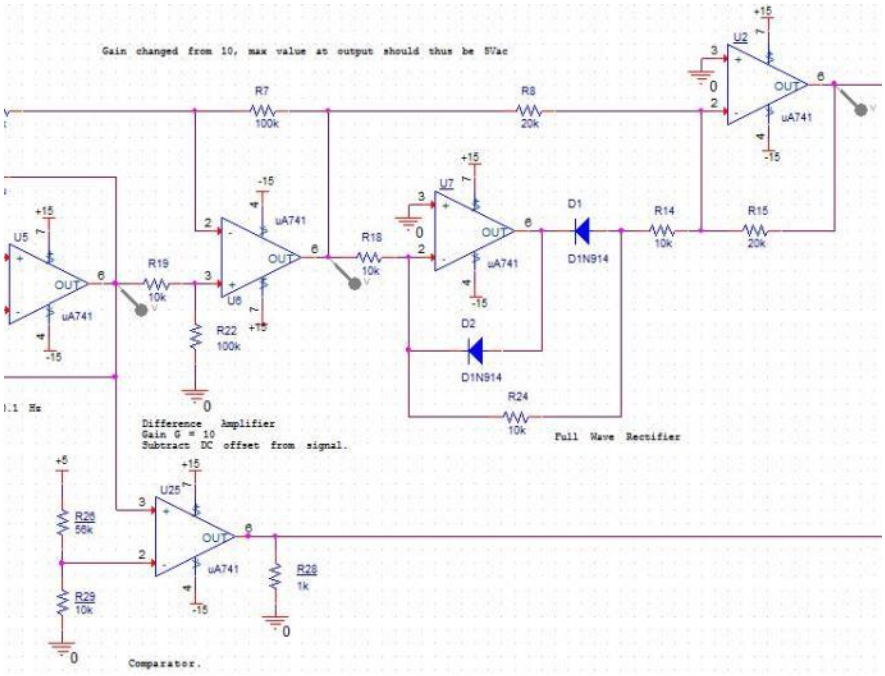


Figure 30: Label B of Figure 28.

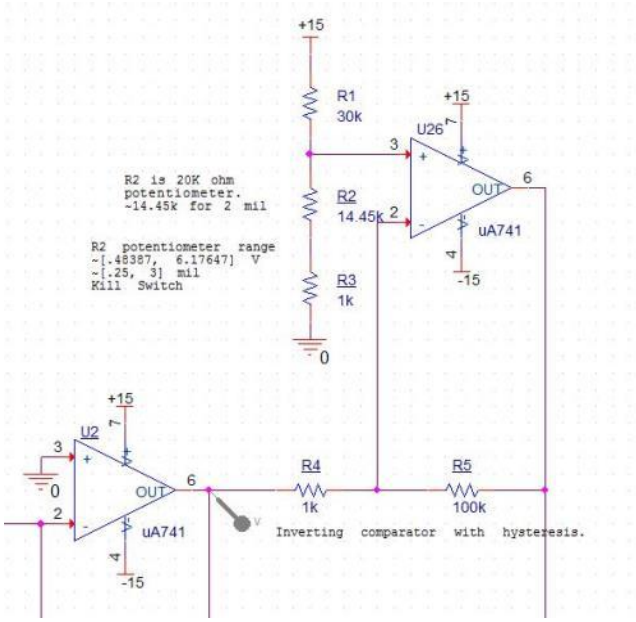


Figure 31: Label C of Figure 28.

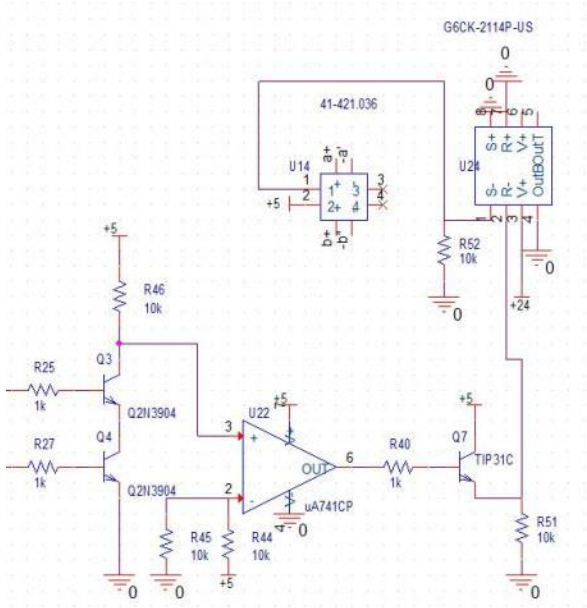


Figure 32: Label D of Figure 28.

SETTING #1

Balanced (B)	Probe Monitor Signal (S)	Run
1	1	1

Table 3: Setting #1 signal input configuration.

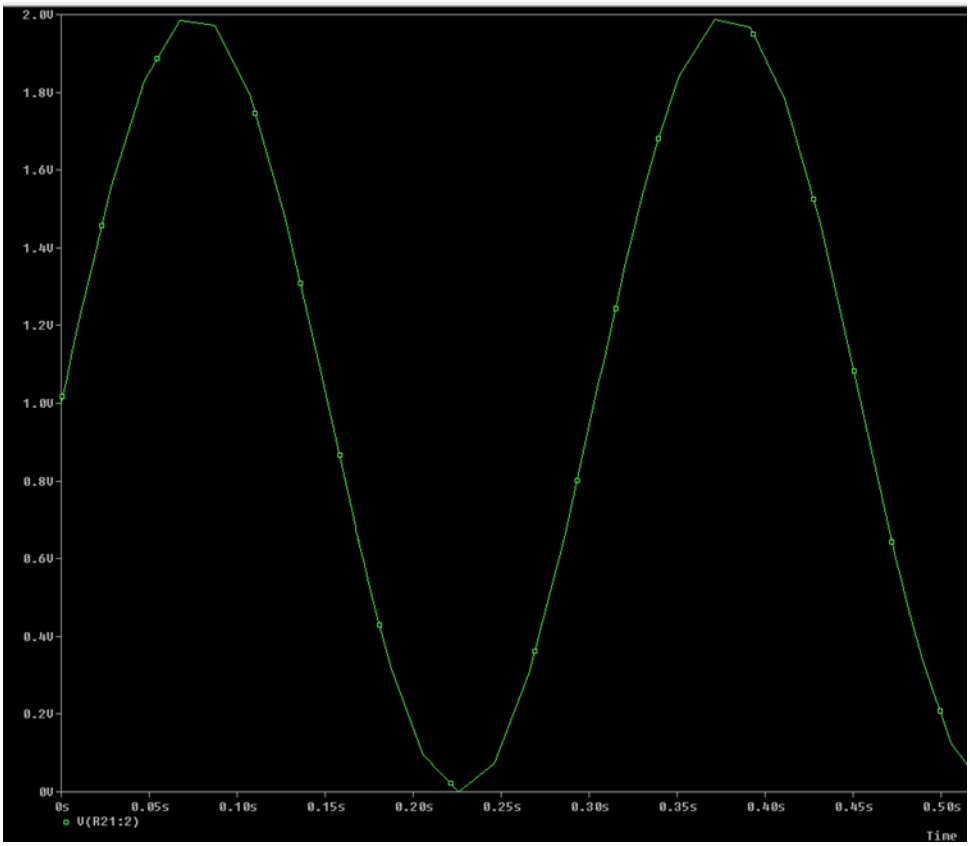


Figure 33: Differential Amplifier (Gain 1) output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (0:2 V).

The $1V_{DC}$ offset voltage is present (Probe Monitor Signal is '1') and the system is within balance as the peak-to-peak voltage is under 2 volts (Balanced is '1'). This is shown in Figure 33.

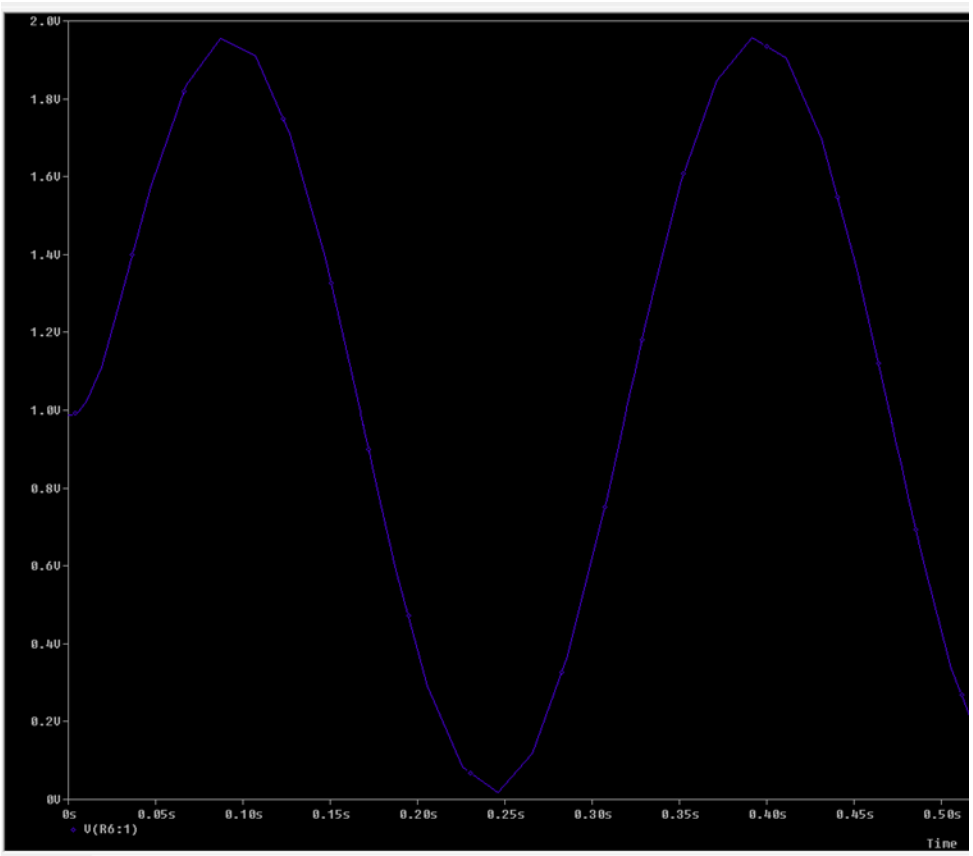


Figure 34: Low Pass Filter with cutoff frequency 20 Hz output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (0:2 V).

The test was performed with a 300 RPM assumption and thus 5 Hz max signal. This means that the $.1f_C$ will have very minimal effects from the 3dB cutoff frequency point. As such the signal is practically unaltered at the output.

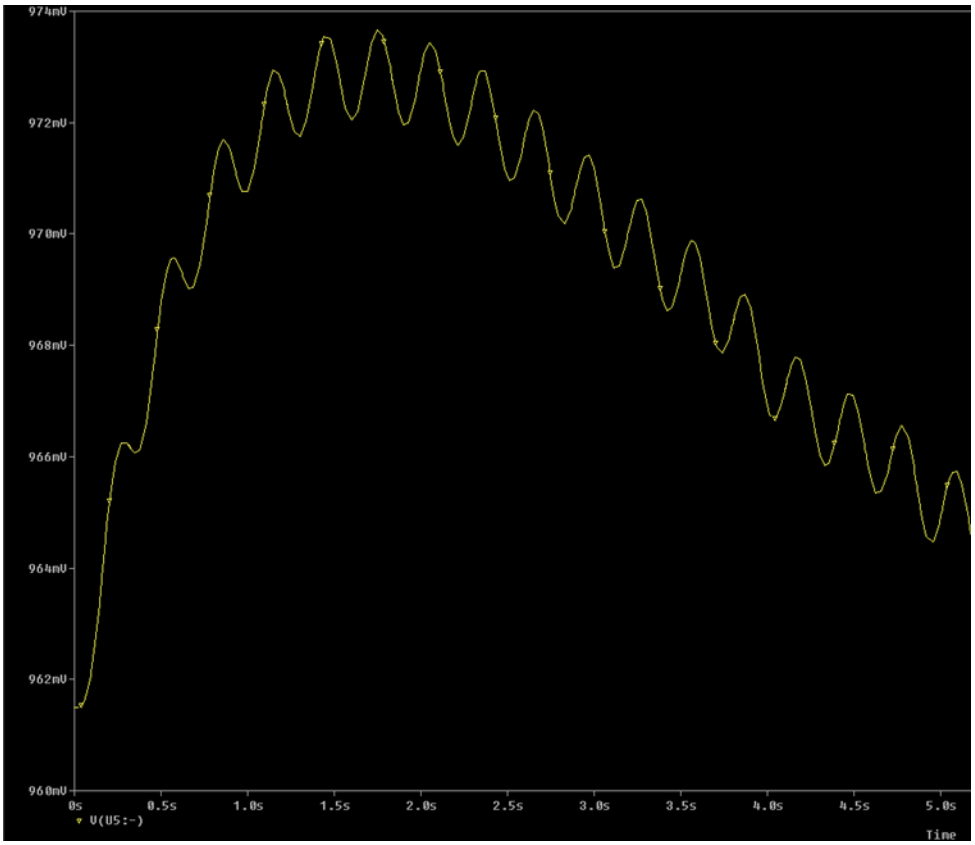


Figure 35: Low Pass Filter with cutoff frequency 0.1 Hz output waveform. Axes: X – time (0:5 sec); Y – output voltage (960:974 mV).

The AC signal is removed and only a DC signal remains. Figure 35 only shows approximately 12 mV fluctuation after passing through the 0.1 Hz low pass filter. Initially, there is overshoot as voltage is applied. After the initial five seconds the voltage stabilizes to approximately 964 mV. The 964 mV is approximately a steady DC voltage

which satisfies the ‘1’ condition for the Probe Monitor Signal (S).

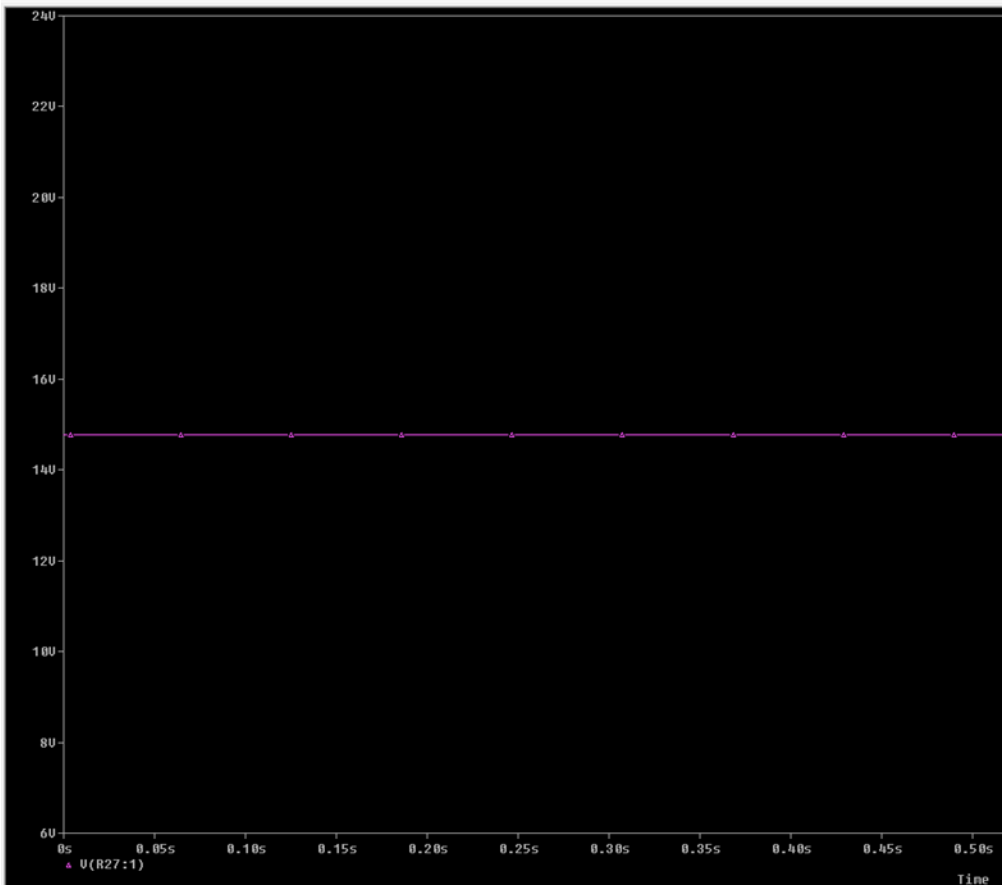


Figure 36: Comparator verifying offset voltage is present output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (6:24 V).

The comparator effectively detects the presence of the input offset voltage and outputs a ‘1’ or $+V_{rail}$ which in this simulation profile is +15V.

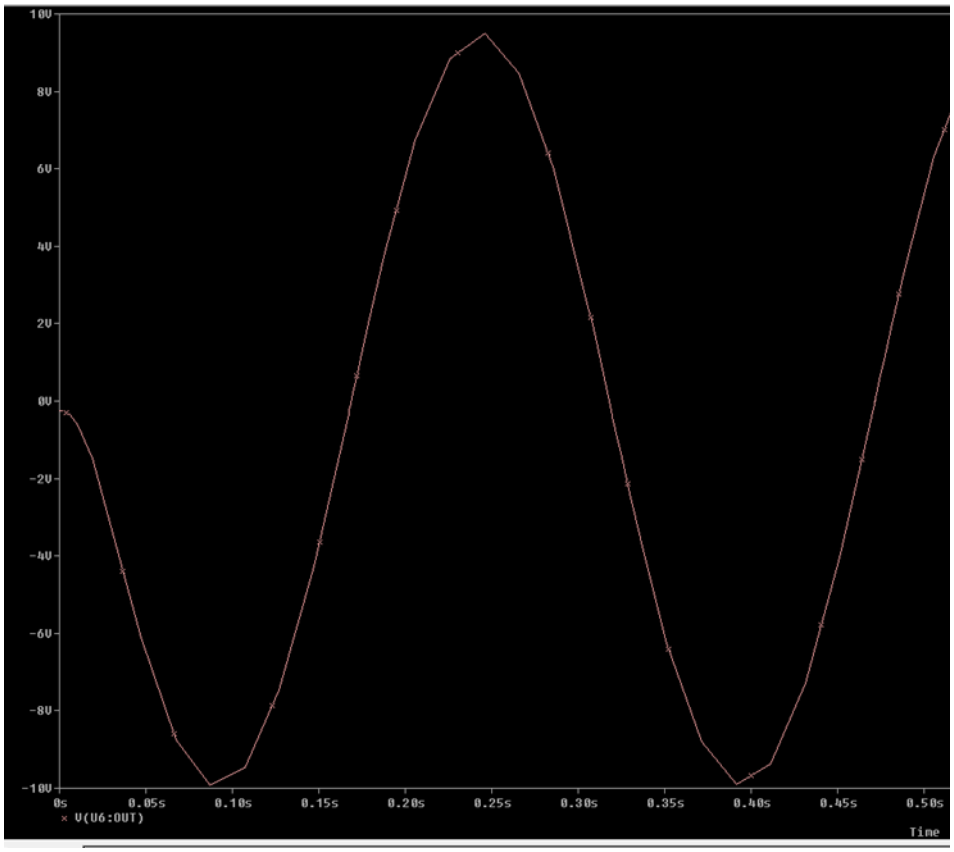


Figure 37: Difference Amplifier (G = 10) output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-10:10 V).

The system amplifies the approximate $1V_{PP}$ signal by a gain of 10 to now have an approximate 10 V_{PP} signal at the output of the difference amplifier. The difference amplifier also used the output voltages from the 20 Hz and 0.1 Hz LPF to cancel out the DC voltages present at each stage output. Checking the simulation data we can notice there is just minor negligible offset voltage still remaining (mV in a 10 V_{PP} signal).

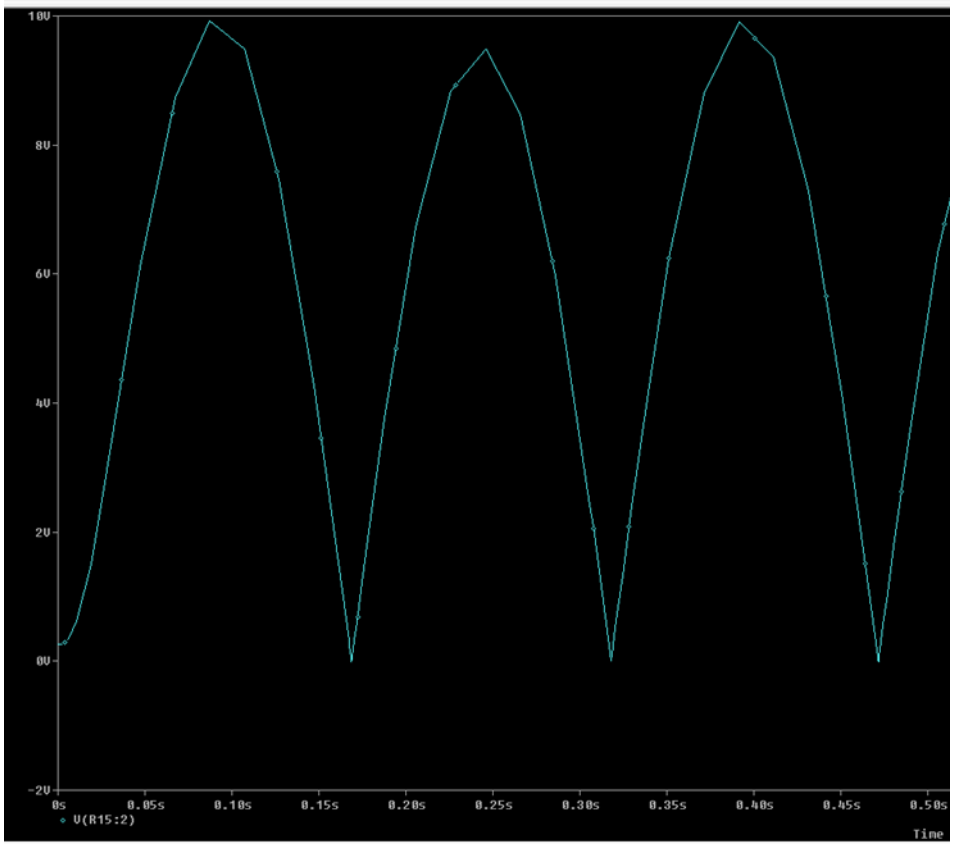


Figure 38: Full Wave Rectifier output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-2:10 V).

The Full wave rectifier prepares the signal to be compared against the comparator that is just comparing $+V_P$ against a set DC voltage from a potentiometer. The voltage is still below 10 V_P (the threshold that was set to test the system for 2 mil offset) and as such should still work.

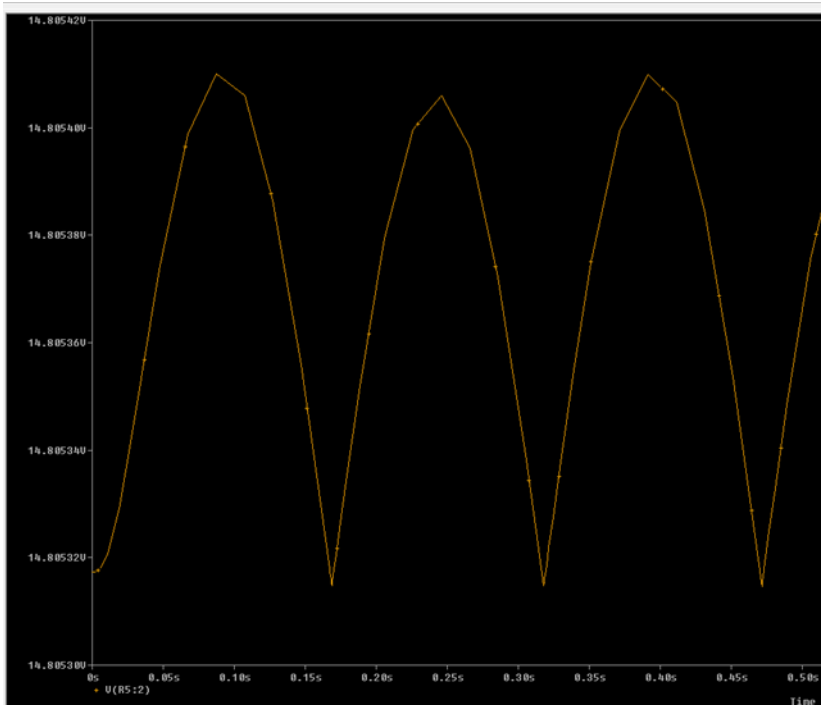


Figure 39: Inverting Comparator w/ hysteresis. Axes: X – time (0:0.5 sec); Y – output voltage (14.80530:14.80542 V).

The signal is balanced so the comparator outputs a '1' or approximately 15V. The output fluctuates between 32-41 μV which is negligible in this case. The full wave rectifier can be seen due to the hysteresis in the system which was added for quicker response time in turning off the centrifuge if the user set threshold is exceeded. Because the comparator output is a '1' the centrifuge can continue to run.

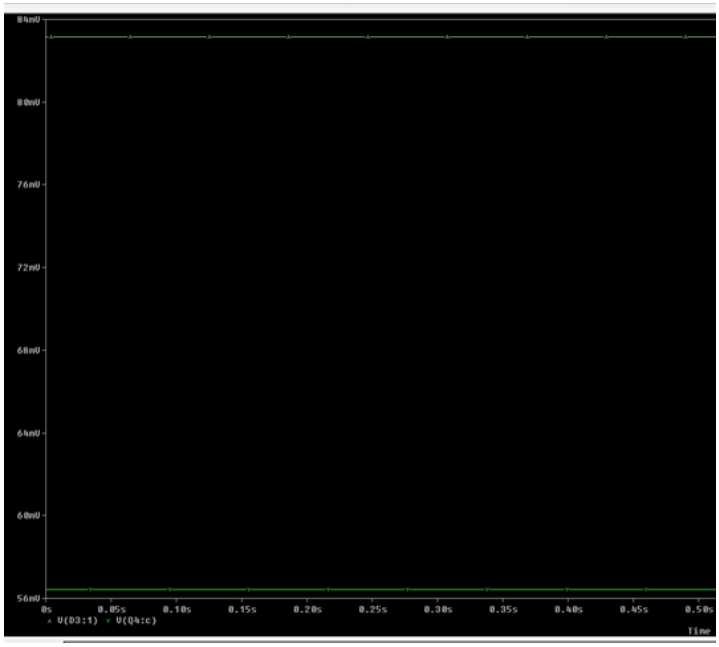


Figure 40: AND gate output waveforms. Axes: X – time (0:0.5 sec); Y – output voltage (56:84 mV).

The system runs as both transistors are on (outputting 1's). Transistor #1 is the top (B) transistor and correlates to Q3 in the schematic and Transistor #2 is the bottom (S) transistor and correlates to Q4 in the schematic. With both present the SR Latch will always see a '0'. The value will never change to a '1' so the centrifuge will always run with this condition.

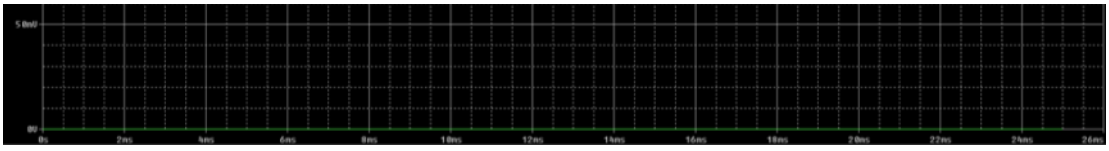


Figure 41: Final Comparator. Axes: X – time (0:26 ms); Y – output voltage (0:60 mV).

With both transistors outputting a '1' the SR Latch will always see a '0'. The value will never change to a '1' so the centrifuge will always run with this condition.

SETTING #2

Balanced (B)	Probe Monitor Signal (S)	Run
0	0	0

Table 4: Setting #2 signal input configuration.

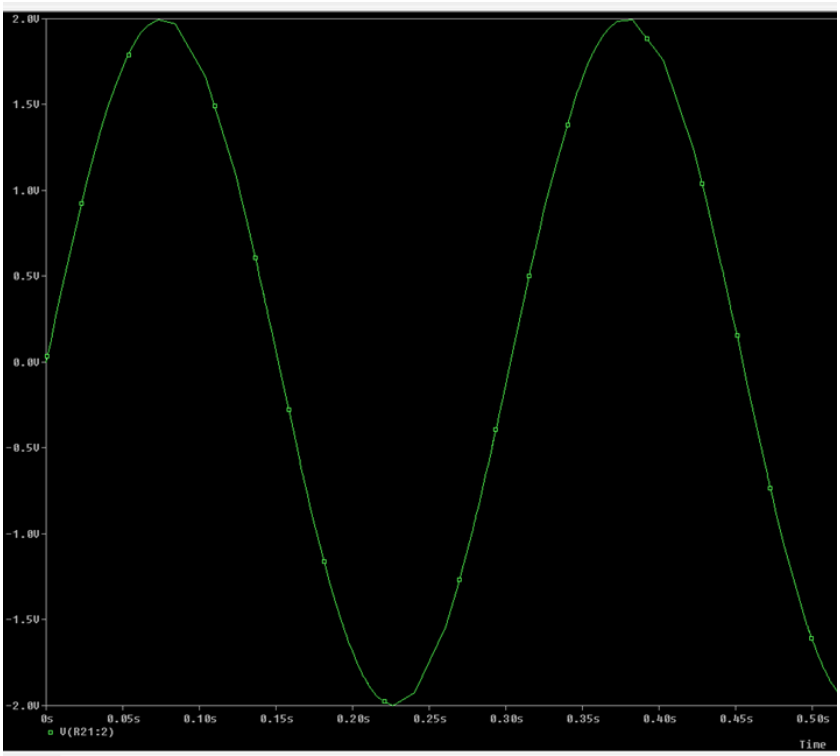


Figure 42: Differential Amplifier (Gain 1) output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (0:2 V).

The $1V_{DC}$ offset voltage is not present (Probe Monitor Signal is '0') and the system is out of balance as the peak-to-peak voltage is over 2 volts (Balanced is '0'). This is shown in Figure 42. As such the system should not work.

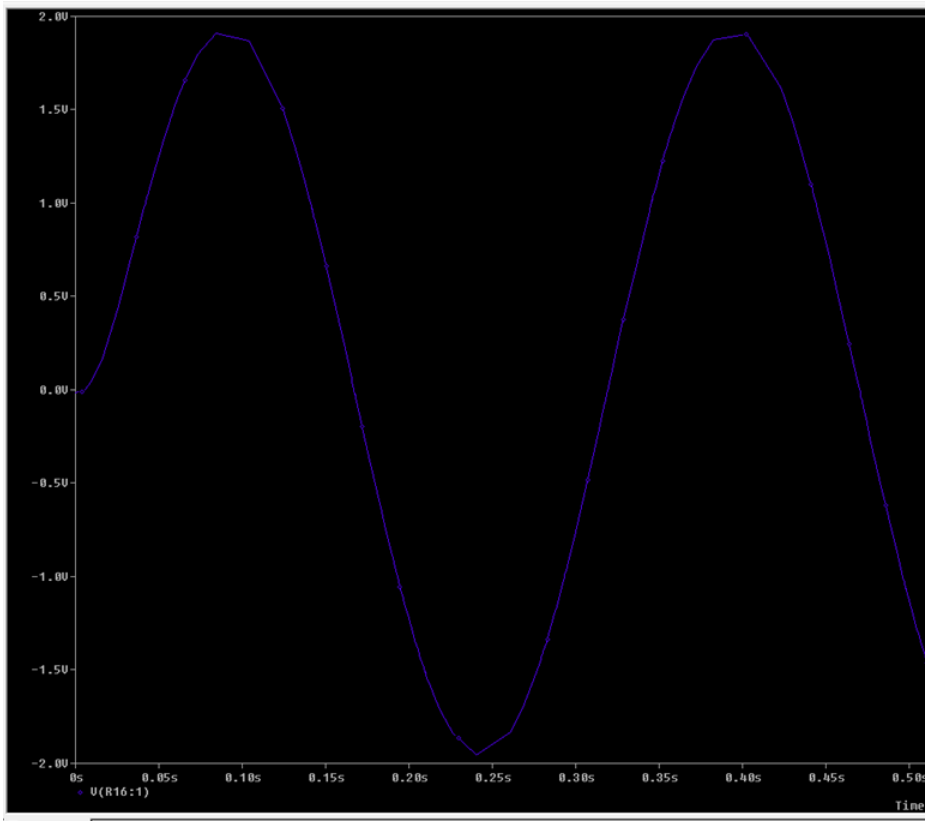


Figure 43: Low Pass Filter with cutoff frequency 20 Hz output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-2:2 V).

The test was performed with a 300 RPM assumption and thus 5 Hz max signal. This means that the $.1f_C$ will have very minimal effects from the 3dB cutoff frequency point. As such the signal is practically unaltered at the output from the input signal.

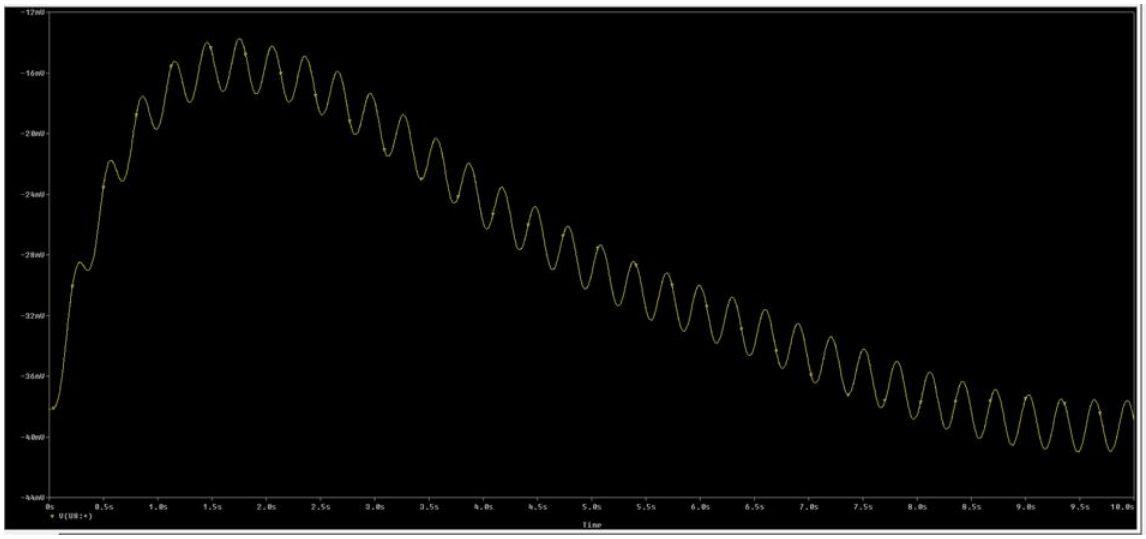


Figure 44: Low Pass Filter with cutoff frequency 0.1 Hz output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-44:-12 mV).

The AC signal is removed and there is no offset voltage present. Figure 44 only shows approximately 24 mV fluctuation after passing through the 0.1 Hz low pass filter. Initially, there is overshoot as voltage is applied. After the initial five seconds the voltage stabilizes to approximately -40 mV. The -40 mV is approximately a steady DC voltage which satisfies the '0' condition for the Probe Monitor Signal (S).

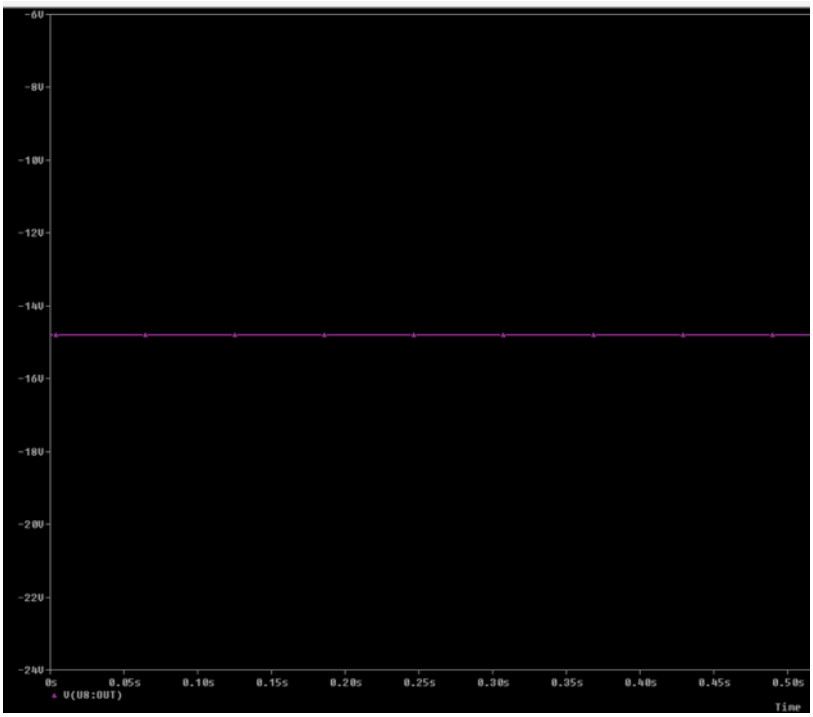


Figure 45: Comparator verifying offset voltage is present output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-24:-6 V).

The comparator detects no input offset voltage and outputs a '0' or $-V_{rail}$ which in this simulation profile is -15V. This should prevent the system from working.

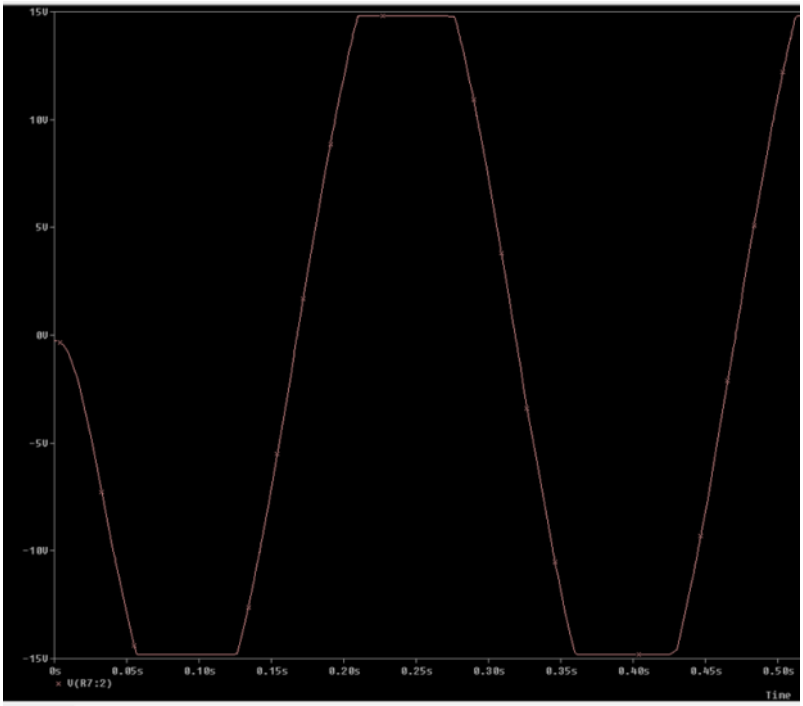


Figure 46: Difference Amplifier (G = 10) output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-15:15 V).

The system amplifies the approximate $2V_{PP}$ signal by a gain of 10 to now have an approximate 15 V_{PP} signal at the output of the difference amplifier. However, the 15 V_{PP} signal is clipping and losing 10 volts worth or signal. There was no DC voltage for the Difference Amplifier to cancel out. Checking the simulation data we can notice there is just minor negligible offset voltage still remaining (mV in a 15 V_{PP} signal).

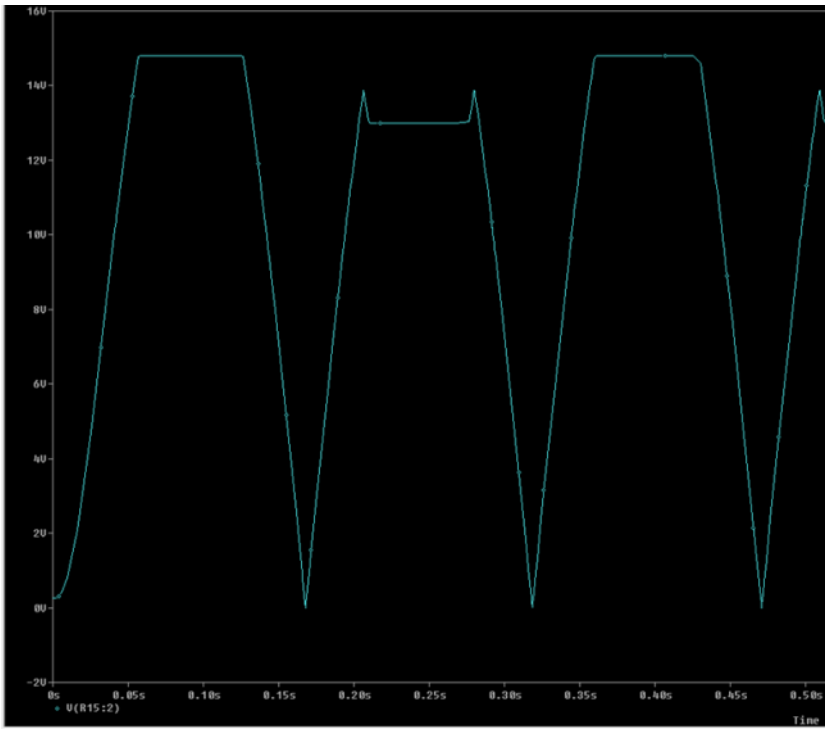


Figure 47: Full Wave Rectifier output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-2:16 V).

The Full wave rectifier prepares the signal to be compared against the comparator that is just comparing $+V_P$ against a set DC voltage from a potentiometer. The voltage is still above 10 V_P (the threshold that was set to test the system for 2 mil offset) and is still clipping. As such should not work.

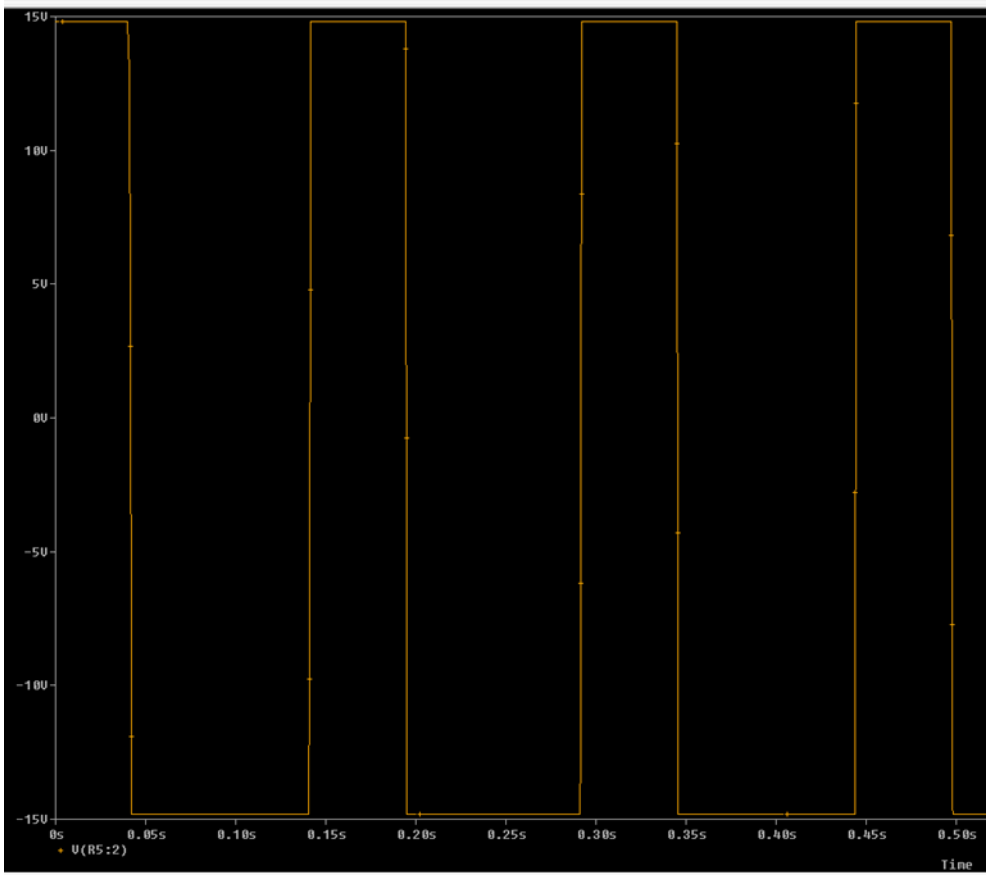


Figure 48: Inverting Comparator w/ hysteresis. Axes: X – time (0:0.5 sec); Y – output voltage (-15:15 V).

The signal is balanced when the AC signal is below 10 V_P but when the signal goes higher than that and eventually saturated the signal is unbalanced. This means that the comparator will fluctuate between a '1' and '0' as the signal fluctuates. This will have the output fluctuate an output voltage of +15 and -15V. As a transistor requires 0.7V to turn on the -15V will not affect the system. The latching relay can only be reset with a manual reset so one '0' will permanently deactivate the system thus the fluctuation does not matter.

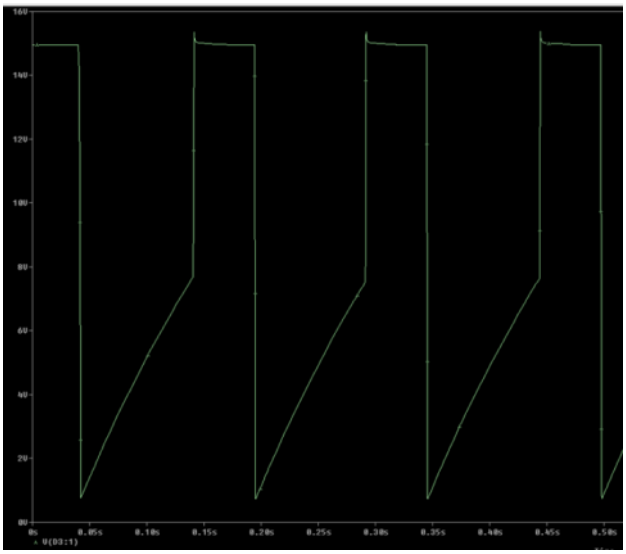


Figure 49: AND gate output waveforms for (B). Axes: X – time (0:0.5 sec); Y – output voltage (0:16 V).

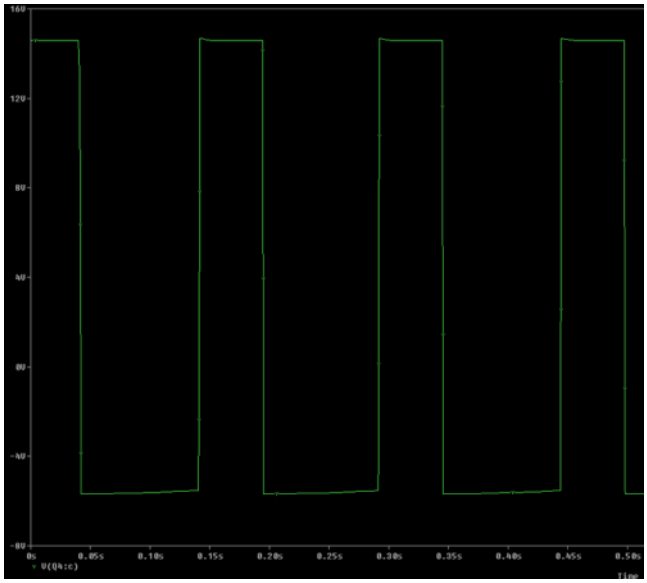


Figure 50: AND gate output waveforms for (S). Axes: X – time (0:0.5 sec); Y – output voltage (-8:16 V).

The system stops running the first time the output voltage reads a +15V. This will cause the final stage transistor to output a '1' which will turn off the SR Latch instead of the SR Latch seeing the normal '0' that allows the centrifuge to normally run.

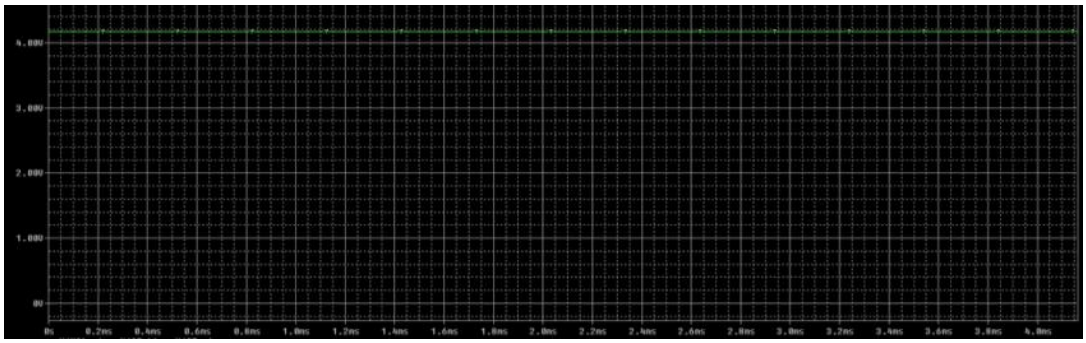


Figure 51: Final Comparator. Axes: X – time (0:4 ms); Y – output voltage (-0.2:4.8 V).

With no offset the SR Latch will always see a '1'. The value will never change to a '0' to allow the centrifuge to run.

SETTING #3

Balanced (B)	Probe Monitor Signal (S)	Run
0	1	0

Table 5: Setting #3 signal input configuration.

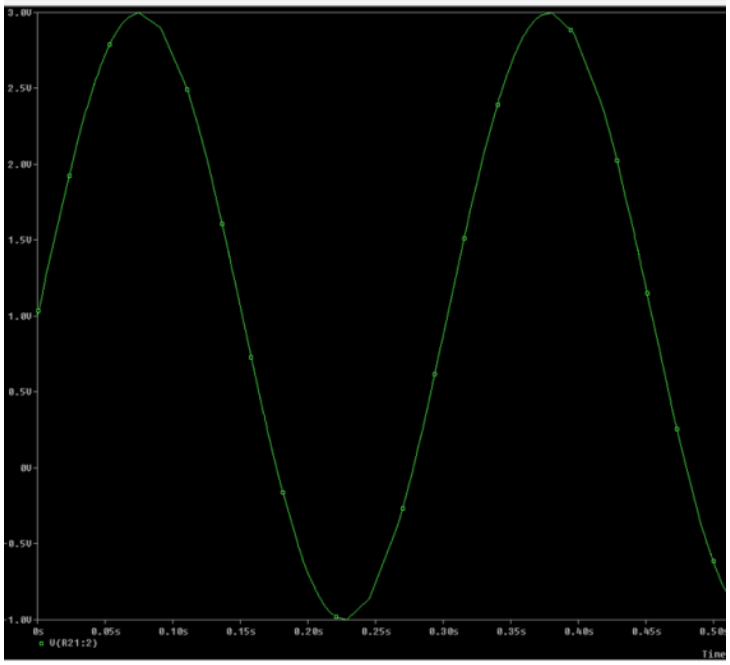


Figure 52: Differential Amplifier (Gain 1) output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (1:3 V).

The $1V_{DC}$ offset voltage is present (Probe Monitor Signal is '1') and the system is out of balance as the peak-to-peak voltage is over 2 volts (Balanced is '0'). This is shown in Figure 52. As such the system should not work.

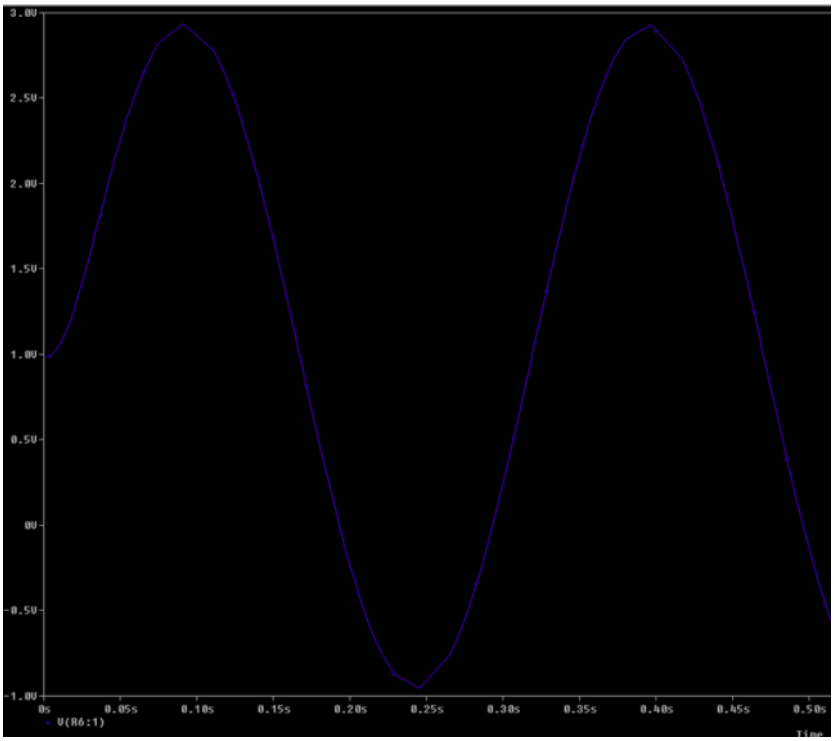


Figure 53: Low Pass Filter with cutoff frequency 20 Hz output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-1:3 V).

The test was performed with a 300 RPM assumption and thus 5 Hz max signal. This means that the $.1f_C$ will have very minimal effects from the 3dB cutoff frequency point. As such the signal is practically unaltered at the output from the input signal.

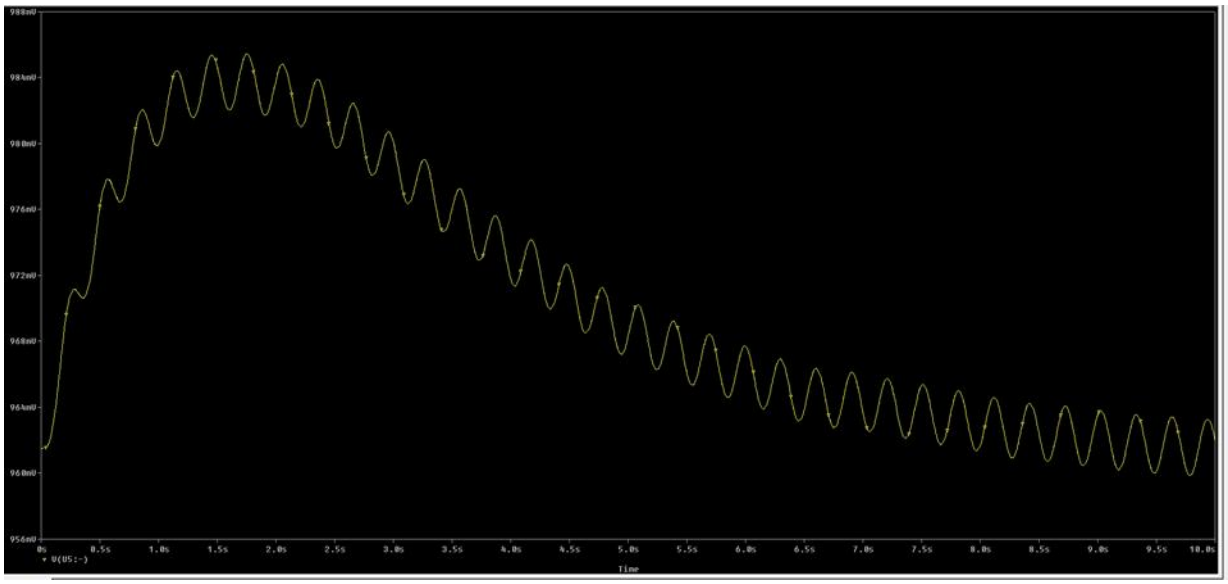


Figure 54: Low Pass Filter with cutoff frequency 0.1 Hz output waveform. Axes: X – time (0:10 sec); Y – output voltage (956:988 mV).

The AC signal is removed and only a DC signal remains. Figure 54 only shows approximately 14 mV fluctuation after passing through the 0.1 Hz low pass filter. Initially, there is overshoot as voltage is applied. After the initial five seconds the voltage stabilizes to approximately 962 mV. The 962 mV is approximately a steady DC voltage which satisfies the '1' condition for the Probe Monitor Signal (S).

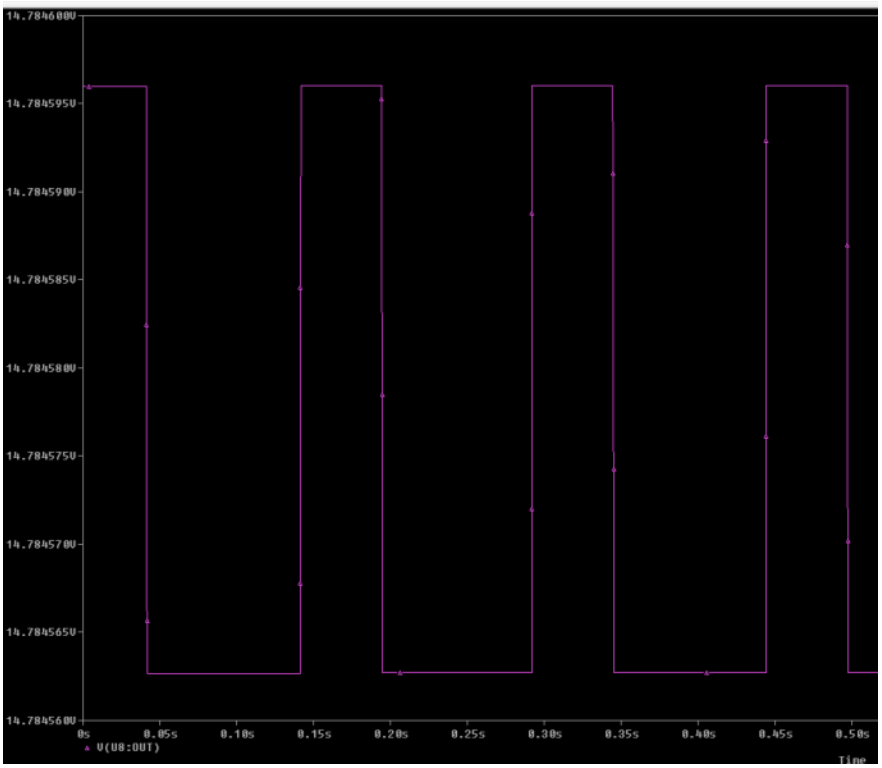


Figure 55: Comparator verifying offset voltage is present output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (14.784560:14.784680 V).

The comparator effectively detects the presence of the input offset voltage and outputs a '1' or $+V_{rail}$ which in this simulation profile is approximately +15V. There is less than 40μV fluctuation in the output voltage which is negligible.

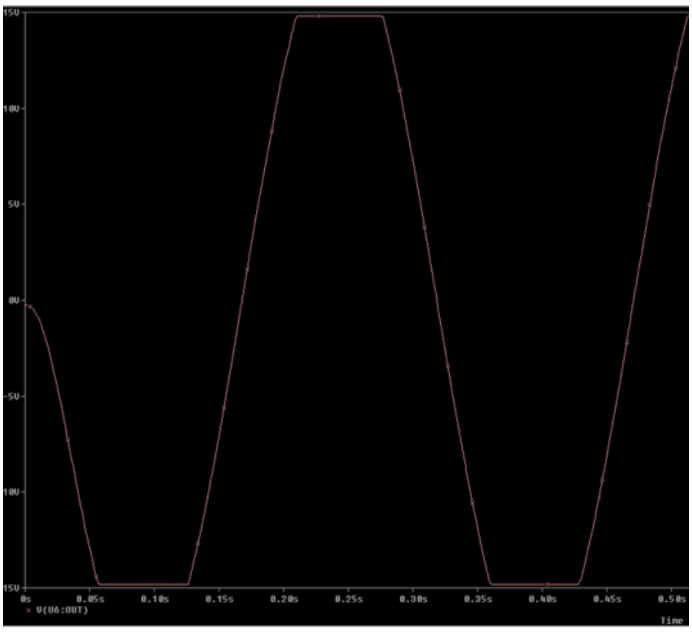


Figure 56: Difference Amplifier (G = 10) output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-15:15 V).

The system amplifies the approximate $2V_{PP}$ signal by a gain of 10 to now have an approximate 15 V_{PP} signal at the output of the difference amplifier. However, the 15 V_{PP} signal is clipping and losing 10 volts worth or signal. There was no DC voltage for the Difference Amplifier to cancel out. Checking the simulation data we can notice there is just minor negligible offset voltage still remaining (mV in a 15 V_{PP} signal).

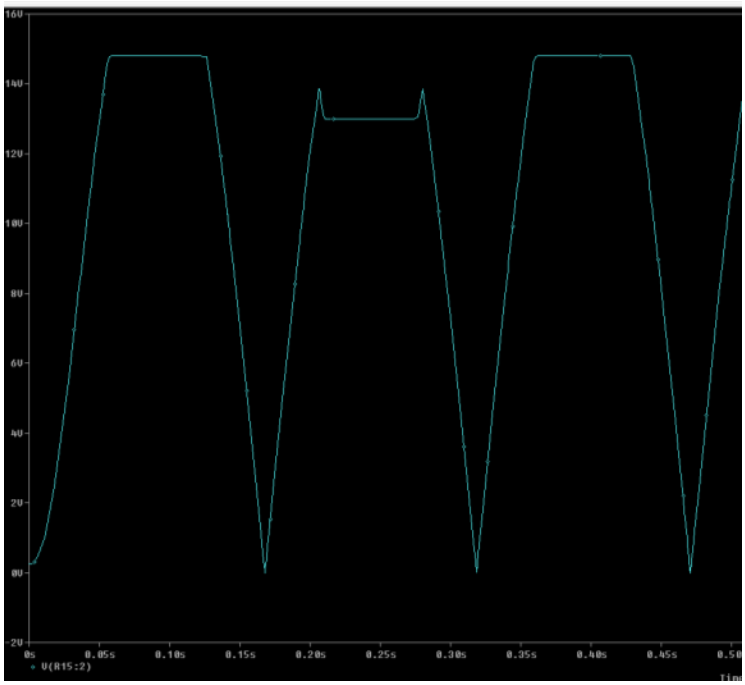


Figure 57: Full Wave Rectifier output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-2:16 V).

The Full wave rectifier prepares the signal to be compared against the comparator that is just comparing $+V_P$ against a set DC voltage from a potentiometer. The voltage is still above 10 V_P (the threshold that was set to test the system for 2 mil offset) and is still clipping. As such should not work.

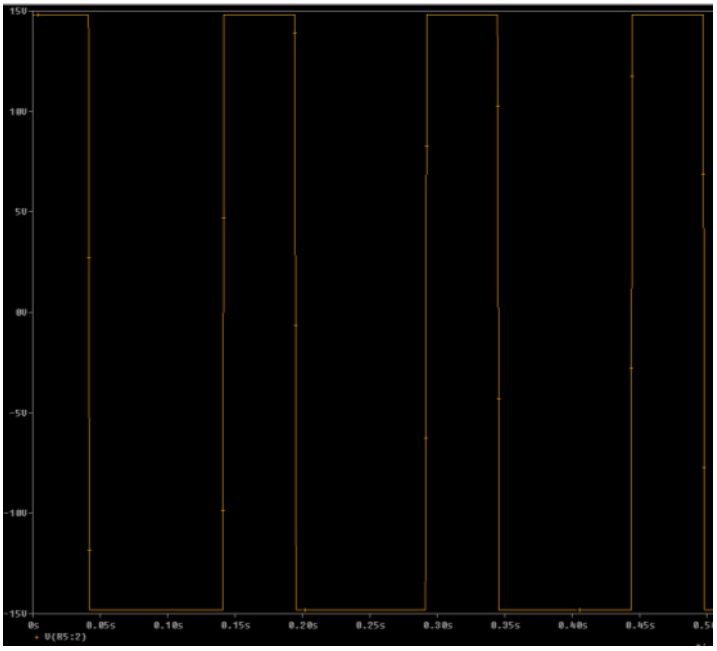


Figure 58: Inverting Comparator w/ hysteresis. Axes: X – time (0:0.5 sec); Y – output voltage (-15:15 V).

The signal is balanced when the AC signal is below 10 V_P but when the signal goes higher than that and eventually saturated the signal is unbalanced. This means that the comparator will fluctuate between a '1' and '0' as the signal fluctuates. This will have the output fluctuate an output voltage of +15 and -15V. As a transistor requires 0.7V to turn on the -15V will not affect the system. The latching relay can only be reset with a manual reset so one '0' will permanently deactivate the system thus the fluctuation does not matter.

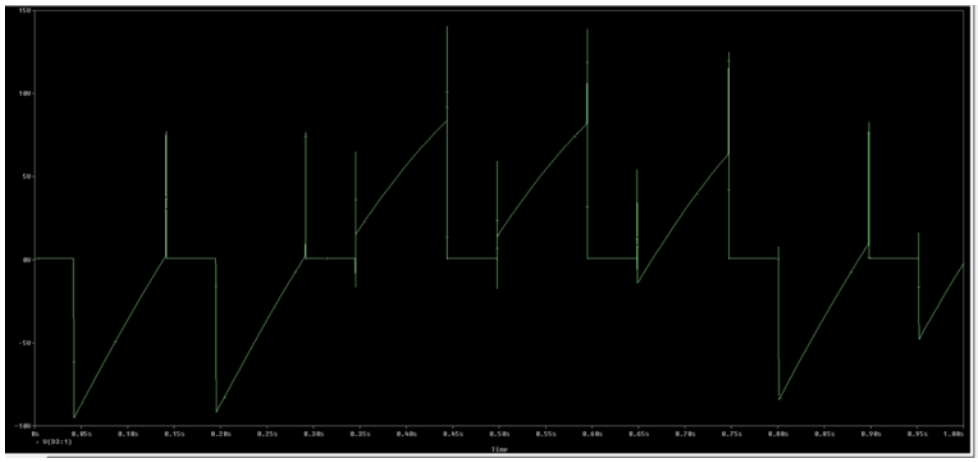


Figure 59: AND gate output waveforms for (B). Axes: X – time (0:1 sec); Y – output voltage (-10:15 V).

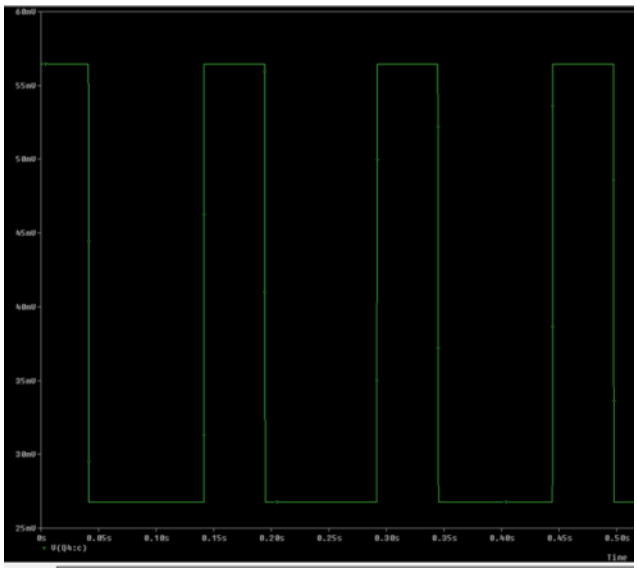


Figure 60: AND gate output waveforms for (S). Axes: X – time (0:0.5 sec); Y – output voltage (25:60 mV).

The system stops running the first time the output voltage reads a +15V. This will cause the final stage transistor to output a ‘1’ which will turn off the SR Latch instead of the SR Latch seeing the normal ‘0’ that allows the centrifuge to normally run.

The probe monitor signal (S) is reading a one and thus outputting the approximate 0 V that is desired but the balanced (B) fluctuates to +15V which causes the system to stop.

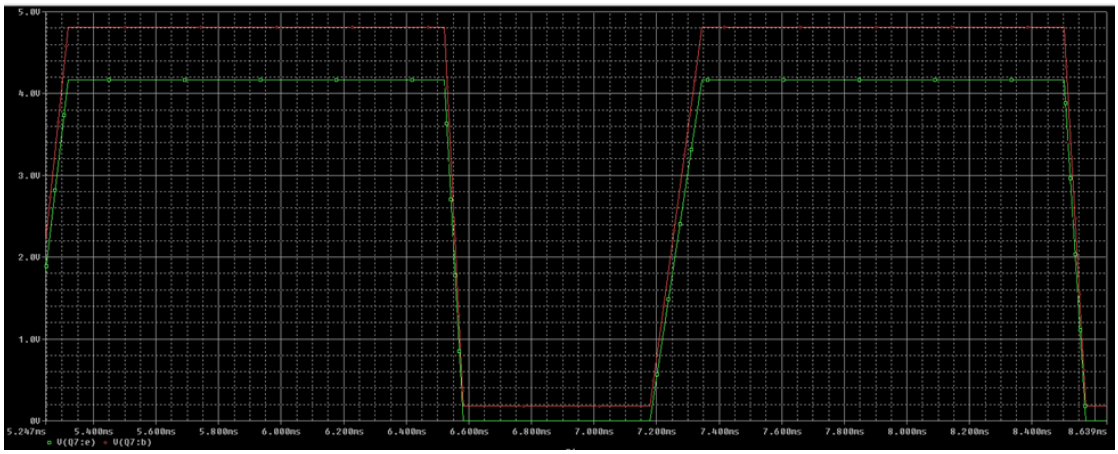


Figure 61: Final Comparator. Axes: X – time (5.24:8.63 ms); Y – output voltage (0:5 V).

The red signal is the output after the final comparator; the green signal is the voltage drop on the transistor. The green signal is fed into the SR Latch to change the logic. As the system voltages exceed the balance condition and the AC signal exceeds the threshold the system will kill power and the centrifuge will not run even though some of the signal appears within balance. The SR Latch will have to be manually reset until the centrifuge can run again.

SETTING #4

Balanced (B)	Probe Monitor Signal (S)	Run
1	0	0

Table 6: Setting #4 signal input configuration.

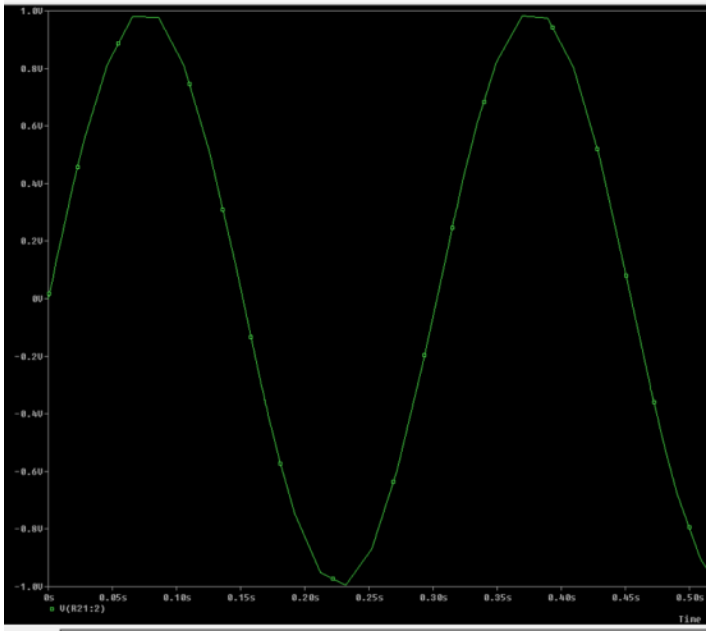


Figure 62: Differential Amplifier (Gain 1) output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-1:1 V).

The $1V_{DC}$ offset voltage is not present (Probe Monitor Signal is '0') and the system is within balance as the peak-to-peak voltage is under 2 volts (Balanced is '1'). This is shown in Figure 58. As such the system should not work.

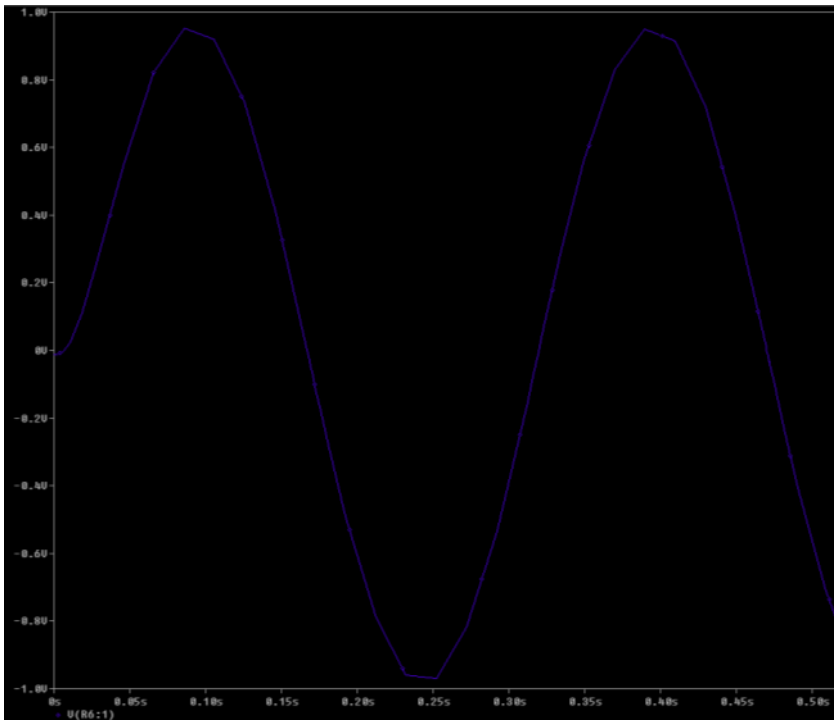


Figure 63: Low Pass Filter with cutoff frequency 20 Hz output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-1:1 V).

The test was performed with a 300 RPM assumption and thus 5 Hz max signal. This means that the $.1f_C$ will have very minimal effects from the 3dB cutoff frequency point. As such the signal is practically unaltered at the output from the input signal.

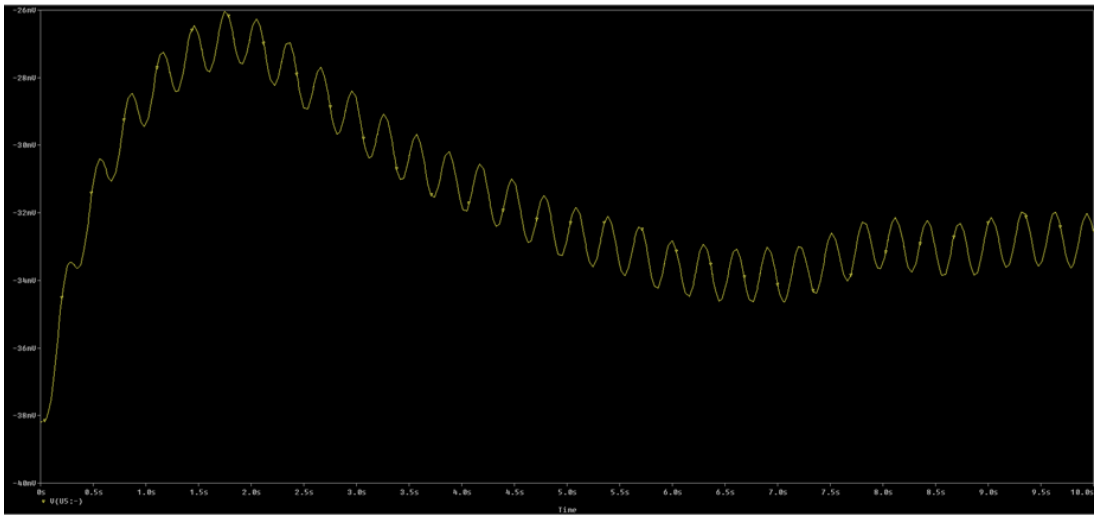


Figure 64: Low Pass Filter with cutoff frequency 0.1 Hz output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-40:-26 mV).

The AC signal is removed and there is no offset voltage present. Figure 64 only shows approximately 12 mV fluctuation after passing through the 0.1 Hz low pass filter. Initially, there is overshoot as voltage is applied. After the initial five seconds the voltage stabilizes to approximately -34 mV. The -34 mV is approximately a steady DC voltage which satisfies the '0' condition for the Probe Monitor Signal (S).

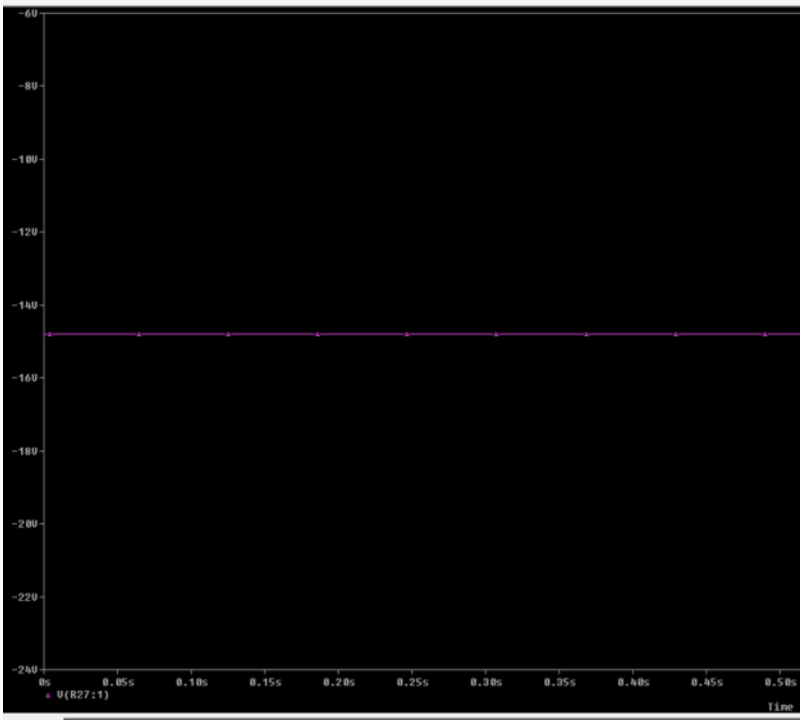


Figure 65: Comparator verifying offset voltage is present output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-24:-6 V).

The comparator detects no input offset voltage and outputs a '0' or $-V_{rail}$ which in this simulation profile is -15V. This should prevent the system from working.

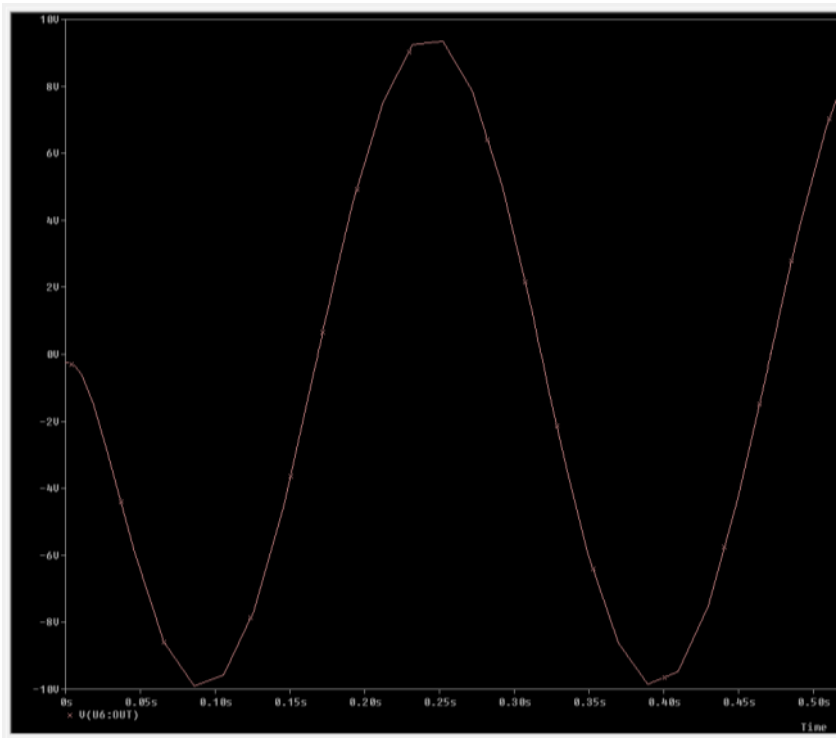


Figure 66: Difference Amplifier (G = 10) output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-10:10 V).

The system amplifies the approximate $1V_{PP}$ signal by a gain of 10 to now have an approximate 10 V_{PP} signal at the output of the difference amplifier. The difference amplifier also used the output voltages from the 20 Hz and 0.1 Hz LPF to cancel out the DC voltages present at each stage output. Checking the simulation data we can notice there is just minor negligible offset voltage still remaining (mV in a 10 V_{PP} signal).

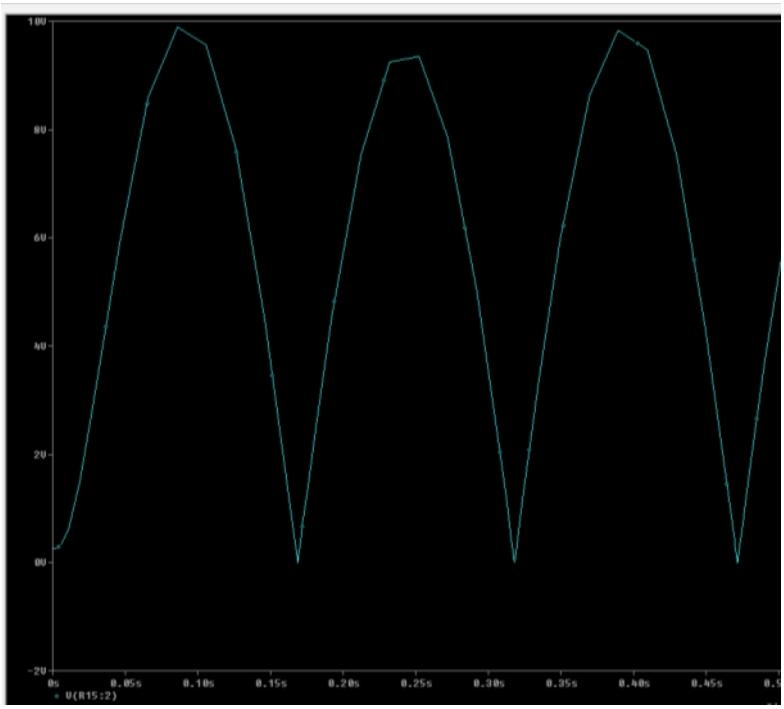


Figure 67: Full Wave Rectifier output waveform. Axes: X – time (0:0.5 sec); Y – output voltage (-2:10 V).

The Full wave rectifier prepares the signal to be compared against the comparator that is just comparing $+V_P$ against a set DC voltage from a potentiometer. The voltage is still below 10 V_P (the threshold that was set to test the system for 2 mil offset) and as such should still work.

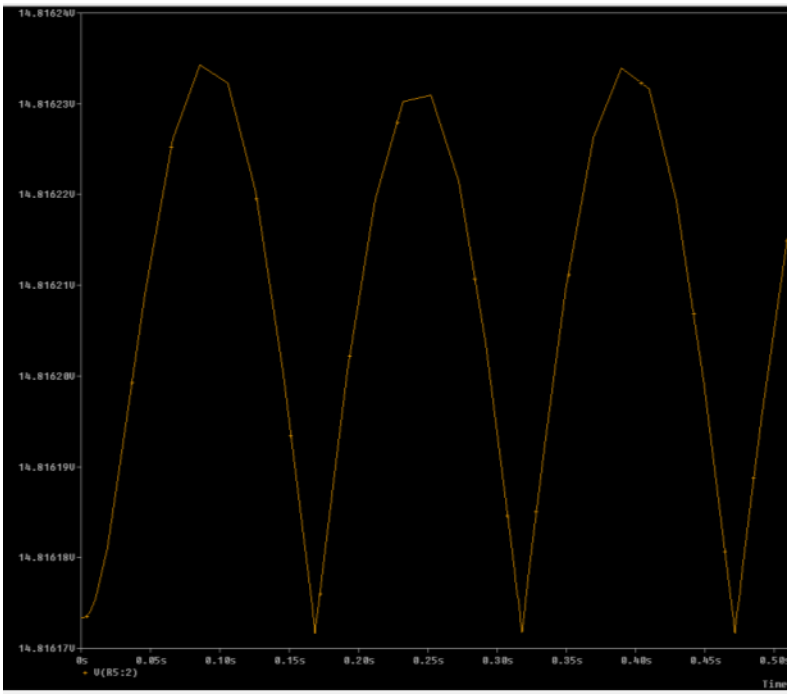


Figure 68: Inverting Comparator w/ hysteresis. Axes: X – time (0:0.5 sec); Y – output voltage (14.81617:14.81624 V).

The signal is balanced so the comparator outputs a '1' or approximately 15V. The output fluctuates between 32-41uV which is negligible in this case. The full wave rectifier can be seen due to the hysteresis in the system which was added for quicker response time in turning off the centrifuge if the user set threshold is exceeded. Because the comparator output is a '1' the centrifuge can continue to run.

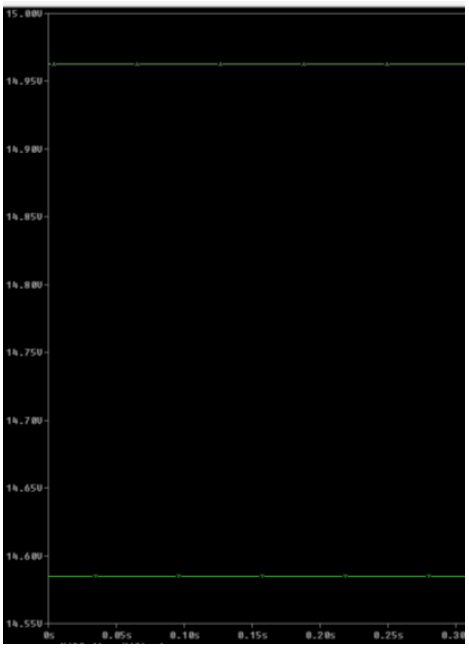


Figure 69: AND gate output waveforms for (B) – top and (S) - bottom. Axes: X – time (0:0.3 sec); Y – output voltage (14.55:15 V).

The system stops running the first time the output voltage reads a +15V. This will cause the final stage transistor to output a '1' which will turn off the SR Latch instead of the SR Latch seeing the normal '0' that allows the centrifuge to normally run.

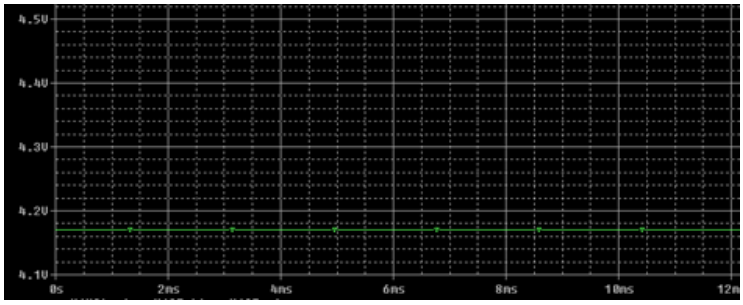


Figure 70: Final Comparator. Axes: X – time (0:12 ms); Y – output voltage (4.1:4.5 V).

With only a '1' present the SR Latch will always see a '1' and the centrifuge cannot run.

POWER SUPPLY AND TRANSFORMER SIMULATION

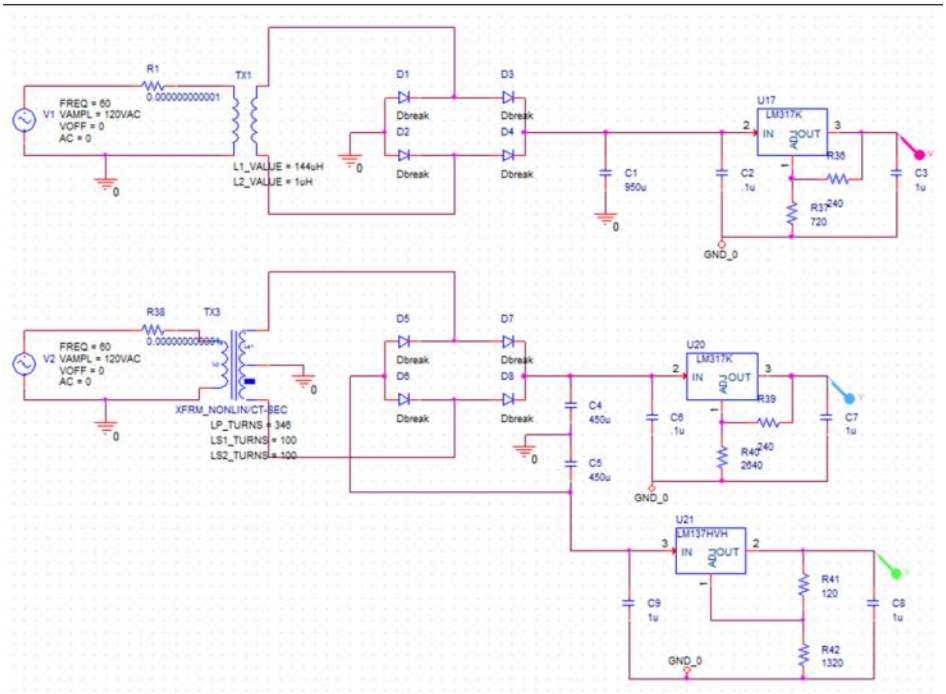


Figure 71: Power Supply Circuit

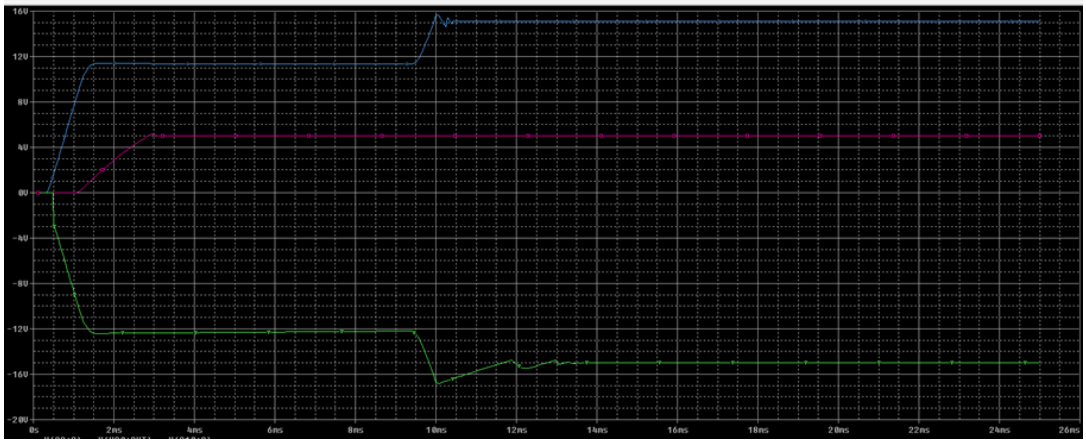


Figure 72: Power Supply Simulations for +5V (purple), +15V (blue) and -15V (green). Axes: X – time (0:26 ms); Y – output voltage (-20:16 V).

The simulation shows that using the design methodology laid out in Chapter 3, a power supply to power the balance probe monitor can easily be designed.

Chapter 7: Tests and Evaluations

Oscilloscope measurements were taken on a prototype that was built after the simulation results successfully showed the operation of the Balance Probe Monitor. These measurements were then compared against the simulated waveforms in Chapter 6 to verify the system worked as intended prior to fabrication of the design.

Signal Legend

- Yellow is the input signal.
- Blue is the signal measured at each op-amp output stage.

SETTING #1

Balanced (B)	Probe Monitor Signal (S)	Run
1	1	1

Table 7: Setting #1 signal input configuration.

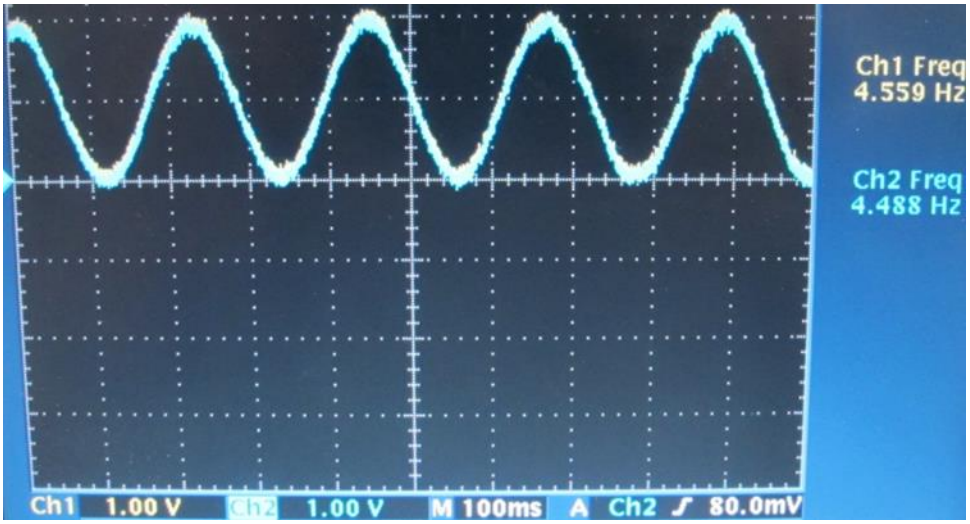


Figure 73: Differential Amplifier (Gain 1) output waveform.

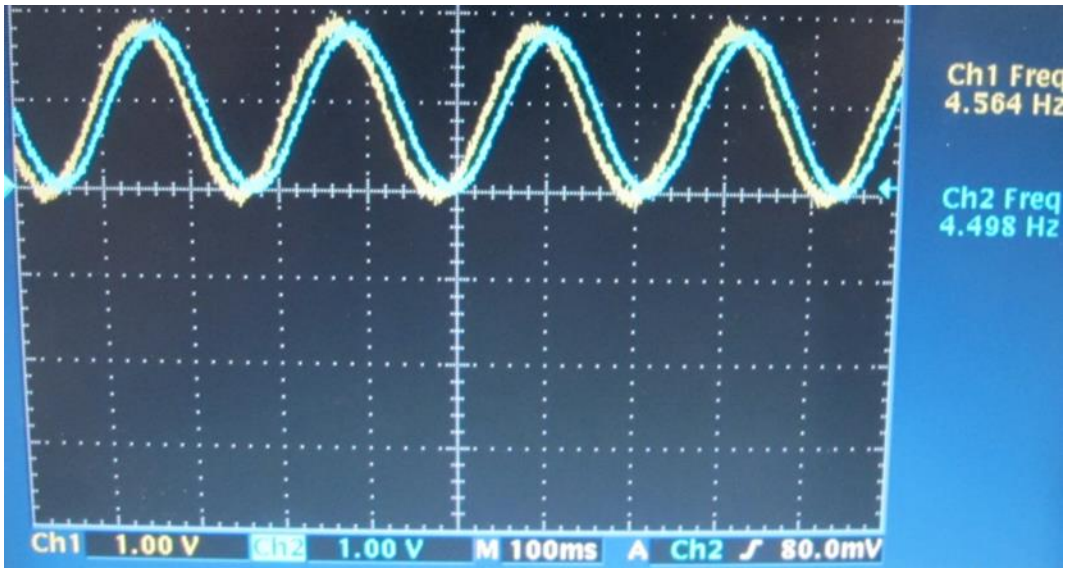


Figure 74: Low Pass Filter with cutoff frequency 20 Hz output waveform.

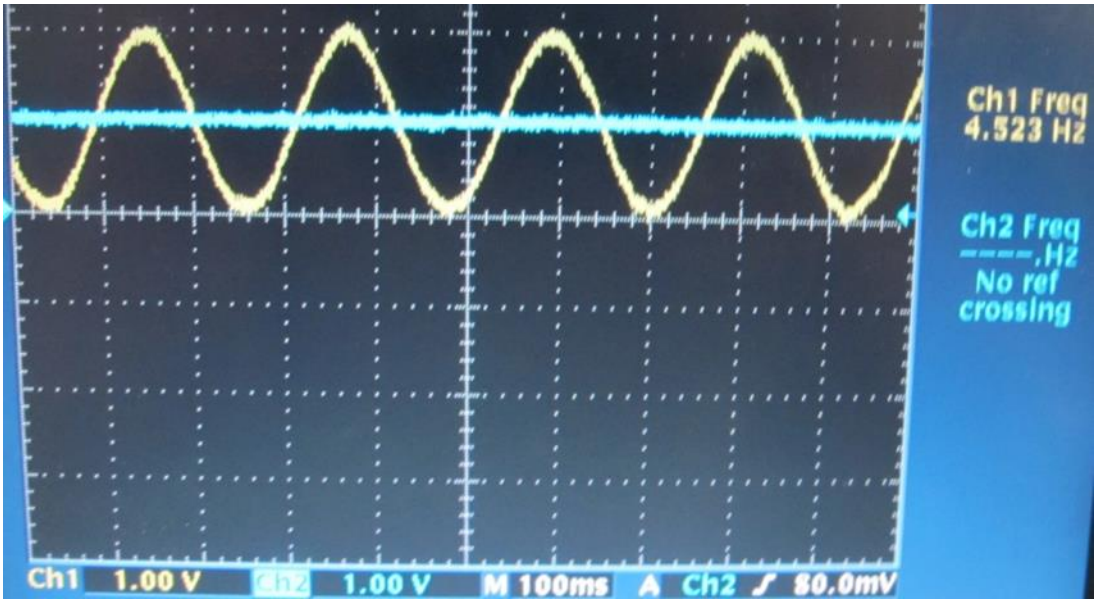


Figure 75: Low Pass Filter with cutoff frequency 0.1 Hz output waveform.

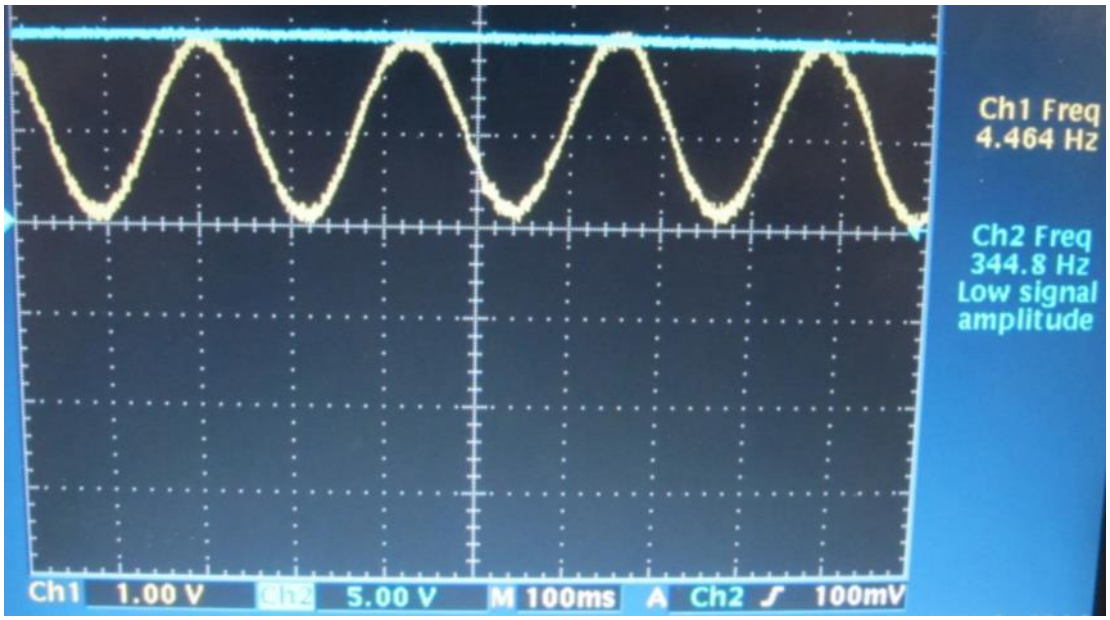


Figure 76: Comparator verifying offset voltage is present output waveform.

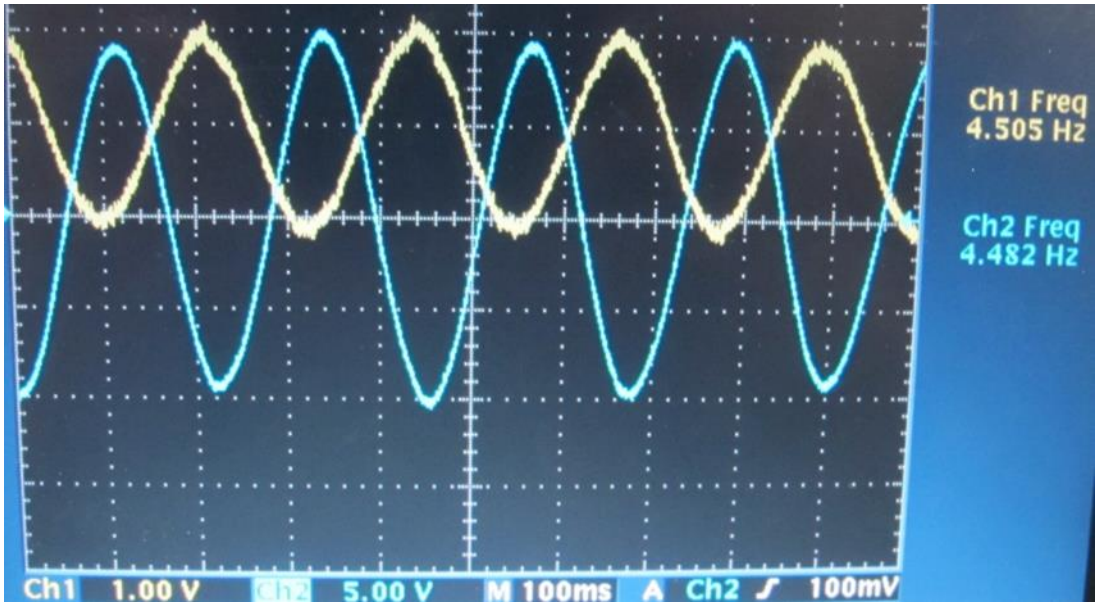


Figure 77: Difference Amplifier (G = 10) output waveform.

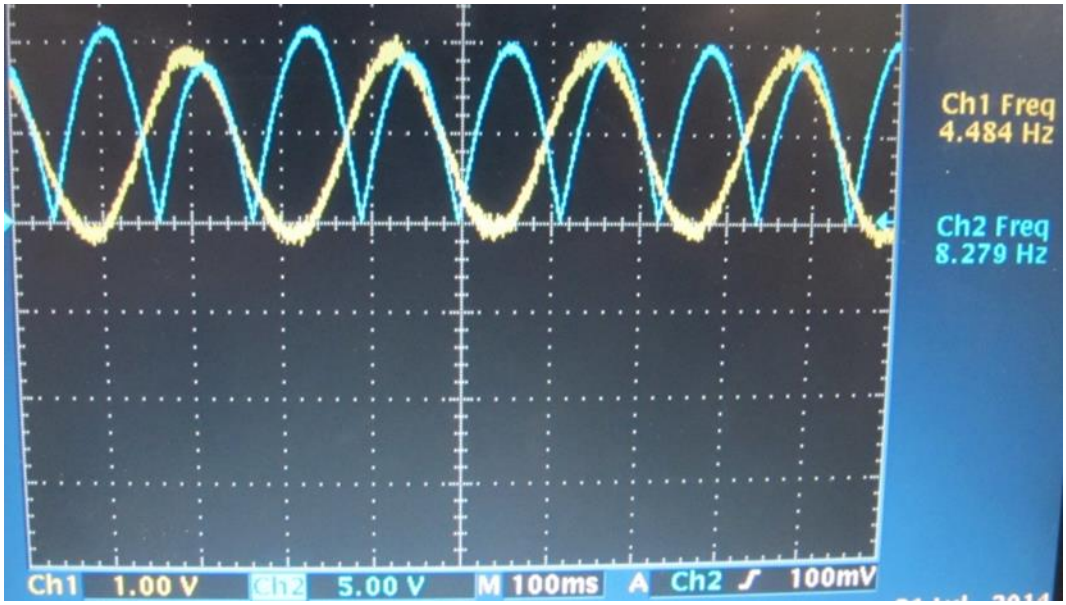


Figure 78: Full Wave Rectifier output waveform.

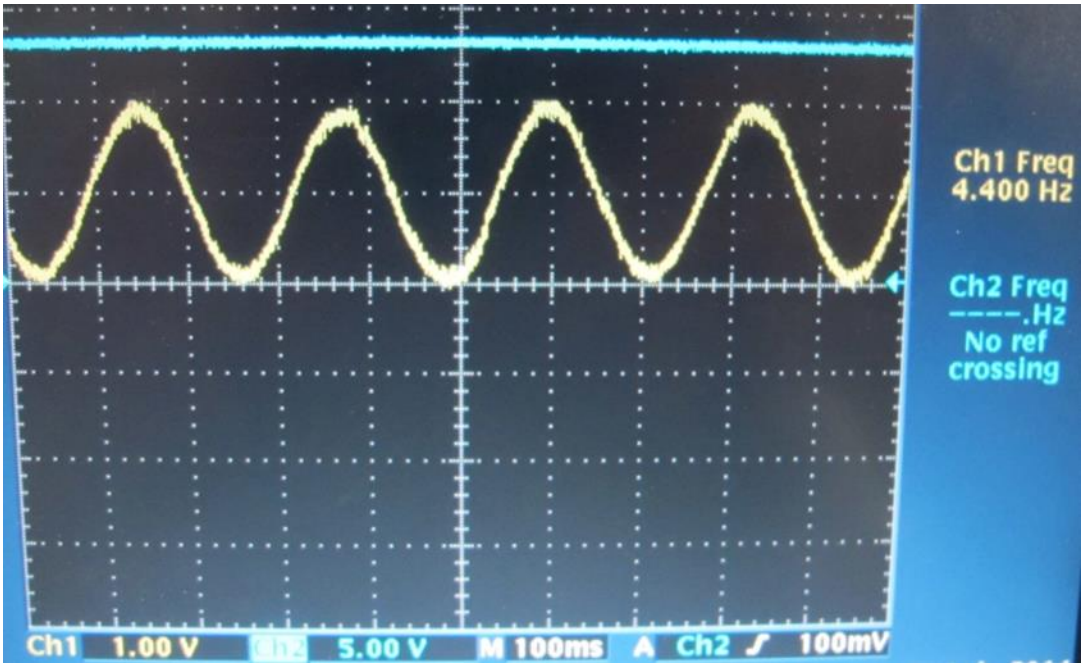


Figure 79: Inverting Comparator w/ hysteresis

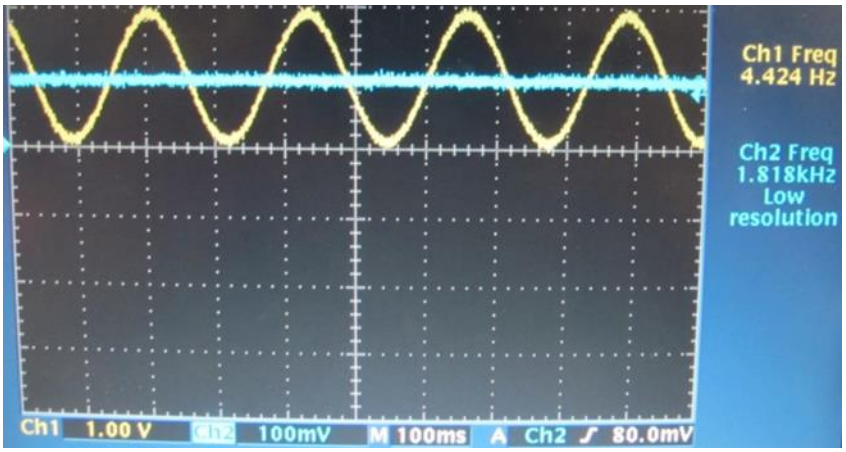


Figure 80: AND gate output waveforms for (B).

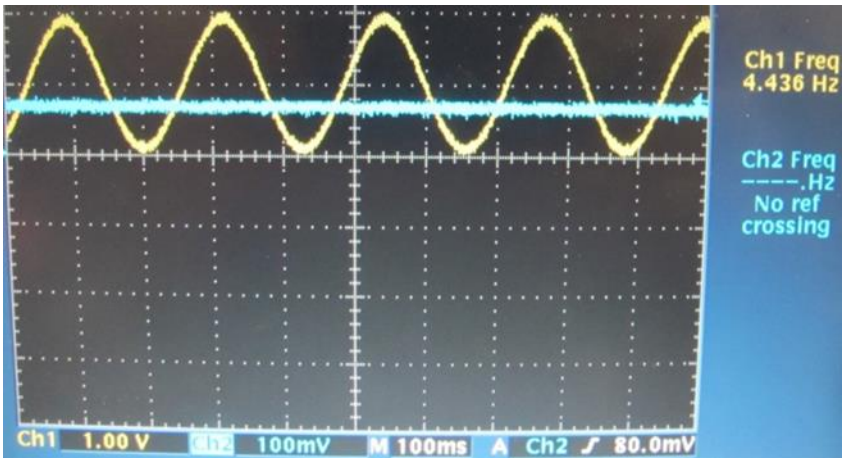


Figure 81: AND gate output waveforms for (S).

Running the BPM in the setting with B = 1 and S = 1 the system did run as intended. As both conditions were met, both transistors of the AND gate opened and the centrifuge was able to have power run to the system.

SETTING #2

Balanced (B)	Probe Monitor Signal (S)	Run
0	0	0

Table 8: Setting #2 signal input configuration.

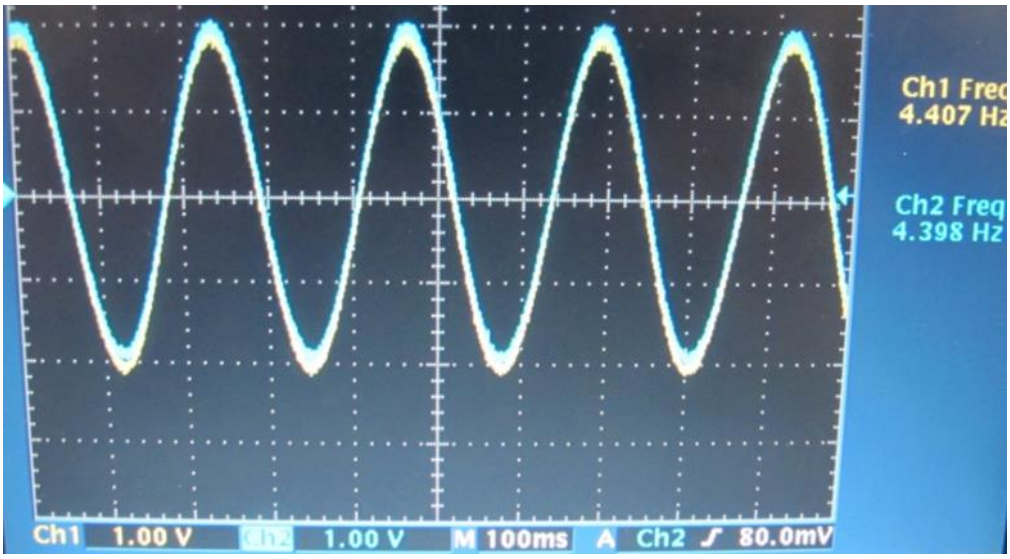


Figure 82: Differential Amplifier (Gain 1) output waveform.

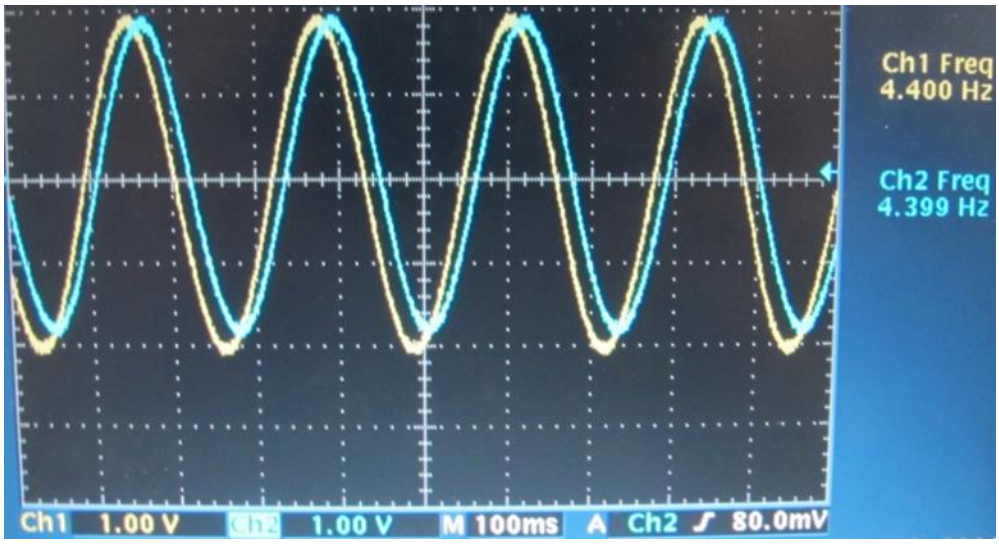


Figure 83: Low Pass Filter with cutoff frequency 20 Hz output waveform.

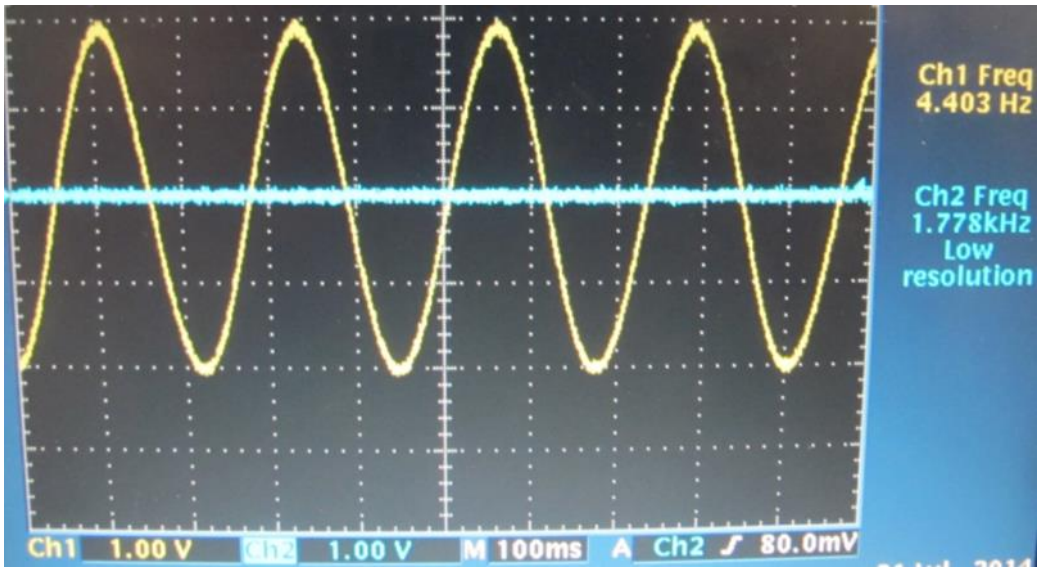


Figure 84: Low Pass Filter with cutoff frequency 0.1 Hz output waveform.

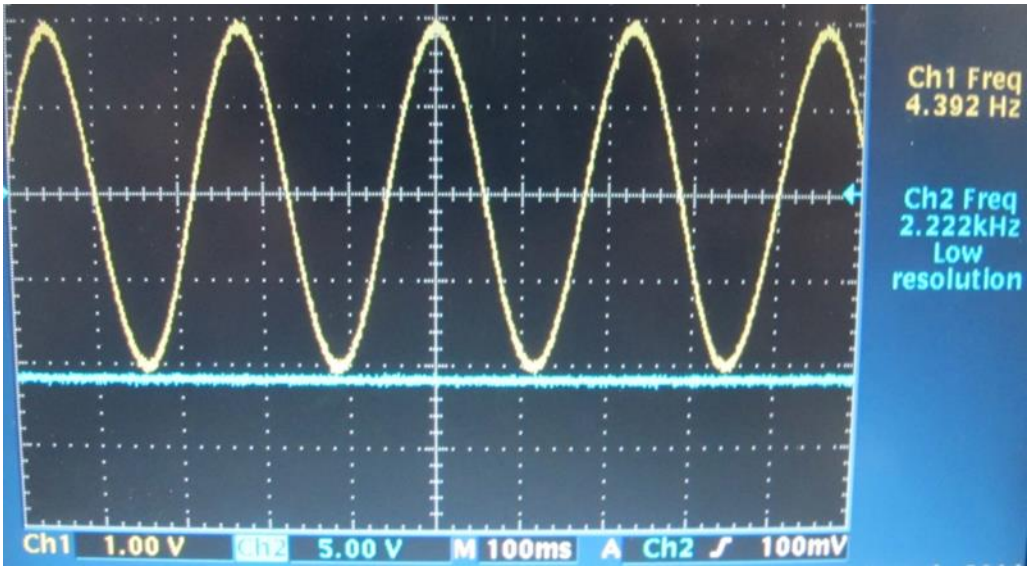


Figure 85: Comparator verifying offset voltage is present output waveform.

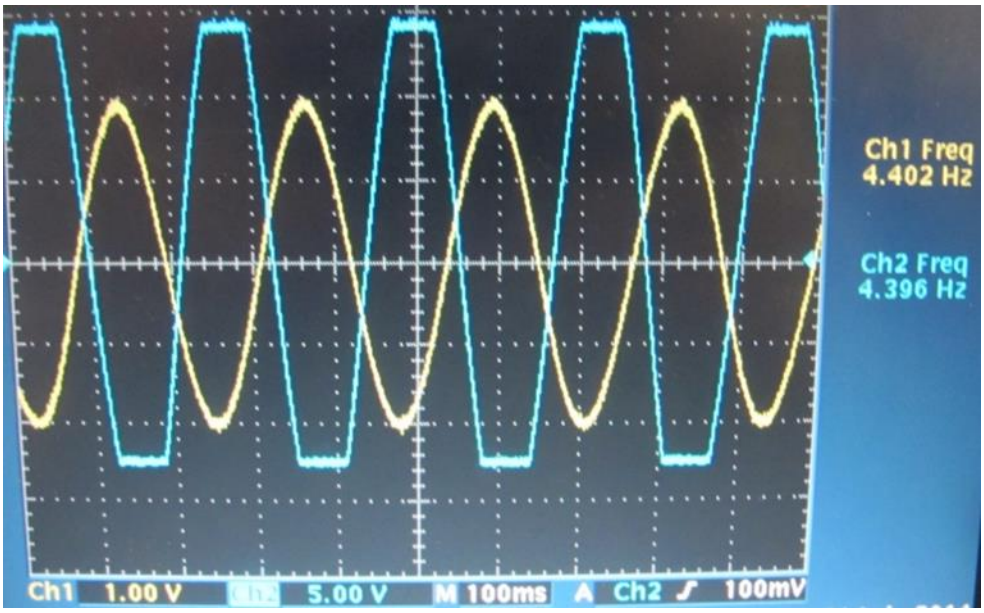


Figure 86: Difference Amplifier (G = 10) output waveform.

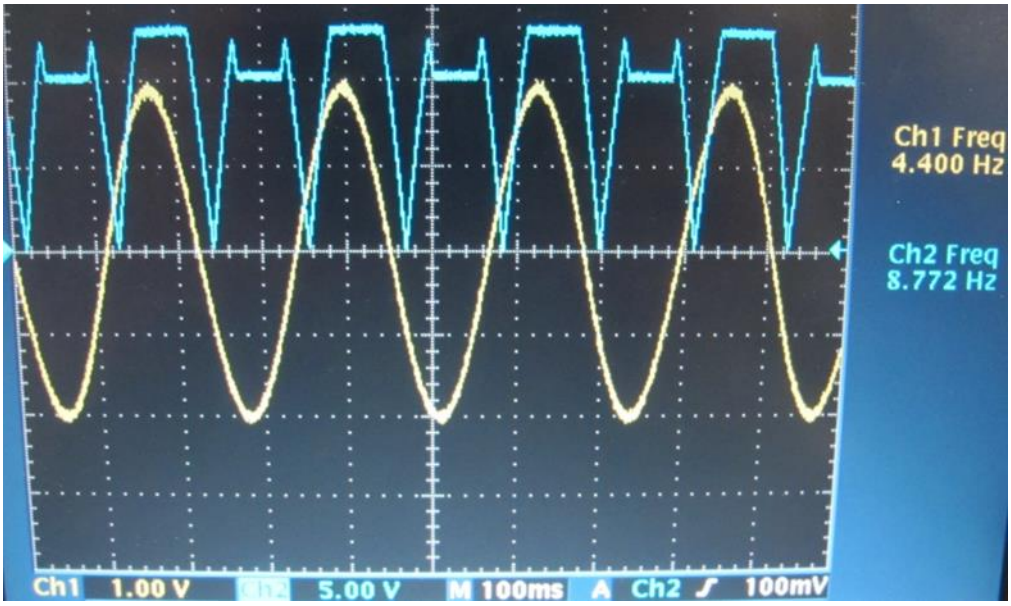


Figure 87: Full Wave Rectifier output waveform.

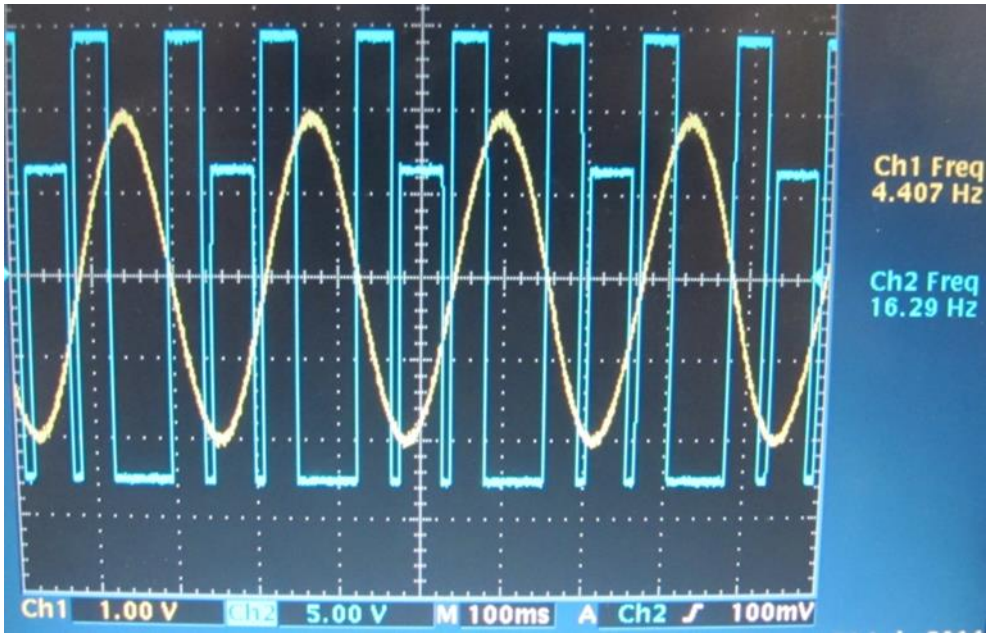


Figure 88: Inverting Comparator w/ hysteresis

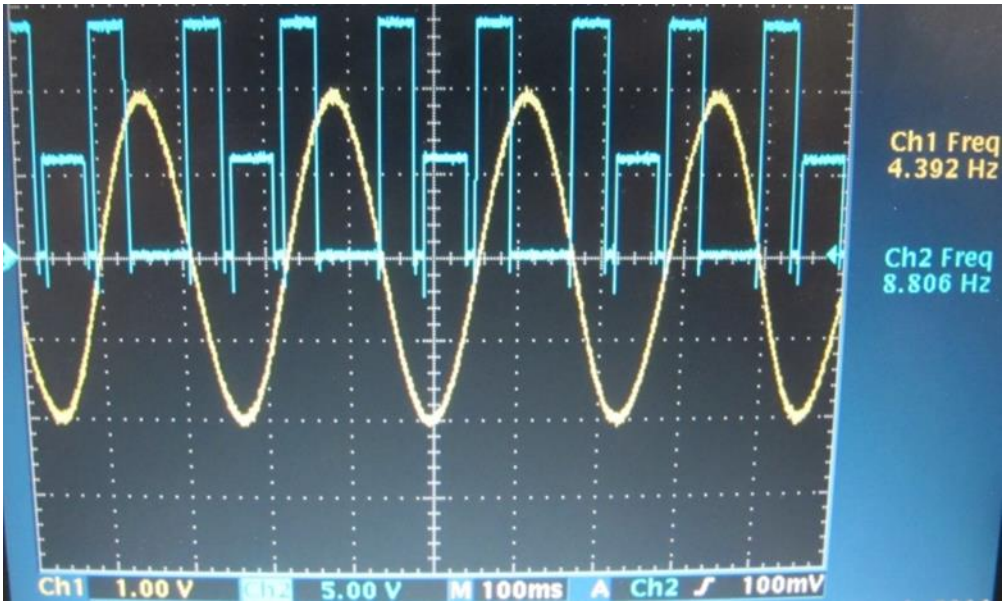


Figure 89: AND gate output waveforms for (B).

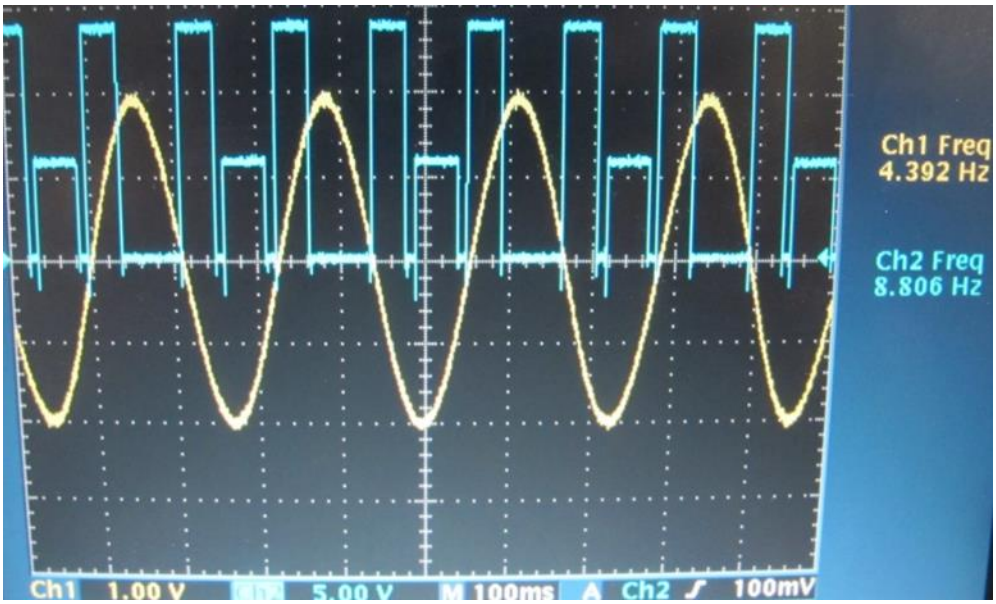


Figure 90: AND gate output waveforms for (S).

Running the BPM in the setting with B = 0 and S = 0 the system did run as intended. As both conditions were not met, neither transistor of the AND gate opened and the centrifuge was unable to have power run to the system.

SETTING #3

Balanced (B)	Probe Monitor Signal (S)	Run
0	1	0

Table 9: Setting #3 signal input configuration.

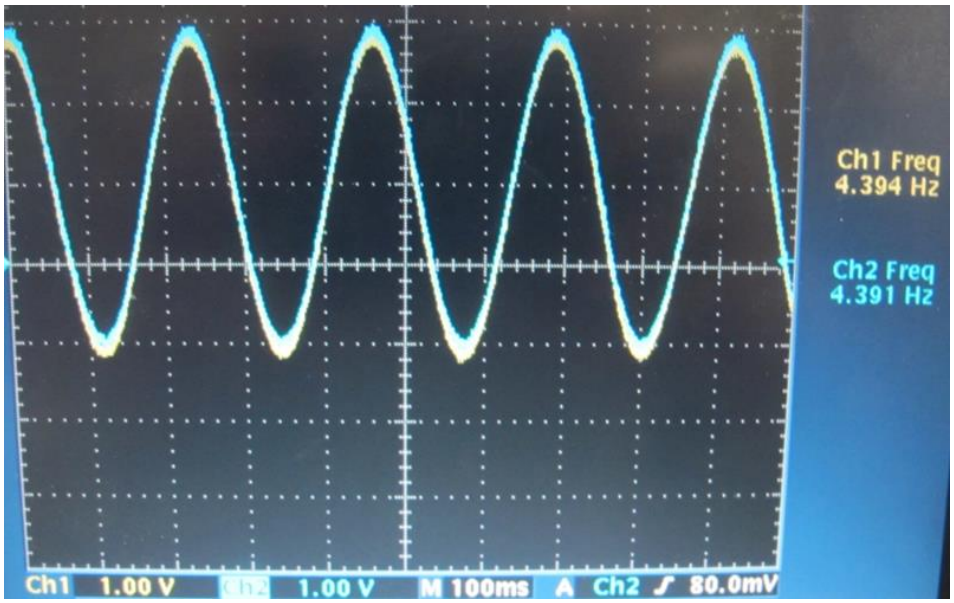


Figure 91: Differential Amplifier (Gain 1) output waveform.

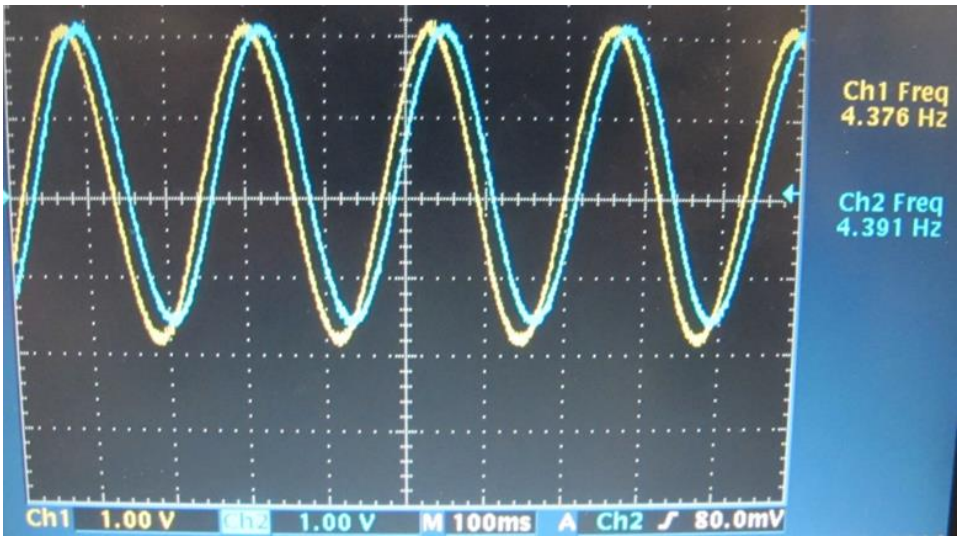


Figure 92: Low Pass Filter with cutoff frequency 20 Hz output waveform.

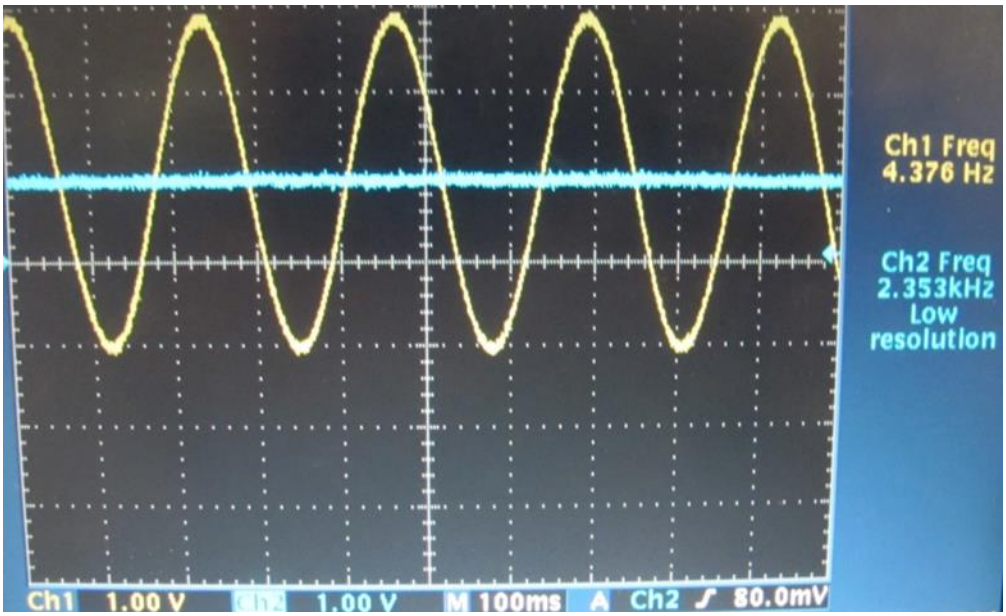


Figure 93: Low Pass Filter with cutoff frequency 0.1 Hz output waveform.

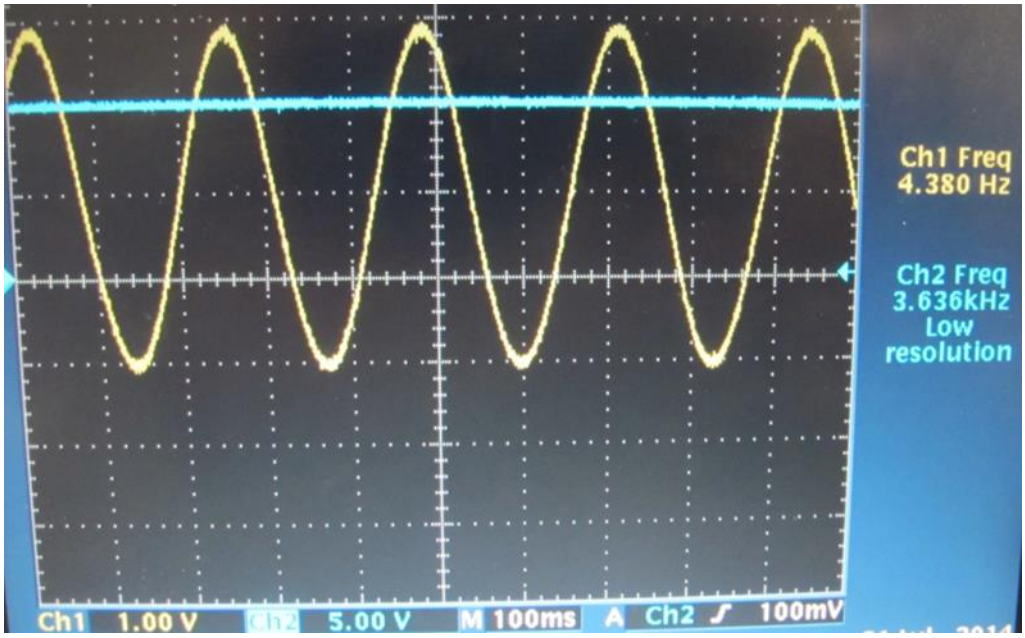


Figure 94: Comparator verifying offset voltage is present output waveform.

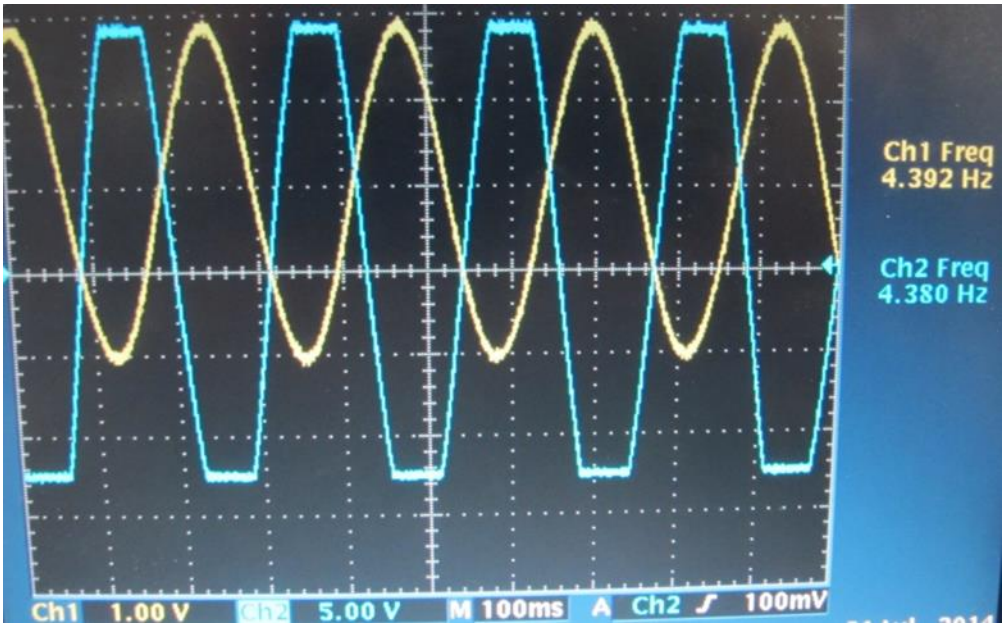


Figure 95: Difference Amplifier (G = 10) output waveform.

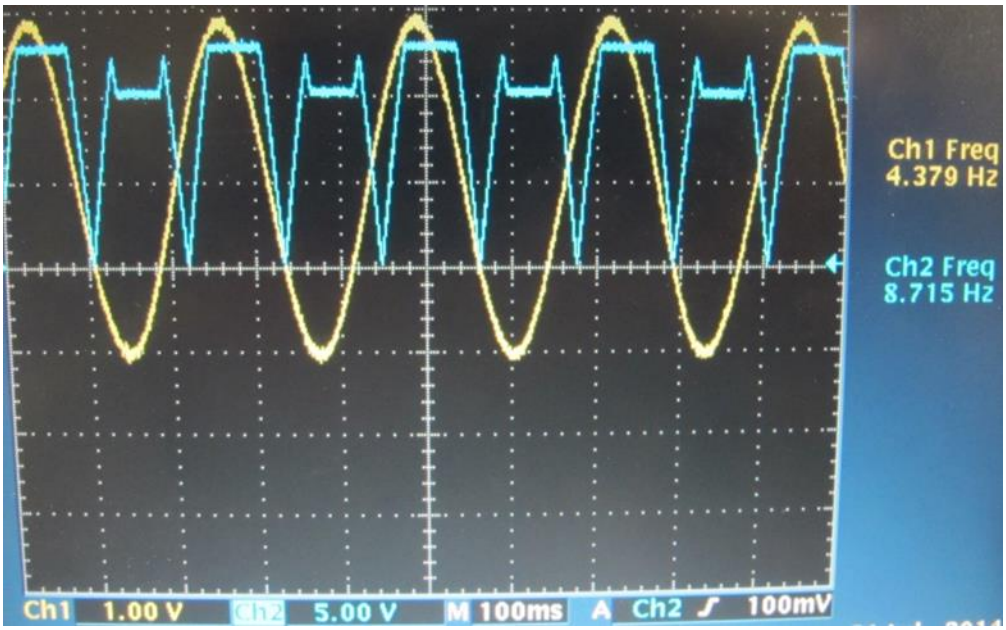


Figure 96: Full Wave Rectifier output waveform.

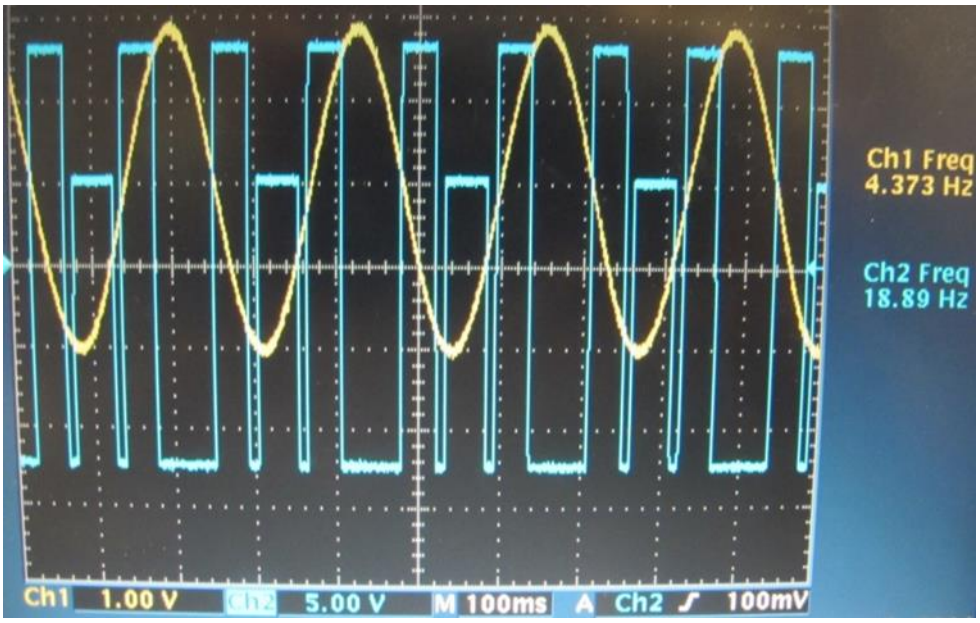


Figure 97: Inverting Comparator w/ hysteresis

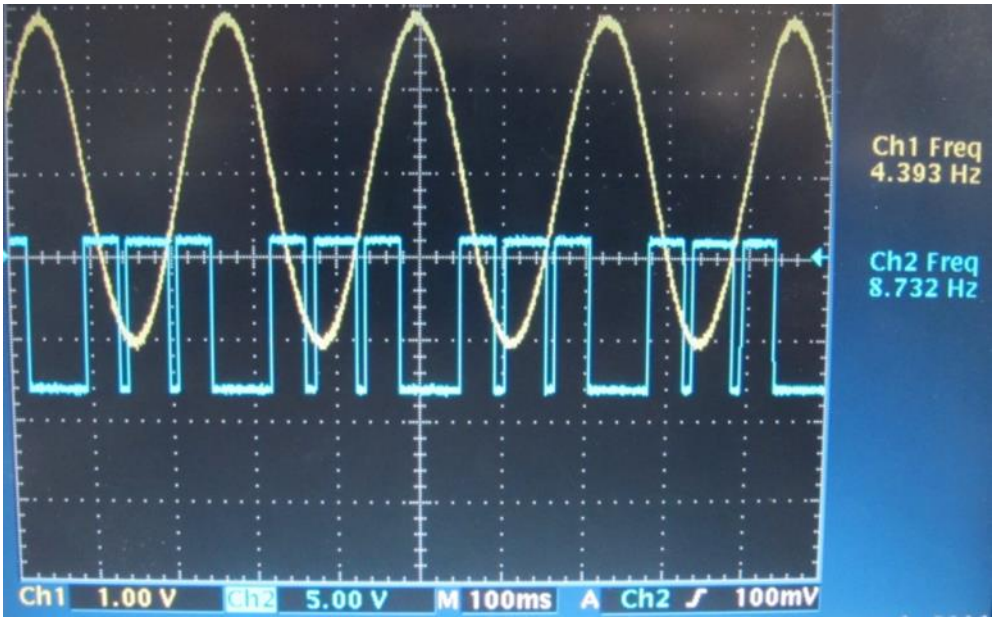


Figure 98: AND gate output waveforms for (B).

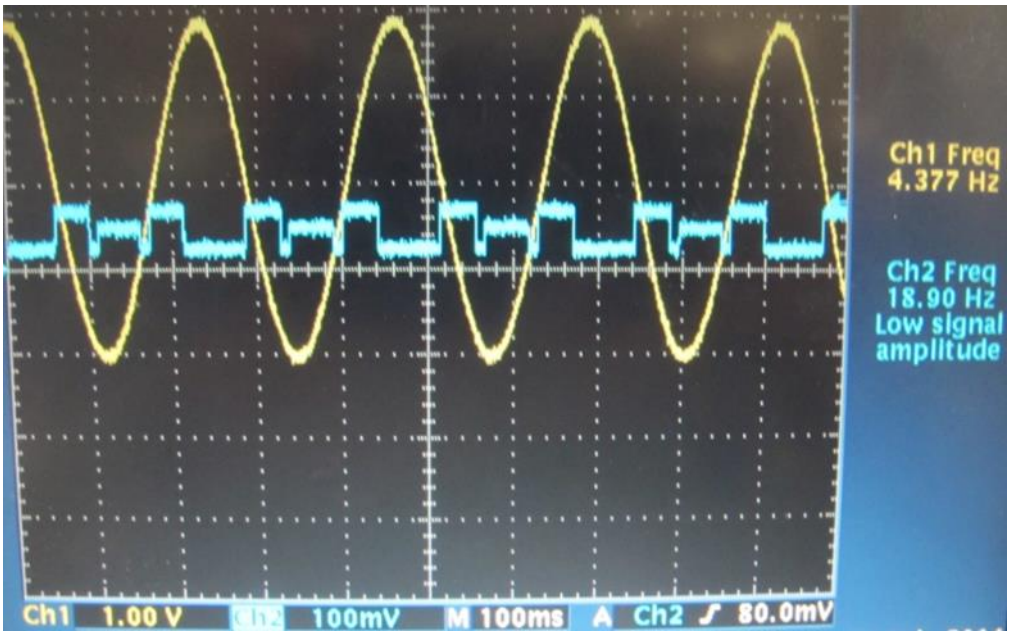


Figure 99: AND gate output waveforms for (S).

Running the BPM in the setting with B = 0 and S = 1 the system did run as intended. As the balance condition was not met, the comparator with hysteresis output a low to the following transistor at the AND gate. In consequence, the centrifuge was unable to have power run to the system.

SETTING #4

Balanced (B)	Probe Monitor Signal (S)	Run
1	0	0

Table 10: Setting #4 signal input configuration.

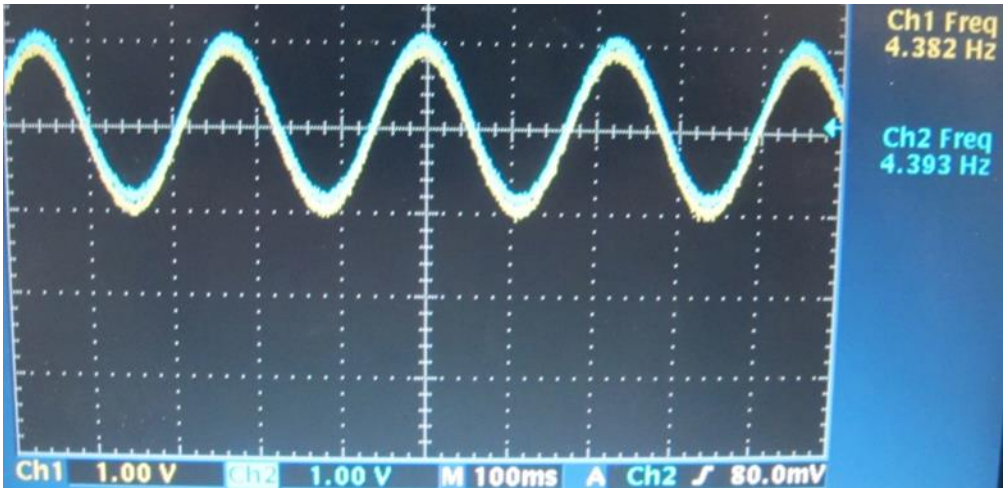


Figure 100: Differential Amplifier (Gain 1) output waveform.

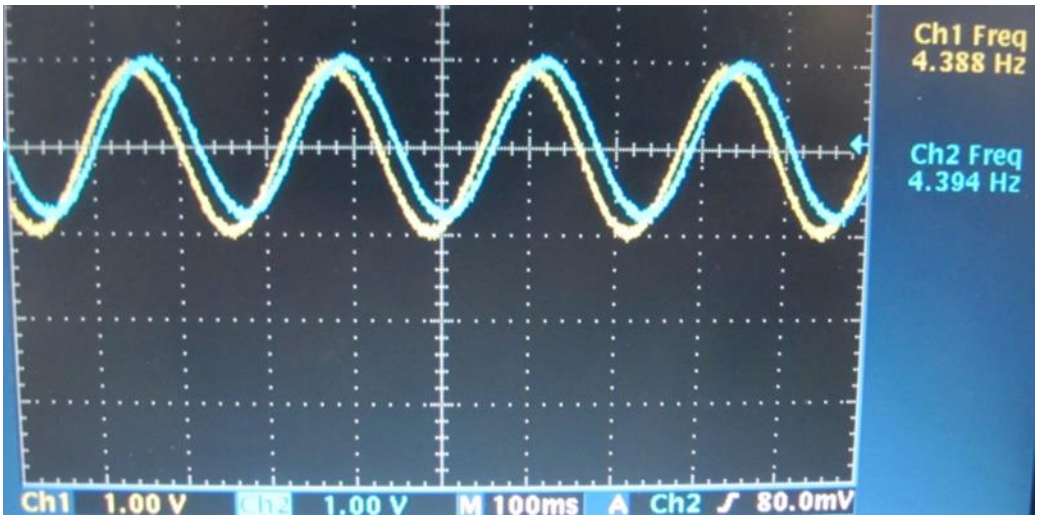


Figure 101: Low Pass Filter with cutoff frequency 20 Hz output waveform.

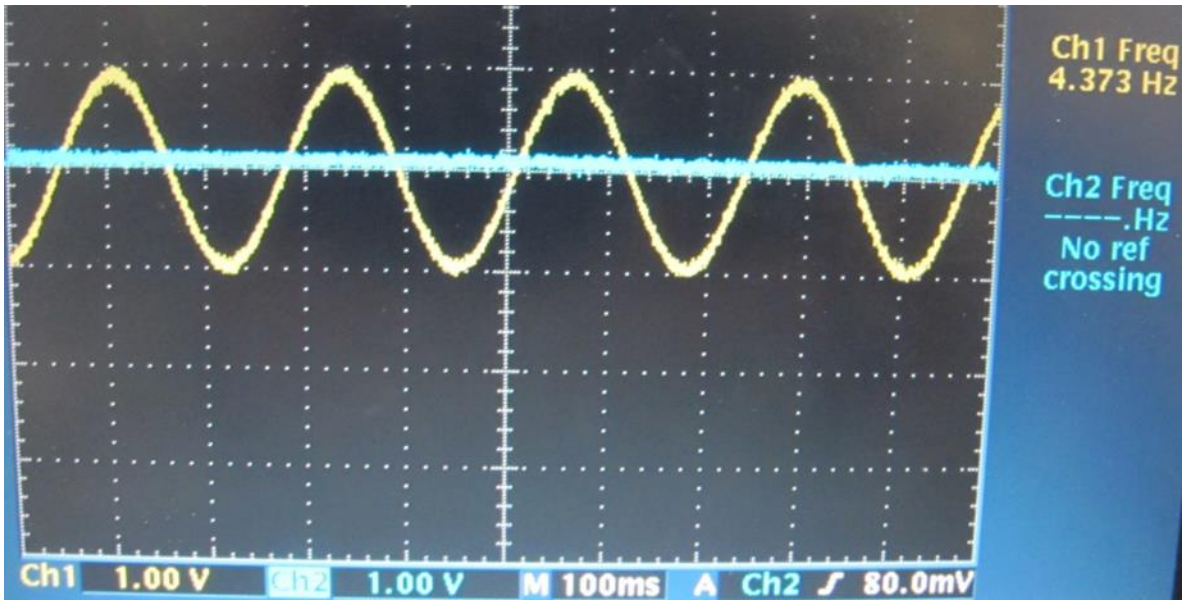


Figure 102: Low Pass Filter with cutoff frequency 0.1 Hz output waveform.

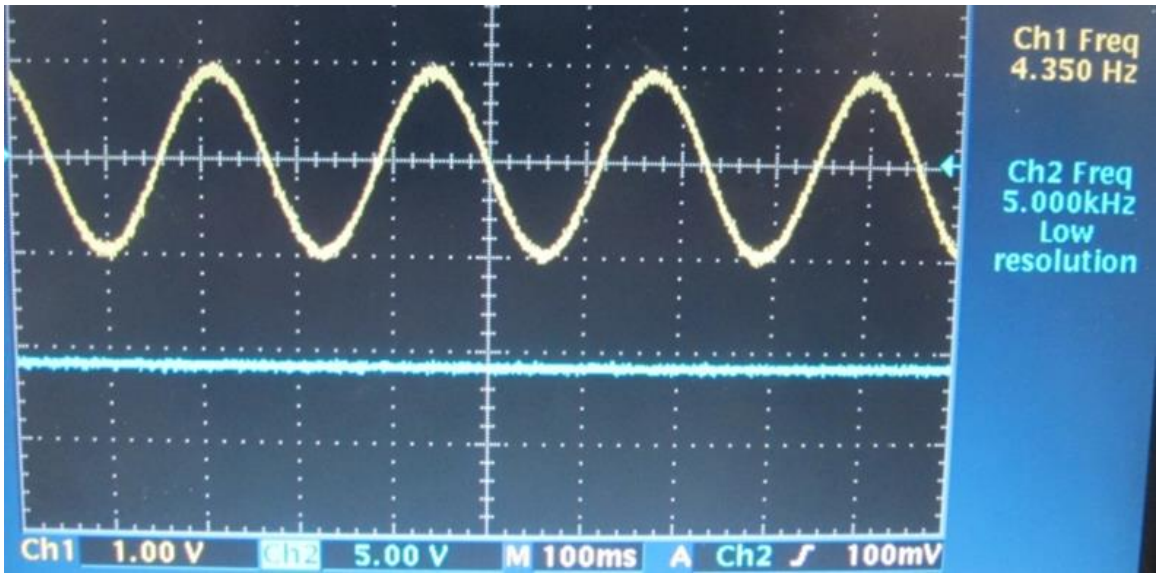


Figure 103: Comparator verifying offset voltage is present output waveform.

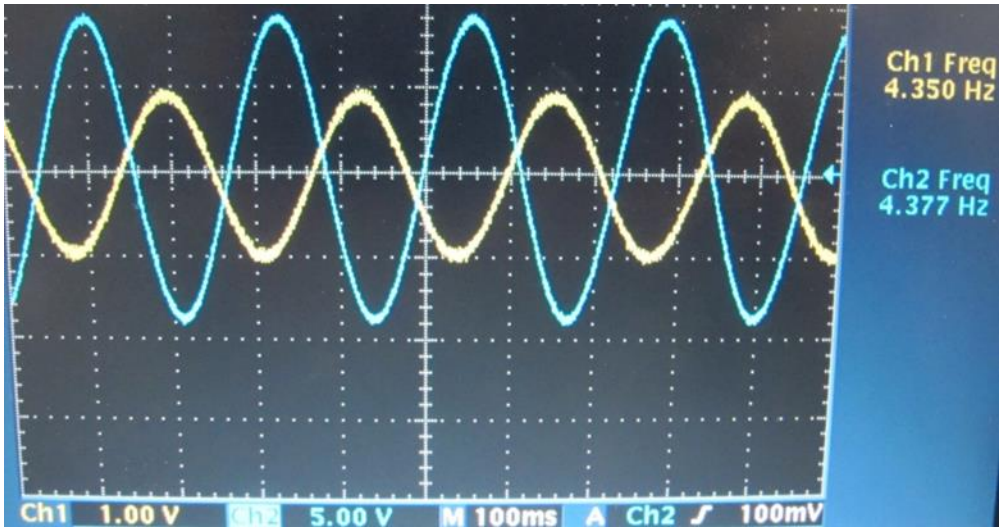


Figure 104: Difference Amplifier (G = 10) output waveform.

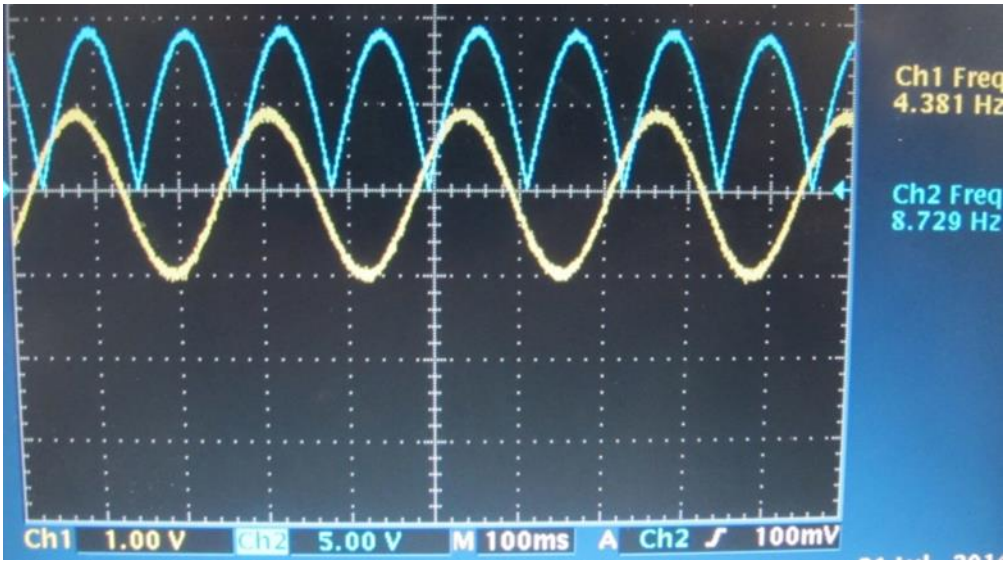


Figure 105: Full Wave Rectifier output waveform.

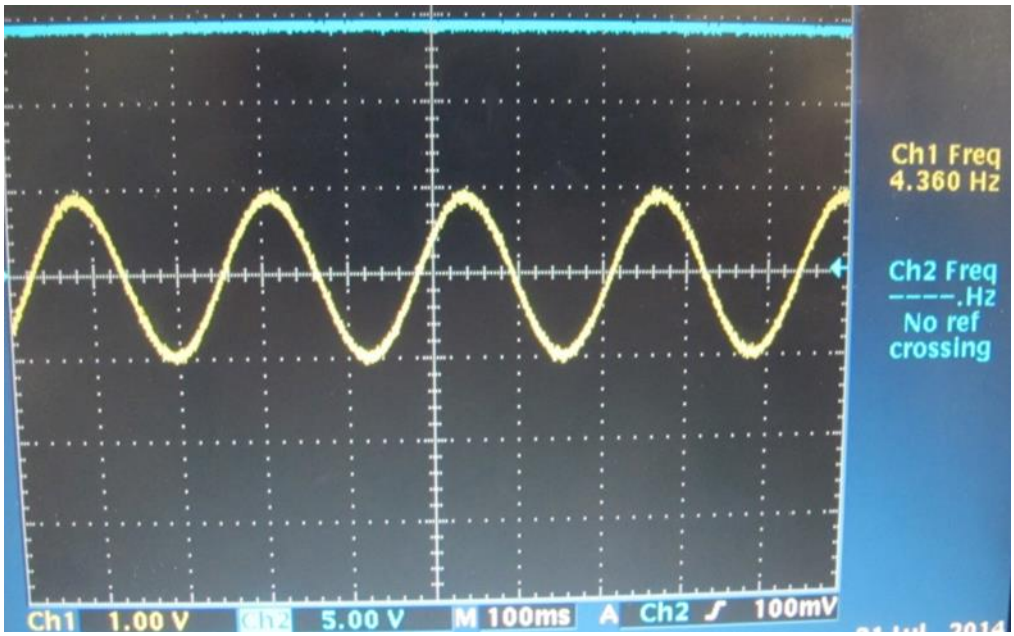


Figure 106: Inverting Comparator w/ hysteresis.

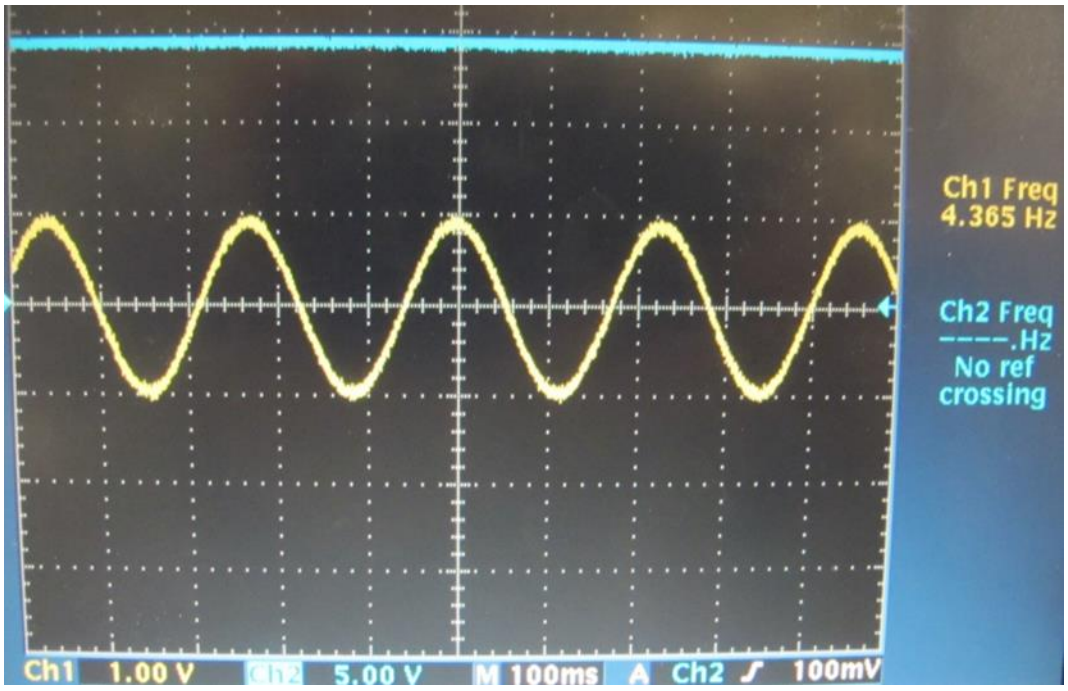


Figure 107: AND gate output waveforms for (B).

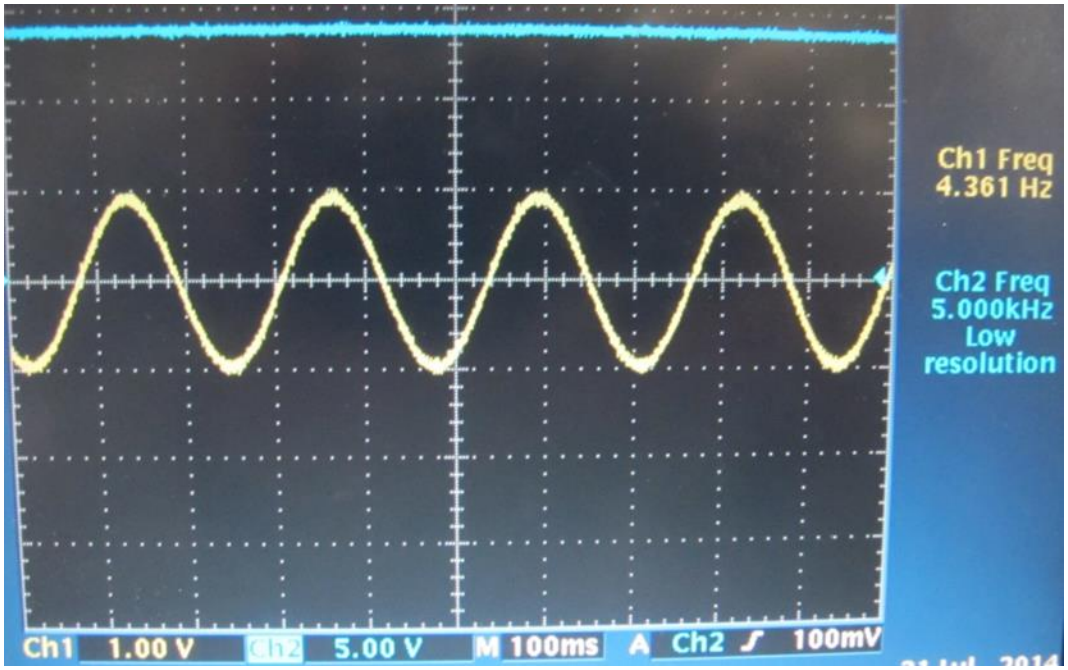


Figure 108: AND gate output waveforms for (S).

Running the BPM in the setting with B = 1 and S = 0 the system did run as intended. As the offset signal was not present, the comparator output a low to the following transistor at the AND gate. In consequence, the centrifuge was unable to have power run to the system.

SIMULATION RESULTS VS TESTED OSCILLOSCOPE RESULTS

After completing the simulated results in OrCAD PSpice and the tested Oscilloscope results on the prototype Balance Probe Monitor the waveforms were compared to one another for consistency as well as to verify that the system did in fact work in every setting as intended.

Comparing every waveform did conclude that the simulated results matched the tested results almost identically, with negligible differences. In addition, the system

worked in all 4 settings (Table 2) as intended. After the successful result comparison, the system was fabricated, and the complete system can be seen below in Chapter 8, Figure 109.

Chapter 8: Kill Switch Testing

COMPLETE SYSTEM

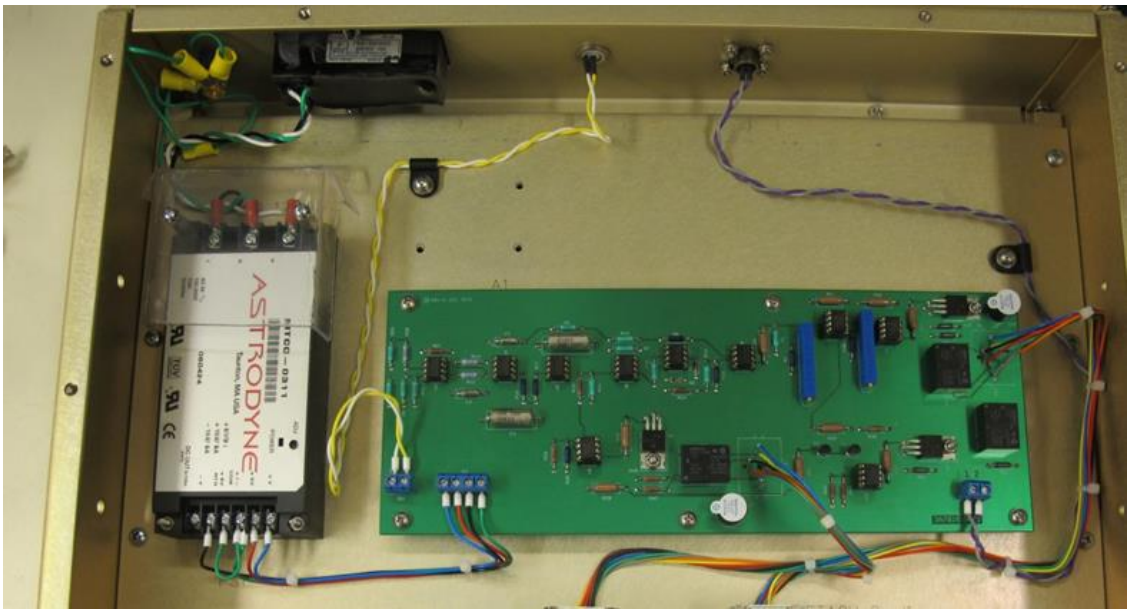


Figure 109: Complete system with power supply and chassis.

TESTING

The board fabrication process was handled by Sandia's drafting department. The drafting department sent the completed schematic to an external vendor to have a two layer Printed Circuit Board (PCB) fabricated then returned to Sandia. Upon receiving the board, all parts were populated onto the PCB. After the board was fabricated and the parts soldered onto the PCB, the board was placed into a system chassis. The board was parametrically tested as a function of: frequency (0-5 Hz), offset voltage (1-5 volts), and displacement tolerance (.5-2 mil where .1 mil = 100mV_{pp}). The initial tasks were checking different frequencies that triggered the kill switch and how the kill switch was

set off by different offset voltages for given displacement tolerances. The measured data can be seen below in Tables 11-14 and Figures 110-113.

Tables 11 and 12 and Figures 110 and 111 tested how accurate the BPM was on triggering the kill switch when a 1 Volt offset was present across relevant frequencies. Testing showed that a system tuned to kill at 0.5 mil (501mVpp) would not consistently kill at 0.5mil across different frequencies. For instance, at 1 Hz the BPM would kill at a different value than had the system been calibrated to kill at 2 Hz. For example, in Table 11 we can see that the BPM was calibrated to kill at .501 mil (501mVpp) at 1 Hz but would kill at .509 mil (509mVpp) at 2 Hz and would kill at .517 mil (517mVpp) at 3 Hz etc. This meant that the system needed to be tuned for a specific frequency for the highest possible precision and accuracy of when the kill triggered. The BPM data showed that the highest centrifuge displacement occurred at higher RPM. The centrifuge could go up to 300 RPM so data was taken to that value but the highest rate the centrifuge is actually run at is 200 RPM so the system was tuned at 3.33 Hz. Test data was taken for 1, 2, 3, 3.33, 4, and 5 Hz.

Tables 13 and 14 and Figures 112 and 113 again tested how accurate the BPM was on triggering the kill switch but with different offset voltages present (this scenario would likely never occur, but the settings were tested to see how the system would perform under such an anomaly). As the system was designed for a 1 volt offset so that was the starting value. The remaining tests were incremented by 1 volt offsets up to 5 volts. Suprisingly, the offset voltages did have impacts on a system. The higher the offset voltage the more premature the kill would trigger (possibly due to thermal

properties and higher current flow in the system) and again, the frequency did have an impact on triggering the kill. This led to the conclusion that the BPS needed to be tuned semi-frequently to ensure the BPM had a 1 volt offset and would trigger at 501 mVpp at .5 mil or 2001 mVpp at 2 mil at 3.33 Hz.

Kill	Hz					
1 V offset	1	2	3	3.33	4	5
mVpp	501	509	517	521	528	542
mVpp	493	501	509	512	520	533
mVpp	485	493	501	504	512	525
mVpp	482	490	498	501	509	522
mVpp	474	481	489	492	501	512
mVpp	463	471	479	481	489	501

Table 11: 0.5 mil kill switch with 1 V offset at different frequencies.

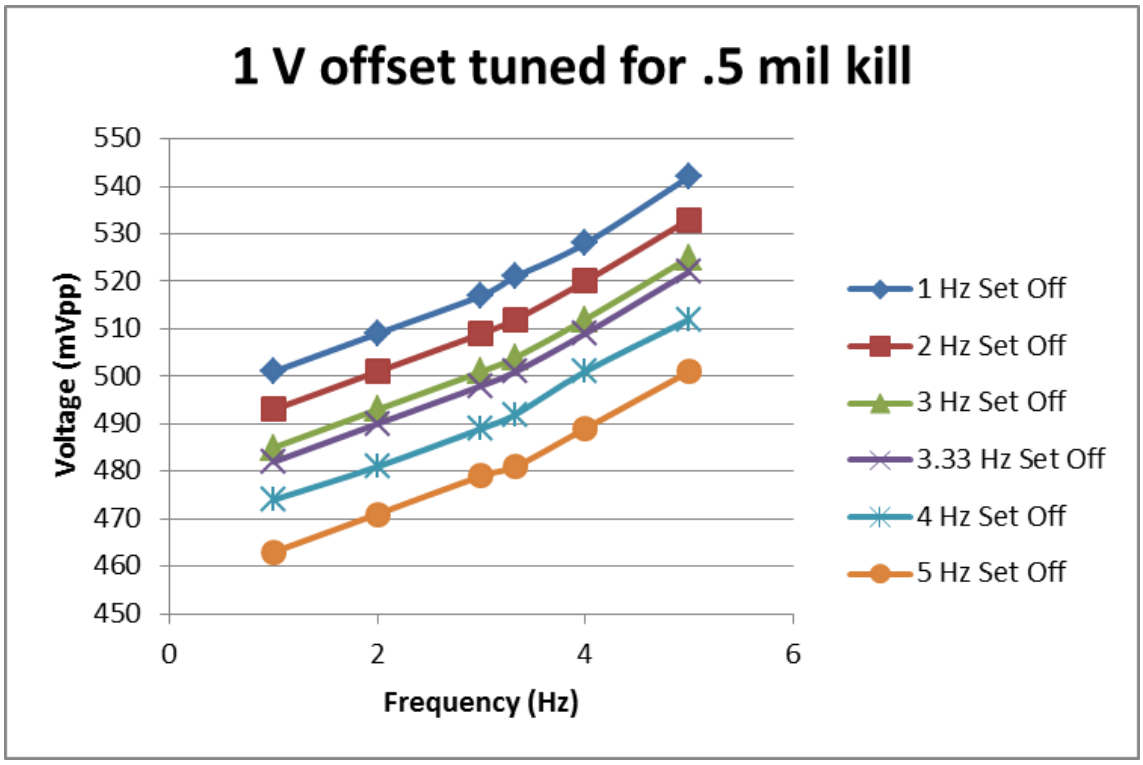


Figure 110: Output data for Table 11 – 1 V offset tuned for .5 mil kill.

Kill	Hz					
1 V offset	1	2	3	3.33	4	5
mVpp	2001	2035	2067	2081	2111	2165
mVpp	1969	2001	2035	2047	2077	2128
mVpp	1939	1971	2001	2015	2045	2099
mVpp	1928	1960	1991	2001	2033	2084
mVpp	1896	1928	1959	1971	2001	2051
mVpp	1850	1881	1912	1924	1953	2001

Table 12: 2 mil kill switch with 1 V offset at different frequencies.

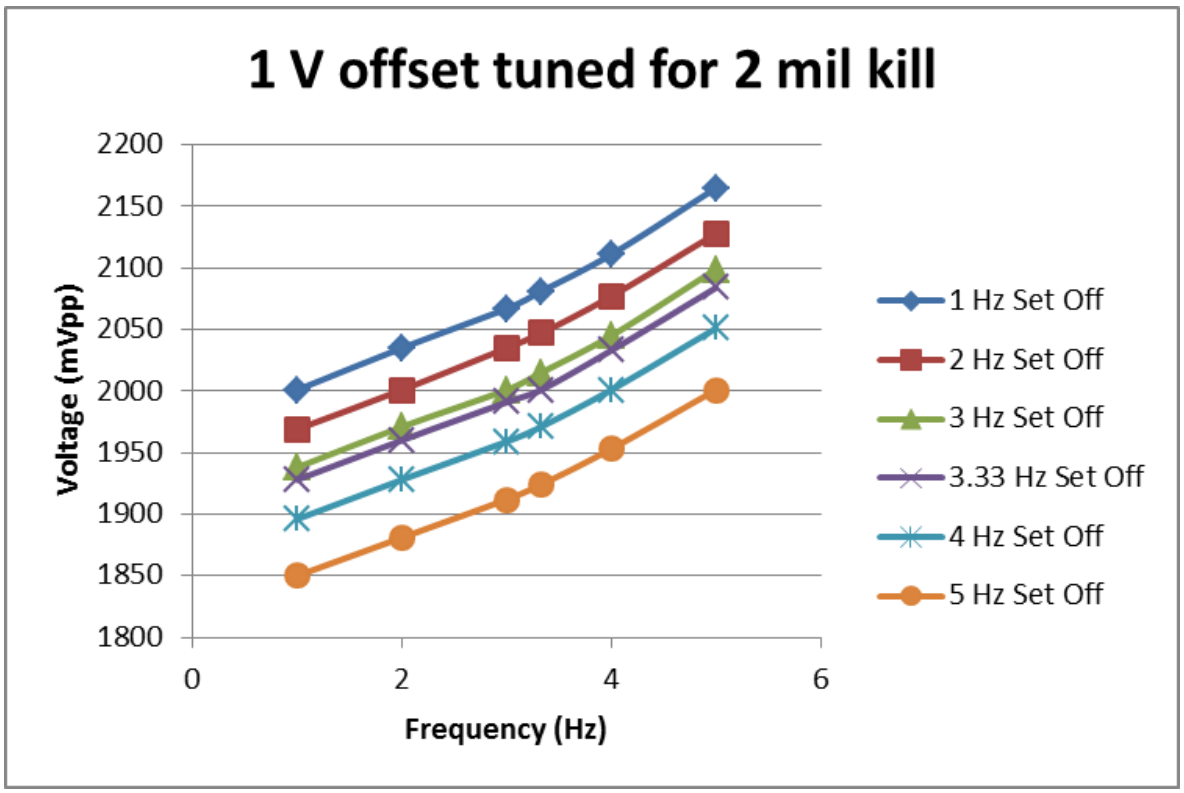


Figure 111: Output data for Table 12 – 1 V offset tuned for 2 mil kill.

Kill	Hz					
Offset	1	2	3	3.33	4	5
1 V offset	501	509	517	521	528	542
2 V offset	501	512	519	522	530	543
3 V offset	497	505	515	519	525	539
4 V offset	486	496	508	509	518	528
5 V offset	465	476	487	488	496	507

Table 13: 0.5 mil kill switch with staggered offset voltages at different frequencies.

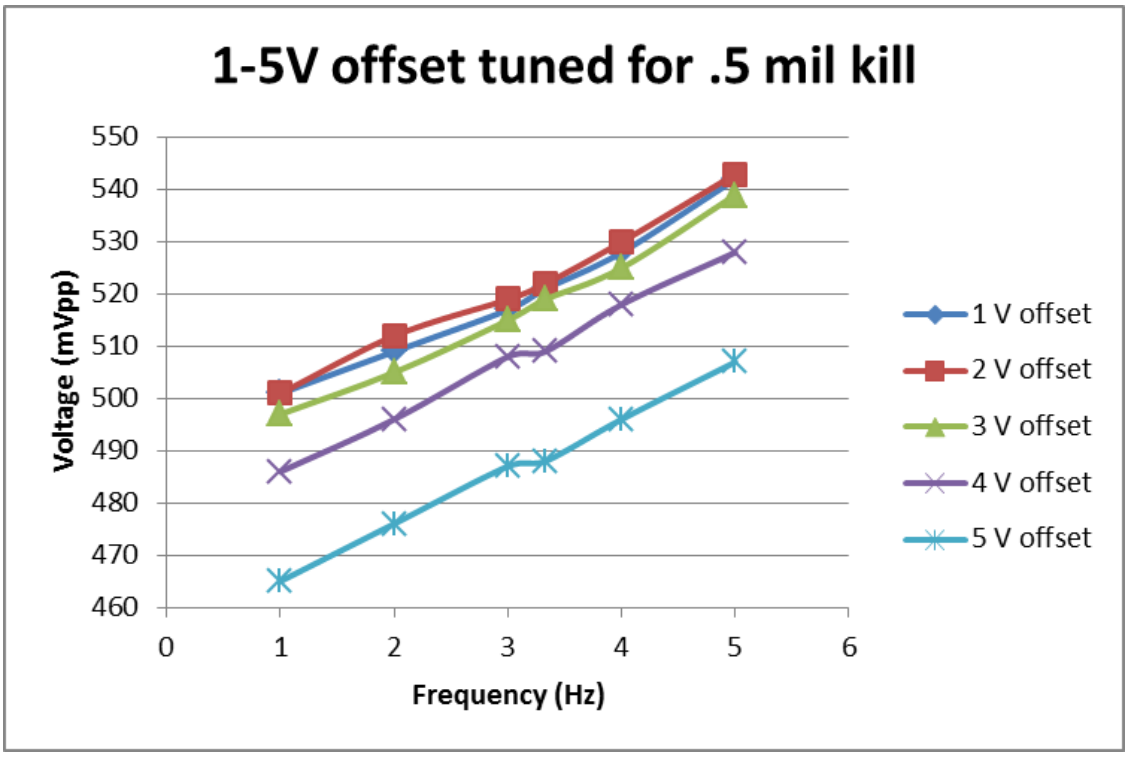


Figure 112: Output data for Table 13 – 1-5 V offset tuned for 0.5 mil kill.

Kill	Hz					
Offset	1	2	3	3.33	4	5
1 V offset	2001	2035	2067	2081	2111	2165
2 V offset	1993	2037	2063	2072	2108	2156
3 V offset	1969	2001	2035	2047	2077	2128
4 V offset	1933	1974	2019	2029	2060	2097
5 V offset	1850	1895	1936	1946	1973	2013

Table 14: 2 mil kill switch with staggered offset voltages at different frequencies.

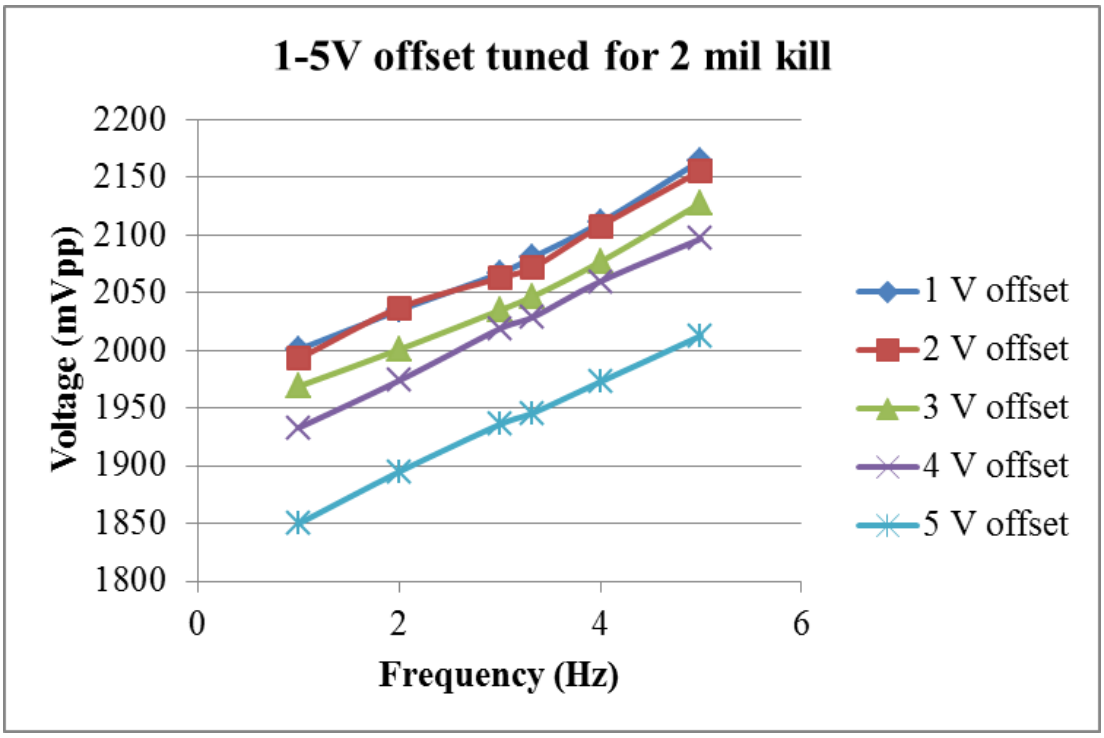


Figure 113: Output data for Table 14 – 1-5 V offset tuned for 2 mil kill.

The system was tuned to kill power to the centrifuge for 501mVpp for each frequency at 0.5 mil and 2001 mVpp for each frequency at 2 mil . The system was designed for a 1V offset so the system was tuned and tested for 1 V offset even when higher offset voltages were applied for testing.

It can clearly be seen the values change over the expected frequencies, but there is not a huge variation as the kill is still activated within hundredths of mils of the desired threshold. A major balance offset would activate the kill all the same.

The Balance Probe Monitor worked as designed and only killed the centrifuge's power when the system was out of balance or did not have an offset voltage present. The system worked for one calibration (within a certain tolerance). Tuning is only required for an extremely precise kill threshold at a known operation RPM.

Chapter 9: Conclusion and Future Work

Referencing the Tests and Evaluations section, we can see that the circuit performed as expected in the four configurations of the AND Gate. When the Signal and Balance were both sending a '1' the circuit worked as designed. However, when the circuit had any configuration where at least one of the two settings were '0' the circuit's BJT transistors did not open because $V_{BE(on)}$ was not met by having the required 0.7 volts to "turn on" the transistor allowing for the current to flow through the circuit. When the circuit is in a setting where the BJT transistors do not turn on or cycle back and forth between off and on, the kill switch is activated. Put another way, power is terminated to the centrifuge, thus preventing system failure and wear and tear, mitigating risks that could harm machine operators, and ensuring the safety of the UUT. As expected, the higher the RPM, the greater the displacement experienced by the centrifuge.

The balance interlock and monitor have to be manually reset if the required parameters are at any given time not met. So if a parameter cycles between the BJT having an on and off setting the moment it hits the "off" setting it will not continue to provide power because the kill switch will have been triggered and needs to be manually reset.

The system was verified by using hand calculations, PSpice simulations, oscilloscope measurements, and as a fabricated breadboard circuit.

As the Balance Probe Monitor worked as prescribed there is little other work needed to enhance this system at this time. However, there are room for improvements. Some suggestions would be to redesign the board with more COTS parts to simplify the

board and mitigate parts count. Another suggestion would be to do a study on what exactly is causing the frequency variation of the kill point and try and resolve that issue for increased precision of the kill point. Future features to consider might be a display of the centrifuge displacement to allow centrifuge operators realtime data to better react to protecting the centrifuge. At this time, that is not needed to meet the requirements of the system, so no future work is currently planned.

Appendix 1: Centrifuges

Centrifuges allow for an object to be spun at different gravitational forces (G's) in relationship to earth's gravitational pull. This is accomplished by rotating the object around a fixed point with a set radius r. From there, the centrifuge capitalizes on the principle of centripetal acceleration to actually apply the G's. Different sized centrifuges are used for different applications (as the radius is adjusted for different applications to achieve different desired G forces). These centrifuges have numerous practical applications across various fields. Some centrifuges are used to give astronauts experience to different gravities they will experience in orbit and prepare them for different forces they will encounter, others are used for testing liquids in medical and clinical research, while others test satellites, and test how the components of the system will survive in harsh terrain, in addition to that, they are also seen at the manufacturing and home level. At the home level they can be seen in washing machines and manufacturers use them to separate out different solids or liquids. This feat is accomplished by applying the G's and watching the entities separate due to their different densities. Another industry to incorporate centrifuge use is the Military Industrial Complex.

A major factor that must be taken into consideration when using a centrifuge is safety, safety of the operators of the machine, safety of the machine, and safety of the unit under test (UUT). This means that the payload or UUT on the centrifuge must be carefully balanced. This is usually accomplished by using a combination of techniques that begin with modeling the UUT, actually running the system to find runout, and

watching the output of the balance probe. These techniques are used to mitigate vibration in the centrifuge that risks altering the integrity of the centrifuge and UUT. Imbalanced rotors can lead to damaged centrifuges, personal injury and wasted UUTs. To try and prevent improper use, failure and catastrophic failure of these centrifuges it is imperative safety kill switches are attached to the centrifuge to maximize the life and usefulness of the device, protect components and most importantly protect machine operators.

The angular frequency, omega (ω), may be specified in the units of radians per second or an equivalent RPM. Angular frequency, specified in radians per second and frequency, specified in Hertz are related through the simple equation of $\omega = 2 \pi f$. As expected, the higher the RPM, the greater the displacement experienced by the centrifuge. The displacement imposed on the centrifuge's structure will be measured in micrometers (μm) to stay consistent with Figure 2 measurement data of the AccuMeasure. The AccuMeasure 9000 converts the displacement into an equivalent voltage. The time varying motion of the centrifuge's displacement establishes an AC voltage signal related to position as a function of time.

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