Circuits for Protecting and Triggering SCRs in High Power Converters

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***Abstract*-- The performance of high-power converters employing SCRs operating at several kilovolts and switching several thousands of Amperes is strongly dependent on the triggering circuit and the protecting circuit (snubber) used. In this paper two stand-alone trigger circuit topologies are discussed and test results are given for one of them in particular, built with off-the-shelf components. A standard snubber circuit configuration was used and its ability to protect the SCR was examined by classical analytical methods and by computer simulation. Results of these calculations are reported as well as predictions about the fault tolerance afforded by the snubber design to a high power converter using SCRs.**

Since the components of the SCR protective circuits affect strongly the overall package size of the converter and tend to determine the minimum size and weight achievable, a conceptual design is also presented for a combined snubber/trigger circuit with the potential for reduced size and weight for the whole assembly.

I. INTRODUCTION

THE performance of SCRs used in high power converters is strongly dependent on the circuit used for triggering them. In general, the trigger circuit is specified in terms of the minimum gate drive needed (both open circuit voltage and short circuit current), the length of time in which it must be active, and the maximum time allowed for the drive signal to rise from zero to its specified amplitude. These parameters can often be quite demanding especially in the case of circuits used to trigger SCRs operating at several kilovolts and kiloamperes. Likewise, the designer of circuits used to protect SCRs or other solid state power switches (commonly referred to as "snubber circuits") may be faced with operational conditions severe enough that often the physical size of the protective components dwarfs that of the circuit they are meant to protect. Although it is recognized that advances in solid state technology continuously improve device characteristics, it is still worthwhile considering the extent to which such auxiliary circuits, like gate trigger and snubber circuits, affect the overall system performance, size, and weight. This paper will consider specifically the case of the SCR model SPT402BHTW360 manufactured by Silicon Power Corporation, which is one of the most powerful and demanding SCRs on the market today. It is believed that most of the considerations made herein will be applicable in general to other devices as well.

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II. TRIGGER CIRCUIT

A general treatment of SCR trigger circuits can be found in reference [1] and, in fact, if allowance is made for the subsequent progress in technology, most trigger circuits in use today can be considered variants or adaptations of the ones found in this reference. The trigger circuits with which we experimented are no exception and our focus will be on the specific challenges posed to their realization in our particular application. In our application SCR model SPT402BHTW360 was used in a three-phase regenerative ac-dc converter bridge of standard topology and specified to handle a 10 kV dc bus at 48 kA dc bus current. Because of the voltage and current levels, each leg of the converter consisted of two branches in parallel, with each branch having three SCRs in series. The multiplicity of series and parallel paths and the reliability requirements of the converter further aggravated the already demanding specifications for both the trigger and snubber circuits. The on-off cycle time of the SCRs was in the 500-1,000 Hz range. The desired di/dt capability for each SCR was 1,000 A/μs.

From the SCR specifications we can construct the envelopes of minimum requirements for the gate drive circuit (Figs. 1 and 2, solid lines). Note that the pulse rise-time shown is the maximum allowable in order to maintain the specified di/dt capability of 1000 A/μs for the SCR and, therefore, it is an intrinsic part of the specifications. This insures that the whole cross sectional area of the SCR is turned on at the same time and is available for conduction. It is remarkable, however, that in order to guarantee the 1000 A/μs for the SCR, a minimum current rise-time capability of 400 A/μs is required from the triggering circuits. These stringent requirements on current amplitude and rise-time make it imperative to keep any inductance in the gate current path, either discrete or distributed, to a minimum.

The first gate drive circuit built for our application used a pulse transformer to couple the trigger pulse to the SCR gate (Fig. 3). Whereas this configuration had the advantage of isolating the trigger circuit from the SCR, it was soon realized that it was difficult to manufacture a suitable pulse transformer

with low inductance and sufficient current handling capability without incurring large penalties in size and cost. An alternate approach proved to be preferable and resulted in the circuit shown in Fig. 4. Here the pulse transformer is removed from the gate circuit proper and is used only to initiate the discharge of a storage capacitor via a fast acting IGBT switch in series with the SCR gate. The penalty for this approach is that the gate drive circuit is no longer isolated from the SCR, although the isolation is provided at the pulse transformer and at the power transformer through which the storage capacitor is recharged.

The circuit shown in Fig. 4 was realized in a printed circuit configuration with off-the-shelf components. One gate trigger circuit per SCR was used. Particular care was exercised in keeping circuit reactances at their lowest possible level but no special effort was expended, in this first realization, in optimizing the design with regard to overall trigger circuit size. This would certainly impact the circuit layout and parasitic effects and, therefore, its performance, as is well known [2]. It is recognized, therefore, that opportunities do exist for size and weight reduction of the trigger circuit assemblies. Even as designed and built, however, the circuit met the stringent performance requirements specified, as shown by the experimental gate drive pulses in Figs. 5, 6 and 7.

What has been said above applies to any SCR with specifications comparable to those of the SPT402BHTW360 device used. Other devices are already available that do not need the aggressive triggering of this SCR (e.g. the SPT411 SCR also manufactured by SPCO). The advent of these newer devices should also allow a dramatic reduction in both volume and weight of the triggering circuit.

III. Snubber circuit

The snubber circuit was implemented simply as the series combination of a capacitor and a resistor placed in parallel with the SCR. Its function is to keep the electrical stresses on the power switch within safe levels and to reduce unbalances between the SCRs in series due to differences in response of the devices under transient conditions. Specifically, the snubber limits the voltage level and the rate of voltage change (dv/dt) across the SCR during turn-off and, furthermore, it allows more time for the slower SCRs to recover their voltage standoff capability by providing an alternate path for the reverse recovery current. Likewise, at turn-on, the snubber limits any unbalance between slow turn-on devices and fast turn-on devices. In our case, using the methods discussed in [1], the acceptable range for the snubber capacitor was determined to be between 1.3 and 4.7 μF and that for the snubber resistor to be between 3.2 and 5.7 Ω. These results matched the values respectively of 3.5 μF and 3.5 Ω that were suggested by the supplier of the SCRs and that were eventually used in our circuit.

Both selections of capacitor and resistor present challenges for the designer of the snubber circuit. At issue are the amount of voltage overshoot that can be tolerated across the SCR, the distribution of losses between the switch and the snubber circuit, and the allowable dv/dt and di/dt for the SCR and capacitor. One finds very quickly that the physical size of the capacitor tends to dwarf that of all the other components, thus dominating the issue of optimization of size and weight of the assembly. Size, of course, affects directly the issue of the unavoidable parasitic reactances that further complicate the design process. Applying the analytical model described in [3] to our case, the snubber we used would lead to an over-damped voltage response across the SCR with calculated voltage overshoot and dv/dt across the SCR of 112 V and 2200 V/μs respectively, as shown in Figs. 8 and 9. Thus we can say that, within the limits of the approximations of the analytical solution, the snubber is expected to be very effective in containing the voltage overshoot, but not the dv/dt, within the specifications of the SCR. A computer simulation performed on the whole supply-converter-load system with the commercially available software SABER results in a larger value (~1,000 V) for the voltage overshoot, but still keeps the total voltage within the device specifications. On the other hand the SABER simulation predicts a dv/dt smaller by an order of magnitude (~200 V/μs) than the one calculated analytically, which is well within the SCR specifications. Considering that the analytical solution relied on a simplified model of an isolated SCR in order to obtain results in a closed form, it seems reasonable to give more weight to the more comprehensive SABER simulation and conclude that the values used for the snubber capacitor and resistor are expected to be adequate for protecting the SCR. Additionally, the SABER simulation demonstrated the robustness of the converter design by showing that the failure for any reason of any single SCR module (SCR with trigger and snubber circuits) in the three SCR series combination in each leg of the converter did not impair the overall operation of the system. In fact, in the simulation, the system performed within the specifications even after the failure of one SCR module. This will have to be verified in actual tests. The design of the converter was meant to have this degree of redundancy, fully recognizing that two SCR series combinations would be sufficient instead of three. The limiting action of the snubber circuits is crucial in affording this level of robustness. Unless new devices with higher performance capability are used, any further optimization of the system will probably require a compromise between size and weight on one hand and reliability and fault tolerance on the other.

IV. Integrated snubber-trigger

Both snubber circuits and trigger circuits discussed above were built with off-the-shelf components and are shown in Figures 10 and 11. Obviously, they could be reduced in size and weight if special components were used. Another alternative exists, however, and is described briefly below.

In an effort to minimize the size and weight of the entire converter, a circuit combining both functions of the trigger and

snubber circuits was developed, built and tested [4]. Fig. 12 shows the conceptual design. When the SCR is in the forward blocking mode, the snubber capacitor charges through the charging resistor R_c to a voltage limited by the Zener diode D_z. This voltage is then used to trigger the SCR gate at the desired time via the IGBT switch. Upon turn-off, when the voltage across the SCR changes polarity, the snubber works in the normal fashion via diode D_s. In this circuit, the snubber capacitor also provides the trigger pulse for the SCR gate. This circuit has the potential of minimizing the overall size and weight of the snubber-trigger combination even if three additional diodes (one of them a Zener) and a resistor are required over the simple RC snubber circuit. Some variations of this concept are possible and have to be investigated as to their benefits and effectiveness.

V. Conclusions

In this paper, results are given for the design of a trigger circuit and a snubber circuit used in connection with a specific high power SCR. Two stand-alone trigger circuit topologies and their electrical performance and potential for miniaturization are discussed. Experimental results are included for the case of a specific trigger circuit design. The selection of snubber components is also discussed, again with consideration given to size and weight optimization. The analysis then continues with the presentation of an integrated snubber/trigger circuit topology with potential for reduced part count, size, and weight.

VI. Acknowledgement

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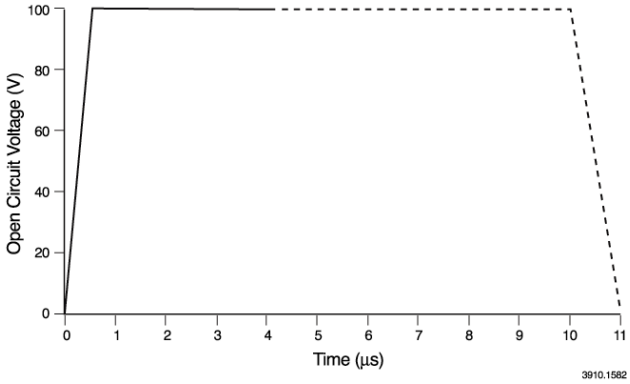

Fig. 1. Gate drive open circuit voltage requirements

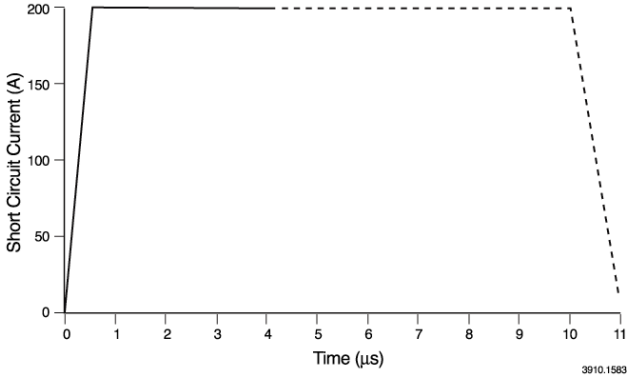

Fig. 2. Gate drive short circuit current requirements

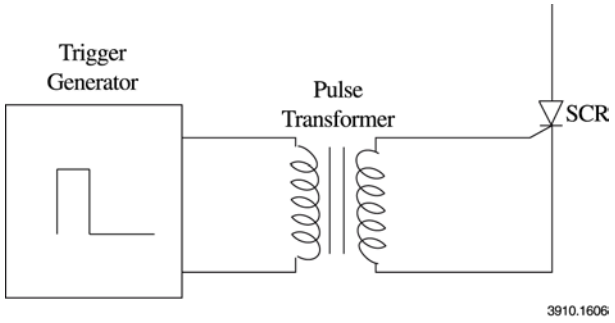

Fig. 3. Pulse transformer coupled trigger circuit

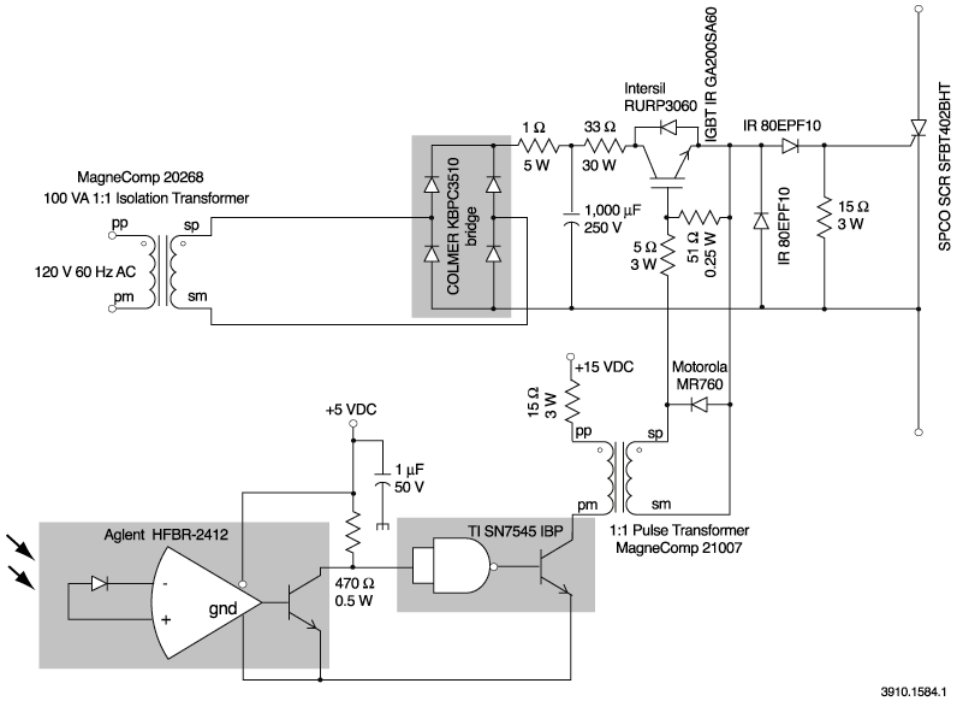

Fig. 4. Gate trigger circuit (black arrows indicate optical signal input)

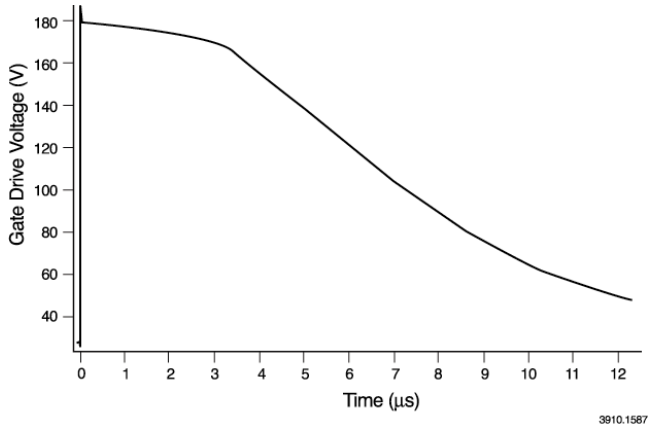

Fig. 5. Open circuit output voltage of trigger circuit

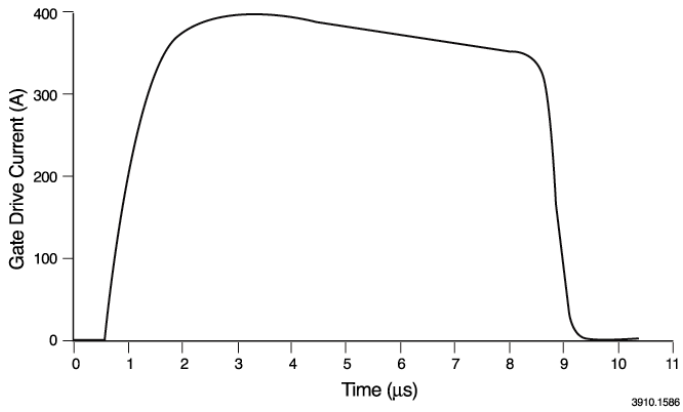

Fig. 6. Short circuit output current of trigger circuit

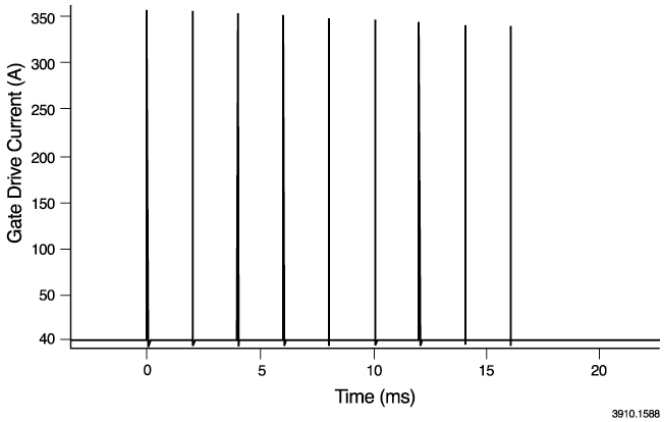

Fig. 7. Current output of trigger circuit loaded by SCR gate in a repetitive mode

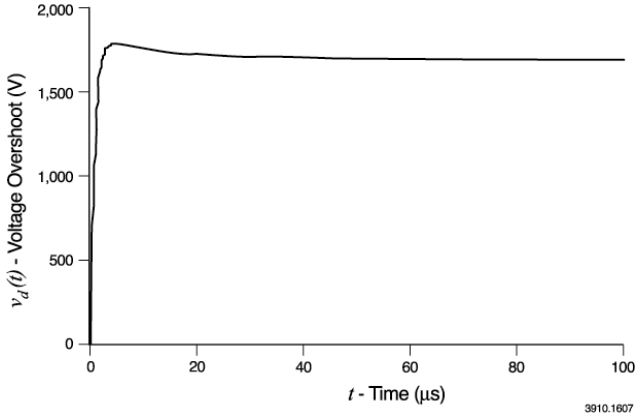

Fig. 8. Calculated voltage overshoot across the SCR during turn-off (steady state value is 1,667V)

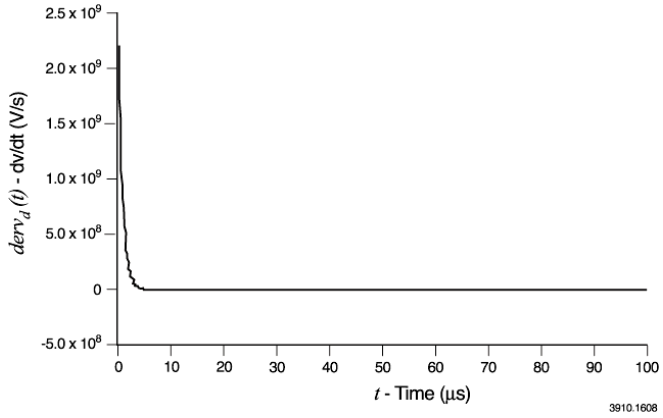

Fig. 9. Calculated dv/dt across SCR during turn-off

Fig. 10: Snubber for one SCR with DC equalizer circuit branch

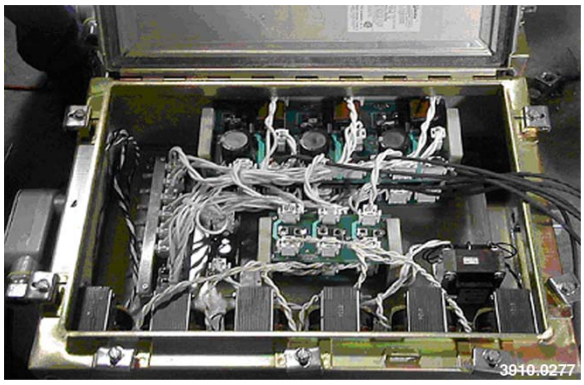

Fig. 11: Shielded box with supply and trigger circuitry for six SCRs (one leg of converter); box outside dimensions are 16x20x7 in.

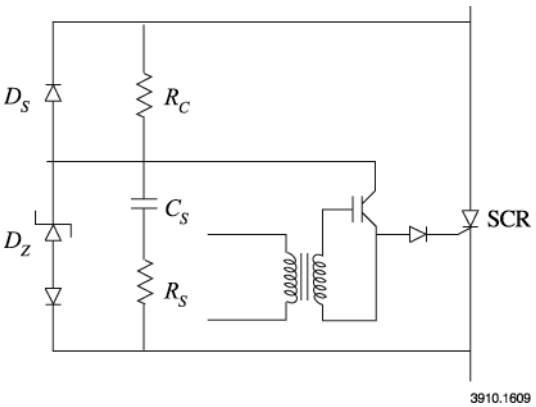

Fig. 12. Conceptual design of a combined snubber/trigger circuit