The Dissertation Committee for Arindam Sanyal
certifies that this is the approved version of the following dissertation:

Digital Enhancement Techniques For Data Converters In Scaled CMOS Technologies

Committee:

Nan Sun, Supervisor

T. R. Viswanathan

Michael Orshansky

Neal Hall

Shouli Yan

Digital Enhancement Techniques For Data Converters In Scaled CMOS Technologies

by

Arindam Sanyal, B.E.; M.Tech.

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Dedicated to my parents and my wife.

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Digital Enhancement Techniques For Data Converters In Scaled CMOS Technologies

Arindam Sanyal, Ph.D.
The University of Texas at Austin, 2015

Supervisor: Nan Sun

This thesis presents digital enhancement techniques for data converters in advanced technology nodes. With technology scaling, traditional voltage-domain (VD) analog-to-digital converters (ADCs) face two major challenges: (1) reduction of dynamic range due to supply voltage scaling, and (2) decrease in intrinsic gain of transistors which makes high gain amplifier design tough. To address these challenges, a two-stage ADC architecture is presented which uses time-domain quantization to exploit the advantages of technology scaling. The architecture, consisting of a first stage successive approximation register (SAR) and a second stage ring oscillator, is highly digital and scaling friendly. Two prototypes have been developed to validate the proposed architecture. The 40nm CMOS prototype achieves 75.7 dB dynamic range at an excellent Schreier figure-of-merit of 172.2 dB. The proposed architecture has been extended to a capacitance-to-digital converter and a prototype has been developed in 40nm CMOS. The prototype can sense capacitances with a

resolution of 1.3fF and has a Walden figure-of-merit of 60 fJ/step which is more than two times better than the current state-of-the-art.

This thesis also presents digital techniques to improve performance of continuous-time(CT), delta-sigma ($\Delta\Sigma$) digital-to-analog converters (DACs). Recently, CT $\Delta\Sigma$ DACs have received more attention than their discrete, switched-capacitor counterpart mainly because of low power and/or higher speed of operation. However, a critical disadvantage of CT, $\Delta\Sigma$ DACs is their greatly increased sensitivity to inter-symbol interference (ISI) error. To address this shortcoming of CT DACs, this thesis presents several algorithms that can mitigate ISI error simultaneously with static mismatch error. Further, the proposed algorithms are fully digital in nature and as such, are best poised to take maximum advantage of technology scaling. Thus, the techniques presented in this thesis will be important enabling factors in raising the envelope of performance of CT $\Delta\Sigma$ DACs in advanced technology nodes.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation

Moore's law has been driving semiconductor industry growth for several decades. It has resulted in ever shrinking technology nodes and the increased ability to fit billions of transistors in a chip. The advancement in technology nodes has been propelled in turn by the demand for higher performance. As a result, the transistors have become smaller and faster while consuming less power. This in turn has given a great boost to digital design, making complex digital designs cheaper to implement both in terms of design effort and cost.

However, the physical world round us is still analog and interfaces are required between the analog and digital domains. While technology scaling has greatly benefited digital design, it has made analog design more challenging. With technology scaling, intrinsic transistor gain has reduced and so has the dynamic range of signals. This poses a great challenge for traditional analog blocks which depend on high gain and large voltage headroom. Thus, a natural tendency has been to shift towards digitally-assisted analog design. The aim of digitally-assisted analog design is to design low performance analog blocks in advanced technologies and then correct for the deficiencies through digital algorithms.

The motivation behind this thesis is to enhance the performance of data converters in advanced CMOS processes by using digital enhancement techniques. Data converters are an integral block in every electronic system that needs to interact with the outside world, be it cellphones or computers or sensors. Traditional analog-to-digital converters (ADCs) are dependent on high performance analog blocks which are challenging to design in advanced CMOS technologies. An alternative highly digital ADC architecture is presented in this thesis. The proposed ADC quantizes the input signal in time domain rather than the traditional voltage domain. The rationale behind adopting time domain quantization is that the quantization step is essentially dictated by gate delay which improves with technology scaling. Further, the constraint of voltage headroom is no longer applicable to time domain quantizers. Thus, time domain quantization is very suitable for advanced technologies. However, time domain quantization comes with its own challenges. The fundamental obstacle to time domain quantization is the non-linear voltage-to-time domain transformation that precedes the quantizer. In this thesis, a highly digital ADC architecture is presented which overcomes the nonlinearity associated with voltage-to-time transformation and achieves 12-bit resolution at high energy efficiency. Two prototypes have been designed in 180nm CMOS and 40nm CMOS technologies and measured in the lab. The performance of the prototypes serve as an important validation of the proposed ADC architecture.

Another area where time domain quantization can be made use of is in sensor applications. Capacitance to digital converters (CDCs) are widely used to sense proximity, position, humidity. They are also used in biomedical implants. Thus,

it is highly desirable to have a high energy efficiency CDC wth good resolution. It turns out that time domain quantization can be applied to CDCs to maximally leverage the benefits of technology scaling. The proposed time-domain ADC architecture is extended to design a CDC in 40nm CMOS. The prototype has been measured and it improves the energy efficiency by more than two times compared to the state-of-the-art.

In recent times there has been a shift from continuous-time (CT) $\Delta\Sigma$ modulators to discrete-time (DT) $\Delta\Sigma$ modulators. This is because CT $\Delta\Sigma$ modulators allow higher speed of operation and/or consume less energy than their DT counterparts. However, CT operation leads to a much increased sensitivity to jitter and inter-symbol interference (ISI) error. Jitter sensitivity can be reduced by using multi-bit digital-to-analog converter (DAC). Use of multi-bit DAC results in static mismatch error. There are dynamic element matching (DEM) algorithms which can address the static mismatch error in DACs. However, the conventional DEM algorithms are optimized for DT $\Delta\Sigma$ modulators and fail to address ISI error in CT $\Delta\Sigma$ modulators. In fact, the conventional DEM algorithms can actually exacerbate ISI error. ISI error can be addressed in an analog fashion by adopting the return-to-zero (RZ) switching at the cost of increased jitter sensitivity of the modulator and greater linearity requirement of the output filter. Fully digital techniques are proposed in this thesis to simultaneously address both static mismatch and ISI errors. The proposed techniques, being digital, can take full advantage of technology scaling by achieving high speeds while consuming low power and area, and are important enabling factors to enhance the performance of CT $\Delta\Sigma$ modulators.

1.2 Organization

Chapter 2 of the thesis presents the proposed time domain quantization ADC architecture. It also includes the measurement results of two prototypes designed in 180nm and 40nm CMOS technologies. Chapter 3 extends the architecture presented in Chapter 2 to the design of a capacitance-to-digital converter. The measurement results for a prototype designed in 40nm CMOS technology are also discussed. Chapter 4 presents digital techniques for addressing static mismatch and ISI error in CT $\Delta\Sigma$ modulators. Simulation results are also presented to verify the proposed techniques.

Chapter 2

Hybrid SAR-VCO $\triangle\Sigma$ ADC

2.1 Introduction

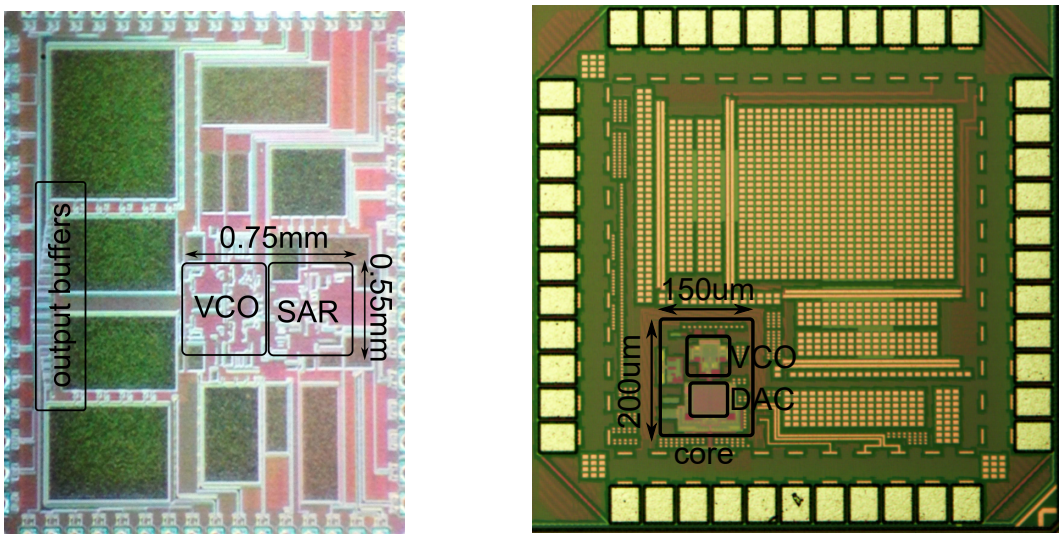
This chapter[1]presents our time-domain two-stage ADC architecture. Two prototypes have been developed, the first in 180nm CMOS and the second in 40nm CMOS. The die photographs are shown in Fig. 2.1.

This chapter is organized as follows: first a review of existing time-domain ADCs is presented. The proposed ADC architecture is introduced next, followed by a detailed discussion on prototype–I design in 180nm and its measurement. Finally, design of prototype–II in 40nm CMOS is presented, along with measurement results and comparison with existing state-of-the-art.

2.2 Review of existing time-domain ADCs

With technology scaling, traditional voltage domain design of data converters face several challenges. The dynamic range of the ADC is reduced as the supply voltage is scaled with technology. In addition, most voltage domain data convert-

[1]This chapter is a partial reprint of the publication: Arindam Sanyal, Kareem Ragab, Long Chen, T. R. Viswanathan, Shouli Yan and Nan Sun, "A hybrid SAR-VCO $\Delta\Sigma$ ADC with first-order noise shaping", *IEEE CICC* , pp. 1–4, 2014. I thank all the co-authors for their valuable advice in designing and testing of the prototypes.



(a) (b)

Figure 2.1: Die photograph of (a) 180nm prototype–I (b) 40nm prototype–II

ers use high gain operational transconductance amplifiers (OTAs). With technology scaling, the intrinsic gain of transistor is reduced, thus making the design of high gain OTAs very challenging.

To address these challenges, data converters operating in time domain have been proposed [Taylor and Galton [2010]; Straayer and Perrott [2008]; Hamilton et al. [2012]; Reddy et al. [2012]; Gupta et al. [2011]; Rao et al. [2011]]. The most popular technique is to use a ring voltage-controlled oscillator (VCO) to perform a voltage-to-time conversion. Time domain quantization is performed by simply reading the phase/frequency information from the VCO by simple digital logic cells. Thus, the overall ADC becomes highly digital which is very suitable for advanced technologies. Furthermore, with technology scaling, gate delay is reduced.

Reduction in gate delay results in finer quantization step, and hence, increased resolution for VCO-based ADCs. However, VCO-based ADCs suffer from inherent non-linearity which limits the ADC dynamic range.

Multiple approaches have been proposed to address this issue. The work in [Taylor and Galton [2010]] uses a complicated digital calibration engine to reduce VCO nonlinearity. However, for the technique to work, an accurate replica matching is required. Moreover, the input-swing is still limited to reduce higher-order distortion. Another approach is to put the VCO inside a closed loop with a high gain before the VCO [Straayer and Perrott [2008]]. The distortion of the VCO is reduced by the gain block. A two-stage ADC with a VCO-based second stage is put inside a high gain loop in [Rao et al. [2011]]. The gain block/loop filter is implemented through an OTA. However, this approach still shares the challenge faced by traditional voltage domain ADC design, namely, the need for a high gain OTA which is difficult to design in advanced technology nodes, in addition to being power hungry.

A third approach has been to linearize the VCO in an open-loop configuration without digital calibration. A high linearity delay cell design has been used to address the non-linearity issue in [Hamilton et al. [2012]]. The approach in [Reddy et al. [2012]] has been to convert the analog input to a two-level signal by using a naturally sampled pulse width modulator and switching the VCO between two frequencies. By switching the VCO between only two points on its tuning curve, the non-linearity problem is eliminated. However, [Reddy et al. [2012]] still uses OTAs to implement the pulse width modulator. Yet another approach is to use a two-stage

ADC with a VCO-based second stage as in [Gupta et al. [2011]], where a 5-bit flash ADC has been used as the first stage to reduce the swing of the second-stage. However, it still requires an OTA for residue amplification.

2.3 Proposed two-stage architecture

In this work, we propose a novel two-stage architecture which combines a SAR ADC with a VCO. The SAR ADC has a highly digital structure and has a very good energy efficiency at medium resolutions (< 10 bits). On the other hand, VCO based ADC is very good at integrating small input swings at time domain. The proposed ADC does not make any use of any OTAs which makes it very amenable to technology scaling.

The SAR ADC is used to perform a coarse quantization of the input signal. The residue which is available at the comparator input after the SAR conversion, is fed directly to the VCO through switches without requiring any OTAs for residue amplification. The VCO integrates the residue in phase domain, and the VCO's output is differentiated digitally to form the second stage output. Combining SAR with VCO brings several key benefits:

1. the non-linearity of the VCO is greatly relaxed as it only sees a small signal swing.

2. the design of the SAR stage is relaxed too as any decision error due to incomplete settling or quantization noise is absorbed by the VCO provided it is not overloaded.

3. phase domain integration by the VCO is used to shape the quantization noise to first-order, thus allowing increase in resolution by trading off sampling speed.

The block-level model of the proposed ADC is shown in Fig. 4.3. In the model, q_1 represents the quantization error of the first stage, δ represents the error due to capacitor mismatches, V_{os} represents the input-referred offset of the comparator, and q_2 represents the quantization error of the VCO stage. The effect of non-zero comparator input capacitance C_{in} and parasitic capacitance C_{par} is captured by the term $G \equiv C_{tot}/\left(C_{tot} + C_{par} + C_{in}\right)$ where C_{tot} is the total capacitance of the DAC. The input swing of the comparator is scaled by the factor G.

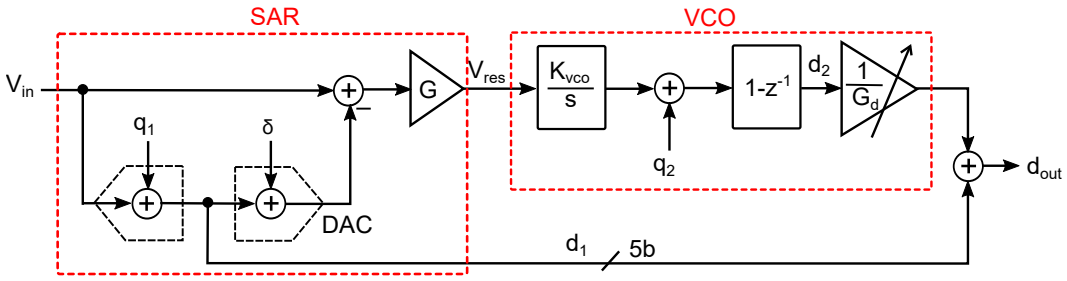


Figure 2.2: Model of the proposed ADC.

The overall ADC output is given by

$$d_{out} = V_{in} + \left(1 - \frac{GK_{vco}}{G_d}\right) q_1 - \delta \frac{GK_{vco}}{G_d} + \frac{(1-z^{-1})q_2}{G_d} \tag{2.1}$$

where G_d is the digital interstage gain factor.

It can be seen from (2.1) that the quantization error from the first-stage will not show up in the overall output if $G_d = GK_{vco}$, i.e, if the digital interstage gain G_d

matches the analog interstage gain GK_{vco}. The only quantization noise in the overall output is the quantization noise of the second stage which is first-order shaped. Thus the proposed ADC can also be viewed as a 0-1 MASH $\Delta\Sigma$ ADC. To ensure linearity, it is important to calibrate DAC capacitor mismatch δ.

2.4 Prototype ADC–I

A prototype implementing the proposed SAR-VCO architecture was designed in 180nm CMOS process.The following subsections provide detailed description of the prototype.

2.4.1 Detailed circuit schematics

The proposed ADC and its timing diagram is shown in Fig. 2.3. The first-stage is a 5-bit SAR which performs a coarse quantization of the input signal. Once the SAR finishes comparison, the conversion residue is available at the comparator input. Since the VCO can do fine quantization for small signals in the time domain, the residue is directly transferred to the VCO without the need of any OTA-based residue amplification. The absence of OTA makes the design more scaling friendly and reduces the ADC power consumption. The clocks required for the 3 phases (ϕ_1, ϕ_2, ϕ_3) are generated synchronously from a master clock. 3 cycles of the master clock are used for sampling the input and 5 cycles of the master clock are allotted for SAR and VCO operation each.

The VCO consists of a source-degenerated V/I converter and two 7-stage, differential current-controlled oscillators (CCOs) as shown in Fig. 2.4. The V/I

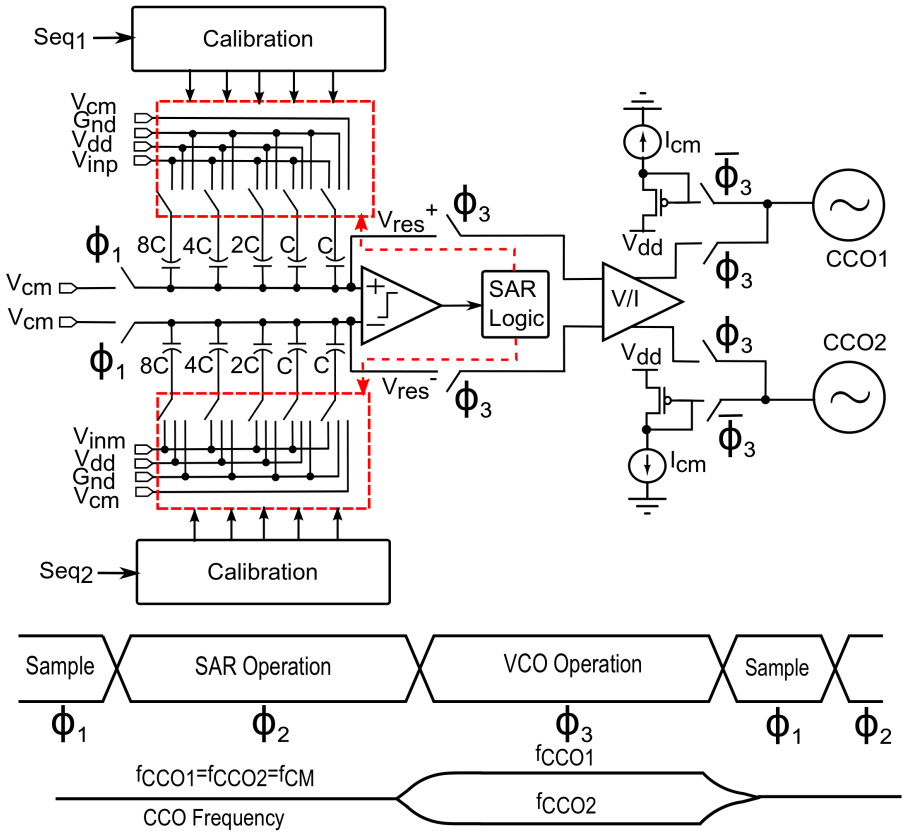


Figure 2.3: Proposed hybrid $\Delta\Sigma$ ADC architecture.

converter has a simulated linearity of 9-bit. The delay cells use weak cross-coupled inverters and are buffered before they are sampled by comparator-based flip-flops. The buffers isolate the delay cells from the kickback noise of the comparators. The use of two CCOs cancel out any major second-order distortion. The CCO phase is obtained by sampling the outputs of all 7 stages and subsequently encoding them to produce a 4 bit output. A 6-bit counter is used to record how many times the phase overflows over one sampling period [Daniels et al. [2010]]. The final CCO output is the counter output plus 14 times the phase encoder output.

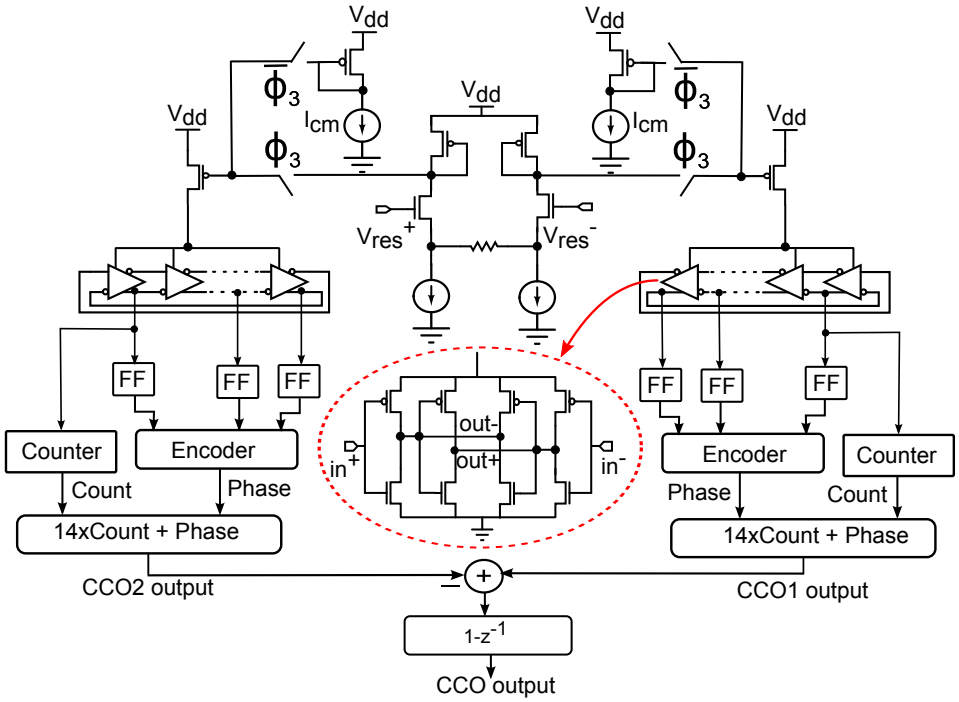


Figure 2.4: VCO schematic.

The number of bits available from the VCO stage is given by

$$n_{vco} = \log_2 \left(2N_{stage} \cdot K_{vco} \Delta v_{in} T_{vco}\right) \tag{2.2}$$

where N_{stage} is the number of VCO stages, K_{vco} is the VCO gain in Hz/V, Δv_{in} is the VCO input swing and T_{vco} is the time-period over which the VCO acts as an integrator (ϕ_3 in Fig. 2.3). The VCO linearity requirement is relaxed as the VCO input swing is reduced by 32 by the 5-bit SAR front-end. The use of a counter to keep a record of the phase overflow increases the VCO dynamic range by a factor of 2^M, where M is the number of bits in the counter. This effectively decouples the ADC sampling frequency from both the VCO tuning gain and the VCO center frequency and allows variable ADC sampling rates. For a 6-bit counter, the mini-

mum ADC sampling rate is given by $f_s \geq (5/13)\,(K_{vco}\Delta v_{in}/2^6) \approx 1$ MHz, where the factor (5/13) comes from the fact that the VCO integrates for 5 cycles out of 13 (phase ϕ_3). Reducing the sampling rate allows the VCO to integrate for a longer time and thus more bits can be obtained from the second stage which improves the SQNR of the ADC. Thus, the proposed ADC can have a higher resolution by reducing the sampling rate. This is in contrast to typical $\Delta\Sigma$ converters where reducing the sampling rate does not increase the resolution.

To reduce the VCO phase noise, the delay cells use only a PMOS tail current source as shown in Fig. 2.4. This is because the $1/f$ noise corner for PMOS is much lower than NMOS in 180 nm technology. During the ADC sampling operation (ϕ_1) and SAR operation (ϕ_2) (see Fig. 2.3), the CCOs are not reset but switched to the same fixed current source; the counter is also kept running. Thus, the VCO is used as a phase integrator and the first-order noise shaping capability is retained.

The VCO stage uses switched current sources rather than switched voltage buffers. Switching between voltage sources require very large switches with very low resistance, thus incurring a large power penalty. By switching between current sources rather than voltage sources, power can be saved by using smaller switches.

To remove the capacitor mismatches in the DAC, a digital calibration technique similar to [Lee et al. [1984]] is employed. A calibration block (see Fig. 2.3) configures the SAR capacitor array and uses the VCO to measure capacitor mismatches and GK_{vco}. Then G_d is adjusted to match the extracted GK_{vco} and δ is compensated via a digital adder.

The SAR used in the proposed technique adopts the novel low-power switching technique of [Sanyal and Sun [2014a]] in which only one-side of the differential DAC array needs to be switched every cycle. The proposed technique is compared with the conventional switching technique in Fig. 2.5 with a 2-bit example. Switching the LSB capacitor between $(0, V_{cm})$ instead of $(0, V_{dd})$ allows the proposed technique to generate a zero-mean residue for the 2-bit ADC with only 4C capacitance. If a zero-mean residue is not required, the proposed technique can give 3-bit resolution with the same 4C capacitance [Sanyal and Sun [2014a]]. In contrast, a 2-bit conventional SAR requires 8C capacitance for nonzero-mean residue and 16C capacitance if a zero-mean residue is required which is more desirable for a two-stage architecture due to lower swing at second-stage input. Thus, the proposed switching technique achieves 4X capacitance reduction compared to the conventional technique and this holds true for an ADC with any resolution. For a 5-bit SAR, the simulated saving in switching energy of the proposed technique is 86% when compared to the conventional SAR.

It should be noted here that any error in the value of V_{cm} has the same effect as mismatch in the LSB capacitor and can be calibrated. Bottom-plate switching is used to ensure linearity of the ADC. The SAR ADC uses a strong-arm latch based comparator without any pre-amplifier. The simulated 3σ offset of the comparator is 15 mV.

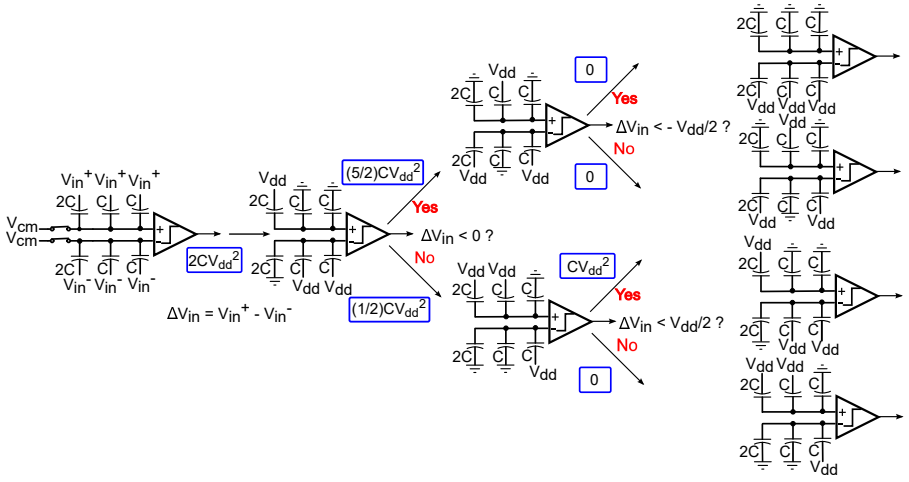


Figure 2.5: Switching technique for 2-bit (a) conventional SAR, and (b) proposed SAR ADC.

2.4.2 Capacitor mismatch calibration

A simple foreground technique can be used to extract the capacitor mismatches in the DAC. In presence of mismatches in the DAC, each capacitor in the array can be written as the sum of the ideal capacitor value plus an error term due to mismatch, i.e., $C_i^{'} = C_i + \Delta C_i, i \in [0, N]$. By definition, $\sum_{i=0}^{N} \Delta C_i, i = 0$. The voltage error term contributed by the mismatch in i-th capacitor in the DAC, is given by

$$V_{\epsilon,i} = \Delta C_i V_{ref} / C_{DAC} \tag{2.3}$$

where $V_{ref} = V_{refp} - V_{refn}$, $C_{DAC} = \sum_{i=0}^{N} C_i^{'}$.

The error due to capacitor mismatches can be written as

$$\delta \;\; = \;\; \sum_{i=0}^{N} V_{\epsilon,i} D_i \tag{2.4}$$

where D_i controls the voltage that C_i is connected to at the end of the i-th comparison cycle and $D_i \in [-1, 0, 1]$. The first stage output, d_1, can then be written as $d_1 = \sum_{i=1}^{N} 2^{i-1} D_i + D_0$.

The total error contributed by mismatches in all the capacitors to the final output, would then be given by

$$\delta K_{vco} G \;\; = \;\; \sum_{i=1}^{N} \left(V_{\epsilon,i} K_{vco} G \right) D_i \equiv \sum_{i=1}^{N} \Delta_{\epsilon,i} D_i \tag{2.5}$$

In order to know $\delta K_{vco} G$ the key is to extract $\Delta_{\epsilon,i}$. To this end, different sequences are used to compare each capacitor in the array with the ones following

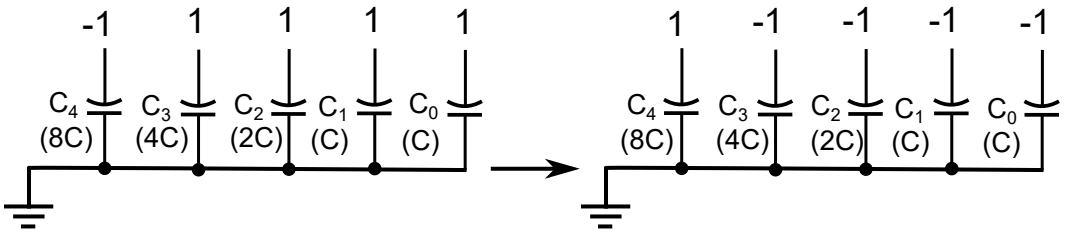


Figure 2.6: Calibration of mismatch in C_4.

it, to get an estimate of its deviation from the ideal value. As an example let us take the case of MSB capacitor, C_4, in the DAC array shown in Fig. 2.6.

A sequence of $\{$-1 1 1 1 1$\}$ is sampled onto the capacitor array. Next the charge is redistributed by forcing a sequence $\{$1 -1 -1 -1 -1$\}$ onto the capacitor bottom plates. Using charge conservation, the voltage at the bottom-plate of the DAC array, after charge redistribution, is given by

$$V_x = 2(C_4^{'} - C_3^{'} - C_2^{'} - C_1^{'} - C_0^{'})/C_{DAC} = 2V_{\epsilon,4} \tag{2.6}$$

The output of the second stage, after a full conversion cycle, is then given by $d_{2,4} = 2\Delta_{\epsilon,4}$. Thus, a measure of mismatch in C_4 is given by $d_{2,4}/2$. To extract the mismatch in C_3, a sequence of $\{$0 -1 1 1 1$\}$ is sampled on the capacitor array. Next a sequence of $\{$0 1 -1 -1 -1$\}$ is forced onto the capacitor bottom plates as shown in Fig . 2.7.

Using charge conservation, the bottom-plate DAC voltage after charge redistribution is given by

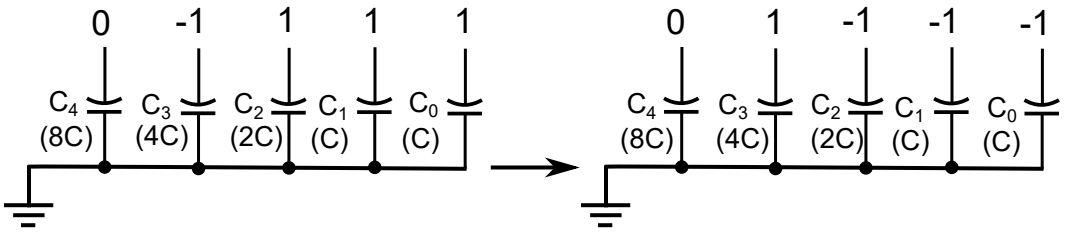


Figure 2.7: Calibration of mismatch in C_3.

$$V_x = 2(C_3' - C_2' - C_1' - C_0')/C_{DAC} = 2V_{\epsilon,3} + V_{\epsilon,4} \tag{2.7}$$

The corresponding second stage output is then given by

$$\begin{aligned} d_{2,3} &= \Delta_{\epsilon,4} + 2\Delta_{\epsilon,3} \\ \implies \Delta_{\epsilon,3} &= \frac{1}{2}\left(d_{2,3} - \Delta_{\epsilon,4}\right) \end{aligned} \tag{2.8}$$

In general, a measure of the voltage error contribution due to mismatch in the i-th capacitor is given by

$$\Delta_{\epsilon,i} = \begin{cases} d_{2,i}/2 & i = N \\ \frac{1}{2}\left(d_{2,i} - \sum_{j=i+1}^{N} \Delta_{\epsilon,j}\right) & i \in [1, N-1] \end{cases}$$

Due to the Δ-Σ action of the VCO stage, the values of $d_{2,i}$ can be obtained with great precision if averaged over many cycles.

2.4.3 Interstage gain calibration

Once $\delta K_{vco} G$ is known, and the capacitor mismatch term in (2.1) can be removed, the only remaining error that has to be cancelled is the interstage gain

mismatch. To that end, $K_{vco}G$ has to be evaluated and G_d set to that value. For evaluating K_{vco}, two different values of d_1 are needed. We choose the sequences $\{0\ 0\ 0\ 0\ 0\}$ and $\{0\ 0\ 0\ 1\ 0\}$ for that purpose. The reason behind choosing these sequences is to keep the VCO's input swing to be small so as not to introduce non-linearities in d_2. Once again, the sequence $\{0\ 0\ 0\ 0\ 0\}$ is first sampled onto the DAC, and then the charge is redistributed by forcing the sequence $\{0\ 0\ 0\ 1\ 0\}$ on the capacitor bottom plates. The output of the second stage can then be written as

$$\begin{aligned} d_2^* &= K_{vco}GV_{ref}/32 + \Delta_{\epsilon,1}/2 \\ \implies K_{vco}G &= \frac{32}{V_{ref}}\left(d_2^* - \frac{\Delta_{\epsilon,1}}{2}\right) \equiv G_d \end{aligned} \tag{2.9}$$

2.4.4 Noise analysis

The sampling noise is given by $\sqrt{2kT/C_{tot}} = 226\mu V_{rms}$. The input-referred thermal noise of the VCO is given by

$$\overline{v_{vco,in}} = \sqrt{2}\left(\frac{\sqrt{2D_1\left(T_s - T_{vco}\right) + 2D_2T_{vco}}}{2\pi K_{vco}T_{vco}}\right)\cdot\frac{1}{G}$$

where D_1 is the phase diffusion constant [Ham and Hajimiri [2003]] of the VCO during ϕ_1 and ϕ_2 phases, and, D_2 is the phase diffusion constant of the VCO when it is integrating (ϕ_3 phase).

The phase diffusion constant D is evaluated from the value of phase noise $\mathcal{L}(\Delta\omega)$ at an offset of $\Delta\omega$ as $D = \{\mathcal{L}(\Delta\omega)\cdot(\Delta\omega)^2\}/2$. $\mathcal{L}(\Delta\omega)$ at 1 MHz offset during ϕ_1 and ϕ_2 phases is -73.6 dBc/Hz and $\mathcal{L}(\Delta\omega)$ at 1 MHz offset during ϕ_3

phase is -69.2 dBc/Hz. For T_s = 28.6 ns, T_{vco} = 11 ns, K_{vco} = 3.6 GHz/V, and G = 0.8, the input-referred VCO noise, $\overline{v_{vco,in}}$ can be calculated to be $203\mu V_{rms}$.

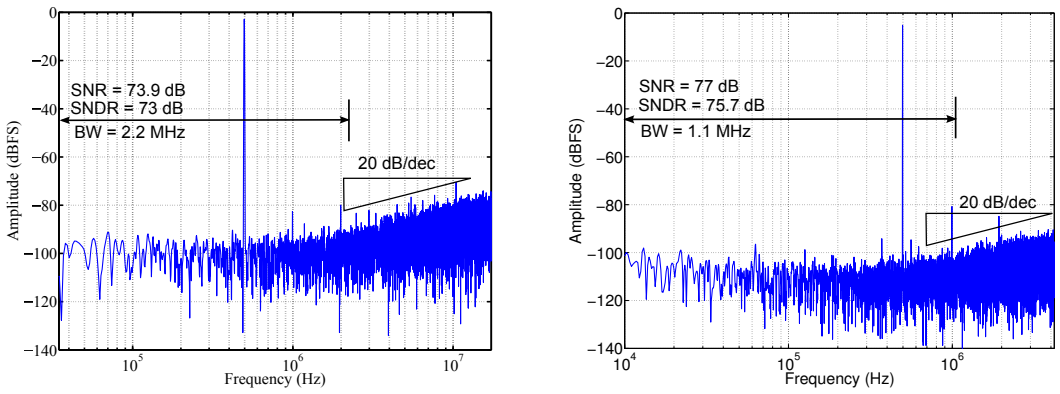
The input-referred thermal noise of the V/I stage for this design is $283\mu V_{rms}$. Thus, the overall input-referred thermal noise is $414\mu V_{rms}$. For an OSR of 8, the in-band input-referred thermal noise is $146\mu V_{rms}$. Thus, for an input swing of $3.2V_{p-p}$, the thermal noise limited SNR is 77.7 dB.

In order to calculate the quantization noise of the ADC, we need to calculate the number of bits available from both the stages. The first-stage has 5 bits, and the number of bits available from the VCO stage, n_{vco}, is given by $\log_2\left(2N_{stage} \cdot K_{vco}\Delta v_{in}T_{vco}\right) = 4.6$. For an OSR of 8, the SQNR is given by $\{6(5+4.6)+1.76+30\log_{10}(8)-5.2\} = 81.2$ dB. Thus, the overall SNR is 75.6 dB.

2.4.5 Measurement Results for Prototype ADC–I

A prototype ADC was designed in 180nm CMOS process. Fig. 2.8 shows the spectrum of the measured output for two different sampling frequencies of 35 MHz and 8.4 MHz respectively. The input frequency is 497 kHz and the input swing is $3.2V_{p-p}$. The first-order noise shaping can be clearly seen at both the sampling frequencies. The SNDR is 73 dB with an input bandwidth of 2.2 MHz and OSR of 8. The SNDR is 75.7 dB at an OSR of 4 if the sampling frequency is lowered to 8.4 MHz. The CCO center frequency is 487 MHz. The ADC sampling rate is variable. As long as the sampling rate is greater than 1 MHz, there is no phase overflow issue.

The measured SNDR versus amplitude is shown in Fig. 2.9. The departure between the two curves start when the SAR ADC outputs start changing. It can be



(a) (b)

Figure 2.8: 32768-pt windowed FFT of the measured ADC output for (a) f_s = 35 MHz and (b) f_s = 8.4 MHz with $V_{in} = 3.2V_{p-p}$ and f_{in} = 497 KHz.

seen from Fig. 2.9 that digital calibration improves the SNDR by about 13 dB.

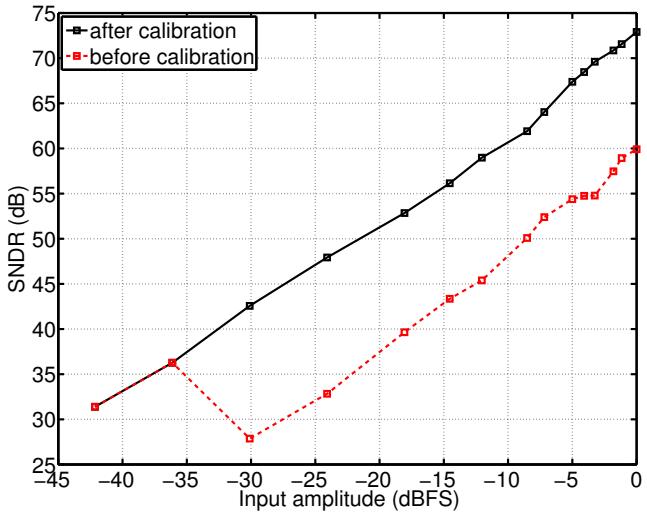


Figure 2.9: Measured SNDR vs input amplitude.

The prototype consumes 5 mW from a 1.8V supply. The V/I consumes 0.3 mW, while the remaining 4.7 mW goes to the SAR, CCO and counter which are

Table 2.1: Comparison with prior art.

	[Taylor and Galton [2010]]	[Straayer and Perrott [2008]]	[Hamilton et al. [2012]]	[Reddy et al. [2012]]	**This work**		
Process(nm)	65	130	180	90	**180**		
Area(mm^2)	0.07	0.42	–	0.1	**0.4**		
F_s(MHz)	500	950	128	640	**35**	**35**	**8.4**
BW(MHz)	3.9	10	2	8	**3.5**	**2.2**	**1.1**
OSR	64	47.5	32	40	**5**	**8**	**4**
SNDR(dB)	71	72.4	63.5	59.1	**70**	**73**	**75.7**
Power(mW)	8	40	6	4.3	**5**	**5**	**4.1**
FoM(fJ/step)	344	587	1243	366	**272**	**303**	**382**

mostly digital and whose power is limited by the 180 nm technology.

A comparison of this work with previously reported state-of-the-art VCO-based ADCs with similar resolution and similar bandwidth is summarized in Table 2.1. It can be seen that the proposed ADC has achieved competitive performance. The power-efficiency can be improved dramatically in an advanced technology as the current prototype's power consumption comes almost entirely from digital blocks.

2.5 Prototype ADC–II

While the first prototype ADC adequately validates the proposed architecture, its FoM is still not among the best as reported in the literature. Also, the interstage gain variation can only be calibrated in foreground which is an impediment considering that the VCO gain varies across process, voltage and temperature. To address these issues, a second prototype was designed in 40nm CMOS.

In prototype–I, the VCO counter consumed about 40% of the total power. To reduce power in prototype–II, the counter was removed. The removal of the counter reduced the dynamic range of the VCO. This loss was compensated by increasing the resolution of the first stage SAR from 5bits to 8bits. The increase in the SAR resolution allows the VCO to operate without overload. The V/I converter was also removed and this led to reduction in both power and noise. A simple calibration technique was incorporated in prototype–II to extract the interstage gain in a background fashion. A random number (Rn) is injected into the second stage VCO, and the interstage gain can be extracted by taking the difference of the average of the second stage output for Rn = 1 and Rn = 0. The block diagram for prototype–II is shown in Fig. 2.10. A 384-tap FIR filter is used for averaging the second stage output.

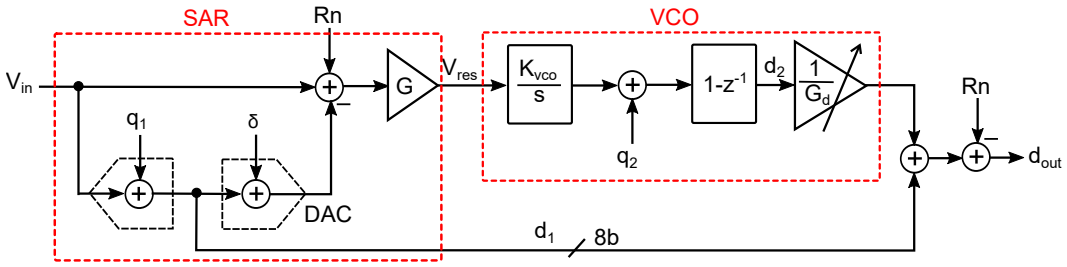


Figure 2.10: Model of prototype–II.

From Fig. 2.10, output of second stage, d_2, can be written as

$$d_2 = \{-(q_1 + \delta) + Rn\}GK_{vco} + q_2\left(1 - z^{-1}\right) \tag{2.10}$$

The output of the ADC can be written as

$$\begin{aligned} d_{out} &= V_{in} + q_1\left(1 - \frac{GK_{vco}}{G_d}\right) - \frac{\delta GK_{vco}}{G_d} \\ &+ Rn\left(\frac{GK_{vco}}{Gd} - 1\right) + \frac{q_2\left(1 - z^{-1}\right)}{G_d} \end{aligned} \tag{2.11}$$

From (4.3), it can be seen that if G_d = GK_{vco}, quantization noise of the first stage as well as the injected random noise, Rn, can be cancelled at the output.

G_d can be obtained from (4.2) from the observation that $\{\overline{d_2(Rn=1)} - \overline{d_2(Rn=0)}\} = GK_{vco}$.

The detailed circuit schematics are presented in the following sub-section.

2.5.1 Detailed circuit schematics

The detailed architecture of prototype–II alongwith the timing diagram, is shown in Fig. 2.11. An 8-bit SAR was used as the first stage. An on-chip pseudo random number generator (PRNG) was designed by linear feedback shift register (LFSR). The pseudo random number has a periodicity of $2^{20} - 1$. The pseudo random number, Rn, is injected differentially into a unit cap in the DAC array.

Average of the VCO output is maintained separately for Rn = 1 and Rn = 0 and the difference gives G_d. The second stage VCO schematic is shown in Fig. 2.12. The counter and the V/I converter from prototype–I are removed in prototype–II. The removal of the counter, clocked by the high speed VCO output, greatly reduced the power consumption. The reduction in VCO input swing is sufficient to prevent its overloading in the absence of the counter. The removal of the V/I converter reduces both power consumption as well as noise.

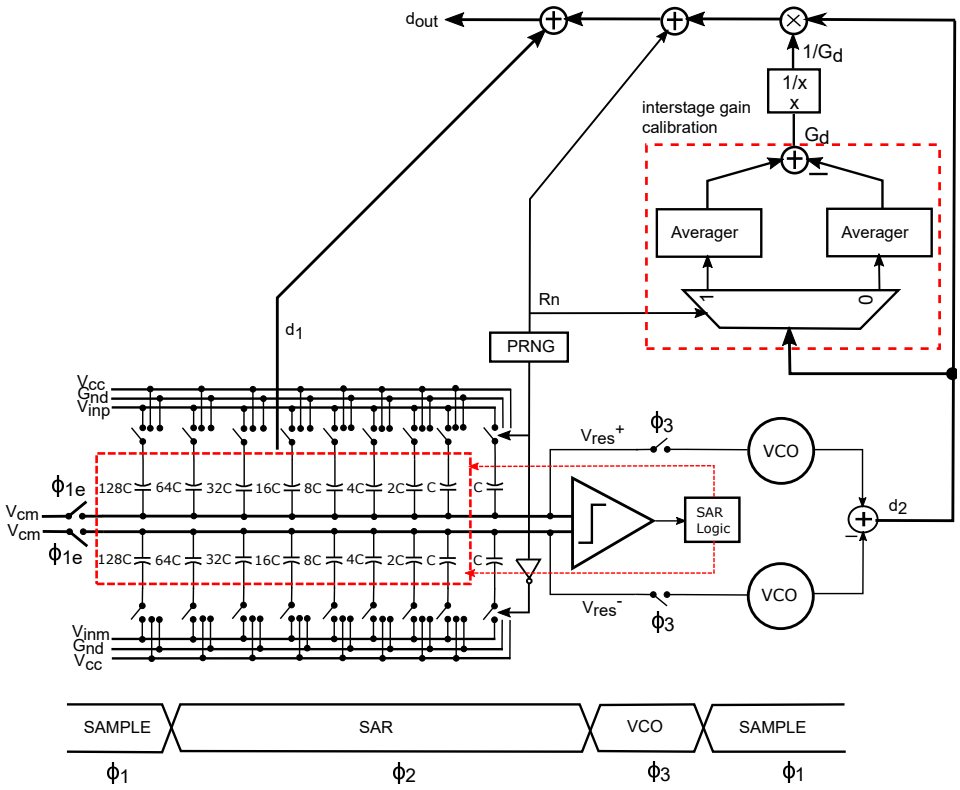


Figure 2.11: Architecture of prototype–II.

2.5.2 Choice of SAR stage resolution

To decide on the resolution of the first stage SAR, an optimization was carried out to decide on the SAR resolution with the best energy efficiency for each conversion. A simple model was used with power numbers obtained from simulation of the different circuit blocks. Some assumptions were made so that the model is not too complex but can still provide reasonably accurate insights. It was assumed that the VCO is linear over the entire range of operation. It was also assumed that the overall ADC has a thermal noise limited resolution when the resolution exceeds 12 bits (at an OSR of 8) and limited by quantization noise otherwise. It was also

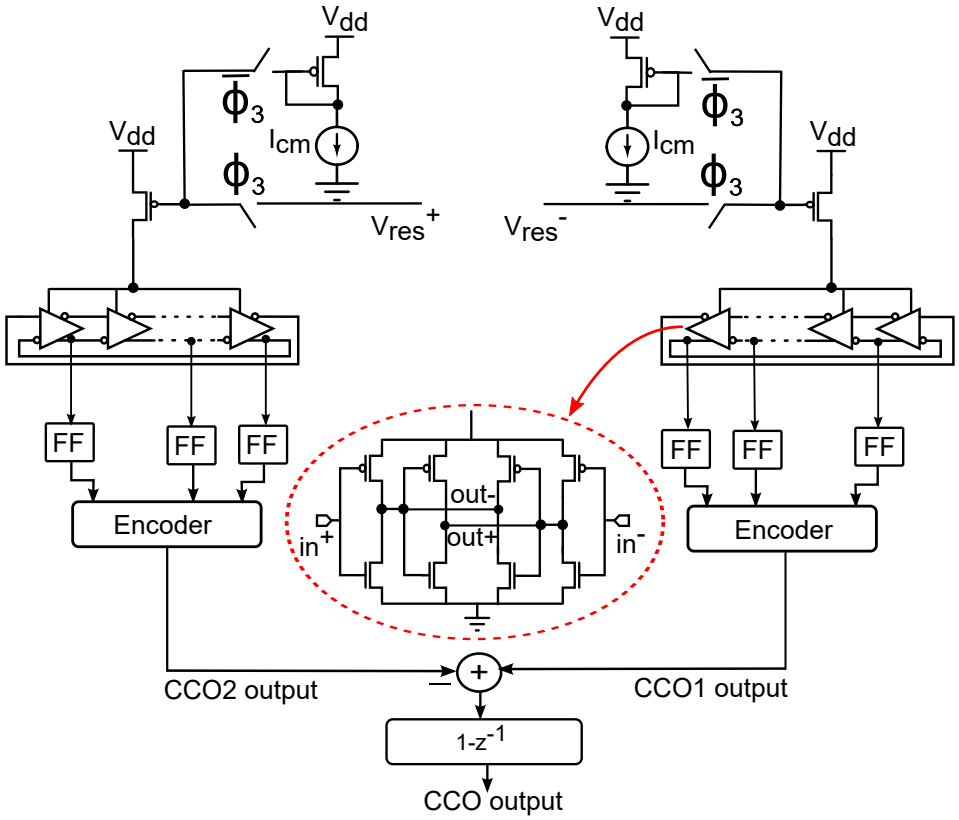


Figure 2.12: VCO stage schematic for prototype–II.

assumed that the second stage noise dominates the kT/C noise of the SAR DAC when the SAR resolution is below 6 bits. The result of the optimization is shown in Fig. 2.13.

It can be seen from Fig. 2.13 that at low SAR ADC resolution, it is beneficial in terms of energy efficiency to increase SAR resolution as the number of SAR cycles grow linearly but the resolution increases exponentially. Since, the VCO is the dominant noise source at low SAR resolutions, the SAR DAC capacitance does not have to be scaled up to reduce its kT/C noise. Thus, the SAR power increase

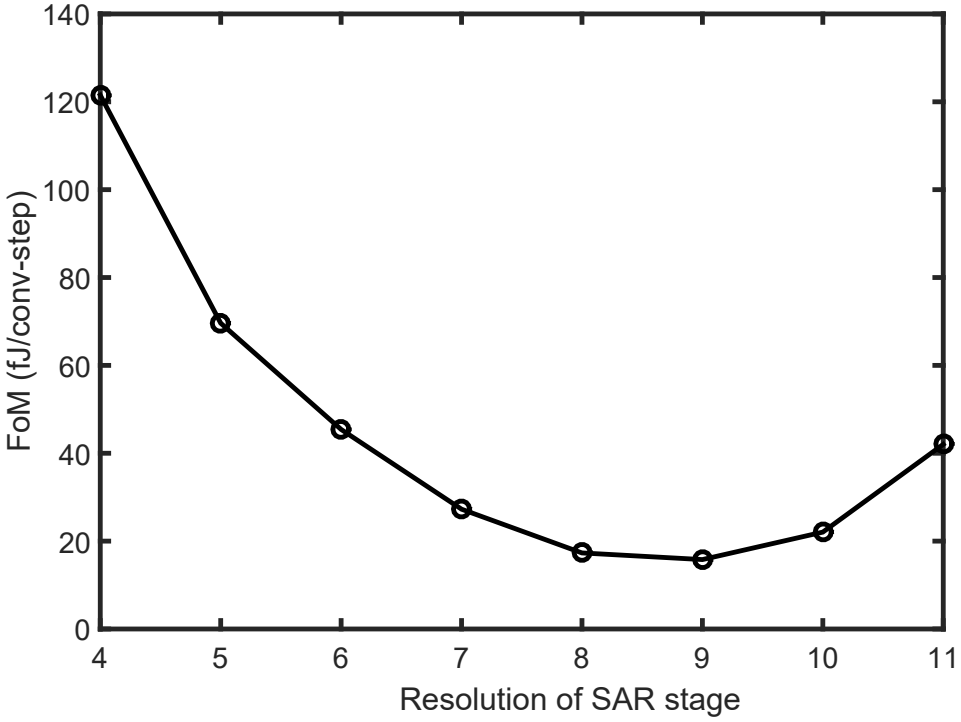


Figure 2.13: SAR stage resolution optimization.

is from the digital logic which increases linearly while the overall ADC resolution increases exponentially. Thus, the energy efficiency of the ADC increases with SAR resolution for medium resolution range. There is a shallow optimum between SAR resolutions of 7-10. Above SAR resolution of 10, the ADC resolution is dominated by thermal noise and kT/C noise. To increase the resolution by 1 bit, the analog power increases by 4 times. This leads to reduction in energy efficiency above 10 bits of SAR resolution. For this prototype, a resolution of 8 bits is chosen for the SAR stage.

Another constraint that dictates the first stage resolution is the speed of convergence of the background calibration technique. In deriving the relation,

$\{\overline{d_2(Rn=1)} - \overline{d_2(Rn=0)}\} = GK_{vco}$, it has been implicitly assumed that averaging significantly reduces the noise. However, even though the quantization noise of the first stage is canceled at the output, it can still affect the background calibration convergence speed. If the first stage resolution is low, then the background calibration will take longer to converge. To verify this, a MATLAB behavioral model was built for the SAR-VCO architecture. The resolution of the SAR stage was varied keeping the overall ADC resolution same. The result of MATLAb simulation for two different SAR resolution, 5 and 8 bits, is plotted in Fig. 2.14. It can be clearly seen that the background calibration takes much longer to converge if the SAR has a resolution of 5 bits compared to a resolution of 8 bits. Hence, from calibration convergence speed perspective, it is also favorable to have a high resolution from the first stage.

2.5.3 Measurement results

The printed circuit board (PCB) used for testing the ADC prototype–II is shown in Fig. 2.15. Voltage regulator ICs (LT3082) are used to generate the voltage supplies for the ADC prototype. An Agilent 811505A signal generator is used to generate the input signal for testing the ADC. The 720 MHz clock needed for SAR comparisons is provided from high frequency signal generator E8257D. The 720 MHz clock is divided down to 36 MHz inside the prototype for sampling. The outputs are captured using an Agilent 16802A logic analyzer.

The measured spectrum of prototype–II is shown in Fig. 2.16. A sampling frequency of 36 MHz and input frequency of 0.5 MHz was used. At an input swing

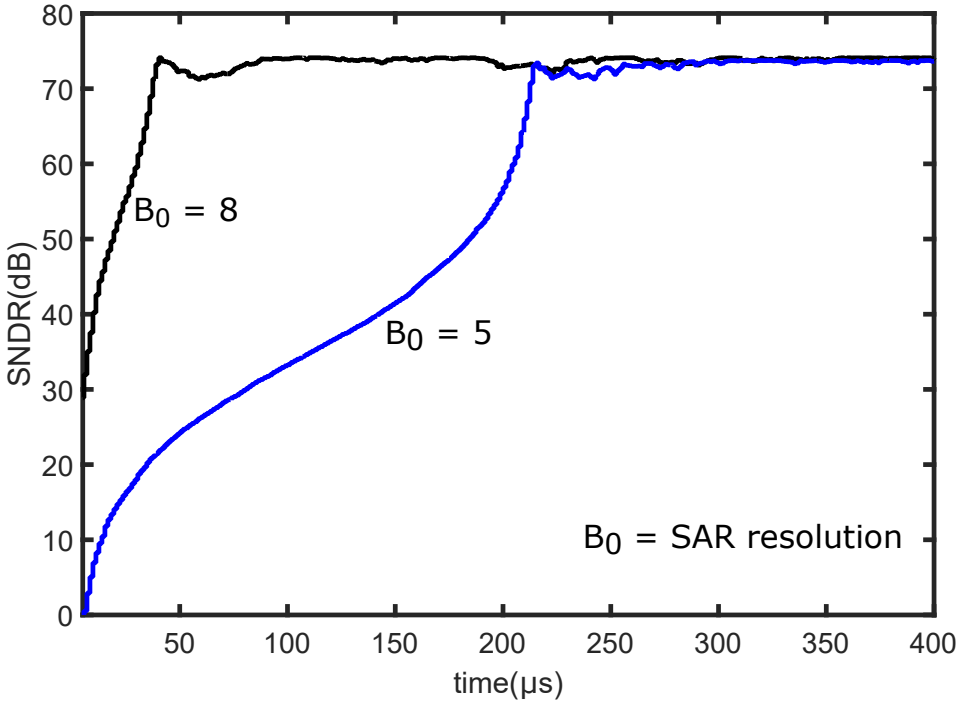


Figure 2.14: Background calibration convergence speed for different SAR resolutions.

of 2.2V peak-peak, the prototype has an SNDR of 74.3 dB and SNDR of 74.5 dB at an OSR of 10. The in-band SFDR is -86 dB, while the out-of-band SFDR is -81 dB both of which are comfortably low enough not to distortion limit the output.

Measured SNDR versus amplitude sweep for the prototype is shown in Fig. 2.17. The ADC has a very good linearity as can be seen from Fig. 2.17. The prototype has a measured dynamic range of 75.7 dB.

Foreground calibration is used to extract the capacitor mismatches. The interstage gain is extracted through background calibration. Fig. 2.18 compares the measured spectrum with and without calibration. Calibration reduces the second

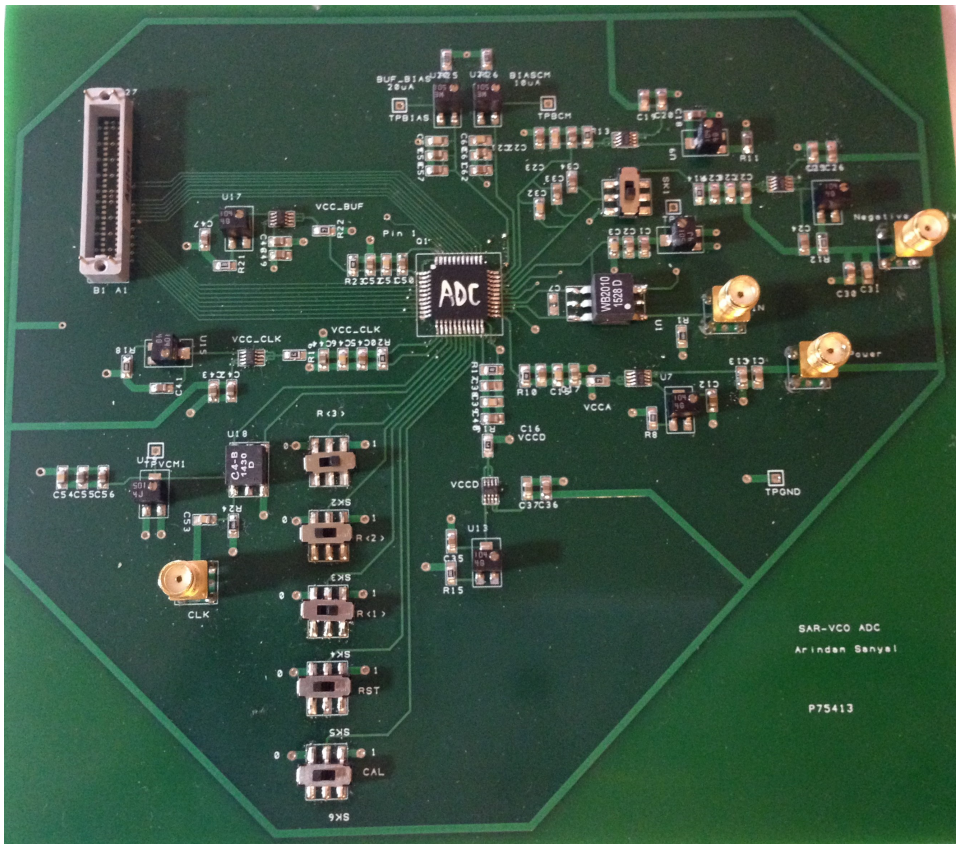


Figure 2.15: PCB for testing prototype–II.

harmonic distortion by 10.3 dB and the third harmonic distortion by 22.2 dB. The overall SNDR is improved by 9.8 dB with calibration.

Fig. 2.19 shows how the SNDR varies with time when background calibration is enabled. Initially, the SNDR starts at a low value and as the background calibration is kept running, the SNDR converges to its final value. The proposed background calibration is quite fast and converges in 40 μs.

To compare the performance of prototype–II with the state-of-the-art, two

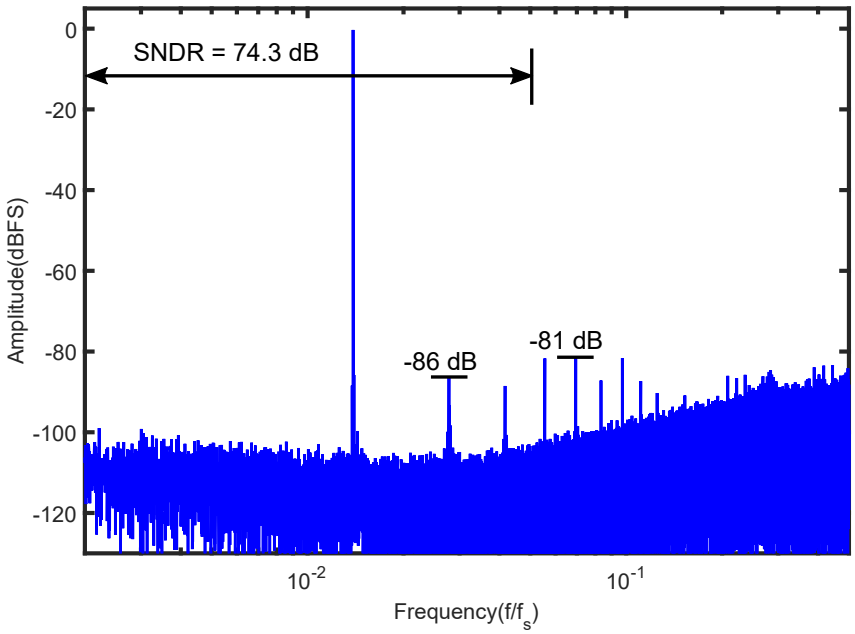


Figure 2.16: 2^{18} point windowed spectrum of prototype–II for f_{in} = 0.5 MHz and f_s = 36 MHz.

figure-of-merits (FoMs) are used, namely, the Walden FoM and the Schreier FoM. The Walden FoM is defined as FoM $=$ Power$/2^{\text{res}}/(2\text{BW})$. The Schreier FoM is defined as FoM $=$ SNDR $+ 10\log_{10}$ (BW/Power).

Fig. 2.20 shows the variation of SNDR and Walden FoM versus OSR. It can be seen from Fig. 2.20 that the prototype has an FoM of 18.5 fJ/step at an OSR of 6. The Schreier FoM for prototype–II is 172.2 dB.

Prototype–II is compared with other state-of-the-art VCO-based ADCs in Table 2.2. It can be seen that prototype–II achieves the best Walden FoM.

The two prototypes are compared with previously published state-of-the-art oversampled ADCs in Fig. 2.21 and Fig. 2.22. The data for the figures are

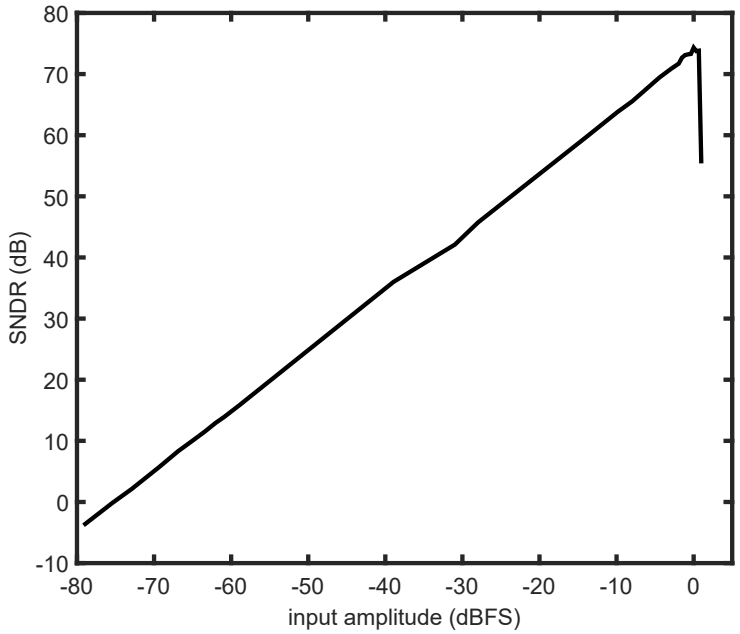


Figure 2.17: Measured SNDR vs amplitude sweep for prototype–II

taken from the survey made available by Dr. Boris Murmann (`http://web.stanford.edu/~murmann/adcsurvey.html`). It can be seen that the prototype–II has a significantly improved performance over prototype–I. Prototype–II compares very favorably with the best reported works.

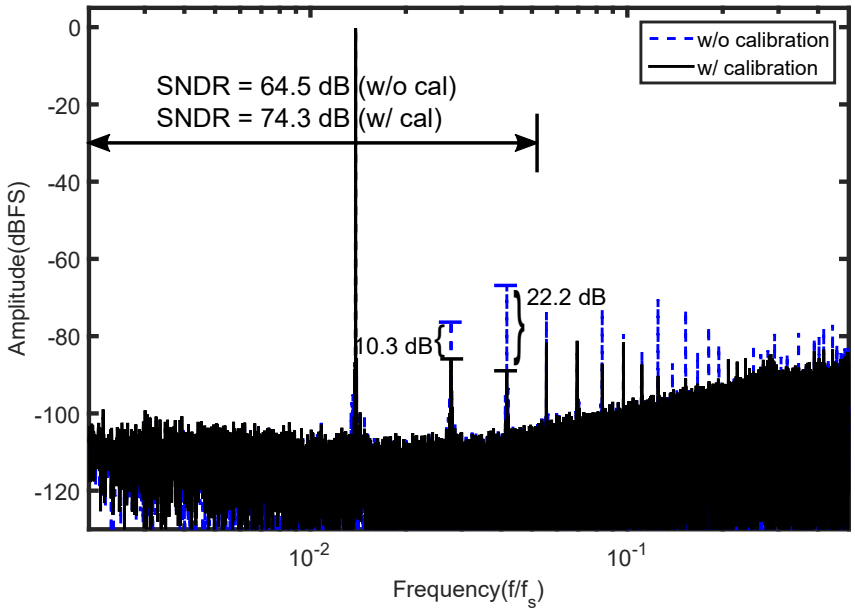


Figure 2.18: Measured spectra showing the effect of calibration.

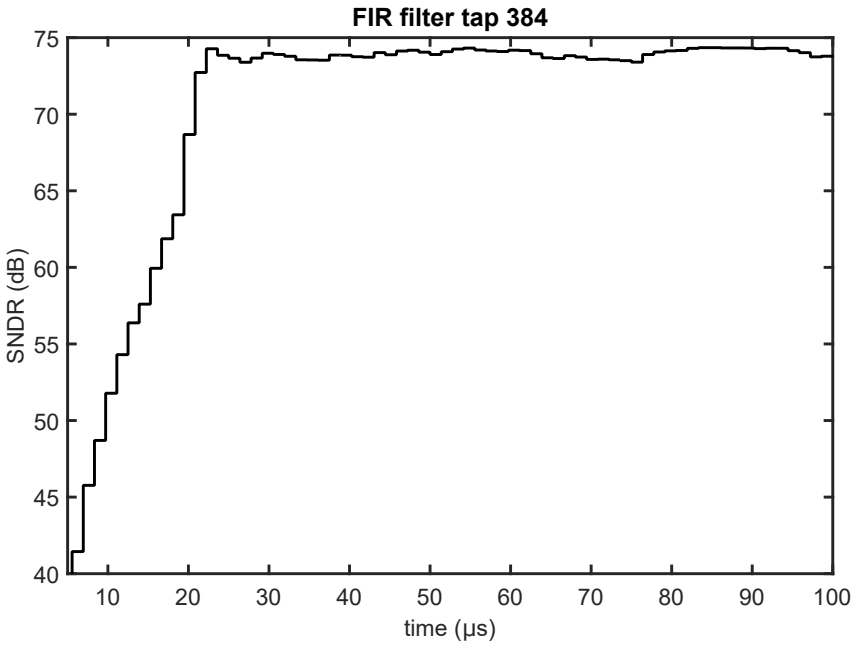


Figure 2.19: SNDR variation with time in presence of background calibration.

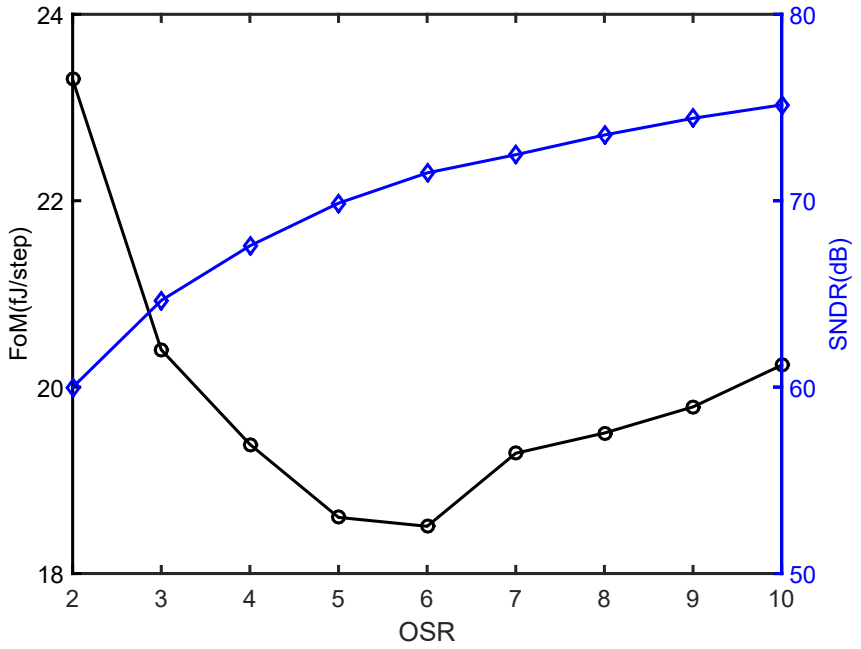


Figure 2.20: Walden FoM and SNDR versus OSR for prototype–II.

Table 2.2: Comparison with existing VCO-based ADCs.

	[Reddy et al. [2012]]	[Rao et al. [2013]]	[Young et al. [2014]]	[Reddy et al. [2015]]	**This work**
Process(nm)	90	90	65	65	**40**
Area(mm^2)	0.36	0.16	0.49	0.5	**0.03**
F_s(MHz)	600	640	1280	1200	**36**
BW(MHz)	10	5	50	50	**1.8**
OSR	30	64	13	10	**10**
SNDR(dB)	78.3	74.7	64	71.5	**74.3**
Power(mW)	16	4.1	38	54	**0.35**
FoM(fJ/step)	120	92	294	176	**18.5**

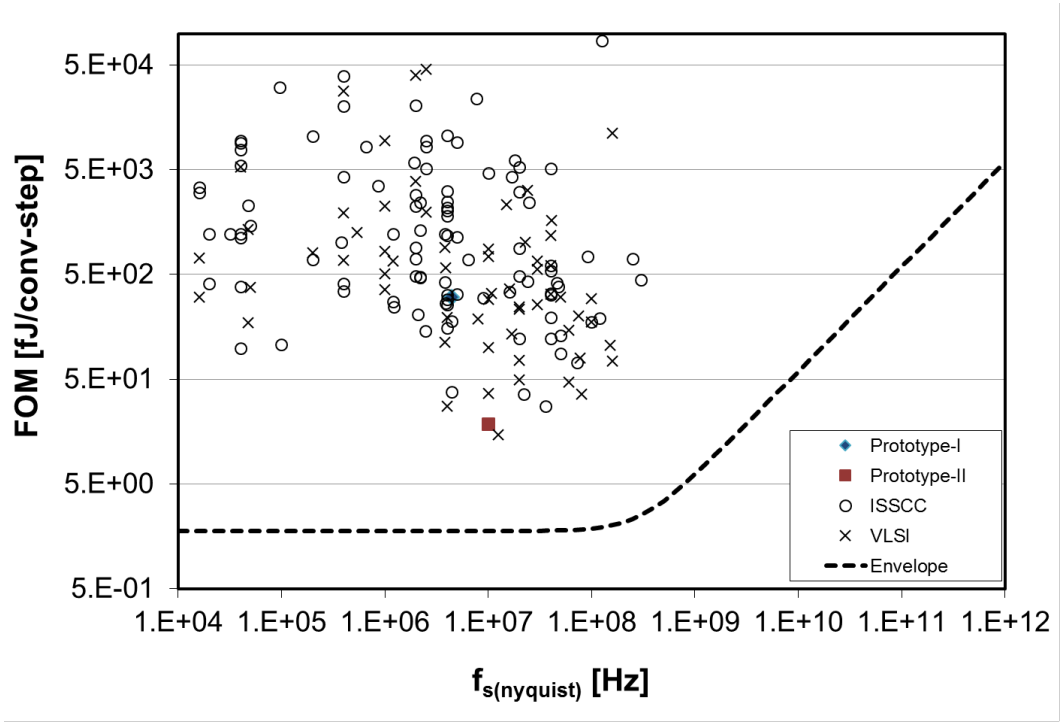


Figure 2.21: Comparison of Walden FoM of the two prototypes with existing work

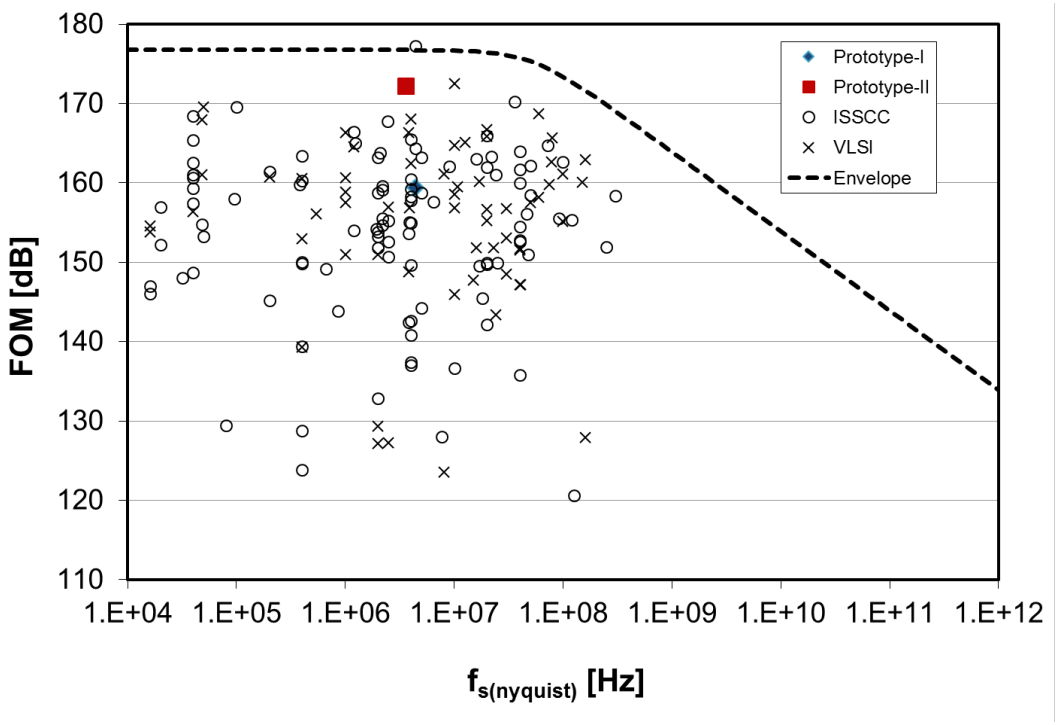


Figure 2.22: Comparison of Schreier FoM of the two prototypes with existing work

Chapter 3

Capacitance to digital converter

3.1 Introduction

Capacitive sensors can measure a variety of physical quantities, such as pressure, position, and humidity. They are widely used in emerging applications, such as wireless sensor nodes and biomedical implants. These applications require high resolution and low-energy capacitive-to-digital converters (CDCs). A very popular way to sense capacitance is to sample a known voltage on the sensing capacitor, and then quantizing the charge across the capacitor. The quantized charge is proportional to the value of the sensing capacitor. This is quite similar in operation to ADCs with capacitive DAC, which sample a variable voltage across a known capacitor and then quantize the charge, the quantized charge being proportional to the sampled voltage. Thus, a CDC can be built from an ADC. In this chapter, we extend our proposed SAR-VCO $\Delta\Sigma$ ADC architecture to design a very high energy-efficiency CDC. The CDC prototype has been designed and fabricated in 40nm CMOS technology. The photograph of the die is shown in Fig. 3.1.

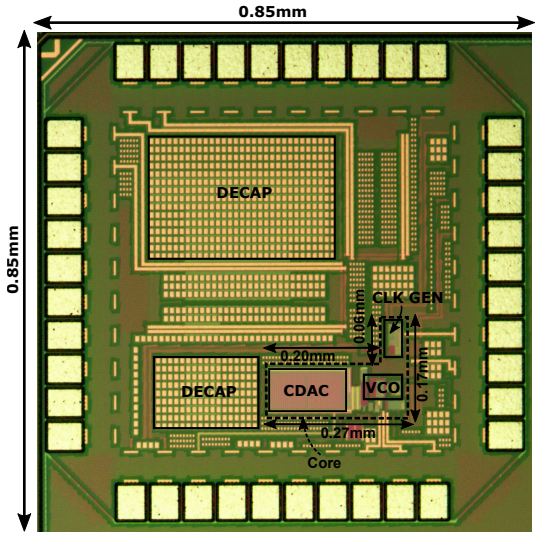


Figure 3.1: Die microphotograph for CDC prototype.

3.2 Review of existing CDCs

Most CDCs work by sampling a known voltage on the sensing capacitor, and then quantizing the charge using an ADC. SAR ADC is a good candidate for energy efficient CDCs. Nevertheless, it is challenging to achieve high resolution with a SAR based CDC alone as the voltage swing at the comparator input is greatly reduced due to charge sharing between the sensing capacitor and the capacitive DAC. One way to address this issue is to use an OTA to perform an active charge transfer as in [Ha et al. [2014]], however at the cost of increased power. Switched capacitor $\Delta\Sigma$ ADC is suitable for high resolution CDCs, but they rely on the use of OTAs that are power hungry and scaling unfriendly [Xia et al. [2012]; Tan et al. [2013]]. Additionally, because of the low resolution of their internal quantizer, they require a large oversampling ratio (OSR). This means that the large sensing capacitor has to be charged many times, which also degrades the energy efficiency.

A recent work [Oh et al. [2014]] combines a $\Delta\Sigma$ ADC with 9-bit SAR quantizer to reduce OSR, but it still uses 2 OTAs. To reduce power and obviate the need for OTAs, a delay chain based CDC was developed in [Jung et al. [2015]], but its resolution is limited and it is not suitable for sensing small capacitors despite its wide sensing range.

3.3 Proposed CDC

Since the SAR-VCO ADC presented in the previous chapter achieves a very good energy efficiency, we will extend the SAR-VCO architecture to design a CDC. The SAR-VCO architecture is naturally suitable for quantization of charge across the sensing capacitor. Thus, the SAR-VCO ADC architecture can be adopted for the CDC design with minor changes. The main advantages of the SAR-VCO architecture are

1. the VCO relaxes the precision requirement for the SAR comparator and permits the use of a small dynamic comparator for power saving.

2. the VCO provides an intrinsic 1st-order noise shaping, which further increases the resolution.

3. The SAR significantly reduces the requirements on the VCO linearity and the OSR.

The proposed CDC is highly digital and scaling friendly. No OTA is needed. Compared to the state-of-the-art [Ha et al. [2014]; Xia et al. [2012]; Tan et al.

[2013]; Oh et al. [2014]; Jung et al. [2015], the proposed CDC achieves the best FoM of 60fJ/conversion-step, which is more than 2 times smaller than the next best reported in literature.

Fig. 3.2 illustrates the circuit implementation and timing diagram of the proposed CDC. A 9-bit SAR has been used as the first stage. During the sampling phase ϕ_1, C_{SENSE} samples V_{CC}, C_{REF} samples G_{nd}, and the SAR CDAC is in reset. At the end of ϕ_1, the bottom plate of CDAC is left open, C_{SENSE} is switched to G_{nd} and C_{REF} is switched to V_{CC}. As a result, a net charge proportional to $(C_{SENSE} - C_{REF})$ is transferred onto CDAC. During ϕ_2, this charge is quantized by a 9-bit SAR ADC. The size of the unit capacitor in CDAC is 12fF, so that the CDC can sense a maximum differential capacitance $(C_{SENSE} - C_{REF})$ of 6pF. No redundancy is provided in the CDAC because the VCO can absorb SAR quantization error.

After SAR finishes, its residue voltage V_{res}, directly available at the comparator input, is sent to a ring VCO for fine quantization during ϕ_3. The VCO performs a phase domain integration of V_{res} and its output d_2 is obtained by sampling the inverter outputs and performing a first-order differentiation $(1-z^{-1})$ using XOR gates. The VCO consists of a single PMOS input transistor and a 7-stage current-starved inverter chain. PMOS is chosen over NMOS to reduce flicker noise. Since the VCO sees only a very small signal swing, it is highly linear and does not require any nonlinearity calibration. Each VCO cell is made pseudo-differential to improve power supply rejection. During ϕ_1 and ϕ_2, the VCO is not switched off as charge leakage will introduce error in the phase value held by the VCO and degrade the

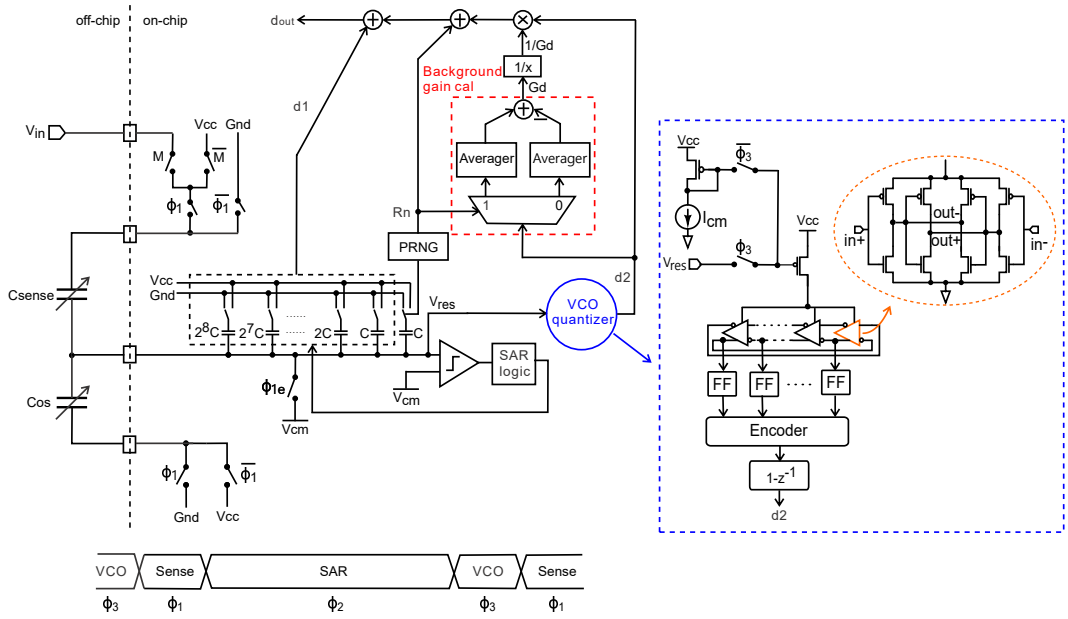


Figure 3.2: Schematic diagram of the proposed CDC.

CDC linearity. Instead, the VCO is controlled by a small current source I_b which keeps the VCO running at a low frequency. To facilitate the testing of the CDC, we provide two operation modes controlled by M. When M=1, the CDC is in the normal operation mode. When M=0, the CDC is in test mode and C_{SENSE} samples an external voltage Vin. This allows the full-range testing of CDC using a fixed C_{SENSE} by varying Vin.

The final CDC output dout is obtained by combining the 1st-stage SAR output d_1 and the 2nd-stage VCO output d_2. To ensure high linearity, d_2 needs to be scaled with an appropriate digital gain G_D that matches the analog interstage gain G_A. This is a challenge for the proposed CDC because G_A depends on the VCO tuning gain which is PVT sensitive. To address this issue, a digital background

calibration technique is developed. A pseudo-random number generator (PRNG) is built on-chip using a 20-stage linear feedback shift register (LFSR). Its output Rn controls an LSB capacitor in CDAC. When Rn=0, the LSB capacitor is always connected to Gnd. When Rn=1, the LSB capacitor is switched to Vcc by the end of ϕ_2. As a result, V_{res} increases, resulting in a larger d_2 compared to when Rn=0. Since the amount of shift in d_2 corresponds to an LSB change in d_1, it exactly reflects the interstage gain G_A. As a result, we can extract G_A from the difference between the d_2 averages for Rn=1 and Rn=0. This can be implemented easily in the hardware by passing d_2 through a 1-to-2 DEMUX followed by two averaging blocks and a subtractor. This calibration technique operates in the background without disturbing the normal operation of the CDC.

Fig. 3.3 shows the signal flow diagram of the proposed CDC. The factor G reflects the voltage attenuation at the comparator input node due to the charge sharing between C_{SENSE}, C_{REF}, C_{DAC}, and the parasitic capacitance C_{par}. G is given by $C_{DAC}/(C_{DAC}+C_{SENSE}+C_{REF}+C_{par})$. K_{VCO} is the VCO tuning gain. d_2 is scaled by the digital gain G_D and then combined with d_1.

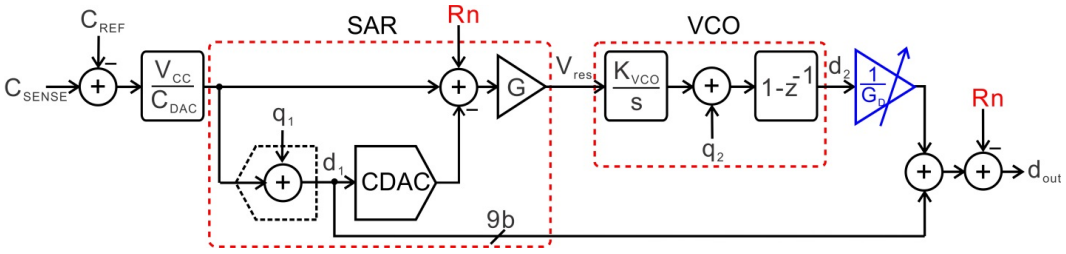


Figure 3.3: Signal flow diagram of the proposed CDC.

Based on Fig. 3.3, it is easy to derive that:

$$
\begin{aligned}
d_{out} &= ((C_{SENSE} - C_{REF})V_{CC})/C_{DAC} + q_1(1 - G_A/G_D) \\
&+ (q_2(1 - z^{-1}))/G_D - R_n(1 - G_A/G_D) \qquad (3.1)
\end{aligned}
$$

where G_A is the analog interstage gain given by GK_{VCO}. If $G_A = G_D$, the SAR quantization noise q_1 as well as Rn is cancelled at the output. The final quantization noise at dout comes solely from the VCO q_2 and is 1st-order shaped. Any mismatch between G_A and G_D will result in q_1 and Rn leaking to the output, thus significantly increasing the in-band noise floor. To ensure G_A=G_D, we digitally adjust G_D to match G_A. More specifically, we set $G_D = \overline{(d_2(R_n = 1))} - \overline{(d_2(R_n = 0))}$, where d_2 is given by: $d_2 = -q_1G_A + q_2(1 - z^{-1}) + G_AR_n$. Note that only the last term in d_2 depend on Rn. The first two terms in d_2 do not depend on Rn, and thus, are canceled in the subtraction between d_2 for Rn=1 and Rn=0.

The capacitance sensing range can be extended by increasing the value of C_{REF}. This is illustrated graphically in Fig. 3.4.

3.4 Measurement Results

The proposed CDC is designed and fabricated in 40nm CMOS process. It consumes 75μW under 1V power supply while operating at 3MS/s. The printed circuit board (PCB) used for testing the CDC prototype is shown in Fig. 3.5. A ceramic capacitor is used as the sensing capacitor and is clearly marked on the PCB diagram. Voltage regulator ICs (LT3082) are used to generate the voltage supplies for the CDC prototype. An Agilent 811505A two-channel signal generator is used

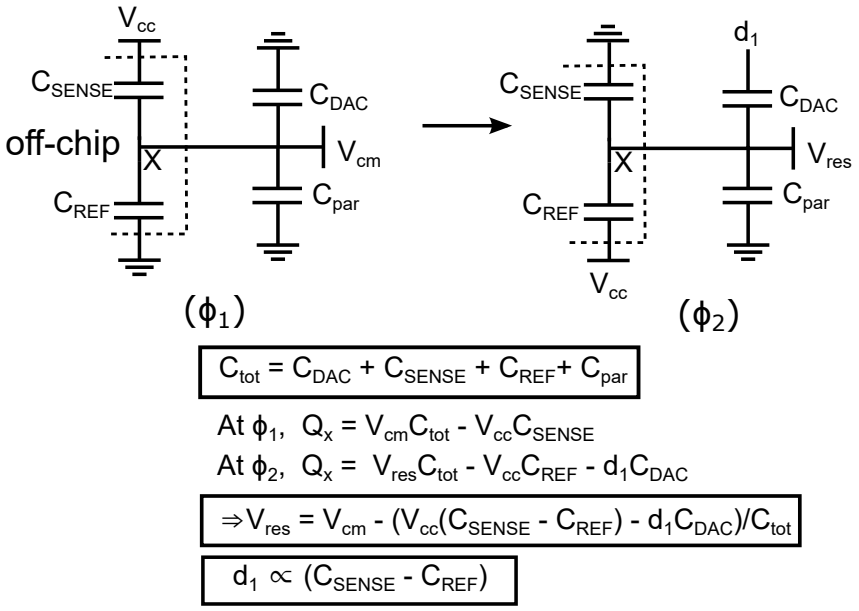


Figure 3.4: Illustration of sensing capacitance range extension using C_{REF}.

to provide the 45 MHz clock for the SAR comparator, and a 450 KHz signal for testing the CDC in the ADC mode (M=0). The 45 MHz clock is divided down to 3 MHz inside the prototype for sampling. The outputs are captured using an Agilent 16802A logic analyzer.

During the testing mode (M=0), a fixed capacitor C_{SENSE} of 5pF is connected to CDC, and CREF is set to 0. A sine wave at 40kHz is applied at Vin. Fig. 3.6 shows the measured CDC output spectra.

Without background calibration, we use the interstage gain value from the post-layout simulation, resulting in an SNR of 65dB at the OSR of 8. With background calibration, an accurate interstage gain is obtained, leading to an SNR of 69.8 dB. The harmonics in Fig. 3.6 are produced by the signal generator, not the

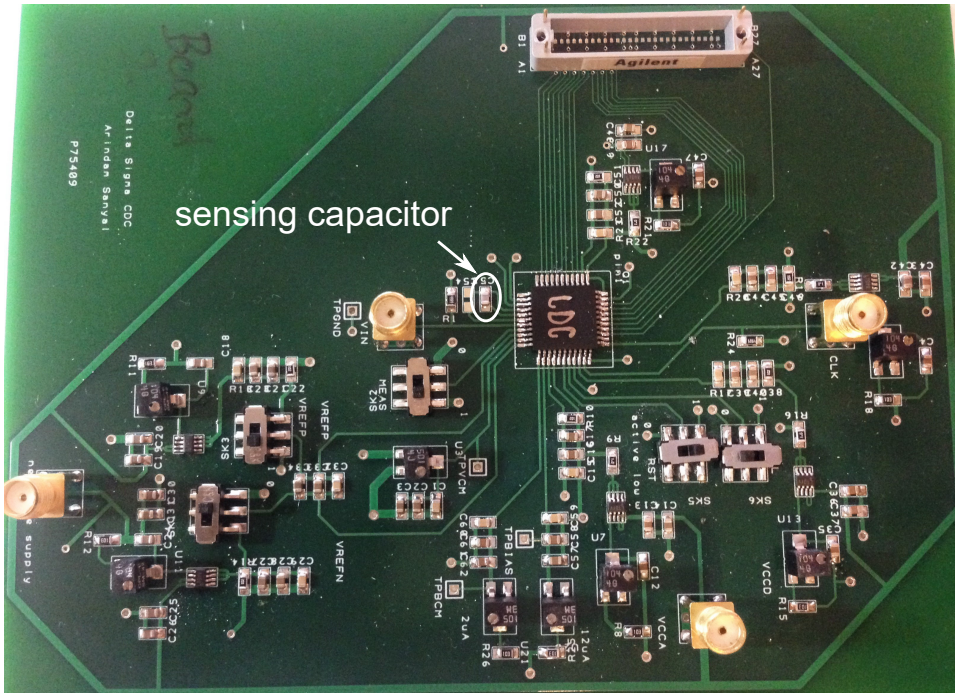


Figure 3.5: PCB used for CDC testing

CDC chip. Our lab currently does not have high-quality low-pass filters that can filter out them.

Fig. 3.7 shows the measured distribution of d_2. When Rn=1, the average of d_2 is 8.64. When Rn=0, the average of d_2 is 8.23. From this difference, we can extract G_A=0.41.

Fig. 3.8 shows the CDC output digital code versus sensor capacitance. The noise standard deviation is superimposed on the output digital code.

Fig. 3.9 plots SNR and FoM as a function of OSR. The FoM is defined as

$$\text{FoM} = \frac{\text{conversion energy}}{2^{[20\log_{10}(\text{input range}/2/\sqrt{2}/\text{resolution})-1.76]/6}}$$

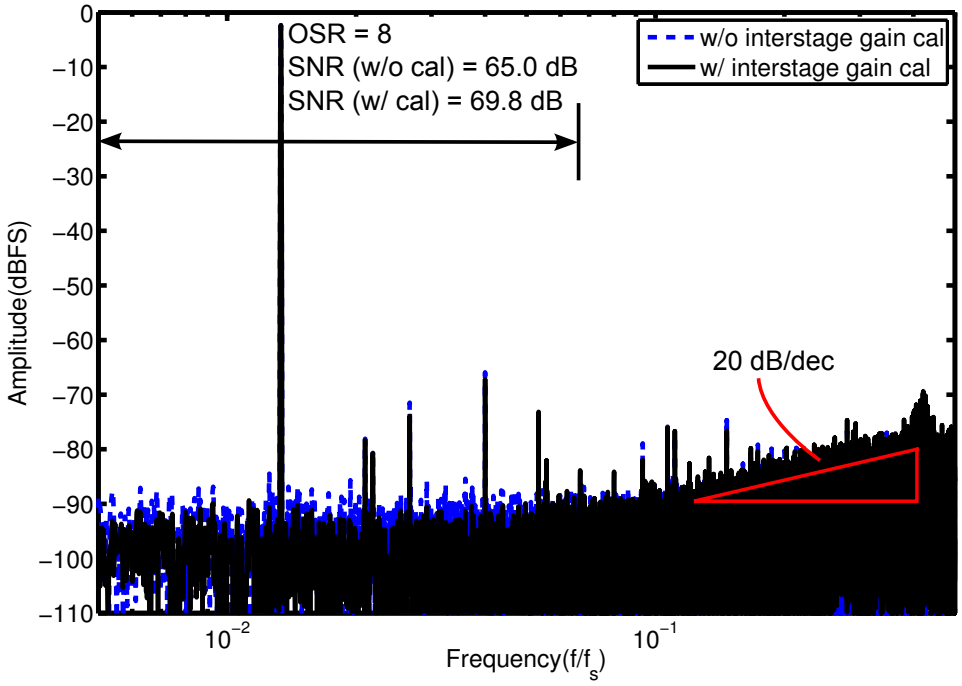


Figure 3.6: Measured CDC output spectra.

where the conversion energy is defined as the product of measurement time and power consumed by the CDC, the measurement time being OSR/sampling frequency.

The best FoM is obtained at the OSR of 4, with an SNR of 66 dB and a resolution of 1.3fF. At the OSR of 4, the effective measurement time is 1.3us, and the total conversion energy is 100pJ.

The performance of the proposed CDC is compared with the existing work in Table 3.1. It can be seen from the table that the energy efficiency of the proposed CDC is more than 2 times better than the next best technique reported in the literature.

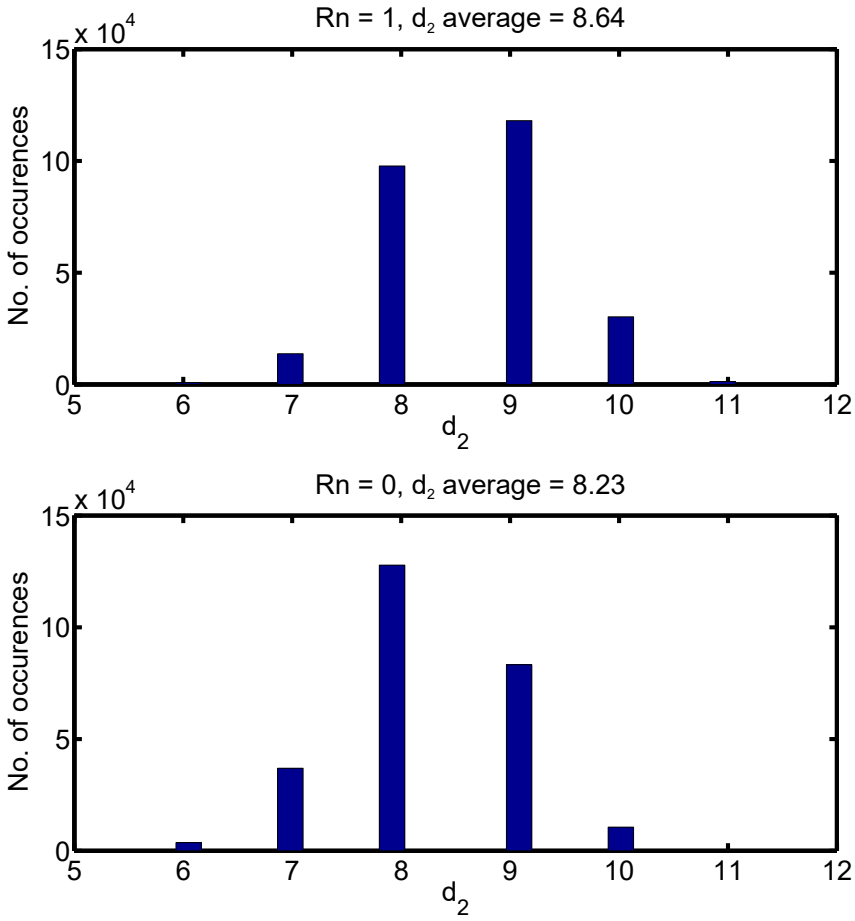


Figure 3.7: Measured d_2 histogram for Rn = 1 and Rn = 0.

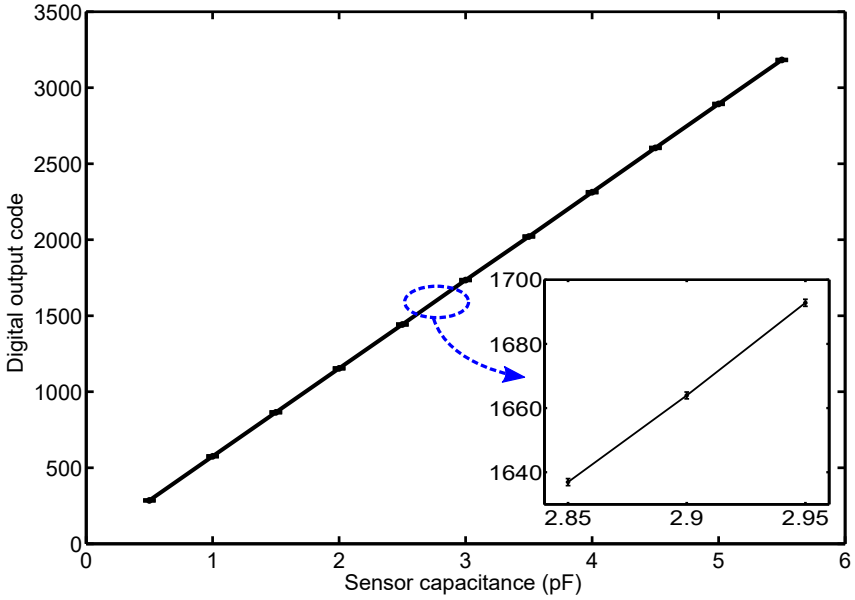


Figure 3.8: Measured CDC output code versus sensor capacitance.

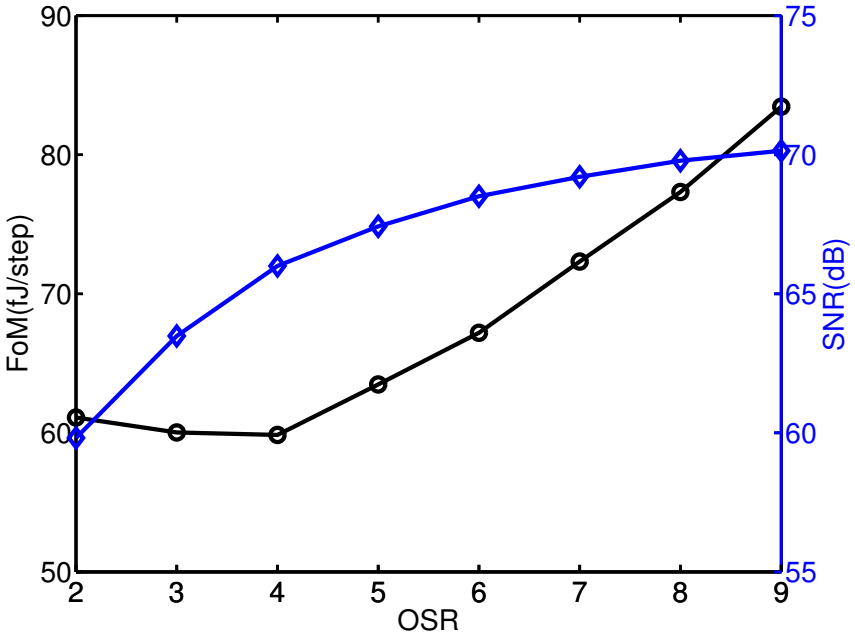


Figure 3.9: Measured SNR and FoM as a function of OSR.

Table 3.1: Comparison with prior art.

	Ha et al. [2014]	Tan et al. [2013]	Oh et al. [2014]	Jung et al. [2015]	**This work**
Process(nm)	180	160	180	40	**40**
Method	CDS + SAR	$\Delta\Sigma$	SAR + $\Delta\Sigma$	Delay chain	**SAR + VCO**
Input range	2.5 - 75.3pF	0.54 - 1.06pF	0 - 24pF	0.7pF - 10nF	**0 - 6.25pF**
Resolution	6fF	70aF	0.16fF	12.3fF	**1.3fF**
Measure Time	4ms	0.8ms	230μs	19μs	**1.3μs**
Power	160nW	10.3μW	33.7μW	1.84μW	**75μW**
Conversion energy	640pJ	8.26nJ	7.75nJ	35.1pJ	**100pJ**
FoM (fJ/conv-step)	181	3900	175	141	**60**

Chapter 4

Simultaneous Mitigation Of Static and Dynamic Errors in CT $\Delta\Sigma$ Modulators

4.1 Introduction

There has been a shift from discrete-time (DT) $\Delta\Sigma$ modulators to continuous-time (CT) $\Delta\Sigma$ modulators. This is mainly because CT modulators can operate at higher speeds than DT modulators for the same power consumption. In addition, CT ADCs have intrinsic anti-aliasing filters and thus can do without an explicit power hungry, anti-alias filter at the front end, unlike DT ADCs. However, CT operation introduces dynamic inter symbol interference (ISI) error which is not present in DT modulators. Traditional dynamic element matching (DEM) algorithms are designed to reduce static mismatch in DT modulators and fail to handle dynamic ISI error. In this chapter, we present digital techniques to address static mismatch error and dynamic ISI error simultaneously. This chapter[1] is organized as follows: a brief background of non-idealities in CT modulators is presented along with the motivation for the proposed algorithms. This is followed by a general model for ISI error and a review of the existing state-of-the-art. Three techniques are pre-

[1] This chapter is a partial reprint of the publication: Arindam Sanyal and Nan Sun, "Dynamic element matching techniques for static and dynamic errors in continuous-time multi-bit $\Delta\Sigma$ modulators", *accepted in IEEE JETCAS*, 2015. I thank Dr. Sun for his advise and help in preparing this manuscript.

sented to address both static and dynamic errors in CT, $\Delta\Sigma$ modulators, namely, (1) a modified thermometer coding technique which minimizes ISI error while high-pass shaping static mismatch [Sanyal et al. [2014]] (2) an enhanced ISI shaping technique [Sanyal and Sun [2014b]] which improves the in-band signal-to-noise ratio compared to the existing work, and (3) a technique to shape ISI and static mismatch error of each DAC element while decorrelating the instantaneous transition density from the input [Sanyal et al. [2015]; Sanyal and Sun]. Finally, the proposed techniques are compared with the existing work.

4.2 Background and Motivation

In advanced CMOS technologies, as more efforts are put into increasing the performance of $\Delta\Sigma$ modulators, there has been a natural shift towards adopting multi-bit, continuous-time (CT) $\Delta\Sigma$ modulators. CT modulators are gaining more popularity than their discrete-time (DT) counterparts due to higher speed of operation and/or lower power consumption. In both CT and DT $\Delta\Sigma$ modulators, multi-bit modulators are more popular than single-bit modulators because they can achieve higher stability while ensuring higher signal-to-quantization noise ratio (SQNR) due to more aggressive noise shaping. By doing a finer quantization than single-bit modulators, multi-bit modulators result in a low out-of-band noise (OBN). The main advantages of using a multi-bit modulator over a single-bit modulator are as following:

1. low OBN leads to reduced jitter sensitivity.

2. A low OBN also relaxes the linearity and slew rate requirement for the first-stage integrator in an analog-to-digital converter (ADC) or the reconstruction filter in a digital-to-analog converter (DAC).

However, multi-bit modulators suffer from nonlinearity due to static element mismatch which degrades their performance. Analog/digital calibration, and DEM are two popular ways to handle static element mismatch. Calibration techniques [Moon et al. [1999]; Baird and Fiez [1996]; De Bock et al. [2013]] usually require some apriori knowledge of the device mismatch and very precise measurement of the mismatch error. By contrast, DEM techniques do not need any information about device mismatch. In addition, DEM techniques are purely digital and thus scaling friendly. They consume low power and area at advanced technology nodes. There are several DEM techniques that have been reported in literature. The technique in [Van De Plassche [1976]] whitens element mismatch by randomly selecting the elements. The data weighted averaging (DWA) technique [Jackson [1993]; Baird and Fiez [1995]; Chen and Kuo [1999]] can first-order shape element mismatch by barrel shifting the element selection pattern. Higher order mismatch shaping can be done by more advanced DEM algorithms [Schreier and Zhang [1995]; Galton [1997]; Sun [2011]; Sun and Cao [2011]; Sun [2012]].

In addition to static mismatch, CT $\Delta\Sigma$ modulators also suffer from inter-symbol interference (ISI) which does not affect DT $\Delta\Sigma$ modulators. ISI is a dynamic error which shows up during transition of DAC elements and is present in both single-bit and multi-bit CT modulators. Different from static mismatch, ISI error increases with sampling frequency. Hence, it is more problematic for high

speed CT $\Delta\Sigma$ modulators. ISI can be caused by asymmetric on and off switching, clock skew and parasitic memory effects.

An analog approach to reduce ISI error is to use return-to-zero (RZ) coding. However, it increases sensitivity to clock jitter compared to non-return-to-zero (NRZ) coding. RZ coding also reduces the output signal amplitude for the same total DAC power, and introduces large discontinuities in the output waveform. This in turn increases the linearity and slew rate requirements of the output filter.

Researchers have attempted to reduce ISI error by reducing the asymmetry between on and off switching in the DAC. The technique in [Shui et al. [1998]] controls the on/off delay by adjusting the threshold of the switching transistors. The work of [Mu et al. [2010]] shows that differential DACs can reduce ISI by using relatively fast and identical transistors. The work of [Kauffman et al. [2013]]reports that they can reduce ISI error by using only native NMOS transistors to build a current steering DAC. These techniques rely on the ability to ensure good matching between the switches.

The techniques of [Doorn et al. [2005]; Rueger et al. [2004]; Hezar et al. [2010]] use pulse-width modulation (PWM) to force the switching rate of the DAC to be dominated by the PWM carrier frequency and thus be independent of the input. Thus, use of PWM can prove to be very effective against ISI error. PWM is usually followed by a finite-impulse-response (FIR) DAC which places notches at the PWM carrier frequency and its harmonics to reduce nonlinearity associated with PWM. Mismatches in the FIR DAC will shift the placement of the notches and will increase the out-of-band noise and distortion but will not affect the in-band

noise. Also, the PWM technique itself does not increase the in-band quantization noise. However, in this approach the FIR DAC requires a clock frequency which is much higher than the sampling frequency f_s. It may not be possible to generate such a high clock rate for many applications specially when f_s itself is quite high.

In contrast to the PWM approach, DEM algorithms do not require clock frequencies higher than the sampling frequency. However, most existing mismatch shaping DEM algorithms are designed for DT $\Delta\Sigma$ modulators and cannot mitigate ISI error. This is because DEM algorithms increase the DAC element switching rate to shape static mismatch. However, increased switching activity deteriorates ISI error. DWA is the worst when it comes to ISI error, because it has the highest element switching activity among the traditional DEM algorithms. Higher order DEMs perform better than DWA because they can shape away the static mismatch with lower element switching activity than DWA. Nonetheless, traditional DEM algorithms are still not suitable to address both static mismatch and ISI error simultaneously.

From a purely ISI point of view, thermometer coding is the best technique as it has the minimum element switching rate. Also, for sufficiently large out-of-band noise gain and/or high over-sampling ratio (OSR), the switching activity of thermometer coding will be dominated by quantization noise. Hence, thermometer coding will show low ISI induced distortion as the element transition density has low dependence on input. However, as the OSR is reduced, thermometer coding will show higher ISI induced distortion as the element transition density will have more dependence on input. Also, thermometer coding cannot handle static mismatch. To address this issue, modified thermometer coding schemes [Shen et al.

[2010]; Lee et al. [2009]; Wang and Sun [2014]] have been developed which use intrinsic quantization noise to randomize the element selection pattern. The limitation of this approach is that the static mismatch reduction is not as effective as other DEM techniques, since the static mismatch is not high-pass shaped.

The modified thermometer coding techniques rely on minimizing the number of transitions to reduce ISI error. The modified mismatch shaping (MMS) technique [Shui et al. [1999]] presents another way of reducing ISI error. It made an important observation that ISI error can be reduced significantly by reducing the correlation between the input and DAC element transition sequence. This way, a large part of the ISI error is simply turned into an offset and does not degrade output linearity. Accordingly, the MMS technique tries to ensure that the DAC maintains the total number of up and down transitions every cycle relatively constant. Despite its clear advancement over prior works, MMS technique has some limitations. It assumes both up and down transitions contribute equal ISI error which does not cover all possible ISI scenarios. Also, it requires good matching between ISI errors of individual DAC elements.

The ISI shaping technique of [Risbo et al. [2011]] represents a major improvement over the MMS technique. A general model for ISI error is developed in [Risbo et al. [2011]] and it has been shown that nonlinearity due to ISI can be attributed completely to only one of the four possible transitions ($0 \rightarrow 0, 0 \rightarrow 1, 1 \rightarrow 0, 1 \rightarrow 1$). Thus, by ensuring that the long term average of only the up transition ($0 \rightarrow 1$) remains constant, the ISI error can be high-pass shaped.

In this chapter, we present 3 different techniques to address both ISI and static mismatch errors. We first present a modified thermometer technique that achieves high-pass shaping of static mismatch in addition to minimizing ISI error. Then we present an improvement on the ISI shaping technique of [Risbo et al. [2011]] in which both the up transition and the down transition are monitored, rather than monitoring only the up transition as in the work of [Risbo et al. [2011]]. The proposed technique improves the ISI shaping performance as the transition count resolution is improved. However, similar to the technique of [Risbo et al. [2011]], the performance is limited by ISI induced distortion at large signal amplitudes. This is because at large signal amplitudes, the instantaneous number of DAC element transitions is still correlated with the input signal even though the long term average of the transitions is constant. To address this issue, we present yet another technique which ensures that the number of transitions of the DAC element is uncorrelated with the input signal at every cycle. Thus, it can achieve a very good decorrelation between instantaneous transition density and the input signal. Further, the proposed technique also ensures that the long term transition density of each element is identical. Thus, the ISI error for each element is high-pass shaped.

4.3 ISI model

In this Section, the ISI model is presented for a $\Delta\Sigma$ DAC. However, the model is equally valid for a $\Delta\Sigma$ ADC as the effects of ISI error is same for both $\Delta\Sigma$ ADC and DAC. The general architecture of a $\Delta\Sigma$ DAC is shown in Fig. 4.1. Let us use $d_i[n]$ to represent the single-bit digital input for the i-th unit element

DAC in a multi-bit DAC.

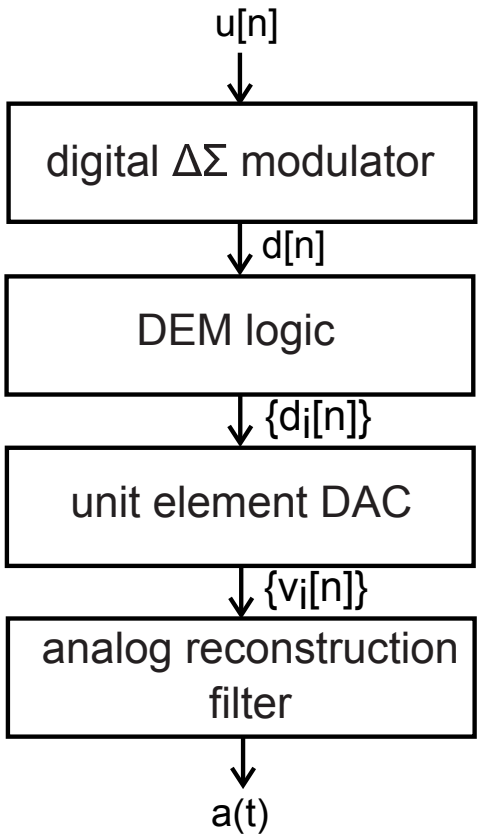


Figure 4.1: General architecture of a $\Delta\Sigma$ DAC.

The vector-quantizer (VQ) based structure [Schreier and Zhang [1995]] of Fig. 4.2, is a well known way to implement the DEM logic in Fig. 4.1.

The discrete time representation of the unit element DAC output $v_i[n]$ in the presence of mismatch and ISI errors can be written as

$$v_i[n] = (1 + \delta_i)\, d_i[n] + ISI_i[n] \tag{4.1}$$

where δ_i represents the static mismatch and $ISI_i[n]$ represents the dynamic ISI error

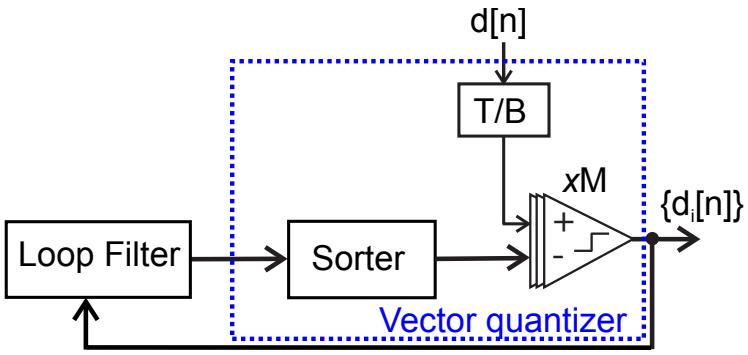


Figure 4.2: Standard vector quantizer diagram.

during transition from $d_i[n-1]$ to $d_i[n]$.

The ISI error model is shown in Fig. 4.3. For the i-th element in the DAC, the time integral of the ISI error pulses are denoted by e_{00i}, e_{01i}, e_{10i} and e_{11i} corresponding to the four transitions $(0 \to 0, 0 \to 1, 1 \to 0, 1 \to 1)$. The ISI error can then be written as

$$\begin{aligned} ISI_i[n] &= e_{00i}(1-d_i[n-1])(1-d_i[n]) \\ &+ e_{10i}d_i[n-1](1-d_i[n]) + e_{11i}d_i[n-1]d_i[n] \\ &+ e_{01i}(1-d_i[n-1])d_i[n] \\ &= e_{00i} + (e_{10i}-e_{00i})d_i[n-1] + (e_{11i}-e_{10i})d_i[n] \\ &+ (e_{10i}+e_{01i}-e_{11i}-e_{00i})(1-d_i[n-1])d_i[n] \\ &\equiv \alpha_i + \gamma_i d_i[n-1] + \beta_i d_i[n] + \epsilon_i \Gamma_i[n] \end{aligned} \tag{4.2}$$

where α_i, β_i, γ_i and ϵ_i are the normalized ISI error coefficients and given by $\alpha_i = e_{00i}$, $\beta_i = (e_{11i}-e_{10i})$, $\gamma_i = (e_{10i}-e_{00i})$ and $\epsilon_i = (e_{10i}+e_{01i}-e_{00i}-e_{11i})$. The coefficients α_i, β_i, γ_i and ϵ_i are constants which depend on the circuit im-

plementation but do not depend on $d[n]$. Their values increase with increase in f_s. $\Gamma_i[n]$ represents the up-transition sequence given by $(1 - d_i[n-1])d_i[n]$.

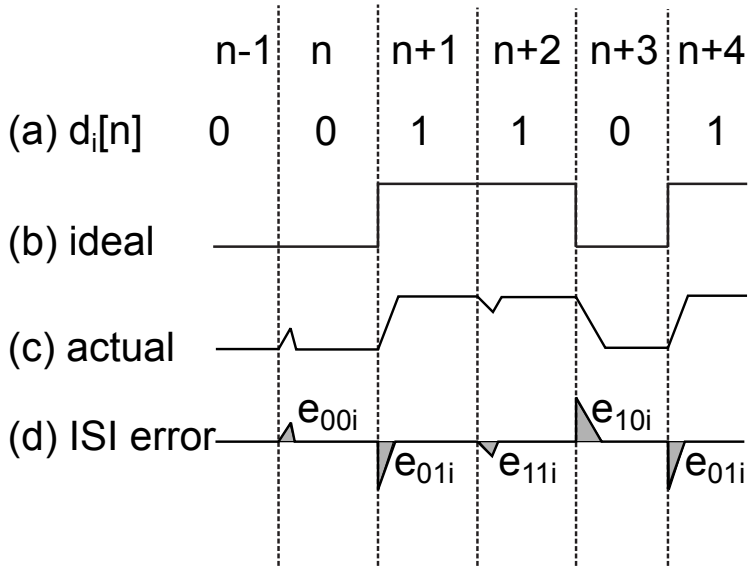


Figure 4.3: (a) 1-bit digital sequence (b) ideal DAC output (c) DAC output with ISI error (d) ISI error.

The first three terms of (4.2) represent a 2-tap filtering of $d_i[n]$ and constitute the linear part of ISI error, while the fourth term introduces nonlinearity. As has been shown in [Risbo et al. [2011]], the nonlinearity can be also associated with any one of the other 3 transitions ($0 \rightarrow 0$, $1 \rightarrow 0$, $1 \rightarrow 1$). It should be noted that in presence of static mismatch, β_i and γ_i will introduce distortion in the DAC output.

Plugging (4.2) into (4.1), we get

$$v_i[n] = \alpha_i + (1 + \delta_i + \beta_i)d_i[n] + \gamma_i d_i[n-1] + \epsilon_i \Gamma_i[n] \tag{4.3}$$

Assuming law of superposition holds, the output of M-element DAC can be written as

$$
\begin{aligned}
v[n] &= \sum_{i=1}^{M} v_i[n] \\
&= d[n] + \sum_{i=1}^{M} \alpha_i + \sum_{i=1}^{M} (\delta_i + \beta_i) d_i[n] \\
&+ \sum_{i=1}^{M} \gamma_i d_i[n-1] + \sum_{i=1}^{M} \epsilon_i \Gamma_i[n] \qquad (4.4)
\end{aligned}
$$

From (4.4), it can be seen that distortion in $v[n]$ can come from static mismatch or from nonlinear ISI error which is contributed by $\Gamma_i[n]$.

$$
\begin{aligned}
\sum_{i=1}^{M} \epsilon_i \Gamma_i[n] &= \sum_{i=1}^{M} \epsilon \left(1 + \epsilon_{ri}\right) \Gamma_i[n] \\
&= \epsilon \left(\sum_{i=1}^{M} \Gamma_i[n] + \sum_{i=1}^{M} \epsilon_{ri} \Gamma_i[n] \right) \\
&= \epsilon \left(\Gamma[n] + \sum_{i=1}^{M} \epsilon_{ri} \Gamma_i[n] \right) \qquad (4.5)
\end{aligned}
$$

where ϵ_{ri} represents the relative mismatch in ϵ_i among the different DAC elements. This model shows that for the DAC output $v[n]$ to be free of distortions, we have to ensure no distortion in $d_i[n]$ and $\Gamma_i[n]$.

Even though the ISI model assumes that law of superposition holds, in practice this maybe a simplification of the real scenario. This is because ISI error of one DAC element may influence ISI error of another DAC element. However, even with this limitation, the model is still useful as it provides key insights into ISI error and ways to reduce it.

4.4 Review of prior DEM techniques

4.4.1 Modified thermometer coding techniques

DWA has been a much used technique to address static mismatch. DWA high-pass shapes static mismatch error and thus reduces its contribution to the in-band noise. Thus, DWA is a very good technique for discrete time $\Delta\Sigma$ modulators where static mismatch is the main source of error. The strength of DWA is that it has the highest element switching activity and thus can scramble the element selection very effectively. However, it follows from the ISI model that a high element switching rate increases the ISI error. Thus, use of DWA is not beneficial for CT $\Delta\Sigma$ modulators where ISI is a major concern. From ISI perspective, thermometer coding is a very good candidate as it minimizes the element switching rate. Further, since the switching rate in thermometer coding is usually determined by the intrinsic quantization noise for high OSR and/or large out-of-band NTF gain scenarios, the correlation between DAC switching sequence and the input signal is also very low. Thus, thermometer coding does not show ISI induced distortion. This makes thermometer coding much more attractive than DWA for CT $\Delta\Sigma$ modulators in presence of ISI error. Fig. 4.4 shows the simulated transition density versus dc signal for both DWA and thermometer coding. A 32 element second-order $\Delta\Sigma$ DAC with an out-of-band NTF gain of 2 was used for the simulation. The input dc signal's amplitude was swept to get the transition density variation. It can be seen that thermometer coding has a very low transition density with very low correlation with the input. On the other hand, DWA has a large transition density and the folding of the transition density around the middle of the signal range contributes to the large

nonlinearity in $\Gamma[n]$ for DWA. Note that the transition density of DWA in Fig. 4.4 is slightly lower than the theoretical maximum of 0.5 due to the presence of random noise in the simulation which reflects real operating conditions.

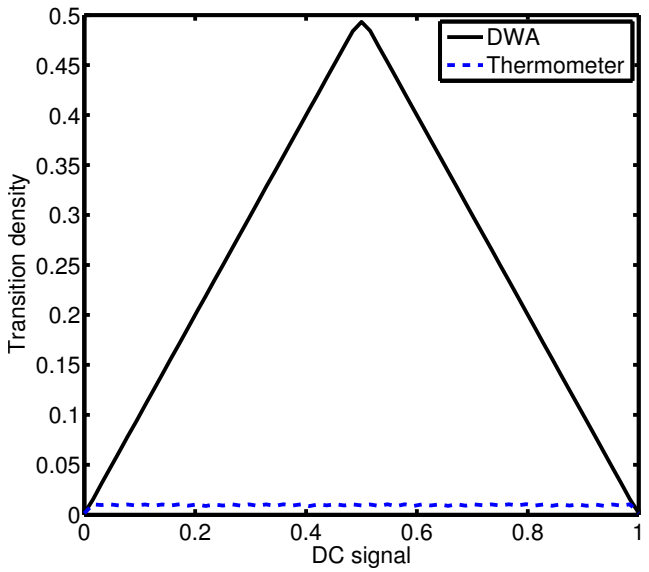


Figure 4.4: Simulated transition density versus signal amplitude for DWA and thermometer coding.

Even though thermometer coding has a very low switching activity, it still cannot handle static mismatch error. This has prompted researchers to modify the basic thermometer coding and build on it to address both static mismatch and ISI error. The randomized thermometer coding (RTC) technique of [Lee et al. [2009]] tries to keep a low element switching activity by using a modified thermometer coding. To randomize the static mismatch, the starting element of thermometer coding is changed randomly after a certain number of input samples. Thus, it tries to balance both static mismatch and ISI error. However, the element switching activity of

[Lee et al. [2009]] is still more than the basic thermometer coding as it allows more transitions to randomize element mismatch. The random swapping thermometer coding (RSTC) algorithm [Shen et al. [2010]] tries to address this limitation in the RTC technique by randomizing the element selection pattern while maintaining the same number of transitions as thermometer coding. RSTC technique does this by randomizing the start/stop position of the element selection while ensuring maximum overlap in the element selection pattern. However, it does not fully whiten static mismatch leading to increased noise floor. The technique proposed in [Wang and Sun [2014]] achieves a better randomization of element mismatch than RSTC while still having the same minimum switching activity as thermometer coding. The operation of the technique in [Wang and Sun [2014]] can be described as

1. If $d[n] = d[n-1]$, no change in the element selection pattern.
2. If $d[n] > d[n-1]$, turn on $(d[n] - d[n-1])$ unselected elements randomly.
3. If $d[n] < d[n-1]$, turn off $(d[n-1] - d[n])$ selected elements randomly.

An advantage of the technique of [Wang and Sun [2014]] over RSTC is that the DAC element usage for [Wang and Sun [2014]] is more distributed than RSTC. Thus, a DAC using the technique in [Wang and Sun [2014]] has better protection from gradient errors, and thus better performance than RSTC.

4.4.2 MMS algorithm

The MMS algorithm [Shui et al. [1999]] presents a change of perspective in addressing ISI error. Different from modified thermometer coding techniques

which rely on minimizing element transition to reduce ISI error, MMS algorithm tries to ensure that the total number of transitions is independent of $d[n]$. Making the total number of transitions independent of $d[n]$ can turn ISI error to just an offset and thus significantly improve DAC linearity. However, the MMS algorithm has the following limitations

1. It assumes that all the elements have the same values for e_{00i}, e_{01i}, e_{10i} and e_{11i}.

2. It assumes that $e_{01i} = e_{10i}$.

Inspite of these limitations, MMS algorithm represents a major advancement in the field of ISI reduction. Further, by achieving decorrelation of the total number of transitions and $d[n]$ over a large range of $d[n]$, it reduces ISI induced distortion to a great extent.

4.4.3 ISI shaping techniques

Another major advancement came in the form of the ISI shaping technique proposed in [Risbo et al. [2011]]. This technique showed that ISI error can be high-pass shaped similar to static mismatch. The technique of [Risbo et al. [2011]] achieved simultaneous ISI and mismatch shaping by using two separate loops as shown in Fig. 4.5.

ISI shaping is done by a $\Delta\Sigma$ loop which monitors the up-transition density $\Gamma_i[n]$ of each DAC element and ensures their long term average is equal to a fixed number R_{tran}. By controlling the switching activity of individual DAC elements,

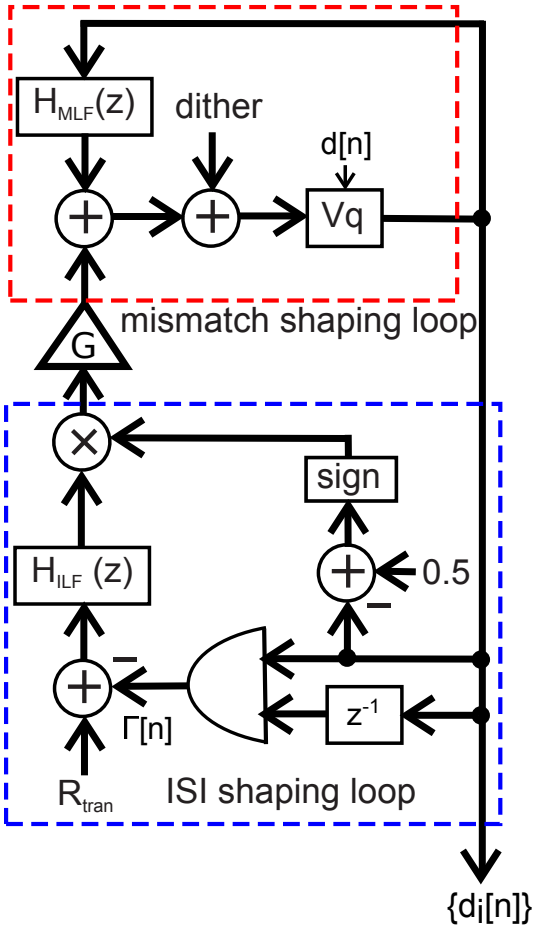


Figure 4.5: Architecture of ISI shaping technique of [Risbo et al. [2011]].

the technique of [Risbo et al. [2011]] solves the limitations of the MMS technique in that it does not require e_{01i} to be equal to e_{10i} and it does not require ISI errors of each DAC element to match.

4.5 Proposed DEM techniques

4.5.1 Modified thermometer coding

While the techniques of [Shen et al. [2010]; Lee et al. [2009]; Wang and Sun [2014]] all randomize static mismatch and ISI error simultaneously, they share the limitation of not high-pass shaping static mismatch error. To address this limitation, we propose a modified thermometer coding technique which introduces the capability to high-pass shape static mismatch while maintaining DAC switching activity similar to thermometer coding. We call this technique thermometer coding with mismatch shaping (TCMS). The TCMS algorithm builds directly on the work of [Wang and Sun [2014]]. Fig. 4.6 shows the architecture of the proposed DEM. The structure is similar to the conventional VQ structure. The only difference is the insertion of an additional feedback loop with a gain G.

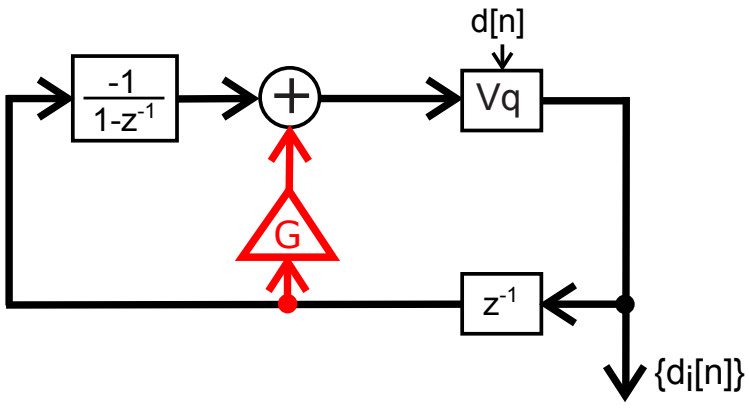


Figure 4.6: Architecture of TCMS DEM.

The operation of the TCMS technique can be divided into 3 cases.

1. If $d[n] = d[n-1]$, no change in the element selection pattern.

2. If $d[n] > d[n-1]$, turn on $(d[n] - d[n-1])$ unselected elements that have been least frequently used.

3. If $d[n] < d[n-1]$, turn off $(d[n-1] - d[n])$ selected elements that have been most frequently used.

This way, the transition rate of TCMS is as low as that of thermometer coding, while still shaping static mismatch in the DAC. There is a design trade-off in selection of the feedback loop gain, G. If $G = 0$, the DEM is equivalent to a first order VQ, or DWA, which only shapes the static mismatch, but has a large ISI error. If G is high, the element transition rate starts approaching that of pure thermometer coding, thus having low ISI error but not shaping the static mismatch. This trade-off can also be seen from Table 4.1. The simulations for Table 4.1 are performed with a 15-element third-order $\Delta\Sigma$ DAC with a maximum out-of-band noise transfer function (NTF) gain of 6 and a -3 dBFS input.

Table 4.1: Variation of SNDR with G

	G					
SNDR(dB)	0	0.1	1	10	100	1000
0.5% static, 0.1% ISI	66	73.5	77.4	72.4	71.4	71.4
0.1% static, 0.1% ISI	67.4	74.9	78.8	80.8	79.9	79.9
0.1% static, 0.5% ISI	53.3	60.7	64.7	72.1	71.7	71.7
0.3% static	103.1	99.7	95	73.8	72.9	72.9
0.3% ISI	58.5	66	69.9	77.7	77.5	77.5

As can be seen from Table 4.1, a lower value of G increases the signal-to-noise-and-distortion ratio (SNDR) if static mismatch is the dominant source of DAC non-ideality. If ISI error dominates, SNDR increases with G. At very high

G, the proposed technique becomes the same as basic thermometer coding, and no further improvement is seen in SNDR for ISI error limited DAC.

Table 4.2: Variation of up-transition density with G

	G					
	0	0.1	1	10	100	1000
up-transition density	0.28	0.19	0.13	0.05	0.05	0.05

Table 4.2 shows the variation of up transition density with G. The simulation conditions used to generate Table 4.2 are the same as for Table 4.1. It can be seen from Table 4.2 that at very high G, the up-transition density does not change with G. This is because the transition density of TCMS becomes the same as that of basic thermometer coding at very high G.

Fig. 4.7 shows the simulated selection pattern $\{d_i[n]\}$ for thermometer coding, the technique of Shen et al. [2010], and the proposed TCMS technique. All of these three coding schemes have the same element transition activity $\Gamma[n]$, but the selection pattern $\{d_i[n]\}$ for the TCMS technique is more random. It also ensures that the total number of usages for all elements are the same.

To verify the efficacy of the static mismatch shaping performance of the proposed TCMS and compare it with basic thermometer coding and RSTC technique [Shen et al. [2010]], the spectra of the selection pattern $\{d_i[n]\}$ for the three techniques are plotted in Fig. 4.8. Note that the spectrum of $\{d_i[n]\}$ refers to the spectrum of $d_i[n]$ averaged over all the elements. A 32-element fifth-order $\Delta\Sigma$ DAC with a maximum out-of-band NTF gain of 6 was used for the simulation. An input of -3 dBFS and frequency of $f_s/64$ was used. G was set to 10 for the simula-

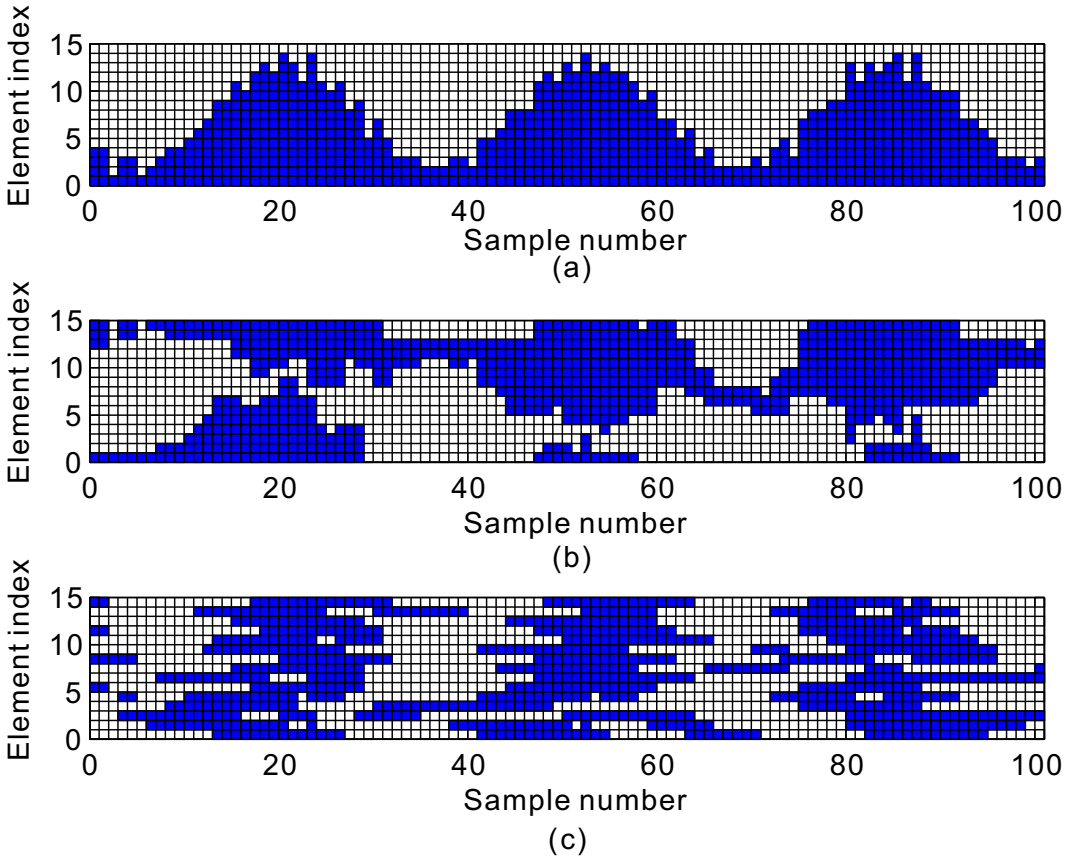


Figure 4.7: Element selection pattern for (a) basic thermometer coding, (b) technique of Shen et al. [2010], and (c) proposed TCMS technique.

tion. The basic thermometer coding has a lot of tones because its element selection pattern is highly correlated with the input $d[n]$. Both [Shen et al. [2010]] and the TCMS technique do not show harmonics due to randomization of the element selection pattern. The TCMS technique also shapes the mismatch error and has a much lower in-band error component than the RSTC technique of [Shen et al. [2010]].

To get an understanding of the noise-shaping characteristic of the proposed

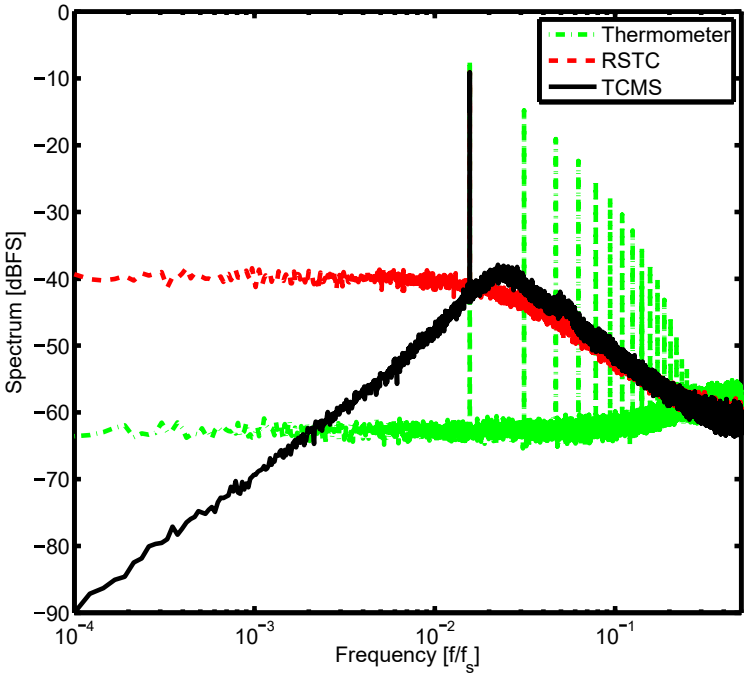


Figure 4.8: Spectra of $\{d_i[n]\}$ for thermometer, RSTC [Shen et al. [2010]] and TCMS.

DEM, let us model the VQ by a linear gain K and a quantization error q.

$$\begin{aligned} d_i &= \left(\frac{z^{-1}}{1-z^{-1}}(d-d_i)+Gz^{-1}d_i\right)K+q \\ \Longrightarrow\ d_i &= \left(\frac{z^{-1}K}{1+(K-1-GK)z^{-1}+GKz^{-2}}\right)d \\ &+ \left(\frac{1-z^{-1}}{1+(K-1-GK)z^{-1}+GKz^{-2}}\right)q \\ &\equiv H_1(z)d+H_2(z)q \end{aligned} \tag{4.6}$$

It can be seen from (4.6) that $H_2(z)$ has a first-order shaping at low frequencies and a low gain at high frequencies. The gain of $H_2(z)$ at high frequencies ($z=-1$) is $2/(2-K+2GK) \approx 1/GK$. For high values of G, this gain will

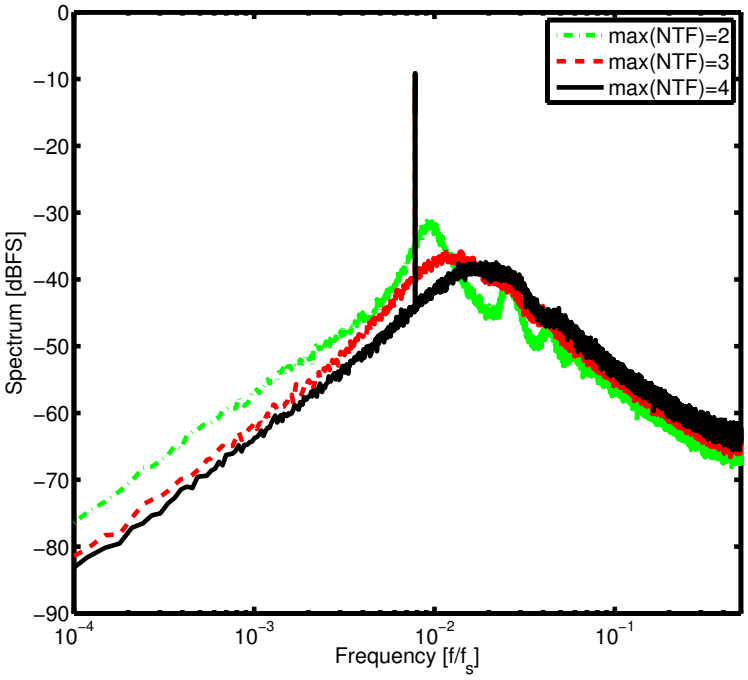


Figure 4.9: Spectra of $\{d_i[n]\}$ for TCMS for different maximum NTF gains.

be low. This can also be seen from the spectrum in Fig. 4.8. A low gain at high frequency indicates a low transition rate.

It should be pointed here that the mismatch shaping performance of TCMS depends on the randomization of DAC element selection. The randomization depends heavily on the quantization noise. Thus, it is expected that increase in maximum out-of-band NTF gain will improve the mismatch shaping performance of the DEM. This can also be seen from Fig. 4.9 which shows that for higher out-of-band NTF gain, TCMS will achieve a lower in-band noise when only static mismatch is present.

4.5.2 Enhanced ISI shaping

The ISI shaping technique of [Risbo et al. [2011]] monitors only the up transition and not the down transition. A better ISI shaping can be obtained by taking both the up and down transitions into account. The improvement in ISI shaping performance can be intuitively understood by recognizing a down transition as an intermediate state between two up transitions. Thus, counting down transition can double the resolution of transition rate count, and hence improve the ISI shaping performance. We will call this technique as enhanced ISI shaping (EIS) technique. Since the up transition density is equal to the down transition density, shaping the total transition sequence guarantees that both up as well as down transition sequences are shaped. The architecture monitoring both the transitions is shown in Fig. 4.10.

Comparison of the ISI shaping techniques of [Risbo et al. [2011]] and EIS is shown in Fig. 4.11 for a -3 dBFS input. First order filter is used for both static mismatch and ISI shaping loops. A 32-element DAC with 1% static mismatch and 3% ISI error is used for the comparison. At an OSR of 16, the EIS technique shows 4 dB higher SNDR than the ISI shaping technique of [Risbo et al. [2011]]. This validates the idea of monitoring both up and down transitions in order to achieve a better ISI shaping performance.

Since the ISI shaping and mismatch shaping loops are coupled, it is meaningful to study the impact of the relative strength of the two loops on the shaping result by varying G. The result is shown in Fig. 4.12. It shows that as the ISI loop strength increases with G, both the 2nd-order distortion and total in-band component of $\Gamma[n]$ decrease [see Fig. 4.12(a) and (b)], leading to an improved ISI shaping

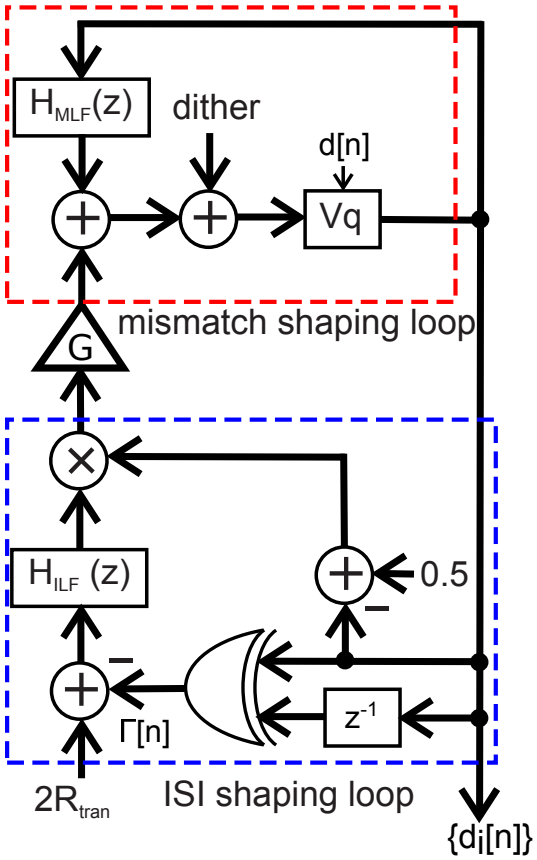


Figure 4.10: Architecture of DEM using EIS.

result. However, the drawback is that the mismatch shaping result is worsened due to an increase in the total in-band component of $d[n]$ [see Fig. 4.12(c)]. Thus, there is a clear trade-off between the ISI shaping effect and the mismatch shaping effect.

Note that the proposed EIS technique always shows a better performance compared to that of [Risbo et al. [2011]], but the advantage becomes clearer at larger G. This is easy to understand. When G is small, the mismatch shaping loop dominates the overall loop behavior. Since both techniques use the same mismatch

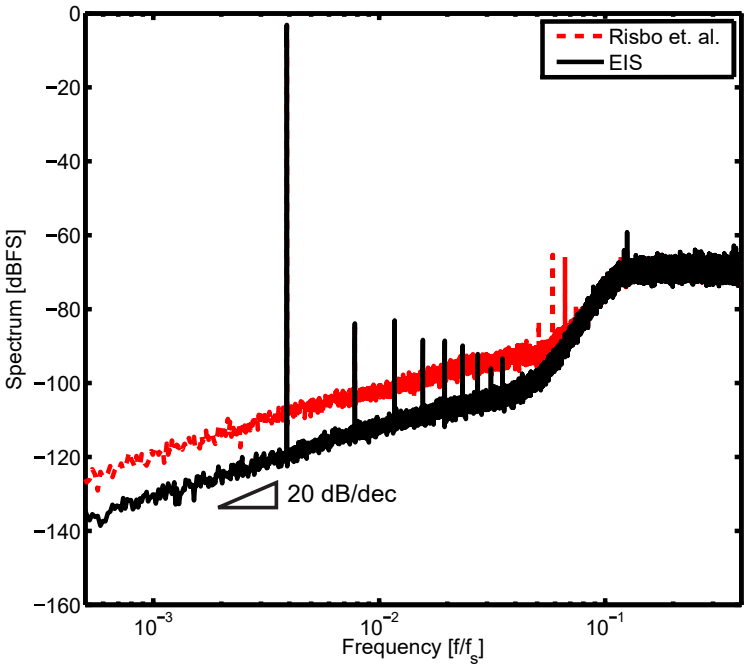


Figure 4.11: DAC output spectra comparison between ISI shaping technique of [Risbo et al. [2011]] and EIS.

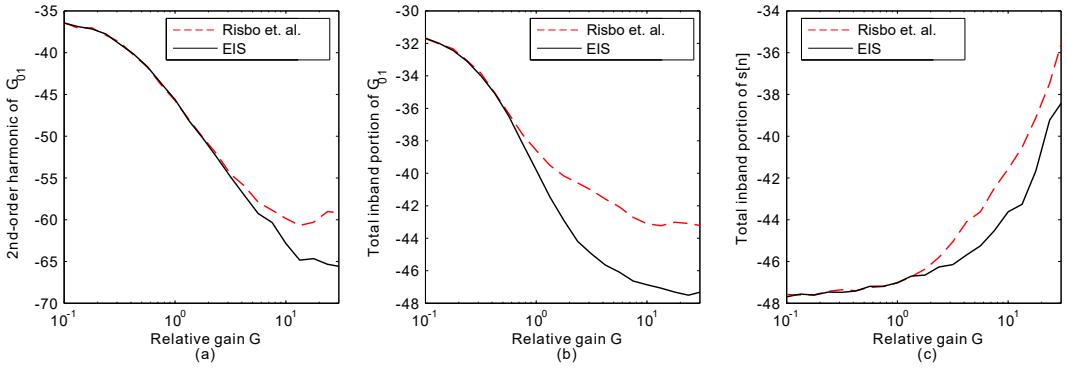


Figure 4.12: Simulation results as a function of the relative gain G.

shaping loop, there is very small difference between them. By contrast, when G is large, the ISI shaping loop dominates over the mismatch shaping loop, and thus, there is a big difference in performance. At large G, the proposed technique can

lower the ISI induced 2nd-order distortion by as much as 5 dB, which is significant especially given almost no additional hardware cost for the EIS technique, compared to the technique of [Risbo et al. [2011]] .

It should be pointed here that a limitation of both the ISI shaping technique of [Risbo et al. [2011]] and EIS is the presence of distortion at large signal amplitudes. This is also evident from Fig. 4.11. The distortion comes from the coupling between ISI and mismatch shaping loops. At large signal amplitudes, this coupling is very tight and causes the instantaneous transition density to be dependent on $d[n]$ even though the average transition density is independent of $d[n]$. This is unlike the thermometer based techniques which show excellent decorrelation between instantaneous transition density and $d[n]$. As an example, $\Gamma[n]$ of the ISI shaping technique of [Risbo et al. [2011]] and TCMS technique is shown in Fig. 4.13. An input amplitude of -3 dBFS was used for the simulation. It can be seen that the TCMS technique shows a much lower second harmonic than ISI shaping technique of [Risbo et al. [2011]]. This is due to the decorrelation between $\Gamma[n]$ and $d[n]$ for the TCMS technique. Thus, Fig. 4.13 also highlights the limitation of the ISI shaping technique [Risbo et al. [2011]], namely, increased distortion at large signal amplitudes.

4.5.3 ISI shaping with signal independent element transition rates

To address the limitations of TCMS and EIS techniques, we propose another DEM that achieves simultaneous mismatch and ISI shaping while ensuring that the total number of transitions remains independent of $d[n]$. We will call this technique

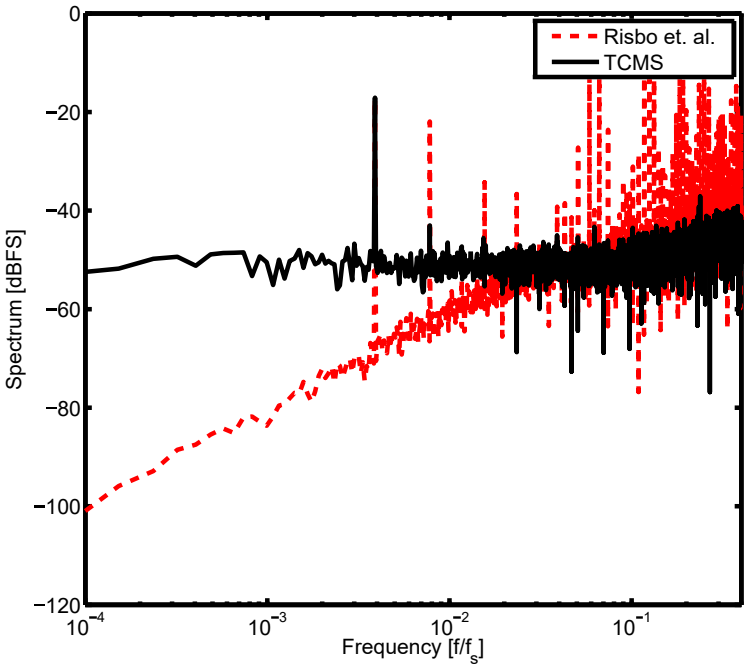


Figure 4.13: Spectra of $\Gamma[n]$ for ISI shaping technique [Risbo et al. [2011]] and TCMS.

as simultaneous mismatch and ISI shaping (SMIS). The key idea behind this algorithm is to vary the instantaneous number of transitions between three adjacent integers, $L-1$, L and $L+1$. To see how this can be done, let us use $K[n]$ to denote the total number of up and down transitions. The total number of up transitions, $\Gamma[n]$, can then be written as

$$\Gamma[n] = \frac{K[n] + d[n] - d[n-1]}{2} \tag{4.7}$$

It can be seen from (4.7) that if $K[n]$ is high-pass shaped and uncorrelated with $d[n]$, ISI error can be shaped without any distortion. $K[n]$ cannot be a constant as $(K[n] + d[n] - d[n-1])$ has to be even, which means that $K[n]$ cannot be completely independent of $d[n]$. Assuming the long term average of $K[n]$ to be L, $K[n]$

can be chosen in the following way to ensure a good decorrelation with $d[n]$:

1. if $(L + d[n] - d[n-1])$ is even, $K[n] = L$.

2. if $(L + d[n] - d[n-1])$ is odd, a $\Delta\Sigma$ modulator sets $K[n]$ to $L-1$ or $L+1$.

The hardware implementation for generation of $K[n]$ and $\Gamma[n]$ is shown in Fig. 4.14.

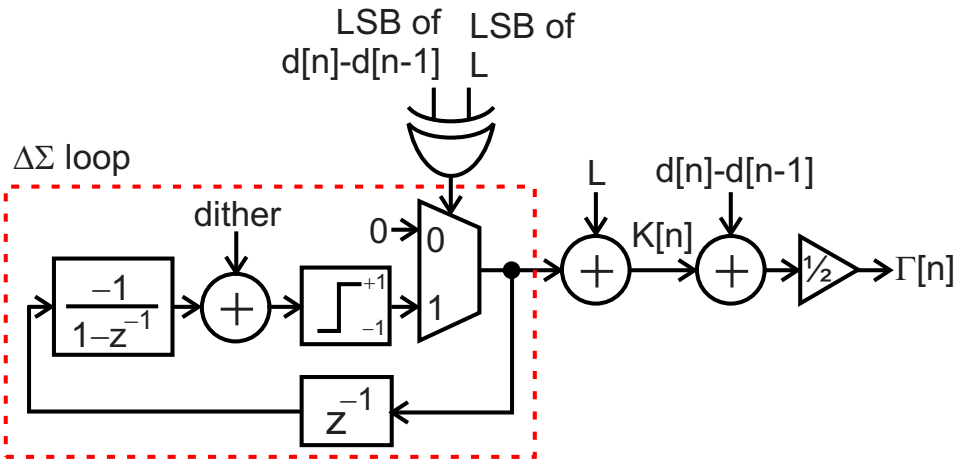


Figure 4.14: Circuit block diagram that generates first-order high-pass shaped $K[n]$ and $\Gamma[n]$.

An XOR gate checks parity of $(L + d[n] - d[n-1])$. If it is even, the $\Delta\Sigma$ modulator produces 0 and $K[n]$ is set to L. If $(L + d[n] - d[n-1])$ is odd, $K[n]$ is set to $L \pm 1$ according to the output of the modulator. A small and efficient dither is added to remove spurs [Sanyal and Sun [2011]].

Once $K[n]$ is generated, $\Gamma[n]$ is obtained from (4.7), and the element selection is decided every cycle in the following manner:

1. turn on $\Gamma[n]$ unselected elements that have been least frequently used.

2. keep on $(d[n] - \Gamma[n])$ selected elements that have been least frequently used.

There are requirements on $d[n]$ and $\Gamma[n]$ in order for this algorithm to work. First, $(d[n-1] + \Gamma[n]) \leq M$. If this inequality is violated, step 1) of the algorithm is unrealizable, as the total number of unselected elements is smaller than $\Gamma[n]$. By plugging in (4.7), this inequality is essentially

$$K[n] \leq (2M - d[n] - d[n-1]) \tag{4.8}$$

The second requirement is $0 \leq (d[n] - \Gamma[n]) \leq d[n-1]$. If violated, step 2) of the algorithm is invalid because there is insufficient number of elements to keep on. Again plugging in (4.7), we have

$$(d[n] - d[n-1]) \leq K[n] \leq (d[n] + d[n-1]) \tag{4.9}$$

These requirements impose constraints on $K[n]$ and the range of $d[n]$. The lower limit for $K[n]$ is $(d[n] - d[n-1])$. In a low-pass $\Delta\Sigma$ modulator with high OSR, the range of $(d[n] - d[n-1])$ is typically set not by the signal but by the noise transfer function. Thus, this limit essentially states that $K[n]$ or L must be equal or greater than the maximum NTF gain. For example, if $\max\{|NTF(\omega)|\} = 2$, we have $L \geq 2$. Note that for a $\Delta\Sigma$ modulator with low OSR, the maximum value of $(d[n] - d[n-1])$ may be larger than $\max\{|NTF(\omega)|\}$. In such a case, L needs to be set even larger. Similarly, we can derive the constraints on the range of $d[n]$ from $K[n] \leq (d[n] + d[n-1])$ and $K[n] \leq (2M - d[n] - d[n-1])$. They are

equivalent to $K[n] \leq (d[n] + d[n-1]) \leq (2M - K[n])$. Thus, the maximum range for $d[n]$ is smaller than $[0, M]$. For example, if $M = 32$ and $L = 2$, we have $1 \leq d[n] \leq 31$. This constraint is mild as it is only about 1 dB loss in the signal swing. Only if $\max\{|NTF(\omega)|\}$ is large and M is small simultaneously, the constraint will become tighter. It should be noted here that a moderate value of $\max\{NTF(\omega)\}$ (e.g., 2 or 3) is sometimes preferred over a large $\max\{NTF(\omega)\}$. For a $\Delta\Sigma$ ADC, a moderate out-of-band NTF gain results in smaller input swing for the first-stage integrator, thereby improving its linearity and relaxing the slew rate requirement. For a $\Delta\Sigma$ DAC, it relaxes the performance requirement of the analog reconstruction filter. Moreover, a moderate out-of-band gain together with a large M can reduce the amount of out-of-band noise, and thus, reduce the clock jitter sensitivity. In addition to high-speed CT $\Delta\Sigma$ modulators, ISI reduction is also of great importance in high-resolution but low-speed ADCs/DACs, such as those used in high quality audio applications. A large value of M is common in high-quality audio DACs. As an example, the modulator in [Risbo et al. [2011]] has a segmented DAC with both the primary and secondary DACs having 32 elements each. In this scenario, the signal swing loss is still small.

It should also be pointed out here that the restriction on the range of $d[n]$ is actually a manifestation of the trade-off between redundancies in element selection and ISI error reduction. There should be adequate redundancy in the DAC for the DEM to select elements so as to reduce ISI error. MMS algorithm [Shui et al. [1999]] also has a similar restriction on the range of $d[n]$. The ISI shaping technique [Risbo et al. [2011]] allows for a larger input swing but suffers from increased

distortion.

Hardware implementation of the proposed DEM with SMIS is shown in Fig. 4.15. The modification from the DEM in TCMS is the presence of an additional VQ and an additional direct feedback path. A high value of G ensures that the vector quantizer $Vq1$ gives higher priority to elements that are not selected previously and the vector quantizer $Vq2$ gives higher priority to previously selected elements. For efficient hardware implementation, the two summers before $Vq1$ and $Vq2$ can be removed and replaced by a sign bit for inputs to $Vq1$ and $Vq2$. For previously selected elements, the sign bit will be set to '1' for inputs to $Vq2$ and set to '0' for the remaining inputs to $Vq2$. The sign bit for inputs to $Vq1$ are complementary to the inputs to $Vq2$. It should be noted here that G cannot be too small as a very small value of G will violate the condition $d[n] = \sum_{i=1}^{M} d_i[n]$ and result in a high quantization noise. As long as G is sufficiently high, the value of G does not affect the trade-off between static mismatch and ISI error. This can also be seen from the results in Table 4.3. A fifth-order $\Delta\Sigma$ DAC with maximum out-of-band NTF gain of 3 was used for the simulation. A -3 dBFS input at frequency of $f_s/1332$ was used. It can be seen that if ISI is the dominant source of nonlinearity, then the presence of the feedback path with gain G results in a better SNDR than if static mismatch is the dominant source of output nonlinearity. However, change in the value of G does not present any trade-off between static mismatch and ISI error provided that the condition $d[n] = \sum_{i=1}^{M} d_i[n]$ is not violated.

Fig. 4.16 shows the spectra of up-transition sequence $\Gamma[n]$ for ISI shaping technique of [Risbo et al. [2011]] and SMIS for an input amplitude of -3 dBFS. A

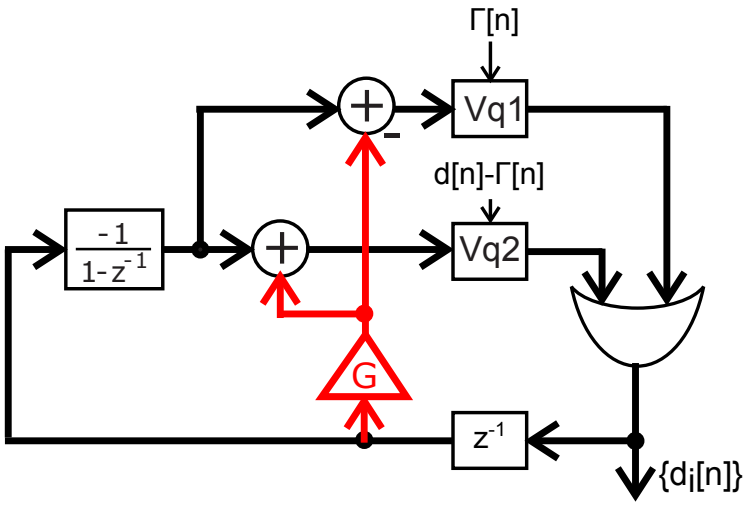


Figure 4.15: Implementation of the proposed DEM with SMIS.

Table 4.3: Variation of SNDR with G

	G			
SNDR(dB)	5	10	100	1000
1% static, 1% ISI	86.4	86.8	86.8	86.0
5% static, 1% ISI	71.7	73.0	73.1	73.2
1% static, 5% ISI	85.4	85.9	85.7	86.3
3% static	76.6	76.7	76.3	76.9
3% ISI	101.7	101.7	101.5	101.7

32-element DAC with 1% static mismatch error and 1% ISI error was used for the simulation. A maximum out-of-band NTF gain of 3 was used. As can be seen from Fig. 4.16, the SMIS technique achieves a good decorrelation between $K[n]$ and $d[n]$ and hence, does not show harmonic distortion like the ISI shaping technique of [Risbo et al. [2011]].

The SMIS technique monitors only the total number of transitions $K[n]$ as opposed to the ISI shaping technique [Risbo et al. [2011]] that monitors the

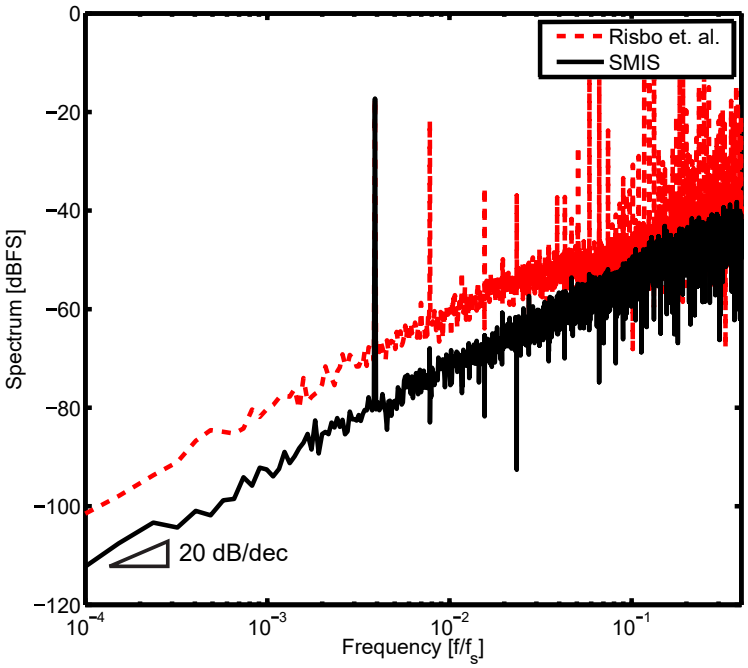


Figure 4.16: Spectra of $\Gamma[n]$ for ISI shaping technique of [Risbo et al. [2011]] and SMIS.

transition of each DAC element. The result is having less hardware complexity at the expense of not shaping the transition sequence for each element even though the overall transition sequence is shaped. This can also be seen from Fig. 4.17 which shows the spectra of $\Gamma_i[n]$ for ISI shaping technique of [Risbo et al. [2011]] and SMIS. The simulation conditions are the same as used for Fig. 4.16. $\Gamma_i[n]$ for the SMIS technique is not shaped even though $\Gamma[n]$ is shaped. The limitation of not shaping $\Gamma_i[n]$ is an increased noise floor at low frequencies in presence of mismatch in ISI error between the different DAC elements. Note that the spectrum of $\Gamma_i[n]$ shows peaks at frequencies of $k \cdot f_s \cdot L/(2M)$ where k is an integer. The reason is that on an average $L/2$ new DAC elements are turned on every cycle. Since there

are M elements in the DAC, each $d_i[n]$ takes on average $2M/L$ cycles to repeat its pattern. Since, $\Gamma_i[n] = (1 - d_i[n-1])d_i[n]$, each $\Gamma_i[n]$ also repeats every $2M/L$ cycles on average. This leads to noise peaks at $k \cdot f_s \cdot L/(2M)$.

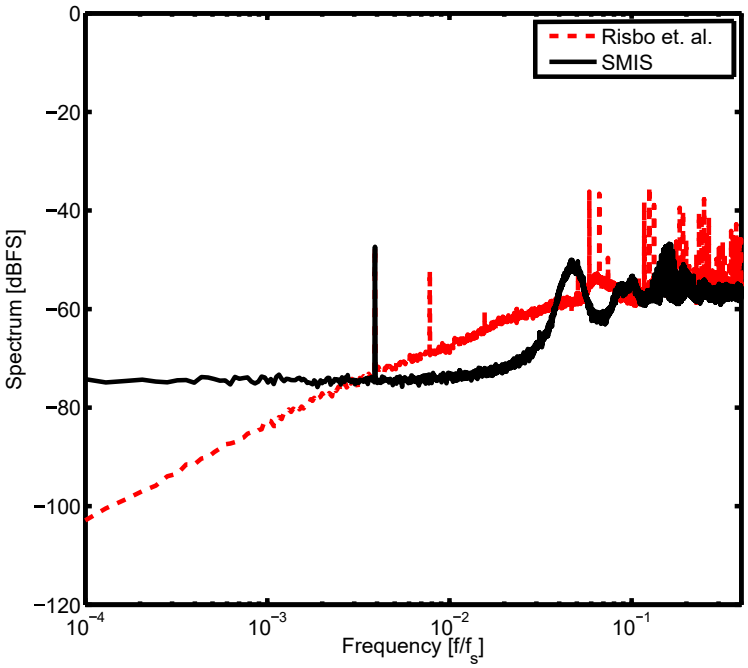


Figure 4.17: Spectra of $\Gamma_i[n]$ for ISI shaping technique [Risbo et al. [2011]] and SMIS.

Note that presence of noise peaks will increase in-band noise. Thus, there is a trade-off with respect to the choice of L. A higher value of L will increase the element switching rate and push the noise peaks away. This comes at the expense of reducing the range of $d[n]$ and degrading the redundancy available for ISI shaping. Note that this is similar to the trade-off in DWA which has the highest element switching rate, and hence, the best first-order static mismatch shaping, but also the worst ISI error.

The limitation of not shaping $\Gamma_i[n]$ can be solved by keeping track of the transition rates of each DAC element. This can be done by modifying the DEM in Fig. 4.15 as shown in Fig. 4.18.

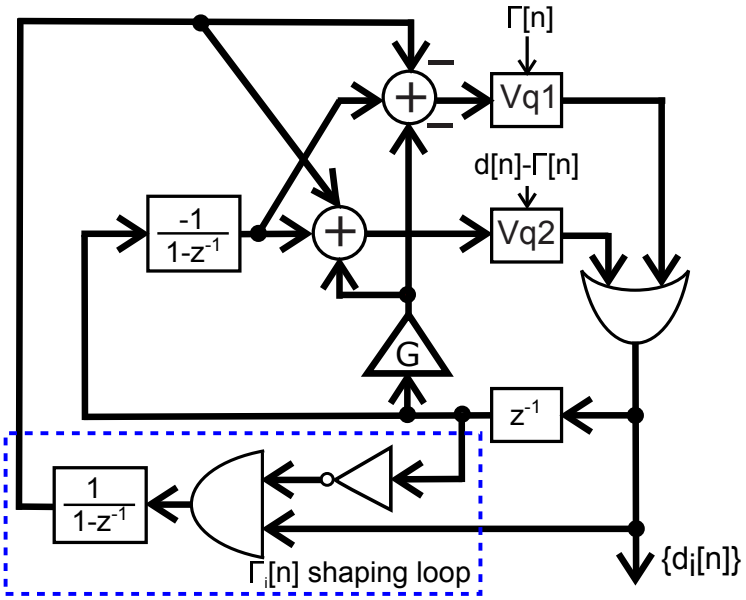


Figure 4.18: Architecture of SMIS with $\Gamma_i[n]$ shaping.

The modification from the architecture in Fig. 4.15 are the two feedback loops that take into account the accumulation of up-transition rate for each DAC element. If any element in the DAC has made many up-transitions in previous cycles, the feedback loop will lower the priority for selection of the element by $Vq1$, and the feedback loop will increase the priority for selection of the element by $Vq2$. Thus, if an element in the DAC has a high accumulated $\Gamma_i[n]$, the proposed DEM tries to ensure that $d_i[n]$ does not make a transition in the next cycle. As a result, the long term average of $\Gamma_i[n]$ is identical for all elements leading to a high-pass shaped spectrum. Henceforth, the modified architecture with $\Gamma_i[n]$ shaping

will be referred to as modified simultaneous mismatch and ISI shaping (MSMIS) technique.

The element selection pattern every cycle is then decided in the following manner:

1. $\Gamma[n]$ unselected elements are turned on that have been least frequently used and have the lowest accumulated $\Gamma_i[n]$.

2. $(d[n] - \Gamma[n])$ selected elements are kept on that have been least frequently used and have the highest accumulated $\Gamma_i[n]$.

The total number of transitions, $K[n]$, as a function of time is shown in Fig. 4.19. It can be clearly seen that $K[n]$ varies between $L - 1$, L, and $L + 1$. The spectra of $K[n]$ for different L values are shown in Fig. 4.20. The first-order shaping of $K[n]$ can be clearly seen from Fig. 4.20. The absence of any tones in Fig. 4.20 show that $K[n]$ has good decorrelation with $d[n]$.

The spectra of $\Gamma_i[n]$ for SMIS and MSMIS are shown in Fig. 4.21. A 32-element DAC, with an input of -3 dBFS was used for the simulation. A static mismatch error with a standard deviation of 1% and an ISI error with a mean of 1% and standard deviation of 1% was used. The first-order shaping of $\Gamma_i[n]$ for MSMIS can be clearly seen.

Fig. 4.22 shows the spectra of the DAC output for the techniques of SMIS and MSMIS. The same simulation conditions as for Fig. 4.21 were used. It can be clearly seen from Fig. 4.22 that the MSMIS technique has a lower in-band noise

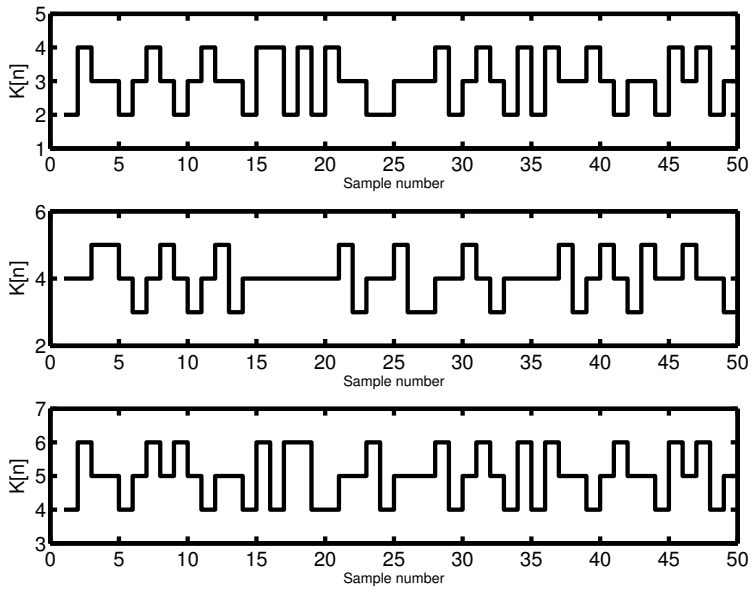


Figure 4.19: $K[n]$ as a function of time for (a) $L = 3$ (b) $L = 4$ (c) $L = 5$.

and maintains in-band noise shaping even in the presence of mismatch between ISI errors in the DAC elements. These simulation results demonstrate that MSMIS can high-pass shape static mismatch and ISI error of each DAC element.

4.5.4 Hardware complexity

Compared to the technique of SMIS, the technique of MSMIS has an additional feedback loop with integrator and logic gates. This is a small increase in terms of hardware cost, specially for advanced technology nodes. The architecture of MSMIS has two vector quantizers. Each VQ has to perform a sorting of M elements which can be hardware intensive when M is large. As M increases, the hardware complexity increases in a super-linear fashion. To reduce the hardware complexity, the tree-structure of [Galton [1997]] can be adopted. Fig. 4.23 shows

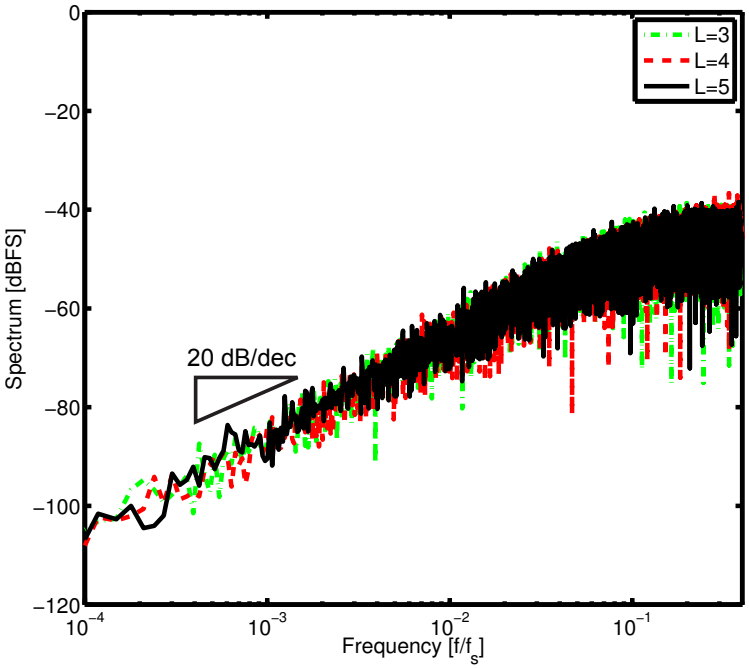


Figure 4.20: Spectra of $K[n]$ for different L values.

an example for $M = 32$. A splitter separates $d[n]$ into two 4-bit paths. Thus, two 4-bit sorters are needed instead of a 5-bit sorter which reduces the hardware complexity considerably. To use this splitting technique, each path has to ensure an average $L/2$ transitions to keep the overall number of transitions at L.

4.5.5 Second-order $\Gamma_i[n]$ shaping

The proposed technique can be extended to achieve higher order mismatch and ISI shaping. Fig. 4.24 shows the architecture for second-order mismatch and ISI shaping with the proposed technique. The filter used for second-order shaping of $\Gamma_i[n]$ is similar to the filter structure used in higher order VQ as shown in [Sun [2011]]. Fig. 4.25 shows the implementation of second-order high-pass shaped

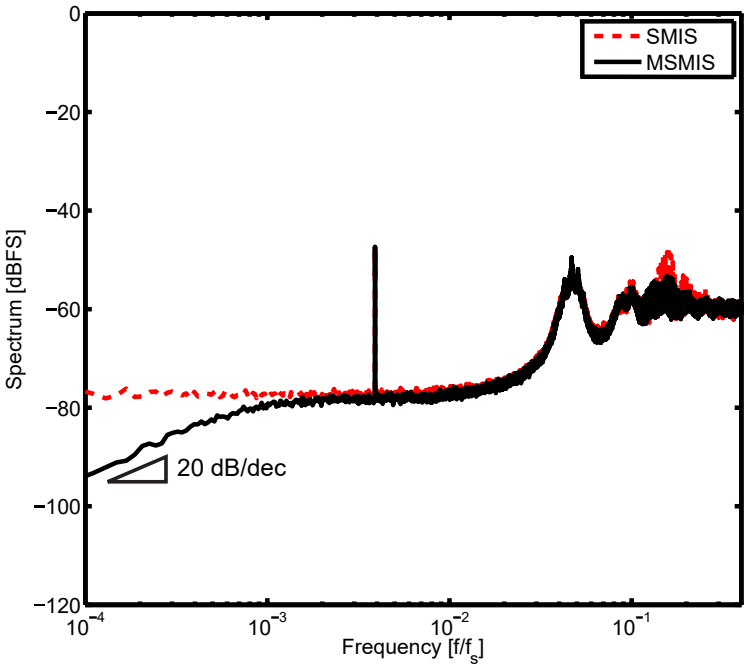


Figure 4.21: Spectra of $\Gamma_i[n]$ for SMIS and MSMIS techniques.

$K[n]$ generation block.

Fig. 4.26 shows second-order shaped $\Gamma_i[n]$ and $d_i[n]$ obtained using the architecture of Fig. 4.24. The second-order shaping can be clearly seen.

4.6 Simulation results

To compare the proposed technique with the existing techniques, a 32-element, fifth-order $\Delta\Sigma$ DAC was used and 2^{17} point discrete-time simulation was performed. A maximum out-of-band NTF gain of 3 and input amplitude of -3 dBFS was used. The $\Delta\Sigma$ modulator is designed and optimized by using the Matlab $\Delta\Sigma$ modulator toolbox [Schreier and Zhang [1995]]. An input signal frequency of

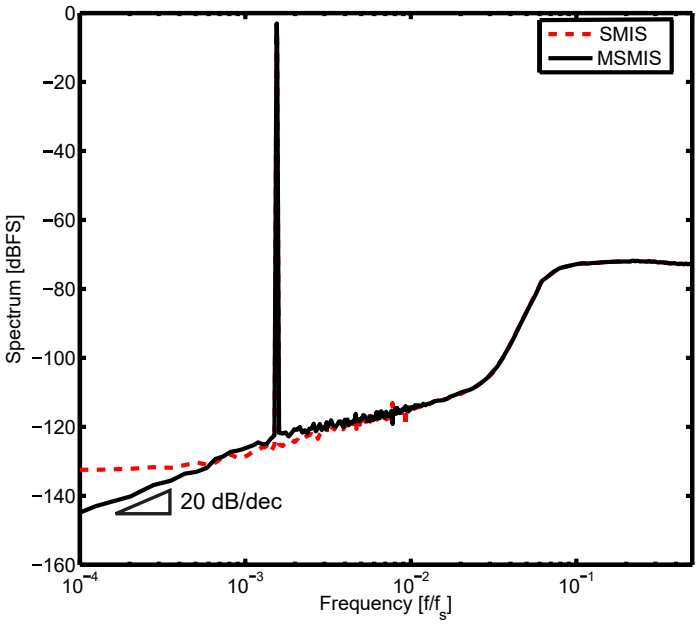


Figure 4.22: Output spectra for SMIS and MSMIS techniques.

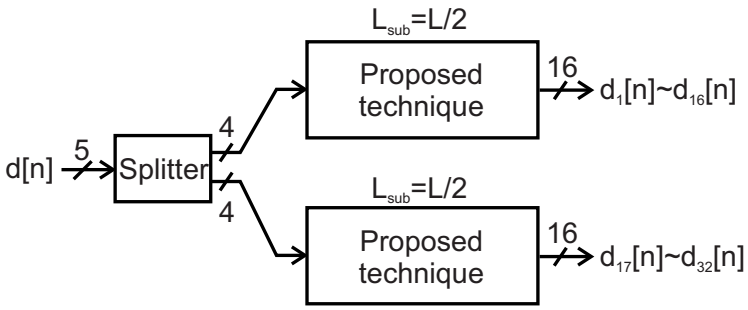


Figure 4.23: Implementation of the MSMIS technique with reduced hardware complexity.

$f_s/2664$ and OSR of 64 was used. The DAC elements are assumed to have a static mismatch with a zero mean and standard deviation of 1%. The ISI error is assumed to have a mean of 2% with a standard deviation of 1%. Thermal noise is added so that the thermal noise limited signal-to-noise ratio (SNR) at an OSR of 64 is 103.7

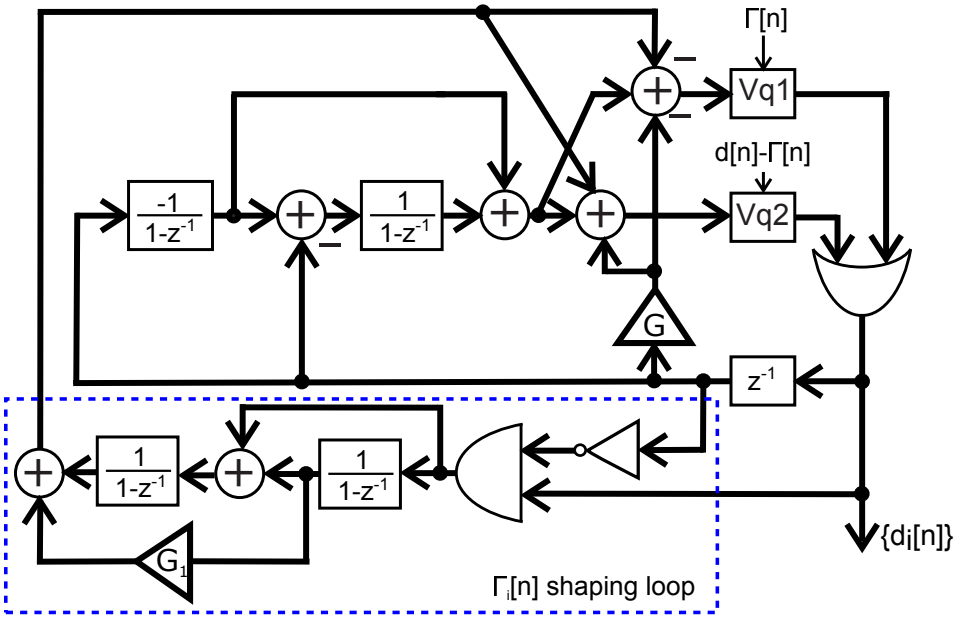


Figure 4.24: Second-order mismatch and ISI shaping with MSMIS technique.

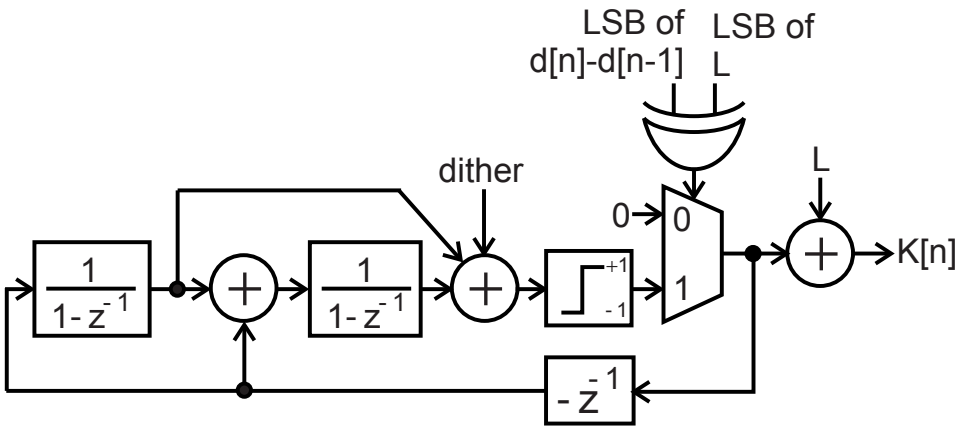


Figure 4.25: Second-order shaped $K[n]$ generation technique.

dB.

Fig. 4.27 shows the performance of the various DEM techniques. The basic thermometer coding minimizes the ISI error but shows a lot of harmonics due to

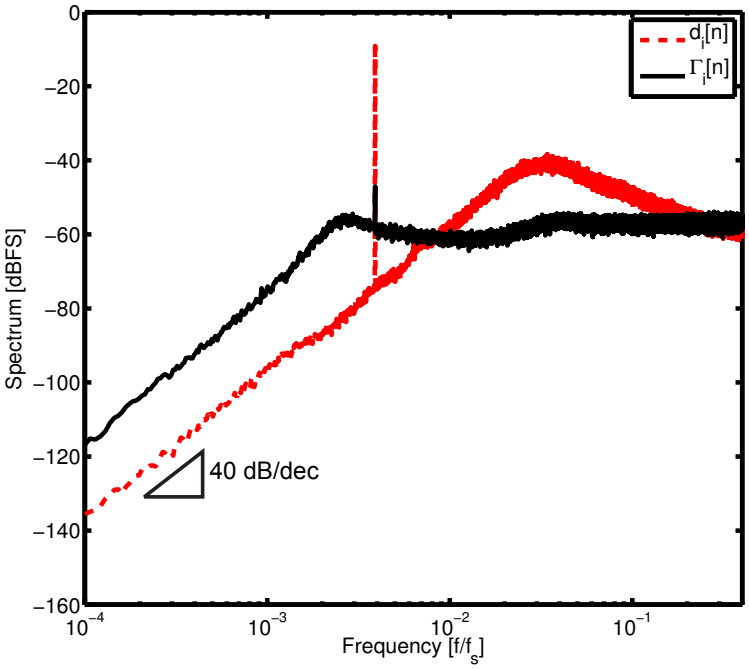


Figure 4.26: Spectra of $\Gamma_i[n]$ and $d_i[n]$ for second-order mismatch and ISI shaping with the MSMIS technique.

static mismatch in the DAC elements and has an SNDR of 55.3 dB and SFDR of 60.7 dB. The random element selection technique whitens the static mismatch error, but cannot handle ISI error. As a result, its SNDR is reduced to 48.9 dB and the SFDR is 52.2 dB. DWA shapes the static mismatch error, but has a very large ISI error due to the increase in element switching rate. Thus, it shows a low SNDR of 41.2 dB and an SFDR of 44.5 dB. Second-order DEM has lower element switching rate than DWA, but its in-band noise is still dominated by ISI induced distortions. It has an SNDR of 48 dB and SFDR of 51.1 dB. The RSTC technique [Shen et al. [2010]] whitens both the static mismatch and ISI error and has an SNDR of 53.7 dB and an SFDR of 76.2 dB which is better than pure thermometer coding. The

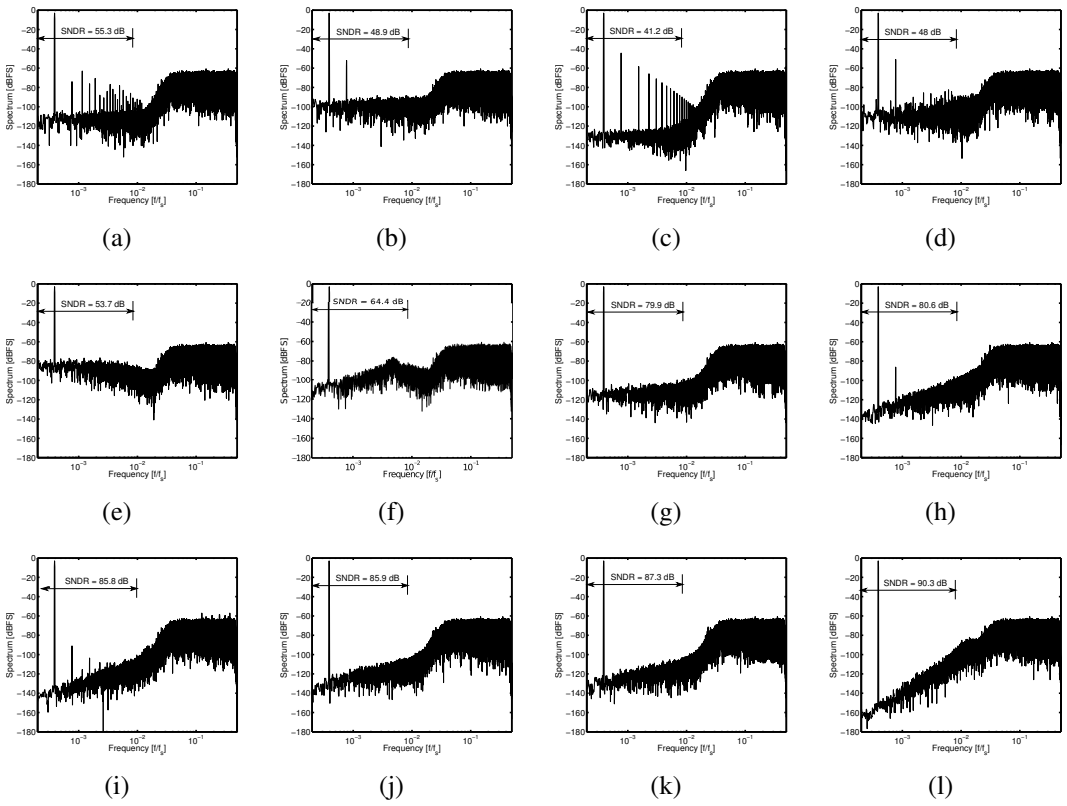


Figure 4.27: DAC output spectra for (a) thermometer coding, (b) random selection, (c) DWA, (d) 2nd-order DEM, (e) RSTC [Shen et al. [2010]], (f) TCMS, (g) MMS [Shui et al. [1999]], (h) ISI shaping [Risbo et al. [2011]], (i) EIS, (j) SMIS, (k) MSMIS with first-order shaping, and (l) MSMIS with second-order shaping for -3 dBFS input.

TCMS technique minimizes the DAC element switching rate and also shapes the static mismatch error. However, at moderate values of out-of-band NTF gain, its static mismatch shaping performance is not as good as DWA. Thus, it has an SNDR of 64.4 dB and SFDR of 96 dB. The MMS technique [Shui et al. [1999]] reduces the ISI induced distortion significantly and also shapes the static mismatch. It has an SNDR of 79.9 dB and an SFDR of 101.8 dB. The ISI shaping technique [Risbo et al.

[2011]] high-pass shapes both static mismatch and ISI error. However, it shows a second-order distortion at -3 dBFS. Thus it has an SNDR of 80.6 dB and SFDR of 86.4 dB. The EIS technique monitors both up and down transitions and thus has a better ISI shaping performance than [Risbo et al. [2011]]. It has an SNDR of 85.8 dB and SFDR of 89.9 dB. The SMIS technique shapes both static mismatch and ISI error while maintaining good decorrelation between instantaneous transition rate and input. Thus it has an SNDR of 85.9 dB and a very good SFDR of > 110 dB. The MSMIS technique builds on the technique of SMIS and removes its limitation of not shaping ISI error of individual elements. Thus, it has a better in-band noise than SMIS. It has an SNDR of 87.3 dB and SFDR of > 110 dB. The proposed DEM with second-order static mismatch and ISI shaping has an SNDR of 90.3 dB and SFDR of > 120 dB. The simulation results are summarized in Table 4.4. It can be clearly seen that the proposed DEM maintains its superior performance over the existing art at both moderate and low OSR.

To compare the performance of the different ISI mitigation techniques, it is very important to look at their noise and distortion performance at different amplitudes. To this end, an input amplitude sweep was performed with the same simulation settings as used for Fig. 4.27. The SNR versus amplitude sweep plot is shown in Fig. 4.28. The proposed technique has the best SNR. The EIS technique has a better SNR performance than the ISI shaping technique of [Risbo et al. [2011]] as it monitors both the up and down transitions thereby achieving finer resolution in transition rate count. The total-harmonic distortion (THD) versus input amplitude is shown in Fig. 4.29. The THD was computed by using the formula

THD $= 10\log_{10}(\text{signal power}/\text{summation of power in harmonic bins})$. To get an accurate estimate of the power in the harmonics, a 2^{20} point simulation was performed with an averaging of 10 times. From Fig. 4.29, it can be seen that the MSMIS technique has the best THD performance at large signal amplitudes. This is due to the excellent decorrelation between instantaneous transition density and input achieved by the MSMIS technique. The ISI shaping techniques of [Risbo et al. [2011]] and EIS show degradation in THD performance above -6 dBFS due to increased correlation of instantaneous transition density with the input resulting in increased harmonic distortion. The MMS technique [Shui et al. [1999]] performs better than the ISI shaping techniques of [Risbo et al. [2011]] and EIS at large signal amplitudes due to better decorrelation between instantaneous transition density and input signal. At low signal amplitudes, the power in the harmonic bins is dominated by noise rather than distortion. For the MSMIS and SMIS techniques, which have very low distortion, harmonic distortions go below the noise floor at input amplitudes smaller than -3 dBFS.

Finally, the output spectrum of different state-of-the-art ISI mitigation techniques at a small input amplitude of -60 dBFS is shown in Fig. 4.30. All the simulation conditions, except the input amplitude, are same as used for Fig. 4.27. It can be seen that at low signal amplitudes, the MSMIS technique has no visible distortions and has a good SNDR of 29.5 dB. As is expected, at low input amplitudes, the EIS technique has the best SNDR due to its better ISI shaping performance as it keeps count of both up and down transitions rather than only one transition.

Table 4.4: Comparison of different DEM techniques for multi-bit $\Delta\Sigma$ DAC

	OSR=64		OSR=16	
	SNDR(dB)	SFDR(dB)	SNDR(dB)	SFDR(dB)
Ideal	103.7	> 130	81.7	> 130
Thermometer	55.3	60.7	55.1	60.7
Random selection	48.9	52.2	48.7	52.2
DWA	41.2	44.5	41.2	44.5
2nd-order DEM	48.0	51.1	47.9	51.1
Random swap [Shen et al. [2010]]	53.7	76.2	51.3	76.2
TCMS	64.4	96.0	51.5	81.7
MMS [Shui et al. [1999]]	79.9	101.8	69.3	101.8
ISI shaping [Risbo et al. [2011]]	80.6	86.4	64.6	74.2
EIS	85.8	89.9	69.4	76.5
SMIS	85.9	> 110	71.4	> 110
MSMIS	87.3	> 110	73.9	> 110

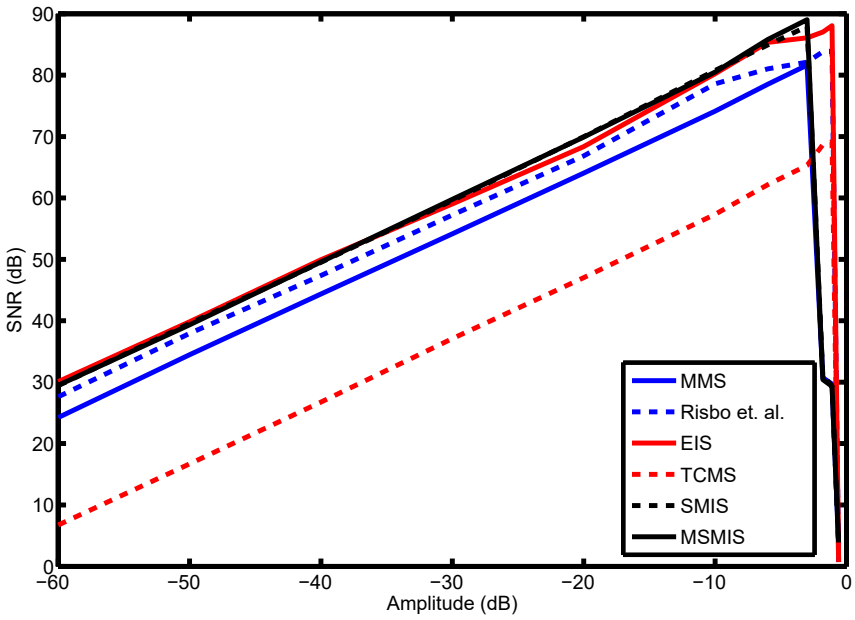


Figure 4.28: Comparison of SNR versus amplitude for ISI reduction techniques.

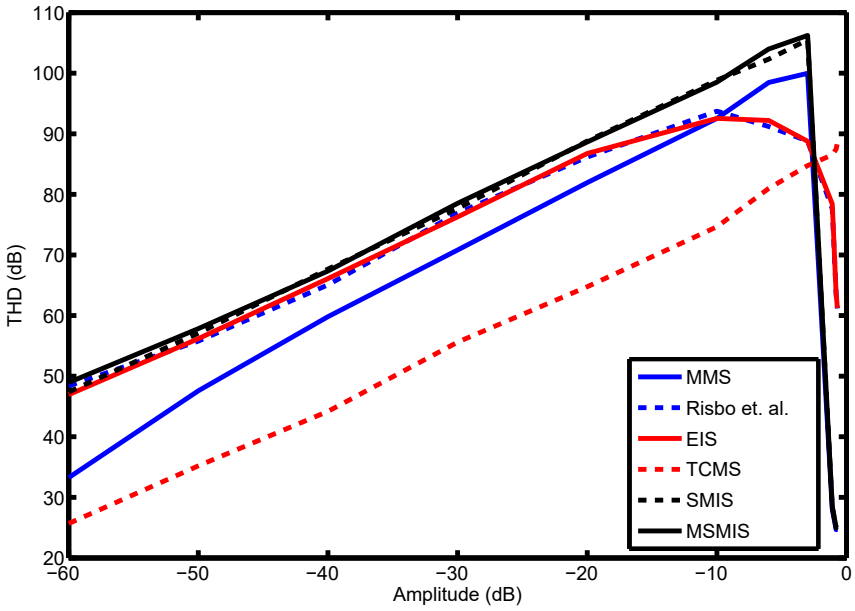


Figure 4.29: Comparison of THD versus amplitude for ISI reduction techniques.

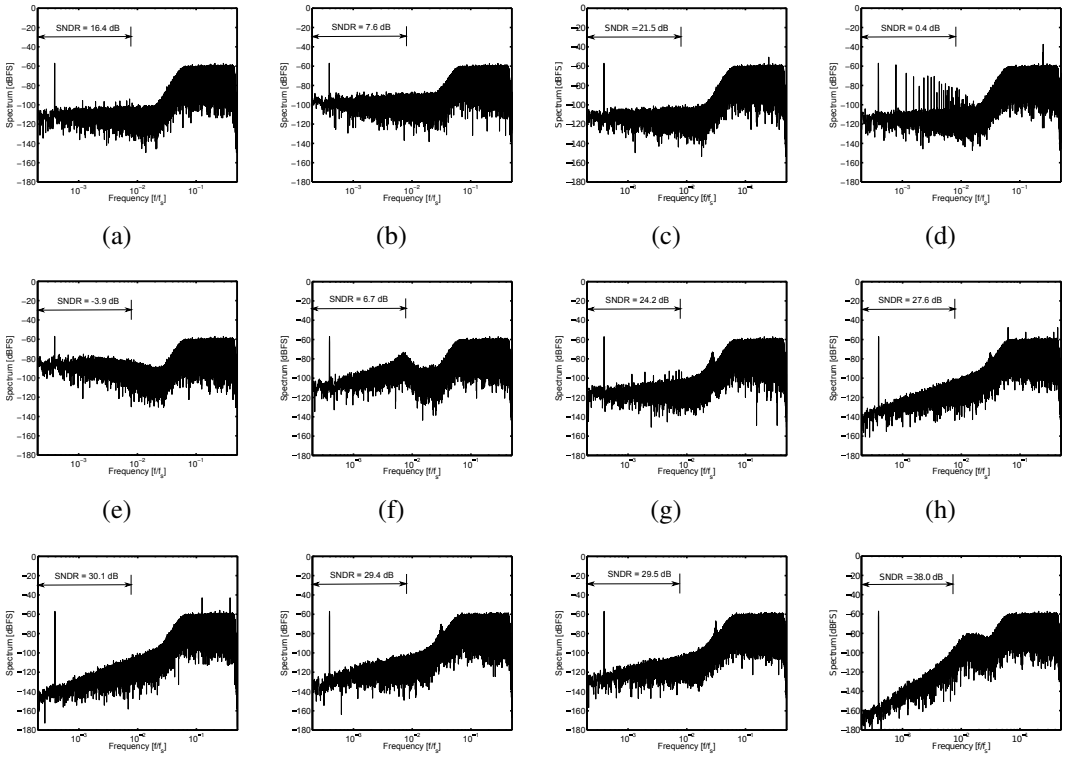


Figure 4.30: DAC output spectra for (a) thermometer coding, (b) random selection, (c) DWA, (d) 2nd-order DEM, (e) RSTC [Shen et al. [2010]] (f) TCMS, (g) MMS [Shui et al. [1999]], (h) ISI shaping [Risbo et al. [2011]], (i) EIS, (j) SMIS, (k) MSMIS with first-order shaping, and (l) MSMIS with second-order shaping for -60 dBFS input.

Chapter 5

Conclusion

A time-domain quantization ADC architecture has been presented in this thesis. The proposed ADC is highly digital and uses a SAR as the first stage and a ring VCO as the second stage. The ADC behaves like a 0-1 $\Delta\Sigma$ MASH and does not use any opamps. Two prototypes, in 180nm CMOS and 40nm CMOS, have been designed and tested. The measurement results show a very good energy efficiency at 12 bit resolution. The proposed architecture shows how digital techniques can be employed to design high performance ADCs in advanced technologies. The proposed technique is a promising example of digital assisted analog design in advanced CMOS technologies in which traditional analog design can be challenging.

The proposed ADC architecture has been extended to a capacitance to digital converter. CDCs are widely used in various sensing applications as well as in biomedical implants. The proposed CDC design has shown how the benefits of technology scaling can be leveraged to design high energy efficiency sensors. The measurement results with a 40nm prototype validates the high energy efficiency that can be achieved with the proposed CDC design technique.

This thesis also presents techniques to address static and dynamic errors in CT $\Delta\Sigma$ modulators. The proposed techniques are fully digital in nature and are

expected to improve in performance with technology scaling. As such, the proposed techniques can prove to be important enabling factors in raising the performance envelope of future CT, $\Delta\Sigma$ modulators.

Appendix

Appendix 1

List of publications

1. Arindam Sanyal and Nan Sun, "Dynamic element matching techniques for static and dynamic errors in continuous-time multi-bit $\Delta\Sigma$ modulators", *accepted in IEEE JETCAS*, 2015.

2. Arindam Sanyal, Long Chen, and Nan Sun, "Dynamic element matching with signal-independent element transition rates for multibit delta sigma modulators", *IEEE TCAS – I*, pp. 1325–1334, May, 2015.

3. Long Chen, Xiyuan Tang, Arindam Sanyal, Yeonam Yoon, Jie Cong, and Nan Sun, "A 10.5-b ENOB 645nW 100kS/s SAR ADC with Statistical Estimation Based Noise Reduction", *IEEE CICC*, pp. 1–4, Sept. 2015.

4. Manzur Rahman, Arindam Sanyal, and Nan Sun, "A novel hybrid radix-3/radix-2 SAR ADC with fast convergence and low hardware complexity", *IEEE TCAS – II*, pp. 426-430, May. 2015.

5. Kareem Ragab, Long Chen, Arindam Sanyal, and Nan Sun, "Digital background calibration for pipelined ADCs based on comparator decision time quantization", *IEEE TCAS – II*, pp. 456-460, May. 2015.

6. Arindam Sanyal, Kareem Ragab, Long Chen, T. R. Viswanathan, Shouli Yan and Nan Sun, "A hybrid SAR-VCO $\Delta\Sigma$ ADC with first-order noise shaping", *IEEE CICC* , pp. 1–4, 2014.

7. Long Chen, Arindam Sanyal, Ji Ma and Nan Sun, "A 24-uW 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique", *IEEE ESSCIRC*, pp. 219–222, 2014.

8. Arindam Sanyal, Peijun Wang and Nan Sun, "A thermometer-like mismatch shaping technique with minimum element transition activity for multi-bit delta-sigma DACs", *IEEE TCAS – II*, pp. 461–465, 2014.

9. Arindam Sanyal and Nan Sun, "An energy-efficient, low frequency-dependence switching technique for SAR ADC", *IEEE TCAS – II*, pp. 294–298, 2014.

10. Arindam Sanyal and Nan Sun, "An enhanced ISI shaping technique for multi-bit delta sigma DACs", *IEEE ISCAS*, pp. 2341–2344, 2014.

11. Arindam Sanyal and Nan Sun, "A low frequency-dependence, energy-efficient switching technique for bottom-plate sampled SAR ADC", *IEEE ISCAS*, pp. 297–300, 2014.

12. Arindam Sanyal and Nan Sun, "A very high energy-efficiency switching technique for SAR ADCs", *IEEE MWSCAS*, pp. 229–232, 2013.

13. Arindam Sanyal and Nan Sun, "A SAR ADC with 98% reduction in switching energy over conventional scheme", *Electronics Letters*, pp. 248–250, Feb 2013.

14. Wenjuan Guo, Youngchun Kim, Arindam Sanyal, Ahmed Tewfik and Nan Sun, "A single SAR ADC converting multi-channel sparse signals", *IEEE ISCAS*, pp. 2235–2238, 2013.

15. Arindam Sanyal and Nan Sun, "A Simple and Efficient Dithering Method for Vector Quantizer Based Mismatch-Shaped Delta Sigma DACs ", *IEEE ISCAS*, pp. 528–531, 2012.

Future publications

1. Arindam Sanyal and Nan Sun, "A 60fJ/step capacitance-to-digital converter with VCO-based first-order noise shaping", *to be submitted to IEEE VLSIC*.

2. Arindam Sanyal and Nan Sun, "A 76 dB dynamic range VCO-based $\Delta\Sigma$ ADC", *to be submitted to IEEE VLSIC*.

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Vita

Arindam Sanyal earned his Bachelor of Engineering degree from The Electronic and Telecommunication Engineering Department, Jadvpur University, India in 2007 and his Master of Technology from the Electronics and Electrical Communication Engineering Department, Indian Institute of Technology, Kharagpur, India in 2009. He has interned in Intel Corporation, Austin and Silicon Laboratories, Austin. He is currently working as a Design Engineer in Silicon Laboratories, Austin. His research interests are in data converter design.

email address: arindam3110@utexas.edu

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