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Automated Model-Based Transmission Line Fault Location Method Using Reduced Equivalent Circuit

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Automated Model-Based Transmission Line Fault Location Method Using Reduced Equivalent Circuit

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Abstract

Automated Model-Based Transmission Line Fault Location Method Using Reduced Equivalent Circuit

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Transmission lines are a vital part of power systems and are prone to a variety of short-circuit faults. Transmission line faults must be accurately identified and cleared so as to restore the faulted line back to normal operation in the shortest amount of time possible. Common fault locating practices used by utilities involve multiple manual data analysis stages which could cause time delays. This thesis presents an automated model-based transmission line fault location approach to improving the existing manual process.

A fault location process comprises of data preprocessing of the fault record and estimating the fault location using impedance-based techniques. This thesis first elucidates the data preprocessing steps, proposes and validates an algorithm for determining the fault current and voltage. It then proposes an automated fault location method by simulating relevant fault scenarios on a reduced equivalent circuit to determine the fault location. The proposed fault location method is implemented using MATLAB and OpenDSS. The need and process of forming reduced equivalent circuits for automating the fault location process

are presented. A test circuit was used to illustrate the method and to evaluate the technical capabilities of the algorithm.

The technical performance of the proposed fault location method was analyzed on a variety of aspects such as line and generator outage, the presence of mutual coupling, the presence of fault resistance, and multiple combinations of the above. The algorithm is robust and capable of handling the above mentioned issues which affect the fault location estimate.

Table of Contents

List of Tables

List of Figures

1. INTRODUCTION

1.1 MOTIVATION

Transmission lines are a vital part of a power system as they transfer electrical power over long distances from the source to the load. They are subjected to a variety of electrical faults as they are exposed to environmental effects such as lightning strikes or conductors coming in contact with each other during stormy weather conditions, animal or tree contact with a transmission line and insulation failure [1]. When a transmission line fault occurs, the fault has to be cleared as soon as possible so as to prevent permanent damage to equipment and devices, reduce the duration of power quality problems faced by customers and to restore the line to normal operating conditions.

Transmission line fault analysis has been a major topic for research for decades. Over the years, there has been development in communication technology, computational capability and system modeling which has led to the availability of more data and development of several algorithms for fault analysis. When there is a transmission line fault, protection equipment operates to de-energize the faulted line. Different recording devices located in substations will be triggered by the fault event and will record the required current, voltage and status signals. These records are used by different groups for fault investigation.

Fault records obtained from devices like digital relays and digital fault recorders need to be pre-processed to obtain the required useful fault data. This data is then analyzed and used in a fault location algorithm to obtain the fault location. As the fault analysis progress through each stage, it requires quick operation of personnel with different capabilities present at different locations to gather the required data and perform the tests, which may result in delays. For example, for a fault occurring at night, the maintenance

crew even if available have to wait until the next day for the protection engineer (who may only work normal day shifts) to calculate and estimate the fault location. Hence, this necessitates the need for an effective, reliable and automated fault location approach.

The major contribution of this thesis is to propose an approach for automated fault location and analyze the proposed method. The proposed approach aims at producing rapid and accurate fault location estimates as and when a fault record is received by the protection engineer.

1.2 PRIOR ART

Modern day digital relays use impedance-based fault location algorithms to produce fault location estimates. Over the years, several impedance-based fault location methods have been developed as they are simple to use and provide reasonable fault location estimates. Impedance-based fault location algorithms have specific requirements and the fault location estimates are affected by several factors which have been studied by several researchers. Some of the components which are sources of error in the fault location estimates calculated by impedance-based fault location methods are loads, mutual coupling between two lines, DC offset, CT saturation, inaccuracy in the line model, inaccuracy in extracting the fault current and voltage, presence of 3 terminal lines, tapped radial lines and many others. [2] [3] [4] [5] [6]. Hence, the fault location estimate obtained directly from the relays need not be always accurate.

A common procedure utilized by most utilities for identifying fault location is presented below. This method is not completely automated and requires manual manipulation to obtain the fault location.

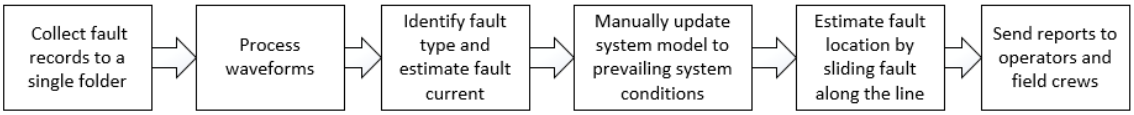

Figure 1-1: Outline of fault location process used by utilities

Figure 1-1 gives the outline of the fault location process followed by utilities to determine or estimate fault location. First, the disturbance records from digital fault recorders (DFRs) and digital relays are automatically brought to a single folder. The appropriate waveforms are analyzed to extract the magnitude and phasor relationships of fault voltages and current as well as to determine the fault type. The entire system modeled in a short-circuit program such as CAPE (Computer-Aided Protection Engineering) [7] or ASPEN (Advanced Systems for Power Engineering) [8] is available to the utility. This model is manually manipulated by the utility to represent the prevailing system conditions. The fault location is then identified by 'sliding' fault down the line till calculated current values match the measured current values. Finally, after identifying the fault location, reports with the estimated fault location is sent to operators and field crews.

1.3 OBJECTIVE

The above mentioned process for fault location commonly used by utilities is not completely automated and requires manual manipulation to obtain the fault location estimate. The aim of the proposed solution is to preserve the existing fault location technique (sliding fault along the length of the line and comparing it with actual values from fault record) but implement it in a different way so that the fault location process can be automated as well as make it convenient to use. The data preprocessing steps such as finding the appropriate fault current and voltage levels as well as the type of fault is to be automated. For this purpose, a novel method to calculate appropriate fault current and fault voltage to be used in fault location algorithms from the fault record is presented.

A modern technique using reduced equivalent circuits for model-based fault location is developed to reduce the complexity of the fault location process. The performance and capability of the developed algorithm are evaluated. This is done by analyzing the accuracy of the fault location estimates as well as by studying other factors which may influence the fault location estimates such as effects due to the presence of mutual coupling between lines, fault resistance, generator outage, line configuration change, and fault location reach of a circuit (distance up to which accurate fault location can be identified).

1.4 THESIS ORGANIZATION

The work presented in the following chapters are organized as follows. Chapter 1 presents the introduction to the thesis and explains the motivation for developing the proposed model-based fault location using reduced equivalent circuit approach.

Chapter 2 provides an outline of the proposed approach. It explains the potential of the proposed method and working scheme of the method.

Chapter 3 discusses fault records and explains how to interpret fault records present in COMTRADE file format which is one of the most commonly used industry standard file format for transient waveform and event data. This chapter further discusses the fault record preprocessing steps required before being able to apply any fault location algorithm. This chapter also proposes a method to identify the appropriate fault current and fault voltage to be used in the fault location algorithms.

Chapter 4 describes the proposed fault location method in detail. This chapter discusses different software packages used for analysis and the sample system model used for analysis. This chapter illustrates the process of formation of reduced equivalent circuits,

modeling of different circuit components in OpenDSS and implementing the proposed approach in MATLAB.

Chapter 5 presents the technical analysis of the proposed method. It begins with validating the reduced equivalent circuit short-circuit characteristics followed by demonstrating ways to tackle the common issues faced by utilities such as line and generator outages, the presence of mutual coupling and fault resistance. This chapter illustrates the robustness and advantages of the proposed method.

Chapter 6 presents a concise summary of the contents of the thesis. It also recapitulates the advantages of the proposed method and discusses the scope of future work.

2. OUTLINE OF MODEL-BASED FAULT LOCATION APPROACH

This chapter provides an outline of the proposed methodology. This chapter starts by discussing the potential of using a reduced equivalent circuit for model-based fault location. The working scheme of reduced equivalent circuits for model-based fault location is introduced. The chapter briefly presents the role of different components involved in the proposed method.

2.1 Potential of Reduced Equivalent Circuit for Model-Based Fault Location Method

Existing fault location approaches commonly used by utilities are not completely automated and requires manual manipulation to obtain the fault location. Based on initial preprocessing of the fault record, the faulted line and fault characteristics are obtained. Several fault scenarios are then simulated with faults along the entire length of the transmission line. Fault location is identified when the simulated fault characteristics of a fault scenario match the measured fault characteristics obtained from the recorded fault waveform. These approaches make use of the full circuit model available to the utility in some power system simulation software such as CAPE or ASPEN.

The tasks of simulating sliding faults and comparing simulated fault currents to the actual measured fault current are laborious. This process can be automated provided the short-circuit analysis software can be commanded or driven to perform the desired actions. Unfortunately, there is no third-party software to drive CAPE externally. Other short-circuit programs may be driven by a third-party program, however, switching from one software program to another may introduce disruption and incur operational changes. For

these reasons, automating fault location search using a full-circuit model where the short-circuit program cannot be driven using an external software is difficult and cumbersome.

The above discussion describes the necessity of developing an alternative approach to overcome the difficulties of automating fault location search using a full-circuit model. The solution proposed below is to emulate the full-circuit model-based fault location approach, however, with reduced-circuit models. In the proposed approach, a series, i.e., a library, of equivalent circuits are developed to replicate short-circuit characteristics of circuits and buses where digital fault recording devices (DFR) are located. Each equivalent circuit is converted into a short-circuit analysis program that can be driven by an external software. OpenDSS is chosen for this purpose because it is a freeware and developed by EPRI (Electric Power Research Institute). MATLAB developed by Mathworks is chosen as the driver because it has been widely used to drive OpenDSS as well as its scripts are easier to edit to improve an existing algorithm if required. Furthermore, MATLAB can be used to preprocess fault record data and post-process results from OpenDSS as well.

The proposed solution intends to preserve the existing successful fault location technique (sliding fault along the length of the line and comparing it with actual values from fault record) used by utilities but implements it differently so that the fault location process can be automated as well as make it convenient to use. By implementing this approach, fault location can be estimated for a variety of scenarios such as tapped lines, three terminal lines as well as a fault at lines farther away from the recording device. The fault location process is automated and can produce the fault location estimate as and when data from a DFR is put in the data folder. This eliminates the tedious and cumbersome process of obtaining fault current and voltages from the fault records as well as manually performing the sliding fault process to obtain fault location.

Furthermore, the approach is universal. Most utilities have the entire transmission system modeled in CAPE or ASPEN or any other software. Even if a third party software can drive one of these short-circuit analysis softwares, the coding and development for automating the fault location process has to be done for each short-circuit analysis software separately and is not universal. Hence, equivalent circuits are implemented using OpenDSS and are independent of the software used by utility (CAPE, ASPEN or any other software) in which the whole system model is available. The library of equivalent circuits in OpenDSS, driven by MATLAB is used for estimating fault location and no other software is required. The hardware requirements to implement this approach is also minimal. It does not require any large investments or any new equipment to be installed. Hence, the proposed approach can be implemented by any utility with their existing infrastructure and system.

2.2 Working Scheme Summary of Model-Based Fault Location Approach

This approach aims at identifying the exact location of a fault occurring in the transmission or distribution system by using data from intelligent electronic devices (IEDs) or fault recorders which monitor different lines at different locations throughout the system. The information from these fault recording devices, which are placed at the end of certain lines, are sent to a data folder through supervisory control and data acquisition (SCADA) and other communication systems. The centralized data folder where data from all the DFRs arrive is monitored continuously. As and when a DFR record arrives in that folder, it is processed automatically and the location of the fault will be identified. This process is done using MATLAB, a user friendly software which provides the opportunity to control and drive OpenDSS. The process can be done either in real-time or off-line.

Several different commercially available fault analysis platforms are used by utilities to model electrical transmission network and its protection systems. For the development and illustration of the proposed approach, CAPE software has been used. The entire electrical transmission network is assumed to be available in CAPE.

Network reduction is a common feature found in most power system analysis and protection engineering software. CAPE has a similar feature where a large complex system can be reduced to a small equivalent circuit that depicts the short-circuit characteristics of the actual large system for the elements under consideration. This is done by using the Short Circuit Reduction module in CAPE. The developed equivalent circuit in CAPE can be modeled in OpenDSS using network data obtained from CAPE after reducing the network. This conversion from CAPE to OpenDSS is done using MATLAB which highlights the versatility of MATLAB and OpenDSS. Using the above steps, a library of equivalent circuits would be created in OpenDSS. These equivalent circuits can be easily manipulated using MATLAB to perform fault analysis. OpenDSS software is used here because CAPE doesn't allow external software to drive it.

MATLAB reads and processes data from DFR present in the data folder and appropriately selects the equivalent circuit from equivalent circuit library based on DFR location. The selected equivalent circuit in OpenDSS will be driven by MATLAB to perform fault analysis by sliding a fault along the suspected faulted lines. By comparing the data obtained from fault analysis and that which was obtained from DFRs, fault location would be estimated.

2.2.1 Reduced Equivalent Circuit in CAPE

In CAPE software, the equivalent circuit can be obtained using Short Circuit Reduction module. The user can choose the size of the equivalent circuit by choosing the

buses to retain from the large original circuit in the equivalent circuit. The equivalent circuit represents the portion of original circuit present surrounding the DFR device. The circuit would be reduced such that the short-circuit characteristics of the equivalent circuit are same as that of the original circuit. Each DFR or a group of DFRs will have its own equivalent circuit model stored in the library of circuits. This library of equivalent circuits is modeled in OpenDSS from the network data obtained from reduced equivalent circuits in CAPE.

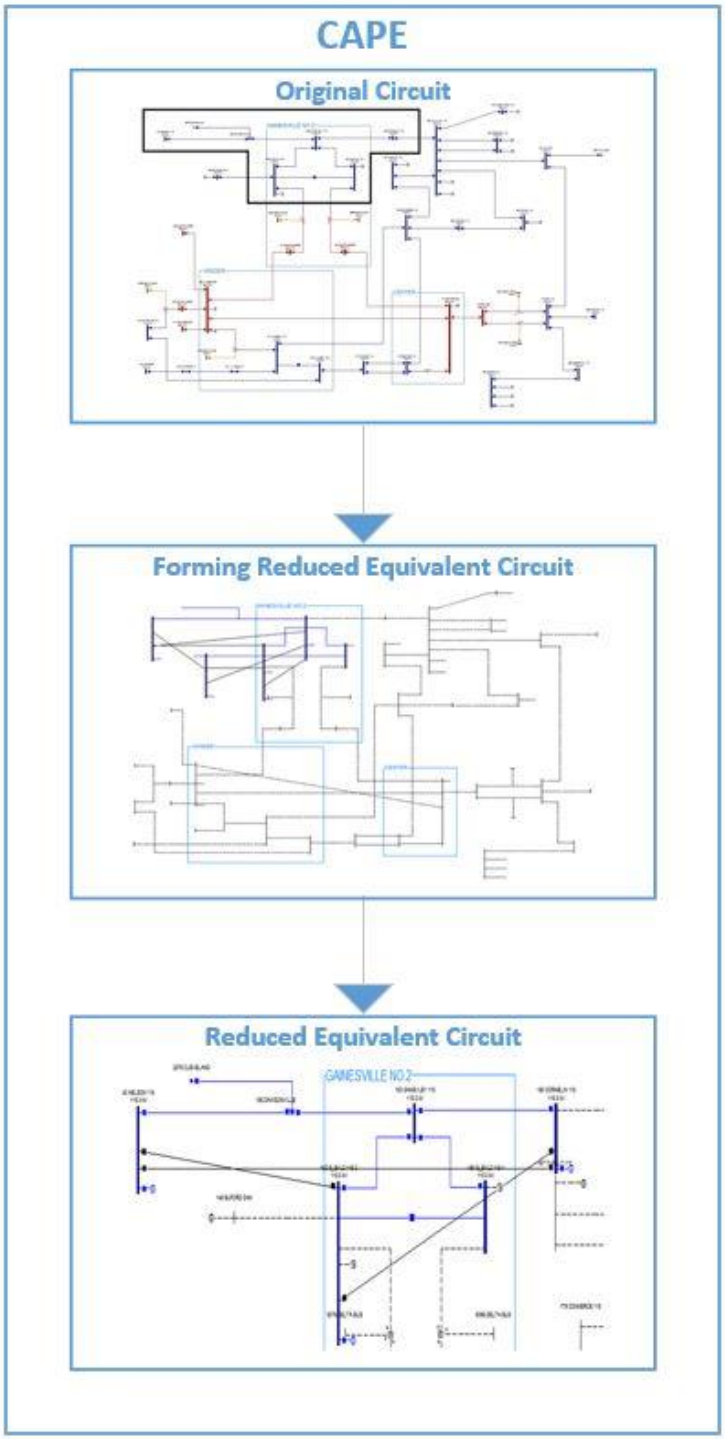

Figure 2-1 : Reduction of large complex circuit into smaller equivalent circuits based on DFR location

2.2.2 Reduced Equivalent Circuit in OpenDSS

Using the network data of the reduced equivalent circuit obtained from Short Circuit Reduction module in CAPE, the reduced equivalent circuit is modeled in OpenDSS to run different fault scenarios. The data in CAPE is translated to OpenDSS as CAPE does not have the facility to be driven or controlled by other software platforms like MATLAB. OpenDSS provides that feature where it can be driven by MATLAB for modeling, editing and simulating the equivalent circuit. The equivalent circuit would be driven by MATLAB to simulate faults at several fault locations along the line and with various fault impedances. The results of each iteration of faulted scenarios are collected by MATLAB. Modeling of the equivalent circuit in OpenDSS from the network data of the equivalent circuit obtained in CAPE is done manually, but this process can be automated too.

2.2.3 Role of MATLAB in Model-Based Fault Location

MATLAB is used to read the fault records from DFRs as and when it receives them in the data folder. MATLAB calculates the fault current, fault voltages, instant of fault occurrence and the location of the DFR from the fault record. MATLAB would then identify the correct equivalent circuit from the library of circuits. Once the equivalent circuit is identified, MATLAB would then run several iterations of the chosen equivalent circuit in OpenDSS to simulate faults at various locations along the length of the line and obtain the fault currents and voltages. It then compares the simulated data with the actual fault voltages and currents obtained from the fault record from data folder to estimate the fault location. MATLAB provides the fault location estimate based on the best possible match that it sees from the comparison. In order to calculate the fault current and voltages, the channel mapping information associated with each DFR must be preloaded into MATLAB. Figure 2-2 shows the role of MATLAB in the proposed model-based fault location.

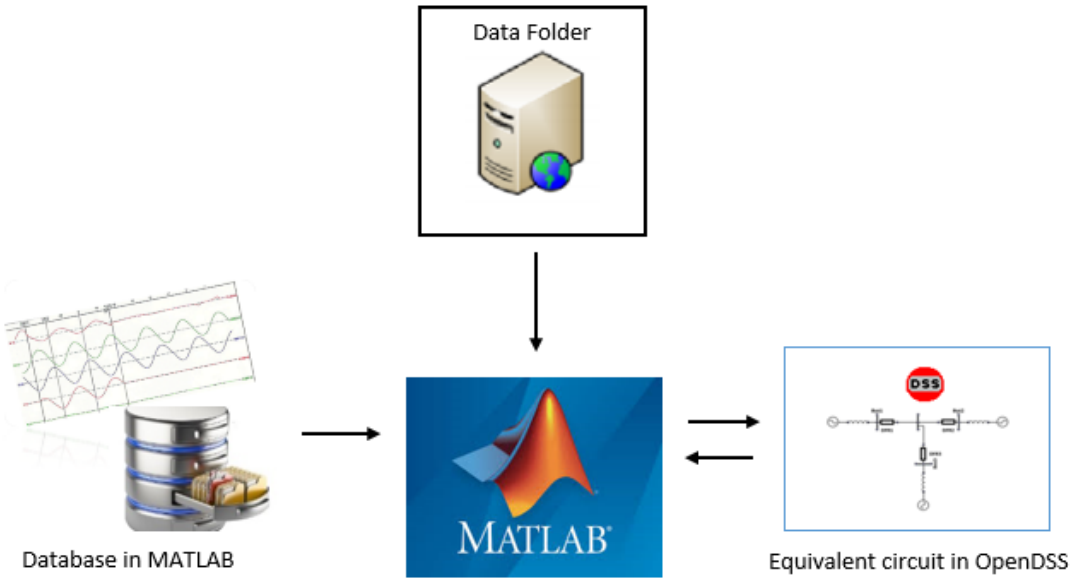

Figure 2-2 : Role of MATLAB in the model-based fault location

The following is a flow chart explaining the role of MATLAB and OpenDSS and their sequential tasks in determining the fault location.

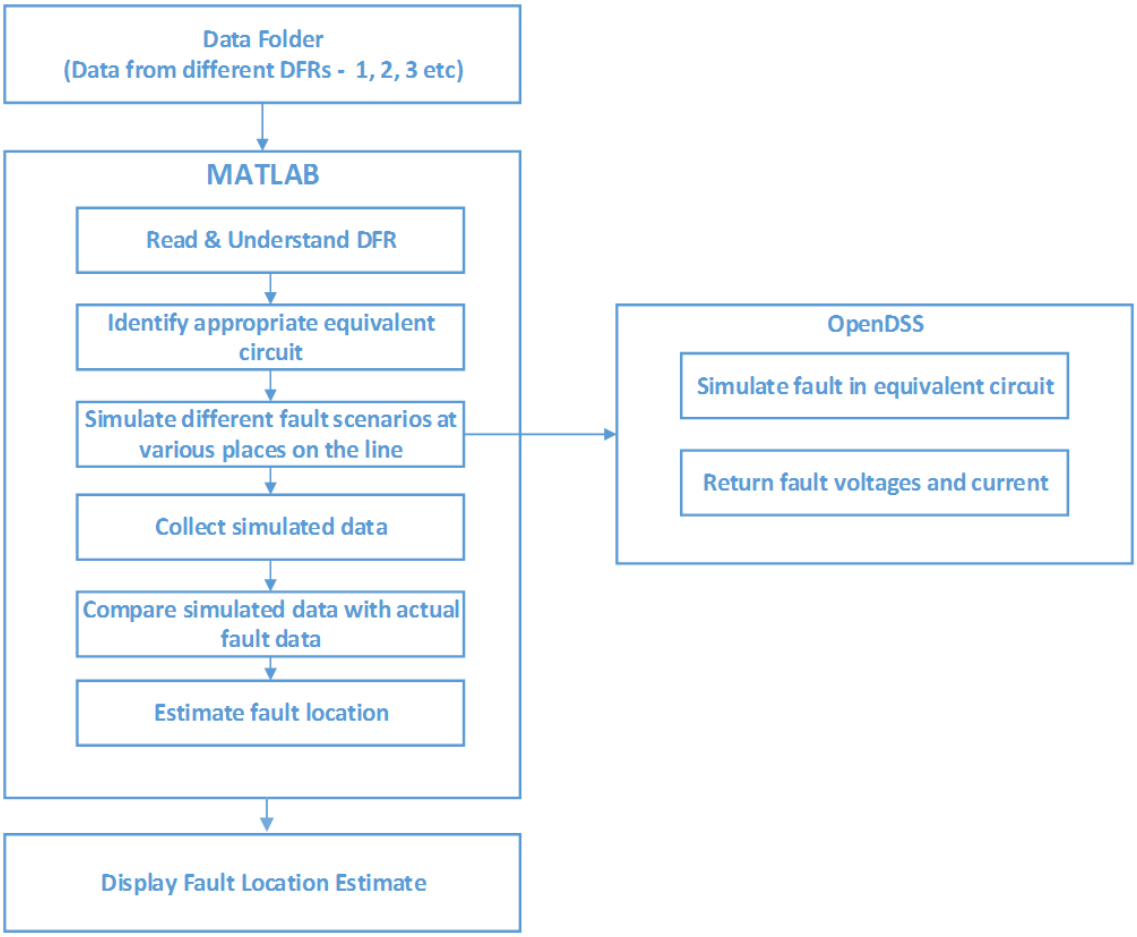

Figure 2-3 : Flowchart depicting the sequential workflow of MATLAB and OpenDSS

3. FAULT RECORD PREPROCESSING

The need for an automated fault location approach and the potential of the proposed method have been discussed in the previous chapters. Chapter 2 provided an outline of the proposed approach. The following chapters discuss the proposed technique in detail.

This chapter discusses the data preprocessing steps when a fault record is received by the operator. The chapter starts with introducing fault recording devices and the common industry standard file format in which fault records are present in (Common Format for Transient Data Exchange - COMTRADE file format). The raw data present in fault records need to be processed, appropriate prefault/fault voltage and current have to be obtained to estimate the fault location accurately. This chapter compares the fault location estimates obtained using data from different time intervals in the fault record and uses one-ended impedance-based algorithms to prove the efficacy of the proposed method. The entire process of fault location has been implemented using MATLAB. Hence, no additional software is required for data preprocessing.

3.1 FAULT RECORDING DEVICES AND FAULT RECORD

Recording devices are primarily used to monitor the status of various devices in the power system and to record voltages and currents at a particular location during certain events. Recording devices may differ in sampling rate, length of record and type of record they can capture based on their purpose of usage [9]. Some examples of recording devices are Digital Fault Recorders (DFRs) and microprocessor-based relays.

Recording devices produce fault records when they detect any disturbance in the instrument they monitor. The recording device can be triggered by a variety of conditions based on their setting such as over-current, change in observed voltage or impedance. Recording devices monitoring transmission lines are configured to produce fault records

such that they contain pre-fault information, event or fault data and post-fault information. Recording devices monitoring transmission line for faults require fast recording systems as transmission line faults are usually short lived.

Prefault section of fault record contains information regarding the normal system conditions before the disturbance or fault event has occurred. Event data contains fault voltages and currents and status of protective devices (if monitored by the DFR). Post-fault information shows how the system has responded and operated under the fault condition.

3.1.1 Common Format for Transient Data Exchange - COMTRADE File Format

The rise in measurement and digital technology has led to increasing usage of recording devices for a variety of purposes. Fault records can be in a variety of data formats depending on the manufacturer of the recording device and have to be read in specific software platforms. Hence, IEEE had defined a common data file format for exchanging various fault, test and simulation data of electrical power system components, namely, IEEE Standard Common Format for Transient Data Exchange (COMTRADE) for Power Systems (IEEE Standard C37.111-1999) [10]. This format of representing data contains up to 4 types of files. They are header file, configuration file, data file and information file. This section provides an outline to the different types of files present in COMTRADE file format.

The header file is an optional ASCII text file which provides supplementary information other than the fault data and configuration data. It can contain a variety of information such as additional details regarding the fault, system parameters and status of the system components. Header file has ".hdr" extension to distinguish it from other file types.

A single fault record can contain several measurements of a variety of quantities in different scales stored in the data file. The configuration file contains the information required to interpret the contents of the data file. The configuration file has ".cfg" extension to distinguish it from other file types. It contains the following information in the given order. The first line consists of station name along with identification of the recording device followed by COMTRADE Standard revision year. The next line contains the total number of channels and type of channels. A number followed by 'A' represents the number of analog channels and number followed by 'D' represents the number of digital channels present. The analog channel information is next followed by status (digital) channel information. Each line represents a channel recorded in the DFR. This is followed by line frequency, sampling rate information, date/time stamp, data file type and time stamp multiplication factor. Figure 3-1 shows a sample configuration file.

```
StationA, Device1,2013
40,16A,24D
1,IA,,, Amps,0.001000000000,0.0,0.0,-842000,846000,400,1,P
2,IB,,, Amps,0.001000000000,0.0,0.0,-6186000,6090000,400,1,P
……                                  (represents multiple line of analog channel information)
1,ENT,,,0
2,TP,,,0
3,50_51,,,0
……                                  (represents multiple line of status channel information)
60.000000
1
 960.0000,240
17/03/2016,17:47:40.027375
17/03/2016,17:47:40.093000
ASCII
1
```

Figure 3-1 : Sample configuration file

Each line of analog channel information contains the following: analog channel index number, channel identifier, phase identification, circuit component monitored,

channel units, channel multiplier, channel offset, channel time skew from start of sample period, range of data value (minimum followed by maximum) for that channel, voltage or current transformer ratio (primary followed by secondary) and primary or secondary data scaling identifier.

From the above example, the third line has information about the first channel. From Figure 3-1, we can infer that the analog channel contains measurements of current in 'A' phase in amperes. If the data value were 100, the actual current value would be 100 multiplied by channel multiplier (0.001 in this case) and then the offset factor (0 in this case) is added. The minimum data value that could be present is -842000 in the data file for that channel (not the actual measured value in amperes) and the maximum value is 846000. The current transformer ratio used for measurement of this channel quantity is 400:1. Finally, 'P' represents that the measured quantity is the primary value and hence the actual current value in phase A. In the example, there are no channel identifier or phase identification element present and are hence left empty.

Each line of digital channel information contains the following: status channel index number, channel name, channel phase identification, circuit component monitored and normal state of the status channel (0 or 1). From Figure 3-1, consider the first digital channel. It has the status channel index number which is '1' and channel name which is 'ENT'. Information about channel phase identification and circuit component monitored are not specified and are hence empty in the configuration file. The normal state of the channel is '0'.

Line frequency and sampling data information come next after digital channel information. Line frequency is specified in hertz (Hz). The sampling data information is as follows: number of sampling rates in the data file, sampling frequency in Hertz and last sample number at the given sampling rate. In the above example, there is one sampling rate

of 960 Hz and the last sample number is 240. Date/time stamp is specified as day, month, year, hour, minute and seconds. The data file according to this example will be in ASCII format and hence is denoted by 'ASCII' in the second last line. Finally, the time stamp multiplication factor is the last line and is 1 in our example.

The order of contents must be maintained throughout according to IEEE Standard C37.111-1999 [10] so that the records are interpreted correctly by any human or computer.

The data file contains scaled values of the channel measured. Configuration files contain the conversion factors which need to be implemented to get the actual measured values. Hence, the data files will be in the exact order and format as defined in the configuration file. The data file has ".dat" extension to distinguish it from other file types.

Information can be stored in binary or ASCII format in the data file. In this section, we shall discuss ASCII data file format. Each row contains the data of different channels for that sample number and hence the total number of rows depends on the length of the recording. The first column contains the sample number followed by the time stamp for the data of that sample number. The next set of columns contain data values for each analog channel followed by data for status channels. At the end of the file after the last row of measurement data, an ASCII end of file marker (EOF) is placed to denote the end of the data file.

Information file contains additional information required apart from the standard information provided in the above files to be able to analyze the fault record by different users. This file can contain public information which is accessible by all users and private information that is available only to certain users. The information file is an optional file and has ".inf" file extension.

A fault record in COMTRADE format have a configuration and data file and may or may not contain header file and information file as they are optional files. The file names can be the same for all the 4 types of files, and they are distinguished by their file type.

3.2 Proposed Algorithm for Determining Fault Instant and Prefault Instant

In this section, an algorithm is proposed for determining the appropriate instant for taking fault current and fault voltage measurement. This step is crucial in fault analysis as the values obtained in this step directly affects the fault location estimate. The efficacy of the proposed algorithm is demonstrated in this chapter by implementing the algorithm on sample fault records and using the identified fault current and voltage measurement for fault location.

Transmission line faults are accompanied by significant raise in current along with voltage drop in the faulted phase. Different algorithms have been proposed and implemented over the years for fault detection in relays. For our analysis, we sweep through the current values obtained from previous step and fault is said to be detected when the magnitude of current corresponding to that sample set is higher than three times the magnitude of current corresponding to sample set 3 cycles before it. In other words, fault (event) starts when current at that instant is three times the value of current 3 cycles before that instant. This sample number is considered as fault instant and the sample number which was 3 cycles before it is considered as prefault instant. Usually, when a fault occurs, the current flowing through the line raises to large values within a few cycles. In some fault records, data only for few cycles before the fault occurs may be available and data for many cycles before the occurrence of the fault may not be available. Hence, the instant 3 cycles before the first detection of large current value is considered as prefault instant. On continuing examining the set of current values beyond the fault instant, we compare current

value obtained corresponding to each sample with three times the prefault current value. The fault exists until this condition fails. In other words, all the sample sets which have RMS currents larger than 3 times the prefault current value are considered as fault instants.

The instant where the fault current settles after rising and voltage settles after falling down is the appropriate moment for taking values to be used in fault location algorithms. This can be achieved by using the following two criteria to obtain the fault current and voltage. The percentage change in the calculated fundamental RMS current between successive sample data set is within 1 percent and the percentage change in the calculated fundamental RMS voltage between successive sample data set is within 3 percent. These threshold values were determined experimentally and were found appropriate for a variety of fault records which were studied. These criteria also depend on sampling frequency. The above values are for 960 Hz. At higher sampling rate, the percentage change in current and voltage between successive sample data would be much lesser because the signal is sampled more frequently. Hence, dividing it by the number of times the sampling frequency exceeds 960 Hz gives the required threshold value. For example, for 5760 Hz, the current criterion would be 0.16 percent and voltage criterion would be 0.5 percent. To further ensure that the waveforms have settled, we further check if the current and voltage condition is satisfied for the next half cycle (next 8 sample sets for 960 Hz).

The fault current and voltage of most permanent faults settles to a steady state value and can be estimated using the above method. In cases where the above criteria could not be satisfied, the highest RMS current value and the corresponding voltage can be considered as fault current and fault voltage. This may lead to inaccuracies in measurement due to transients or small spikes in current which may occur.

3.3 MATLAB IMPLEMENTATION OF DATA PREPROCESSING PROCEDURE

This section contains discussion and implementation of the data preprocessing steps of the fault record using MATLAB.

Fault records present in COMTRADE file format have at least 2 files as discussed in previous sections. When a new fault record is received by the utility, it is to be imported into MATLAB and processed. Furthermore, a single DFR record can have measurements from monitors measuring different lines. Hence, the appropriate channels measuring the fault current and voltage have to be identified. This can be done in several ways based on the setup implemented by the utility.

One approach is that separate folders can be used for disturbance or fault records corresponding to each transmission line monitored. Hence, when a fault record is received from a DFR, it is automatically put into its corresponding folder. MATLAB can be programmed to check for new files in each DFR folder, and when a file is received, it can then process the fault record and select the appropriate equivalent circuit based on the folder in which it is present. Another approach is to identify the faulted line using the header file which may contain information regarding the fault. Once the faulted line is known, the appropriate current and voltage channels can be processed. Another approach which can be used if the above two methods are not viable is by having to process all the channels present in the fault record and identifying the channels containing the fault data. This method can be tedious if the fault records have several channels recorded in it as every channel may have to be processed till the channels corresponding to the faulted line is identified.

Once the faulted line is known, the voltage and current measurements of the faulted line can be processed. In the data file, each column refers to a channel and each row is a sample. The data in the configuration file is used to obtain the right conversion parameters

to acquire the measurements in engineering units such as volts (V) and amperes (A). Care should be taken to avoid mismatch in units such as kilovolts (kV) and amperes (A) or volts (V) and kiloamperes (kA). The data obtained after conversion can be plotted in a graph to ensure that the right channels have picked up from the fault record. Other data such as sampling rate of the fault record and length of the fault records can be identified from the configuration file.

The measurements obtained from fault records are discrete samples and hence Discrete Fourier Transform (DFT) [11] [12] is applied to obtain the phasor quantities. The fundamental RMS quantity is required for using the fault location algorithm. This can be obtained from the result of DFT on the raw data.

DFT is applied on one cycle data. Hence, the number of samples present in one cycle depends on the sampling frequency of the recorder. DFT in this manner is applied to the entire sample set with moving rate of the window as one sample. Hence, a fundamental RMS quantity is present corresponding to each sample in the set. This is done because the fault instant and prefault instant is unknown and has to be identified later. Else, DFT can be applied to a sample set starting with prefault and fault instant to determine the prefault and fault current/voltage for using in the fault location algorithm. This quantity is referred to as fundamental RMS quantity or as just voltage/current accordingly.

The algorithm proposed in the previous section is implemented in MATLAB to calculate prefault as well as fault current and fault voltage. These values obtained are then used in fault location algorithms to estimate the location of the fault.

3.4 Transmission Line Fault Data for Evaluating the Proposed Algorithm for Determining Fault Instant and Prefault Instant

In this section, two transmission line fault data are considered to illustrate the process.

3.4.1 Case 1: A Single-Line-to-Ground Fault

The first case taken for analysis is a transmission line fault on a 345 kV line which is 69.94 miles long and connects station A and station B as shown in Figure 3-2. From the event analysis performed by utility using data at station A, the report revealed that there was a single line-to-ground fault on the line creating around 6 kA of fault current on the B phase of the line. The actual location of the fault was at 15.33 miles from station A caused by buzzard droppings on the insulator. Table 3-1 summarizes the characteristics of the fault event along with the line impedance data.

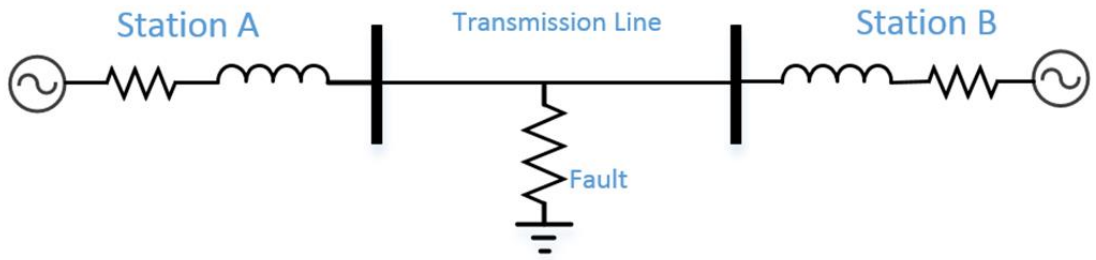

Figure 3-2 : Transmission line fault

Table 3-1 : Event analysis for Case 1

Line Data	Fault Data
Line Voltage (kV) = 345 Total Line Length (miles) = 69.94 Total Line Impedance: R1 (ohms) = 3.9159 X1 (ohms) = 43.2536 R0 (ohms) = 41.6944 X0 (ohms) = 122.9647	Fault Type = BG Distance to fault from Station A (line miles) from event analysis = 15.33

The relevant waveforms of the faulted line present in the fault records are shown in Figure 3-3. The sampling frequency of the fault record was 960 Hz. The first three

waveforms from top show the currents in phase A, B and C of the line respectively and the bottom three waveforms show the phase voltages of phases A, B and C respectively. Phase B current waveform clearly shows an increase in magnitude while phase B voltage waveform shows a sag which is indicative of a single line-to-ground fault on phase B.

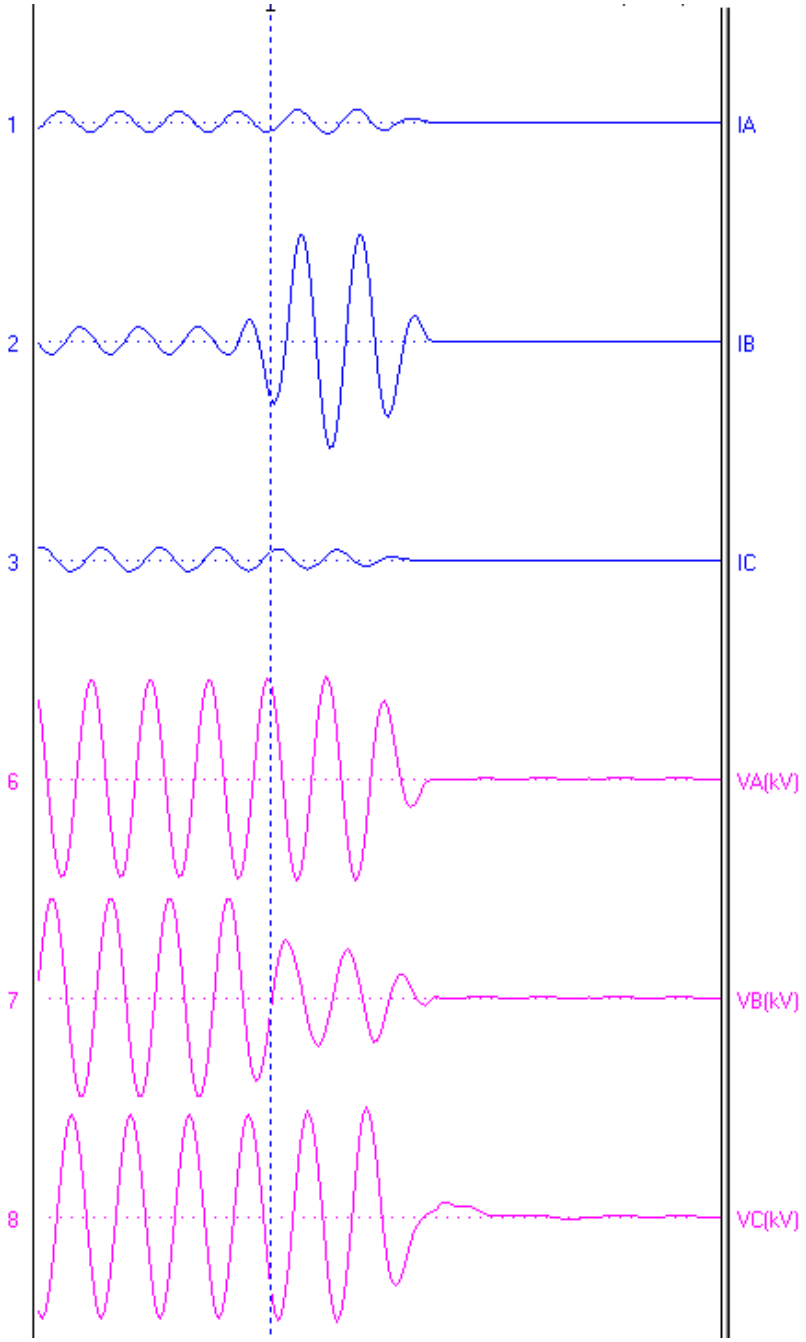

Figure 3-3 : Phase voltage and current waveform of phase A, B and C for Case 1

3.4.2 Case 2: A Line-to-Line Fault

The second case taken for analysis is a line-line fault involving B and C phases. The breakers protecting the circuit tripped and locked out because a tree fell on the line about 2.6 miles from station C. The breakers at both ends of the circuit had tripped, reclosed, and tripped back out. The faulted line is a 138 kV, 12.88-mile long line between station C and station D. The fault current was more than 20 kA. Table 3-2 summarizes the characteristics of the fault event along with the line impedance data.

Table 3-2 : Event analysis for Case 2

Line data	Fault Data
Line Voltage (kV) = 138 Total Line Length (miles) = 12.88 Total Line Impedance: R1 (ohms) = 1.4702 X1 (ohms) = 6.6083 R0 (ohms) = 7.8176 X0 (ohms) = 23.1480	Fault Type = BC Distance to fault from Station 1 (line miles) from event analysis = 2.64

Figure 3-4 shows the waveforms related to the faulted line present in the fault records. The sampling frequency of the fault record was 3840 Hz. The first three waveforms show the currents in phase A, B and C of the line. The first waveform is the current in phase A followed by current in phases B and C respectively. The last 3 waveforms show the phase voltage waveforms where the first waveform corresponds to phase A followed by phase B and C respectively. The swell in the current waveforms in phase B and C clearly indicate the presence of a line-to-line fault. It also clearly shows the circuit has tripped, reclosed and tripped back out. The actual location of fault for this event is at 2.64 miles from station C.

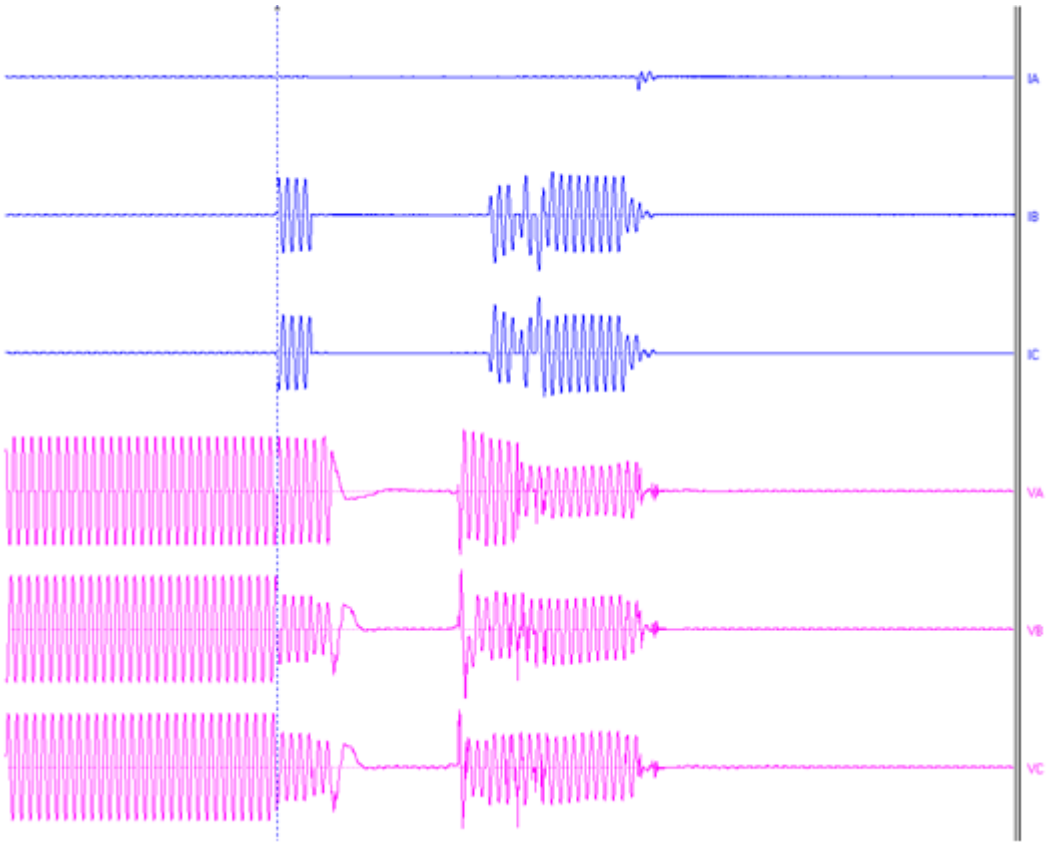

Figure 3-4 : Phase voltage and current waveform of phase A, B and C for Case 2

3.5 Evaluation of the Proposed Algorithm for Determining the Fault Instant and Prefault Instant

This section illustrates the proposed method and describes the results obtained from using the method on the two test cases mentioned previously. Simple and commonly used impedance-based fault location techniques such as Reactance method, Takagi method and Novosel method [2] [3] [13] [14] [15] are used to demonstrate the efficacy of the proposed method. The fault location results obtained by using the proposed method to get fault current and voltage is compared with the results obtained by using voltage and current data at other time intervals.

Case 1 is a single line-to-ground fault in phase B of the line (BG fault). The fault record has a total of 240 samples which includes prefault, fault and post-fault information. The sampling frequency of the recorder was 960 Hz, hence, there are 16 samples per cycle (60 Hz fundamental frequency). On applying DFT on once cycle data, we get 224 RMS current and voltage values (one for each nth sample as the starting sample and the sample set contains 1 cycle of data samples). The last 16 samples (or 1 cycle data) is omitted as the DFT will not contain data of 1 complete cycle. Furthermore, the last cycle data is usually post-fault data and has no useful information for fault location.

On sweeping through the calculated current values, it was observed that the current value corresponding to the 55th sample was thrice that of the current value corresponding to the 7th sample value (3 cycles correspond to 48 samples). Hence, the fault is considered to have started at the 55th sample. The value of current and voltage corresponding to the 7th sample was taken as prefault values. The fault existed for 41 samples (until the 95th sample). On applying the proposed method for identifying fault current and voltage, it was observed that the voltage and current had stabilized starting from the 68th sample. The prefault and fault current and voltage values were used in 3 impedance-based algorithms. Comparison between results obtained by using the proposed method and results obtained by taking the faulted cycle at several other different time instants are shown in Table 3-3. The actual fault location was at 15.33 miles from station A. It can be observed from Table 3-3 that the proposed method gives accurate fault location estimate compared to taking data from other faulted cycles for estimating fault location.

Table 3-3 : Comparison of fault location results for Case 1

	At instant of identification of fault inception	Half cycle after fault inception	Proposed Method	One and a half cycle after fault inception	Two cycles after fault inception
Sample number of data obtained for fault analysis	55	63	68	79	87
Reactance (miles)	57.88	20.38	15.40	14.23	12.90
Takagi (miles)	59.64	20.35	15.33	14.23	13.26
Novosel (miles)	58.50	20.30	15.25	14.23	13.11

There are several sources of error while using impedance-based fault location methods [2]. Hence, impedance-based fault location may not accurately pinpoint the exact fault location but location estimates closer to the actual fault location is always better. This can be seen in Case 2. The fault location obtained using the proposed method gives a result closer to the actual fault location than fault location obtained using data from other fault instants as shown in Table 3-4.

The sampling frequency of fault record in Case 2 is 3840 Hz and the total number of samples is 7757. The fault is a line-line fault involving phases B and C. Hence, the line to line current and voltages of phase B and C are calculated instead of phase currents and voltages corresponding to each sample. Also, line-to-line currents and voltages are used in the fault location algorithms as well. On following the above procedure, the fault was identified to start at the sample number 1908. The voltages and currents of the sample number 1716 (3 cycles correspond to 192 samples) were taken as prefault voltages and currents. As the sampling frequency of this record was 4 times compared to 960 Hz, the criteria used for checking if the voltage and current has reached steady state is also altered accordingly. The criteria were changed such that the percentage change in calculated fundamental RMS current between successive sample data set should be within 0.25

percent and the percentage change in the calculated fundamental RMS voltage between successive sample data set should be within 0.75 percent (1/4 times the value used for 960 Hz). The sample number of data used for fault analysis derived using the proposed method is 1972. The actual fault location was 2.64 miles from Station A. The proposed algorithm gives a closer result to the actual fault location than that calculated by using data from other faulted cycles for the same impedance-based fault location methods.

Table 3-4 : Comparison of fault location results for Case 2

	At instant of identification of fault inception	Half cycle after fault inception	Proposed Method	Two cycles after fault inception	Two and a half cycles after fault inception
Sample number of data obtained for fault analysis	1908	1940	1972	2036	2068
Reactance (miles)	22.04	9.57	3.11	3.13	3.13
Takagi (miles)	23.87	9.56	3.11	3.13	3.13
Novosel (miles)	-	9.63	3.12	3.16	3.15

The above results show that the proposed method is a suitable technique for obtaining the appropriate fault current and voltages. Having processed the fault record and obtained the fault current and voltages, they can be used in to estimate the fault location. The following chapters discuss model-based fault location process using reduced equivalent circuit.

4. AUTOMATED FAULT LOCATION USING REDUCED EQUIVALENT CIRCUIT FOR MODEL-BASED FAULT LOCATION APPROACH

The previous chapters had highlighted the need for an automated fault location method and an outline of the proposed automated fault location method using reduced equivalent circuit method. The working scheme and some of the advantages of using the proposed approach have also been discussed in the previous chapters. This chapter discusses in detail the implementation of the proposed approach.

First, the system model used for demonstrating the proposed approach is described followed by the procedure for formation of reduced equivalent circuits in OpenDSS. The modeling of different power system components in openDSS is also explained. This is followed by implementation of the proposed fault location approach using MATLAB.

4.1 SOFTWARE TOOLS USED

The approach is universal as explained in Chapter 2. Most of the present day commercially available power system packages have the capability to form equivalent circuits. Here, reduced equivalent circuits modeled in OpenDSS which are driven by MATLAB is used to find fault location. Hence, it is independent of the software used by utility in which they have their system model.

CAPE is a prominent software for power system protection engineering and is used widely by utilities across the world. To illustrate the proposed method, an example system model present in CAPE is used throughout the thesis for implementation, analysis and validation of the proposed method.

4.1.1: CAPE - Computer-Aided Protection Engineering

CAPE is a powerful tool developed for protection engineers dealing with high voltage transmission and distribution systems. CAPE has several modules for this purpose

such as Database Editor, Short-Circuit, One Line Diagram, Coordination Graphics, Relay Setting, Relay Checking, System Simulator, Line Constants and Power Flow [7] The hardware requirements for CAPE are simple. It runs on Windows PC and supports any Windows compatible printer.

CAPE uses the Short-Circuit Module for fault studies. The process of fault study is simplified by using the One-Line Diagram interface it provides. Along with the conventional fault types such as balanced three-phase, phase-to-phase (line-to-line), balanced two-phase-to-ground and one-phase-to-ground (single-line-to-ground) faults, CAPE allows the users to define a fault condition consisting of any connection among different phases and ground with fault impedance at any place on the network. Hence, real life fault conditions such as fallen conductors or simultaneous faults involving several buses with arbitrary impedances or current injections can be studied. Furthermore, CAPE has Short-Circuit Reduction Module which can reduce large circuit into a small equivalent circuit. The components of the reduced equivalent circuit exhibit the same characteristics as that it exhibited when it was part of the large circuit model.

CAPE provides the user with a variety of tools and options to model the network accurately and in detail. The fault analysis study can be made more accurate by providing precise initial system conditions rather than using a flat prefault voltage profile. The Power Flow module in CAPE can be used to give these initial conditions to Short-Circuit module.

As CAPE has the ability to model a particular system in great detail, the data conversion ability is of great importance as it allows CAPE to import data from several other software such ASPEN as well as export network data into similar formats. Though CAPE cannot be driven by an external software, the capability to export data accurately is used to obtain reduced equivalent circuit data to be modeled in OpenDSS.

4.1.2: OpenDSS - Open Distribution System Simulator

The Open Distribution System Simulator (*OpenDSS*, or simply, *DSS*) [16] is a comprehensive electrical system simulation tool. OpenDSS can perform a variety of RMS steady-state analysis. In addition, it supports many new types of analyses that are designed to meet future needs. OpenDSS is capable of performing power flow calculations and study harmonics, dynamics and faults in a power system.

OpenDSS is implemented as both a stand-alone executable program and a COM DLL designed to be driven from a variety of existing software platforms. For example, it can be driven entirely from an MS Office tool through VBA, or from any other 3rd party analysis program that can handle COM. OpenDSS is commonly driven by the familiar Mathworks MATLAB program. The COM interface also provides direct access to the text-based command interface as well as numerous methods and properties for accessing many of the parameters and functions of the simulator's models. Many of the results can be retrieved through the COM interface as well as from various output files. Output files are typically written in Comma-separated Value (CSV) format that can be imported easily into other tools for post processing. This provides powerful external analytical capabilities as well as excellent graphics for displaying results, hence, making it is easier to understand and analyze the results.

4.1.3: MATLAB

MATLAB [17] is a very common software used by engineers and scientists worldwide to analyze and design systems. MATLAB offers a plethora of tools to choose from to perform a variety of operations. The MATLAB platform has been optimized for solving engineering and scientific problems. The matrix-based MATLAB language makes it is easy to express computational mathematics. Built-in graphics make it easy to visualize

and gain insights from data. A vast library of prebuilt toolboxes helps users to implement algorithms effortlessly and efficiently.

4.2 System Model Used

For the purpose of analysis and verification of the proposed algorithm, the example circuit available in CAPE called “cape.gdb” is used. The database file of the test system is a repository of all the network data of the test system. Several reduced equivalent circuits will be made from this circuit model and fault analysis will be performed to demonstrate the capabilities of model-based fault location using reduced equivalent circuit algorithm.

This sample circuit has 103 buses, 187 branches, 26 sets of lines with mutual coupling and 2 sets of bus ties present. Figure 4-1 shows the one line diagram representation of the circuit.

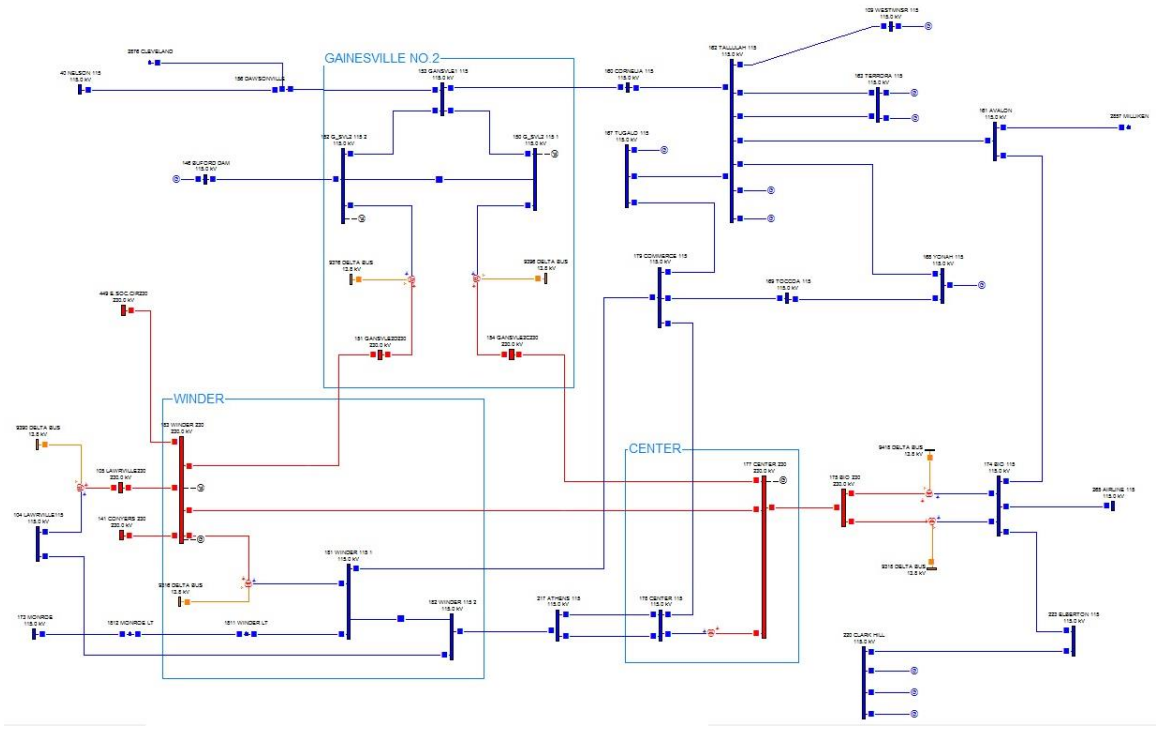

Figure 4-1 : One line diagram of cape.gdb

4.3 FORMATION OF REDUCED EQUIVALENT CIRCUITS IN CAPE

The advantages of forming reduced equivalent circuit have been discussed in Chapter 2. Most commercial power system analysis software offer a network reduction module. This section shows how to form reduced equivalent network using CAPE.

CAPE uses two methods of network reduction. In the first method, CAPE completely reduces the specified set of buses, leading to an equivalent network with a minimum number of buses but with possibly many additional equivalent sources and impedances. In the second method, CAPE retains some extra buses in an attempt to minimize the number of equivalent branches created. [18]. Throughout the thesis, the first method of circuit reduction is used.

The steps to reduce the network are as follows:

1. Load the database file into CAPE
2. Select the Short Circuit Reduction module and create a new bus set as shown in Figure 4-2. This bus set may be the set of buses you want to reduce or the set of buses you want to retain. Add the set of buses you want to reduce/retain to that bus set.
3. Once the bus set is defined, select reduce set if you want to remove the selected buses from the system or select retain to retain the selected set of buses and remove all the other buses. A sample circuit after network reduction is shown in Figure 4-3 where only certain buses near Gainesville station are retained and all the other buses are removed. It can also be observed that several new branches and generators have been added to the existing set of lines and generators to be able to replicate the retained system's behavior before network reduction.

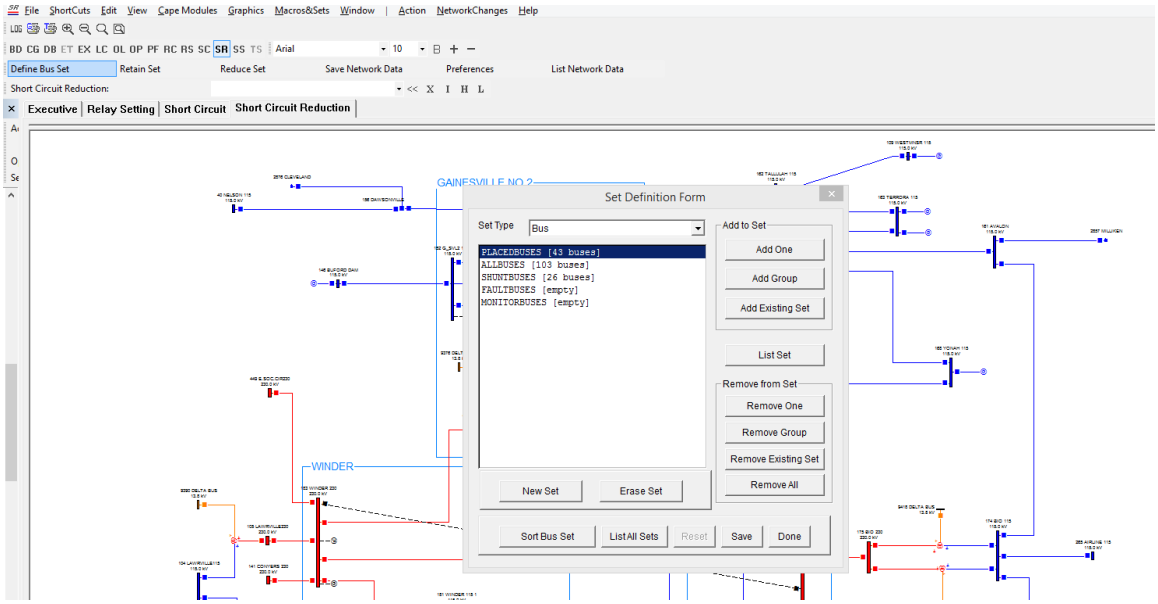

Figure 4-2 : Network reduction using CAPE – 1

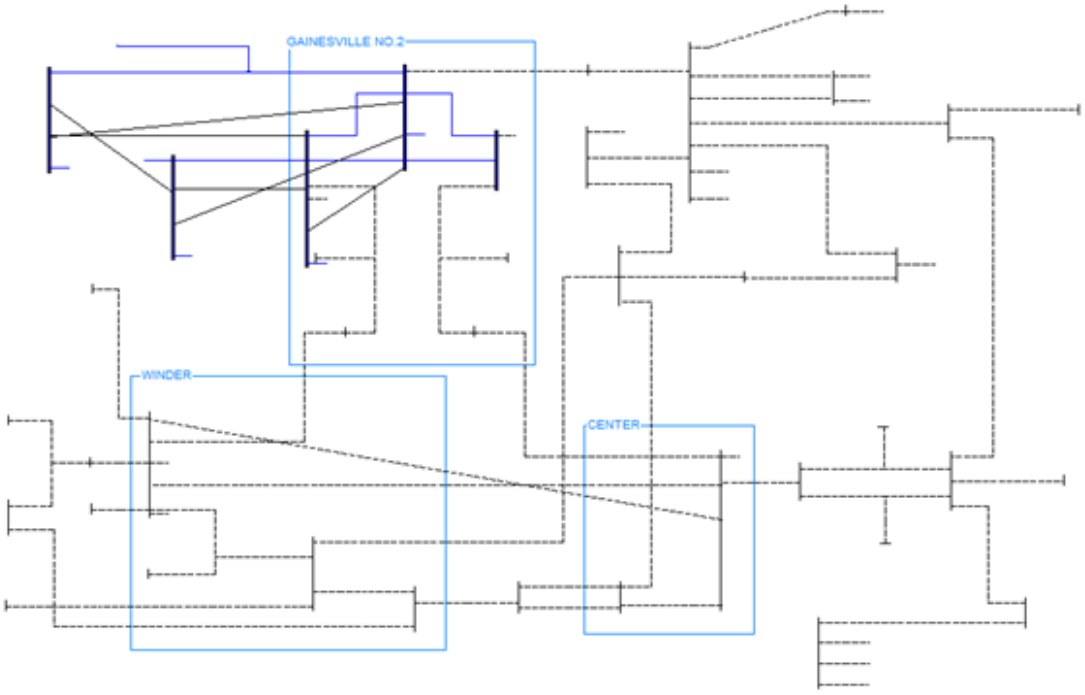

Figure 4-3 : Network reduction using CAPE – 2

4. After the system has been reduced, the network data can be saved as a new database file which can be used as and when required. The reduced network data is also exported to build reduced equivalent circuits in OpenDSS.

4.4 MODELING IN OPENDSS

This section presents the data exported by CAPE and the data required by OpenDSS to model the components of a power system. This section discusses four major components commonly encountered while forming reduced equivalent circuits for the purpose of fault location. These are generators, transmission lines, tie bus and mutual coupling.

OpenDSS does not require the list of buses to be defined at the beginning. If a bus name is not present at the time of creating any power system component, a new bus is created with that name.

4.4.1 Generator

CAPE exports the following details for a generator: bus voltage, bus name and bus number to which the generator is connected, MVA rating of the generator and positive-, negative- and zero-sequence impedance parameters of the generator.

A generator model can be created in OpenDSS either by defining its short-circuit capacity or by directly defining its impedance parameters. In this case, the generators are defined using the impedance parameters as all the required impedance data are available. The other requirements to create a generator in OpenDSS are the bus to which the generator is connected, the base kV of the generator, per unit value of the generated voltage, phase angle shift (if present), the frequency of the generator and the number of phases present (which is 3 by default).

4.4.2 Transmission Line

CAPE exports the following details for branches or transmission lines: bus number and bus name of from bus and to bus, operating line voltage and impedance parameters of the line. Transmission lines are simple to define in OpenDSS. The above parameters are sufficient to define a line in OpenDSS. The line length is taken as unity while defining in OpenDSS as CAPE is made to export total impedance of the line and not impedance per unit length so that it is easy to implement sliding fault analysis. Fault location is represented in terms of percentage distance of the total line length from a bus at one end of the line.

To create a fault at distance 'x' per unit (pu) from Bus A on a transmission line of length '1 (one)' pu in OpenDSS, a temporary bus has to be created at the point of fault on the transmission line between the two buses. This temporary bus splits the transmission line into two lines, one with length 'x' and other with length 'l-x' as shown in Figure 4-4.

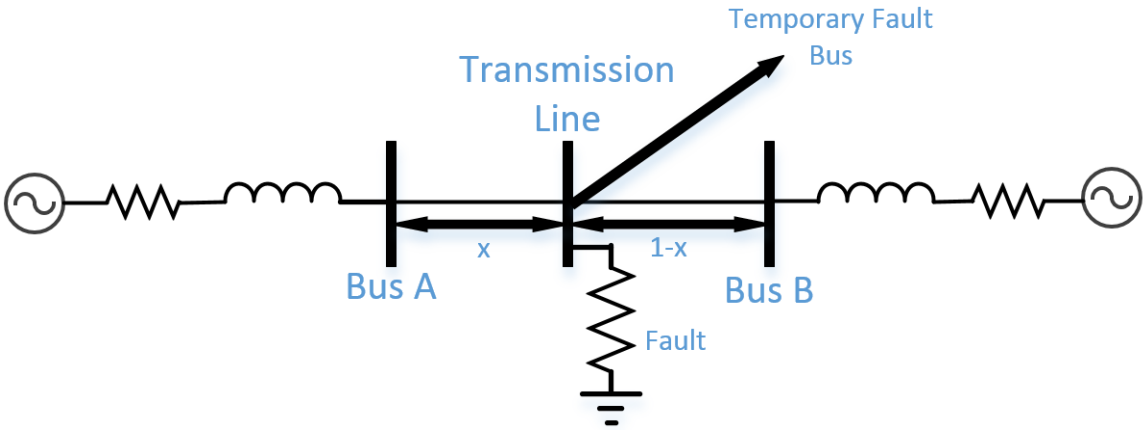

Figure 4-4 : Transmission Line Fault in OpenDSS

The ability of OpenDSS to be driven by MATLAB gives the advantage of being able to vary 'x' and obtain results for each case without any manual intervention to get fault data for faults at various distances.

4.4.3 Bus Tie

A tie breaker acts as a coupler between feeders for circuits with two feeders or more. During failure of any one feeder, the power is fed through the second feeder and tie breaker. Bus tie data in CAPE are from bus, to bus and status of breaker which is open or closed.

In OpenDSS, a bus tie which is closed is modeled as a line with almost zero impedance between the two buses which acts as a closed switch between two buses. When a bus tie is open, the line is not modeled at all. Hence, it is like an open switch.

4.4.4 Mutual Coupling

Mutual coupling between transmission lines is a common phenomenon that occurs when two lines travel close to each other, for example, in the same tower. As a result, it affects the transmission line impedance and the fault characteristics of the system. Hence, two parallel lines which are affected by mutual coupling cannot be modeled in the similar manner as normal transmission lines explained in Section 4.4.2.

Mutual coupling mainly affects the zero-sequence parameters in a transmission line [19]. Hence, its effect can be observed majorly in unbalanced ground faults and not in three-phase faults. The positive- and negative-sequence circuits are unaffected and need not be modified. In CAPE, the mutual coupling data are given as follows: from and to bus data of the first line, from and to bus data of the second line and mutual impedance parameters between the two lines.

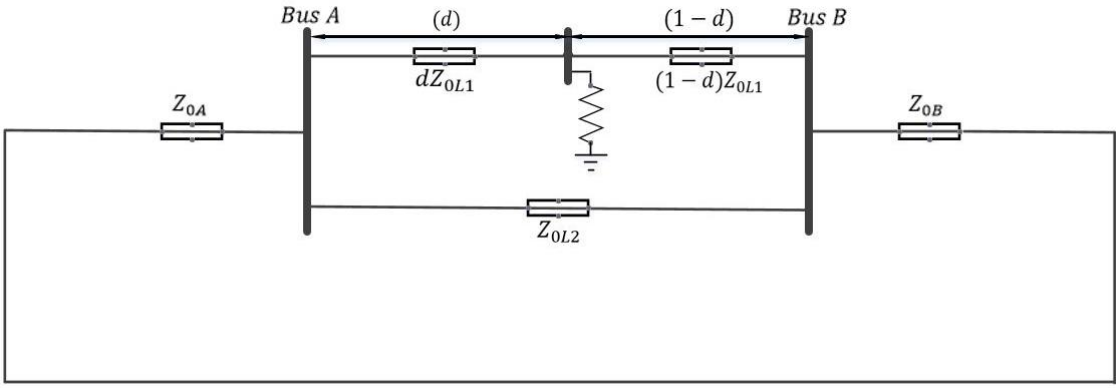

Figure 4-5 : Zero-sequence circuit without mutual coupling

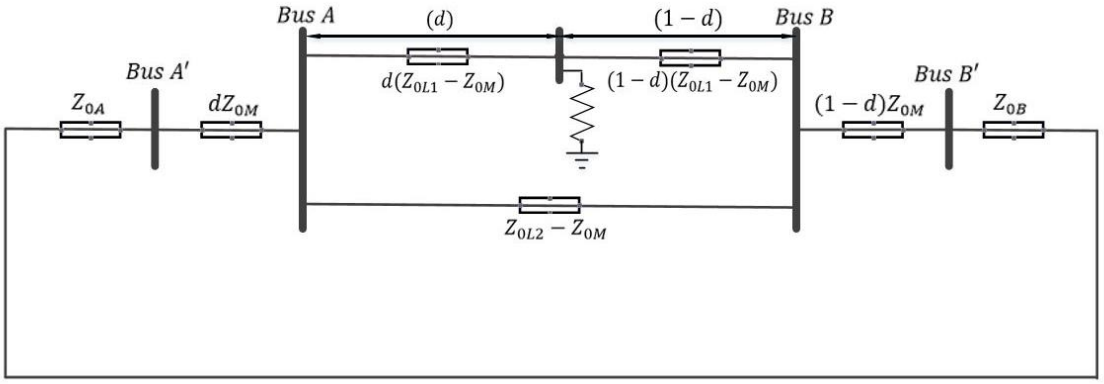

Figure 4-6 : Effect of mutual coupling on zero-sequence circuit

In OpenDSS, as the positive- and negative-sequence line parameters are unaffected, the positive- and negative- sequence line impedances are not modified and modeled like two normal transmission lines discussed in Section 4.4.2. The modeling of zero-sequence circuit showing the effect of mutual coupling is presented in Figure 4-6 [20] .

Once again, the ability of OpenDSS to be driven by MATLAB gives the advantage of being able to vary the modeling of transmission lines and its parameters according to our requirement without any manual intervention. When mutual coupling data is read by MATLAB, the zero-sequence parameters of the corresponding lines are changed as well as the way the lines are modeled are modified from the circuit diagram shown in Figure

4-5 to the circuit diagram shown in Figure 4-6. The zero-sequence parameter of line 1 is changed from Z_{0L1} to Z_{0L1}-Z_{0M} and zero-sequence parameter of line 2 is changed from Z_{0L2} to Z_{0L2}-Z_{0M}. Two new buses are introduced (Bus A' and Bus B') at each end of the transmission line between the ends of the transmission line and the rest of the reduced equivalent circuit as shown in Figure 4-6. A line of impedance dZ_{0M} is introduced between Bus A and Bus A' and another line of impedance $(1-d)Z_{0M}$ is introduced between Bus B and Bus B' where 'd' is the distance of the fault from Bus A. When there is no fault, 'd' is zero. Z_{0A} and Z_{0B} are source impedances on the sides of Bus A and Bus B respectively. The rest of the reduced equivalent circuit around the mutually coupled line is represented in the circuit diagram shown in Figure 4-6 using Z_{0A} and Z_{0B}.

4.5 Implementation of Proposed Approach in MATLAB

In Chapter 2, the usefulness of MATLAB being able to drive OpenDSS has been discussed. This section discusses the how the proposed algorithm is implemented using MATLAB and OpenDSS.

Preprocessing of fault records is a key step as described in Chapter 3.The outcome of the above process gives the fault voltage and fault current of the fault event. Using the DFR data, the location of the fault recorder and the appropriate equivalent circuit is selected. The above steps have been accomplished using MATLAB. MATLAB polls the folder where fault record arrives at regular intervals to process new fault records as and when they reach the monitored folder. This is followed by the preprocessing steps described in Chapter 3.

The required equivalent circuit data exported by CAPE is available in ".csv" file format. This data is read by MATLAB and dynamically creates the circuit in OpenDSS. Additionally, MATLAB is programmed to place monitors at all the ends of all the lines to

obtain the current and voltage measurement which can be used for analysis other than fault location. A sliding fault is placed on each line and the voltages and currents corresponding to each fault scenario at all the locations being monitored are available. The resolution of the sliding fault can be varied according to the requirement, for example, the sliding fault can be programmed to create a fault at every 10% of the total line distance or it can be programmed to create a fault at every 5% of the total line distance. Similarly, the above sliding fault analysis can be performed with various fault resistances as well. The voltages and current measurements obtained for different fault scenarios are made into a table for simplifying the analysis.

The actual fault current and voltage is then compared with the current and voltage measurements obtained by simulations. The closest match in the comparison process gives the fault location. Once the database consisting of library of equivalent circuits exported by CAPE is set up, the above method can estimate the fault location as and when a new fault record is received without any human intervention.

5. ANALYSIS OF REDUCED EQUIVALENT CIRCUIT BASED FAULT LOCATION METHOD

The usefulness and success of an algorithm or technique depend on its technical capability as well as its ease of usage. The functioning and capability of a proposed method are identified by testing the proposed method in various aspects and in a variety of scenarios. This chapter discusses in detail the various aspects of the algorithm that had been analyzed to verify the robustness of the proposed method to the common scenarios faced by utilities.

The analysis in this chapter is made by comparing the results obtained using the full circuit model in CAPE and the results obtained using reduced equivalent circuit implemented using MATLAB and OpenDSS. This ensures that the reduced equivalent circuit in OpenDSS behaves in the same way as the full circuit model in CAPE as well as the benefits of using reduced equivalent circuit in OpenDSS is also reaped. The full circuit model used in CAPE is a classical short-circuit model. Hence, it does not have any load currents. All the faults scenarios presented this chapter are single-line-to-ground faults (SLG faults) on phase A as it is the most commonly occurring type of transmission line fault.

5.1 REDUCED EQUIVALENT CIRCUIT VALIDATION

This section verifies the short-circuit characteristics of the reduced equivalent circuit using an appropriate example circuit as shown in Figure 5-1. This is done by comparing the fault characteristics of the reduced equivalent circuit implemented using MATLAB and OpenDSS and that of the full model present in CAPE. The black box in Figure 5-1 shows the portion of reduced equivalent circuit. The circuit shown in Figure 5-2

is chosen such that all the locations which are 1 bus away from Bus 153 (Gansvle1 115) are included in the reduced equivalent circuit as well as a pair of lines with mutual coupling are also present. Bus 40 (Nelson 115) and 2876 (Cleaveland) have also been included in the reduced equivalent circuit to check if fault location can be correctly estimated when faults are much farther away from the point of measurement and also verify the suitability of one equivalent circuit for DFRs at different locations.

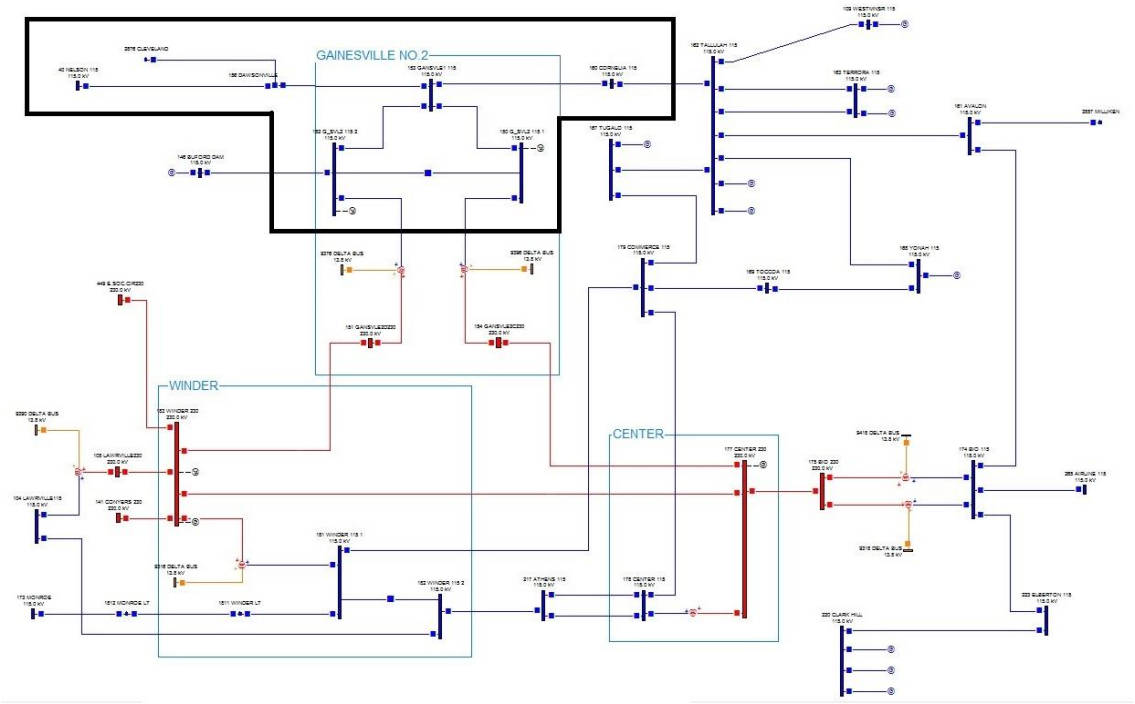

Figure 5-1 : Reduced Equivalent Circuit -1

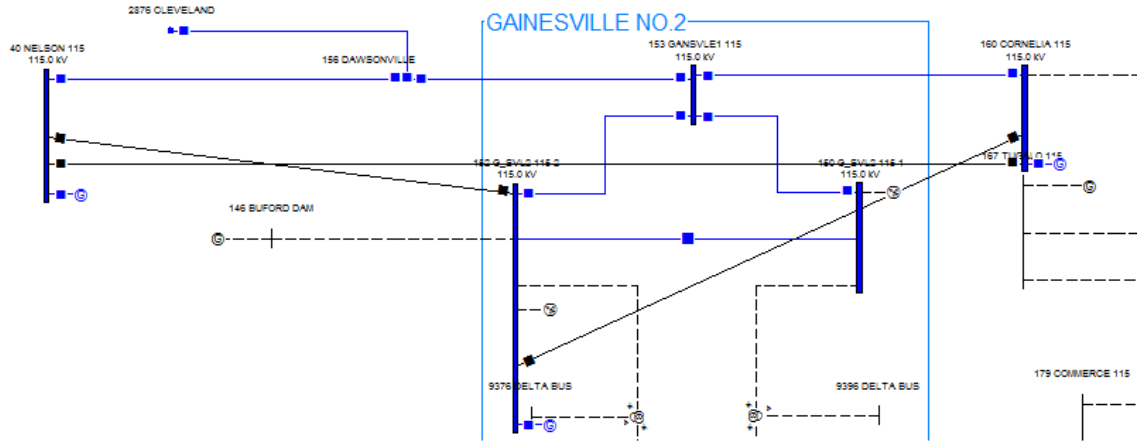

Figure 5-2 : Reduced Equivalent Circuit -2

It can be observed from Figure 5-2 that equivalent sources and impedances have been introduced during the process of circuit reduction. As discussed in Chapter 4, this form of circuit reduction reduces the number of buses as required and introduces equivalent sources and impedances to emulate the original short-circuit characteristics after reduction. Also, faults on the newly created equivalent impedances after circuit reduction can be ignored as these lines are not actually present in the original power system.

Table 5-1 : Equivalent circuit validation

SLG fault (phase A) on the line between Bus 153 and Bus 156 at 20% of line length from Bus 153 with fault resistance of 0 Ohms						
	Line currents from Bus 153 (A)			Line currents from Bus 156 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit (CAPE)	4693.02 ∠ -76.7	7.94003 ∠ 97.3	7.94003 ∠ 97.3	1245.27 ∠ -73.7	7.94003 ∠ -82.7	7.94003 ∠ -82.7
Reduced equivalent circuit (MATLAB and OpenDSS)	4693.02 ∠ -76.7	7.94003 ∠ 97.3	7.94003 ∠ 97.3	1245.27 ∠ -73.7	7.94003 ∠ -82.7	7.94003 ∠ -82.7
Fault Location Detection	Fault at line between Bus 153 and Bus 156 at 20% of line length from Bus 153 with fault resistance of 0 Ohms					
SLG fault (phase A) on the line between Bus 156 and Bus 2876 (remote line) at 20% of line length from Bus 2876 with fault resistance of 1 Ohms						
	Line currents from Bus 156 (A)			Line currents from Bus 2876 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit (CAPE)	1344.86 ∠ -72.6	0.0000	0.0000	0.0000	0.0000	0.0000
Reduced equivalent circuit (MATLAB and OpenDSS)	1344.86 ∠ -72.6	0.0000	0.0000	0.0000	0.0000	0.0000
Fault Location Detection	Fault at line between Bus 156 and Bus 2876 at 20% of line length from Bus 2876 with fault resistance of 1 Ohms					

Table 5-1 continued

SLG fault (phase A) on the line between Bus 153 and Bus 152 (mutually coupled line) at 50% of line length from Bus 153 with fault resistance of 0.4 Ohms						
	Line currents from Bus 153 (A)			Line currents from Bus 152 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit (CAPE)	3252.52 ∠ -74.9	145.691 ∠ 110.4	145.691 ∠ 110.4	5375.81 ∠ -78.2	145.691 ∠ -69.6	145.691 ∠ -69.6
Reduced equivalent circuit (MATLAB and OpenDSS)	3252.52 ∠ -74.9	145.691 ∠ 110.4	145.691 ∠ 110.4	5375.81 ∠ -78.2	145.691 ∠ -69.6	145.691 ∠ -69.6
Fault Location Detection	Fault at line between Bus 153 and Bus 152 at 50% of line length from Bus 153 with fault resistance of 0.4 Ohms					

Table 5-1 shows the fault currents obtained in full circuit model implemented in CAPE and the reduced equivalent circuit implemented in OpenDSS at different fault location with different fault impedances. The three fault scenarios considered are faults on three different lines chosen such that they represent three different types of lines which are most common in a power network. Hence, different cases taken for studying the performance of the proposed fault location algorithm involves analyzing different aspects of these lines with similar fault conditions.

The first fault scenario considered is an SLG fault on phase A in the line between Bus 153 and Bus 156 at 20 % of line length from Bus 153 with a fault resistance of 0 ohms. This line has been chosen because it represents one of the most common scenarios where the line is part of a network with interconnections on both ends of the line. When the line is faulted, the fault current can flow from both ends of the line into the fault. From Table 5-1, it can be observed that the line currents flowing into the fault from Bus 153 in the full circuit model implemented in CAPE are 4693.02∠-76.7, 7.94003∠97.3 and 7.94003∠97.3

corresponding to phase A, phase B and phase C respectively. The line currents flowing into the fault from Bus 156 are 1245.27∠-73.7, 7.94003∠-82.7 and 7.94003∠-82.7 corresponding to phase A, phase B and phase C respectively. It can be observed that the same current values are obtained for the same fault condition implemented using reduced equivalent circuit in OpenDSS.

The second fault scenario is an SLG fault on phase A in the line between Bus 156 and Bus 2876 at 20% of line length from Bus 2876 with fault resistance of 1 Ohms. This line has a remote terminal at one end. Hence, when this line is faulted, fault current flows in only from Bus 156. As mentioned earlier in this chapter, the full circuit model used in CAPE for analysis is a classical short circuit model which does not take the load currents into consideration. As a result, for a fault on phase A, the fault current flowing in from Bus 156 is only on phase A and there is no fault current flowing in other phases. The third fault scenario considered is an SLG fault on phase A in the line between Bus 153 and Bus 152 at 50% of line length from Bus 153 with fault resistance of 0.4 Ohms. This line is a mutually coupled with another line between Bus 150 and Bus 153. Similar to the first fault scenario, it can be observed that the same current values are obtained for the same fault condition implemented using reduced equivalent circuit in OpenDSS and full circuit model implemented in CAPE.

The results shown in Table 5-1 demonstrate that the reduced equivalent circuit (formed using the Short Circuit Reduction module in CAPE and then implemented in OpenDSS using MATLAB) produce identical fault characteristics of that of the full circuit system present in CAPE. This shows the system behavior is preserved and no error is introduced during the process of formation of reduced equivalent circuit or while implementing in OpenDSS using MATLAB.

5.2 SIZE OF CIRCUIT

The complexity of a power system can vary from location to location. Hence, the size of the required equivalent circuit may vary from a small circuit consisting of only 3 buses to a large circuit as large as 10 or more buses. In this section, a small as well as a large reduced circuit is tested to show that the proposed method is capable of handling circuits of any size.

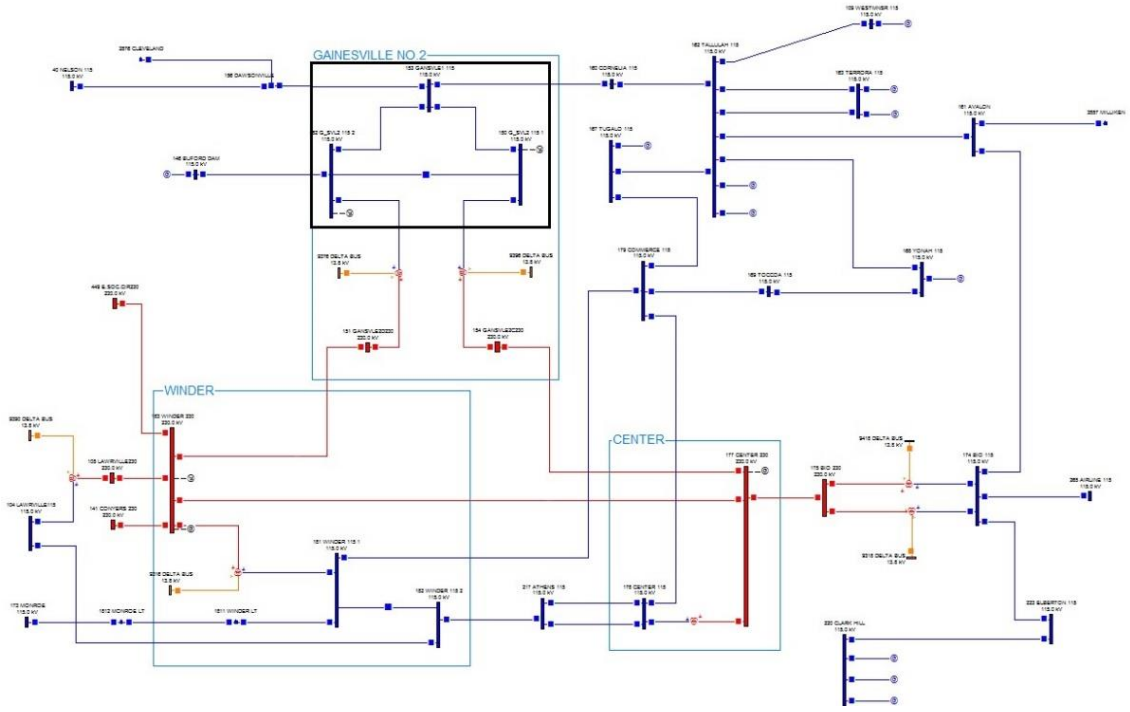

Figure 5-3 : Small reduced equivalent circuit – 1

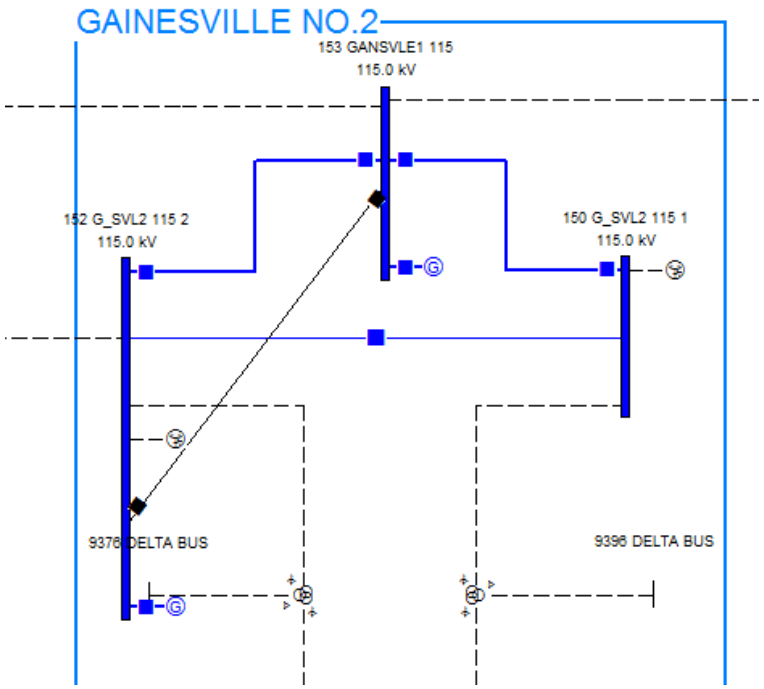

Figure 5-4 : Small reduced equivalent circuit – 2

Table 5-2 : Equivalent circuit validation for small circuit

SLG fault (phase A) on the line between Bus 153 and Bus 152 at 70% of line length from Bus 152 with fault resistance of 0.4 Ohms						
	Line currents from Bus 153 (A)			Line currents from Bus 152 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit	4056.03 ∠ -75.0	121.584 ∠ 110.9	121.584 ∠ 110.9	4141.04 ∠ -78.2	121.584 ∠ -69.1	121.584 ∠ -69.1
Reduced equivalent circuit	4056.03 ∠ -75.0	121.584 ∠ 110.9	121.584 ∠ 110.9	4141.04 ∠ -78.2	121.584 ∠ -69.1	121.584 ∠ -69.1
Fault Location Detection	Fault at line between Bus 153 and Bus 152 at 70% of line length from Bus 152 with fault resistance of 0.4 Ohms					
SLG fault (phase A) on the line between Bus 153 and Bus 150 at 60% of line length from Bus 153 with fault resistance of 0.1 Ohms						
	Line currents from Bus 153 (A)			Line currents from Bus 150 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit	2926.88 ∠ -76.8	202.737 ∠ 107.7	202.737 ∠ 107.7	6573.70 ∠ -80.7	202.737 ∠ -72.3	202.737 ∠ -72.3
Reduced equivalent circuit	2926.88 ∠ -76.8	202.737 ∠ 107.7	202.737 ∠ 107.7	6573.70 ∠ -80.7	202.737 ∠ -72.3	202.737 ∠ -72.3
Fault Location Detection	Fault at line between Bus 153 and Bus 150 at 60% of line length from Bus 153 with fault resistance of 0.1 Ohms					

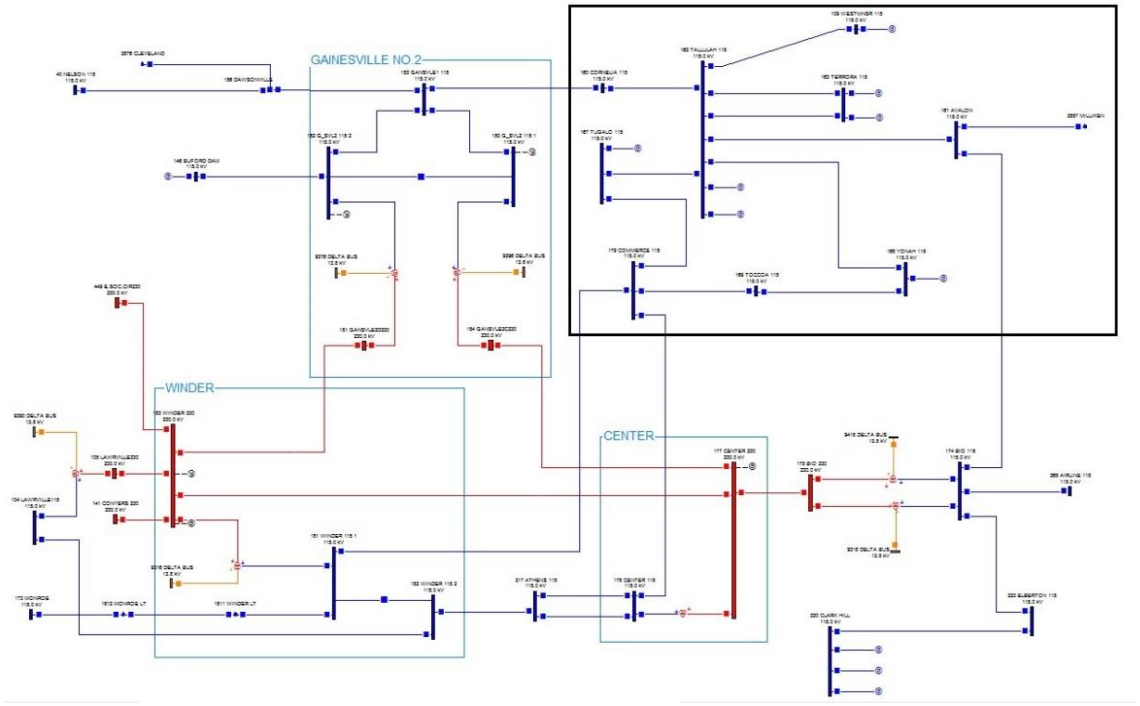

Figure 5-5 : Large reduced equivalent circuit – 1

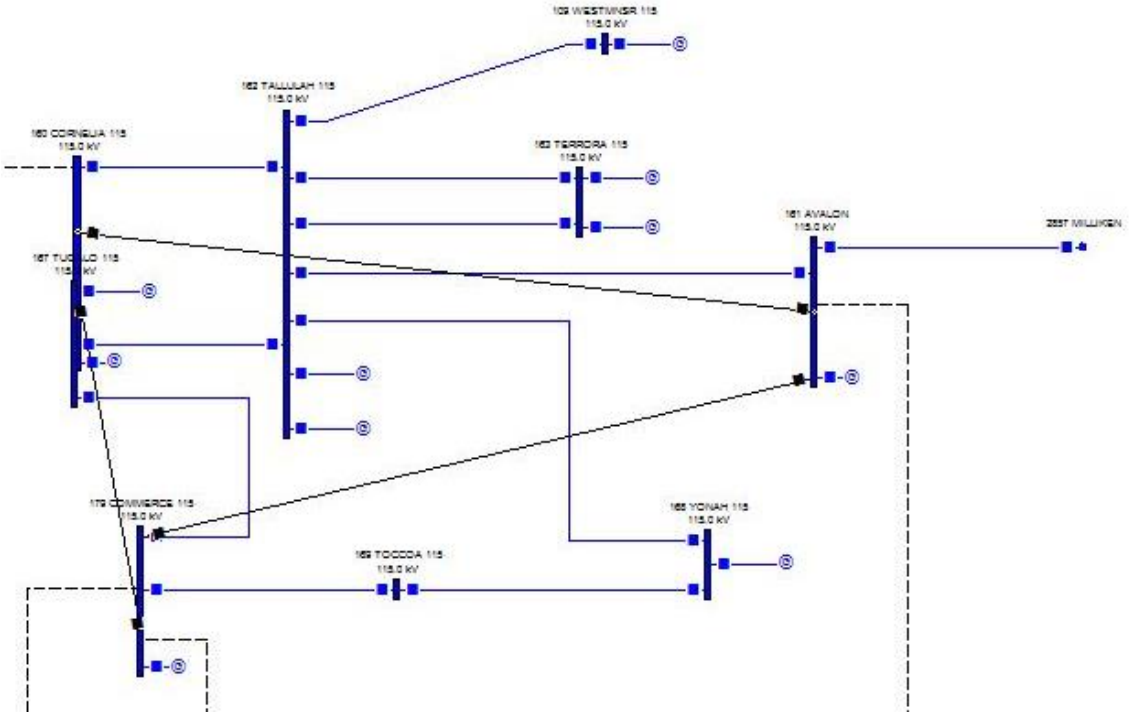

Figure 5-6 : Large reduced equivalent circuit – 2

Table 5-3 : Equivalent circuit validation for large circuit

SLG fault (phase A) on the line between Bus 162 and Bus 161 at 50% of line length from Bus 161 with fault resistance of 0 Ohms						
	Line currents from Bus 161 (A)			Line currents from Bus 162 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit	1245.14 ∠ -75.3	53.6853 ∠ 93.4	53.6853 ∠ 93.4	3084.51 ∠ -74.1	53.6853 ∠ -86.6	53.6853 ∠ -86.6
Reduced equivalent circuit	1245.14 ∠ -75.3	53.6853 ∠ 93.4	53.6853 ∠ 93.4	3084.51 ∠ -74.1	53.6853 ∠ -86.6	53.6853 ∠ -86.6
Fault Location Detection	Fault at line between Bus 162 and Bus 161 at 50% of line length from Bus 161 with fault resistance of 0 Ohms					
SLG fault (phase A) on the line between Bus 169 and Bus 168 at 10% of line length from Bus 169 with fault resistance of 0.5 Ohms						
	Line currents from Bus 169 (A)			Line currents from Bus 168 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit	1338.58 ∠ -72.4	121.934 ∠ 115.3	121.934 ∠ 115.3	3112.29 ∠ -72.8	121.934 ∠ -64.7	121.934 ∠ -64.7
Reduced equivalent circuit	1338.58 ∠ -72.4	121.934 ∠ 115.3	121.934 ∠ 115.3	3112.29 ∠ -72.8	121.934 ∠ -64.7	121.934 ∠ -64.7
Fault Location Detection	Fault at line between Bus 169 and Bus 168 at 10% of line length from Bus 169 with fault resistance of 0.5 Ohms					

Figure 5-4 shows a small circuit with just 3 buses and Figure 5-6 shows a large equivalent circuit consisting of 10 buses. From Table 5-2 and Table 5-3, it can be observed that the fault current flowing in each phase from two ends of the faulted line in the full circuit model implemented using CAPE and the reduced equivalent circuit implemented using OpenDSS are identical The above two cases are extreme cases and the results present in Table 5-2 and Table 5-3 demonstrate that the reduced equivalent circuit is able to exhibit

the same short-circuit characteristics as that of the full circuit model. Hence, the formation of reduced equivalent circuit is successful irrespective of the size of the reduced network. Another advantage this presents is that a single equivalent circuit can be used for obtaining fault location for data from different fault recorders. This can eliminate the need for a separate equivalent circuit for each fault recorder but limitations on the size of the circuit are discussed in Section 5.5.

5.3 FAULT RESISTANCE

One of the major advantages of model-based fault analysis is the ability to emulate the power system condition and fault scenario so as to obtain high accuracy in results. Hence, the better the modeling of the system as well as the fault scenario and minimizing any assumptions which may be made, more accurate the fault location estimates will be. One of the key components modeling the fault scenario is the fault impedance as it affects the fault current and fault voltage.

Fault impedance is present because of the presence of an object which has an impedance between an energized line and ground or between two or more energized lines. Fault impedance is usually resistive in nature and is caused because by objects such as trees and animals. As discussed earlier, single line-ground fault is the most common transmission line fault case. Figure 5-7 shows the circuit diagram for a single line to ground fault analysis.

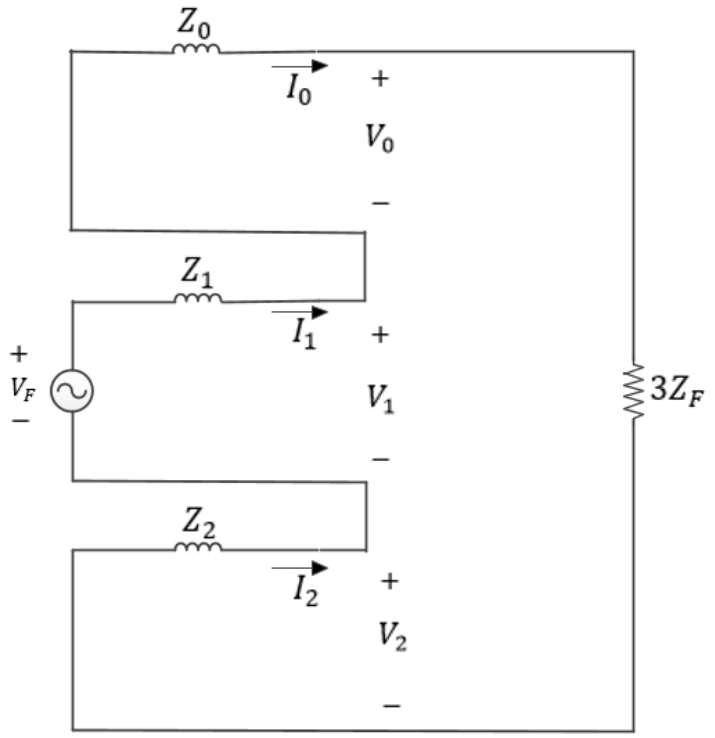

Figure 5-7 : Single line to ground fault analysis

$$Phase\ Current\ (I_a) = I_0 + I_1 + I_2 = 3I_1 = \frac{3V_F}{Z_0 + Z_1 + Z_2 + 3Z_F}$$ Equation 5-1

From Equation 5-1, it can be observed that variation of fault resistance, affects the real and imaginary component of the fault current or the fault current phasor's magnitude and angle. Furthermore, as fault impedance is resistive in nature, the fault current phasor in this case will not overlap with fault current phasors obtained while placing faults at various distances along the transmission line (because transmission lines are primarily inductive in nature). This is illustrated in the following paragraphs using Figure 5-8 and Figure 5-9.

Consider the reduced equivalent circuit shown in Figure 5-2. Figure 5-8 shows the variation of fault current with resistance on the transmission line between Bus 153 and Bus

156 with monitor placed at Bus 153 monitoring the faulted line. Single line- ground faults on phase A were created at several locations along the entire transmission line for each fault resistance value and the resulting phase A fault currents obtained has been plotted. It can be observed that varying the fault resistance causes lines parallel to the corresponding bolted fault case and does not overlap with any other case. Hence, this ensures that the fault location estimate using the proposed method will not be affected by fault impedance. Furthermore, the fault impedance could also be identified.

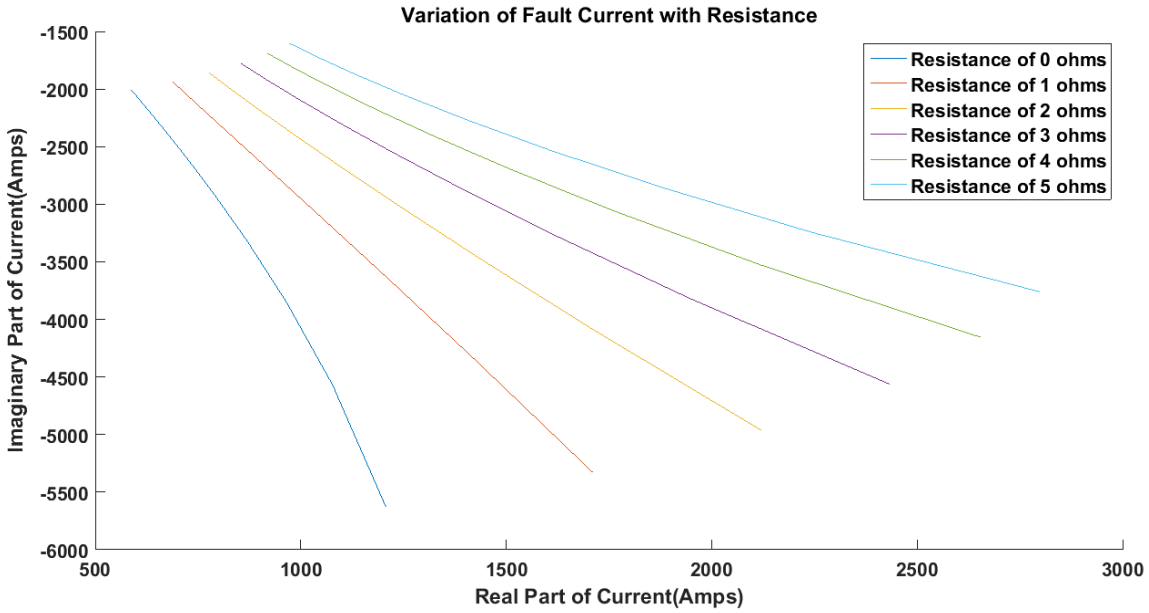

Figure 5-8 : Variation of fault current with resistance - 1

This property is exhibited irrespective of whether the line is mutually coupled or not. Consider another example where the transmission line is mutually coupled to another line. Figure 5-9 shows the variation of fault current with resistance on a mutually coupled transmission line between Bus 152 and Bus 153 with monitor placed at Bus 153 measuring current in the faulted line. It can be seen that similar characteristics are exhibited in this case as well.

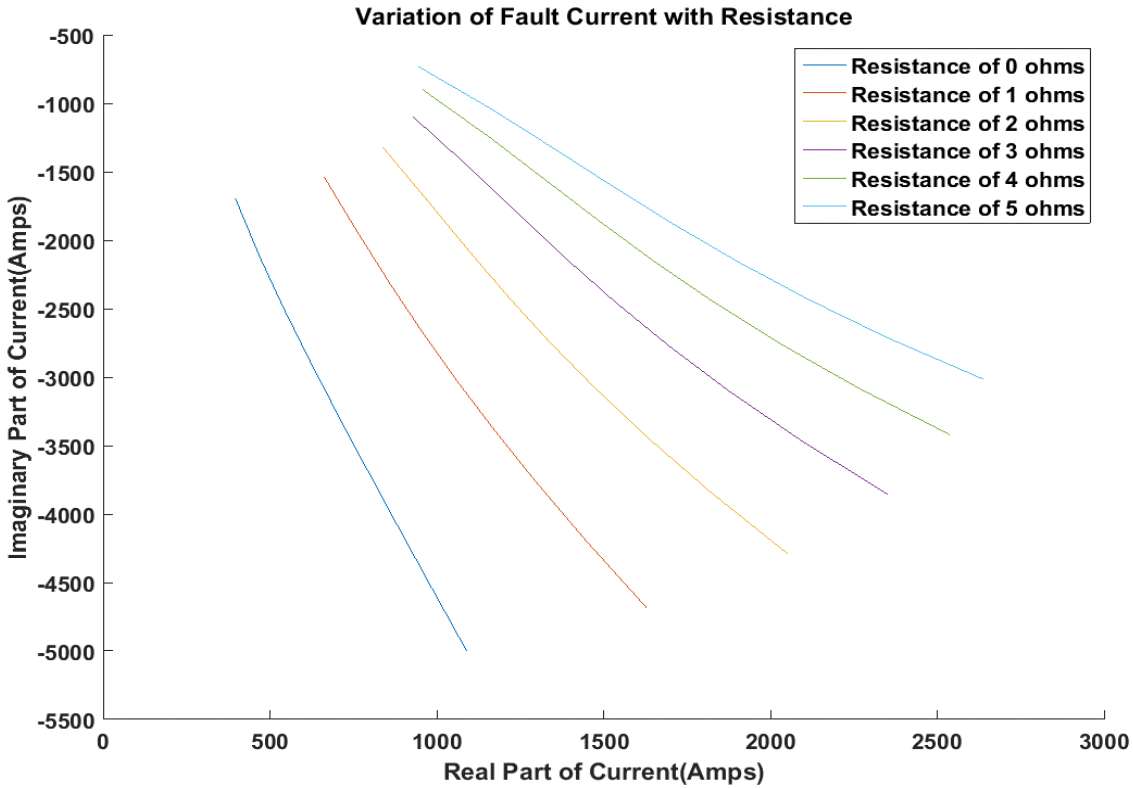

Figure 5-9 : Variation of fault current with resistance - 2

Hence, it can be concluded that the presence of fault resistance does not hinder the proposed fault location algorithm. MATLAB is programmed to drive OpenDSS to simulate cases with different fault resistance as well and the data obtained is used to estimate fault location when fault impedance is present.

5.4 Line Configuration Change and Generator Outage

The proposed algorithm requires forming a library of reduced equivalent circuits. The library of equivalent circuits is a simplified representation of the existing system conditions. The system conditions regularly keep changing because of outages caused due to a variety of reasons and one of the most common reason is maintenance. Every utility keeps updating the system models regularly reflecting the changes in various power system

elements. This means the library of equivalent circuits also needs to be updated accordingly. This section discusses transmission line configuration changes.

There are two cases which are analyzed. One case is where the transmission line affected is part of the reduced equivalent circuit. Another case is where the transmission line affected is out of the reduced equivalent circuit. This problem would be completely eliminated if the process of formation of reduced equivalent circuits is automated and is scope for future work.

While forming reduced equivalent circuits, the line parameters of lines which are to be present in the reduced circuit are not changed at all. Extra lines and generators are inserted in the reduced circuit to reflect the surrounding system conditions so as to reciprocate the short-circuit characteristics of the full system. Hence, if a transmission line within the reduced equivalent circuit is affected, then the changes can be reflected easily by changing the affected line's parameters in the data exported by CAPE for that reduced circuit. If the transmission line affected is out of the reduced equivalent circuit, the change in line configuration has to be made in the large circuit and reduced equivalent circuit has to be formed again. Formation of reduced equivalent circuit is a simple and quick process as shown in Section 4.3. Similar steps have to be followed for generator outage as well.

Consider the circuit in Figure 5-2 and the line between Bus 153 and Bus 150 is out of service. Table 5-4 shows the comparison between the results obtained after line outage with and without modifying the reduced equivalent circuit to reflect the change caused by line outage. As the line affected is part of the reduced equivalent circuit, the modification that was made was removing that particular line from the reduced equivalent circuit data.

Table 5-4 : Analysis of line configuration change

SLG fault (phase A) on the line between Bus 153 and Bus 156 at 20% of line length from Bus 153 with fault resistance of 0 Ohms						
	Line currents from Bus 153 (A)			Line currents from Bus 156 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit (after line outage)	3831.45 ∠ -76.3	34.2484 ∠ 105.8	34.2484 ∠ 105.8	1229.88 ∠ -73.7	34.2484 ∠ -74.2	34.2484 ∠ -74.2
Reduced equivalent circuit (without circuit modification)	4693.02 ∠ -76.7	7.94003 ∠ 97.3	7.94003 ∠ 97.3	1245.27 ∠ -73.7	7.94003 ∠ -82.7	7.94003 ∠ -82.7
Reduced equivalent circuit (after circuit modification)	3831.45 ∠ -76.3	34.2484 ∠ 105.8	34.2484 ∠ 105.8	1229.88 ∠ -73.7	34.2484 ∠ -74.2	34.2484 ∠ -74.2
Fault Location Detection	Fault at line between Bus 153 and Bus 156 at 20% of line length from Bus 153 with fault resistance of 0 Ohms					
SLG fault (phase A) on the line between Bus 156 and Bus 2876 (remote line) at 20% of line length from Bus 2876 with fault resistance of 1 Ohms						
	Line currents from Bus 156 (A)			Line currents from Bus 2876 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit (after line outage)	1326.75 ∠ -72.6	0.0000	0.0000	0.0000	0.0000	0.0000
Reduced equivalent circuit (without circuit modification)	1344.86 ∠ -72.6	0.0000	0.0000	0.0000	0.0000	0.0000
Reduced equivalent circuit (after circuit modification)	1326.75 ∠ -72.6	0.0000	0.0000	0.0000	0.0000	0.0000
Fault Location Detection	Fault at line between Bus 156 and Bus 2876 at 20% of line length from Bus 2876 with fault resistance of 1 Ohms					

Table 5-4 continued

SLG fault (phase A) on the line between Bus 153 and Bus 152 (mutually coupled line) at 50% of line length from Bus 153 with fault resistance of 0.4 Ohms						
	Line currents from Bus 153 (A)			Line currents from Bus 152 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit (after line outage)	2226.12 ∠ -71.1	260.157 ∠ 110.8	260.157 ∠ 110.8	5987.43 ∠ -78.6	260.157 ∠ -69.2	260.157 ∠ -69.2
Reduced equivalent circuit (without circuit modification)	3252.52 ∠ -74.9	145.691 ∠ 110.4	145.691 ∠ 110.4	5375.81 ∠ -78.2	145.691 ∠ -69.6	145.691 ∠ -69.6
Reduced equivalent circuit (after circuit modification)	2226.12 ∠ -71.1	260.157 ∠ 110.8	260.157 ∠ 110.8	5987.43 ∠ -78.6	260.157 ∠ -69.2	260.157 ∠ -69.2
Fault Location Detection	Fault at line between Bus 153 and Bus 152 at 50% of line length from Bus 153 with fault resistance of 0.4 Ohms					

Consider the same circuit as in Figure 5-2 but with a generator outage which is out of the reduced equivalent circuit. The generator connected to Bus 146 is considered to be out of service. Even though this generator is out of the reduced equivalent circuit, it is very close to a majority of the components present in reduced circuit. Table 5-5 shows the comparison between the results obtained after generator outage with and without modifying the reduced equivalent circuit to reflect the change caused by generator outage. As the generator affected is not part of the reduced equivalent circuit, the modification that was made was forming a new updated reduced equivalent circuit after reflecting the generator change in the full circuit model.

Figure 5-10 shows the full circuit model which is reduced. The black box shows the portion of reduced equivalent circuit and the red box shows the generator which is out of service.

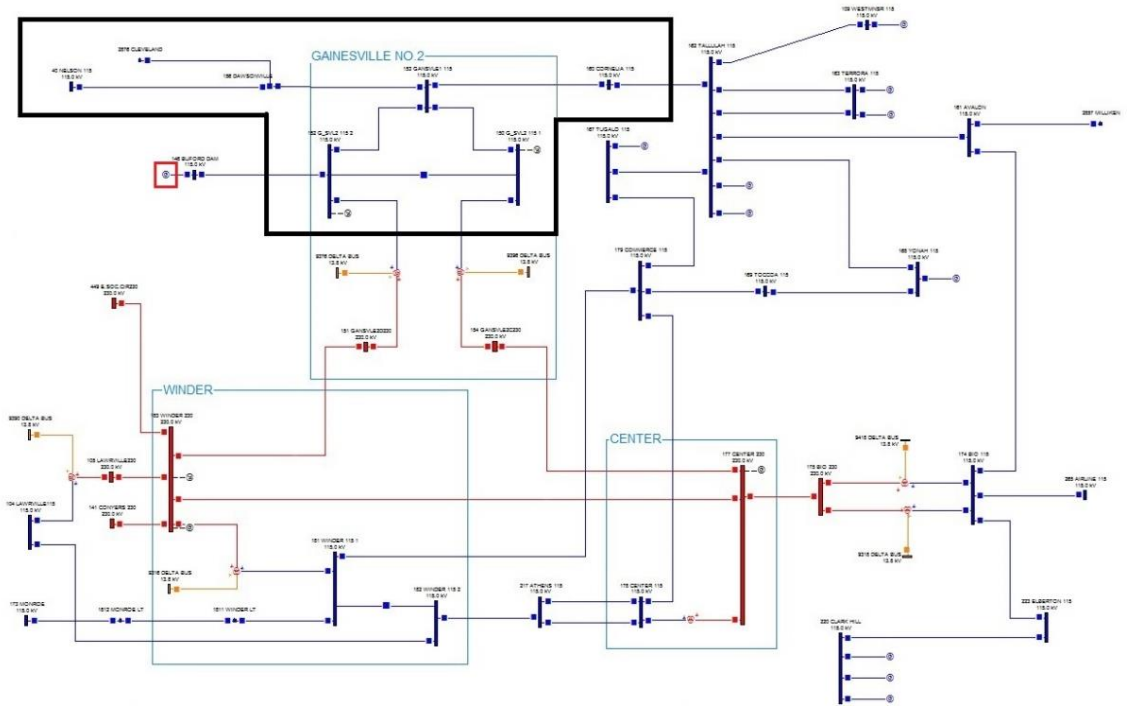

Figure 5-10 : Circuit diagram with generator outage

Table 5-5 : Analysis of generator outage

SLG fault (phase A) on the line between Bus 153 and Bus 156 at 20% of line length from Bus 153 with fault resistance of 0 Ohms						
	Line currents from Bus 153 (A)			Line currents from Bus 156 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit (after generator outage)	4666.00 ∠ -76.8	6.73881 ∠ 98.6	6.73881 ∠ 98.6	1245.51 ∠ -73.7	6.73881 ∠ -81.4	6.73881 ∠ -81.4
Reduced equivalent circuit (without circuit modification)	4693.02 ∠ -76.7	7.94003 ∠ 97.3	7.94003 ∠ 97.3	1245.27 ∠ -73.7	7.94003 ∠ -82.7	7.94003 ∠ -82.7
Reduced equivalent circuit (after circuit modification)	4693.09 ∠ -76.73	7.8835 ∠ 96.80	7.9056 ∠ 97.91	1195.49 ∠ -73.54	10.4231 ∠ 124.79	10.4009 ∠ 124.79
Fault Location Detection	Fault at line between Bus 153 and Bus 156 at 20% of line length from Bus 153 with fault resistance of 0 Ohms					
SLG fault (phase A) on the line between Bus 156 and Bus 2876 (remote line) at 20% of line length from Bus 2876 with fault resistance of 1 Ohms						
	Line currents from Bus 156 (A)			Line currents from Bus 2876 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit (after generator outage)	1344.28 ∠ -72.6	0.0000	0.0000	0.0000	0.0000	0.0000
Reduced equivalent circuit (without circuit modification)	1344.86 ∠ -72.6	0.0000	0.0000	0.0000	0.0000	0.0000
Reduced equivalent circuit (after circuit modification)	1344.87 ∠ -72.5	0.0000	0.0000	0.0000	0.0000	0.0000
Fault Location Detection	Fault at line between Bus 156 and Bus 2876 at 20% of line length from Bus 2876 with fault resistance of 1 Ohms					

Table 5-5 continued

SLG fault (phase A) on the line between Bus 153 and Bus 152 (mutually coupled line) at 50% of line length from Bus 153 with fault resistance of 0.4 Ohms						
	Line currents from Bus 153 (A)			Line currents from Bus 152 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit (after generator outage)	3234.02 ∠ -75.0	146.936 ∠ 110.1	146.936 ∠ 110.1	5315.70 ∠ -78.2	146.936 ∠ -69.9	146.936 ∠ -69.9
Reduced equivalent circuit (without circuit modification)	3252.52 ∠ -74.9	145.691 ∠ 110.4	145.691 ∠ 110.4	5375.81 ∠ -78.2	145.691 ∠ -69.6	145.691 ∠ -69.6
Reduced equivalent circuit (after circuit modification)	3252.62 ∠ -74.94	145.744 ∠ 110.4	145.689 ∠ 110.4	5375.86 ∠ -78.2	145.807 ∠ -69.5	145.807 ∠ -69.5
Fault Location Detection	Fault at line between Bus 153 and Bus 152 at 50% of line length from Bus 153 with fault resistance of 0.4 Ohms					

From Table 5-4 and Table 5-5, based on the faults currents values in different models, it is apparent that change in system configuration or parameters affects the fault current. Hence, this necessitates the need to update the library of reduced equivalent circuits regularly. It can also be observed that if the faulted line is too far from the line or generator which is out of service, there is not much change in the fault current between the equivalent circuit without modification and the equivalent circuit with modification. Therefore, modification or formation of updated reduced equivalent circuits can be skipped if the out of service power system component is temporary and very far away from the primary components of the reduced equivalent circuit with minimal loss in accuracy of the fault location estimation.

5.5 FAULT LOCATION REACH

A major advantage of using the proposed approach is that it can be used to verify the fault location estimate using data from other DFRs which are not monitoring the faulted line or use data to identify transmission line faults farther away from the line of measurement. This cannot be done with impedance-based fault location methods which is one of the most commonly used methods for fault location. Furthermore, impedance-based fault location techniques may not provide accurate fault location estimates in cases of tapped lines or three terminal lines [2].

The section analyses how far away from the fault recording device can accurate fault location be obtained. Accurate fault location estimate is expected when fault record obtained from the fault recorder monitoring the faulted line is processed. As we move away from the line monitored, the DFR records the fault current contribution flowing through that particular line monitored caused by a fault farther away from that line. This fault current contribution depends on the type of fault and fault location.

As the fault location technique is primarily based on search and find algorithm, an accurate result can be found as long as the fault current measurements obtained for a fault scenario are unique. This property which needs to be satisfied for the proposed method to work accurately also limits the size of the equivalent circuit, thus preventing the user from using the large full circuit model for fault location directly without forming reduced equivalent circuits. This is illustrated in the following paragraphs.

5.5.1 Fault Location Reach - Case 1

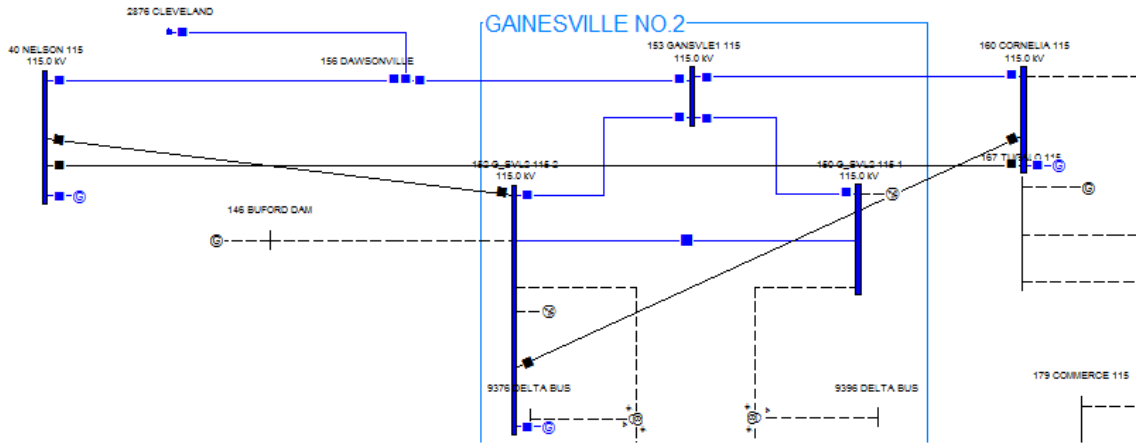

Figure 5-11 : Reduced Equivalent Circuit

Figure 5-11 is same as Figure 5-2. The circuit diagram is shown here again for easier referencing during analysis in the forthcoming paragraphs.

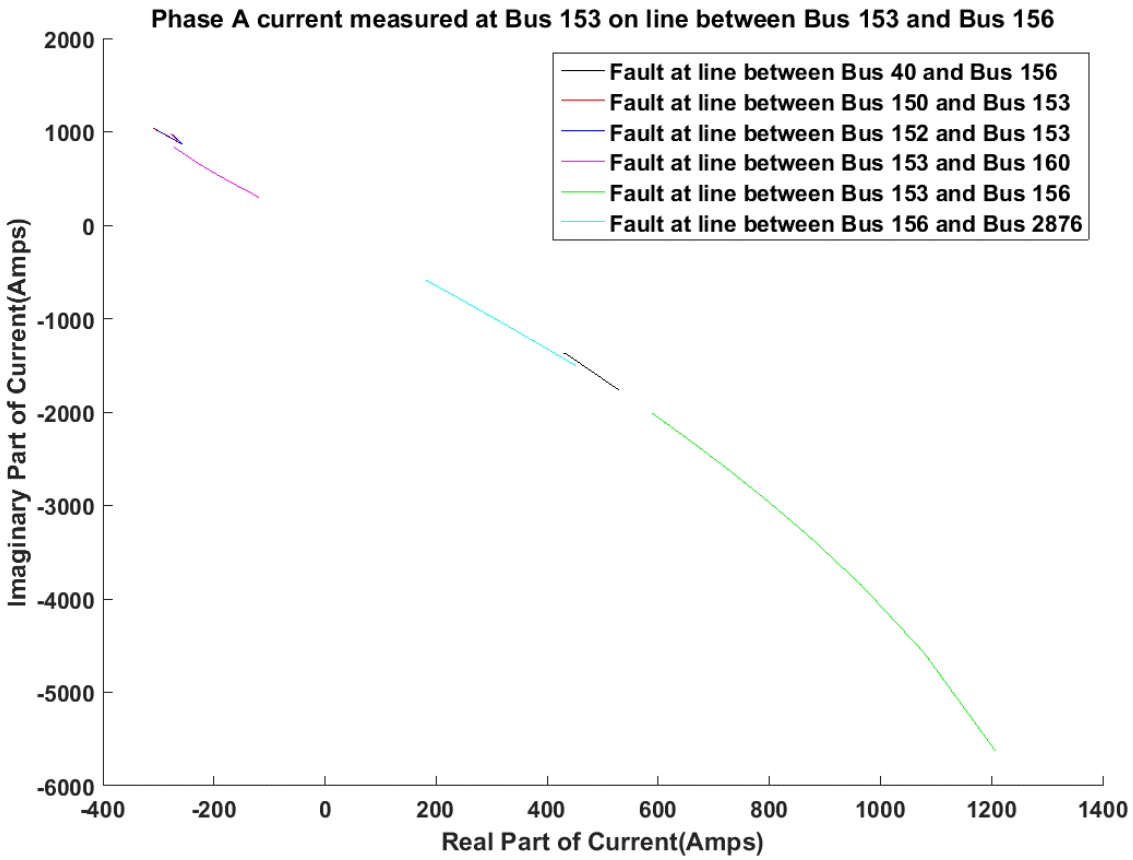

Figure 5-12 : Case 1 - Fault location reach without fault resistance

Figure 5-12 shows the phase A current measurement at Bus 153 on the transmission line between Bus 153 and Bus 156 for faults along the entire length of various lines of the transmission network in the reduced equivalent circuit model shown in Figure 5-11. This plot shows that fault current measurements from one terminal (at Bus 153) of the line being monitored (line between Bus 153 and Bus 156) show large variation with varying location with fault on that line. This implies that fault location search will be accurate as there is considerable variation in fault current with fault location and the fault currents are unique for faults at different positions on that line. This is expected as the fault recorder or monitor measures the fault current at a terminal of the faulted line. As we move the faults further away from the line that is monitored, there is a variation in the fault current that flows

through the line being monitored but the amount of variation of fault current with changing fault position is reduced. This can be seen in lines adjacent to the monitored line in different directions such as the line between Bus 156 and Bus 40 and the line between Bus 156 and Bus 2876. If the fault is too far away from the point being monitored, the fault contribution through the line being monitored will be small and similar for multiple fault locations and hence the search algorithm cannot accurately distinguish between the different cases. This problem can also occur if the line farther away from the monitoring location is a parallel transmission line such as the line between Bus 152 and Bus 153 and the line between Bus 150 and Bus 153. It can be observed from Figure 5-12 that plotted red and blue lines which correspond to faults on the above two mentioned lines overlap each other. This implies that fault on either of the two lines cannot be distinguished and identified using fault current measurement on the line between Bus 153 and Bus 156 measured at Bus 153. So, to identify fault on either of the above two lines, measurements are required at a different location.

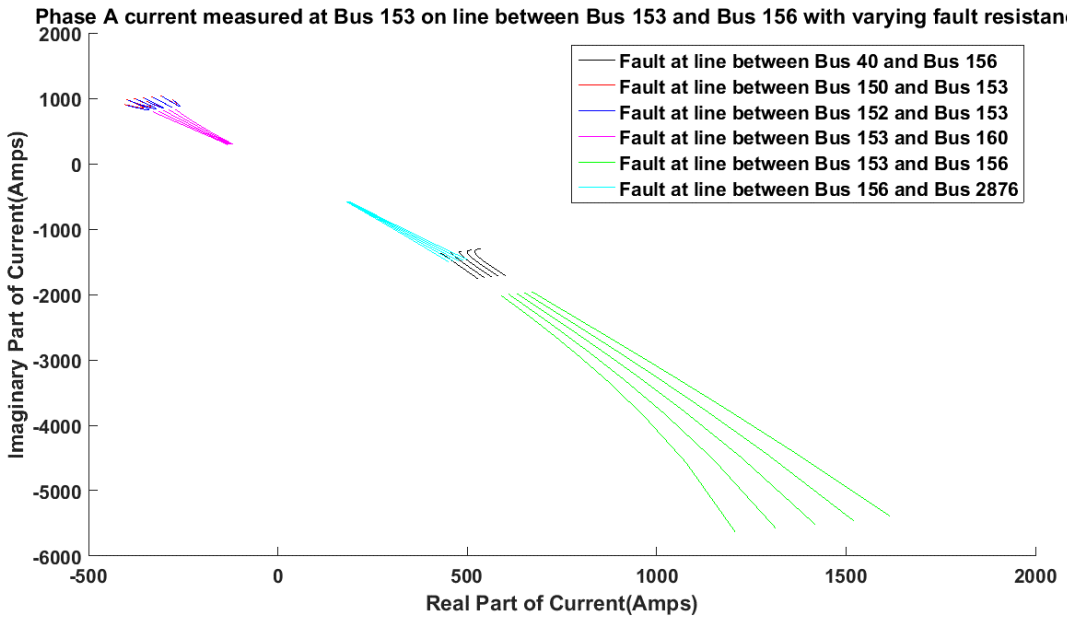

Figure 5-13 : Case 1 - Fault location reach with fault resistance

Now consider Figure 5-13. It is similar to Figure 5-12 but this plot includes the effect of fault resistance. The same color parallel lines correspond to fault along that particular line but with varying fault resistance between 0 ohms and 1 ohm in steps of 0.2 ohms where each parallel line represents a different fault resistance similar to the discussion in Section 5.3 The set of green lines which represent the monitored line (line between Bus 153 and Bus 156) do not overlap with any other set of lines as expected. This means that the fault current measurements are unique for different fault resistances along the line and hence, fault location using the proposed technique would be accurate. From the Figure 5-13, we can observe that there would be no problem in identifying the fault location on the line between the Bus 153 and Bus 160 even though the line is farther away than the line being monitored. We also observe that there is a small overlap between the cyan colored lines and black colored lines which mean that fault current flowing through our point of measurement overlap for faults in those lines. Hence, the current monitoring location may not be entirely accurate for faults on the line between Bus 156 and Bus 2876 and line between Bus 156 and Bus 40.

5.5.2 Fault Location Reach - Case 2

Figure 5-14 and Figure 5-15 analyze the same circuit as in Figure 5-11 from a different location. The monitor is at Bus 150 measuring the fault currents in the line between Bus 150 and Bus 153. Similar to the previously discussed case, it can be observed that red lines which represent the cases where the line monitored (transmission line between Bus 150 and Bus 153) is faulted at different locations with varying fault impedances produce unique fault current values.

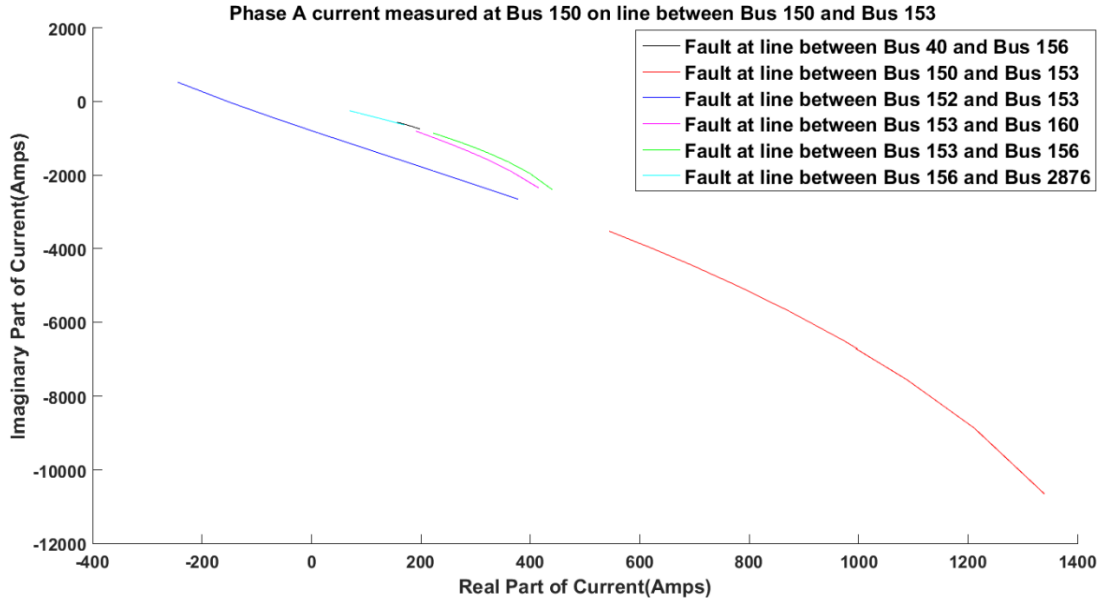

Figure 5-14 : Case 2 - Fault location reach without fault resistance

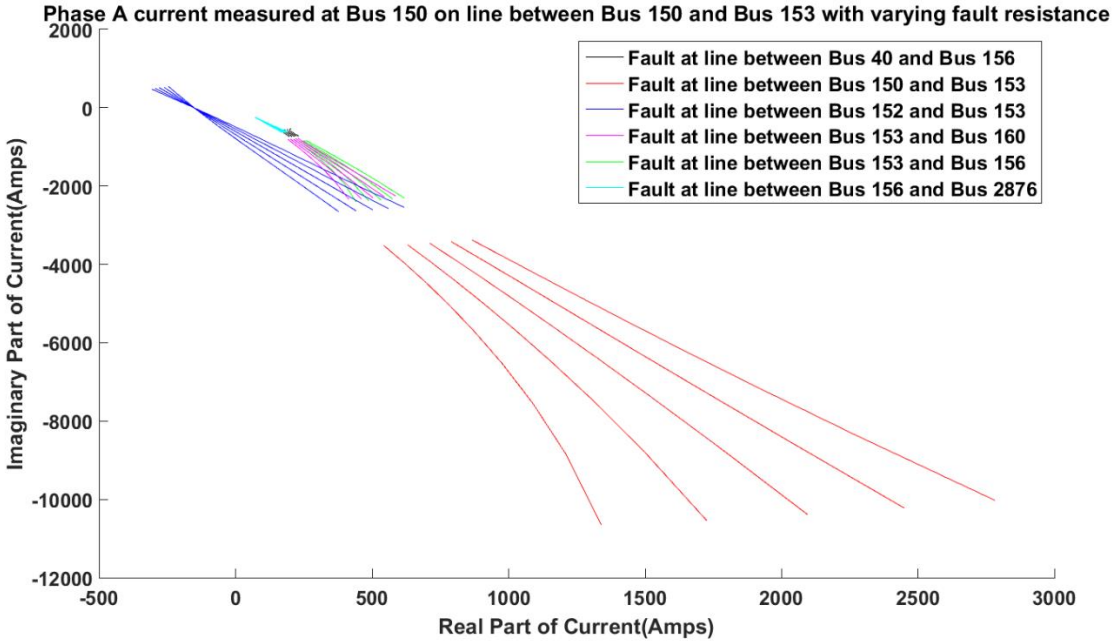

Figure 5-15 : Case 2 - Fault location reach with fault resistance

From Figure 5-15, it can be observed that the set of lines of color cyan, black, green and pink are very close to each other or overlap each other. This means that using the monitor at its current position, faults location on those transmission lines cannot be correctly identified. Hence, using measurement at Bus 150 monitoring the line between Bus 150 and Bus 153 is suitable only for obtaining fault location on that particular line only and not useful for obtaining fault location farther away from the measuring point.

From the above analysis, it can be concluded that fault location will be accurate at least when the fault is on the line being monitored. Fault location may be successful for some cases where faulted transmission line is farther away from the line being monitored. Furthermore, if the circuit is too large, there are greater chances that fault currents corresponding to different scenarios may overlap. Hence, an optimal size of circuit must be used while forming reduced equivalent circuits as too large or small a circuit does not produce distinctive advantages.

5.6 TEST CASE INCLUDING ALL THE ABOVE SCENARIOS

In the previous sections in this chapter, the effects of different issues such as the size of the circuit, transmission line and generator outage, the effect of fault resistance and fault location reach and how they affect the performance of the proposed method have been studied individually. This section will analyze a test case taking all the above issues in a single case to check the performance of the proposed method.

Consider the circuit in Figure 5-11. The line between Bus 153 and Bus 150 and the generator connected to Bus 146 are out of service. Figure 5-16.and Figure 5-17 show studies similar to that discussed in Section 5.5 about fault location reach. As the out of service generator was outside the reduced equivalent circuit, a new reduced equivalent

circuit was formed after reflecting the system changes in the full circuit model using the simple procedure explained in Section 4.3.

The plots show Phase A fault current measured at Bus 153 on the line between Bus 152 and Bus 153. As expected, there is a change in the direction of fault current through the location monitored for a fault on the line between Bus 152 and Bus 153 compared to faults on every other line in reduced equivalent circuit. From the figures, we can also observe that fault location estimates may not be accurate for any other case other than faults on the line between Bus 152 and Bus 153 (which is the line being monitored). Table 5-6 shows the comparison of fault current before and after modification of the reduced equivalent circuit.

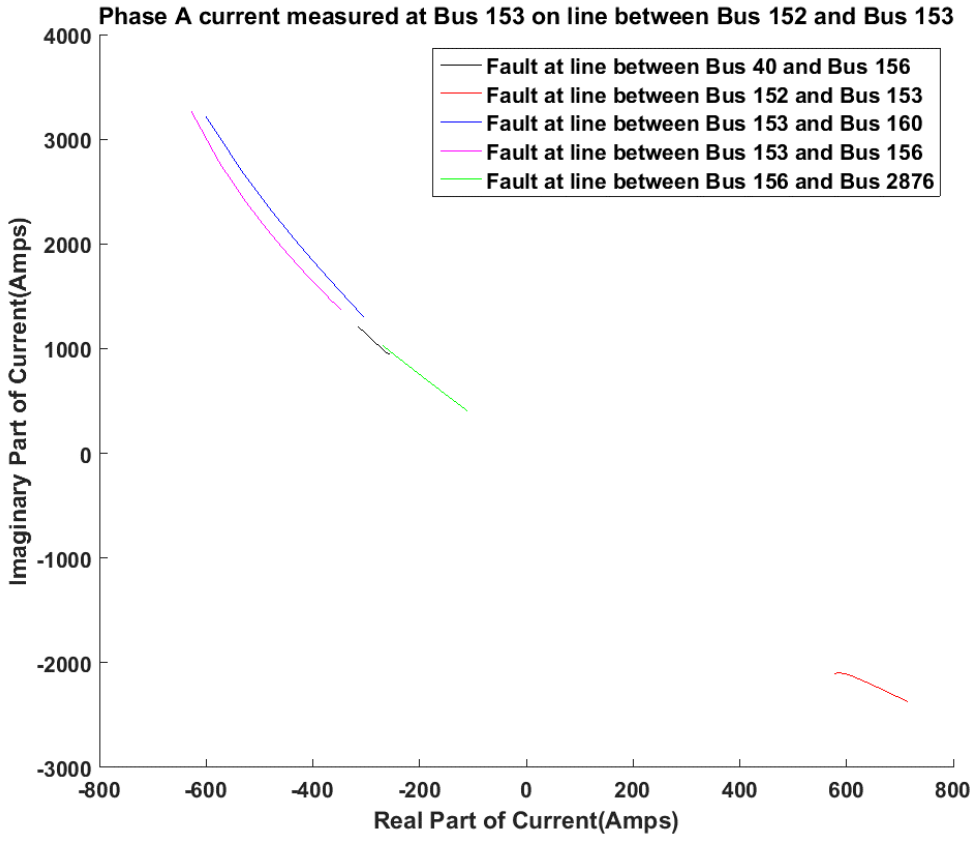

Figure 5-16 : Case 3 - Fault location reach without fault resistance

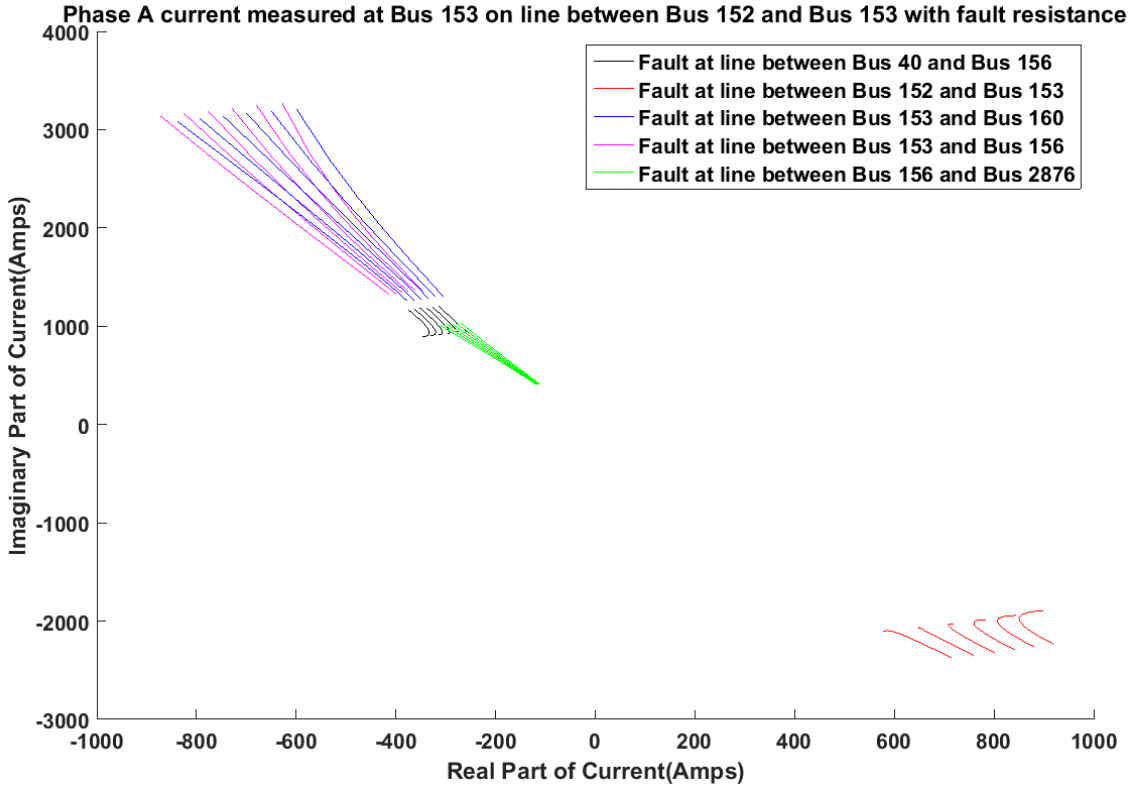

Figure 5-17 : Case 3 - Fault location reach with fault resistance

Table 5-6 : Analysis of test case including all the scenarios discussed

SLG fault (phase A) on the line between Bus 153 and Bus 156 at 20% of line length from Bus 153 with fault resistance of 0 Ohms						
	Line currents from Bus 153 (A)			Line currents from Bus 156 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit (after line outage)	3815.70 ∠ -76.3	33.3296 ∠ 106.2	33.3296 ∠ 106.2	1230.07 ∠ -73.7	33.3296 ∠ -73.8	33.3296 ∠ -73.8
Reduced equivalent circuit (without circuit modification)	4693.02 ∠ -76.7	7.94003 ∠ 97.3	7.94003 ∠ 97.3	1245.27 ∠ -73.7	7.94003 ∠ -82.7	7.94003 ∠ -82.7
Reduced equivalent circuit (after circuit modification)	3831.47 ∠ -76.3	34.1765 ∠ 105.7	34.2233 ∠ 106.0	1229.92 ∠ -73.7	34.2401 ∠ -74.2	34.2466 ∠ -74.14
Fault Location Detection	Fault at line between Bus 153 and Bus 156 at 20% of line length from Bus 153 with fault resistance of 0 Ohms					
SLG fault (phase A) on the line between Bus 156 and Bus 2876 (remote line) at 20% of line length from Bus 2876 with fault resistance of 1 Ohms						
	Line currents from Bus 156 (A)			Line currents from Bus 2876 (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Full circuit (after line outage)	1326.29 ∠ -72.6	0.0000	0.0000	0.0000	0.0000	0.0000
Reduced equivalent circuit (without circuit modification)	1344.86 ∠ -72.6	0.0000	0.0000	0.0000	0.0000	0.0000
Reduced equivalent circuit (after circuit modification)	1326.75 ∠ -72.59	0.0000	0.0000	0.0000	0.0000	0.0000
Fault Location Detection	Fault at line between Bus 156 and Bus 2876 at 20% of line length from Bus 2876 with fault resistance of 1 Ohms					

From Table 5-6, it is seen that the fault current flowing for faults at different locations change because the system configuration has been altered. The fault currents in the reduced equivalent circuit formed after circuit modification were similar to that of the modified full circuit model implemented in CAPE. Also, the proposed method has provided accurate fault location results even when all the common problems which may hinder its accuracy such as line and generator outage as well as the presence of fault resistance occur at the same time, as can be seen from Table 5-6.

This chapter has provided analysis on the technical capability of the proposed technique. From the above discussion, it can be concluded that the proposed method is progressive towards fault location automation with further scope for improvement. The method provides a variety of advantages discussed in the following section.

6. SUMMARY AND FUTURE WORK

6.1 SUMMARY

Transmission lines are a vital part of power systems as they connect power generating stations to load. Transmission lines are subjected to a variety of electrical faults as they are uninsulated and exposed to environmental effects. Hence, transmission line faults need to be cleared quickly. Commonly used transmission line fault location process by utilities are a multi-staged process which requires human intervention and manual manipulation of data which causes time delays. So, this thesis proposes an approach for fault location automation which can produce a fault location estimate as and when fault records are received by the utility without any human intervention.

A model-based fault location technique using reduced equivalent circuits is presented and analyzed. Fault records are aggregated into a folder as and when received from fault recorders. This folder is monitored by MATLAB. A commonly used industry standard fault record format (IEEE Standard Common Format for Transient Data Exchange - COMTRADE file format) and fault record data preprocessing steps required have been discussed. MATLAB is then used to process the fault record to obtain the fault current and fault voltage. MATLAB then identifies the faulted line and selects the appropriate circuit from a library of reduced equivalent circuits. OpenDSS is used for performing fault analysis as it can be driven by MATLAB. The existing successful fault location technique used by utilities (sliding fault along the length of the line and comparing it with actual values from fault record) is preserved and is implemented using MATLAB.

The success of a proposed technique depends on its technical performance and ease of usage. A sample circuit present in CAPE (which is a widely used commercial software for protection engineering) is used to illustrate the proposed method and to test the

technical capabilities of the algorithm. The proposed method was analyzed on a variety of aspects starting from validating the usage of reduced equivalent circuit to evaluating a method to tackle common issues faced by utilities such as line and generator outage. The presence of mutual coupling and fault resistance are some of the major components associated with transmission line faults which affect fault location estimation but the proposed algorithm proved to be robust and produced accurate results. Apart from fault location automation, this method of analysis has several other advantages which are discussed in the following section

6.2 ADVANTAGES

The primary advantage of the proposed method is that it automates the process of fault location. The proposed method is reliable and capable of producing accurate fault location estimate as and when a fault record is received by the utility without any human intervention. This saves precious time which may be lost waiting for personnel with different capabilities to perform their course of action and pass on the results for next set of action.

The proposed method makes use of the circuit model available for analysis and derives its several advantages because of availability of system parameters. The algorithm uses OpenDSS which is a powerful tool that can be driven by MATLAB. Hence, it allows flexibility in the analysis method of the commonly used fault location procedure when it does not produce satisfactory results. Additionally, several other power system components such as loads, capacitors and transformers can also be modeled in OpenDSS which further increase the accuracy of fault location. Furthermore, simulation results data are imported into MATLAB. This provides powerful external analytical capabilities as well as excellent graphics for displaying results, hence, making it is easier to understand and analyze the

results. This enables the protection engineer to visualize the short-circuit characteristics of the system as well.

Another major advantage is that this method is capable of accurate fault location even on transmission lines which are farther away from the line (up to a certain distance) where the currents and voltages are measured. This has been analyzed in Chapter 5. This helps overcome some of the problems faced by impedance-based fault location algorithms such as the inability to produce accurate fault location estimation for three terminal lines and tapped lines. It also facilitates fault location verification process where data from adjacent or remote DFRs can also be used to identify the fault location.

6.3 FUTURE WORK

The proposed method has great potential in revolutionizing the existing fault location approach but it is still in its nascent stages. Following are several suggestions to improve the method:

- The process of formation of reduced equivalent circuit from the full circuit model can be automated and customized according to the characteristics of the circuit. This could simplify the reduced equivalent circuit updating process whenever system parameters vary. This can be implemented in a couple of ways. One simple way is to automate the process of forming the library of reduced equivalent circuits for each different software used by various utilities for maintaining their current full circuit model. Once a library of reduced equivalent circuits is formed, they can be easily converted to OpenDSS. Another approach which can be complex and tedious is to convert the entire large circuit from other software to OpenDSS and then implement the circuit reduction algorithm using MATLAB or any other software to obtain the library of reduced equivalent circuit. The latter

method can have several sources of error as the circuit being converted is complex and not a simple reduced small equivalent circuit.

- An efficient graphic user interface (GUI) could be developed to visualize the location of the fault which can help in easy identification of the location of fault for the maintenance crew.
- Data mining techniques can be implemented to optimize the sliding fault analysis procedure for fault location (sliding fault along the length of the line and comparing it with actual values from fault record).

BIBLIOGRAPHY

[1] B. Ram and D. N. Vishwakarma, Power system protection and switchgear, Tata Mc-Graw Hill Publicaiton Company Limited, 2005.

[2] S. Das, S. Santoso, A. Gaikwad and M. Patel, "Impedance-based fault location in transmission networks: theory and application," *Access, IEEE,* vol. 2, pp. 537-557, 2014.

[3] "IEEE Guide for Determining Fault Location on AC Transmission and Distribution Line," *IEEE Std C37.114-2014 (Revision of IEEE Std C37.114-2004),* pp. 1-76, Jan. 30 2015.

[4] M. Dragomir, A. Miron, M. Istrate and A. Dragomir, "A review of impedance-based fault location approaches for transmission lines," in *International Conference and Exposition on Electrical and Power Engineering*, 2014.

[5] M. M. I. Hashim, H. W. Ping and V. K. Ramachandaramurthy, "Impedance-based fault location techniques for transmission lines," in *TENCON*, 2009.

[6] J. Mora-Flòrez, J. Meléndez and G. Carrilllo-Caicedo, "Comparison of impedance based fault location methods for power distribution systems," *Electric Power Systems Research,* vol. 78, no. 4, pp. 657-666, April 2008.

[7] "CAPE Software," Electrocon International, [Online]. Available: http://www.electrocon.com/capeintro.php. [Accessed 28 December 2015].

[8] "ASPEN Software," [Online]. Available: http://www.aspeninc.com/web/. [Accessed 27 10 2016].

[9] "A Guide to Digital Fault Recording Event Analysis," [Online]. Available: http://www.erlphase.com/downloads/papers/A_Guide_To_Digital_Fault_Recording_Event_Analysis_ERLPhase_GATech2010.pdf.

[10] "C37.111-1999 - IEEE Standard Common Format for Transient Data Exchange (COMTRADE) for Power Systems".

[11] A. V. Oppenheim and R. W. Schafer, Discrete Time Signal Processing, Pearson, 2009.

[12] S. J. Orfanidis, Introduction to signal processing, Prentice-Hall, 1996.

[13] T. Takagi, Y. Yamakoshi, M. Yamaura, R. Kondow and T. Matsushima, "Development of a new type fault locator using the one-terminal voltage," *IEEE Transactions on Power Apparatus and System,* Vols. PAS-101, no. 8, pp. 2892-2898, Aug. 1982.

[14] K. Zimmerman and D. Costello, "Impedance-based fault location experience," in *58th Annual Conference for Protective Relay Engineers*, 2005.

[15] Edmund O. Schweitzer III, "A Review of Impedance-Based Fault," in *14th Annual Iowa-Nebraska System Protection Seminar*, Oct 1990.

[16] "OpenDSS," [Online]. Available: https://sourceforge.net/projects/electricdss/.

[17] "MATLAB - Mathworks," [Online]. Available: http://www.mathworks.com/products/matlab/index.html.

[18] M. K. Enns and J. J. Quada, "Sparsity-Enhanced Network Reduction for Fault Studies," *IEEE Transactions on Power Systems,* vol. 6, pp. 613-621, May 1991.

[19] F. Calero, "Mutual Impedance in Parallel Lines," Schweitzer Engineering Laboratories, Inc., May 2015. [Online]. Available: https://selinc.cachefly.net/assets/Literature/Publications/Technical%20Papers/6283_MutualImpedance_FC_20150513_Web.pdf?v=20151124-113324.

[20] J. Izykowski, E. Rosolowski and Saha M M, "Locating faults in parallel transmission lines under availability of complete measurements at one end," *IEE Proceedings - Generation, Transmission and Distribution,* vol. 151, no. 2, pp. 268-273, March 2004.