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High step-up interleaved boost converter utilising stacked half-bridge rectifier configuration

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Musbahu Muhammad[1] ✉, *S. Lambert*[1], *M. Armstrong*[1], *V. Pickert*[1]

[1]*School of Engineering Newcastle University, UK*

✉ *E-mail: musbahu.muhammad@ncl.ac.uk*

Abstract: This paper proposes a solution to complement the insufficient voltage gain and voltage stress distribution of classical interleaved boost converter in high step-up application. An interleaved converter integrating coupled inductor and voltage multiplier cell, which provides an additional voltage gain is proposed. By stacking the secondary side of the interleaved coupled inductor to its primary side, a high step-up voltage gain and distributed voltage stress are realised. Low-voltage rated devices ultimately reduce the conduction losses. The principle of operation and the performance characteristic of the converter are presented and verified by an experimental prototype of 140 W, 12 V input, and 120 V output.

1 Introduction

There is an increasing demand of distributed energy sources (DES) such as solar PV, batteries, and fuel cells in applications ranging from smart grids, energy storage system (ESS), distributed generation, and electric vehicle (EV). However, the typical output of DES used in such applications has relatively low-voltage level compared to the required voltage level of emerging applications, which ranges from 200 to 400 V [1]. High efficiency high step-up DC–DC converters are required to facilitate the connection of DES to the grid. To date, various topologies have been proposed to achieve this voltage step-up and they are either transformer [2] based or transformer-less [3] and their variations [4–9].

The classical boost converter is the simplest converter for voltage step-up. However, it suffers extreme duty cycle operation, the power devices sustain high-voltage stress and reverse recovery loses, which inhibits the efficiency. To overcome the problem of extreme duty cycle operation, many single switch converters have been proposed. These include switched capacitor/switched inductor techniques [5], voltage lift [6], and voltage multiplier [7]. These methods require multiple cells to achieve high-voltage conversion ratio, which typically results in complex structures.

A common alternative technique is to use a coupled inductor to enlarge the voltage gain in non-isolated DC–DC converters [2, 10]. Coupled inductor boost converters can provide high-voltage gain without extreme duty cycle operation, with a relatively simple topology. Consequently, they can reduce the switch voltage stress and allow the use of low-voltage rated, high performance, semiconductor devices. However, the main drawbacks of coupled inductor converters typically include severe voltage spikes across the switch due to the leakage energy of the coupled inductor and the large input current ripple. To mitigate the current ripple, interleaving is usually adopted as an effective solution in high power applications to reduce the passive component size, increase the power level, minimise the current ripple, improve the transient response, and realise thermal distribution. However, the voltage gain of the conventional interleaved boost converter is also limited.

To address this issue, one can find many promising interleaved hybrid topologies integrating magnetic and capacitive means mainly for voltage gain [8, 9]. To limit the switch voltage excursion due to the leakage energy of the coupled inductor, energy recycling schemes are usually adopted.

Here, an alternative structure based on half-bridge-doubler rectifier configuration in both the primary and secondary side is investigated to obtain a high efficiency and high step-up DC–DC conversion. To further exploit this advantage, stacking the secondary-side half-bridge-doubler rectifier on top of its primary-side counterpart is considered, the stack structure would ultimately enlarge the voltage gain and distribute the voltage stress of the devices as well. Importantly, lower turns' ratio can be employed to achieve high conversion ratios, which reduce the copper losses and leakage inductance of the coupled inductor. Interleaving is adopted on the primary side to share the input current and cancel the current ripple of the coupled inductors.

2 Converter operational analysis

2.1 Topology description

Fig. 1 shows the circuit configuration of the proposed topology integrating coupled inductor and stacked half-bridge-doubler rectifier. The converter employs two coupled inductors (L_1 and L_2) with the same number of turns in the primary and secondary sides. The primary winding of the coupled inductors n_{1p} and n_{2p} are connected in parallel to share the large input current on the low-voltage side and are coupled to their corresponding secondary windings n_{s1} and n_{s2}. The primary and secondary windings are denoted by coupling references ''*'' and ''o''. The secondary windings are in series on the high-voltage side to achieve windings coupled configuration and extend the voltage conversion ratio. The output voltage of the converter is realised by stacking the primary-side bridgeless boost rectifier voltages formed by capacitors C_1, C_2 and diodes D_1, D_2 and that of the coupled inductors secondary windings bridgeless boost rectifier formed by the C_3, C_4 and diodes D_3, D_4 respectively.

The equivalent circuit of the proposed converter is shown in Fig. 2. The coupled inductor can be modelled as an ideal

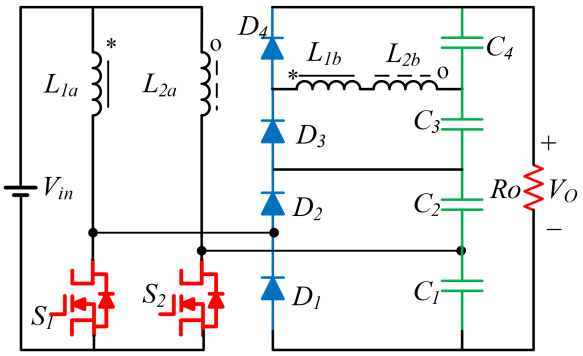

Fig. 1 *Circuit configuration of the proposed converter*

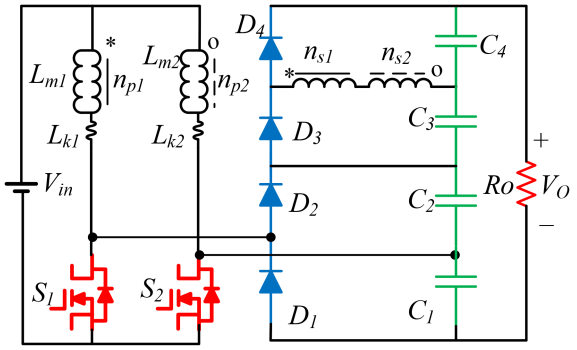

Fig. 2 *Equivalent circuit*

transformer with defined turns' ratio [2, 10]. The primary winding of the ideal transformer is connected in parallel with the magnetising inductor L_{m1}, L_{m2} and then in series with leakage inductance L_{k1}, L_{k2}. S_1, S_2 are the main power switches of the converter. The power diodes D_1, D_2 serve as clamp diodes and C_1, C_2 are the clamp capacitors. C_o is the output capacitor and V_{in}, V_o represent the input and output voltages, respectively.

To simplify the analysis, the following assumptions are made:

(i) The power switch is ideal, but the parasitic capacitor is considered in the analysis.
(ii) The voltages across capacitors C_1, C_2, C_3, and C_4 are large enough and assumed to be constant.
(iii) The turns ratio of the coupled inductor N is equal to n_2/n_1 and coupling coefficient k is expressed as $L_m/L_{\text{Lk}} + L_m$

2.2 Operational modes

The following analysis is confined to continuous current mode (CCM) operation, and the operation is guaranteed throughout the full range of the duty cycle variation with resistive loads. Fig. 3 shows the typical steady state waveform of the converter in one switching cycle. During steady-state operation, the duty cycle D is higher than 0.5. Typical steady-state waveform of the operation in one switching cycle, the equivalent circuits and current flow path corresponding to each operational stage are shown in Fig. 4. The converter operation is analysed as follows:

Stage 1 $[t_0 - t_1]$ (Fig. 4*a*): before t_0, the main switch S_1 is off and S_2 is on, the diodes D_2 and D_3 are reverse biased, while D_1, D_4 are forward biased. Magnetising inductor L_{m2} as well as the leakage inductor L_{k2} are charged linearly by the input voltage. Consequently, capacitor C_4 is charged by the induced voltage of n_{s2}. The leakage inductor energy L_{k1} is released into the capacitor C_2.

Stage 2 $[t_1 - t_2]$ (Fig. 4*b*): S_1 and S_2 are both on at time t_1. All the diodes are reversed biased, the load is supplied by the capacitors C_1, C_2, C_3, and C_4, respectively. The coupled inductors are linearly charged by the input voltage V_{in}.

Stage 3 $[t_2 - t_3]$ (Fig. 4*c*): At time t_2, the power switch S_2 turns off. The drain-source voltage of main switch S_2 rise to the capacitor voltage V_{C1}, which makes the diode D_1 to conduct. The leakage inductor energy of L_{k1} is released to the capacitor C_1. During this time, the coupled inductor L_1 acts as a filter inductor and L_2 acts as a transformer. Consequently, capacitor C_3 is charged by the induced voltage of n_{s1}. The voltage of the main switch S_2 is clamped to the voltage of the capacitor C_1.

Stage 4 $[t_3 - t_4]$ (Fig. 4*d*): The gating signal of the power switch S_2 is applied at time t_3 and the diode D_2 equally becomes reversed biased. The current through the diode D_3 has reached its peak and begins to fall; the current falling rate of the diodes is controlled by leakage inductors L_{k1} and L_{k2}

Stage 5 $[t_4 - t_5]$ (Fig. 4*e*): This operating stage is similar to stage 2, all the power switches are on and all the power diodes are reversed biased. The load is supplied by the capacitors C_1, C_2, C_3, and C_4, respectively. The coupled inductors are charged linearly by the input voltage source.

Stage 6 $[t_5 - t_6]$ (Fig. 4*f*): At time t_5, switch S_1 turns-off and the diode D_1 becomes forward biased. A new switching cycle ensue in similar fashion.

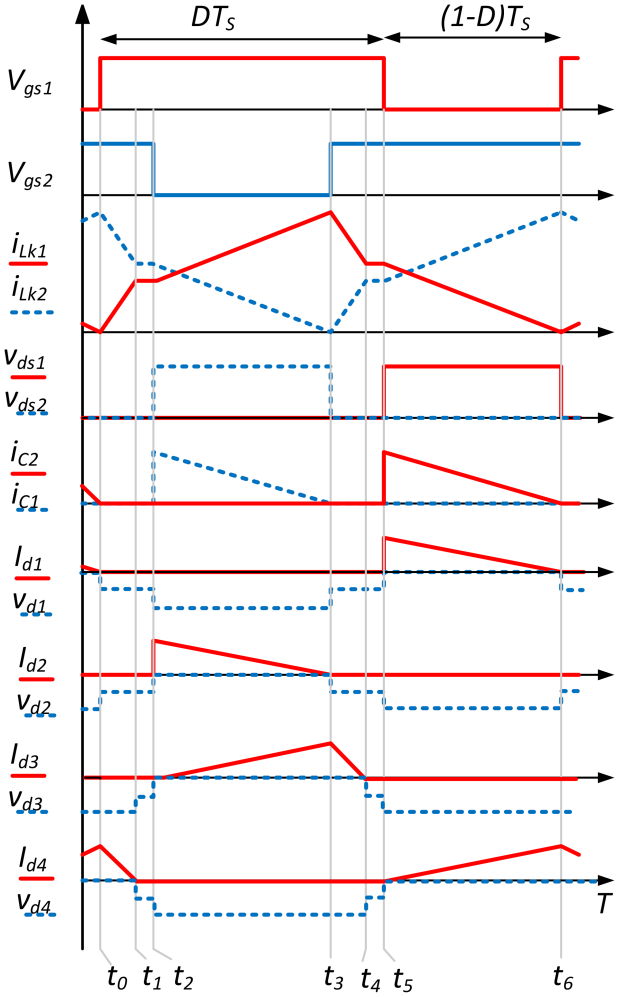

Fig. 3 *Typical steady state waveform of the converter in one switching cycle*

3 Circuit analysis

3.1 Voltage conversion ratio

Here, the coupled inductors are assumed to be ideal with no leakage inductance, the power switches are also considered lossless with zero conduction voltage drops, and no parasitic capacitances. Therefore, the voltage stress of the power switches and that of capacitors C_1, C_2 when either of the main switches turns off is given by

$$V_{\text{ds1}} = V_{\text{ds2}} = V_{C1} = V_{C2} = \frac{V_{\text{in}}}{(1-D)} \tag{1}$$

The output capacitors C_3 and C_4 are charged by energy transformation from the coupled inductor primary side when either of the primary switches is on or off. For example, each capacitor is charged by the sum of the induced voltages from the respective primary windings. Therefore, V_{C3} and V_{C4} are derived as

$$V_{C3} = V_{C4} = \frac{NV_{\text{in}}}{(1-D)} \tag{2}$$

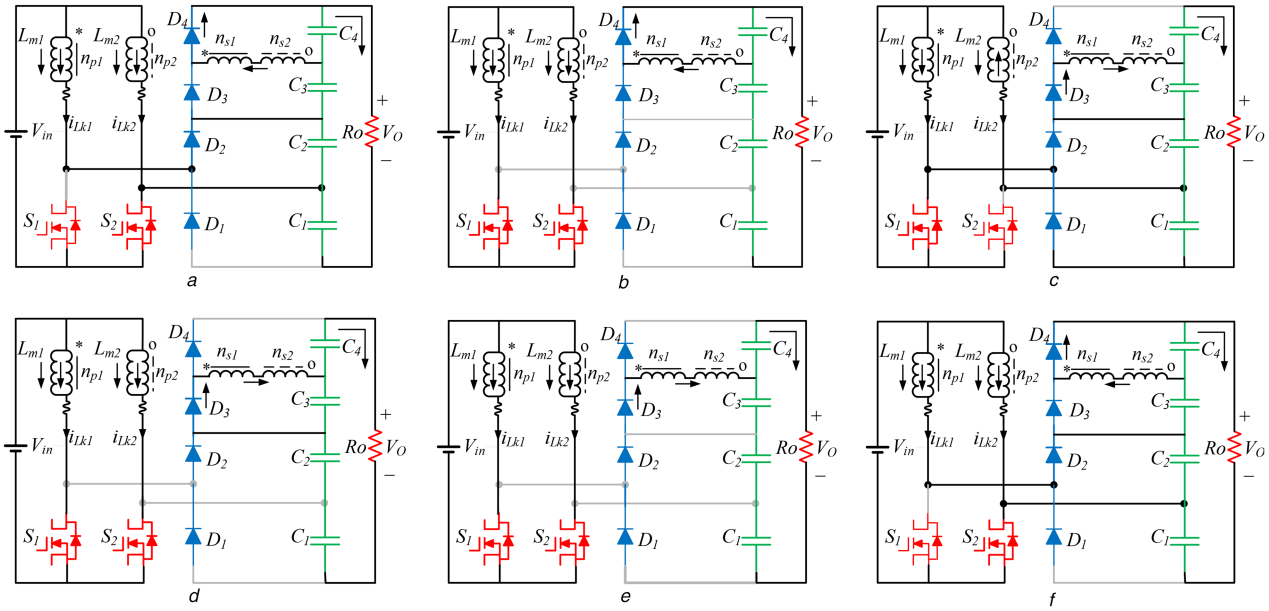

Fig. 4 *Operational modes equivalent circuit*
(a) Stage 1 $[t_0 - t_1]$, ***(b)*** Stage 2 $[t_1 - t_2]$, ***(c)*** Stage 3 $[t_2 - t_3]$, ***(d)*** Stage 4 $[t_3 - t_4]$, ***(e)*** Stage $[t_4 - t_5]$

The output voltage of the converter is the summation of the capacitor voltages given by

$$V_O = V_{C1} + V_{C2} + V_{C3} + V_{C4} = \frac{2V_{\text{in}}}{(1-D)} + \frac{2NV_{\text{in}}}{(1-D)} \tag{3}$$

From (1), (2), and (3), the ideal voltage gain is given by

$$M_{\text{ideal}} = \frac{V_o}{V_{\text{in}}} = \frac{2(N+1)}{(1-D)} \tag{4}$$

The coupled inductor turns ratio N can be adjusted to achieve the desired voltage conversion ratio without resorting to extreme duty cycle operation. The curve relating the voltage gain as a function of duty cycle and turns ratio is shown in Fig. 5.

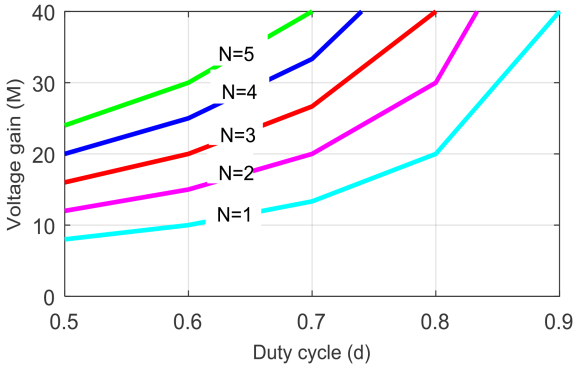

Fig. 5 *Voltage gain as a function of duty ratio and turns ratio*

3.2 Power devices voltage stress

By neglecting the voltage ripple on the capacitors, the voltage stress of the switches are the same given by.

$$V_{\text{ds1}} = V_{\text{ds2}} = \frac{V_O}{2(N+1)} \tag{5}$$

The voltage stress on the diodes D_1, D_2 is the sum of the voltage stresses of capacitor C_1 and C_2, respectively, given by

$$V_{D1} = V_{D2} = \frac{2V_{\text{in}}}{(1-D)} = \frac{V_O}{(N+1)} \tag{6}$$

The voltage stress of the power diode D_3, and D_4 is the summation of the voltage across capacitors C_3 and C_4, respectively, expressed as

$$V_{D3} = V_{D4} = \frac{2NV_{\text{in}}}{(1-D)} = \frac{NV_O}{(N+1)} \tag{7}$$

The relationship between the power devices voltage stress and turns ratio is plotted in Fig. 4. The voltage stress on the power switches S_1, S_2 and that of power diodes D_1, D_2 decrease as the coupled inductor turns ratio increase. Conversely, the voltage stress on the diodes D_3, D_4 increases as the turns ratio increases (Fig. 6).

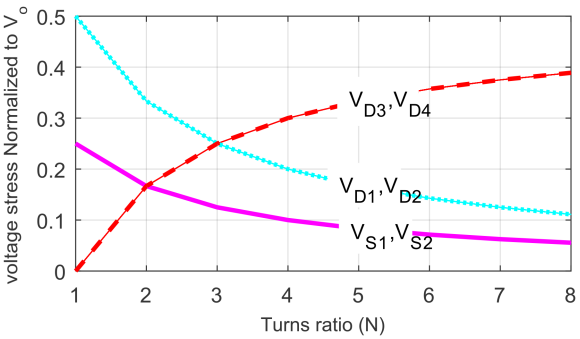

Fig. 6 *Turns ratio and power devices voltage stress effect*

4 Experimental validation

In order to verify the operation and evaluate the performance of the converter, a 12 V input, 120 V output 140 W prototype circuit is built and tested in the laboratory. The specification of the converter along with the components rating is listed in Table 1. The following experimental results are measured under full load conditions with 12 V input voltage. The 180 degrees out of phase gating signals along with power switches drain-source voltages of the power switch are shown in Fig. 7.

It can be seen that the voltage stress of the switches is 30 V, which is one-quarter of the output voltage. This allows low-rated devices with low $R_{\text{ds-on}}$ to be employed and reduce the conduction loss. Fig. 8 shows the current and voltage stress of the power switches. The voltage and current waveforms of the diodes $\boldsymbol{D}_1$, $\boldsymbol{D}_2$ are illustrated in Fig. 9. When either of the main switches turns-off the diodes $\boldsymbol{D}_1$, $\boldsymbol{D}_2$ conducts and the leakage inductor energy is

Table 1 Converter prototype specifications

output Power (P_O)	140 W
input Voltage (V_{in})	12 V
output Voltage (V_O)	120 V
switching Frequency (f_s)	50 KHz
main Switches (S)	FDP047AN
diodes (D_1, D_2, D_3 and D_4)	MBUR42050G
capacitors (C_1 C_2)	4.7 μF
capacitors (C_3 C_4)	10 μF
turns Ratio (n_2/n_1)	1:1
magnetising Inductance (L_m)	35 µH
leakage Inductance (L_{Lk})	1.3 µH

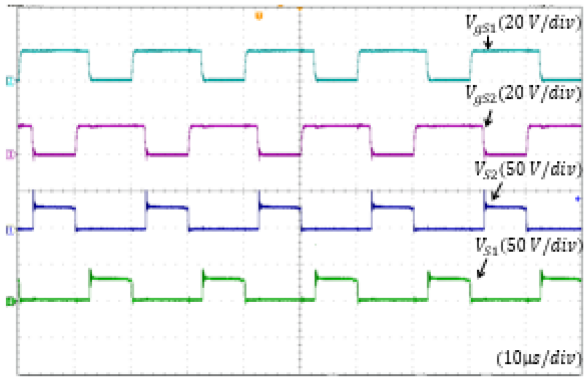

Fig. 7 *Switches gating signals and drain source voltages*

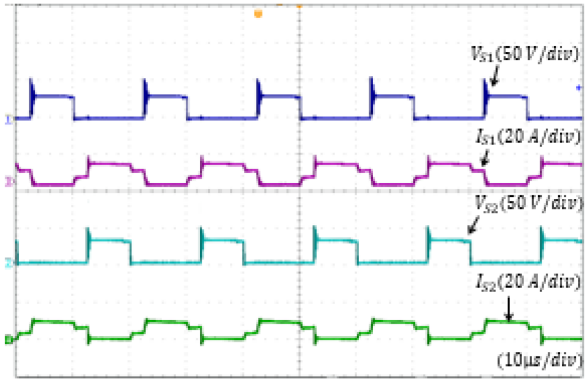

Fig. 8 *Main switches voltage and current waveforms*

released to the capacitors $\boldsymbol{C}_1$, $\boldsymbol{C}_2$. The diodes act as a passive clamp circuit for limiting the switch voltage excursion due to leakage inductor energy. Both diodes turns-off naturally with no reverse recovery problem. It is worth noting that the diodes voltage stress is far less than the output voltage. The voltage and current waveforms of the diodes $\boldsymbol{D}_3$, $\boldsymbol{D}_4$ are shown in Fig. 10. The voltage stress of the diodes is 65V which is also less than the output voltage of 120 V; this further confirms the voltage stress distribution of the converter. As illustrated in Fig. 10, the diodes turn-off naturally, leading to the reverse recovery alleviation.

Fig. 11 shows the leakage inductor currents (coupled inductor primary current) and the input current. Typical coupled inductor primary current is large due to the magnetising inductor and reflected secondary winding currents. However, the ripple magnitude of the input current is small due to interleaving. The input current is continuous over the entire switching cycle. Fig. 12 shows the measured efficiency of the converter. The maximum efficiency is 96% at an output power of 60 W, the conversion efficiency is 95% at a full load of 140 W.

5 Conclusion

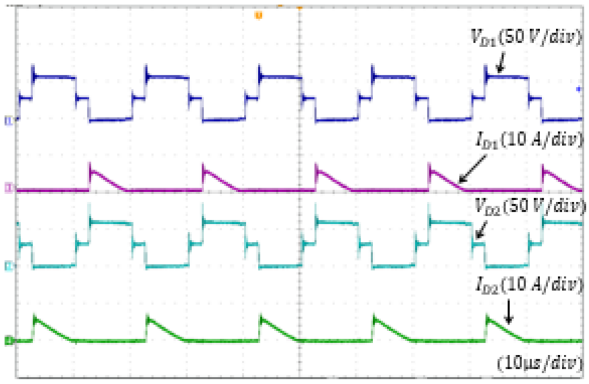

Fig. 9 *Diodes D_1, D_2 voltage and current stress*

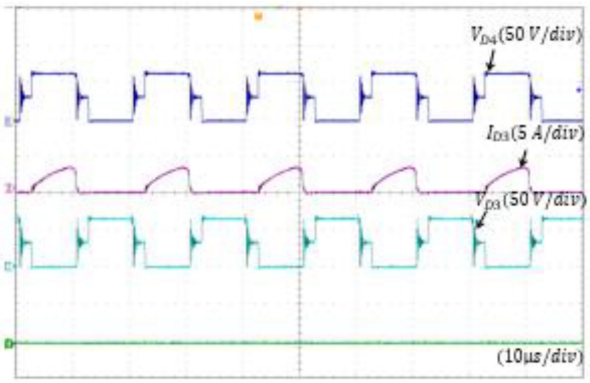

Fig. 10 *Diodes D_3, D_4 voltage and current stress*

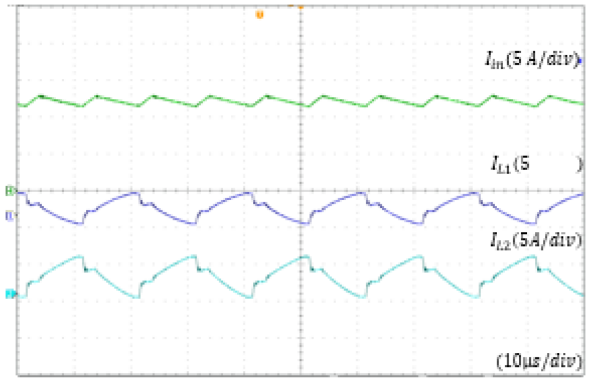

Fig. 11 *Input and leakage inductor currents*

This paper presents a new high step-up interleaved DC–DC boost converter based on half-bridge-doubler rectifier configuration in both the primary and secondary side. The turns' ratio of the coupled inductor can be adjusted to enlarge the voltage gain. The interleaved structure allows currents sharing and reduce the current stress of the components. The stack arrangement distributes the power devices voltage stress, hence lower voltage rated devices can be utilised to reduce the conduction losses. The leakage energy of the coupled inductor is recycled to the output. Theoretical analysis of the circuit's principle of operation and experimental results presented from a 140 W prototype confirm the effectiveness of the proposed topology as a high step-up power converter.

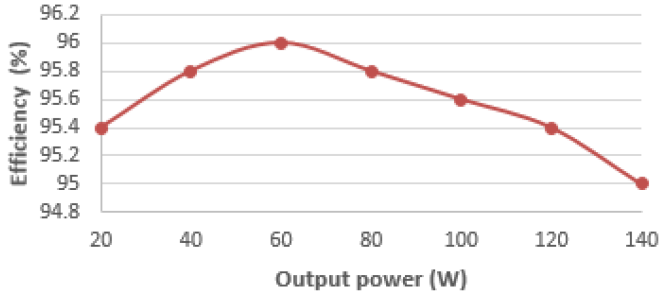

Fig. 12 *Measured converter efficiency*

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