IEEE Int. Workshop VLSI Design & Video Tech.
Suzhou, China, May 28~30, 2005

A LOW POWER SUPPLY AND HIGH FREQUENCY DRIVER DESIGN FOR DC-DC CONVERTER APPLICATIONS

Donglai Xu, Wendan Xu and Jianyong Zhang*

School of Science and Technology, University of Teesside, Middlesbrough, TS1 3BA, UK
e-mail: d.xu@tees.ac.uk, j.zhang@tees.ac.uk
* Department of Computer Engineering, Xi'an Aero-technical College, Xi'an, 710077, P. R. China
e-mail: xuwendan24@sohu.com

ABSTRACT

This paper presents an improved driver circuit design for boost DC-DC converter applications. The circuit possesses the characteristics of low power supply and high speed and is, thus, suitable for portable equipment and mobile applications. The simulation results demonstrate that the design has achieved a low power voltage of 1.0V, which is ideal for single battery applications. The operational frequency of the circuit can be as high as 1MHz, which meets the increasing demand for high switch speed. Using Samsung Bipolar Process, this design has been prototyped, and the testing on chips confirms that the prototypes fully meet design specifications and are ready for commercial products applications.

1. INTRODUCTION

With the rapid development of portable electronic equipment and wireless products, high performance analogue devices have been becoming increasingly important for systems integration. As one of the most basic components in analogue VLSI, DC-DC converter circuit has been widely used in many applications that require low power supply and high switch frequency, such as 3G mobile phones, portable audio/video devices, and other multimedia products. In this paper, a bipolar DC-DC converter driver circuit that targets at single battery power supply applications and provides the capability of megahertz switch speed is presented. It features a minimum power supply voltage of 1.0V and is able to operate at a frequency as high as 1MHz.

The rest of the paper is organised as follows. In section 2, conventional bipolar DC-DC converter driver structures are briefly described. Section 3 presents improved circuit design and performance analysis in detail. In section 4, simulation results of the circuit are given in terms of minimum power supply, maximum operational frequency and output transition times. Finally, conclusions are drawn in section 5.

2. DC-DC CONVERTER DRIVER STRUCTURES

Bipolar DC-DC converter drivers are frequently used to generate the output voltage and current with desired performance. Among the most popularly used driver structures are emitter follower driver and Totem pole output driver. Figure 1 shows a typical principle structure of an emitter follower driver [1], in which V_{OH} and V_{OL} are output high level and output low level, respectively; I_{OMAX} is maximum output current; and t_{TLH} and t_{THL} are output low-to-high transition time and output high-to-low transition time, respectively.

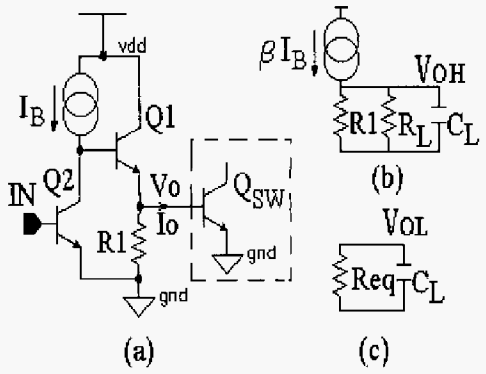

Figure 1. A typical emitter follower driver
(a). Principle circuit
(b). Equivalent circuit of output high level
(c). Equivalent circuit of output low level

From this structure, the following equations can be easily derived

$$V_{OH} \le V_{DD} - V_{beQ1} \quad (1)$$

$$V_{OL} \ge 0V \quad (2)$$

$$I_{OMAX} \approx \beta I_B \quad (3)$$

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$$t_{TLH} \approx \frac{V_{OH} C_L}{\beta I_B} \quad (4)$$

$$t_{THL} \approx R_{eq} C_L \ln \frac{V_{OH}}{V_{OL}} \quad (5)$$

where C_L is the equivalent output capacitance of the driver and R_{eq} is Thevenin equivalent resistance of the output node of the driver [2]. Consider that the switch transistor Q_{SW} is NPN type, we have

$$V_{OH} \geq V_{beQSW} \quad (6)$$

By combining the equations (1) and (6), the equation below can be obtained

$$V_{DD} \geq V_{beQSW} + V_{beQ1} \approx 0.7 + 0.7 = 1.4V \quad (7)$$

Thus, the minimum power supply voltage of the driver is approximately 1.4V. Here, since the R_{eq} usually has a considerable value, the t_{THL} is relatively long.

A typical structure of Totem pole output driver is shown in Figure 2 [3].

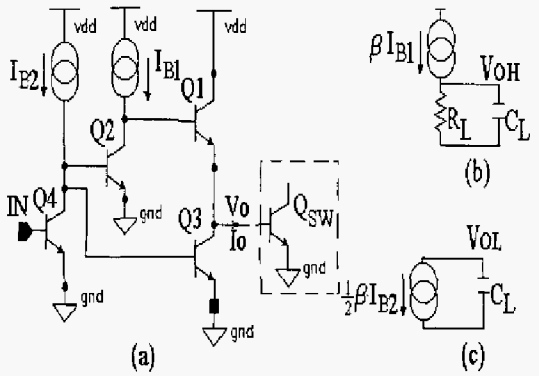

Figure 2. A typical Totem pole driver
(a). Principle circuit
(b). Equivalent circuit of output high level
(c). Equivalent circuit of output low level

Similar to the analysis of the emitter follower driver given above, the output characteristic equations of Totem pole structure are as follows.

$$V_{OH} \leq V_{DD} - V_{beQ1} \quad (8)$$

$$V_{OL} \geq V_{CESATQ3} \quad (9)$$

$$I_{OMAX} \approx \beta I_{B1} \quad (10)$$

$$t_{TLH} \approx \frac{V_{OH} C_L}{\beta I_{B1}} \quad (11)$$

where $V_{CESATQ3}$ is the saturation voltage of the transistor $Q3$. Assume that the base currents of the transistors $Q2$ and $Q3$ are the same; the t_{THL} of this circuit can be derived

$$t_{THL} \approx 2 \frac{(V_{OH} - V_{OL}) C_L}{\beta I_{B2}} \quad (12)$$

Similarly, considering that the switch transistor Q_{SW} is NPN type and combining the equations (6) and (8), the minimum power supply of Totem pole driver can be easily expressed as

$$V_{DD} \geq V_{beQSW} + V_{beQ1} \approx 0.7 + 0.7 = 1.4V \quad (13)$$

Therefore, both emitter follower driver and Totem pole driver have the same minimum power supply voltage (V_{DD}), the same maximum output current (I_{OMAX}) and the same output low-to-high transition time (t_{TLH}). However, Totem pole driver has improved output high-to-low transition time (t_{THL}) over emitter follower driver, because this time is no longer relevant to R_{eq} in the structure.

3. IMPROVED DC-DC CONVERTER DRIVER

In order to enhance performance of the DC-DC converter drivers described in section 2, the improvements on these traditional structures have been made in two aspects. First of all, to reduce the minimum power supply voltage, the transistor $Q1$ in the Figure 1 has been replaced by a PNP-type transistor, as shown in Figure 3.

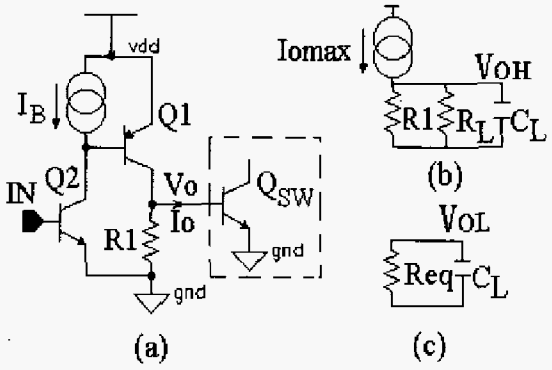

Figure 3. V_{DD} improvement of DC-DC converter driver
(a). Principle circuit
(b). Equivalent circuit of output high level
(c). Equivalent circuit of output low level

From the circuit, the output high level of the driver is given below

$$V_{OH} = V_{DD} - V_{CESATQ1} \quad (14)$$

where $V_{CESATQ1}$ is the saturation voltage of the PNP-type transistor $Q1$. By combining the equations (6) and (14), the minimum V_{DD} is obtained

$$V_{DD} \geq V_{beQSW} + V_{CESATQ1} \approx 0.7 + 0.3 = 1.0V \quad (15)$$

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Clearly, this reduced minimum V_{DD} suits single battery applications.

When the output of the circuit is high level, i.e., during V_{OH}, the PNP-type $Q1$ operates in saturation region and both its base-emitter junction and base-collector junction are forward biased with very low resistance. As a result, the maximum output current I_{OMAX} of the driver is determined by the maximum output current capability of the $Q1$, which is largely dependent upon fabrication process [4].

Once the $Q1$ is saturated, its collector has very low equivalent resistance, and therefore output voltage rises up very rapidly and the rising time spent is negligible [4]. Consequently, the output low-to-high transition time t_{TLH} is decided by the time the $Q1$ enters into saturation. Usually, in order to have high output current capability, the area of the $Q1$ has to be big enough. This leads to large parasitic capacitance, and hence the time the $Q1$ enters into saturation is prolonged.

When the output of the circuit is low level, i.e., during V_{OL}, the equivalent circuit of the output low level is the same as the Figure 1 (c), and, therefore, the output high-to-low transition time t_{THL} is still expressed by the equation (5). Again, due to the large R_{eq}, the t_{THL} is relatively long.

In order to reduce both t_{TLH} and t_{THL}, further improvement on the circuit of the Figure 3 has been made, as shown in Figure 4. This is described below.

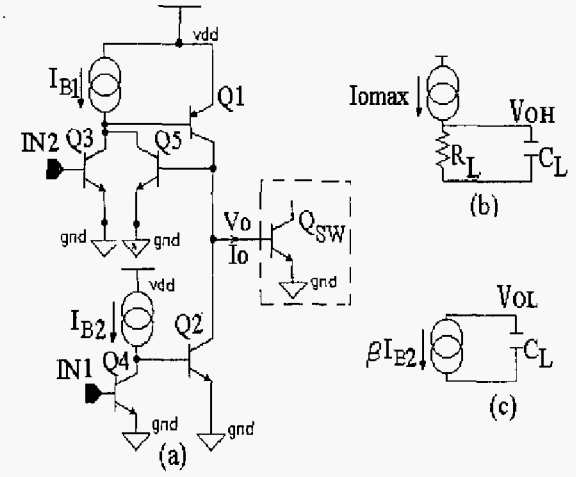

Figure 4. Improved DC-DC converter driver
(a). Principle circuit
(b). Equivalent circuit of output high level
(c). Equivalent circuit of output low level

To reduce t_{TLH}, the transistor $Q5$ is introduced, which, together with $Q1$, forms a positive feedback. The feedback significantly accelerates the $Q1$'s speed entering saturation, thus reducing the low-to-high transition time of output voltage.

As indicated in the section 2, Totem pole structure has improved t_{THL} over emitter follower structure. In the Figure 4, the transistors $Q2$ and $Q4$ are introduced to incorporate Totem pole structure into our design. The result is that the t_{THL} of the circuit can be reduced and given as follows

$$t_{THL} \approx \frac{(V_{OH} - V_{OL})C_L}{\beta I_{B2}} \tag{16}$$

Ideally, the two inputs $IN1$ and $IN2$ of the circuit should be the same, but in practice, it is difficult to keep them identical. In order to have correct logic sequence at output, the relationship between $IN1$ and $IN2$ has to be specified, as shown in Figure 5, and has the following features [5].

- If $IN1$ is low level, output must be low level.
- When $IN1$ becomes high level, output may still be low level if $IN2$ is low level. Output becomes high level only if $IN2$ goes high level before $IN1$ does.
- Once output is high level, as long as $IN1$ remains high level, output will be high level even if $IN2$ changes from high level to low level. This is because that the self-lock feature of the positive feedback formed by the $Q1$ and $Q5$ keeps output at high level.

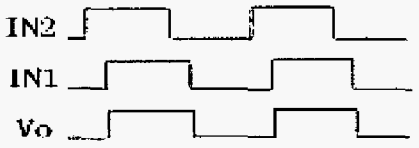

Figure 5. Relationship between $IN1$, $IN2$ and output

In a word, as long as the change of $IN2$ from low level to high level is ahead of $IN1$, corresponding to the input sequence of the $IN1$, the circuit will be able to produce required output sequence.

4. SIMULATION RESULTS

To evaluate the performance of the designed circuit, the simulations based on the Samsung Bipolar Process BCH4 model have been carried out. The results of HSPICE simulation suggest that the minimum power supply, under which the circuit functions properly, is 1.0V. This achieves the design specification of single-battery applications (less than 1.2V). When the input sequences of $IN1$ and $IN2$ are as described in the Figure 5, the output voltage Vo and the output current Io can be obtained, as shown in Figure 6. Here, when the circuit operates at 1MHz frequency, integrity of the output signals is kept very well. This demonstrates fast switching capability of

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the circuit.

Through the simulations, the main parameters of the output signals are also obtained. The maximum output current I_{OMAX} is 10.3mA. The output low-to-high transition time t_{TLH} is 20.3ns and the output high-to-low transition time t_{THL} is 39.4ns.

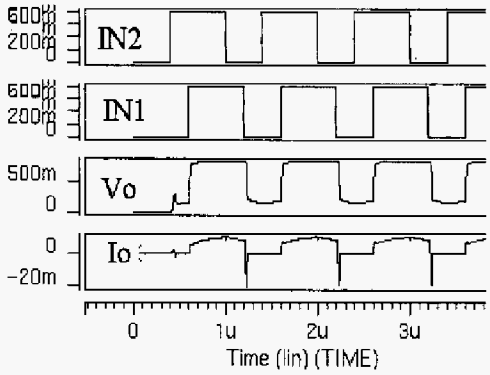

Figure 6. Simulation results of improved driver circuit

5. IMPLEMENTATION

In order to fabricate the circuit designed above, minor adjustment has been made to the Figure 4, as shown in Figure 7. This is because that the following assumptions have been made for practical operation of the circuit. When output is high level, the circuit operates exactly as the one described in the section 3. When output becomes low level, the *IB1* and *IB2* (in the Figure 4) should shut, i.e., the transistors *Q1*~*Q5* are off. Although this will result in a slight increase of output voltage, there will be no current supplied to turn on the switch transistor Q_{SW}. Therefore, there will be no affect on output logic.

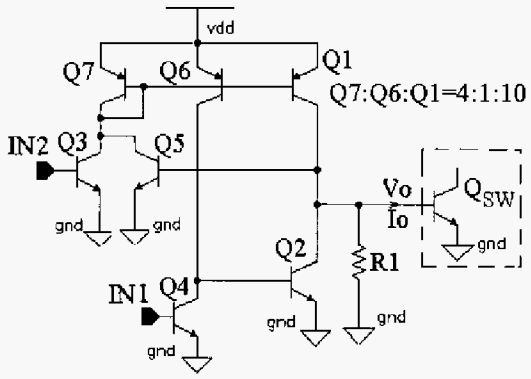

Figure 7. Implementation circuit

This adjustment practically minimises the static power consumption of the circuit and further reduces the low-to-high transition time of output. In the Figure 7, *Q7*:*Q6*:*Q1* = 4:1:10 is the ratio of the emitter areas between the transistors *Q7*, *Q6* and *Q1*. The tests carried out on prototype chips suggest that the chips function correctly and fully meet specifications of design.

6. CONCLUSIONS

Based on traditional emitter follower driver and Totem pole driver, a bipolar driver circuit with low power supply, high switch speed, and reduced output transition times has been designed for boost DC-DC converter applications. The circuit analysis and simulation results show that while the improved circuit can effectively operate at 1.0V power supply and at 1MHz frequency, its output also has a low-to-high transition time of 20.3ns and a high-to-low transition time of 39.4ns. Therefore, the circuit design presented in this paper is particularly suitable for the wireless and portable equipment/devices powered by single battery and operating in a wide range of frequency.

7. REFERENCES

[1] P. R. Gray, P. J. Hurst, and R. G. Meyer, *Analysis and Design of Analogue Integrated Circuits (Fourth Edition)*, John Wiley & Sons Inc., New York, 2001.

[2] A. Razavi, *Design of Analogue CMOS Integrated Circuits*, McGraw-Hill Companies Inc., Boston, MA, 2001.

[3] A. B. Grebene, *Bipolar and MOS Analogue Integrated Circuit Design*, John Wiley & Sons Inc., New York, 1984.

[4] Y. Liu and F. Zhang, *Principle of Transistors*, National Defence Industry Press, China, 2002.

[5] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Oxford University Press, Oxford, UK, 2004.

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