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# A HIGH PERFORMANCE CMOS BAND-GAP REFERENCE CIRCUIT DESIGN

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## ABSTRACT

This paper presents a CMOS band-gap reference design, which possesses the characteristics of low noise and high power supply rejection capability. Thus, it is suitable for the applications of a wide range of frequency and power input. In order to reduce thermal noise and to provide the output reference voltage that is resistant to power supply variations, the design incorporates an RC filter into conventional reference structure. Moreover, a fast turn-on circuit is introduced into the design to improve turn-on time of the circuit. The simulation results show that within the frequency range from 100Hz to 10MHz, the design has achieved an average power supply rejection ratio (PSRR) of more than 80dB and an average noise of 8.5uVrms. With the fast turn-on circuit, the improved band-gap reference circuit can reach its steady state within 100 microseconds.

## 1. INTRODUCTION

With the development of modern electronic systems, high performance analogue devices have been becoming increasingly important for systems integration. As one of the most basic components in analogue VLSI, band-gap voltage reference circuit has been widely used in many applications that require highly accurate voltage reference, such as LDO regulators, high-precision comparators, D/A and A/D converters, and RF circuits and so on [1, 2]. In this paper, a CMOS band-gap voltage reference circuit that incorporates an RC filter and a fast turn-on circuit into traditional reference structure is presented. It features high power supply rejection ratio (more than 80dB) and low noise voltage (8.5uVrms on average) when circuit frequency varies between 100Hz and 10MHz. And with the proposed fast turn-on circuit, it has a turn-on time of less than 100ms.

The rest of the paper is organised as follows. In section 2, a typical CMOS band-gap structure is briefly described. Section 3 presents the improved circuit with RC filter and fast turn-on circuit in detail. In section 4, simulation results of the circuit are given in terms of power supply rejection capability, noise voltage and circuit turn-on time. Finally, conclusions are drawn in section 5.

## 2. CMOS BAND-GAP REFERENCE

CMOS band-gap structures are frequently used to generate the reference voltage with desired accuracy performance. Since the key factors that affect the reference accuracy are power supply, temperature, and output noise, etc., various methods and techniques have been adopted to improve PSRR, minimise temperature coefficient and reduce noise. Figure 1 shows a typical kernel circuit of CMOS band-gap reference [3]. In this circuit, through the feedback from reference output, the input voltages ($V_X$ and $V_Y$) of operational amplifier tend to be equal, therefore the voltage across the resistor $R3$ is

$$V_{R3} = I_2 R_3 = V_{EB2} - V_{EB1} = \frac{KT}{q}\ln(\frac{J_2}{J_1}) = V_T \ln(\frac{J_2}{J_1}) \quad (1)$$

where $V_T = KT/q$ is thermal voltage, $J_1$ and $J_2$ are the emitter current densities of the transistors $Q1$ and $Q2$, respectively, and their ratio is

$$\frac{J_2}{J_1} = \frac{I_2 A_{E2}}{I_1 A_{E1}} = N\frac{R_2}{R_1} \quad (2)$$

where $N$ is the ratio of the emitter area ($A_{E2}$) of $Q2$ to the emitter area ($A_{E1}$) of $Q1$. Combining the equations (1) and (2) gives

$$V_{R3} = V_T \ln N\frac{R_2}{R_1} \quad (3)$$

Thus,

$$V_{R2} = \frac{R_2}{R_3} V_T \ln N\frac{R_2}{R_1} \quad (4)$$

The output reference voltage $V_{REF}$ can be derived as

$$V_{REF} = V_{EB2} + V_{R2}$$

$$= V_{EB2} + \frac{R_2}{R_3}.V_T \ln\left(N.\frac{R_2}{R_1}\right) \qquad (5)$$

The principle to achieve temperature performance is that the thermal voltage $V_T$ with a positive temperature coefficient compensates the emitter-to-base voltage $V_{EB2}$, which has a negative temperature coefficient. Therefore, theoretically, by choosing appropriate parameters of resistors and transistors, the reference output can display a zero temperature coefficient. In terms of the effect of power supply ripple on accuracy of the reference, since $V_T$ is irrelevant to power supply and such ripple has very limited influence on $V_{EB2}$, the output reference $V_{REF}$ can effectively resist power supply variation.

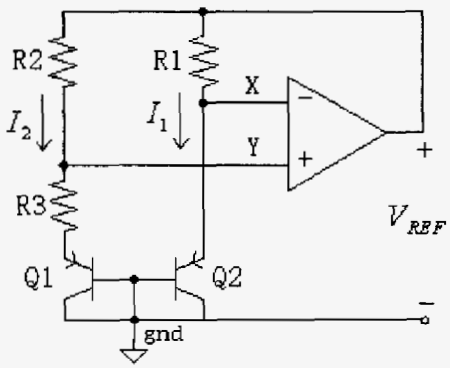


Figure 1. Typical structure of CMOS band-gap reference

## 3. IMPROVED BAND-GAP REFERENCE

A practical CMOS band-gap reference circuit is shown in Figure 2. The kernel part of the reference is compose of the transistors *Q1* and *Q2*, the resistors *R1~R4* and the operational amplifier $A_1$. The current mirror that consists of the PMOS *M1~M4* provides quiescent bias current for the circuit. Similar to the derivation given in the section 2, the voltage across the resistor $R_3$ can be written as

$$V_{R3} = V_{EB2} - V_{EB1} = V_T \ln\left(N\frac{R_2}{R_1 + R_4}\right) \qquad (6)$$

The current that flows through the resistor *R2* is given below

$$\frac{V_T}{R_3}\ln\left(N\frac{R_2}{R_1 + R_4}\right)$$

Thus, the reference output voltage $V_{bg}$ can be easily determined by

$$V_{bg} = V_{EB2} + \left(\frac{R_2}{R_3}\right)V_T \ln\left(N\frac{R_2}{(R_1 + R_4)}\right) \qquad (7)$$

To obtain an optimal (minimal) temperature coefficient, the following parameters has been assumed/chosen

$V_{EB2} = 0.67$V
$R1 = 11R4$
$R2 = 22R4$
$R3 = 3R4$
$N = 8$

Therefore, the reference output $V_{bg}$ is 1.25V.

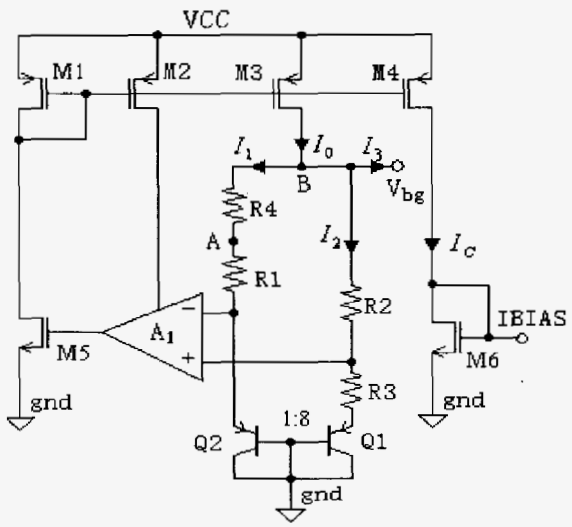


Figure 2. A practical CMOS band-gap reference circuit

In order to improve the ability of output reference voltage in resisting power supply ripples and reducing output noise, an improved CMOS band-gap reference structure is proposed in this paper by connecting an RC filter to the output of the reference, as shown in Figure 3.

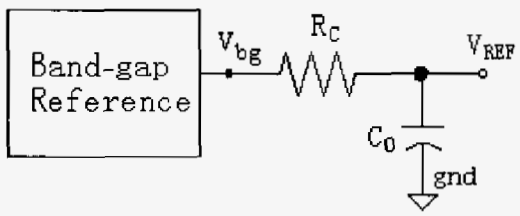


Figure 3. Improved CMOS band-gap reference structure

In the structure, bringing in the filtering components $R_C$ and $C_0$ means that a pole at the frequency $1/2\pi RC$ has been introduced. This is equivalent to that there is a zero

point of 1/PSRR (or a maximum PSRR) at the frequency, since the PSRR is the ratio of the variation of power supply to the variation of reference output. As a result, the average PSRR over entire working frequency bandwidth has been significantly increased through the RC filter. The frequency corresponding to the zero point is expressed by

$$f_0 = 1/2\pi RC = 1/2\pi(R_C + Z_O)C_0 \qquad (8)$$

where *Zo* is output impedance of the band-gap reference. If we choose $R_C$=200KΩ, $C_0$=10nF, then the $f_0$ is about 30Hz.

In addition to the improved PSRR, the RC filter also reduces output noise. When operating at high frequency, noise of the reference is caused primarily by thermal noise [2, 4]. Since a pole at the frequency $f_0 = 1/2\pi RC$ has been introduced, the noise with a frequency that is equal to or higher than the $f_0$ can be effectively filtered out. If the same parameters ($R_C$ and $C_0$) are used as the above, the $f_0$ is approximately 30Hz.

While introduction of an RC filter improves PSRR and reduces noise, it also increases the turn-on time of the reference circuit. This is because that high output impedance of the reference prolongs time to charge the capacitor $C_0$ (approximately 15ms for a 10nF capacitor). Generally, once power is on, the $V_{bg}$ can reach its steady value (for example 1.25V) very quickly (typically less than 50us). However, with the RC filter, the resistor $R_C$ (200KΩ) separates the capacitor $C_0$ from the $V_{bg}$ and only a small current $I_3$ from the $V_{bg}$ charges the capacitor. As a result, it takes a much longer time (than 50us) to allow the $V_{REF}$ to reach its steady value (1.25V). In order to avoid this turn-on delay, a fast turn-on circuit has been designed, as shown in Figure 4, which achieves a turn-on time of less than 100us for a $C_0$=10nF while maintaining the PSRR and noise performance of the reference circuit.

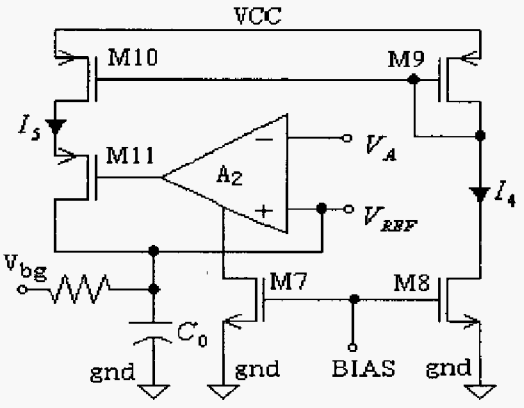


Figure 4. Fast turn-on circuit

In this circuit, the $V_A$ is voltage of point A (Figure 2) and the BIAS, which provides bias current for the fast turn-on circuit, is connected to IBIAS (Figure 2). The PMOS *M10* and *M11* form a current source that is controlled by output of the comparator $A_2$. The rationale of the fast turn-on circuit is explained below.

The $V_A$ is normally set to be approximately 50 mV less than $V_{bg}$' value to prevent overshooting $C_0$ and to overcome input offset error of the $A_2$ [5, 6]. When power is on, initially, the value of the voltage $V_{REF}$ across the capacitor $C_0$ is zero and the value of the $V_A$ is higher than that of the $V_{REF}$, therefore, the $A_2$ outputs a low voltage (i.e. the switch *M11* is on) and the constant current $I_5$ from the current source charges the $C_0$ rapidly. Once the $V_{REF}$ reaches the value of the $V_A$, which is very close to steady value of the $V_{REF}$, the $A_2$ outputs a high voltage (i.e. the switch *M11* is off) and the $C_0$ is no longer charged by the $I_5$. This effectively shuts down the fast turn-on circuit and allows only the small current $I_3$ (Figure 2) to continue charging the $C_0$ (through $R_C$) in order to reach the final steady value (e.g. 1.25V). Since the bias current $I_5$ in this improved reference circuit is constant, charge time can be accurately estimated by the following equation

$$\Delta t = \frac{C_0 \Delta V_{REF}}{I_5} \qquad (9)$$

From the Figure 2, the current of point B is derived by

$$I_0 = I_1 + I_2 + I_3 = \frac{V_{bg}}{R_C} + \frac{\Delta V_{BE}}{R_3}\left(\frac{R_2}{R_1 + R_4} + 1\right) \qquad (10)$$

If we use the parameters as given above in this section and assume that the ratio of W/L (width/length of transistor) of *M3* to *M4* is 6:1 and the same for *M8* to *M6* (Figure 2), we have $I_4 = I_C = I_0/6$. Furthermore, if we assume that the ratio of W/L of *M9* to *M10* is 1:150, then the $I_5$ can be calculated and it is approximately 150uA. Thus, the charge time given in the equation (9) can be accurately determined.

## 4. SIMULATION RESULTS

To evaluate the performance of the designed circuit, the simulations based on 0.6um CMOS process have been carried out. Figure 5 gives the HSPICE simulation results of PSRR versus frequency of the circuit shown in Figure 3. The results demonstrate that with introduction of an RC filter, PSRR of the reference has been significantly improved, particularly at high frequencies. If we take $C_0$=10nF as an example, PSRR is always above 80dB across whole range of frequency. In contrast, without the

RC filter ($C_0$=0), PSRR starts falling sharply at 30Hz and reaches no more than 20dB at high frequencies.

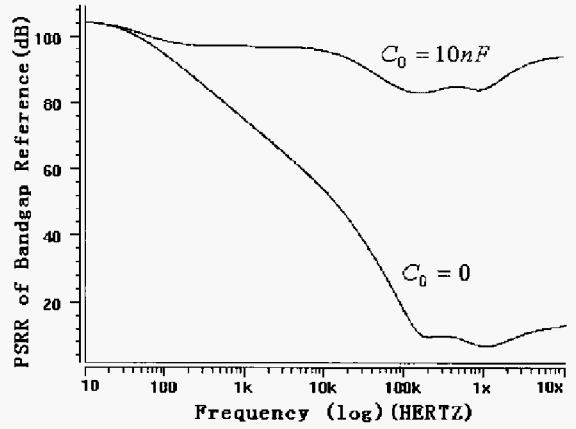


Figure 5. PSRR improvement of band-gap reference

The HSPICE simulation results of noise reduction are presented in Figure 6, which shows that with the RC filter, noise of the reference has been greatly suppressed within certain frequency range. If a 10nF capacitor is used, a pole will be generated at 30Hz, from which noise starts to reduce. When the circuit operates between 100Hz and 10MHz, average noise voltage is only about 8.5uVrms.

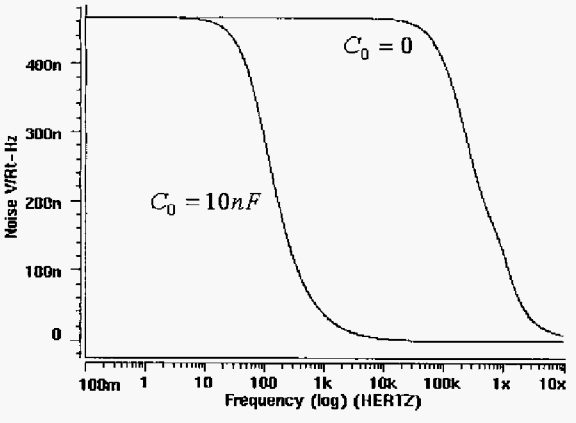


Figure 6. Noise reduction of band-gap reference

In order to estimate turn-on time of the reference, we obtained the turn-on delays from simulations, as illustrated in Figure 7. As can be seen, with incorporation of a fast turn-on circuit into the circuit shown in Figure 3, the speed that the $V_{REF}$ reaches its steady value has been dramatically increased. With a $C_0$=10nF, turn-on time is less than 100us, while it is about 15ms without the turn-on circuit.

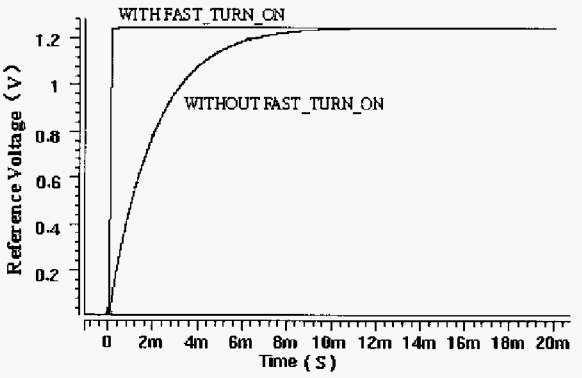


Figure 7. Turn-on time reduction of band-gap reference

## 5. CONCLUSIONS

By introducing an RC filter into traditional CMOS band-gap reference structure and designing a fast turn-on circuit, a CMOS band-gap reference circuit with high power supply rejection capability, low output noise and quick turn-on has been designed for modern analogue VLSI applications. The circuit analysis and simulation results show that while the improved circuit design effectively resists power supply variations and significantly reduces high-frequency noise level, it also maintains a rapid turn-on time. Therefore, the circuit is able to operate in a wide range frequency and power supply conditions.

## 6. REFERENCES


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