Over Sampling Successive Approximation Technique for MEMS Differential Capacitive Sensor

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***Abstract*—This paper proposed an over sampling successive approximation (OSSA) technique to build switched-capacitor capacitance-to-voltage convertor (SC-CVC) for readout circuit of MEMS differential capacitive sensor. The readout circuit employing the OSSA technique has significantly improved resistance to common-mode parasitic capacitance of the input terminal of the readout circuit. In the OSSA readout circuit, there are 5 main non-ideal characteristics: holding error, recovery degradation, increment degradation, rise-edge degradation and charge injection which reduce the accuracy and the settling time of the circuit. These problems are explained in detail and their solutions are given in the paper. The OSSA readout circuit is fabricated in a commercial 0.18um BCD process. To show the improvement evidently, a reported traditional readout circuit is also reproduced and fabricated using the same process. Compared with the traditional readout circuit, the proposed readout circuit reduces the affect of common-mode parasitic capacitance on the accuracy of SC-CVC by more than 23.8 dB, reduces power dissipation by 69.3%, and reduces die area by 50%.**

***Index Terms*—Differential capacitive sensor, accelerometer, common-mode parasitic capacitance, parasitic capacitance insensitive, micro-electromechanical systems (MEMS) sensors, low power circuits, readout circuit**

I. Introduction

MEMS (Micro-electromechanical Systems) differential capacitive sensor is a popular form of sensors for recent IoT (Internet of things) applications, such as accelerometer [1] [2], gyroscope [3], barometer [4], etc.. This is because compared to the sensors implemented based on other physical principles such as piezoresistive or tunneling, capacitive sensor has great advantages of lower power consumption, better temperature coefficient and manufacturability [5]-[7].

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In order to read out the differential capacitive sensor, an AC excitation is needed. The most popular AC excitations are sine excitation and rectangular excitation [8], [9]. The sine excitation is able to measure resistance, capacitance and inductance at the same time [9]. However, if the capacitance is the only parameter to be measured, rectangular excitation is a better choice for cost efficiency [8].

To implement the readout circuit, fully differential switched-capacitor circuit is employed which can generate rectangular excitation, provide accurate operation with the well matched values between CMOS capacitors and overcome the common-mode interferences caused by voltage, process and temperature [10]-[13]. The Correlated Double Sampling (CDS) technique is also compatible with switched-capacitor circuit to further improve the resistance to flicker noise and DC offset [11]-[13].

However, a particular phenomenon "1/A error deterioration" will happen in traditional fully differential switched-capacitor readout circuit with CDS due to the parasitic capacitance introduced by the MEMS manufacturing and packaging process (refers to die-to-die bonding), which affect the accuracy of output severely. Although the predicating techniques and the track-and-hold (or sample-and-hold) techniques had been proposed to solve the 1/A error [14], [15], it is hard to apply them to the readout circuit for MEMS capacitive sensor for "1/A error deterioration" solution. This is because these techniques require well matching of the values between the capacitors in predictive/tracking path and the capacitors in measuring/holding path, which is impractical in the situation where those capacitors are manufactured in different processes (MEMS and CMOS).

In this paper, "over sampling successive approximation "(OSSA) technique is proposed to solve the "1/A error deterioration" in the readout circuit for MEMS capacitive sensor. The rest of the paper is organized as follows. In the section II, an example of differential capacitive sensor is described and the "1/A error deterioration" is analyzed in detail. In the section III, the principle of the OSSA technique is illustrated. In the section IV, the circuit implementations of an OSSA amplifier are presented, and the non-ideal characteristics are analyzed in detail. In the section V, the OSSA amplifier is applied in a readout circuit for accelerometer, and the post simulation and test results are shown. The conclusions are then drawn in the section VI.

II. 1/A Error Deterioration

The structure of basic fully differential readout circuit with

CDS for measuring differential capacitive sensor is shown in Fig. 1. [2], [11]-[13]. C_{S1} and C_{S2} are equivalent capacitors of differential capacitive sensor, whose values change with the environmental physical variable such as force, i.e.

$$C_{S1} = C_0 + \Delta C$$
$$C_{S2} = C_0 - \Delta C \quad (1)$$

where C_0 is the common-mode capacitance, ΔC is the differential capacitance of differential capacitive sensor.

In ideal condition, the gain A_0 of differential amplifier is infinite. As a result, the output voltages V_{O+} and V_{O-} of the charge amplifier are,

$$V_{o+}C_i = C_{s2}V_R - C_0V_R$$
$$V_{o-}C_i = C_{s1}V_R - C_0V_R \quad (2)$$

where V_R is the reference voltage. Apply the equation (1) to the equation (2),

$$V_o = V_{o+} - V_{o-} = \frac{2\Delta C}{C_i}V_R \quad (3)$$

The equation (3) suggests that in ideal conditions, the outputs is completely a linear function of variable ΔC, which is the exact situation we expected.

However, in the practical situations, the gain of amplifier A_0 is finite. As a result, the voltage difference across the input terminals of the amplifier (A_+ and A_- in Fig. 1) is not zero in order to maintain the output voltage level and is in proportion to the level of the outputs. The 1/A error is denoted by the symbol $\Delta V_{1/A}$

$$\Delta V_{1/A} = \frac{1}{A_0}V_o \quad (4)$$

where A_0 is the open-loop gain of the amplifier. Notice that the 1/A error is different from the concept of "gain error" (defined as the fractional error between the desired gain and the actual gain [21]). With the definition of the 1/A error, the explanation of the reduction of output accuracy by the parasitic capacitance is simplified.

The $\Delta V_{1/A}$ is added to the reference voltage V_R when the circuit executes conversion. That means the output voltages of the charge amplifier in this situation are,

$$V_{o+}C_i = C_{s2}\left(V_R - \frac{1}{2}\Delta V_{1/A}\right) - C_0\left(V_R + \frac{1}{2}\Delta V_{1/A}\right)$$
$$V_{o-}C_i = C_{s1}\left(V_R + \frac{1}{2}\Delta V_{1/A}\right) - C_0\left(V_R - \frac{1}{2}\Delta V_{1/A}\right) \quad (5)$$

Apply the equation (1) to the equation (5),

$$V_o = V_{o+} - V_{o-} = \frac{2\Delta C}{C_i}\left(V_R - \Delta V_{1/A}\right) - \frac{2C_0}{C_i}\Delta V_{1/A} \quad (6)$$

In general, $\Delta V_{1/A}$ is in the order of 10^{-3} volt, which is far smaller than V_R. So the equation (6) is simplified as,

$$V_o = \frac{2\Delta C}{C_i}V_R - \frac{2C_0}{C_i}\Delta V_{1/A} \quad (7)$$

Then apply the equation (4) to the equation (7), the final expression of the output is,

$$V_o = \frac{2\Delta C}{C_i}V_R\left(\frac{1}{1+\sigma_d/A_0}\right)$$
$$\sigma_d = \frac{2C_0}{C_i} \quad (8)$$

where σ_d is the deterioration factor. Compared to the ideal output in the equation (3), the equation (8) indicates that the 1/A error decreases the output. And a much more important fact is that the 1/A error has deteriorated by a coefficient σ_d. That means this switched-capacitor readout circuit for differential capacitive sensor in Fig. 1 suffers much severer 1/A error than other forms of switched-capacitor amplifier [14], [15].

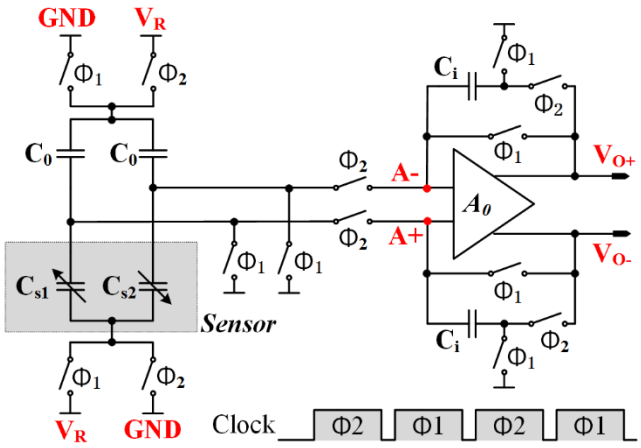


Fig. 1 basic fully differential readout circuits for differential capacitive sensor

This is due to the large common-mode parasitic capacitance introduced by the MEMS sensor's package [11], [16]. A measurement on a commercial 3-axis MEMS accelerometer is conducted. As shown in Fig. 2, the MEMS capacitive sensor is sealed under silicon cap and connected to ASIC via gold bounding wire side by side. The capacitance of the sensor is measured with test excitation varying in full range. The measurement results show that,

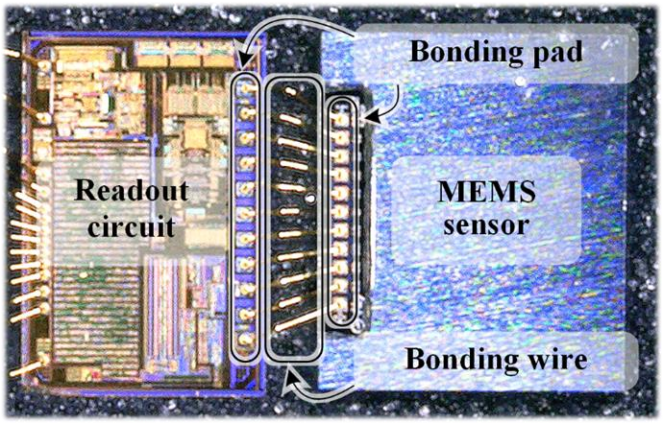
- the maximum range is ΔC_{max}=145 fF;
- the sensor's total capacitor is 905 fF;

And the main common-mode parasitic capacitances of readout circuit extracted through post simulation are that,

- the capacitance of bonding pad is 534fF;
- the capacitance of ESD protection to VDD is 954fF;
- the capacitance of ESD protection to GND is 726fF;

So the deterioration factor σ_d is approximately 42 (C_0=905fF+534fF+954fF+726fF, C_i=ΔC_{max} =150fF). This means that the 1/A error is amplified by more than 32dB.

The above characteristic of the sensor is called "low modulation depth". That is to say, the value of the capacitance producing signal charge is far smaller than the value of the parasitic capacitance producing interference charge, which significantly decreases the output accuracy of readout circuit. Furthermore, the increase of C_0 or decrease of C_i will make the problem worse. For example, in order to get high resolution, the value of C_i is selected as the 1/4 the value of ΔC_{max} or even lower [10]-[13].Then the deterioration factor σ_d would easily reach 168 or even higher. This means that the 1/A error will be amplified by more than 45dB.



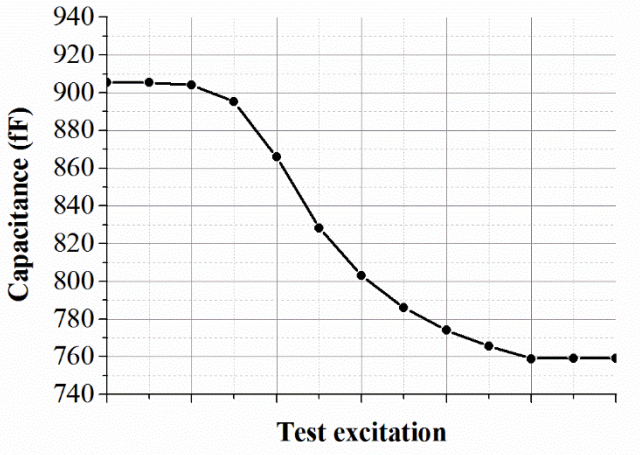


Fig. 2. Measurement results of capacitance of a commercial MEMS accelerometer to illustrate the practical deterioration factor σ_d

III. OVER SAMPLING SUCCESSIVE APPROXIMATION TECHNIQUE

To overcome deteriorated 1/A error mentioned in the section II, the Over Sampling Successive Approximation (OSSA) technique is proposed in this section. The OSSA technique is different from the traditional Over Sampling (OS) technique which is mainly applied in an integrating/adding/averaging operation aimed at improving the noise performance (a statistic method) [11]. The OSSA technique is the OS technique applied in an iteration operation aimed at improving the accuracy (an approximation method).

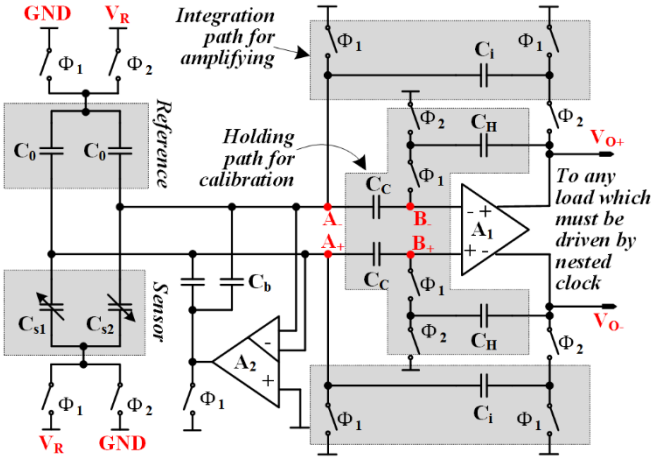
The kernel concept of the OSSA technique is that the system gets its final operation result by several iteration steps rather than one step. During each iteration step, the OSSA system calibrates the system parameters based on the operation errors from the last step, so as to get an operation results more approximate to the ideal results than the system does in the last step.

To implement the OSSA technique in the readout circuit, the strategy is to calibrate the readout circuit based on the 1/A error in each step. Specifically, the voltage difference between the input terminals (A_+ and A_- in Fig. 1) should be minimized. This is done by inserting the calibration capacitor Cc between the input terminals (A_+ and A_-) and the amplifier, as shown in Fig. 3(a). During the phase Φ1, the C_C is calibrated by the holding path which is composed of holding capacitor C_H and relevant switches. And during the phase Φ2, this circuit amplifies the charge from the sensor (C_{S1} and C_{S2}) by the integration path which is composed of integration capacitor C_i and relevant switches. As the 1/A error is reduced by the calibrated C_C during phase Φ1, the readout circuit can achieve a higher accuracy during phase Φ2 in this step than the readout circuit does during phase Φ2 in the last step. The formulas will be derived later.

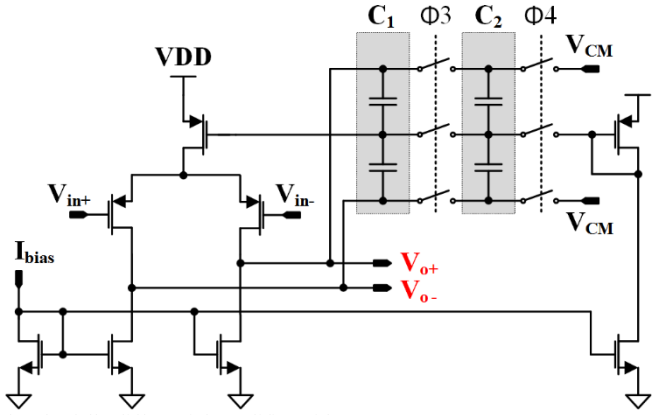
The calibration capacitors Cc must be handled very carefully to achieve high calibration accuracy. In details, when the Cc is been charged or discharged (during the rising/falling edge of Φ1), the loads connected to the terminal Vo+ and Vo- should not have any switching operation to prevent unwanted charge injection into the Cc. The loads refer to the Switched-Capacitor Common-Code Feedback (SC-CMFB) of the fully differential amplifier A1 which is composed of C1, C2 and relevant switches in Fig. 3(b)), as well as any SC circuits in the next stage. The nested non-overlapping clocks is proposed to drive those loads. As shown in Fig. 3(c), the phases Φ3 and Φ4 which are used to drive the loads, are nested inside the phases Φ1 and Φ2 which are used to drive the OSSA amplifier. Driven by the nested clocks, the charge injection from those loads are isolated from the calibration capacitor. Thus the high calibration accuracy is achieved.

The generator of the nested non-overlapping clock is proposed in Fig. 3(d). It is able to generate two nested clocks with each having two phases. Each clock has independent leading edge delay and post edge delay. This generator can also produce more than two clocks by cascading, and these clocks are all non-overlapped and nested. In this work, only two two-phase clocks are needed.

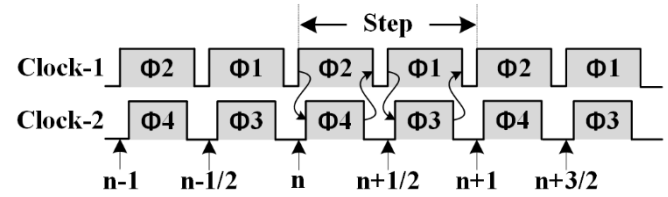
Although the main structure of the OSSA amplifier is based on the single-end T/H amplifier in the reference [14], the major improvement over the accuracy has been achieved through the following 3 aspects of the work: developing the fully differential structure, proposing the nested non-overlapping clocks (alone with the generator) and parameter optimization based on the analysis of non-idealities. This improvement aims specifically at the application of the low modulation depth MEMS sensor, which has not been considered in the published references on T/H SC amplifier.



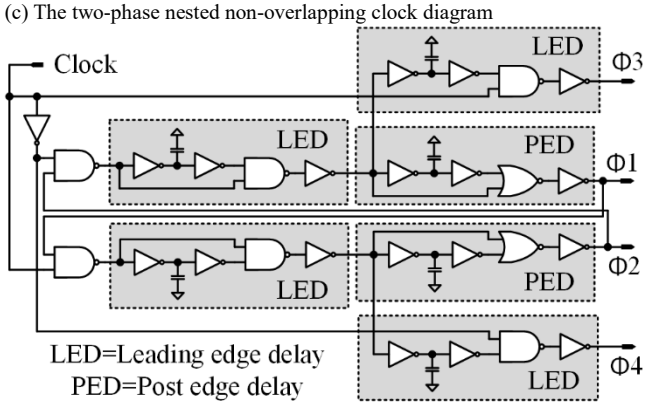
(a) The circuit topology



(b) The fully differential amplifier with SC-CMFB



(c) The two-phase nested non-overlapping clock diagram



(d) The two-phase nested non-overlapping clock generator

Fig. 3. The circuit implementation of OSSA technique (OSSA amplifier) for differential capacitive sensor

The operational process of the OSSA amplifier is explained in detail as follows.

Assuming the output voltage level of the OSSA amplifier in the Fig. 3(a) in the 1st iteration step is denoted by $V_o(n)$, and the increment of output voltage level in the 1st iteration step is denoted by $\Delta V_o(n)$. During the 2nd, 3rd, till the N-th step of the operation, the outputs are denoted by $V_o(n+1)$, $V_o(n+2)$,…, $V_o(n+N)$, respectively, and the increments of the output are denoted by $\Delta V_o(n+1)$, $\Delta V_o(n+2)$,…, $\Delta V_o(n+N)$, respectively, as shown in Fig. 4(a). And assuming that the initial voltage difference of the capacitor Cc is zero.

Now starting with the phase Φ2 in the 1st step, the OSSA amplifier in the Fig. 3(a) works as the traditional amplifier, as there is no voltage information on the Cc for iteration. Thus, the expression of the output can be acquired by replacing the V_o in the equation (8) with $V_o(n)$,

$$V_o(n) = \frac{2\Delta C}{C_i} V_R \left(\frac{1}{1+\sigma_d/A_0}\right) \tag{9}$$

During this period, for the schematic in Fig. 3(a), the voltage difference between A+ and A- (denoted by V_{A+A-} which equals to $\Delta V_{1/A}$) is $V_o(n)/A_0$, the voltage difference between B+ and B- (denoted by V_{B+B-}) is also $V_o(n)/A_0$, as shown in Fig. 4(b).

Then during the next phase Φ1 in the 1st step in the Fig. 4(b), the 1/A error produced by $V_o(n)$ is calibrated to zero. This is because the terminals A+ and A- (in the Fig. 3(a)) are shorted to the ground. Then the V_{A+A-} becomes $zero$ while the V_{B+B-} remains $V_o(n)/A$ due to the holding of the output level by the C_H (The exact value of the V_{B+B-} is slightly smaller than $V_o(n)/A_0$, this non-ideality will be explained later in Section IV). This means that the 1/A error produced by $V_o(n)$ is "absorbed" by the calibration capacitor Cc, which leads to the increasing of the voltage difference of the Cc (that is the dark space between the red line and the blue line), as shown in Fig. 4(b).

During the phase Φ2 in the 2nd step, the iteration takes place. As the "old" 1/A error in the 1st step produced by $V_o(n)$ is eliminated by the calibration capacitor Cc, so the "new" 1/A error in the 2nd step is produced by $\Delta V_o(n+1)$ rather than $V_o(n+1)$, that is,

$$\Delta V_{1/A}(n+1) = \frac{1}{A_0} V_o(n+1) - \frac{1}{A_0} V_o(n) = \frac{1}{A_0} \Delta V_o(n+1) \tag{10}$$

By combining the equation (10) with the equation (7), the output level of the 2nd step is,

$$V_o(n+1) = \frac{2\Delta C}{C_i} V_R - \frac{2C_0}{C_i} \frac{1}{A_0} \Delta V_o(n+1) \tag{11}$$

Similar to the equation (11), the output levels of the other steps are,

$$\begin{aligned} V_o(n+2) &= \frac{2\Delta C}{C_i} V_R - \frac{\sigma_d}{A_0} \Delta V_o(n+2) \\ &\vdots \\ V_o(n+N) &= \frac{2\Delta C}{C_i} V_R - \frac{\sigma_d}{A_0} \Delta V_o(n+N) \end{aligned} \tag{12}$$

where $\sigma_d = 2C_0/C_i$.

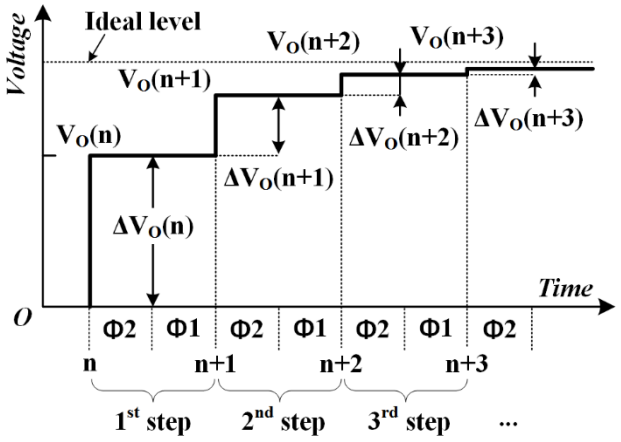
The relationship between two steps is

$$\Delta V_o(n+1) = V_o(n+1) - V_o(n) \tag{13}$$

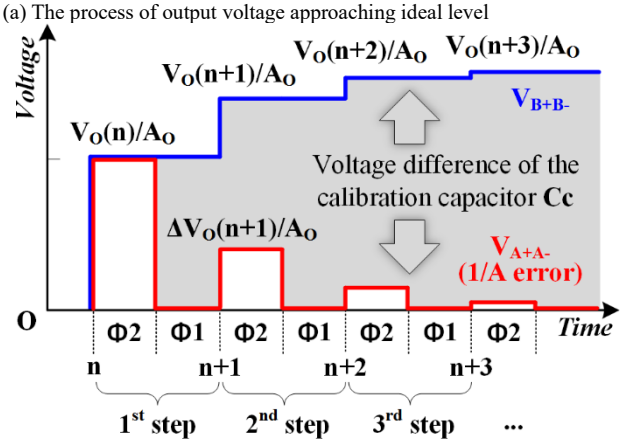
By combining the equations (9), (11), (12) and (13), the output in N-th step is,

$$\begin{aligned} V_o(n+N) &= \frac{2\Delta C}{C_i} V_R \left[1 - \left(\frac{1}{1+A_0/\sigma_d}\right)^{N+1}\right] \\ \sigma_d &= \frac{2C_0}{C_i} \end{aligned} \tag{14}$$

where C_0 is the value of the common mode capacitance of differential capacitive sensor, C_i is the value of integration capacitors, ΔC is the change value of differential capacitive sensor, V_R is the reference voltage acting as readout excitation, and σ_d is the deterioration factor.



(a) The process of output voltage approaching ideal level



(b) The process of the "1/A error" diminishing. The voltage difference between terminals A+ and A- is denoted by V_{A+A-} (red line), and the voltage difference between terminals B+ and B- is denoted by V_{B+B-} (blue line).

Fig. 4. The process of deteriorated output approaching ideal level and the 1/A error diminishing

An important conclusion can be drawn from the equation (14), that is, the limit of the OSSA output is the same as the expected ideal output, regardless of the gain A_0 and the deterioration factor σ_d , i.e.,

$$V_O(\infty) = \lim_{N\to\infty} V_o(n+N) = \frac{2\Delta C}{C_i} V_R \tag{15}$$

This means that, by introducing the OSSA technique, no matter how low the gain of amplifier is, and no matter how large the deterioration factor σ_d is, given enough steps, the output will always reach the near ideal level.

It is worth mentioning that the OSSA proposed here is a technique/method method, rather than a circuit. The T/H amplifier is one of various ways to implement and demonstrate this technique. Any other circuit/system with the kernel concept of the OSSA technique is able to benefit from the performance achieve by it.

IV. Non-Ideal Characteristic Considerations of Circuit Implementation

The non-ideal characteristics (finite gain, bandwidth, etc.) of fully differential amplifier, switches, holding path and integration path would affect the performance of the OSSA amplifier in convergence time (time used to reach the 90% of output) and accuracy. Impacts of the non-ideal characteristics mainly appear as

A. Holding error (when circuit switches from Φ2 to Φ1),

B. Recovery degradation (when circuit switches from Φ1 to Φ2),

C. Rise-edge degradation (during Φ2),

D. Increment degradation (during Φ2), and

E. Charge loss of the holding capacitor (when circuit switches from Φ2 to Φ1),

as shown in Fig. 5.

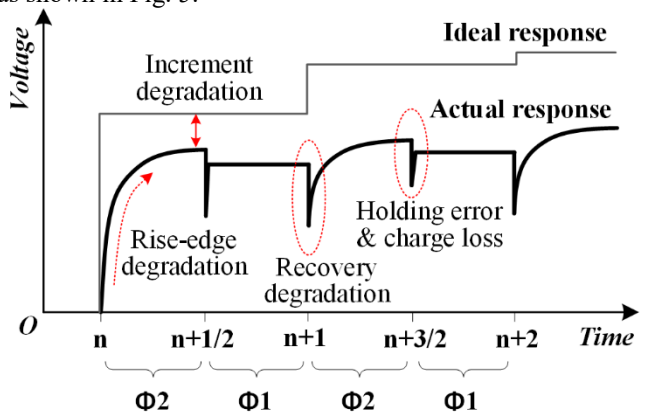


Fig. 5. Five phenomena caused by non-ideal characteristics

These problems are analyzed in detail and the optimized solutions are given in the following.

A. Holding error

Compared with the ideal response, there exists an unexpected decrement of output in holding phase, which is called "holding error". As shown in Fig. 6(a), during the sampling phase Φ2, the capacitor C_C is connected to the input terminals (B+ and B-) of the differential amplifier to provide a "virtue ground" in the terminals (A+ and A-) for conversion. So the node voltages of the capacitor Cc are,

$$\begin{aligned} V_A(n) &= \frac{1}{A_0}\Delta V_O(n) \\ V_B(n) &= \frac{1}{A_0} V_O(n) \end{aligned} \tag{16}$$

As shown in Fig. 6(b), when the holding phase Φ1 begins, the capacitor C_H is connected between the output terminal of differential amplifier and the input terminal (B+ and B-) of the differential amplifier to hold the output voltage. The capacitor C_C is connected to ground to get charged, in order to provide a more accurate "virtue ground" for next charge transfer to amplify signal. So the node voltages of the capacitor C_C are,

$$\begin{aligned} V_A\left(n+\frac{1}{2}\right) &= 0 \\ V_B\left(n+\frac{1}{2}\right) &= \frac{1}{A_0} V_O\left(n+\frac{1}{2}\right) \end{aligned} \tag{17}$$

By applying the charge conservation law from time "n" to "n+1/2", the charge transfer relationship is,

$$\begin{aligned} C_C\left(V_A(n) - V_B(n)\right) + C_H\left(V_O(n) - V_B(n)\right) = \\ C_C\left(V_A\left(n+\frac{1}{2}\right) - V_B\left(n+\frac{1}{2}\right)\right) \\ + C_H\left(V_O\left(n+\frac{1}{2}\right) - V_B\left(n+\frac{1}{2}\right)\right) \end{aligned} \tag{18}$$

Then by combining the equations (16)-(18), the final transfer function for output during holding phase Φ1 is

$$V_O\left(n+\frac{1}{2}\right)=\frac{C_H+\frac{C_C}{A_0}\left(1-\frac{\Delta V_{O-}(n)}{V_{O-}(n)}\right)}{C_H\left(1+\frac{1}{A_0}\right)+\frac{C_C}{A_0}}V_O(n) \quad (19)$$

The holding error V_{HE} is the voltage decrement at the time n+1/2,

$$V_{HE}(n)=V_O(n)-V_O\left(n+\frac{1}{2}\right) \quad (20)$$

The equation (20) shows that, when $C_H \ll C_C/A_0$,

$$V_{HE}(n)=\Delta V_O(n) \quad (21)$$

When $C_H \gg C_C/A_0$,

$$V_{HE}(n)=\frac{1}{A_0+1}V_O(n) \quad (22)$$

The result in the equation (19) suggests that, if the value of C_H is far less than value C_C/A_0, the charge loss will introduce holding error as large as the increment of output $\Delta V_O(n)$ during the sampling phase Φ1. This means that the holding path cannot accurately keep the stable output due to large holding error. As a result, the stable output of the OSSA amplifier is still at a deteriorated level as described by the equation (8).

The result in the equation (22) suggests that, when $C_H > C_C/A_0$, the charge loss only introduces a slight decrement of the stable output.

As the increment of the stable output from Φ2 to Φ1 is

$$\Delta V_o(n+1)=V_o(n+1)-V_o\left(n+\frac{1}{2}\right)$$
$$=V_o(n+1)-\frac{A_0}{A_0+1}V_O(n) \quad (23)$$

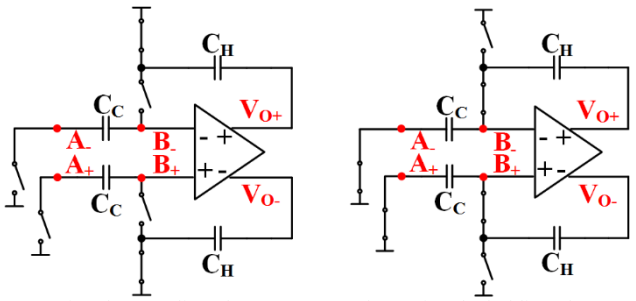
by combining the equation (23) with the equations (11) and (12), the general expression of level of the output in N-th OSSA step considering holding error in each OSSA step is,

$$V_o(n)=\frac{2\Delta C}{C_i}V_R\frac{1-\left(\frac{1}{1+A_0/\sigma_d}\frac{A_0}{1+A_0}\right)^{n+1}}{1+\frac{\sigma_d}{A_0(1+A_0)}} \quad (24)$$

The limit of the equation (24) is,

$$V_O(\infty)=\lim_{N\to\infty}V_o(n)=\frac{2\Delta C}{C_i}V_R\frac{1}{1+\frac{\sigma_d}{A_0(1+A_0)}} \quad (25)$$

It is therefore concluded that, in order to achieve the minimum holding error, the condition $C_H \gg C_C/A_0$ has to be met.



(a) During the sampling phase (b) During the holding phase

Fig. 6. The simplified equivalent circuit of operation process of holding path

B. *Recovery degradation*

At the beginning of Φ2, a decrement of output occurs when the OSSA amplifier recovers the output which is held during last holding phase Φ1. This is called "recovery degradation". Recovery degradation will increase convergence time of the OSSA amplifier and should be minimized. Recovery degradation is caused by the charge sharing between the holding capacitor and other differential load connected at the beginning of Φ2. So according to the charge conservation law, the degradation level ΔV_{RD} is,

$$\Delta V_{RD}(n)=\frac{C_i+C_2}{C_i+C_2+C_1+C_H}V_O(n) \quad (26)$$

where the capacitors C_1 and C_2 are common-mode feedback capacitors shown in Fig. 3(b), C_i is the integration capacitor and C_H is the holding capacitor. As the capacitor C_2 is relatively large in order to ensure the settling time of common-mode feedback loop, it contributes more to differential load.

According to the equation (26), the recovery degradation could be reduced by connecting the feedback capacitors C_2 to circuit during the holding phase Φ1 rather than during the sampling phase Φ2, as shown in Fig.6. Thus, the capacitor C_2 will not affect the recovery in any way. So the degradation level ΔV_{RD} which excludes C_2 becomes,

$$\Delta V_{RD}(n)=\frac{C_i}{C_i+C_1+C_H}V_O(n) \quad (27)$$

To further reduce the recovery degradation, the best way is to increase the value of holding capacitor C_H, since the capacitor C_1 would better be small so as not to affect the settling time of common-mode loop.

C. *Increment degradation*

The increment degradation refers to the lower stable level that the OSSA amplifier is able to reach in a single OSSA step, which increases the convergence time of OSSA amplifier. This phenomenon is caused by the attenuation of the fully differential amplifier's effective gain A_{eff}, which is due to the signal loss caused by the insertion of holding capacitor C_C between the sensor and the input stage of the fully differential amplifier. The effective gain A_{eff} is

$$A_{eff}=\frac{C_C}{C_{gs}+g_mR_{out}C_{gd}+C_C}g_mR_{out} \quad (28)$$

where C_{gs} is the gate-source parasitic capacitance of the fully differential amplifier's input transistors, C_{gd} is gate-drain parasitic capacitance of the fully differential amplifier's input transistors, which is amplified by Miller's effect, and g_m and R_{out} are the trans-conductance and output resistor of the fully differential amplifier, respectively. The equation (28) indicates that the value of the holding capacitor C_C should be as large as possible to achieve better performance. For example, in order to achieve 90% of original gain, the value of holding capacitor C_C should be 9 times as large as the value $\left(C_{gs}+g_mR_{out}C_{gd}\right)$.

D *Rise-edge degradation*

The long rise-time is caused by the decrease of -3dB bandwidth due to the holding capacitor C_H. To figure out how the -3dB bandwidth of OSSA amplifier is limited, the model to illustrate dominant pole formed by output terminal is shown in

Fig. 7, where ΔC is the differential capacitance of differential capacitive sensor which has been mentioned in the equation (1), C_C and C_H are the holding capacitors, C_i is the integration capacitor, C_{gd} and C_{gs} are parasitic capacitance of the fully differential amplifier's input transistors, and g_m and R_{out} are the fully differential amplifier's trans-conductance and output resistor, respectively.

As the impedance of ΔC is much higher than any other capacitance parallelly connected with it at node A, i.e.,

$$\frac{1}{s\Delta C} \gg \frac{1}{sC_C} + \frac{1}{s\left(C_{gs} + g_m R_{out} C_{gd}\right)} \tag{29}$$

The ΔC is negligible in the feedback signal path. As a result, the feedback transfer coefficient β formed by C_i, C_C, C_{gd} and C_{gs} is

$$\beta = \frac{C_C C_i}{C_C C_i + \left(C_{gs} + g_m R_{out} C_{gd}\right)(C_C + C_i) + 2C_0\left(C_C + C_{gs} + g_m R_{out} C_{gd}\right)} \tag{30}$$

The equivalent impedance Z_{equ} formed by the feedback loop is

$$Z_{equ} = \frac{1}{\beta g_m} \tag{31}$$

Then the dominant pole mainly formed by Z_{equ} and C_H is,

$$f_{-3dB} = \frac{1}{2\pi Z_{equ} C_H} \tag{32}$$

By combining the equation (30) with the equation (32), the final expression for -3dB bandwidth is,

$$f_{-3dB} = \frac{g_m}{2\pi C_H} \frac{1}{1 + \frac{C_{gs} + C_{gd}}{C_C}\left(1 + \frac{C_i}{C_C}\right) + \sigma_d\left(1 + \frac{C_{gs} + C_{gd}}{C_C}\right)} \tag{33}$$

Further, if the $C_C >> C_{gs}+C_{gd}$,

$$f_{-3dB} \approx \frac{g_m}{2\pi C_H} \frac{1}{1 + \sigma_d} \tag{34}$$

The first term of the equation (34) is known as unit gain bandwidth or GBW. The second term suggests that, the deteriorate factor is also a main factor affecting the -3dB bandwidth.

Though the factors affecting the -3dB bandwidth of the fully differential amplifier are uncovered, it is still very hard to improve the -3dB bandwidth. This is because all these factors are determinative to resist the other degradations. For example, C_H is set to resist holding error, C_i is set to resist recovery degradation, and the ratio of C_H and C_i is also set to minimize the holding error.

However, there exist other solutions. Overclocking is one of them, which improves the -3dB bandwidth of the OSSA amplifier without improving the -3dB bandwidth of the fully differential amplifier. But it comes with a modest sacrifice of final accuracy. This will be demonstrated in the next section.

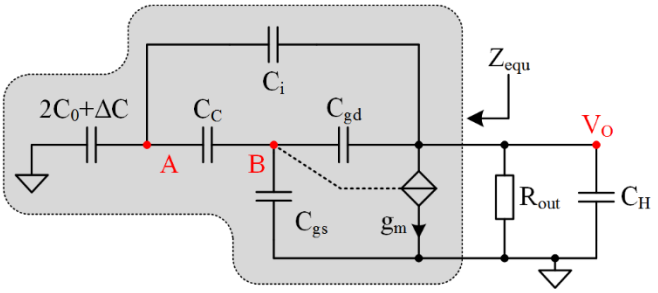


Fig. 7. The model of electrical characteristic of output terminal

E Charge injection form CMFB

The charge injection from capacitors C_1 and C_2 in CMFB network in Fig. 3(b) will cause the charge loss of the holding capacitor C_H, which as a result significantly causes additional holding error and decreases the final accuracy of the OSSA amplifier. At the beginning of the holding phase Φ1, the holding capacitors C_H is switched to the input terminal of the fully differential amplifier to form a stable negative feedback loop to hold the output voltage level. At the same time (beginning of Φ1), the CMFB capacitor C_2 is connected as a differential load. As the feedback loop needs several micro-seconds to reach stable state, during this period the charge of the capacitor C_H will be shared by C_2. As a result, the holding error will increase, and thus the output accuracy will decrease.

Applying charge conservation law, the extra holding error produced by charge injection is,

$$\Delta V_{HR}(n) = \frac{C_1 + C_H}{C_2 + C_1 + C_H} V_O(n) \tag{35}$$

where the capacitors C_1 and C_2 are common-mode feedback capacitors shown in Fig. 3(b), C_H is the holding capacitor. One of the simplest way to solve this problem is using the nesting clock (Φ3 and Φ4) to drive the switches of the CMFB network. In other words, the CMFB capacitors are connected after holding loop is settled and disconnected before the holding loop is disconnected, so as to prevent differential load C_2 sharing charge of the holding capacitor C_H. Apart from the CMFB network, any differential loads which are connected during the holding phase Φ1 also have to be driven by the nesting clock, in order to achieve higher accuracy.

In this section, a readout circuit for differential MEMS capacitive sensor based on the OSSA technique is proposed. There are 5 problems that will cause long convergent time (or low -3dB bandwidth) and low accuracy. These problems will deteriorate the output level in each of the OSSA steps, making the convergence time long. However, these problems are controllable by the methods described in this section.

V POST SIMULATION AND PHYSICAL VERIFICATION

The OSSA amplifier is prototyped in a readout circuit for differential capacitive accelerometer (MEMS sensor), as shown in Fig. 8. The conventional readout circuit includes the capacitance-to-voltage convertor (CVC), the sample & holding (S&H), the anti-alias filter (AAF) as front-end block, and Σ-Δ ADC as back-end block [11], [12]. In our new design, the OSSA amplifier replaces the CVC, S&H and AAF and serves as front-end block. This is because the OSSA amplifier is able

to act as CVC during the sampling phase Φ2 and act as S&H during the holding phase Φ1. The OSSA amplifier has a much higher -3dB bandwidth and driving ability during Φ1 than it does during Φ2 as there is no increment degradation during Φ1. This makes the OSSA amplifier perform S&H function during Φ1. Besides, by synchronizing the operational frequency of the OSSA amplifier with the operational frequency of the Σ-Δ ADC, the high frequency noise produced by switches in the OSSA amplifier is avoided by dedicated timing control. Hence, AAF is no longer needed. Conventionally, both S&H and AAF need fully differential difference operational amplifiers (FDDA) to build, which typically consumes twice the power and chip area of a single fully differential amplifier. As the OSSA amplifier does not require a separate AAF, it consumes much less power and chip area.

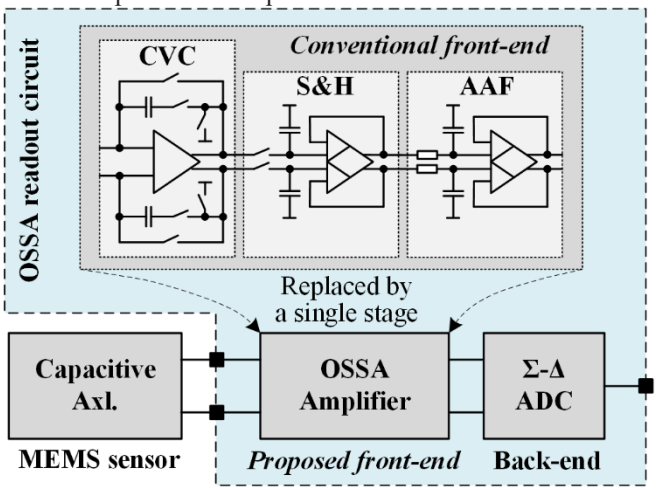


Fig. 8. The block diagram of the OSSA readout circuit

The proposed circuit is simulated using SPECTRE based on Dongbu Hiteck 0.18um 1.8V BCD process parameters. The results verify the theoretical analysis in the sections III and IV.

A Parameter analysis by simulation

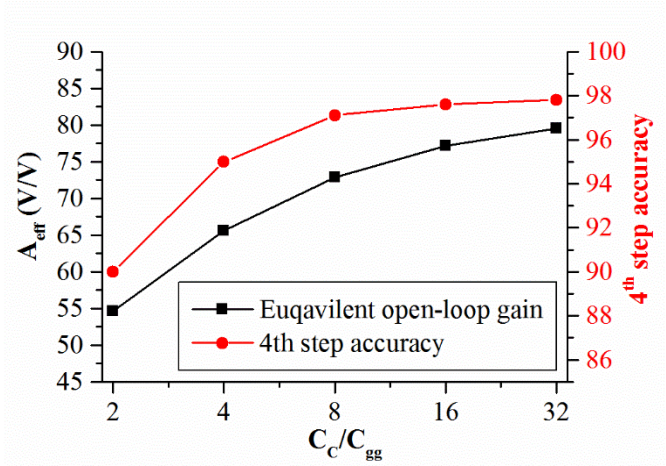
The main parameters simulated are listed in the table I. The $6*C_{ELE}$ means that C_H has 6 basic capacitors C_{ELE} connected in parallel, with each basic capacitor's value being 178fF. The test range 1-96 of C_H means that the number of capacitors connected in parallel varies from 1 to 96. Important variables such as frequency and holding capacitors are analyzed in certain range, in order to verify the considerations (solutions to non-ideal characteristics) described in the section IV. The typical values of the variables are also listed in the table.

TABLE I: THE VALUE OF MAIN PARAMETERS OF TESTED OSSA AMPLIFIER

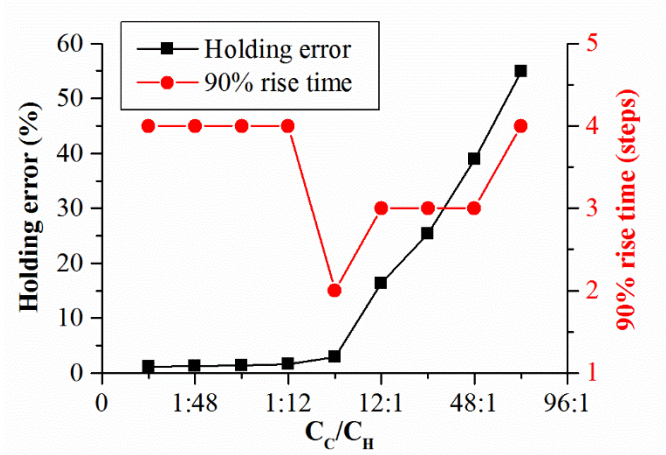
Symbol	Variable	Typical Value	Analysis range
σ_d	Deterioration factor	42	5.5-88
A_0	Gain(open loop)	82.5 (38dB)	-
$S_{\Delta C}$	Sensitivity	20mV/Ff	-
gm	Trans-conductance	289us	-
f_C	Operational frequency	1MHz	500kHz-5MHz
Ci	Integration capacitor	90fF	-
ΔC	Differential capacitance	10fF	10aF-100fF
C_H	Holding capacitor	$6*_{CELE}$	$1\text{-}96*C_{ELE}$
C_C		$12*_{CELE}$	$1\text{-}96*C_{ELE}$
C1	CMFB capacitor	90fF	-
C2		270fF	-
V_R	Reference voltage	0.9V	-

According to the equations (21)-(23), the holding error obviously increases with the increase of the C_C/C_H, which results in a low convergence speed. The results in Fig. 9. (a) suggest that in order to maximize convergence speed, the ratio of C_C/C_H would be around 12:12, where it takes the least time (only 2 steps) to reach 90% of the output.

According to the equation (28), the choice of absolute value of C_C is considered with the increment degradation. As shown in Fig. 9. (b), to achieve good accuracy, C_C/C_{gg} is at least 8. As the parasitic capacitance C_{gg} is about 250fF, the capacitance of C_C is set to be 2pF.



(a) The convergence speed change with ratio C_C/C_H



; (b) The accuracy varying with the ratio of C_C/C_{gg}

Fig. 9. The convergence speed and accuracy of OSSA amplifier varying with capacitances

The recovery degradation varies significantly with the ratio of C_H and C_i, according to the equation (27). However, compared to increment degradation and holding error, it has much less influence on the accuracy. So its numerical results is not shown here for simplicity.

The analytic model in Fig. 7 provides an accurate prediction of -3dB bandwidth of the OSSA amplifier during Φ2, as shown in Fig. 10. According to the analytic model, to expand the -3dB bandwidth, large g_m and small C_H are required. In this case, the value of C_H is set to be $6*C_{ELE}$ (or 1pF) in order to set -3dB bandwidth of the OSSA no less than 1MHz (the operational frequency determined by over sampling ratio [11]).

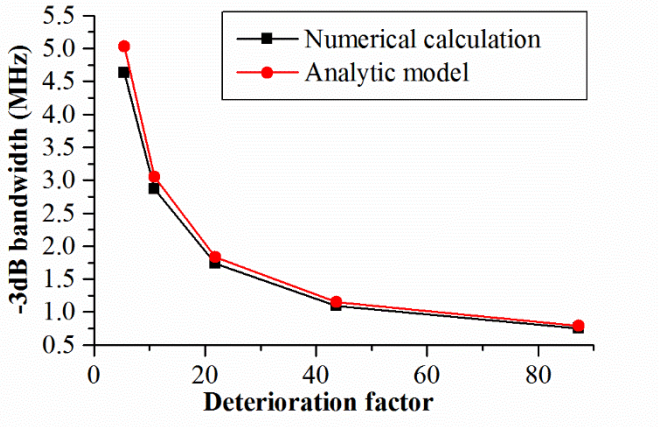
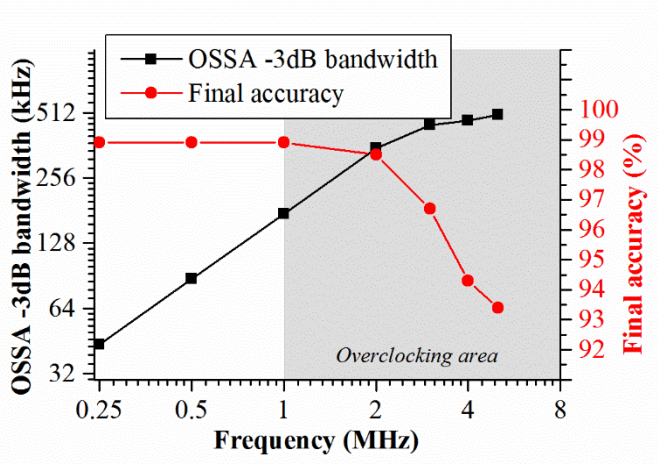


Fig. 10. The result of -3dB bandwidth of OSSA amplifier during Φ2 from analytic model (by Fig. 7.) and numerical simulation (by Spectre Periodic Steady State Analysis and Periodic Transfer Function Analysis)

Over-clocking will further improve the -3dB bandwidth of the OSSA amplifier without improving the -3dB bandwidth of the fully differential amplifier A1 used by the OSSA amplifier, but with an acceptable sacrifice of final accuracy. The -3dB bandwidth of the fully differential amplifier A1 is constant 1MHz, while the -3dB bandwidth of the OSSA amplifier can increase with the rising of the clock frequency. Even though the clock frequency rises beyond the -3dB bandwidth (1MHz) of the fully differential amplifier A1 (i.e., the A1 is overclocked), the -3dB bandwidth of the OSSA amplifier still keep rising, but with increasing sacrifice of the accuracy. Meanwhile, the linearity of the OSSA amplifier does not decrease, as shown in Fig. 11.



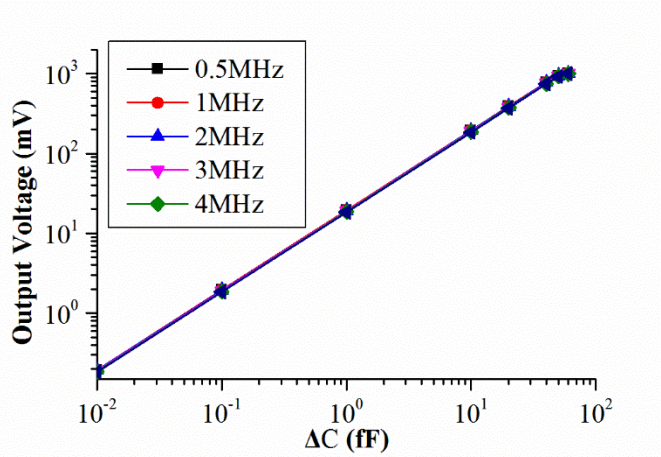


Fig. 11. The accuracy and linearity of OSSA amplifier varying with the overclocking frequency

B Improvement and verification

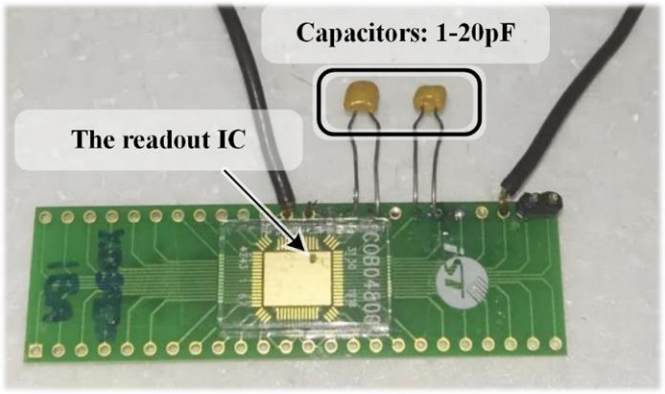
To verify the improvements, both the OSSA readout circuit and the traditional readout circuit [11] are fabricated using the same process. Through the measurement of both circuits, three significant improvements have been observed.

The first is significant improvement of the ability to resist common-mode parasitic capacitance. Similar to the concept of Common-Mode Rejection Ratio (CMRR) [17], which is used to quantify the ability of the differential amplifier to reject common-mode interference, the Parasitic Capacitance Rejection Ratio (PCRR) is defined to quantify the ability of the differential capacitance readout circuit to reject common-mode parasitic capacitance [18], [19], [20], i.e.,

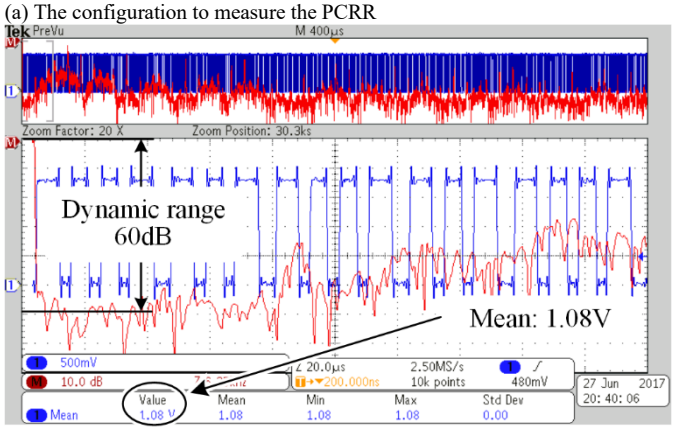
$$PCRR = 20\log\left(\frac{S_{par}}{S_{\Delta C}}\right) \tag{36}$$

where S_{par} is the sensitivity to variations of parasitic capacitance, $S_{\Delta C}$ is the sensitivity to variations of differential capacitance. In this work, the Spar is 40mV/20pF, and the $S_{\Delta C}$ is 20mV/fF. So according to the equation (36), the PCRR of the OSSA readout circuit is -80dB. The PCRR of the traditional readout circuit using the same calculation process is -56.2dB. The PCRR is improved by 23.8dB.

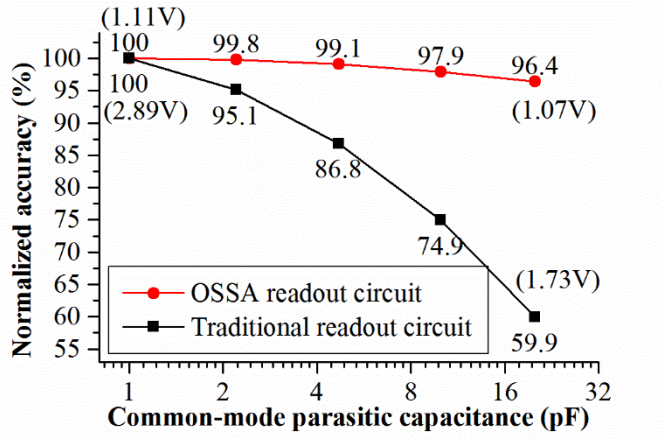
The S_{par} is measured as shown in Fig. 12 (a). The discrete capacitor is used to simulate the parasitic capacitance. When the value of the discrete capacitor changes from 1pF to 20pF, the output changes by 40mV from 1.11V to 1.07V, as shown in Fig. 12 (b) and (c). The transient responses with a parasitic capacitor of 10pF are shown in Fig. 12(b). The mean level is 1.08V and the dynamic range is 60dB (0-10kHz), so the noise floor is 1.08mV. As the sensitivity is 20mV/fF, so the capacitance resolution is 54aF, according to the calculation method in reference [11].



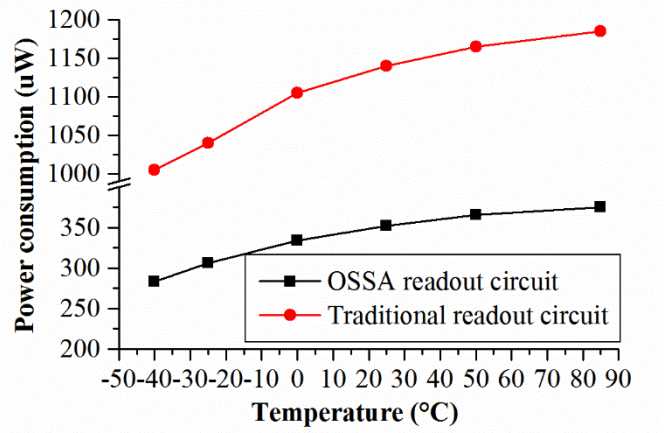
(a) The configuration to measure the PCRR



(b) The transient output waveform and spectrum



(c) The comparison of resistance on deterioration factor

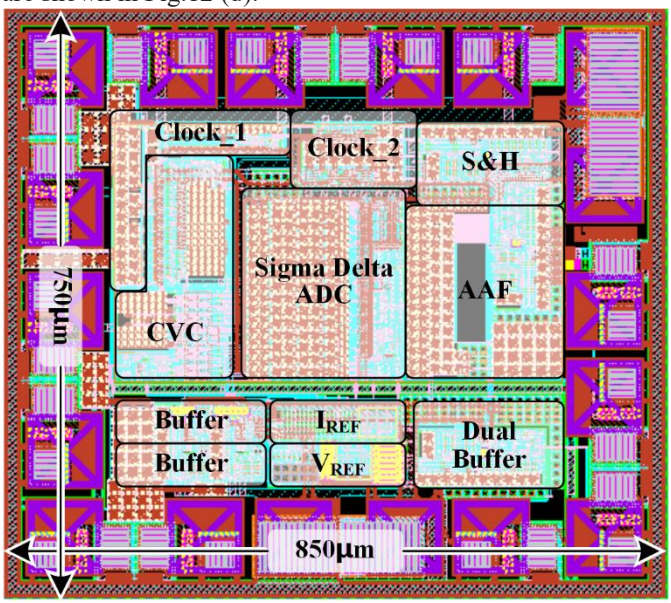


(d) The comparison of power consumption

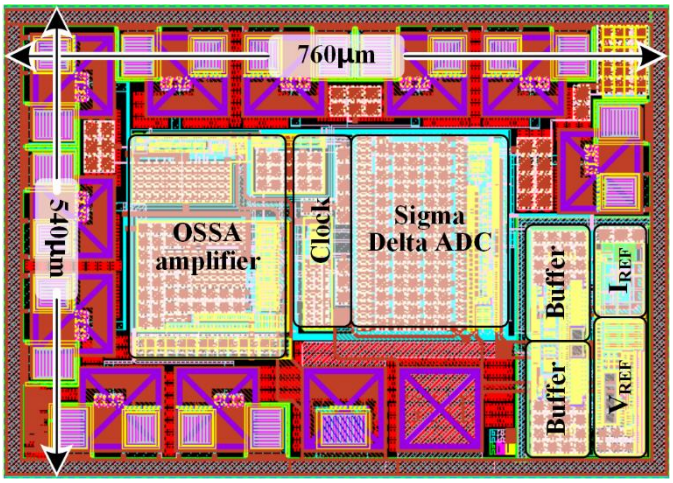
Fig. 12. The measurement results of the OSSA readout circuit and traditional CDS readout circuit

The second improvement is die size reduction. After employing the OSSA technique, the readout circuit shows a significant reduction of die size. The layout of traditional readout circuit is shown in Fig. 13(a), which is mainly composed of capacitance-to-voltage convertor (CVC), two clock generators (100 kHz and 1 MHz), sampling and holding module (S&H), anti-alias filter (AAF) and Σ-Δ ADC. The buffer and reference are placed at the bottom of the layout, which are powered by independent voltage supply, and they are isolated by guard ring for noise suppression. The circuits consumes 0.63 mm^2 die area (with 0.31 mm^2 core area) in total. The structure employing the OSSA amplifier shown in Fig. 13(b) consumes 0.41 mm^2 die area (with 0.15 mm^2 core area) using the same process. It is clear that die area has been reduced by more than 35%, and the core area (the area of circuit which does not include area of pads and ESD) has been reduced by more than 50%. The photographs of the traditional readout circuit and the OSSA readout circuit are shown in Fig. 13(c) and Fig. 13(d), respectively.

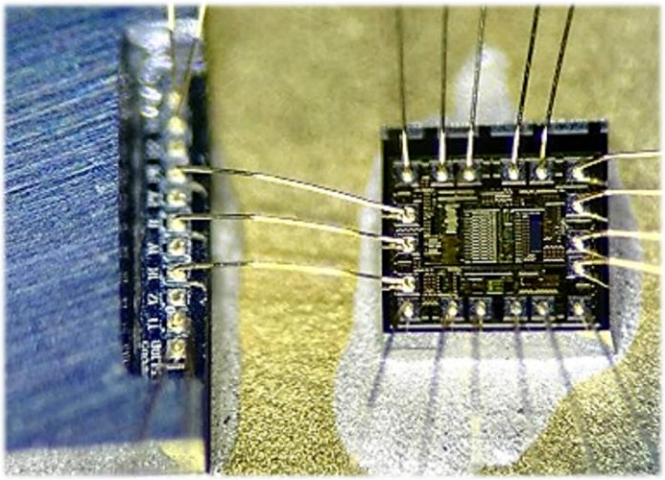
The third improvement is power consumption. As mentioned earlier, the OSSA amplifier is able to serve as high accuracy CVC and active S&H at the same time. This significantly reduces the power consumption, because there is no need for a separate S&H which requires two operational amplifiers (dual buffer) or a fully differential difference amplifier (FDDA) to build. As a result, the total power dissipation of the traditional readout circuit is 1140uW typically, while the OSSA amplifier consumes 350uW typically (27°C). So the power consumption is reduced by over 69.3% typically. The measurement results are shown in Fig.12 (d).



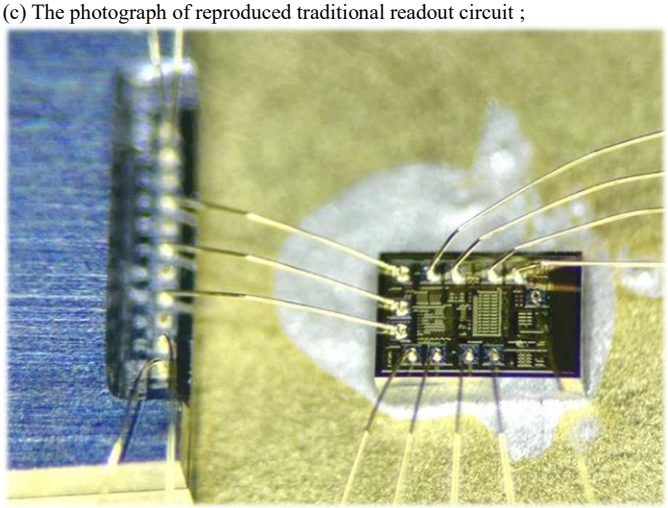
(a) The layout of reproduced traditional readout circuit;



(b) The layout of the OSSA readout circuit;



(c) The photograph of reproduced traditional readout circuit ;



(d) The photograph of the OSSA readout circuit

Fig. 13. The layout and photograph of traditional and proposed readout circuit

Table II compares the measured parameters of the IC with those of other work. It is clear that the power consumption and chip area of this work have been significantly reduced compared with the refabricated work [11]. This is because the OSSA readout circuit has avoided employing FDDA. The references [18] and [19] have less power consumption than this work, and [19] has smaller chip area than this work, but their resolution (the minimum capacitance the IC can detect) is much worse. This is because the resolution of this work benefits from CDS function which is not available to the references [18] and [19] due to their circuit structures. The CDS function greatly reduces the flicker noise, thus the signal to noise ratio has been improved and the resolution has also been improved. The sensitivity of this work varies with different integration capacitor C_i. In this implementation, in order to achieve high application flexibility, 4 sensitivity values have been obtained with only the typical value being shown in the table II. The sensitivity of this work is better than the reference [11], however it is not comparable to the others in the table as they use different parameters to measure their sensitivities. Compared to some recent work focusing on rejecting the effect of common-mode parasitic capacitance [18]-[20], which use various techniques (such as PWM modulation and current-mode amplifier) and different fabrication processes, this work has achieved the best PRCC (-80dB). This is due to use of the OSSA technique. This means that this work outperforms other work in rejecting large common-mode parasitic capacitance.

To provide a complete set of data, the typical parameters of the sensor is summarized in the table III. The device size and the capacitive gap are 0.7mm×0.7mm and 2um, respectively, which are measured by a microscope. The thickness of the device are 15um which is acquired from the design company's official process data. The proof mass is 3.34ug, which is calculated from the measured dimension of the device. The rest capacitance is 905fF, which is the sensor's capacitance (C_{S1}) without any acceleration applied on it. The sensitivity is 13fF/g which is measured by a semiconductor device parameter analyzer.

TABLE II: MEASURED SPECIFICATIONS OF THE READOUT IC

This work	[11]	[18]	[19]	[11] (reproduced)	This work
Power(mW)	6.0	0.08	0.22	1.14	0.35
Area(mm^2)	2.0	0.52	0.03	0.31	0.15
Sensitivity	2.5 mV/fF	32 ns/fF	5 nA/fF	14.1 mV/fF	20 mV/fF
Resolution (aF)	22	800	800	48	54
PCRR(dB)	N/A	-68.6	-44.2	-56.2	-80
Supply voltage (V)	2.5	3.0	2.5	5.0	1.8
Process(nm)	250	320	65	180	180

TABLE III: MEASURED SPECIFICATIONS OF THE SENSORS

Device size	0.7mm×0.7mm×15um (X&Y axis)
Capacitive gap	2um
Proof mass	3.34ug
Rest capacitance	905fF
Sensitivity	12 fF/g

VI. CONCLUSIONS

This paper proposes a new technique the OSSA to be used in the readout circuit for MEMS capacitive sensor applications. The OSSA addresses the 1/A error deterioration problem which occurs in the traditional fully differential switched-capacitor CDS readout circuit due to the large common-mode parasitic capacitance introduced by MEMS manufacturing and packaging process, therefore affecting significantly the accuracy of the readout circuit output. The circuit analysis and

the experimental results obtained demonstrate that the readout circuit using the OSSA outperformances other comparable readout circuits in terms of PCRR, IC die area and power consumption. Compared to the traditional readout circuit fabricated using the same IC process and other recent work [18] [19] that also aim to reduce the effect of parasitic capacitance, the OSSA based readout circuit improves the PCRR by at least 23.8dB. Moreover, the readout IC with the OSSA achieves a 50% reduction of die area and a 69.3% reduction in power consumption compared to the traditional readout IC fabricated using the identical semiconductor process.

REFERENCE

[1] Lemkin, Mark, and B. E. Boser, "Three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics," *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 456-468, Apr. 1999.

[2] Wang, Yan Mei, et al., "A Low-Power Highly Sensitive Capacitive Accelerometer IC Using Auto-Zero Time-Multiplexed Differential Technique," *IEEE Sensors J.*, vol. 15, no.11, pp. 6179-6191, Nov. 2015.

[3] F. Ayazi, K. Najafi, "A HARPSS polysilicon vibrating ring gyroscope," *J. Microelectromech. Syst*, vol. 10, no. 2, pp. 169–179, 2001.

[4] R.E. Oosterbroek, T.S.J. Lammerink, et al., "A micromachined pressure/flow-sensor," *Sensors Actuators A: Phys.*, vol. 77, no. 3, pp. 167–177, Nov. 1999.

[5] Mailly F, Giani A, Martinez A, et al. "Micromachined thermal accelerometer," *Sensors Actuators A: Phys.*, vol. 103, no. 3, pp. 359-363, Feb. 2003.

[6] Amarasinghe, Ranjith, et al., "Development of miniaturized 6-axis accelerometer utilizing piezoresistive sensing elements," *Sensors Actuators A: Phys.,* vol. 134, no. 2, pp. 310-320, Mar. 2007.

[7] Vopilkin, E. A, et al., "MEMS Tunneling Sensor without the Feedback Loop." *IEEE Sensors J.*, vol. 14, no. 6, pp. 1831-1835, Jun. 2014.

[8] Brookhuis, R. A., T. S. J. Lammerink, and R. J. Wiegerink, "Differential capacitive sensing circuit for a multi-electrode capacitive force sensor," *Sensors Actuators A: Phys.*, vol. 234, pp. 168-179, Oct. 2015.

[9] Rodrigues, Shalini, N. Munichandraiah, and A. K. Shukla, "A review of state-of-charge indication of batteries by means of a.c. impedance measurements," *J. Power Sources*. vol. 87, no. 1–2, pp:12-20, Apr. 2000.

[10] Amini S, Johns D A, "A Flexible Charge-Balanced Ratiometric Open-Loop Readout System for Capacitive Inertial Sensors," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 4, pp. 317-321, Apr. 2015.

[11] Amini B V, Ayazi F, "A 2.5-V 14-bit ΣΔ CMOS SOI capacitive accelerometer," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2467-2476, Dec. 2004.

[12] Song, H., et al., "Fully integrated low-noise readout circuit with automatic offset cancellation loop for capacitive micro-sensors," *Sensors*, vol. 15, no. 10, pp. 26009-26017, Oct. 2015.

[13] Shiah, Jack, and S. Mirabbasi, "A 5-V 290-uW, low-noise chopper-stabilized capacitive-sensor readout circuit in 0.8um CMOS using a correlated-level-shifting technique," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 4, pp. 254-258, Apr. 2014.

[14] Yoshizawa, Hirokazu, and G. C. Temes, "Switched-capacitor track-and-hold amplifier with low sensitivity to op-amp imperfections," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 1, pp. 267-270, Jan. 2007.

[15] Yoshizawa, H, T. Yabe, and G. C. Temes, "High-precision switched-capacitor integrator using low-gain opamp," *Electron. Lett.,* vol. 47, no. 5, pp. 315-316, Mar. 2011.

[16] Perruisseau-Carrier, Julien, et al., "Electrical Modeling and Design of a Wafer-Level Package for MEM Resonators," *IEEE Trans. Adv. Packag.,* vol. 33, no.2, pp. 534-542, May 2010.

[17] Razavi B, "Design of analog CMOS integrated circuits," New York, NY, USA: McGraw-Hill, 2001, pp. 100-130.

[18] Nizza N, Dei M, Butti F, et al., "A Low-Power Interface for Capacitive Sensors with PWM Output and Intrinsic Low Pass Characteristic," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 60, no. 6, pp. 1419-1431, Jun. 2013.

[19] Scotti G, Pennisi S, Monsurrò P, et al., "88 uA 1-MHz Stray-Insensitive CMOS Current-Mode Interface IC for Differential Capacitive Sensors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 7, pp. 1905-1916, Jul. 2014.

[20] Cesta S D, Intaschi L, Bruschi P, et al., "A chopper stabilized, low power capacitance to PWM converter for sensor interfacing," *IEEE 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 1-4, Jun. 2016.

[21] Tony Chan Carusone, David Johns, Kenneth Martin. "Analog Integrated Circuit Design", 2nd ed.. USA: John Wiley & Sons, Inc., 2012, pp. 557-605.

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