Differential Capacitive Readout Circuit using Oversampling Successive Approximation Technique

Longjie Zhong, *Student Member, IEEE,* Xinquan Lai, *Member, IEEE,* Hongjiang Song, Donglai Xu, *Senior Member, IEEE*

***Abstract*—This paper designs a close loop Σ-Δ readout circuit for differential MEMS accelerometer. A technique named oversampling successive approximation (OSA) is employed to build basic amplifiers and integrators. This technique can largely reduce the gain error and thus low gain amplifier such as single stage amplifier is allowed to be used. As a result, the power consumption and chip area are reduced. However, the OSA based amplifiers and integrators are vulnerable to the interference caused by charge injection and leakage current from the specific MOSFET switches. This drawback is analyzed in detail and the interference suppressing solutions are given. The OSA based readout circuit is fabricated in a commercial 0.18um BCD process. The measurement results show that the interference is reduced by 20dB in the circuit with interference suppressing solutions compared to the circuit without interference suppressing solutions. And the noise floor is 24ug/rtHz. The readout circuit achieves a 0.07% gain error with a low power consumption of 0.5mW and 9MHz sampling rate.**

***Index Terms*—Accelerometer, closed-loop, compact size, low power, micro-electromechanical systems (MEMS), noise floor, sensor**

I. Introduction

Low power consumption and low supply voltage is one of the most important trends of nowadays MEMS (Micro-electromechanical Systems) differential capacitive sensors, especially in IoT (Internet of things) applications such as wearable devices and implanted bio-sensors [1]. However, reducing the power consumption means reducing the gain or bandwidth of the amplifier in the readout circuit. The low gain amplifier suffers from the "gain error" which significantly decreases the measurement accuracy. What's more, the popular packaging technique System in Package (SiP) for the MEMS device adds more challenges to improving the accuracy of the readout circuit. This is because the SiP technique uses a large amount of pads and bonding wires to integrate the separate MEMS sensor and CMOS readout circuit, which introduce large common-mode parasitic capacitance [2-6], [10], [11]. Common-mode parasitic capacitance can further increase the gain error of the front-end switched-capacitor capacitance-to-voltage convertor (SC-CVC). The principle how the accuracy of the SC-CVC is decreased by the parasitic capacitance is simply explained as follows and shown in Fig. 1.

To make the analyzing process simple and clear, the "1/A error" is used to derive formulas in this paper, which is defined as the voltage difference V_{A+A-} across the input terminals of the amplifier (A+ and A- in Fig. 1). Fig. 1 shows the traditional SC-CVC employing the Correlated Double Sampling operation (CDS) [4-6], [8], [9]. The 1/A error is in proportion to the level of the outputs, and it is denoted by the symbol $\Delta V_{1/A}$

$$\Delta V_{1/A}(n) = V_{A+}(n) - V_{A-}(n) = \frac{V_o(n)}{A_0} \tag{1}$$

where A_0 is the open-loop gain of the amplifier, V_O is the output voltage of the amplifier. Notice that the 1/A error is different from the concept of "gain error" (defined as the fractional error between the desired gain and the actual gain [17]). By applying the charge-conservation law to the differential charge, the relationship between the output $V_o(n)$ and the 1/A error $\Delta V_{1/A}(n)$ is acquired,

$$C_i\big(V_o(n) + \Delta V_{1/A}(n)\big) - \frac{1}{2}C_{s1}\Delta V_{1/A}(n) + \frac{1}{2}C_{s2}\Delta V_{1/A}(n) + C_{P0}\,\Delta V_{1/A}(n) = C_{s1}\,V_R(n-1) - C_{s2}\,V_R(n-1) \tag{2}$$

where $V_O(n)$ is the voltage difference between the output terminals V_{O+} and V_{O-}, C_{S1} and C_{S2} are the sensor capacitor, C_i and C_{P0} are the integration capacitor and the parasitic capacitance, respectively, $V_R(n) = V_R$ is the DC reference voltage. Then the output voltage can be acquired from (2),

$$V_o(n) = \frac{C_{S1}-C_{S2}}{C_i}V_R - \frac{C_{P0}+C_{S1}-C_{S2}-C_i}{C_i}\Delta V_{1/A}(n) \tag{3}$$

where the 1st term of the $V_O(n)$ is the ideal response and the 2nd term is the error. The 2nd term of (3) means that the 1/A error converts part of the common-mode charge produced by C_{P0} to error voltage in the differential output voltage. This error voltage increases with the increasing of the common-mode parasitic capacitance C_{P0}. The deterioration factor σ_d is defined as,

$$\sigma_d = \frac{C_{P0} + C_{S1} - C_{S2} - C_i}{C_i} \tag{4}$$

Then apply (1) and (4) to (3), the final expression of the output of SC-CVC is,

$$V_o = \frac{C_{S1} - C_{S2}}{C_i}V_R\left(\frac{1}{1 + \sigma_d/A_0}\right) \tag{5}$$

where σ_d is the deterioration factor. An important conclusion from (5) is that the error has deteriorated by a coefficient σ_d, which is mainly due to the common-mode parasitic capacitance C_{P0}. Note that the offset voltage of the amplifier does not appear in the derivation, because it is cancelled by the CDS operation [12].

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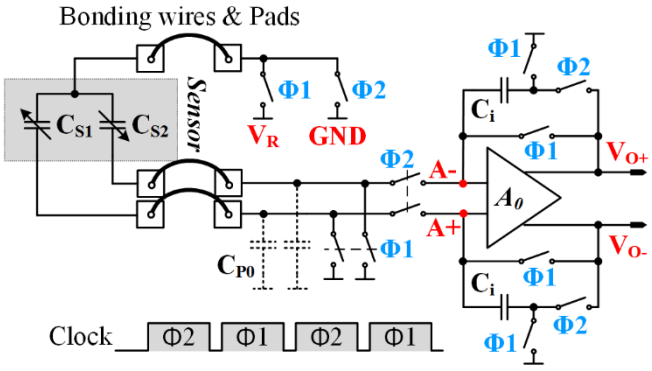
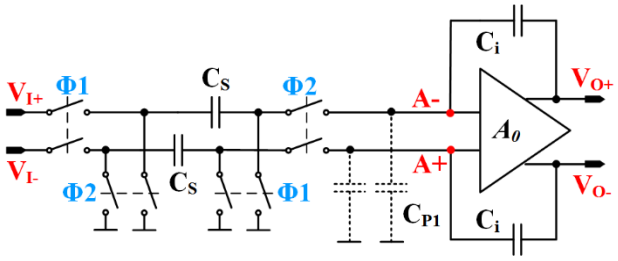
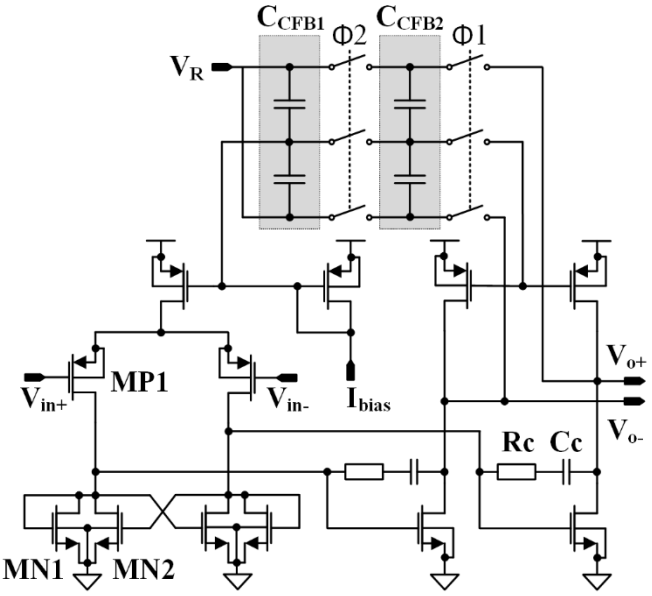


(a) The structure of the traditional SC-CVC with the parasitic capacitance C_{P0}



(b) The structure of the traditional integrator with the parasitic capacitance C_{P1}



(c) The two-stage amplifier used in the traditional SC-CVC and the traditional integrator

Fig. 1 Traditional SC-CVC and integrator

The typical value of the C_{P0} is 2.5 pF (1.0pF for ESD protection in IC die, 0.5pF for the pad in the IC die and 1.0pF for the parasitic capacitance between the proof mass and the substrate in the MEMS die in this work), while the typical value of the C_i is 50fF. This is because the capacitance difference $C_{S1} - C_{S2}$ is in the order of several femto-farad, and the value of C_i has to be small to guarantee the gain of the SC-CVC according to (5). As a result, the value of the σ_d is 50. If the amplifier's gain A_0 is 50dB, the fractional error of the output will be 14%, which is a serious decreasing on the gain accuracy. The fractional error with different deterioration factors is shown in Fig. 2.

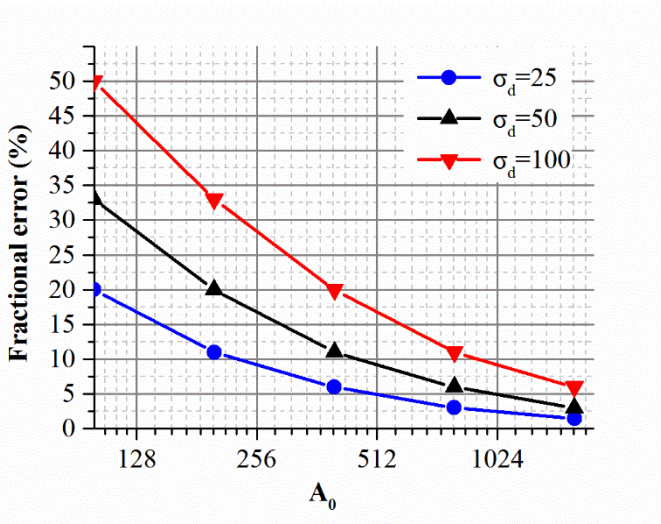


Fig. 2. Fractional error of the output voltage of traditional SC-CVC with different deterioration factor σ_d and amplifier's gain A_0

The 1/A error not only decreases the accuracy of the SC-CVC, but also affects the pole of an integrator. As shown in Fig. 1 (b), applying the charge conservation law in the nodes A+ and A-, the relationship between the input voltage and output voltage of the integrator considering the 1/A error is

$$C_i\big(V_O(n) - V_O(n-1)\big) = C_S\big(V_I(n-1) - \Delta V_{1/A}(n)\big) - C_{P1}\Delta V_{1/A}(n) \quad (6)$$

where $\Delta V_{1/A}(k) = V_O(k)/A_0$. The Z-transform of (6) is

$$V_O(z) = \frac{z^{-1}}{1 + \frac{C_S + C_{P1}}{A_0 C_i} - z^{-1}} \frac{C_i}{C_S} V_I \quad (7)$$

where the C_{P1} is the parasitic capacitance of the input transistors of the amplifier A_0. Equation (7) suggests that the pole of the integrator is the function of the DC gain A_0 of the amplifier and the parasitic acceptance C_{P1}, which makes the pole undetermined [18]. The undetermined pole will put the closed-loop system in the risk of instability, as the integrator is used as the compensator in the closed-loop system.

In order to solve the problems of reduced gain accuracy in the SC-CVC and the undetermined pole in the integrator, (5) and (7) suggest that the amplifier with high gain A_0 is essential. Thus one general solution is to directly improve the gain of the amplifier by using structures such as two-stage amplifier (Fig.1 (c)) [17], [24], fold/double cascode [6], [10] and gain-boosted structure [9], [20], [23]. However, these amplifiers will increase the power consumption and supply voltage significantly, which is contradictory to the requirement of the low power consumption and low supply voltage mentioned in the 1st paragraph of this section.

Another solution is to remove the 1/A error by switched-capacitor networks, so that the equivalent high gain can be achieved without improving the gain of the amplifier, which is very suitable for low voltage and low power applications. The reference [12], [18], [19] and this work adopt this method. The reference [18] employs a digital programmable calibration capacitor to compensate the error charge caused by the finite gain. However, the accuracy of this method is limited by the minimum calibration step of the digital calibration capacitor. The OSA (Oversampling Successive Approximation) technique is an analog calibration method and the calibration

step is continuous [5]. Thus the calibration accuracy is theoretically infinite high. Both the references [12] and [19] employ the basic principle of CDS to reduce the error from $1/A_0$ to $(1/A_0)^2$, while the OSA based circuit can do the CDS operation by N times in an iteration form so that the error can be reduced by N order from $1/A_0$ to $(1/A_0)^N$. So the OSA technique is based on CDS but improves over CDS.

However, the OSA technique has its drawback that the OSA based amplifiers and integrators are easy to be interfered by the charge injection and leakage current from specific switches. These interferences significantly decrease the gain accuracy and the noise performance of the OSA based circuits. This phenomena are analyzed in detail in this paper and solutions are given.

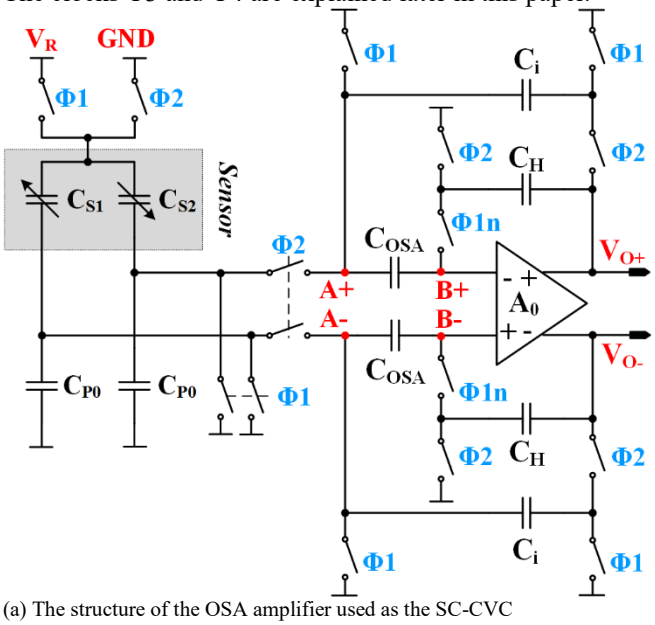
The rest of the paper is organized as follows. In section II, the principle, the drawback and the performance of the OSA technique are illustrated in detail. In section III, the circuit implementation of the closed-loop readout circuit based on the OSA technique is shown. In section IV, the physical verification and measurement results are presented. The conclusions are then drawn in section V.

II. THE OSA TECHNIQUE BASED CIRCUIT

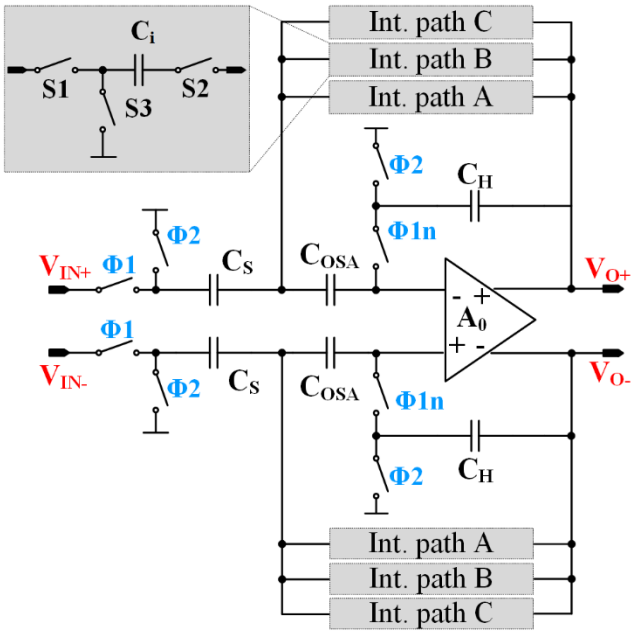
In this section, the principle of the OSA based operational circuits (the OSA amplifier and the OSA integrator) is explained. The drawbacks of the OSA based operational circuits are analyzed and the corresponding solutions are given. Furthermore, the power consumption and noise performance are also analyzed.

A. The principle of the OSA technique

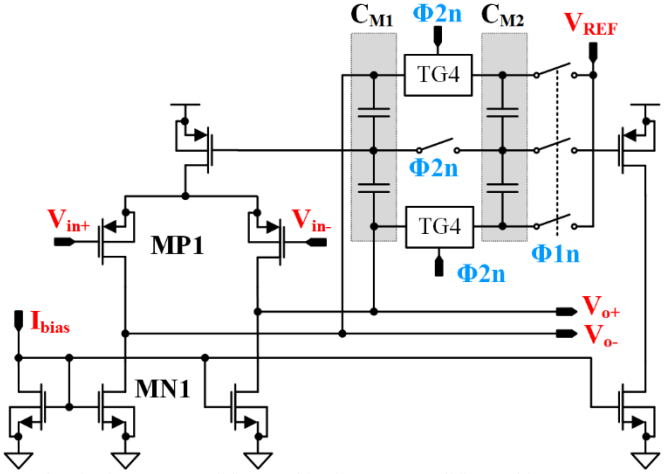
The OSA amplifier, the OSA integrator and the amplifier which is used by the OSA amplifier and the OSA integrator are shown in Fig. 3(a), Fig. 3(b) and Fig. 3(c), respectively. They are driven by the clocks Φ1, Φ1n, Φ2 and Φ2n shown in Fig. 4. The clocks Φ3 and Φ4 are explained later in this paper.



(a) The structure of the OSA amplifier used as the SC-CVC

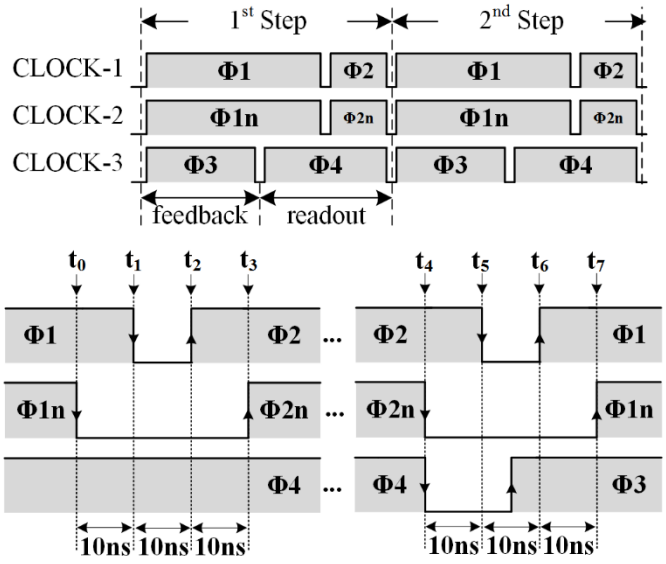


(b) The structure of the OSA integrator

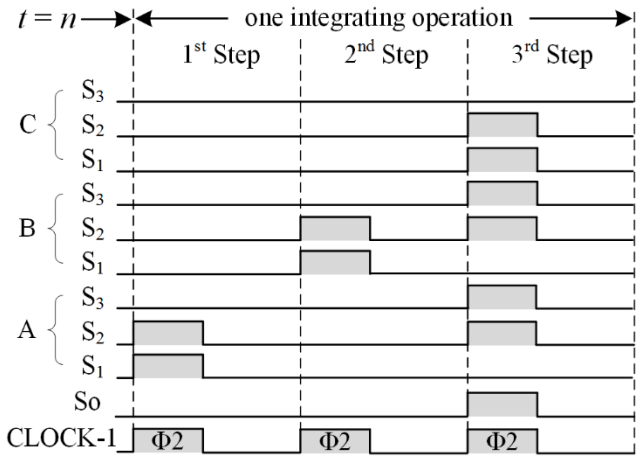


(c) The single-stage amplifier used in the OSA amplifier and integrator

Fig. 3. The schematics of the OSA amplifier and the OSA integrator



(a) The clock diagram of the OSA amplifier and other front-end circuits



(b) The clock diagram of the OSA integrator and other back-end circuits

Fig. 4. The clock diagram of the OSA amplifier and the OSA integrator

The kernel concept of the OSA technique is that the system gets its final operation result by several iteration steps rather than one step. During each iteration step, the system parameters are calibrated based on an operation error from the last step, so as to get an operation result more approximate to the ideal result than the one got from the last step.

During the phase Φ2 of the 1st step, the signal charge is transferred from the sensor's capacitors C_{S1} and C_{S2} to the capacitors C_i, causing an increment $\Delta V_o(n)$ (as shown in Fig. 5(a)) of the output of the OSA amplifier, and the 1/A error is $\Delta V_{1/A} = \Delta V_o(n)/A_0$ (as shown in Fig. 5(b)). By substituting the $\Delta V_{1/A}$ in (4), the level of the first step that the OSA amplifier can achieve is

$$V_o(n) = \frac{C_{S1} - C_{S2}}{C_i} V_R - \sigma_d \frac{\Delta V_o(n)}{A_0} \tag{8}$$

Then during the next phase Φ1 in the 1st step, the 1/A error produced by $V_O(n)$ is calibrated to zero. This is because the terminals A+ and A- (in Fig. 3(a)) are shorted to the ground and the V_{A+A-} becomes zero, while the V_{B+B-} remains $V_O(n)/A_0$ due to the holding of the output level by the C_H. This means that the 1/A error produced by $V_O(n)$ is "absorbed" by the calibration capacitor C_{OSA} with the increasing of the voltage difference of the C_{OSA} (that is the grey-color space between the red line and the blue line as shown in Fig. 5(b)).

During the phase Φ2 of the 2nd step, as the "old" 1/A error in the 1st step is eliminated, the output is able to achieve a more accurate level and produces a "new" increment $\Delta V_o(n+1)$. The "new" increment $\Delta V_o(n+1)$ produces a "new" 1/A error which then is eliminated during the coming phase Φ1 of the 2nd step, making the next step more accurate and producing a "new" increment $\Delta V_o(n+2)$. So according to this iteration pattern, the output levels in the 2nd, 3rd, … , till the N-th step are,

$$\begin{aligned} V_o(n+1) &= \frac{C_{S1} - C_{S2}}{C_i} V_R - \sigma_d \frac{\Delta V_o(n+1)}{A_0} \\ V_o(n+2) &= \frac{C_{S1} - C_{S2}}{C_i} V_R - \sigma_d \frac{\Delta V_o(n+2)}{A_0} \\ &\vdots \\ V_o(n+N) &= \frac{C_{S1} - C_{S2}}{C_i} V_R - \sigma_d \frac{\Delta V_o(n+N)}{A_0} \end{aligned} \tag{9}$$

The relationship between two steps is

$$\Delta V_o(n+1) = V_o(n+1) - V_o(n) \tag{10}$$

By combining (8)-(10), the output level of N-th step is,

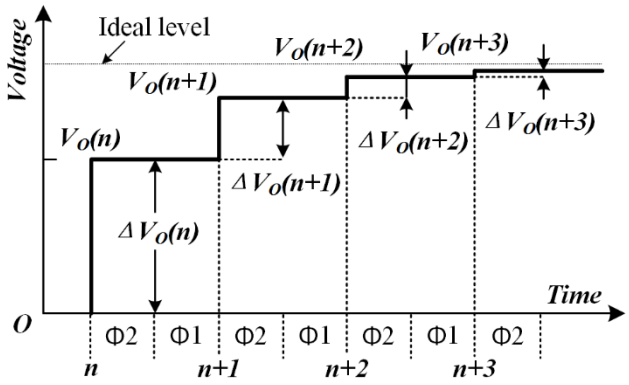
$$\begin{aligned} V_o(n+N) &= \frac{C_{S1} - C_{S2}}{C_i} V_R \left[1 - \left(\frac{1}{1 + A_0/\sigma_d}\right)^{N+1}\right] \\ \sigma_d &= \frac{C_{P0} + C_{S1} - C_{S2} - C_i}{C_i} \end{aligned} \tag{11}$$

where the term $\left(\frac{1}{1+A_0/\sigma_d}\right)$ is the fractional error, which also represents the gain error. The steps required to reach 0.1% fractional error with different gains and deterioration factors are shown in Fig. 6, where Fig. 6(a) is based on the numerical results from (11) and Fig. 6(b) is based on the numerical results from the transistor level simulation. It is seen from Fig. 6 that (11) can effectively predicate the trend. The predication is less accurate when the gain of the amplifier is very low. This is because the voltage difference V_{B+B-} of the OSA based SC-CVC in Fig. 3(a) increases with the decreasing of the amplifier's gain. As a result, the DC operation point of the amplifier is shifted and (11) becomes less accurate.

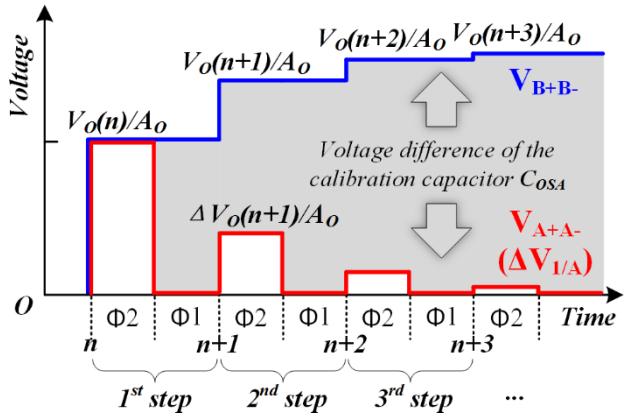
An important conclusion can be drawn from (11), that is the limit of the OSA output is the expected ideal output without the gain error, regardless of the gain A_0 and the parasitic capacitance C_{P0}, i.e.,

$$V_O(\infty) = \lim_{N\to\infty} V_o(n+N) = \frac{C_{S1} - C_{S2}}{C_i} V_R \tag{12}$$

This means that, by introducing the OSA technique, no matter how low the gain of amplifier is, given enough steps, the output will always reach the near ideal level.

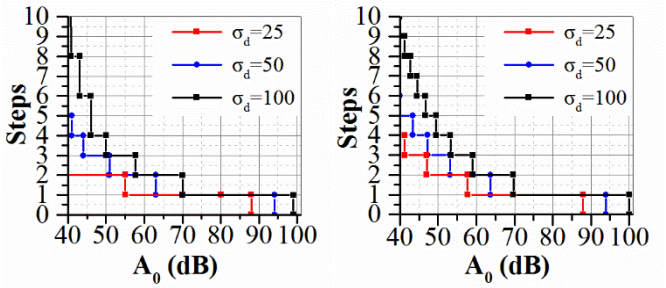


(a) The process of output voltage approaching ideal level



(b) The iteration process of "1/A error"($\Delta V_{1/A}$) diminishing. The voltage difference between terminals A+ and A- is denoted by V_{A+A-} (red line), and the voltage difference between terminals B+ and B- is denoted by V_{B+B-} (blue line).

Fig. 5. The process of the OSA amplifier reaching its ideal output and the "1/A error" diminishing



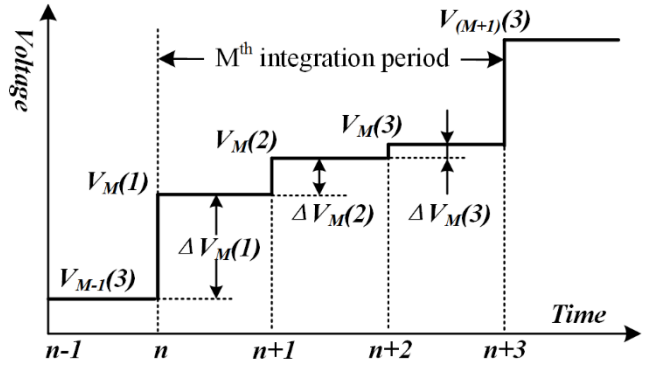
(a) The numerical results from the (11) (left)
(b) The numerical results from the transistor level simulation (right)
Fig. 6. The number of steps the OSA amplifier takes to achieve 0.1% fractional error varying with the amplifier's gain.

The OSA integrator operates in a similar way as the OSA amplifier does. In order to achieve an accurate result, one integrating operation is done by several OSA steps. The peculiar aspect of the OSA integrator is that each OSA step needs one individual integrating path. So the more OSA steps, the more consumption of chip area. Therefore, tradeoff has to be made between accuracy and chip area consumption. In this design, the integrator is designed with 3 OSA steps. As shown in Fig. 7(a), the output levels of 1st, 2nd and 3rd OSA step in the M^{th} integration operation are $V_{(M)}(1)$, $V_{(M)}(2)$ and $V_{(M)}(3)$, respectively.

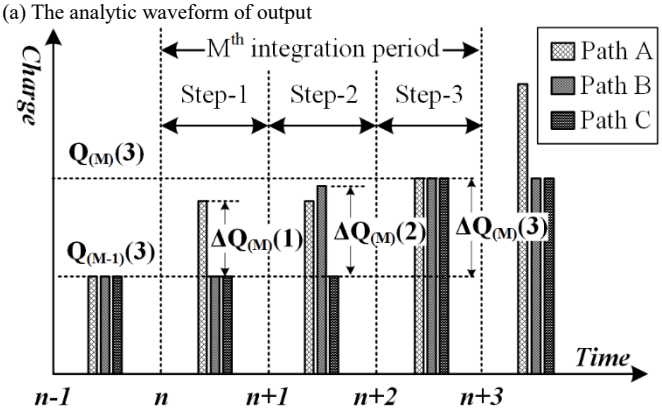
During the 1st step, the path A is connected to the sensor while the other paths are not connected. Signal charge is transferred to the capacitor C_i of the path A and a coarse result of the M^{th} integration $\Delta V_{(M)}(1)$ is produced, as shown in Fig. 7(a).

During the 2nd step, the path A is disconnected and the path B is connected and the M^{th} integration operation is repeated by the path B. As shown in Fig. 7(b), the charge increment $\Delta Q_{(M)}(2)$ of the C_i in the path B is more close to the ideal level than the charge increment $\Delta Q_{(M)}(1)$ of the C_i in the path A. This is also in accordance with the 1/A error diminishing process explained in Fig. 5. It is very important to notice that the path A is not able to repeat the M^{th} integration operation. This is because in order to repeat the M^{th} integration operation, the initial charge of the integration capacitor C_i must be $Q_{(M-1)}(3)$. However, the charge of the integration capacitor C_i in the path A have already got an increment $\Delta Q_{(M)}(1)$, and there is no method to hold back the increment accurately. That is why each OSA step needs its individual integrating path.

During the final step (step-3), the path C is connected to execute the last OSA step. The charge in the C_i in the path C ($Q_{(M)}(3)$) is the final result of this M^{th} integration operation. So all the other paths are connected to the path C to load this result ($Q_{(M)}(3)$), as shown in Fig. 7(b). Switches S3 in each path is used to load result from the output. But since the path C does not need to load result from other path, the S3 in the path C is constantly disconnected.

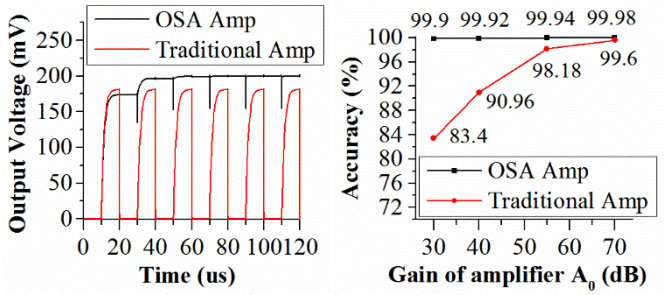


(a) The analytic waveform of output

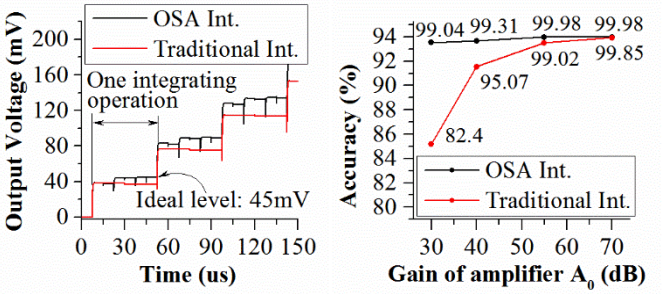


(b) The charge diagram of the integration capacitor C_i in each integration path
Fig. 7 The output waveform and charge diagram of OSA integrator

The transistor level simulation results of the OSA based operational circuits and the traditional operational circuits [8], [9] are shown in Fig. 8 (a)-(d). The transient waveforms in Fig. 8(a) show that although the output of the OSA amplifier in the first OSA step (174.0mV) is less accurate than the traditional amplifier (180.7mV), given enough steps, it will achieve higher accuracy (199.7mV while the ideal level is 200mV) than the traditional amplifier does. Fig. 8(b) shows that when the gain of the amplifier A_0 decreases from 70dB to 30dB, the gain accuracy of the traditional amplifier decreases by 16.2% (from 99.6% to 83.4%) while that of OSA amplifier decreases by only 0.08% (from 99.98% to 99.90%). Fig. 8(c) shows that the output level of the traditional integrator is 37.1mV (the ideal level is 45mV) for one integration operation, while that of the OSA integrator is able to achieve 44.6mV. Fig. 8(d) shows that when the gain of the amplifier A_0 decreases from 70dB to 30dB, the gain accuracy of the traditional integrator decreases by 17.4% (from 99.85% to 82.41%) while that of OSA integrator decreases by only 0.94% (from 99.98% to 99.04%).



(a) The transient waveforms of the amplifiers (left)
(b) The gain accuracy of the amplifiers varying with A_0 (right)



(c) The transient waveforms of the integrators (left)
(d) The gain accuracy of the integrator varying with A_0 (right)

Fig. 8. The comparison of accuracy between OSA based circuits and traditional circuits. The circuits are simulated by SPICE using 0.18um commercial BCD process of Dongbu HiTek Co., LTD.

B. Charge injection in OSA circuit

The OSA based operational circuits are very sensitive to interference charge injected into the calibration capacitor C_{OSA}. This is because the C_{OSA} is directly connected to the input terminal of the amplifier. Any interference charge injected into the C_{OSA} will be amplified by the amplifier. The higher the gain of the amplifier A_0 is, the more sensitive the OSA based circuits will be. So the most important designing principle for the OSA based circuits is to avoid any interference charge injecting into the calibration capacitor C_{OSA}. An example below shows how the interference charge decreases the output accuracy of the OSA based operational circuits.

The example is shown in Fig. 9 (a), the model is the OSA amplifier with the parasitic capacitance C_{P2} connected to the clock Φ1. The C_{P2} is caused by the parasitic capacitance of the MOSFET switches or coupling electrical field between two metal wires in physical layout. The interference charges Q_{P2+} and Q_{P2-} is injected to the OSA amplifier via C_{P2} from the clock Φ1 when the clock is active (known as the clock feed-through [13]). It is important to notice that the interference charges Q_{P2+} and Q_{P2-} are different though they are from the same interference source Φ1. This is because the transmission gate under different drain/source voltages injects different interference charges via the clock feed-though, as shown in Fig. 9(b). As the transmission gates connected to terminals V_{O+} and V_{O-} are biased in different voltages, when driven by Φ1, the charges injected from those transmission gates to the terminals V_{O+} and V_{O-} are different.

The different interference charges produces a differential error voltage $V_C(t_0)$ across the C_{OSA} which is very hard for the amplifier to settle out. This is because the interference charges are injected at the exact time when the C_{OSA} is being disconnected from the output of the amplifier, and the time interval is too short for the amplifier to settle out the interference charge. The equivalent circuit models to explain this settling process are shown in Fig. 9 (c). At the end of phase Φ1, it takes the clock an intervals (t_0 to t_1) to turn-over. This intervals typically varies from several hundred pico-second to several nano-second which is PVT (Process, voltage and temperature) depended. In this work, the intervals t_0 to t_1 is one nano-second. Assume that the interference charges are injected at t_0, as shown on the left of Fig. 9(c). By applying charge distribution law, the error voltage $V_C(t_0)$ across the C_{OSA} is

$$V_C(t_0) = \frac{\Delta Q_P}{C_{equ}}\beta$$

$$C_{equ} = C_{load} + \frac{C_{OSA}C_H}{C_{OSA}+C_H}$$

$$\beta = \frac{C_H}{C_{OSA}+C_H} \tag{13}$$

where $\Delta Q_P = Q_{P2+} - Q_{P2-}$ is the differential interference charge produced by C_{P2}, C_{equ} is equivalent capacitance at the output terminal, β is the feedback coefficient. Given the typical conditions ΔQ_P=1fQ, C_{load}=300fF, C_{OSA}=2pF and C_H=1pF, then the $V_C(t_0) = 0.34mV$, as shown in Fig. 9(d). After the charge injected in t_0, the amplifier tries to settle out this error voltage before the time t_1. As a result, the transient response of $V_C(t_1)$ is,

$$V_C(t_1) = V_C(t_0)\exp\left(-\frac{t_1 - t_0}{R_{equ}C_{equ}}\right)$$

$$C_{equ} = C_{load} + \frac{C_{OSA}C_H}{C_{OSA}+C_H}$$

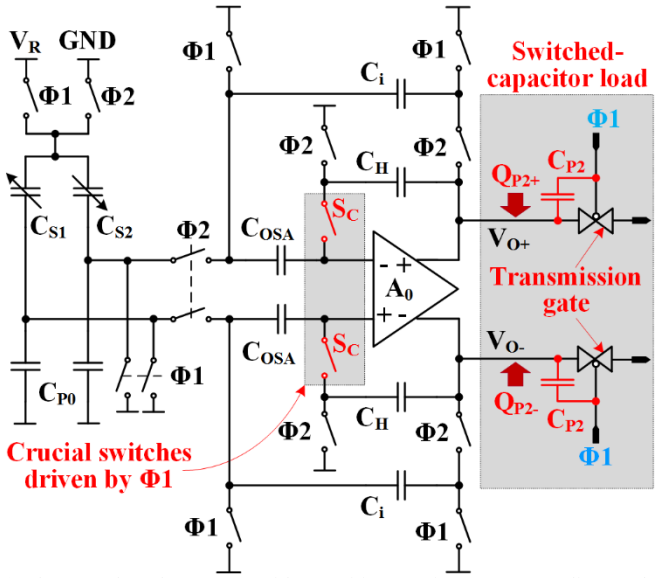
$$R_{equ} = r_o \| \frac{1}{g_m\beta}$$

$$\beta = \frac{C_H}{C_{OSA}+C_H} \tag{14}$$

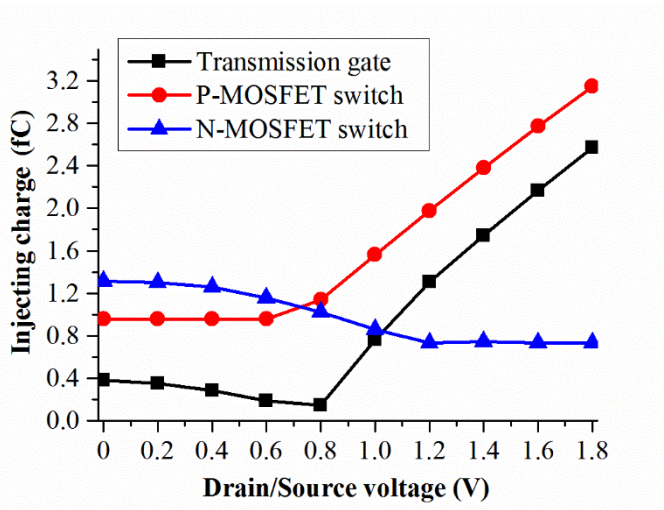
where R_{equ} is the equivalent resistance at the output terminal. Given the typical conditions $t_1 - t_0 = 1ns$, $g_m = 300us$, $r_o = 330k\Omega$, then the error voltage $V_C(t_1) = 0.31mV$, as shown in Fig. 9(d). After the time t_1, the switch S_C is completely disconnected and the amplifier will not be able to settle out the error voltage V_C in the C_{OSA}. As a result, the residual error voltage $V_C(t_1)$ stays in the C_{OSA}, and is amplified by g_mR_O during the Φ2, as shown in Fig. 9(c). So error in the output voltage is,

$$V_{O\_E\_\Phi1} = g_m R_O V_C(t_1) \tag{15}$$

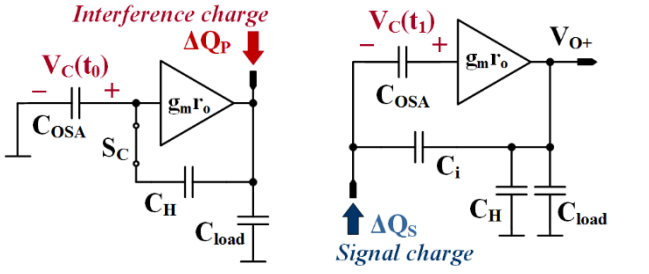
Given the typical conditions $A_1 = 40$dB, $g_m = 300us$, $r_o = 330k\Omega$, then $V_{O\_E\_\Phi1} = 31mV$. For the OSA amplifier designed in this work, the full range of the output signal is 300mV. So this interference is strong (10% of the full range) and must be reduced.



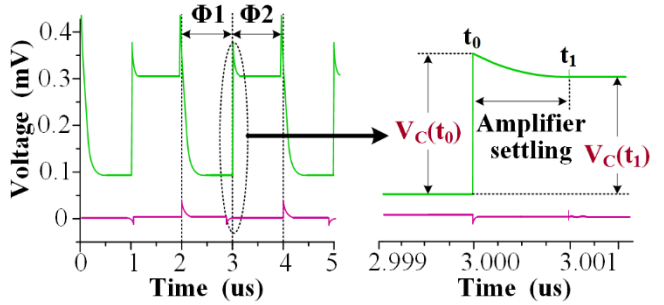
(a) The OSA based SC-CVC with parasitic capacitance C_{P2} coupling to the clock Φ1



(b) The injected charge of PMOS switch, NMOS switch and transmission gate under different drain/source voltages



(c) The simplified models of Fig. 9(a) at the time t_0 (left) and the time t_1 (right)



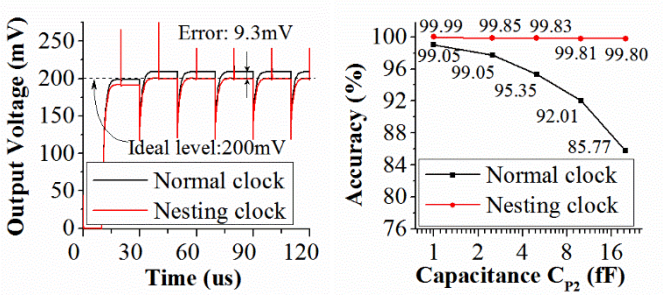
(d) The numerical analysis result of $V_C(t)$ with (the green line) and without (the red line) the parasitic capacitance C_{P2} coupling to the clock Φ1

Fig. 9. The circuit models and simulation results to illustrate the affect of charge injection in the OSA based SC-CVC

The solution to this problem is use of the nesting clocks. The nesting clocks are CLOCK-2 in Fig. 4(a). The switches S_C in the OSA amplifier in Fig. 9(a) are the crucial switches which must be driven by the nesting clock Φ1n. This is because the S_C is the only path through which the C_{OSA} can be charged. When driven by Φ1n, the S_C is enabled after the leading edge of clock Φ1 and is disabled before the post edge of clock Φ1. So during the period Φ1n when C_{OSA} is being charged, there is no switching operation in the whole circuit. As a result, the capacitor C_{OSA} is protected from interference charge caused by clock feed-through.

The transistor level simulation results show that, given the conditions that the A_1 is 40dB and the parasitic C_{P2} is 5fF, then the error voltage $V_{O\_E\_\Phi1}$ is 9.3mV, as shown in Fig. 10 (a). And the accuracy is decreased to 95.35% without using the nesting clock, as shown in Fig. 10(b). When the C_{P2} increases to 20fF, the accuracy is decreased to 85.77%, as shown in Fig. 10 (b). When driven by the nesting clock, the accuracy of the OSA amplifier significantly increases from 85.77% to 99.8%.

Besides, by adopting the dummy MOSFETs in the transmission gate, and given the following conditions [13]: 1) The switches' path lengths should be equal to the main switches, while path width are 1/2 that of the main switches; 2) The dummy switches should not turn off earlier than the main switches do, then the clock feed-through effect from the transmission gates will be further reduced.



(a) The transient waveform of the SC-CVC driven by different clocks (left)
(b) The gain accuracy varying with the parasitic capacitance C_{P2} (right)

Fig. 10. The transistor level simulation results to show the affect of charge injection in the OSA based SC-CVC

C. *Leakage current in OSA circuits*

The use of advanced CMOS process with smaller transistor channel length makes it easy to meet the requirement of low supply voltage. However, short channel length brings increasing leakage current. In a practical example, the normal transmission gate (the structure is shown in Fig. 16 (c)) is composed of a 2.5um channel width NMOS and a 5.0um channel width PMOS, while the channel lengths of the NMOS and PMOS are set to be the same value. The transmission gate is turned off and a 1.8V voltage is applied across the two terminals of the transmission gate to test leakage current. When the channel length increases from 180nm to 500nm, the leakage current I_{leak} of the normal transmission gate is shown in Fig. 11. It is clear that the leakage current increases with the decreasing of channel length and the maximum leakage current is 101pA in this example.

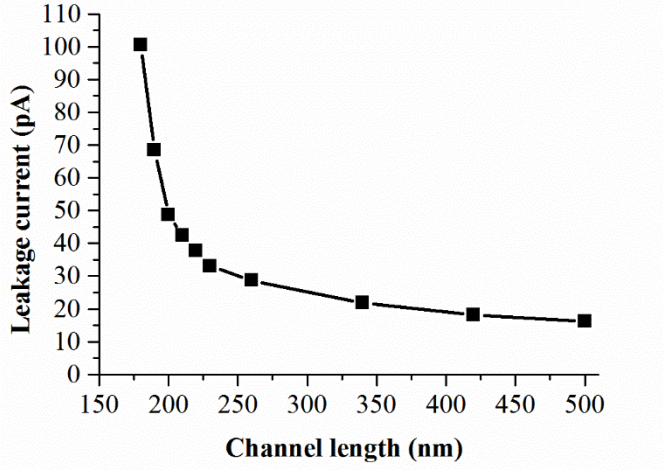


Fig. 11 The leakage current of a normal transmission gate varying with the channel length of MOSFET

The leakage current brings serious interference problem in the OSA based SC-CVC. This is illustrated as follows.

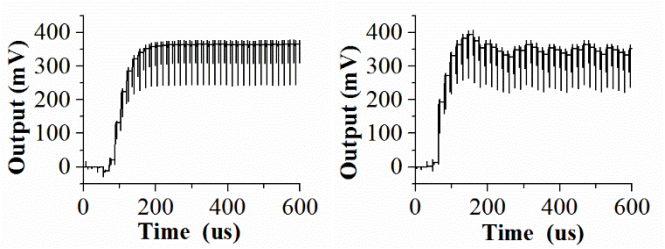
The feedback transmission gates driven by Φ3 in the FBC module (Fig. 16(a)) are connected between the terminals V_{O+}/V_{O-} and the terminals V_{I+}/V_{I-}. During normal operation, the voltages of the terminals V_{O+}/V_{O-} are digitally modulated (i.e.,

switching between V_{DD} and GND) while the voltages of the terminals V_{I+}/V_{I-} are constantly V_{REF}. As a result, the terminals V_{O+}/V_{O-} inject a leakage current I_{leak} into the terminals V_{I+}/V_{I-} during the phase Φ4. The leakage current I_{leak} produces error voltage at the output of SC-CVC, which is then amplified by the Op Amp module (Fig. 16(b)). The magnitude of the interference voltage at the output terminals of Op Amp is

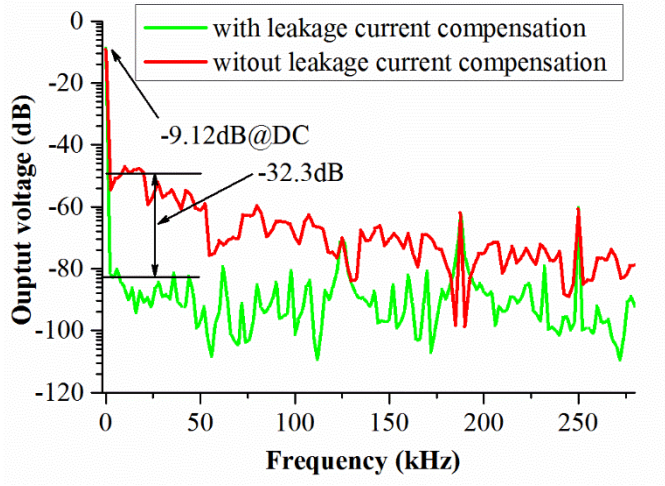
$$V_{N\_OP} = \frac{I_{leak} T_{\Phi 4}}{C_i} G_{OP} \tag{16}$$

where $T_{\Phi 4}$ is the duration of the high level of the readout phase Φ4, G_{OP} is the gain of Op Amp. Given the conditions that transistor channel length is 180nm (I_{leak}=101pA), $T_{\Phi 4}$=1us, G_{OP}=40 and C_i=90fF, the output voltage of Op Amp (the terminals $V_{O3}+/V_{O3-}$ in Fig. 16(b)) is shown in Fig. 12(a). It is clear that the output voltage which is expected to be at a DC level of 375mV is seriously interfered by the interference voltage V_{N_OP} caused by feedback signal. As the feedback signal comes from the output of Σ-Δ ADC, the interference is apparently periodic.

To solve this problem, leakage current compensation is introduced by adding two transmission gates connected between the input terminals V_{I+}/V_{I-} and the feedback terminals V_{O+}/V_{O-}, as shown in Fig. 16(a). These two transmission gates are constantly disconnected so as not to affect the normal operation, but they can provide leakage current whose magnitude is opposite to the leakage current produced by feedback transmission gates. As a result, the leakage current produced by feedback transmission gates is compensated and the periodic interference is effectively reduced, as shown in Fig. 12(b). From the spectrum of the output voltage of Op Amp with and without leakage current control as shown in Fig. 12(c), it is seen that with leakage current control the dynamic range has been improved by 32.3 dB in the low frequency bandwidth (<50 kHz).



(a) The transient waveform without leakage current compensation
(b) The transient waveform with leakage current compensation



(c) The spectrum of output with and without leakage current compensation

Fig. 12 The output voltages of Op Amp with and without leakage current compensation

D. Power consumption and noise performance

The purpose of the OSA is to relax gain requirement of amplifier, so that power consumption of amplifier is reduced. This is discussed in detail as follows. Meanwhile the noise performance is also discussed.

The total power dissipation of switched-capacitor circuits is the sum of two terms: 1) the switching power which is dissipated by charging and discharging the capacitors and 2) the power absorbed by the amplifiers [14]. The 1st term of the total power dissipation is calculated by the average current flowing through the capacitors [15]. In traditional SC-CVC, the average currents of C_i and C_S are,

$$I_{av\_ci} = C_i V_{FS} f_s$$
$$I_{av\_cs} = (C_{S1} + C_{S2}) V_R f_s \tag{17}$$

Given the conditions that C_i=100fF, $C_{S1}+C_{S2}$=300fF, V_{FS} is the full scaled of the output voltage whose value is 500mV, V_R is the reference voltage whose value is 900mV, and fs is the sampling rate whose value is 200kHz, then the power consumptions of C_i and C_S are,

$$P_{av\_ci} = V_{FS} I_{av\_ci} = 5.0\ nW$$
$$P_{av\_cs} = V_{FS} I_{av\_cs} = 48.6\ nW \tag{18}$$

In the OSA based SC-CVC, although there are two more capacitors (i.e. C_{OSA} and C_H) than that in the traditional SC-CVC, but these two capacitors do not consume significant power, because their voltages do not swing from zero to signal level periodically and the average currents flow through them are nearly zero. So the power is still consumed by Ci and Cs,

$$I_{av\_ci\_OSSA} = C_i V_{FS} f_{S\_OSSA}$$
$$I_{av\_cs\_OSSA} = (C_{S1} + C_{S2}) V_R f_{S\_OSSA} \tag{19}$$

where f_{S_OSA} is the sampling rate whose value is 1MHz in this design. The power consumptions of C_i and C_S are,

$$P_{av\_ci\_OSSA} = V_{FS} I_{av\_ci\_OSSA} = 25\ nW$$
$$P_{av\_cs\_OSSA} = V_{FS} I_{av\_cs\_OSSA} = 243\ nW \tag{20}$$

From (18) and (20), it is clear that in both the traditional SC-CVC and the OSA based SC-CVC, the power consumption by the capacitors is negligible compared to the power consumption of the amplifier whose power consumption is typical tens of micro-watt. Thus, the power consumption comparison between the OSA based SC-CVC (Fig. 3) which adopts the single-stage amplifier and the traditional SC-CVC (Fig. 1) which adopts the two-stage amplifier is based on the requirements of the amplifiers they use.

The power consumption of the amplifier depends on the unity gain bandwidth which is determined by sampling rate. The sampling rate of the OSA based SC-CVC is 3 times the sampling rate of the traditional SC-CVC, which is set according to the gain error. This is because it takes 3 steps for the OSA based SC-CVC with single-stage amplifier (typical gain is 39.9dB) to achieve the similar level as the gain error as the traditional SC-CVC with two-stage amplifier (typical gain is 72.4dB). As a result, the unity gain bandwidth of the single-stage amplifier used and the two-stage amplifier are set to be 9.0MHz and 3.0MHz, respectively, which results in 36.8uW and 62.3uW power consumption in the OSA based SC-CVC and the traditional SC-CVC, respectively, as shown in the table I. The load capacitance of the single-stage amplifier is 1pF

larger than that of the two-stage amplifier in order to give a fair comparison, since the capacitor C_H (typical value is 1pF) is added to the load of the OSA based SC-CVC.

TABLE I COMPARISON BETWEEN THE OSSA BASE SC-CVC AND THE TRADITIONAL SC-CVC

Parameter	Single-stage (2pF load)	Two-stage (1pF load)
Unity gain bandwidth	9.0MHz	3.0MHz
Gain	39.9dB	72.4dB
Power consumption	36.5uW	62.2uW
Area consumption	2200um^2	7000 um^2
Phase margin	90 degree	90degree
Thermal Noise (input equivalent)	22nV/√Hz	21nV/√Hz
Parameter	**The OSA based SC-CVC**	**The Traditional SC-CVC**
Power consumption	36.8uW	62.3uW
Sampling rate	900kHz	300kHz
Output Noise	602uVrms	765uVrms
Input equivalent noise	67aF	85aF

The above analysis and calculation explain that the power consumption of the OSA operational circuits is far smaller than that of the traditional ones. The comparison of noise performance is as follows.

The circuit models for noise analysis of the OSA CVC are shown in Fig. 13(a), which contains only the relevant circuit elements and noise sources involved.

During the phase Φ1, the equivalent circuit model is shown in the left of Fig. 13(a), where the R_{ON} is the turn-on resistance of the switches and the R_O is the output resistance of the amplifier. According to the "equipartition theorem" [16] which says that any energy storage element (or "degree of freedom") in thermal equilibrium holds an average noise energy of kT/2, the total noise charge Q_A stored in the equivalent capacitance C_{equ_A} in the node A is,

$$\frac{1}{2}\frac{Q_A^2}{C_{equ\_A}} = \frac{kT}{2}$$

$$C_{equ\_A} = C_i + \frac{C_{OSA}C_H}{C_{OSA}+C_H} \tag{21}$$

The equivalent output noise voltage $\overline{V_{out\_N\_QA}^2}$ produced by Q_A when it is transferred to capacitor C_i is

$$\overline{V_{out\_N\_QA}^2} = \frac{Q_A^2}{C_i^2} = \frac{kT}{C_i^2}\left(C_i + \frac{C_{OSA}C_H}{C_{OSA}+C_H}\right) \tag{22}$$

During the phase Φ2, the equivalent circuit model is shown in the right of Fig. 13(a), where C_{IN} is the input equivalent capacitance of the amplifier. The output referred noise is dominated by the single-stage amplifier's current noise $\overline{I_{N1}^2}$, and the noise sources from the switches are not considered [16]. In this situation, the output reference noise voltage caused by the single-stage amplifier is,

$$\overline{V_{out\_N\_I}^2} = \int_0^\infty \overline{I_{N1}^2}|H(j\omega)|^2 d\omega$$

$$H(j\omega) = \frac{R_E}{1+j\omega R_E C_E} \tag{23}$$

The $\overline{I_{N1}^2}$ is the current noise which is the sum of the noises produced by the output NMOS and output PMOS of the amplifier,

$$\overline{I_{N1}^2} = 4kT\gamma\left(g_{mn}+g_{mp}\right) \tag{24}$$

where g_{mp} and g_{mn} are the trans-conductance of the transistors MP1 and MN1 in Fig. 3(c), respectively. The R_E and C_E are equivalent resistance and equivalent capacitance at the output node, respectively,

$$R_E = \frac{1}{\beta g_{mp}}$$

$$C_E = C_H + (1-\beta)C_i$$

$$\beta = \frac{C_i}{C_i + C_{P0} + C_S + \frac{C_{OSA}C_{IN}}{C_{OSA}+C_{IN}}}\frac{C_{OSA}}{C_{OSA}+C_{IN}} \tag{25}$$

where β is the feedback coefficient. By combining t (23) with (24), the output referred noise in the phase Φ2 caused by the amplifier is,

$$\overline{V_{out\_N\_I}^2} = \frac{1}{\beta}\frac{kT}{C_E}\gamma\left(1+\frac{g_{mn}}{g_{mp}}\right) \tag{26}$$

The total output referred noise $\overline{V_{out}^2}$ by (22) and (26) is,

$$\overline{V_{out}^2} = \frac{kT}{C_i^2}\left(C_i + \frac{C_{OSA}C_H}{C_{OSA}+C_H}\right) + \frac{1}{\beta}\frac{kT}{C_E}\gamma\left(1+\frac{g_{mn}}{g_{mp}}\right) \tag{27}$$

As the gain of the SC-CVC is V_R/C_i, so the total input equivalent noise of the OSA based SC-CVC is,

$$\overline{V_{in\_OSSA}^2} = \frac{kT}{V_R^2}\left(C_i + \frac{C_{OSA}C_H}{C_{OSA}+C_H}\right) + \frac{1}{\beta}\frac{kT}{C_E}\gamma\left(1+\frac{g_{mn}}{g_{mp}}\right)\frac{C_i^2}{V_R^2} \tag{28}$$

where

$$C_E = C_H + (1-\beta)C_i$$

$$\beta = \frac{C_i}{C_i + C_{P0} + C_S + \frac{C_{OSA}C_{IN}}{C_{OSA}+C_{IN}}}\frac{C_{OSA}}{C_{OSA}+C_{IN}}$$

$$\approx \frac{C_i}{C_i + C_{P0} + C_S + C_{IN}}$$

where β is simplified due to the condition $C_{OSA} >> C_{IN}$.

The circuit models for noise analysis of the traditional SC-CVC (shown in Fig.1) are shown in Fig. 13(b). Using the similar calculation process to the OSA based SC-CVC, the equivalent input noise voltage is,

$$\overline{V_{in\_trad}^2} = \frac{kT}{V_R^2}(C_i + C_C + C_{IN}) + \frac{1}{\beta'}\frac{kT}{C_E'}\gamma\left(1+\frac{g_{mn1}+g_{mn2}}{g_{mp1}}\right)\frac{C_i^2}{V_R^2} \tag{29}$$

where

$$C_E' = C_C + (1-\beta)C_i$$

$$\beta' = \frac{C_i}{C_i + C_{P0} + C_S + C_{IN}}$$

and g_{mn1}, g_{mn2} and g_{mp1} are the trans-conductance of transistor MN1, MN2 and MP1 in Fig. 1(c), respectively. Noise is calculated by MN1, MN2 and MP1, as it is dominated by the input stage rather than the second stage [17]. The equivalent capacitance C_E' at the output terminal is dominated by the Miller compensation capacitor Cc in Fig. 1(c).

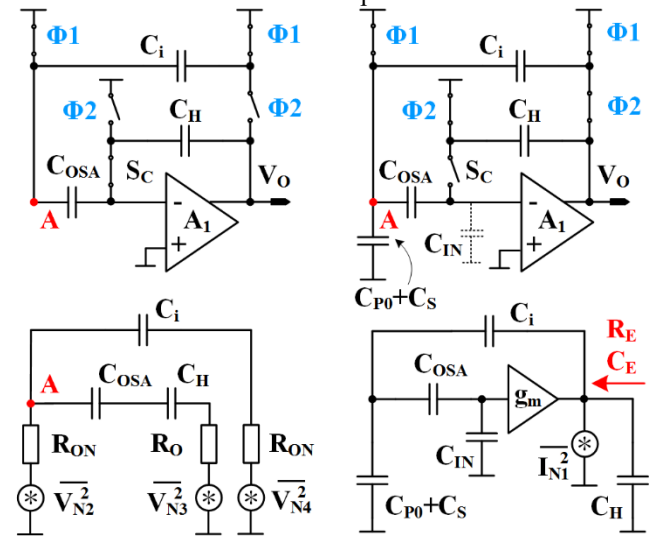
Given the conditions that the C_i=100fF, C_{IN}=200fF, C_L=500fF, C_{P0}=1pF, C_S=1pF, C_H=1pf, C_C=1pF, C_{OSA}=2pF, then the results of (28) is $(67aF)^2$ (where the 1st term and the 2nd term are $(62aF)^2$ and $(24aF)^2$, respectively), and the results of (29) is $(85aF)^2$ (where the 1st term and the 2nd term are $(81aF)^2$ and $(26aF)^2$, respectively). Thus the noises are dominated by the 1st term which are determined by the term $\frac{C_{OSA}C_H}{C_{OSA}+C_H}$ ((28) for the OSA based SC-CVC) and the term $(C_C + C_{IN})$ ((29) for the traditional SC-CVC). It is thus concluded that, if the condition:

$$\frac{C_{OSA}C_H}{C_{OSA}+C_H} < C_C + C_{IN} \tag{30}$$

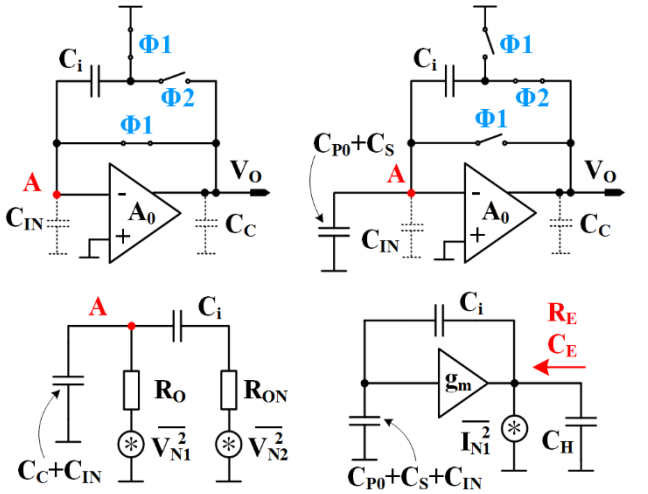
is met, the noise performance of the OSA based SC-CVC (Fig.

3) is better than that of the traditional SC-CVC (Fig. 1).

Although the DC charges of the C_{OSA} and C_H produced by the 1/A error voltage is memorized and accumulated in each step, the noise will not be accumulated. This is because the noise charge in capacitor C_{OSA} is refreshed in phase Φ1 during each step by the DC voltage sources and the amplifier A_1 with certain DC operation point, which means that the noise of the OSA based SC-CVC is memorized for only one step and will not be accumulated in the next step.



(a) The equivalent circuit model and noise model of the OSA based SC-CVC during the phase Φ1 (left) and during the phase Φ2 (right);



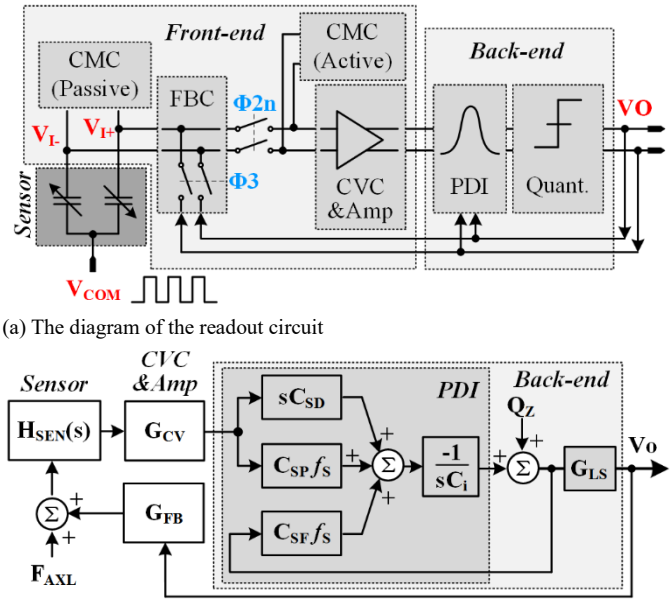
(b) The equivalent circuit model and noise model of the traditional SC-CVC during the phase Φ1 (left) and the phase Φ2 (right)

Fig. 13 The model to explain the noise performance of the OSA based SC-CVC (built with single-stage amplifier) and the traditional SC-CVC (built with two-stage amplifier)

III. THE READOUT CIRCUIT BASED ON THE OSA AMPLIFIERS AND INTEGRATORS

A closed-loop Σ-Δ readout circuit for MEMS accelerometer using the OSA amplifier and integrator is described in this section. The block diagram of the whole readout circuit is shown in Fig. 14(a). The Feed-Back Controller (FBC) transfers the feedback charge from the output terminal V_O of the readout circuit to the sensor in the feedback phase Φ3 and blocks the feedback charge in the readout phase Φ4. The clock phases Φ3 and Φ4 are shown in Fig. 4(a). The Common-Mode charge Controller (CMC) blocks the common-mode charge and passes the differential charge in the readout phase Φ3. The CMC includes both the passive CMC to offer constantly large controlling range and the active CMC to offer self-adaptive small controlling range. The Switched-Capacitor Capacitance-to-Voltage Convertor (SC-CVC) cascaded with the operational amplifier (Op Amp) converts the charge signal to voltage signal with significant gain. The proportional-differential integrator (PDI) provides lead phase compensation. And the last stage is the quantizer, the latch and the level shift.

Capacitive accelerometers usually operate in closed-loop, which has been proven to improve the linearity, dynamic range (DR) and bandwidth [6], [7], [9]. However, the sensor for acceleration detection is generally a two-pole device with high-Q value [4], [6]. This means that the system will be unstable if it is designed in closed-loop structure without any compensation method. So the PDI is introduced as the lead phase compensator to decrease the phase delay caused by the sensor's poles at the unity gain frequency, as shown in the signal flow graph in Fig.14 (b). The detailed formulas are derived as follows.



(a) The diagram of the readout circuit

(b) The signal flow graph of the readout circuit

Fig. 14. The diagram and signal flow diagram of whole readout circuit

The physical structure of the MEMS accelerometer is generally based on the spring-proof mass structure [3-12]. The photograph of the sensor used in this work and its equivalent model are shown in Fig. 15. There are two differential comb-structure capacitive sensors C_{S1} and C_{S2} in the X-axis and the Y-axis. All the capacitive sensors are connected to the proof mass surrounding them. The proof mass is suspended by the spring connected to the substrate of the die. The trans-function of the sensor is [4-6],

$$H_{SEN}(s) = G_{FC}\frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$$

$$Q = \frac{1}{D}\sqrt{\frac{K_S}{M_S}}\ ,\ \omega_0 = \sqrt{\frac{K_S}{M_S}} \qquad (30)$$

where ω_0 and Q are the resonant frequency and the quality factor of sensor, respectively, $G_{F\text{-}C}$ is the sensor's gain/sensitivity from the force to the capacitance, M_S is the proof mass, K_S is the spring coefficient and D is damping

coefficient. For sensor used in this paper, ω_0, Q and G_{FC} are 2kHz, 10, and 1.1fF/nN, respectively.

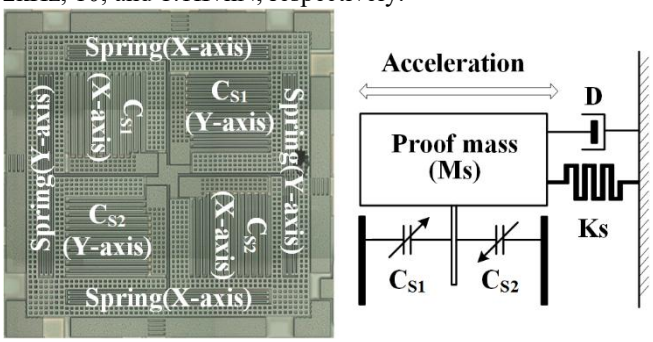


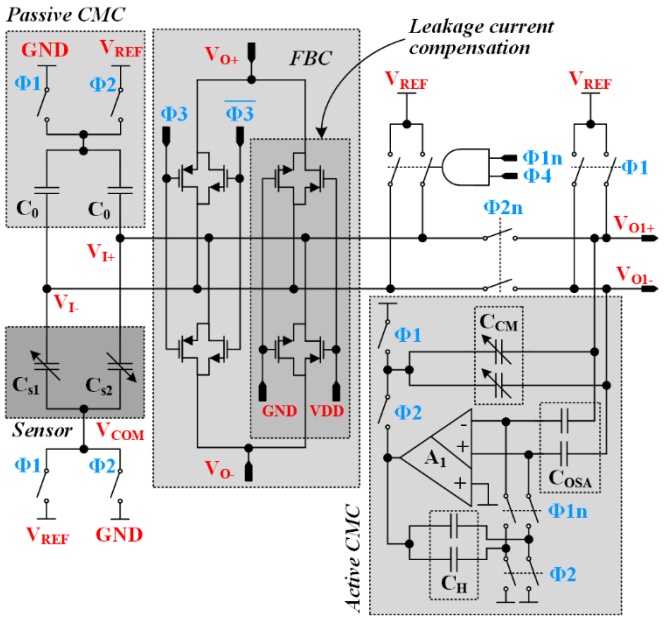
Fig. 15. The photograph and the model of the differential capacitive MEMS sensor for acceleration detection used in this work [25]

The circuit implements are shown in Fig. 16.

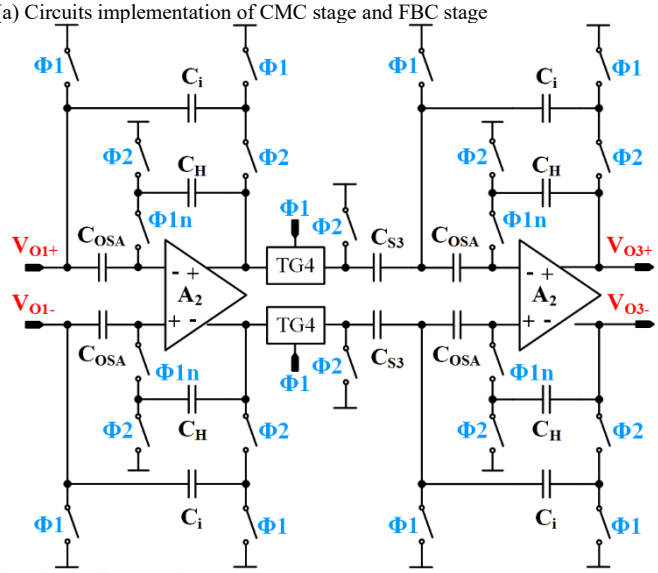
The FBC circuit shown in Fig. 16(a) is composed of four normal transmission gates. Two of these gates are controlled by clock (Φ3), which are the path for feedback signal. The other two transmission gates in the dark-colored box are constantly closed, which are used for leakage current compensation, as mentioned in the part C of section II. The CMC is implemented by a passive CMC at the input terminals V_{I+} and V_{I-} and an active CMC at the output terminals V_{O1+} and V_{O1-}, as shown in Fig. 16(a). As the common-mode charge is inherently unpredictable, the passive CMC is only able to cancel part of the common-mode charge and the rest is cancelled by the active CMC [3]. In this paper, the active CMC is also built based on the OSA amplifier.

Both of the SC-CVC stage and the Op Amp stage are built based on the OSA amplifier for gain accuracy, as shown in Fig. 16(b). All the switches in the circuit are normal transmission gates composed of one PMOS and one NMOS, except the switches (TG4) which are composed of main switches and 4 dummy MOSFETs, as shown in Fig. 5(c). The TG4 is used to reduce the charge injection effect mentioned in the part B of section II.

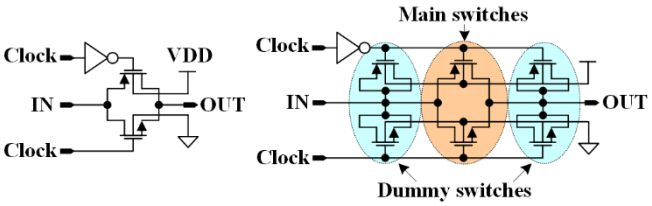
The back-end circuit includes a proportional-differential integrator (PDI) which provides one zero and one pole for lead phase compensation, an 1-bit quantizer (comparator), a latch (D-flip-flop) for sampling control, and a level shift ,as shown in Fig. 16 (d). The PDI is built based on the OSA integrator. It has three input paths, which are the feedback signal path with capacitor C_{SF}, the differential signal path with capacitor C_{SD} and the proportional signal path with capacitor C_{SP}. These three input paths are designed for generating the zero and the pole. The level shift is employed for the following reason. As the voltage slew of the single stage amplifier used by the OSA amplifier is only about 300mV, the DFF is supplied by 300mV reference voltage. Thus a level shift is used to boost the output level of the DFF to full scale (1.8V), in order to drive the sensor more efficiently.



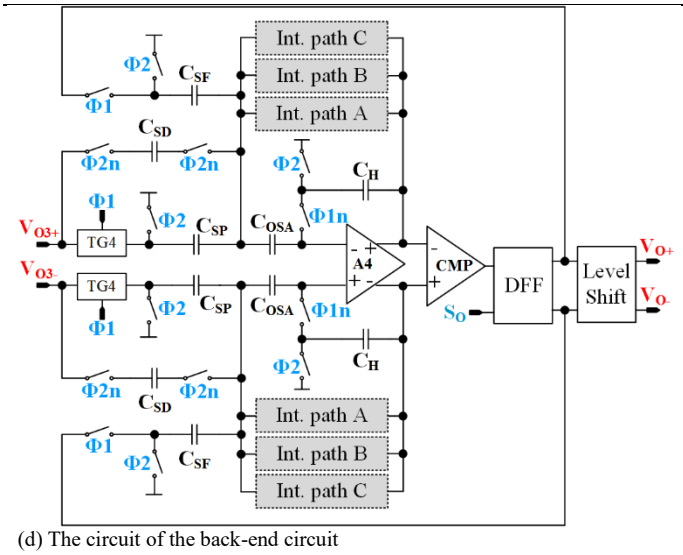
(a) Circuits implementation of CMC stage and FBC stage



(b) Circuit diagram of SC-CVC and Op Amp



(c) Normal transmission gate (left) and the Transmission gate with 4 dummy transistors (TG4) (right)



(d) The circuit of the back-end circuit

Fig. 16. The whole schematic of the readout circuit

The system trans-function of the readout circuit is derived as follows. The S-trans-function of the whole back-end circuit according to the signal flow graph in Fig. 14(b) is,

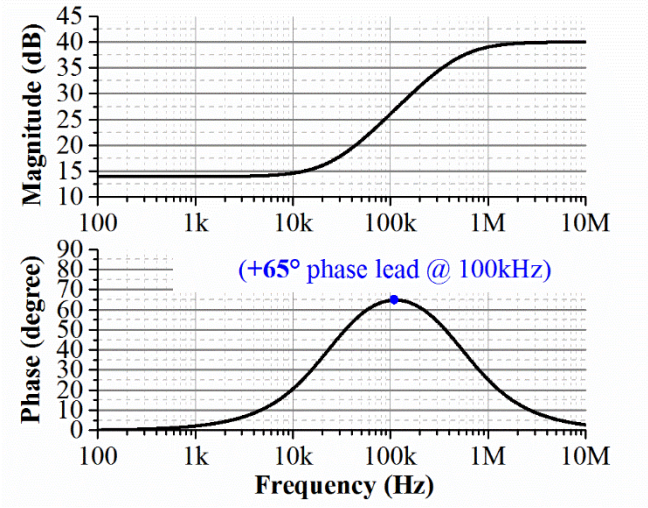
$$H_{Bak}(s) = G_{LS}\frac{C_{SD}}{C_i}\frac{s+\frac{C_{SP}}{C_{SD}}f_s}{s+\frac{C_{SF}}{C_i}f_s} \tag{31}$$

where G_{LS} is the gain introduced by the level shifting of the digital signal level whose value is 6V/V. Equation (31) shows that the PDI provides one pole at the frequency $f_s C_{SF}/C_i$ and one zero at the frequency $f_s C_{SP}/C_{SD}$. As a result, the overall open-loop signal transfer function (STF), the closed-loop STF and the closed-loop noise transfer function (NTF) are,

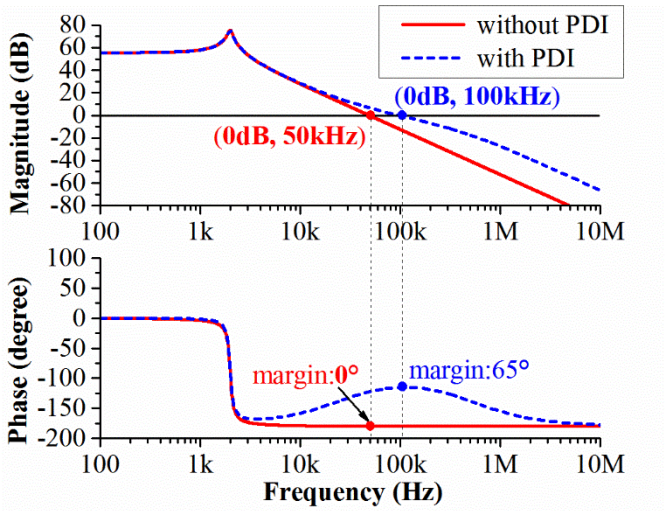
$$\begin{aligned} H_{STF\_OL}(s) &= G_{FB}G_{CV}H_{sen}(s)H_{Bak}(s) \\ H_{STF\_CL}(s) &= \frac{G_{CV}H_{sen}(s)H_{PDI}(s)}{1+G_{FB}G_{CV}H_{sen}(s)H_{Bak}(s)} \\ H_{NTF\_CL}(s) &= \frac{1}{1+G_{FB}G_{CV}H_{sen}(s)H_{Bak}(s)} \end{aligned} \tag{32}$$

where G_{CV} is the gain of the SC-CVC cascaded with Op Amp, whose value is 0.75V/fF, G_{FB} is the gain of the feedback actuator (it is an electrostatic driver), whose value is 111nN/V. The $H_{STF\_CL}(s)$ is a low pass filter and the $H_{NTF\_CL}(s)$ is a high-pass filter, so that the noise is separated from signal in frequency domain, which is the concept of noise shaping [9].

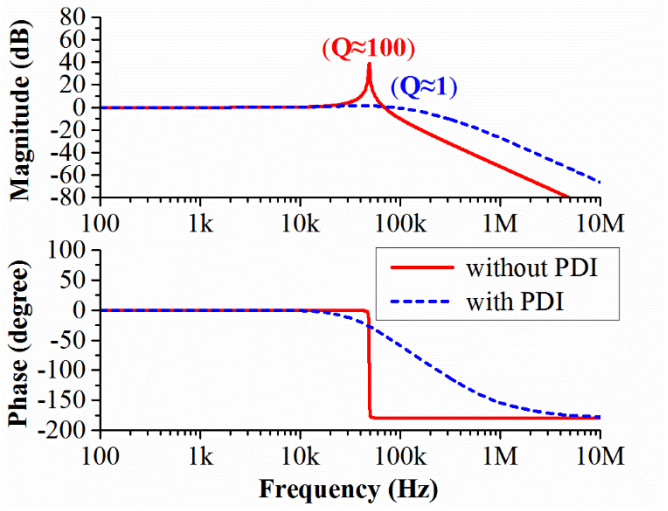
The numerical analysis results of the system are shown in Fig. 17. Given the conditions C_{SP}=50fF, C_{SD}=2pfF, C_{SF}=50fF, C_i=150fF, it is seen from Fig. 17(a) that the PDI provides 65 degree phase lead at the frequency of 100 kHz, according to (31). This phase lead provides important phase margin in the open-loop trans-function of the whole system. The open-loop trans-function of the whole system without PDI has zero phase margin, as shown in Fig. 17(b), which results in unstable closed-loop trans-function (high Q=100), as shown in Fig. 17(c). The open-loop trans-function of the whole system with PDI has a 65 degree phase margin, as shown in Fig. 17(b), which results in a stable (low Q=1) closed-loop trans-function, as shown in Fig. 17(c). The Q value of the closed-loop trans-function is controllable by the phase margin the PDI provides. And the phase margin can be set by the ratio between the capacitors C_{SP} and C_{SD} and the ratio between the capacitors C_{SF} and C_i, according to (31). The readout circuit is a low pass filter for the signal and a high pass filter for the quantization noise according to (32), as shown in Fig. 17(d).



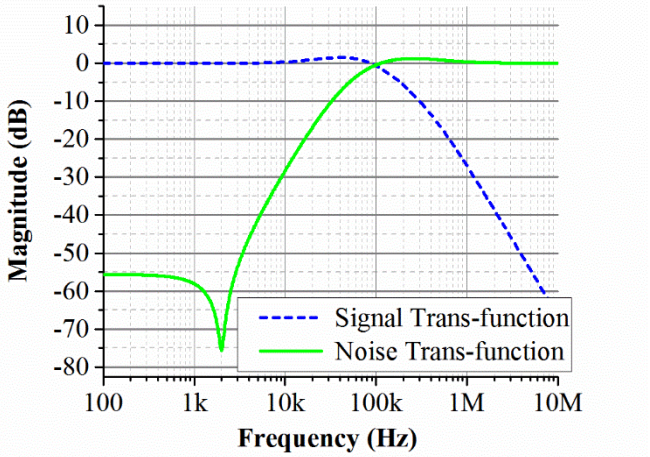
(a) The frequency response of the trans-function H_{BAK}



(b) The frequency response of the open-loop signal trans-function of the whole readout circuit with and without the PDI



(c) The frequency response of the closed-loop signal trans-function of the whole readout circuit with and without the PDI



(d) The magnitude response of the signal trans-function and the noise trans-function.

Fig. 17 The frequency response of the system trans-function explaining how the compensation works

IV. PHYSICAL VERIFICATION

The readout circuit is fabricated by Dongbu Hitek 0.18um BCD process. The gain error is tested under different parasitic capacitance C_{P0} at the input terminal of the readout IC shown in Fig. 1(a). In order to simulate the common-mode parasitic capacitance C_{P0} with different values, the micro-strip line capacitor is used rather than the discrete capacitor. This is because the absolute value of the discrete capacitor are too large for the measurement. The top view and the cross-section view of the micro-strip capacitors are shown in Fig. 18. The width of the micro-strip is 10mil, and the thickness and the permittivity of the dielectric layer are is 10mil and 4.4, respectively. The micro-strip has a capacitance of 3.0fF/mil. As a result, the capacitance with value varying from 1.0pF to 5.0pF are acquired with the micro-strip length varying from 333mil to 1700mil. The values of the micro-strip capacitance are verified by the semiconductor device parameter analyzer B1500A.

The test result is also shown in Fig. 18. The first point in the curve is the gain error of the output without any micro-strip capacitor, which is set as the reference point. It is concluded from the test results that the gain error of the proposed readout IC increases with the increasing of the common-mode parasitic capacitance. For the typical application of the side-by-side SiP package for the MEMS device, the value of common-mode parasitic capacitance is 2.5pF (1.0pF for ESD protection in IC die, 0.5pF for the pad in the IC die and 1.0pF for the parasitic capacitance between the proof mass and the substrate in the MEMS die), where the gain error is 0.07%.

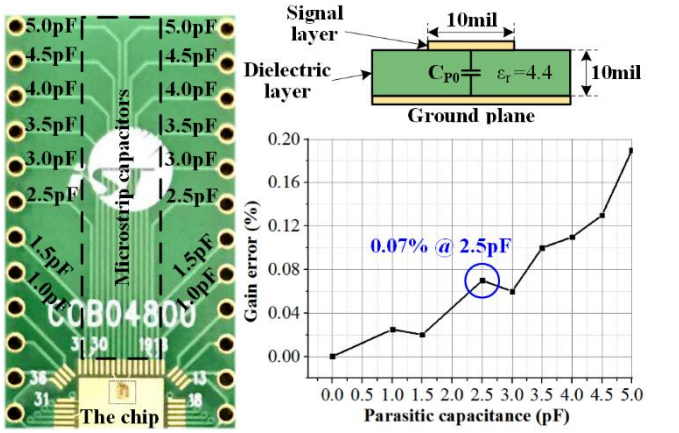


Fig. 18 The measurement results of the gain error against the common-mode parasitic capacitance simulated by the micro strip line capacitor

The comparisons of accuracy and power consumption are shown in the table II. The reference [20] achieves a higher gain accuracy (gain error<0.037%) than this work does (gain error<0.07%), due to the use of Dynamic Element Matching (DEM) technique. However, the gain requirement on the OTA used in the [20] is very high (150dB). This high-gain OTA is implemented with a two-stage amplifier with gain boosted structure which requires high supply voltage (5.0V). And the power consumption of these OTA is also very high. While the reference [20] wants to achieve low power consumption, it has to make a compromise with the unity gain-bandwidth of the OTA (250 kHz) for low current consumption. Even though the bandwidth is sacrificed by 36 times compared to this work (250 kHz vs. 9MHz), the power consumption of the [20] is still larger than that of this work due to the large number of the OTA used to implement its DEM technique. The reference [22] can withstand a larger value of the parasitic capacitance (470pF) than this work does (3.5pF) with the same gain error achieved (0.1%). This is achieved by sacrificing part of the charging current to compensate the charge loss due to the parasitic capacitance, which results in high power consumption (7mW). Both the reference [23] and the reference [24] employ digital calibration to reduce the gain error, which results in complex system due to the use of DAC and ADC. And thus the power consumption is higher than this work.

The other performances of the proposed readout IC are measured as follows.

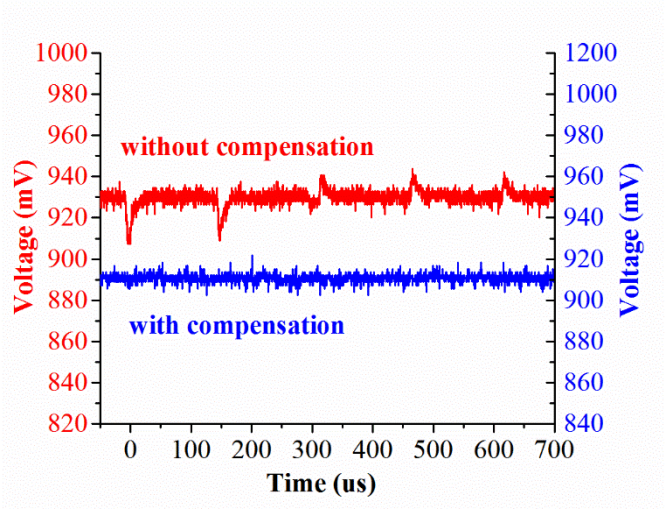
TABLE II PERFORMANCE COMPARISON BETWEEN READOUT CIRCUITS

	JSSC-2012 [20]	ISSCC-2011 [21]	JSSC-2008 [22]	SJ-2015 [23]	Analog-2011 [24]	This work
Gain error	<0.037%	<0.12%	<0.1%†	1%	1.2%	**<0.07%††**
Power consumption	1.35mW	1.35mW	7mW	5mW	5.85mW	**0.5mW**
Supply voltage	5.0V	5.0V	5.0V	5.0V	5.0V	**1.8V**
Structure/number of the amplifier	Two-stage gain boosted OTA/10	10	Specific structure amplifier/1	Three-stage OTA/5	Two-stage cascading OTA/5	**Single-stage OTA/4**
Gain/GBW of the amplifier	150dB/250kHz	-	-	86dB/38MHz	-/26MHz	**39.9dB/9MHz**
Sampling rate	30kHz	20kHz	5MHz	70kHz	1MHz	**1MHz**
System bandwidth	5Hz	-	-	-	500Hz	**100kHz**
Resolution	20bit	21bit	16bit	-	15bit	**15bit**
Area/Process	6mm^2/0.7um	6mm^2/0.7um	2.26mm^2/0.7um	3.76mm^2/0.35um	4.4mm^2/0.5um	**0.45mm^2/0.18um**

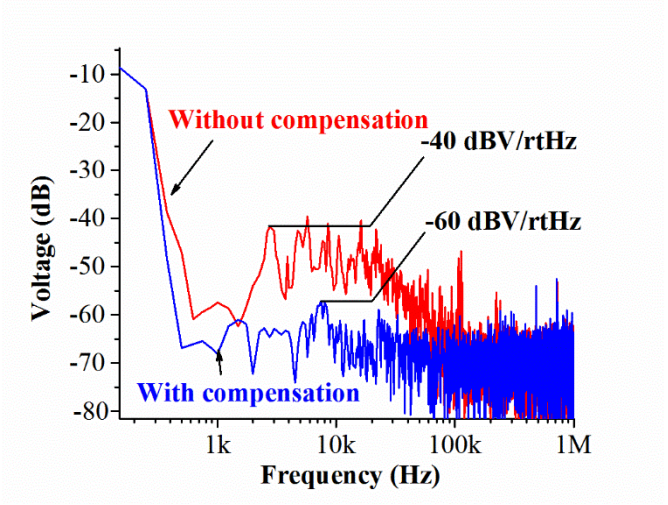
† With the condition that the value of the parasitic capacitance is 470pF. This value is chosen by considering the parasitic capacitance in PCB [22].

†† With the condition that the value of the parasitic capacitance is 2.0pF. This value is chosen by considering the parasitic capacitance in a side-to-side SiP package for MEMS application.

The transient waveform and the spectrum waveform of the output voltage of the output terminal of Op Amp are shown in Fig. 19. The sensor is not bonded in this measurement in order to show the interference more clear. It is seen that with the leakage compensation method in section II, the noise floor of the output is reduced by 20dB from -40dBV/rtHz to -60dBV/rtHz. The resolution of the readout circuit is determined by the noise floor which is calculated by dividing the output noise by the sensitivity of the sensor and the front-end circuit [9]. The sensitivities of the sensor and the front-end circuit are 55fF/g and 0.75V/fF, respectively. Thus the noise floor is 24ug/rtHz. The full scale measurement range of the readout circuit is ±1g, and the linearity within the full scale range is 1.2%, as shown in Fig. 20. The chip area consumption is also significantly reduced by replacing the two-stage amplifier with the single-stage amplifier. The chip area of the SC-CVC employing single stage amplifier is 90um×200um, as shown in Fig. 21(a), while the chip area of the traditional SC-CVC employing the two stage amplifier is 135um×215um, as shown in Fig. 21(b). This is because the Miller compensation network of the two stage fully differential amplifier costs extra 61% of the chip area. Other high gain amplifier structure such as the gain boosted OTA [9] will also easily double the chip area. The size of whole readout circuit is 840um×540um, as shown in Fig. 22 (a). The fabricated readout IC is wire-bonded to the sensor, and then packaged in COB (chip on board). The photograph of the fabricated chip is shown in Fig. 22(b). The summary of the measured parameters of the proposed readout circuit are shown in the table III.



(a) The transient signal



(b) The spectrum with 10k points

Fig. 19. The transient signal and the spectrum of the output of the readout circuit with and without leakage charge compensation

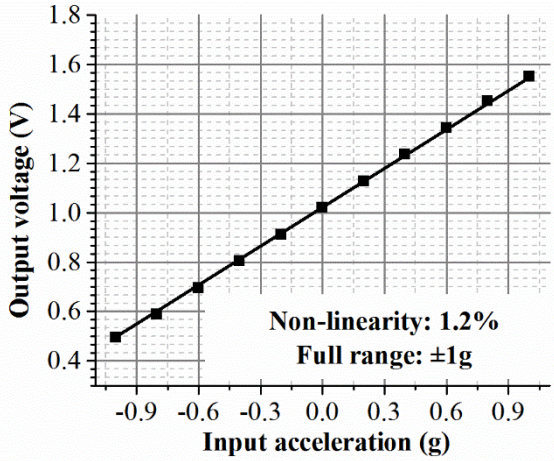
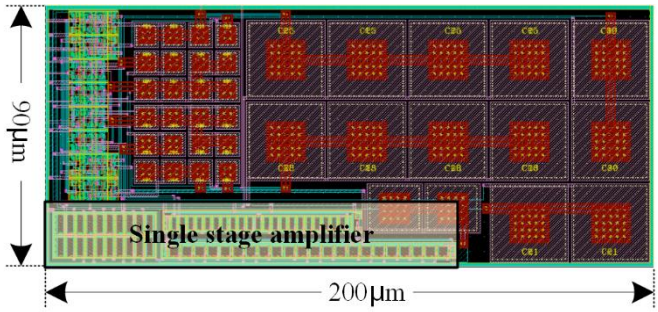
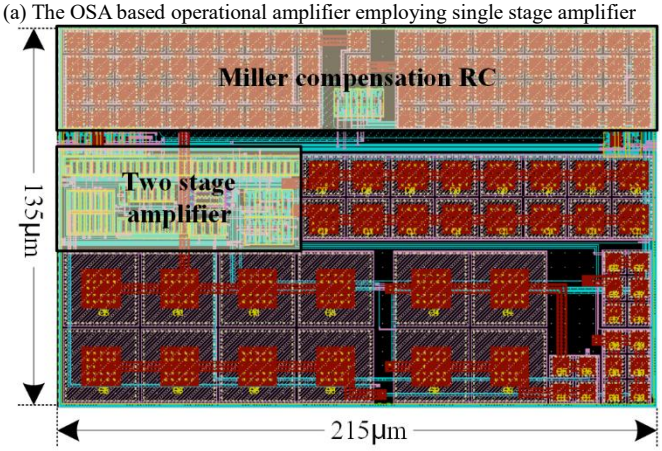


Fig. 20. The static output response to the accelerations in ±1g range.

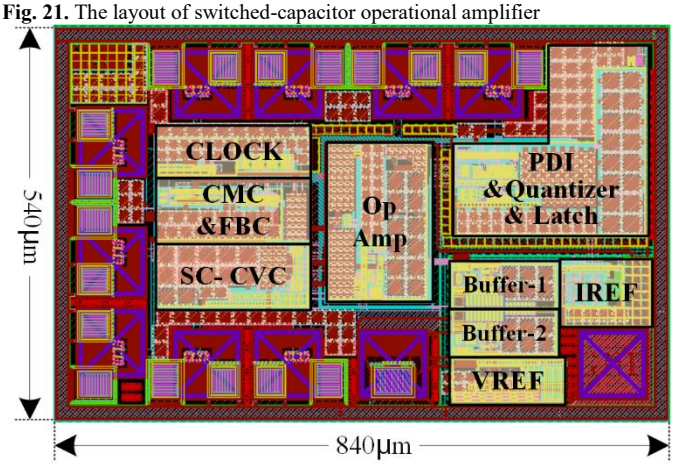


(a) The OSA based operational amplifier employing single stage amplifier

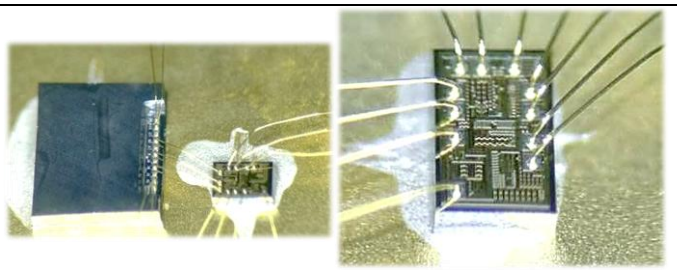


(b) The traditional operational amplifier employing two stage amplifier

Fig. 21. The layout of switched-capacitor operational amplifier



(a) The layout of the whole chip



(b) The photograph of the chip bonding to the sensor (left) and close-up photo of the chip (right)

Fig. 22. The layout and photograph of proposed readout circuit

TABLE III SUMMARY OF THE PARAMETER OF THE PROPOSED READOUT CIRCUIT

Sensor		
Device size	0.7mm×0.7mm×15um (X&Y axis)	
Rest capacitance	900fF	
Sensitivity	55 fF/g	
Bandwidth	2kHz	
Readout IC		
Power consumption	P	0.45uW-0.55uW from -40°C to 80°C
Gain accuracy	A_{CU}	Gain error <0.07% with 2.5pF external parasitic capacitance
Chip area	A_{REA}	0.2mm^2 (pads and EDSs are excluded)
Supply voltage	V_{DD}	1.8 V
Sampling rate	F_S	1MHz
Output Noise	V_{NO}	-60dBV/rtHz
Input range	R	±1g
Noise floor	N_F	24ug/rtHz
Resolution	R_{SOL}	15bit
Sensitivity	S_{FE}	0.75V/fF
Nonlinearity	NL	1.2%

V. CONCLUSION

A closed-loop Σ-Δ readout circuit for differential MEMS accelerometer is designed and fabricated using 0.18um commercial BCD process. The circuit is designed based on the OSA technique to relax the gain requirement of amplifier, thus high gain accuracy is achieved with low power consumption. Compared with other similar work [20-24], this work consumes the least power (0.5mW), which is benefited from the low power consumption single-stage amplifier rather than power-hungry high-gain amplifiers used in other work. Compared with the work [21-24], this achieves the lowest gain error 0.07%. The work [20] has a better gain error (0.037%) than this work does, but its bandwidth is 36 times lower than that of this work.

REFERENCE

[1] Hurtado N C, Zarifi M H, Daneshmand M, et al. "Flexible Microdisplacement Sensor for Wearable/Implantable Biomedical Applications". *IEEE Sensors J.*, vol.17, no.12, pp. 3873-3883, 2017.

[2] Tekin T. "Review of Packaging of Optoelectronic, Photonic, and MEMS Components". *IEEE J. Sel. Topics Quantum Electron.*, vol.17, no.3, pp.704-719, 2011.

[3] Lemkin M, Boser B E. "Three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics. *IEEE J. Solid-State Circuits*, vol.34, no.4, pp.456-468, 1999.

[4] Yucetas M, Pulkkinen M, Kalanti A, et al. "A High-Resolution Accelerometer with Electrostatic Damping and Improved Supply Sensitivity". *IEEE J. Solid-State Circuits*, vol.47, no.7, pp.1721-1730, 2012.

[5] L. Zhong, X. Lai and D. Xu, "Oversampling Successive Approximation Technique for MEMS Differential Capacitive Sensor," *IEEE J. Solid-State Circuits*, to be published. DOI: 10.1109/JSSC.2018.2827922.

[6] Xu H, Liu X, Yin L. "A Closed-Loop Σ Δ Interface for a High-Q Micromechanical Capacitive Accelerometer With 200 ng/√sqrtHz Input Noise Density", *IEEE J. Solid-State Circuits*, vol.50, no.9, pp.2101-2112,

2015.
[7] Wang X, Zhao J, Zhao Y, et al. "A 0.4 μg Bias Instability and 1.2 μg/√Hz Noise Floor MEMS Silicon Oscillating Accelerometer With CMOS Readout Circuit", *IEEE J. Solid-State Circuits*, vol.52, no.2, pp.472-482, 2016.
[8] Amini B V, Ayazi F, "A 2.5-V 14-bit ΣΔ CMOS SOI capacitive accelerometer," *IEEE J. Solid-State Circuits,* vol. 39, no. 12, pp. 2467-2476, 2004.
[9] Amini B V, Abdolvand R, Ayazi F. "A 4.5-mW Closed-Loop Σ Δ Micro-Gravity CMOS SOI Accelerometer", *IEEE J. Solid-State Circuits*, vol.41, no.12, pp.2983-2991, 2006.
[10] Zhao Y, Zhao J, Wang X, et al. "A Sub-μg Bias-Instability MEMS Oscillating Accelerometer With an Ultra-Low-Noise Read-Out Circuit in CMOS", *IEEE J. Solid-State Circuits*, vol.50, no.9, pp.2113-2126, 2015.
[11] Tan S S, Liu C Y, Yeh L K, et al. "An Integrated Low-Noise Sensing Circuit With Efficient Bias Stabilization for CMOS MEMS Capacitive Accelerometers", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.58, no.11, pp.2661-2672, 2011.
[12] Yoshizawa, H, T. Yabe, and G. C. Temes. "High-precision switched-capacitor integrator using low-gain opamp", *Electronics Letters*, vol.47, no.5, pp.315-316, 2011.
[13] Eichenberger C, Guggenbuhl W. "Dummy transistor compensation of analog MOS switches", *IEEE J. Solid-State Circuits*, vol.24, no.4, pp.1143-1146, 1989.
[14] Young C, Casinovi G, Fowler J, et al. "An algorithm for power estimation in switched-capacitor circuits", *IEEE ACM International Conference on Computer-Aided Design*, Iccad-96. Digest of Technical Papers, pp.450-454, 1996.
[15] E.A. Vittoz, "Future of Analog in the VLSI Environment", *Proc. ISCAS'90*, pp.1372-1375, 1990.
[16] Murmann B. "Thermal Noise in Track-and-Hold Circuits: Analysis and Simulation Techniques", *IEEE Solid-State Circuits Magazine*, vol.4, no.2, pp.46-54, 2012.
[17] Razavi B, "Design of analog CMOS integrated circuits," New York, USA: McGraw-Hill, 2001.
[18] S. H. Wu and J. T. Wu, "A 81-dB Dynamic Range 16-MHz Bandwidth ΔΣ Modulator Using Background Calibration," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2170-2179, 2013.
[19] T. Musah and U.-K. Moon, "Correlated level shifting integrator with reduced sensitivity to amplifier gain," *Electronics Letters*, vol. 47, no. 2, pp.91, 2011.
[20] Wu R, Chae Y, Huijsing J H, et al. "A 20-b ±40-mV Range Read-Out IC With 50-nV Offset and 0.04% Gain Error for Bridge Transducers", *IEEE J. Solid-State Circuits*, vol.47, no.9, pp.2152-2163, 2012.
[21] Wu R, Huijsing J H, Makinwa K A A. "A 21b ±40mV range read-out IC for bridge transducers". *IEEE International Solid-State Circuits Conference*, pp.110-112, 2011.
[22] Heidary A, Meijer G C M. "Features and Design Constraints for an Optimized SC Front-End Circuit for Capacitive Sensors with a Wide Dynamic Range", *IEEE J. Solid-State Circuits*, vol.43, no.7, pp.1609-1616, 2008.
[23] Lee D S, Tiwari H D, Kim S Y, et al. "A Highly Linear, Small-Area Analog Front End With Gain and Offset Compensation for Automotive Capacitive Pressure Sensors in 0.35um CMOS". *IEEE Sensors J.*, vol.15, no.3, pp.1967-1976, 2015.
[24] Ko H, Cho D I. "Low noise accelerometer microsystem with highly configurable capacitive interface". *Analog Integrated Circuits & Signal Processing*, vol.67, no.3, pp.365-373, 2011.
[25] Merassi A, Murari B, Zerbini S. "Micro-electromechanical structure with improved insensitivity to thermo-mechanical stresses induced by the package", US patent 7322242 B2, 2008.

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