A Novel Low Delay High-Voltage Level Shifter with Transient Performance Insensitive to Parasitic Capacitance and Transfer Voltage Level

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Abstract In this paper, a new high-voltage level shifter (HVLS) structure is proposed, which has a significantly improved transient response over existing structures. To overcome signal transfer delay of the conventional HVLS caused by parasitic capacitance due to high-voltage MOSFETs, this structure employs a novel circuit module "inverse Schmitt trigger" to drive the pull-up transistors of conventional HVLS. As a result, the "Miller Plateau" caused by parasitic capacitance can be minimized. Hence, the overall transfer delay of the structure is significantly reduced. The simulation results based on SPECTRE and 0.5μm high-voltage CMOS process show that compared to other currently available structures whose transfer delays are several nanoseconds on average, the proposed structure is able to provide a nanosecond transfer delay without using large boost capacitors which are impractical to be integrated or using complex logic units which decrease reliability of circuit. Also, the typical transfer delay of the proposed structure is a constant 1.3ns, which is irrelevant to parasitic capacitance and insensitive to transfer voltage level.

Keywords HV-CMOS, level shifter, inverse Schmitt trigger, transient response, MOSFET.

1 Introduction

Level shifter is an essential connection between circuits in different voltage domains, which is used to transfer logic signals in different voltage levels. It is widely used in multi-rail power supply on-chip systems, such as Very Large Scale Integration circuit (VLSI), Micro-Electro-Mechanical Systems (MEMS), mixed-signal integrated circuits and power-conversion systems [1-7,9-11,14-18,20-22,24-26]. As on-chip systems become more and more complex, level shifter has been developed for a wide range of applications as follows.

For high voltage applications [4-7,11,14-17,18,22,24], the recent years growing markets in smart electronic vehicles, renewable energy systems, high-brightness LED lighting systems, and MEMS

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devices, etc., have created high demands to design innovative high-voltage power converters for both cost and energy efficiencies. Clearly, integrating power transistors into a chip is a good way forward and the thin-oxide high-voltage MOSFETs are commonly used nowadays to realize on-chip power MOSFETs in high-voltage power converters. This is mainly because the thin-oxide high-voltage MOSFETs have advantages of significantly lower on-resistance and threshold voltage than those of the thick-oxide devices [22]. However, the thin-oxide high-voltage MOSFETs have limitations on V_{GS} (voltage difference from gate to source terminals of transistor) swing. For the p-channel thin-oxide high-voltage MOSFETs, a V_{GS} control signal has to be clamped within the range of 0~5V (or 0~1V, depending on process) referenced to the high-voltage supply. Therefore, to design an effective HVLS, clamping structure to prevent thin oxide from breaking down under high supply voltage is essential. However, clamping structure introduces additional parasitic capacitance which will adversely affect the transfer response of HVLS. This problem gets worse as transfer voltage level increases [17].

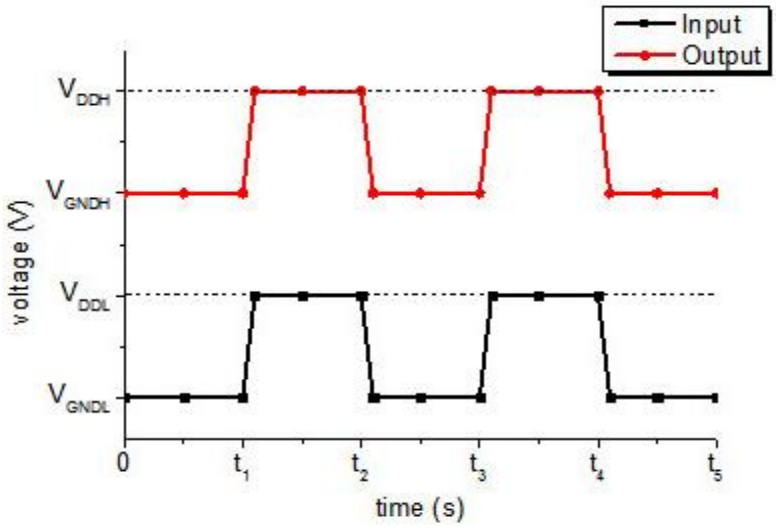
For low voltage applications [3,10,20,25,26], with the supply voltage of logic circuit decreasing to sub-threshold while the supply voltage of analog circuit remains unchanged, level shifter comes across new challenges [3]. The conventional level shifter design based on differential cascode voltage switch topology is limited for robust up-conversion from sub-threshold to super-threshold. This is due to the significant current contention caused by the limited driving strength of the pull-down devices operating in the sub-threshold region. The existing methods to solve this problem are, (a) decreasing the driving strength of pull-up devices by adding current limitation structures [20] or increasing the driving strength of pull-down devices by reducing threshold [20]; (b) converting the sub-threshold signal to the super-threshold signal by a boosting capacitor [10]; (c) employing a differential amplifier to take advantage of its high voltage gain instead of traditional differential cascode voltage switch structures [26]. Other level shifter applications [1,9,21] include its use along with switch capacitor circuit to compensate operational amplifiers.

In this paper, a new level shifter structure is presented for driving thin-oxide high-voltage power MOSFETs with 5V voltage limitation on V_{GS} in power management devices such as DC-DC converters. The transfer delay of this structure is of great significance for two reasons. Firstly, the overall power dissipation and the transfer delay of the gate drivers are usually determined by the transfer delay of level shifters. On one hand, if a level shifters has long transfer period during which big shoot through current may occur, it consumes extra power in proportion to transfer time. On the other hand, the dynamic dead-time control is needed if the transfer delay of level shifter is uncontrollable, which increases the complexity of the system [15]. Secondly, the switching frequency of DC-DC converters keeps increasing to reduce the size and cost. However, the maximum switching frequency is limited by the minimum propagated on-time pulse, which is mainly determined by the level shifter speed. For example, a DC-DC converters with a 50V input voltage and a 5V output voltages which operates at 10 MHz switching frequency, requires a pulse width modulated signal with an on-time less than 5 ns. This cannot be achieved with conventional level shifters [24]. In order to significantly reduce transfer time of this structure, a feed-forward invertor called "inverse Schmitt trigger" is proposed, and as a result, the transient response of this HVLS is improved greatly. The rest of the paper is organized as follows. In Sect. 2, the principles of the conventional HVLS are explained in detail, and the key factors affecting its transient response are analyzed. In Sect. 3, a new circuit module "inverse Schmitt trigger" is proposed

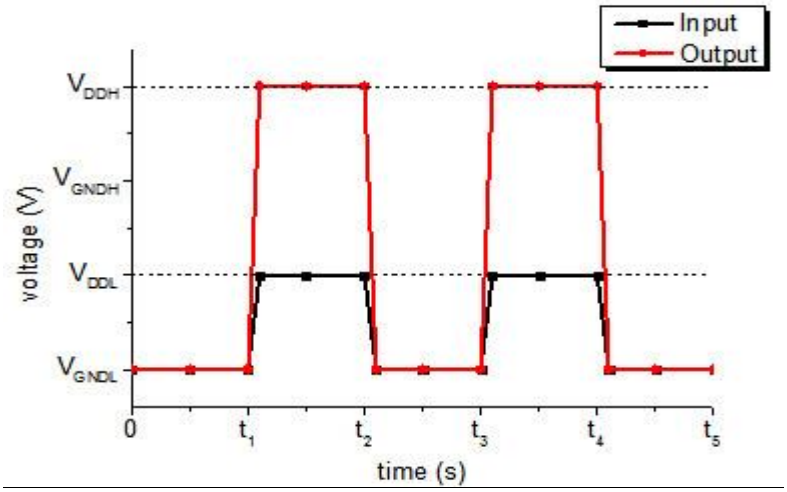
and incorporated into the conventional HVLS. Section 4 shows simulation results and presents analysis. The conclusions are then drawn in the Sect. 5.

2 Conventional High Voltage Level Shifter

As mentioned in the previous section, for the HVLS using the thin-oxide power MOSFETs, clamping structure is vital to protect the gate of power MOSFETs. The outputs of the HVLS with and without clamping structure are shown in Fig. 1. It can be seen that the clamping structure can limit the voltage swing of the output which is the driving voltage of thin-oxide power MOSFETs.



(a)



(b)

Fig. 1 Outputs of HVLS with and without clamping structure. **a** Output of HVLS with clamping structure. **b** Output of HVLS without clamping structure.

The early HVLS used diode-connected transistors or resistors to pull up the output to prevent the voltage level of output from dropping too much [6]. This clamping technique consumes constantly large static power during its operation, thus no longer used nowadays. The currently widely used HVLS structures [15-18] embed clamping structure into differential cascode voltage switch, as shown in Fig. 2. MP1, MP2, MN1, MN2 are normal MOSFETs, which form differential cascode voltage switch. MP3, MP4, MN3, MN4 are high-voltage MOSFETs used to form the clamping structure whose drain terminal can withstand high voltage. The structure eliminates static power consumption successfully.

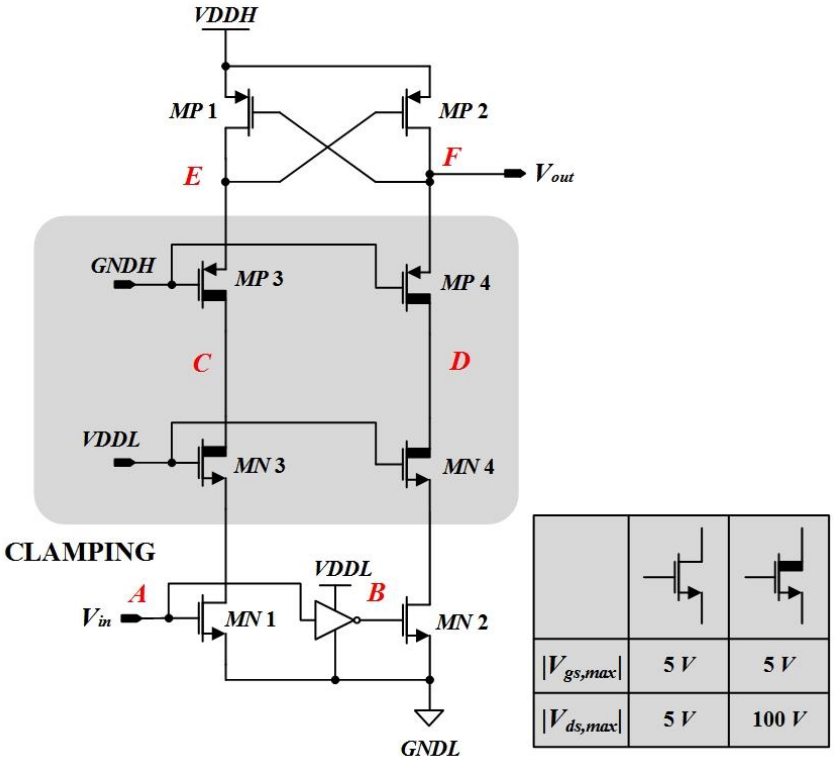


Fig. 2 The conventional HVLS with clamping structure

However, this conventional HVLS has considerable transfer delay, which is caused by the clamping structure. In this structure, the junctions C and D possess big parasitic capacitances due to the large size of high-voltage MOSFET. While they suffer a large voltage slew from V_{GNDL} to V_{DDH} of the same time. As a result, the charging time of the junctions C and inner node D becomes rather long.

Take the charging process of the inner node D as an example and assume that in Fig. 2, at the beginning of conversion, V_A is low. And then, V_A turns high. At this moment, the equivalent charging model of the Fig. 2 can be represented by Fig. 3, where C_C and C_D are the parasitic capacitances of the junctions C and D with their initial voltage equal to V_{DDH} and V_{GNDL}, respectively.

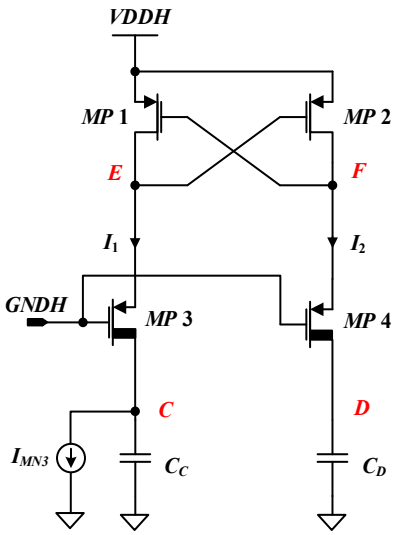


Fig. 3 Charging model of conventional HVLS while converting signal

The current sink source I_{MN3} is formed by the pull-down circuit (MOSFETs MN3 and MN1 in Fig. 2) and determined by MN3 since only MN3 operates in saturation region. The initial current magnitude of I_{MN3} can be described by the well-known "square law" of MOSFET when it operates in saturation region [19],

$$I_{MN3} = \frac{1}{2}\mu_N C_{OX}\left(\frac{W}{L}\right)(V_{DDL} - V_{THN})^2 = \beta_{MN3}(V_{DDL} - V_{THN})^2 \quad (1)$$

$$\beta_{MN3} = \frac{1}{2}\mu_N C_{OX}\left(\frac{W}{L}\right)$$

where μ_N is the N-type electron mobility, C_{OX} is the gate parasitic capacitance per unit-area, W is the width of MOSFET's channel, L is the length of MOSFET's channel, and V_{THN} is the threshold voltage of N-type MOSFET. However, the Eq. (1) will become invalid after a short charging period of time. Since V_C (potential in the junction C) will go down as charging progresses, all the transistors in the pull-up circuits including MP1, MP2, MP3 and MP4 become saturated. Then, there are the following relationships.

$$I_1 = \beta_{MP3}(V_E - V_{GNDH} - V_{THP})^2$$
$$I_1 = \beta_{MP1}(V_{DDH} - V_F - V_{THP})^2$$
$$I_2 = \beta_{MP4}(V_F - V_{GNDH} - V_{THP})^2$$
$$I_2 = \beta_{MP2}(V_{DDH} - V_E - V_{THP})^2 \quad (2)$$

Since the MOSFETs MP3 and MP4 have the same dimension, and so do MP1 and MP2, i.e.,

$$\beta_{MP1} = \beta_{MP2}$$
$$\beta_{MP3} = \beta_{MP4} \quad (3)$$

Combining the equations (2) and (3) results in the following equations.

$$V_E = V_F = V_{Blance} = \frac{\left(\sqrt{\frac{\beta_{MP1}}{\beta_{MP3}}}-1\right)V_{DDH} - \left(\sqrt{\frac{\beta_{MP3}}{\beta_{MP1}}}-1\right)V_{GNDH} - \left(\sqrt{\frac{\beta_{MP1}}{\beta_{MP3}}}+\sqrt{\frac{\beta_{MP3}}{\beta_{MP1}}}-2\right)V_{THP}}{\sqrt{\frac{\beta_{MP1}}{\beta_{MP3}}} - \sqrt{\frac{\beta_{MP3}}{\beta_{MP1}}}} \quad (4)$$

$$I_1 = I_2 = I_{Blance} = \beta_{MP1}(V_{DDH} - V_E - V_{THP})^2 \quad (5)$$

Furthermore, if $\beta_{MP1} = \beta_{MP2} = \beta_{MP3} = \beta_{MP4}$, the equations (4) and (5) become

$$V_E = V_F = V_{Blance} = \frac{V_{DDH} + V_{GNDH}}{2} \quad (6)$$

$$I_1 = I_2 = I_{Blance} = \beta_{MP1}(V_{DDH} - V_E - V_{THP})^2 \quad (7)$$

As the transfer delay is determined by charging speed of parasitic capacitance, employ the volt-ampere characteristic of capacitor, the charging time is

$$T_d = \frac{V_{DDH} - V_{GNDL}}{I_2} C_D \quad (8)$$

Two conclusions may be drawn from the above analysis. First, Eqs (6) and (7) suggest that during the period of transfer, all the MOSFETs in the pull-up circuit (MP1~MP4) remain saturated, which results in a limited charging current and an obvious transfer delay, as shown in Fig. 4. In fact, this phenomenon is a form of the well-known "Miller Plateau" effect [2,19]. Second, the transfer delay which is defined as the time consumed from the input change state till the output change state, is mainly determined by charging time of inner node C/D. To be more precise, the transfer delay mainly depends on the voltage difference (V_{DDH}-V_{GNDL}) to be transferred, the parasitic capacitance of high-voltage MOSFET (C_D) and the strength of the charging current (I_2) which is determined by the dimension of the pull-up MOSFETs.

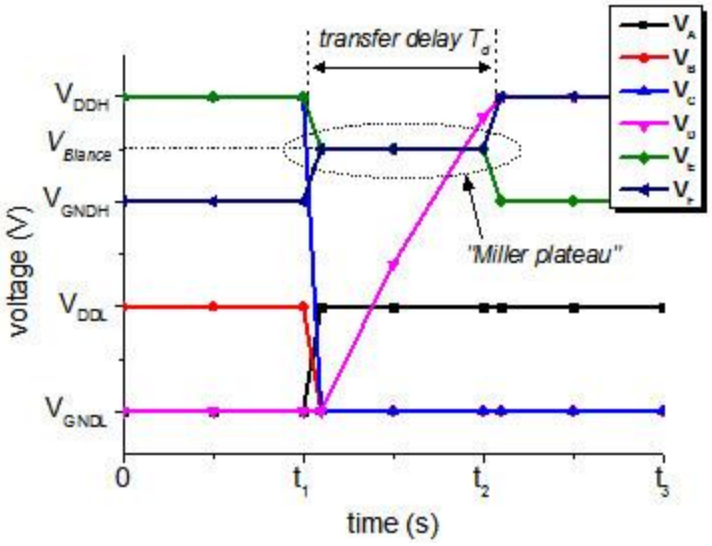


Fig. 4 Transfer waveforms of conventional HVLS

3. Improvement on Conventional HVLS

3.1 Inverse Schmitt Trigger

To overcome the transfer delay T_d in Fig. 4, the most effective method is to reshape the waveforms of V_E and V_F to a step signal. This can be achieved with the proposed inverse Schmitt trigger, which utilizes feed-forward of its input to control its switching threshold in order to achieve an advanced invert. This is different from the traditional Schmitt trigger which utilizes feedback of its output to control its switching threshold in order to achieve a hysteresis invert. The traditional Schmitt trigger is widely used in rejecting interference and data storage [8,12,13]. Figure 5 shows the outputs of the inverse Schmitt trigger, the traditional Schmitt trigger and normal invertor.

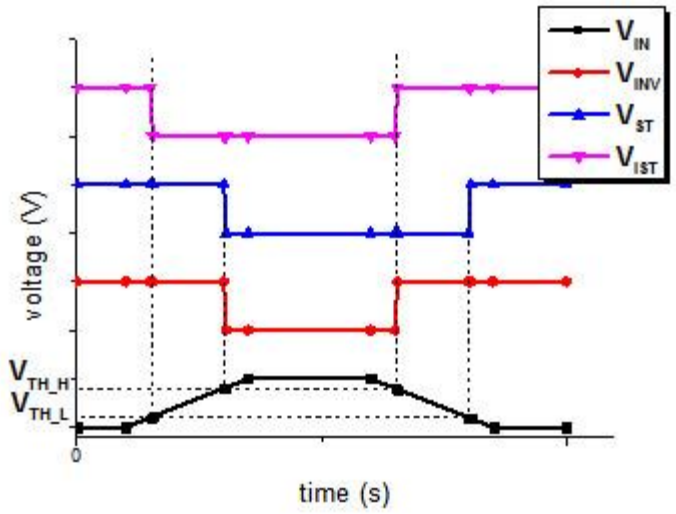


Fig. 5 Outputs of inverse Schmitt trigger (V_{IST}), Schmitt trigger (V_{ST}) and normal invertor (V_{INV})

The circuit of the inverse Schmitt trigger composed of twelve MOSFETs is shown in Fig. 6. The six MOSFETs on the left constitute a traditional Schmitt trigger, whose low switching threshold and high switching threshold are $V_{th\_ST\_L}$ and $V_{th\_ST\_H}$, respectively. The six MOSFETs on the right constitute a variable-threshold invertor, whose low switching threshold and high switching threshold are V_{th_L} and V_{th_H}, respectively. The thresholds of the variable-threshold invertor are controlled by the output of the Schmitt trigger.

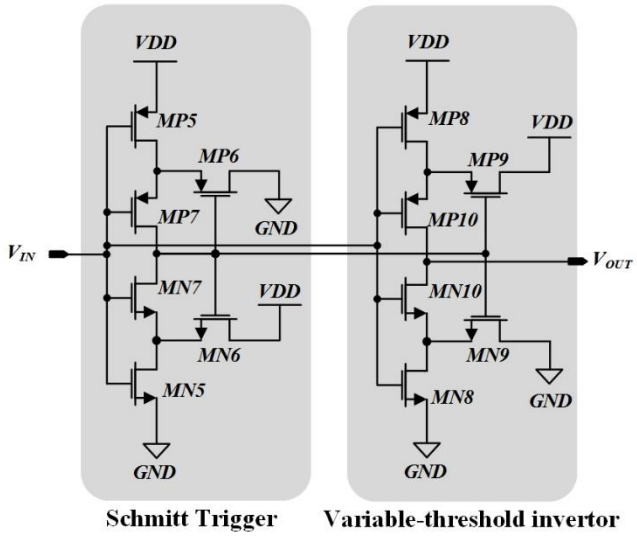


Fig. 6 Circuit of the proposed inverse Schmitt trigger

The low threshold of Schmitt trigger $V_{th\_ST\_L}$ and the high threshold of Schmitt trigger $V_{th\_ST\_H}$ are [8]

$$V_{th\_ST\_L} = \frac{V_{DD}-|V_{thp}|}{1+\sqrt{\frac{(W/L)_{MP6}}{(W/L)_{MP5}}}}$$

$$V_{th\_ST\_H} = \frac{V_{DD}+V_{thn}\sqrt{\frac{(W/L)_{MN5}}{(W/L)_{MN6}}}}{1+\sqrt{\frac{(W/L)_{MN5}}{(W/L)_{MN6}}}} \quad (9)$$

Where $(W/L)_{MP5}$, $(W/L)_{MP6}$, $(W/L)_{MN5}$ and $(W/L)_{MN6}$ are the width to length ratios of the transistors MP5, MP6, MN5 and MN6, respectively.

When the input V_{IN} is lower than $V_{th\_ST\_L}$, the output of Schmitt trigger is high and the active MOSFETs in the variable-threshold invertor are MP8, MP10, MN10 and MN9, as shown in Fig. 7a, in which MN9 and MP10 are not shown since it is in deep triode region and its resistance can be ignored. Similarly, When the input V_{IN} is higher than $V_{th\_ST\_L}$, the output of Schmitt trigger is high and the active MOSFETs in the variable-threshold invertor are MP8, MP10, MN10 and MN9, as shown in Fig. 7b, in which MN10 and MP9 are not shown since it is in deep triode region and its resistance can be ignored. So the low switching threshold and high switching threshold of the variable-threshold invertor can be expressed as thresholds of inverter [19],

$$V_{th\_L} = \frac{V_{DD}+V_{thn}\sqrt{\frac{(W/L)_{MN10}}{(W/L)_{MP8}}}-|V_{thp}|}{1+\sqrt{\frac{(W/L)_{MN10}}{(W/L)_{MP8}}}}$$

$$V_{th\_H} = \frac{V_{DD}+V_{thn}\sqrt{\frac{(W/L)_{MN8}}{(W/L)_{MP10}}}-|V_{thp}|}{1+\sqrt{\frac{(W/L)_{MN8}}{(W/L)_{MP10}}}} \quad (10)$$

Where V_{thp} and V_{thn} are thresholds of PMOS and NMOS, respectively. $(W/L)_{MP8}$, $(W/L)_{MN8}$, $(W/L)_{MP10}$ and $(W/L)_{MN10}$ are the width to length ratio of the transistors MP8, MN8, MP10 and MN10 respectively. Since MP8 is a narrow channel device, whose width-to-length ratio is far less than that of MN10, V_{th_L} is a very low threshold. Similarly, V_{th_H} is a very high threshold.

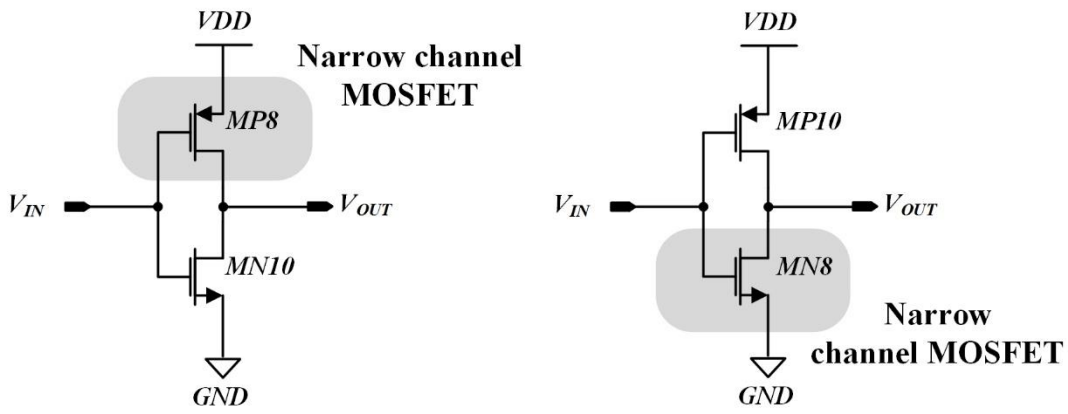


Fig. 7 Switching threshold equivalent circuits of variable-threshold invertor. **a** Low switching threshold. **b** High switching threshold.

During normal operation period, as the Schmitt trigger is the controller of variable-threshold invertor, the Schmitt trigger has to finish conversion and output stable control signal before the variable-threshold invertor starts conversion. That is to say , the thresholds $V_{th\_ST\_L}$, $V_{th\_ST\_H}$, V_{th_L} and V_{th_H} must satisfy the following conditions to guarantee stable function of the circuit.

$$V_{th\_ST\_L} < V_{th\_L} < V_{th\_H} < V_{th\_ST\_H} \quad (11)$$

If the conditions are not met, the output of Schmitt trigger will turn over earlier than the variable-threshold invertor does, which makes improper threshold switch and results in error switching pulses, as shown in Fig. 8. When the conditions in the expression (11) are satisfied, the inverse Schmitt trigger (V_{IST}) operates stably as expected.

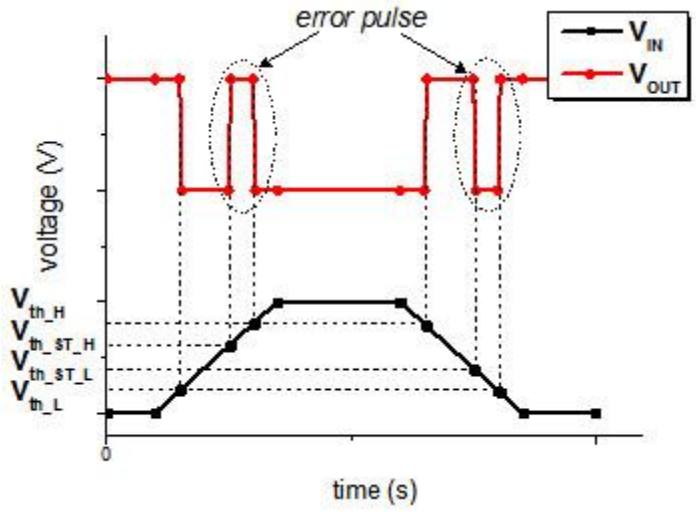


Fig. 8 Error switching pulses caused by improper threshold switch

3.2 The Transient Enhanced HVLS

To improve the transient response, the driving voltage of the pull-up transistors MP1 and MP2 in Fig. 2, which determines the charging current, should be enhanced. As discussed in the Sect. 2, the pull-up transistors MP1 and MP2 of the conventional HVLS cannot provide the maximum charging current in transfer period due to the "Miller plateau" shown in Fig. 4. This problem can be solved by incorporating "Inverse Schmitt trigger" into the conventional HVLS, as shown in Fig. 9, in which the "Inverse Schmitt trigger" is in serial connection with a normal inverter as feedback path to gate-terminal of MP1 and MP2. From the analysis in the previous sections, it can be easily drawn that when the input signal V_{in} reaches its falling edge, V_E reaches its rising edge and V_F reaches its falling edge. The inverse Schmitt trigger recognizes falling edge and uses high switching threshold to process V_E, at the same time it recognizes rising edge and uses low switching threshold to process V_F. During the transfer period, MP1 driven by V_G is able to move out of saturation and provide the maximum charging current, while MP2 driven by V_H is able to close completely. As a result, the transfer delay of V_E and V_F of the proposed HVLS (T_{d2} in Fig. 10) is much smaller than that of the conventional HVLS (T_d in Fig. 4), and the proposed HVLS outputs the expected level V_G (or V_H) before V_E (or V_F) reaches its stable level, as shown in Fig. 10.

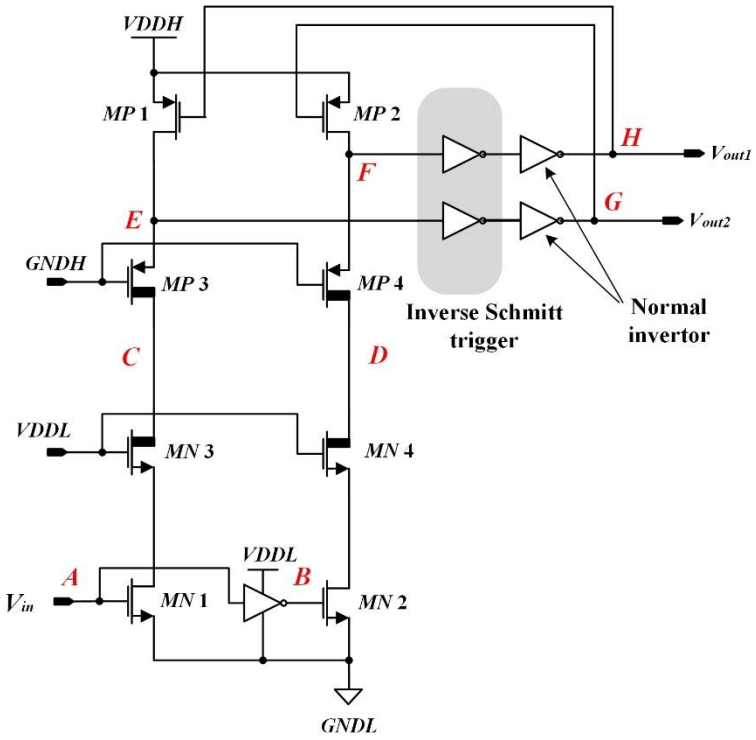


Fig. 9 Proposed HVLS circuit using the inverse Schmitt trigger

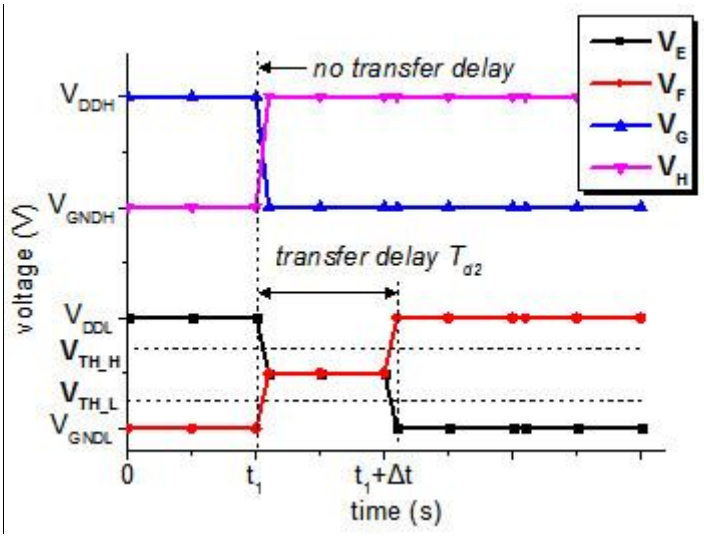


Fig. 10 Output waveforms of the proposed HVLS

Notice that, in Fig. 10, V_G and V_H complete their transfers before V_E and V_F do, and the "Miller Plateau" is removed. This means that the proposed HVLS minimized the transfer delay caused by junction parasitic capacitance In other words, the transfer delay of the proposed structure will not be affected at all by parasitic capacitance and transfer voltage level.

4. Simulation Results and Analysis

The proposed circuit is simulated (pre-layout) using SPECTRE based on UTC (Unisonic Technologies Co., Ltd) 0.5 um HV-COMS process parameters (For low voltage device, the threshold voltages of

NMOS and PMOS are V_{thn} = 0.7619 V and V_{thp} = -0.9570 V, respectively; the electron mobility and hole mobility are u_{0N} = 861.083 cm2/V-s and u_{0P} = 568.314 cm2/V-s, respectively; the thickness of gate oxide is T_{OX} = 25 nm. For high voltage device, he threshold voltages of NMOS and PMOS are V_{thn} = 1.02 V and V_{thp} = -1.01 V, respectively; the electron mobility and hole mobility are u_{0N} = 572.7 cm2/V-s and u_{0P} = 201.35 cm2/V-s, the thickness of gate oxide is T_{OX} = 90 nm, respectively.) [23]. Both the conventional HVLS (Fig. 2) and the proposed HVLS (Fig. 9) use the same transistor parameters (channel length *L* and channel width *W*) as shown in Table 1. The inverse Schmitt trigger uses transistor configuration of Table 2.

Table 1 Transistor dimensions of HVLS

Label	**MP1**	**MP2**	**MP3**	**MP4**	**MN1**	**MN2**	**MN3**	**MN4**
W(um)/L (um)	10/1	10/1	40/3	40/3	20/1	20/1	80/3	80/3

Table 2 Transistor dimensions of inverse Schmitt trigger

Label	**MP5**	**MP6**	**MP7**	**MP8**	**MP9**	**MP10**
W(um)/L (um)	4/0.5	20/0.5	4/0.5	1/1	10/0.5	5/0.5
Label	**MN5**	**MN6**	**MN7**	**MN8**	**MN9**	**MN10**
W(um)/L (um)	2/0.5	15/0.5	2/0.5	0.5/1	5/0.5	5/0.5

The main waveforms of the conventional HVLS are shown in Fig. 11. It outputs 35V~40V signal with 0~5V input signal. The result shows that the charging speed of the inner node D (red line) is the main factor affecting transfer delay. This is in accordance with the analysis in the Sect. 2.

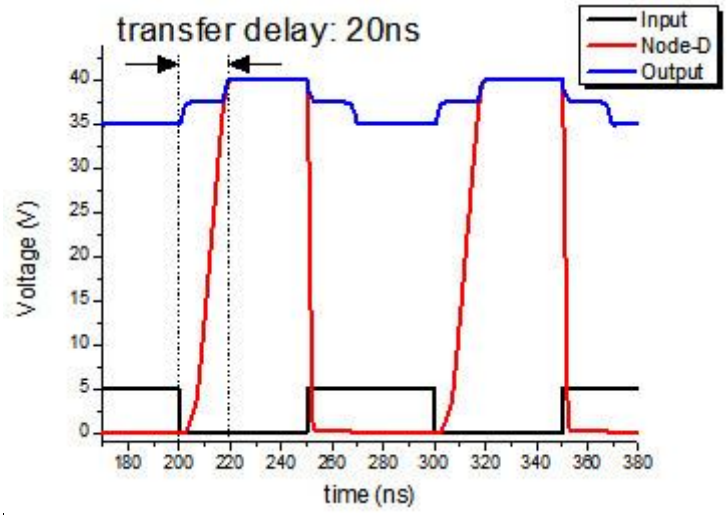
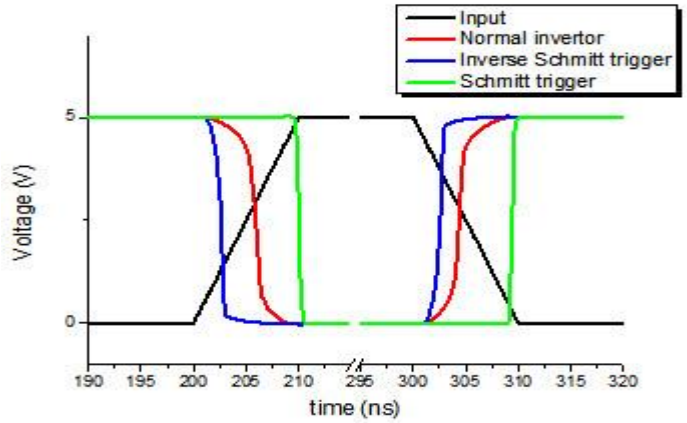
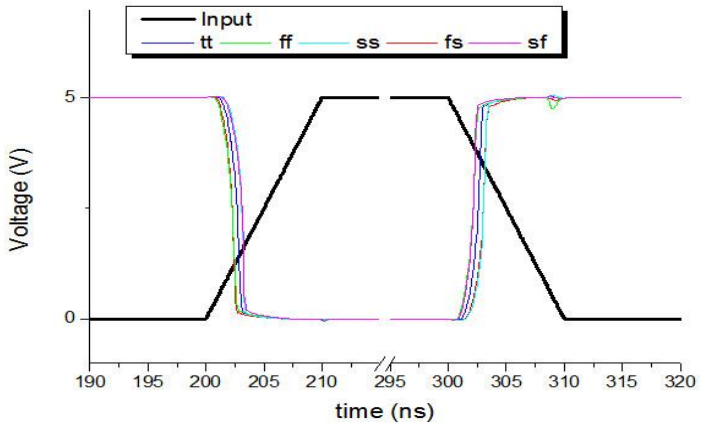


Fig. 11 The inputs voltage waveform is the one whose slew is 0-5V. The output voltage waveform is the one whose slew is 35-40V. And the Node-D voltage waveform is the one whose slew is 0-40V.

The output waveforms of normal inverter (red line), inverse Schmitt trigger (blue line) and Schmitt trigger (green line) with the same input signal (black line) are shown in Fig.12a. The result shows that, inverse Schmitt trigger has the fastest transient response at both rising-edge and falling-edge of the input signal, which is in accordance with the analysis given in Sect. 3. To verify the practicability of inverse Schmitt trigger, corner simulations are conducted under the condition of tt (typical NMOS, typical PMOS), ff (fast NMOS, fast PMOS), ss (slow NMOS, slow PMOS), fs (fast NMOS, slow PMOS) and sf (slow NMOS, fast PMOS). The results illustrate that this circuit works well in all situations, as shown in Fig. 12b.



(a)



(b)

Fig. 12 a From the left to right of X-axis. The 1st, 2nd, 3rd negative edges belong to inverse Schmitt trigger, normal invertor, Schmitt trigger, respectively. The 1st, 2nd, 3rd positive edges belong to inverse Schmitt trigger, normal invertor, Schmitt trigger, respectively. **b** From the left to right of X-axis. The 1st, 2nd, 3rd, 4th, 5th negative edges belong to ff, fs, tt, sf, ss, respectively. The 1st, 2nd, 3rd, 4th, 5th positive edges belong to ff, sf, tt, fs, ss, respectively.

The transfer delays of the conventional HVLS and the proposed HVLS are shown in Fig. 13a. The results show that compared to the conventional HVLS with the same input signal, the proposed HVLS dramatically reduces transfer delay from 20 ns to 1.3 ns under the tt conditions (typical NMOS and typical PMOS), since it removes the transfer delay caused by parasitic capacitance of inner node C/D, i.e. removes "Miller plateau" effect. The corner simulation results show that the best and worst transfer delays are 1.0ns under the ff conditions (fast NMOS and fast PMOS) and 2.8ns under the ss conditions (slow NMOS and slow PMOS), respectively, as shown in Fig. 13b.

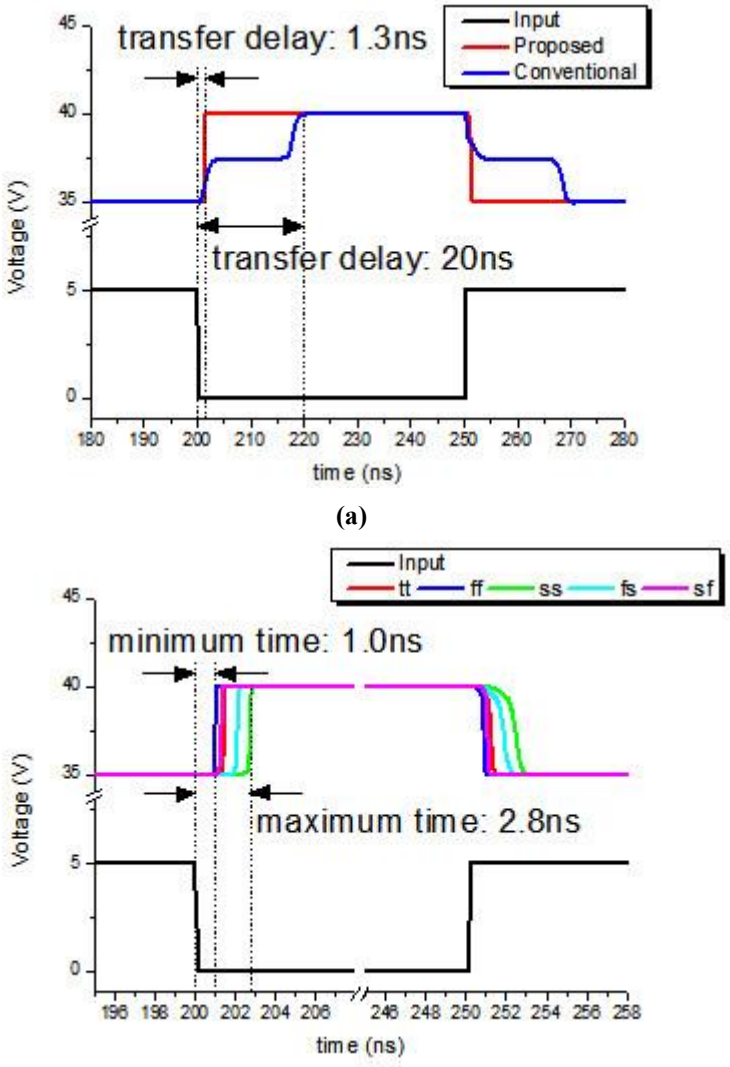


Fig. 13 Simulation results of proposed HVLS. **a** Transfer delays of conventional HVLS and proposed HVLS with the same input signal. **b** Outputs of proposed HVLS under all conditions.

As analyzed in Sect. 3, the transfer delay of the proposed HVLS is insensitive to transfer voltage level. This is also simulated, as shown in Fig. 14. The proposed HVLS has a constant transfer delay of 1.3ns under the tt conditions for a transfer voltage range from V_{DDH}=20V to V_{DDH}=100V.

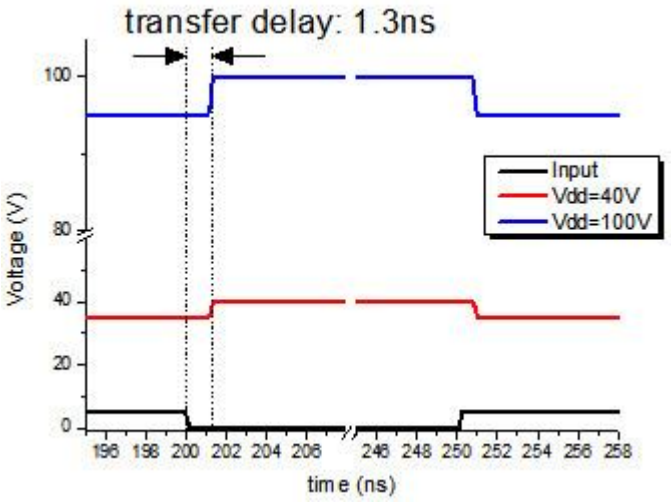


Fig. 14 Transfer delay of proposed HVLS with different transfer voltage levels

The low transfer delay leads to the reduction of power dissipation, this is also verified by the corner simulations, as shown in Fig. 15. Compared to the conventional HVLS under the same operation conditions (VDD=40V, Frequency=5MHz), the proposed HVLS achieves almost 50% reduction of power dissipation.

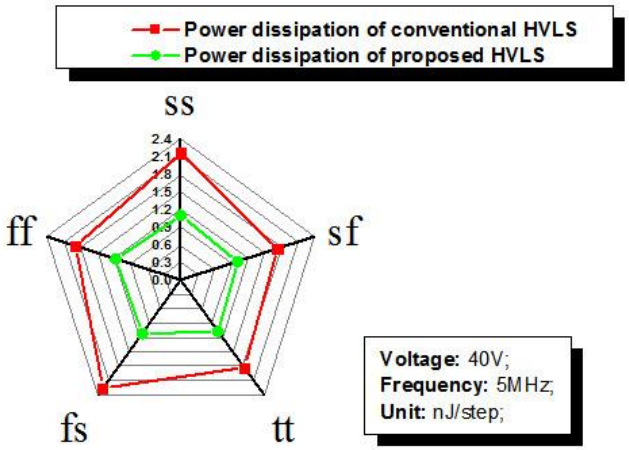


Fig. 15 Corner simulation results of power dissipation of proposed and conventional HVLS

To evaluate the overall performance of the proposed HVLS, the figure of merit (FoM) [17] is used as a benchmark, which takes into consideration of transfer delay, process note length and transfer voltage. The smaller the FoM, the faster the level shifter. Table 3 below presents the comparisons between the proposed HVLS and the relevant/similar structures with different processes and transfer voltages.

Table 3 Comparisons between this work and the relevant/similar structures in references

HVLS structure	**Process Node L (um)**	**V_{DDH} (V)**	**Delay (ns)**	**FoM: Delay/(L·V_{DDH}) (ns/μm·V)**
[7]	HV-CMOS 0.7	100	2000	28.6
[17]	HV-SOI 0.35	20	18	2.6
[18]	HV-CMOS 0.35	10	2.4	0.69
[6]	CMOS 2	75	80	0.53
[4]	HV-CMOS 0.35	25	2.5	0.29
[24]	HV-BiCMOS 0.18	50	2.5	0.28
[14]	HV-CMOS 0.35	50	2.0	0.11
[16]	HV-CMOS 0.5	40	2.0	0.10
		100	0.5	0.01(with boost cap)
[15]	HV-CMOS 0.5	100	0.5	0.01(with boost cap)
This work	HV-CMOS 0.5	20	1.0~2.8 (1.3 under the tt conditions)	0.10~0.28 (0.13 under the tt conditions)
		40		0.05~0.14 (0.65 under the tt conditions)
		70		0.029~0.080 (0.037 under the tt conditions)
		100		0.020~0.056 (0.026 under the tt conditions)

From the table, it is clear that the comparable structures are [14-16] and this work in terms of FoM, in which the order of magnitude of their FoM can reach 10^{-2}. Other structures have much higher FoM. Both [15,16] employ a technique called "bootstrapping" to improve their transient responses. Similar to this work, this technique has the advantage that the node parasitic capacitances do not have to be charged and runs with a much reduced power dissipation. However, the bootstrapping technique needs to use a boost capacitor to execute level shifter, which is normally several nano-farad (the boost capacitor used in [15] is 5nF) and has to withstand high voltage (100V in [15]), therefore consuming significant (even unacceptable in some cases) chip area. This means that considering both FoM and implementation cost, the proposed HVLS outperforms [15,16]. It is worth mentioning that the structures, such as [4,14,16,24], having reasonably low FoM (in the order of magnitude of 10^{-1}) and without boost capacitor, adopt a technique called “Pulse-triggered”. The "Pulse-triggered" technique can also significantly reduce the transfer delay and power dissipation. However, this technique uses pulse signal to execute level shifter instead of level signal. Hence, the extra pulse generator circuit is required, which not only increases complexity but also decreases reliability of overall HVLS structure.

5. Conclusion

This paper has proposed a new low delay high-voltage level shifter, which is based on inverse Schmitt trigger to significantly reduce transfer delay. Simulation results show that the proposed structure has

achieved a transfer delay time of 1.3ns without using boost capacitance, therefore saving significant chip area for implementation. Furthermore, this transfer delay bears no influence from parasitic capacitance and does not increase with change of transfer voltage level, i.e., the transient performance of the proposed HVLS structure is insensitive to parasitic capacitance and transfer voltage level. At last, the proposed structure reduces power dissipation significantly due to its low transfer delay.

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