J Comput Electron (2016) 15:1017–1022
DOI 10.1007/s10825-016-0834-1

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An improved CMOS-based inductor simulator with simplified structure for low-frequency applications

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Published online: 30 May 2016

Abstract In this paper, an improved inductor simulator structure is presented, which can be configured as either grounded or floating inductor simulator with low component count. To achieve simplified structure, inductor simulator circuits are designed using a minimal number of transistors and small capacitance, rather than the complex components/modules such as current convey and operational trans-conductance amplifier which are traditionally used. The simulation results based on 0.5 μm CMOS process parameters show that the proposed structure is able to produce a broad range of inductance values and compared to other similar structures, it provides wider operational frequency bandwidth for the same or comparable inductance value. Furthermore, the structure can be implemented with much smaller chip area using a small capacitance in the circuit, but at the price that it has a higher minimum operational frequency compared to other structures.

Keywords Grounded inductor simulator · Floating inductor simulator · Active inductor · CMOS integrated circuits · MOSFET · Operational frequency

1 Introduction

Inductance is a vital component for many analog and mixed-signal circuits and systems. Large inductances are often needed if operational frequency of a circuit is not very high, but they are difficult to be integrated into an integrated circuit (IC) due to the large chip area required. There have been a number of attempts to develop inductor simulators, which can perform the analog function of inductance [1–12]. The most commonly used structures of these inductor simulators are composed of multiple passive components and complicated operational modules such as current conveyor (CC) [2–5], current feedback operational amplifier (CFOA) [6], operational trans-conductance amplifier (OTA) [7], current backward trans-conductance amplifier (CBTA) [8] and current differencing buffered amplifier (CDBA) [9]. This is because that they attempt to achieve functional flexibility, i.e., to be reconfigured to form other circuit functions such as frequency dependent negative resistor (FDNR), while aiming at low-frequency applications. Other structures [10–12] use fewer and less complicated components to be structurally simple and to minimize the effect of parasitic parameters. However, these are primarily used for high-frequency or RF applications. In this paper, an improved structure for grounded inductor composed of only five active components and one capacitor for low-frequency applications is proposed. Compared to the structure in [1] which was proposed for the same purpose, this structure is further simplified and is able to simulate the same or comparable inductance value with smaller capacitor and wider operational frequency bandwidth. In addition, by adding only three more transistors to the structure, the grounded inductor simulator can be easily upgraded to floating inductor simulator.

The rest of this paper is organized as follows: Section 2 presents the process of designing inductor simulator. Section 3 shows simulation results and analysis of the proposed inductor simulators. Finally, conclusions are drawn in Sect. 4.

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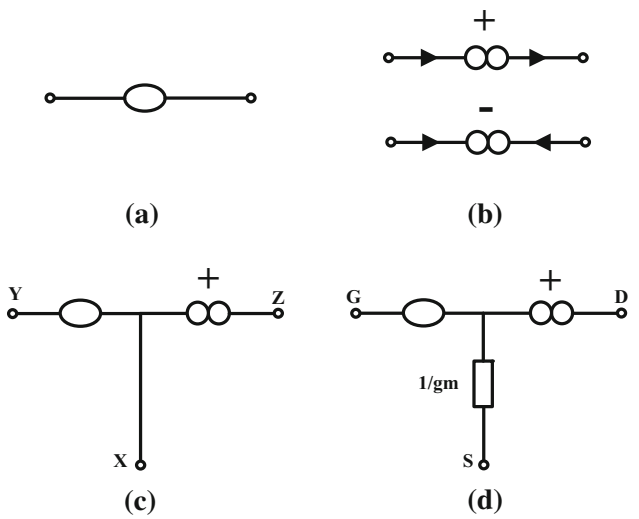

Fig. 1 **a** Nullator, **b** norator, **c** second generation current conveyor (CCII), **d** nullator–norator model of MOSFET

2 Proposed inductor simulator

To achieve simplified structure and simulate a range of inductance values at low operational frequency, MOSFET is to be used as prime component rather than CC or OTA. The design method is based on the nullator–norator technique. A nullator represents a port that has no potential difference across its two terminals and has no current flowing into or out of it, as shown in Fig. 1a. A norator represents a port that has arbitrary current flowing through and has arbitrary potential difference across its two terminals, as shown in Fig. 1b. The nullator–norator models of second generation current conveyor (CCII) and MOSFET are shown in Fig. 1c, d [5]. Figure 1 illustrates clearly the structural similarity between CCII and MOSFET, which suggests that instead of CCII, MOSFET may be used to construct an inductor simulator.

There are two key components that are used to build the proposed inductor simulator, MOSFET and capacitor. MOSFET is used to convert voltage signal into current signal. The capacitor is used to emulate voltage–current characteristic of inductor, i.e., [13]

$$Z_{\mathrm{C}} = \frac{V_{\mathrm{C}}}{I_{\mathrm{C}}} = \frac{1}{j\omega X_{\mathrm{C}}}$$
$$Z_{\mathrm{L}} = \frac{V_{\mathrm{sim}}}{I_{\mathrm{sim}}} = j\omega X_{\mathrm{L}} \qquad (1)$$

where V_{C} and I_{C} are the voltage and the current applied to capacitor, V_{sim} and I_{sim} are the voltage and the current applied to inductor, X_{C} is the value of the capacitor, X_{L} is the value of the inductor, ω is operational frequency, and j is the imaginary unit representing 90-degree phase shift. It is

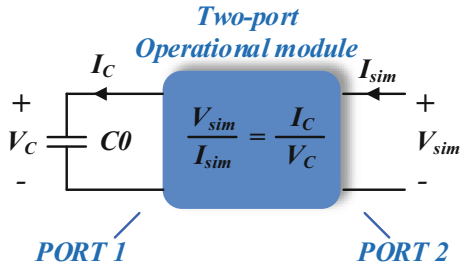

Fig. 2 Block diagram of inductor simulator

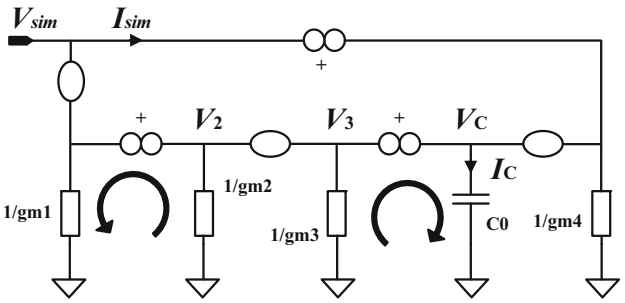

Fig. 3 Nullator–norator structure of inductor simulator

obvious from Eq. (1) that if $X_{\mathrm{C}} = X_{\mathrm{L}}$, the impedance of the capacitor is reciprocal of the inductor's impedance.

To realize simulation of inductor, an inductor simulator is constructed here using a two-port operational module, as shown in Fig. 2. One port (PORT 1) of the module connects to a capacitor $C0$. The other port (PORT 2) connects to an arbitrary external circuit. The function of this operational module is to make $V_{\mathrm{sim}}/I_{\mathrm{sim}}$ equal to $I_{\mathrm{C}}/V_{\mathrm{C}}$, so that the impedance of the simulated inductor $(V_{\mathrm{sim}}/I_{\mathrm{sim}})$ is the same as the reciprocal of the impedance of the capacitor C0. It operates as follows: Once the voltage V_{sim} is applied onto PORT 2, the current I_{C} that is proportional to V_{sim} is generated and fed into the capacitor C0 in PORT 1, therefore producing the voltage V_{C} across the capacitor. Then from the V_{C}, the current I_{sim} that is proportional to V_{C} is generated and fed back into PORT 2.

Following the working explained above, the nullator–norator structure of the inductor simulator is acquired, as shown in Fig. 3.

The relationship between the port voltage V_{sim} and the port current I_{sim} can be deduced as [14]

$$\frac{I_{\mathrm{sim}}}{V_{\mathrm{sim}}} = \frac{g_{m1}g_{m3}g_{m4}}{g_{m2}}\frac{V_{\mathrm{C}}}{I_{\mathrm{C}}} = \frac{1}{j\omega L_{\mathrm{sim}}}, \qquad (2)$$

where $L_{\mathrm{sim}} = \frac{g_{m2}}{g_{m1}g_{m3}g_{m4}}C0$ is the inductor to be simulated through the capacitor C0. By replacing the nullator–norator pairs in Fig. 3 with MOSFETs, we can obtain the grounded inductor simulator circuit, as shown in Fig. 4. The $gm1$, $gm2$, $gm3$, and $gm4$ in Fig. 3 are trans-conductances

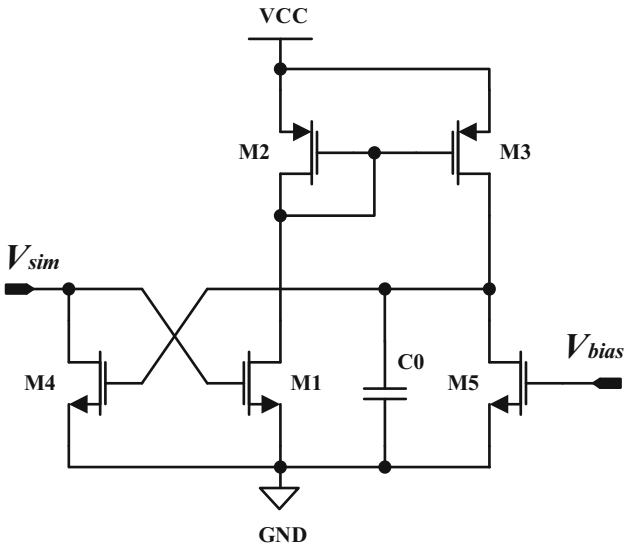

Fig. 4 Grounded inductor simulator circuit

of the MOSFETs M1, M2, M3, and M4 in Fig. 4, respectively. The MOSFET M5 is to provide a current bias for the circuit.

In order to consider the main parasitic parameters that will affect the frequency response of the circuit, Eq. (2) needs to be modified by taking parasitic capacitance and output resistance of MOSFETs into account [14], and then it becomes

$$\frac{I_{\text{sim}}}{V_{\text{sim}}} = G_m R_{\text{O35}} \frac{1}{1+j\frac{\omega}{\omega_0}} \frac{1}{1+j\frac{\omega}{\omega_1}} + \frac{1}{R_{\text{O4}}} + j\omega\left(C_{\text{gs1}} + C_{\text{ds4}}\right) \tag{3}$$

where $G_m = \frac{g_{m1}g_{m3}g_{m4}}{g_{m2}}$ is the open loop trans-conductance, $R_{\text{O35}} = R_{\text{O3}}|R_{\text{O5}}$ is the resultant resistance of the output resistance of M3 (R_{O3}) and the output resistance of M5 (R_{O5}) in parallel connection, R_{O4} is the output resistance of M4, C_{gs} and C_{ds} are the gate-source parasitic capacitance and the drain-source parasitic capacitance of MOSFET, respectively, and $\omega_0 = g_{m2}/\left(C_{\text{gs2}} + C_{\text{gs3}} + C_{\text{ds2}} + C_{\text{ds1}}\right)$ and $\omega_1 = 1/R_{\text{O35}}C0$ are the two poles of the open loop transfer function. The ω_0 is always a very high-frequency pole, which is normally negligible.

According to the conventional calculations [14], if the frequency $\omega > 10\omega_1$, Eq. (3) can be simplified as

$$\frac{I_{\text{sim}}}{V_{\text{sim}}} = \frac{1}{j\omega L_{\text{sim}}} + \frac{1}{R_{\text{sim}}} + j\omega C_{\text{sim}}, \tag{4}$$

where

$$L_{\text{sim}} = \frac{g_{m2}}{g_{m1}g_{m3}g_{m4}}C0,$$
$$R_{\text{sim}} = R_{O4},$$
$$C_{\text{sim}} = C_{\text{gs1}} + C_{\text{ds4}}.$$

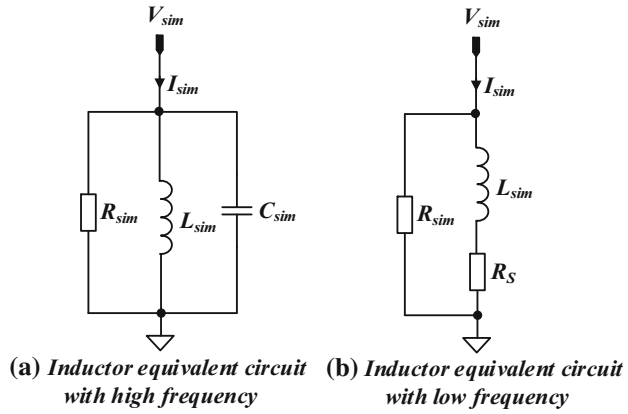

Fig. 5 Equivalent circuits of grounded inductor simulator

If the frequency $\omega < 10\omega_1$, Eq. (3) can be simplified as

$$\frac{I_{\text{sim}}}{V_{\text{sim}}} = \frac{1}{R_{\text{s}} + j\omega L_{\text{sim}}} + \frac{1}{R_{\text{sim}}}, \tag{5}$$

where

$$L_{\text{sim}} = \frac{g_{m2}}{g_{m1}g_{m3}g_{m4}}C0,$$
$$R_{\text{s}} = \frac{g_{m1}g_{m3}g_{m4}}{g_{m2}}R_{\text{O35}},$$
$$R_{\text{sim}} = R_{\text{O4}}.$$

Equations (4) and (5) mean that the circuit in Fig. 4 can be simplified to one of the two equivalent circuits shown in Fig. 5. Figure 5a shows the equivalent inductor simulator circuit operating at high frequency, which is derived through Eq. (4). Figure 5b shows the equivalent inductor simulator circuit operating at low frequency, which is derived through Eq. (5).

From Eqs. (4) and (5) as well as Fig. 5, it is easy to understand that the frequency range of equivalent circuit is determined by C_{sim} at high frequency and by R_{s} at low frequency. This is because that the C_{sim} together with L_{sim} will form a double-pole point (or resonation point), which prevents magnitude response from keeping rising up, and that the R_{s} together with L_{sim} will form a zero point, which prevents magnitude response from keeping going down. Hence, the upper and lower limits of the operational frequency are decided by the following double-pole point $\omega_{\text{D-pole}}$ and zero point ω_{Zero}, respectively:

$$\omega_{\text{D-pole}} = \frac{1}{\sqrt{L_{\text{sim}}C_{\text{sim}}}},$$
$$\omega_{\text{Zero}} = \frac{R_{\text{s}}}{L_{\text{sim}}}. \tag{6}$$

Furthermore, by replacing the V_{bias} terminal in Fig. 4 with another grounded inductor simulator, a floating inductor sim-

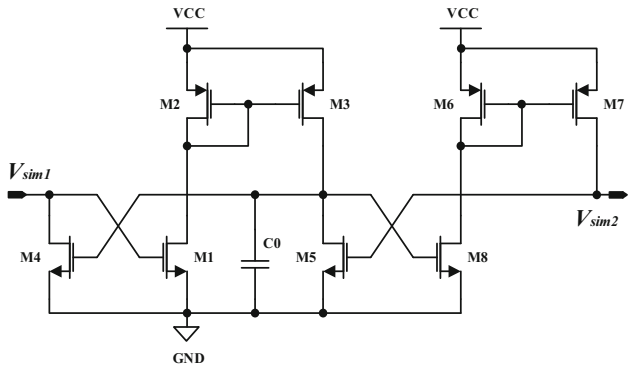

Fig. 6 Floating inductor simulator derived from grounded inductor simulator

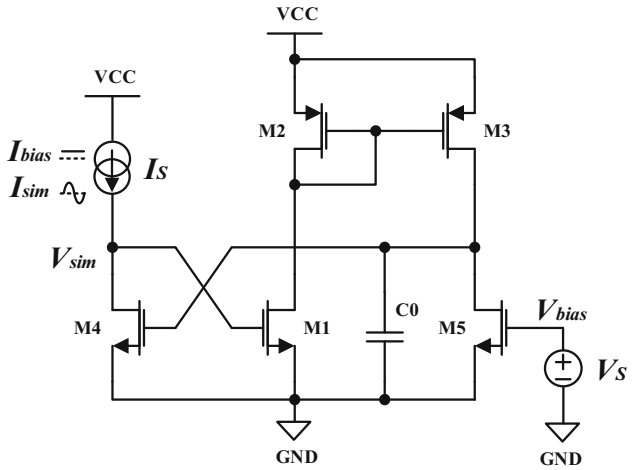

Fig. 7 Configuration for simulations of grounded inductor simulator

ulator can be acquired, as shown in Fig. 6. This floating inductor simulator has the same function and electrical characteristics as the grounded inductor simulator in Fig. 4, but it is more flexible in terms of its applications since both of its terminals can be connected to other circuits.

3 Simulation results and analysis

The circuit of Fig. 4 is simulated using the configuration shown in Fig. 7. The terminal V_{bias} connects to a voltage source V_{S} to provide DC voltage bias for the MOSFET M5. The terminal V_{sim} connects to a current source I_{S} to provide the DC current bias I_{bias} for the MOSFET M4 and to provide the AC signal excitation I_{sim} as well. The bulks of NMOS and PMOS transistors are connected to the ground GND and the power supply VCC, respectively. The simulations are performed using SPICE based on 0.5 μm CMOS process BSIM3v3 model (the threshold voltages of NMOS and PMOS are $V_{\text{TN0}} = 0.7619$ V and $V_{\text{TP0}} = -0.9570$ V, respectively; the electron mobility and hole mobility are $u_{0N} = 861.083\,\text{cm}^2/\text{V s}$ and $u_{0P} = 568.314\,\text{cm}^2/\text{V s}$,

Table 1 Simulation results of grounded inductor simulator: inductance value and operational frequency range

Circuit construction type	Component dimension/value						Testing condition		Simulation result	
	M1 W × L (μm²)	M2 W × L (μm²)	M3 W × L (μm²)	M4 W × L (μm²)	M5 W × L (μm²)	C0 (F) (p)	V_{bias} (V)	I_{bias} (μ A)	Inductance (H)	Frequency (Hz)
Type-1	2 × 10	20 × 2	2 × 20	2 × 20	2 × 20	10	1	1	57.2	15.2–70.3 k
						1	1	1	6.1	173.8–338.8 k
						1	1.25	1	1.08	1.8–870 k
						1	1.25	5	503.9 m	1.5 k–1.28 M
Type-2	10 × 2	2 × 10	2 × 10	2 × 10	2 × 20	10	2	1	35.7 m	1.2 k–2.3 M
						3	2	1	10.6 m	20.6 k–4.0 M
Type-3	2 × 2	5 × 2	5 × 2	10 × 2	2 × 2	10	1.5	25	1.5 m	79.5 k–33.1 M
						5	1.5	10	816.6 μ	150.1 k–33.8 M
						5	1.5	30	692.3 μ	158.5 k–40.7 M
						4	1.5	10	666.3 μ	225.5 k–36.3 M
						6	1.5	50	649.9 μ	114.4 k–50.1 M
						5	1.5	50	550 μ	117.5 k–57.5 M
						1	1.5	30	124.4 μ	717.1 k–33.6 M
						1	1.5	50	107.6 μ	660.7 k–37.1 M
						1	1.5	100	83.8 μ	524.7 k–47.8 M
						1	2	400	30.1 μ	1.3 M–147.9 M

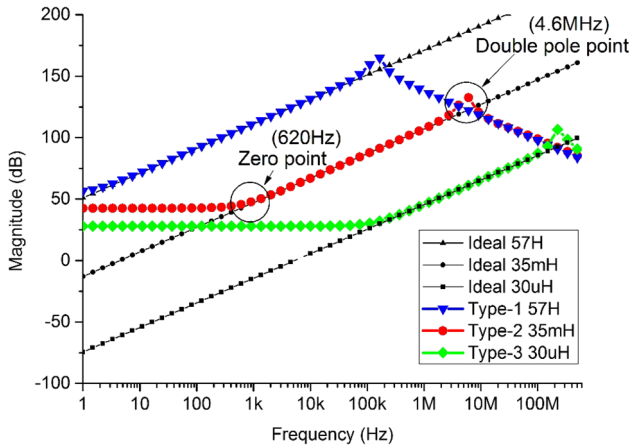

Fig. 8 Magnitude responses of each type compared to ideal inductor

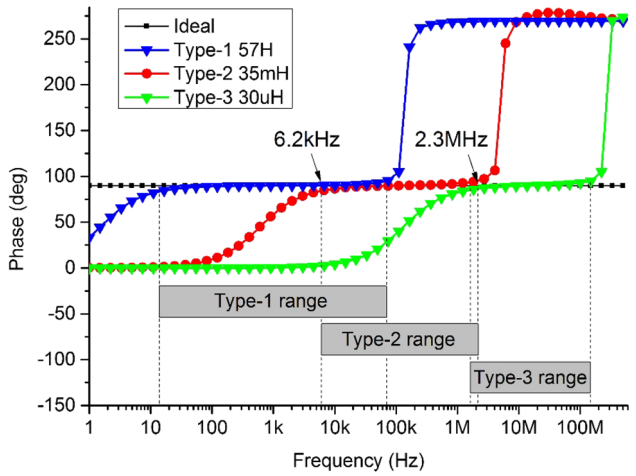

Fig. 9 Phase responses of each type compared to ideal inductor

respectively; the thickness of gate oxide is $T_{OX} = 25$ nm). The dimensions of the CMOS transistors (M1−M5) used in the implementation are given in Table 1. To test the functionality of the circuit in Fig. 4, three types of constructions of the circuit with different sizes of components (Type-1, Type-2, and Type-3) are simulated, as shown in the table, so that a variety of inductor values with their corresponding operational frequency ranges can be produced.

The floating inductor simulator in Fig. 6 has the same simulation results as the grounded inductor simulator in Fig. 4, with the transistors M6−M8 having the same dimensions as the transistors M3−M5.

From the simulation results, it is obvious that compared to an ideal inductor which has no frequency restriction, the simulated inductors work within certain limited frequency range. Taken the Type-2 (35 mH) of the circuit as an example, the magnitude responses of the frequency domain simulations in Fig. 8 show that the circuit has a zero point at 620 Hz and a double-pole point at 4.6 MHz, which are determined by R_s and C_{sim}, respectively. This is in accordance with the theo-

Table 2 Comparisons between this work and the similar structures in references

Circuit structure	Number of component (MOSFET)	Simulated inductor (H)	Operational frequency (Hz)	Area (μm^2)	Test condition (bias) and power consumption
Ref. [1]	7	9.6 m	100–100 k	10^8	2.3 mW@V_{DD} = 1.5 V
Ref. [3]	35	1.5 m	15 K–1.59M	5×10^4	–
Ref. [7]	30	22 μ	10 k–10 M	10^8	6.8 mW@V_{DD} = 3 V; I_{bias} = 50 μA
Ref. [9]	80	1	10–10 k	10^8	4.0 mW@V_{DD} = 5 V; I_{bias} = 20 μA
This work (Type-1)	5 (grounded) or 8 (floating)	1.08	1.8 k–870 k	10^4	62 μW@V_{DD} = 5 V; I_{bias} = 1 μA
This work (Type-2)		10.6 m	20.6 k–4.0 M	3×10^3	187 μW@V_{DD} = 5V; I_{bias} = 1 μA
This work(Type-3)		1.5 m	79.5 k–33.1 M	10^4	215 μW@V_{DD} = 5 V; I_{bias} = 20 μA
		30.1 μ	1.3 M–147.9 M	10^3	2.2 mW@V_{DD} = 5 V; I_{bias} = 400 μA

retical analysis of the frequency limits described in Sect. 2. The phase responses of the frequency domain simulations are given in Fig. 9, which shows that the zero point of 620 Hz and the double-pole point of 4.6 MHz yield an actual working frequency range from 6.2 kHz ($10\omega_{Zero}$) to 2.3 MHz (calculated through R_S and ω_{D-pole}).

To compare with the similar structures proposed recently [1,3,7,9], Table 2 is compiled, in which the area is calculated by only taking capacitor into account, as it consumes most of the chip area. It is assumed that 1 fF capacitance takes 1 μm^2 of chip area. The test conditions (bias) and the power consumptions under these conditions are also given.

Table 2 shows that among the similar structures compared, this structure uses the least number of MOSFETs (only 5 for grounded inductor), leading to the simplest circuit. It is capable of simulating a broad range of inductance values that are covered by all other structures. Meanwhile, for the same or comparable inductance value, its operational frequency bandwidth is much wider (e.g., for 1.0 H inductor, Type 1 of this work and Ref. [9] have a bandwidth of 868.2 Hz and 10 kHz, respectively). However, the proposed structure does not operate at as low frequency as others do (e.g., Type 3 of this work and Ref. [3] with the same inductance value of 1.5 mH have a minimum operational frequency of 79.5 Hz and 15 KHz, respectively), since it uses much smaller capacitors (no more than 10 pF) in order to significantly reduce chip area as shown in the table.

4 Conclusions

This paper describes an improved structure for inductor simulator to be used in CMOS integrated circuits for low-frequency applications. The structure features low component count and use of small capacitance, thus resulting in simplified circuit structure and much reduced chip area. The simulation results demonstrate that this structure not only can produce a broad range of inductance values but also compared to other similar structures, it provides wider operational frequency bandwidth for the same/comparable inductance value. Moreover, the structure is implemented with significantly reduced chip area using a small capacitor in the circuit, but this is at the cost of having a higher minimum operational frequency compared to other structures.

Acknowledgments This work was supported by the Fundamental Research Funds for the Central Universities of China under the Grant Number JB150222.

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