# Evaluation of the Hierarchical Temporal Memory as Soft Computing Platform and Its VLSI Architecture

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## Abstract

*A large number of real world applications, like user support systems, can still not be performed easily by conventional algorithms in comparison with the human brain. Recently, such intelligence has often been reached by using probability based systems. This paper presents results on the implementation of one such user support system, namely an intention estimation information appliance system, on a Bayesian Network as well as Hierarchical Temporal Memory. The latter is a new and quite promising soft computing platform modelling the human brain, though currently only available as a software model. A second part of the paper therefore focuses on a possible VLSI architecture for Hierarchical Temporal Memory. Since it models the human brain, communication as well as memory are of high importance for this VLSI architecture.*