

Towards Interactive Verification of Programmable Logic Controllers using Modal Kleene Algebra and KIV

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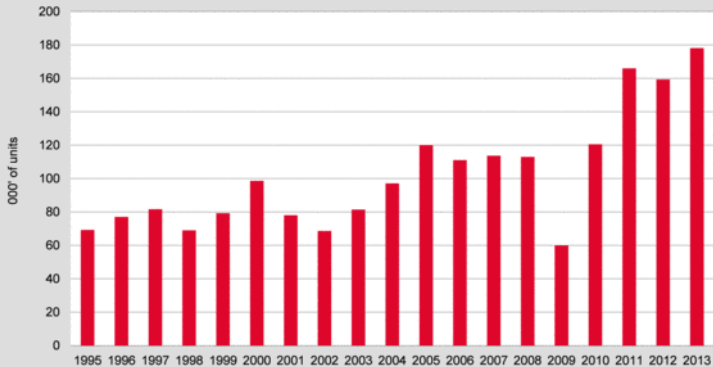


Outline

1. Introduction
2. PLC Crash Course
3. Modal Kleene Algebra and Linear Temporal Logic
4. Function Block Diagrams in Modal Kleene Algebra
5. Case Study: Mutual Exclusion
6. Conclusion and Outlook



Estimated worldwide annual shipments of industrial robots



Source: World Robotics 2014



robots are:



robots are:

- cost saving



robots are:

- cost saving
- reliable



robots are:

- cost saving
- reliable
- strong



robots are:

- cost saving
- reliable
- strong
- very strong



robots are:

- cost saving
- reliable
- strong
- very strong
- insensitive



robots are:

- cost saving
- reliable
- strong
- very strong
- insensitive
- dangerous

⇒ careful control is indispensable



PLC - Purpose and Function

- Programmable Logic Controllers (PLCs) used for controlling various plants
- robots, pumps, valves, mechanical and automated devices, ...
- PLC works in cyclic way (1 - 150 ms):
 - reads input channels (sensors, switches, internal variables)
 - computes new values
 - writes new values to associated output channels/registers (actuators, internal variables)



Data Types and Safety

- possible data types: `bool`, `int`, `float`, `date`, ...
- with usual operations (numerical, comparison, ...)
- special part for safety critical operations with reduced instruction set
- from now on only Boolean data and operations



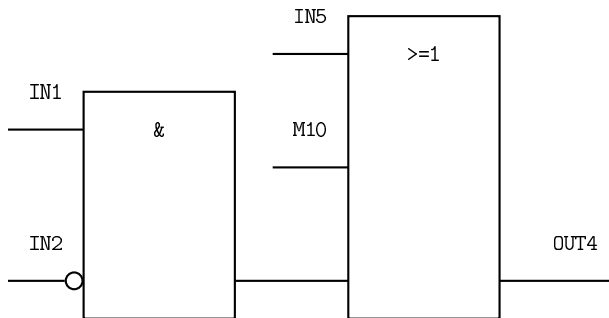
Programming Languages

Programming done via:

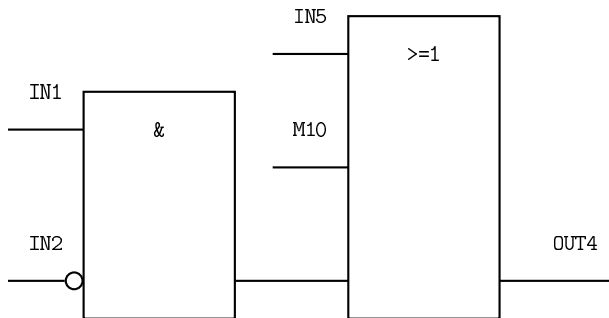
- Instruction List (IL): assembly-like
- Ladder Diagram (LD): similar to circuit diagrams
- Sequential Function Chart (SFC): inspired by state diagrams
- Structured Text (ST): resembles C syntax
- Function Block Diagram (FBD): see next



AND, OR and Negation in FBD



AND, OR and Negation in FBD



$$\text{OUT4} \equiv (\text{IN1} \wedge \neg \text{IN2}) \vee \text{IN5} \vee \text{M10}$$



Flip-Flops (Purpose and Function)

- Flip-Flops show dynamic behavior
- two inputs and one output
- TRUE-signal on set input sets output persistently to TRUE
- TRUE-signal on reset input resets output persistently to FALSE
- (until next signal on set/reset input)
- set/reset dominant depending on winner at set/reset conflict
- storing/clearing depending on input signals

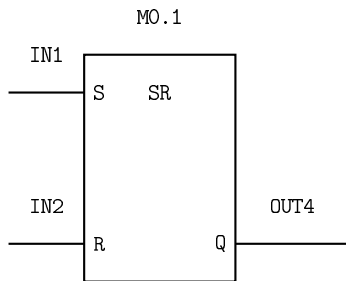


Flip-Flops (Truth Table)

S_n	R_n	Q_{n+1}
TRUE	FALSE	TRUE
FALSE	TRUE	FALSE
FALSE	FALSE	Q_n
TRUE	TRUE	TRUE (set dominant)
TRUE	TRUE	FALSE (reset dominant)



Flip-Flops (FBD)



Kleene Algebra

Definition

A *Kleene algebra* is a structure $(M, +, 0, \cdot, 1, *)$ where $(M, +, 0, \cdot, 1)$ is an idempotent semiring and $*$: $M \rightarrow M$ has the following properties:

$$1 + xx^* \leq x^*$$

$$1 + x^*x \leq x^*$$

$$x + yz \leq z \Rightarrow y^*x \leq z$$

$$x + yz \leq y \Rightarrow xz^* \leq y$$

- $+$ models choice, \cdot composition, $*$ iteration
- natural order defined by $x \leq y \Leftrightarrow_{df} x + y = y$
- examples: formal languages, relations, ...



Tests

given an idempotent semiring $S = (M, +, 0, \cdot, 1)$ subsets of M can be modeled by tests:

Definition

Given an idempotent semiring $S = (M, +, 0, \cdot, 1)$ an element $p \in M$ is called a *test* if an element $\neg p$ (the *complement* of p) exists with the properties $p + \neg p = 1$ and $p \cdot \neg p = 0 = \neg p \cdot p$.

- set of tests denoted by **test**(S)
- in relational context: subsets of identity



Boxes and Diamonds

(pre)image or (pre | post)condition modeled by diamond/box operators:

Definition

A *modal semiring* is a structure $S = (M, +, 0, \cdot, 1, |\cdot\rangle, \langle\cdot|)$ where $S' = (M, +, 0, \cdot, 1)$ is an idempotent semiring and $|\cdot\rangle$ and $\langle\cdot|$ are functions of the type $M \rightarrow (\mathbf{test}(S') \rightarrow \mathbf{test}(S'))$ with the properties $|x\rangle p \leq q \Leftrightarrow \neg q x p \leq 0 \Leftrightarrow \langle x| p \leq \neg q$, $|xy\rangle p = |x\rangle |y\rangle p$ and $\langle xy| p = \langle y| \langle x| p$ for all $x \in M$ and $p, q \in S'$.

- $|a\rangle p$: transition into p is possible
- $|a] p =_{df} \neg |a\rangle \neg p$: transition into p is inevitable



Modal Kleene Algebra

putting all together:

Definition

A *modal Kleene algebra* (MKA for short) is a structure $(M, +, 0, \cdot, 1, |\cdot\rangle, \langle\cdot|, *)$ where $(M, +, 0, \cdot, 1, |\cdot\rangle, \langle\cdot|)$ is a modal semiring and $(M, +, 0, \cdot, 1, *)$ is a Kleene algebra.



Modal Kleene Algebra and Linear Temporal Logic

work by Möller, Höfner and Struth (2006):

- model transition system by a general MKA element a
- transforming sets of traces into sets of successors
- left total function modeled by $|a\rangle p = |a]p$ for all tests p
- formulae in linear temporal logic (LTL) correspond to expressions in MKA
- LTL formula is valid iff corresponding MKA expression evaluates to 1



Explicit Correspondence

$$\begin{aligned}
 [\perp] &= 0 \\
 [\neg\psi] &= \neg[\psi] \\
 [\psi_1 \wedge \psi_2] &= [\psi_1] \cdot [\psi_2] \\
 [\psi_1 \vee \psi_2] &= [\psi_1] + [\psi_2] \\
 [\psi_1 \rightarrow \psi_2] &= [\psi_1] \rightarrow [\psi_2] \quad (p \rightarrow q =_{df} \neg p + q) \\
 [\Box \psi] &= [|a^*] \psi \\
 [\Diamond \psi] &= [|a^* \rangle \psi \\
 [\circ\psi] &= [|a \rangle \psi \\
 [\psi_1 \cup \psi_2] &= |([\psi_1] \cdot a)^* \rangle [\psi_2]
 \end{aligned}$$



Variables and Overall Behavior

FBDs in MKA:



Variables and Overall Behavior

FBDs in MKA:

- inputs/outputs/internal variables correspond to tests
- for every signal/variable p introduce two tests p_0 and p_1
- indicating a value of FALSE and TRUE, resp.
- clearly $\neg p_0 = p_1$ and $\neg p_1 = p_0$
- characterize behavior of elementary gates (OR, AND, Flip-Flops, ...)
- elementary gates do not change noninvolved signals/variables
- remember left total functionality
- write overall behavior a as product of elementary gates



Elementary Gates

- AND-gate AND_k with inputs $in_1, in_2 \dots, inn$:
 - $in_{1_1} \cdot in_{2_1} \cdot \dots \cdot inn_1 \leq |andk\rangle andk_1$
 - $in_{1_0} + in_{2_0} + \dots + inn_0 \leq |andk\rangle andk_0.$
- OR-gate OR_k with inputs $in_1, in_2 \dots, inn$:
 - $in_{1_1} + in_{2_1} + \dots + inn_1 \leq |ork\rangle ork_1$
 - $in_{1_0} \cdot in_{2_0} \cdot \dots \cdot inn_0 \leq |ork\rangle ork_0.$
- negation of s_k : switch s_{k_1} and s_{k_0}

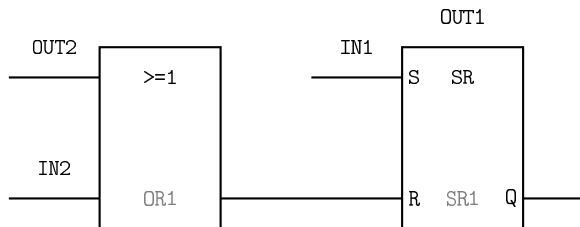


Flip-Flops

- set dominant flip-flop RSk with set input s , reset input r , output q and internal marker m :
 - $s_1 + m_1 \cdot r_0 \leq |rsk\rangle_{q_1}$
 - $s_1 + m_1 \cdot r_0 \leq |rsk\rangle_{m_1}$
 - $s_0 \cdot r_1 + m_0 \cdot s_0 \leq |rsk\rangle_{q_0}$
 - $s_0 \cdot r_1 + m_0 \cdot s_0 \leq |rsk\rangle_{m_0}$



Example Construction (not Complete!)



$$\text{out2}_1 + \text{in2}_1 \leq |\text{or1}\rangle\text{or1}_1$$

$$\text{out2}_0 \cdot \text{in2}_0 \leq |\text{or1}\rangle\text{or1}_0$$

$$\text{in1}_0 \leq |\text{or1}\rangle\text{in1}_0$$

$$\text{in1}_1 \leq |\text{or1}\rangle\text{in1}_1$$

$$|\text{or1}\rangle\text{p} = |\text{or1}\rangle\text{p}$$

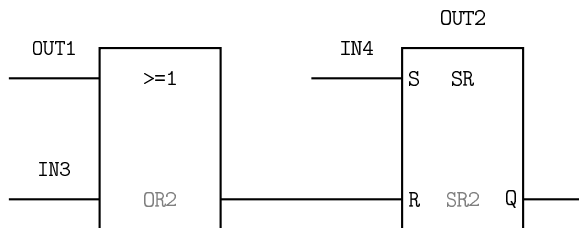
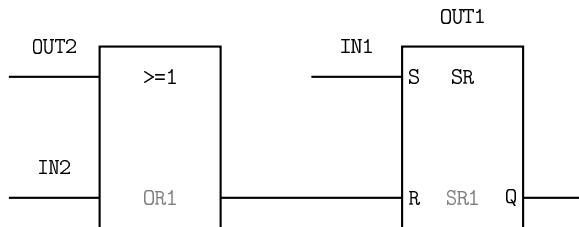
$$\text{or1}_1 + \text{out1}_0 \cdot \text{in1}_0 \leq |\text{sr1}\rangle\text{out1}_0$$

$$\text{in1}_1 \cdot \text{or1}_0 + \text{out1}_1 \cdot \text{or1}_0 \leq |\text{sr1}\rangle\text{out1}_1$$

$$\text{cycle} = \text{or1} \cdot \text{sr1}$$



Mutual Exclusion



Behavior and Desired Properties

- behavior given by $\text{cycle} = \text{or1} \cdot \text{sr1} \cdot \text{or2} \cdot \text{sr2}$



Behavior and Desired Properties

- behavior given by cycle = $or1 \cdot sr1 \cdot or2 \cdot sr2$
- desired properties in LTL:
 - $out1_0 \cdot out2_0 \rightarrow \Box (out1_1 \rightarrow out2_0)$
 - $out1_0 \cdot out2_0 \rightarrow \Box (out2_1 \rightarrow out1_0)$



Behavior and Desired Properties

- behavior given by $\text{cycle} = \text{or1} \cdot \text{sr1} \cdot \text{or2} \cdot \text{sr2}$
- desired properties in LTL:
 - $\text{out1}_0 \cdot \text{out2}_0 \rightarrow \Box (\text{out1}_1 \rightarrow \text{out2}_0)$
 - $\text{out1}_0 \cdot \text{out2}_0 \rightarrow \Box (\text{out2}_1 \rightarrow \text{out1}_0)$
- in MKA (recall $p \rightarrow q =_{df} \neg p + q$):
 - $\text{out1}_0 \cdot \text{out2}_0 \rightarrow [\text{cycle}^*](\text{out1}_1 \rightarrow \text{out2}_0) = 1$
 - $\text{out1}_0 \cdot \text{out2}_0 \rightarrow [\text{cycle}^*](\text{out2}_1 \rightarrow \text{out1}_0) = 1$



Proof Sketch

to show: $out1_0 \cdot out2_0 \rightarrow |cycle^*](out1_1 \rightarrow out2_0) = 1$



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- first: $out1_0 \cdot out2_0 + out1_0 \cdot out2_1 + out1_1 \cdot out2_0$ is an invariant of cycle



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proof sketch:

- first: $out1_0 \cdot out2_0 + out1_0 \cdot out2_1 + out1_1 \cdot out2_0$ is an invariant of `cycle`
- MKA: $out1_0 \cdot out2_0 + out1_0 \cdot out2_1 + out1_1 \cdot out2_0$ is an invariant of `cycle*`



Proof Sketch

to show: $\text{out1}_0 \cdot \text{out2}_0 \rightarrow |\text{cycle}^*](\text{out1}_1 \rightarrow \text{out2}_0) = 1$

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- first: $\text{out1}_0 \cdot \text{out2}_0 + \text{out1}_0 \cdot \text{out2}_1 + \text{out1}_1 \cdot \text{out2}_0$ is an invariant of `cycle`
- MKA: $\text{out1}_0 \cdot \text{out2}_0 + \text{out1}_0 \cdot \text{out2}_1 + \text{out1}_1 \cdot \text{out2}_0$ is an invariant of `cycle*`
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- MKA: $p \leq q \wedge qx \neg q = 0 \wedge q \leq r \Rightarrow p \rightarrow |x]r = 1$
- finish:
 - $\text{out1}_0 \cdot \text{out2}_0 \leq \text{out1}_0 \cdot \text{out2}_0 + \text{out1}_0 \cdot \text{out2}_1 + \text{out1}_1 \cdot \text{out2}_0$
 - $\text{out1}_0 \cdot \text{out2}_0 + \text{out1}_0 \cdot \text{out2}_1 + \text{out1}_1 \cdot \text{out2}_0 \leq \text{out1}_1 \rightarrow \text{out2}_0$



Proof Sketch

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 - $\text{out1}_0 \cdot \text{out2}_0 + \text{out1}_0 \cdot \text{out2}_1 + \text{out1}_1 \cdot \text{out2}_0 \leq \text{out1}_1 \rightarrow \text{out2}_0$
- proof done interactively in KIV



Conclusion

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Conclusion

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- Programmable Logic Controllers



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- Programmable Logic Controllers
- Modal Kleene Algebra



Conclusion

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- Programmable Logic Controllers
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Conclusion

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Conclusion

We saw:

- Programmable Logic Controllers
- Modal Kleene Algebra
- Linear Temporal Logic
- interactive proving with KIV
- and all working together



Outlook

We plan:



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- verification of real safety systems



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- typical features:
 - 32 - 64 signals from sensors
 - plus up to 16 signals from safety doors
 - 50 - 100 elementary gates



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 - 50 - 100 elementary gates
- characterization of other gates in MKA
- embracing numerical operations
- timer
- automated construction of input files



Obrigado pela atenção!



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atenção!**

Perguntas?

