UNIVERSITY OF OSLO
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Exploring laser induced Single Event Latch-up in AMS 0.35μm

Master thesis

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Abstract

This thesis explores different Single Event Latch-up (SEL) hardness techniques against radiation in a commercial 0.35μm technology from AMS. Techniques like increasing nMOS to pMOS distance, guard rings, source to N-well/P-substrate contact distance, increasing N-well size, source/drain diffusion area, transistor width as well as relative transistor orientation are investigated and tested to achieve a high SEL threshold. Several structures holding these techniques are made in two different options of AMS 0.35μm, one option with bulk (C35B4C3) and the other with an exitaxial layer (C35B4O1) in order to investigate the differences. The structures are based on the inverter in order to make the test structures as close to actual circuit design as possible. The inverter is also a favorable structure because it represents a worst case latch-up situation because of the parasitic components arising and the simple model needed to characterize it.

The thesis also investigates whether using a pulsed laser module is suitable to investigate SEL susceptibility in favor of a particle accelerator. The structures were exposed to infrared (1064nm) laser pulses in order to emulate high energy particles striking the ASIC. The use of laser beam with a spot size of 2μm*2μm opened the possibility to choose which structure to expose with minimum impact on the nearby structures. By increasing the energy of the laser pulses, the SEL threshold of each structure could be determined by empirical testing.

A digital input signal is propagated trough the structures in order to confirm which structure experiences latch-up. A set of switches on the PCB is used to choose which structure to monitor. The current usage of the ASIC is monitored in order to detect latch-up and to log the latch-up current.

Measurements presented a “threshold” distance between the contact and source of the transistors. If the contact-source distance is increased beyond 4.5μm the SEL threshold decreased about 70% in the epitaxial device. In the bulk device, if the contact-source distance was increased beyond 2.0μm the SEL threshold decreased to a level 12% beneath the reference structure.

The most effective structure in the epitaxial device was the structure with the N-well/P-substrate contacts placed in between the transistors. This structure presented a 30% decreased area and 87% higher threshold than the structure with the lowest threshold. Though, only 2.5% higher threshold than second place and the same area.

The most effective structure in the bulk device was the structure with

nMOS source to pMOS source distance of 7.4 μm and the minimum N-well/P-substrate contact to source distance of 0.6μm. This structure presented a 17% decreased area, a 465% higher SEL threshold and a 30% higher SEL current in comparison to the reference structure.

Preface

This thesis is submitted as part of the degree *Master of Science* in Microelectronics, to the Department of Informatics, Faculty of Mathematics and Natural Sciences, University of Oslo (UiO). The project was initiated in July 2011, and concluded the following year, May 2012.

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Introduction

Electronics designed to operate in space or other radiation hazardous environments have to be designed in order to withstand Single Event Effects (SEE). SEE occurs when a single energetic particle strikes the chip and causes either Single Event Upset (SEU) or Single Event Latch-up (SEL). SEE causes the chip to malfunction which is not tolerated in critical parts of a system.

SEUs are radiation-induced upset of a logic gate, flipping the gate from 0 to 1 or vice versa. This is a soft error and causes bit-errors and, though not causing any harm to the circuit and can be corrected by rewriting that logic gate. SEUs can cause severe problems if this occurs in a memory cell or in a microprocessor without being detected. Different design techniques as redundancy can be used to suppress SEU [2].

SEL is the radiation induced latch-up of a logic gate and occurs when an energetic particle strikes the substrate of a CMOS circuit causing a low impedance path between power and ground within the device. The latch-up condition can occur because of a P-N-P-N structure inherent in the CMOS circuits which forms a parasitic thyristor. The thyristor function as a positive feedback circuit which can be triggered by a pulse at one of the gates. If this thyristor is triggered, high currents can flow through the substrate causing excessive heating and destruction of both the chip and the bond wires by melting them. Latch-up is a self sustaining condition and power-down is the only way to recover normal operation.

One way to increase the radiation hardness of a system is by creating a physical shield around the electronic components, but this increases both mass and volume significantly. For the space industry is it therefore highly desirable to ensure an ASIC-design which can withstand radiation without any mechanical shielding.

Previous attempts [15] [23] [3] on characterizing the effect of different hardening techniques has been done by making large standardized structures. These structures represent the worst case by placing the P+ anode and the N+ cathode of the parasitic thyristor at a minimum distance from each other, creating short base widths and a high gain. The structures are also very wide (aspect ratio above 20:1) in order to neglect edge effects and mismatch effects [26]. The large structures can be exposed to both radiation and impulsed laser in order to find the least SEL susceptible structure and the most sensitive areas. In this way, different technologies can be compared to each other by these common structures.

The scope of this thesis is to characterize different hardening techniques by empirically testing them and analyze the results. By making several test structures in the AMS 0.35μm process with the different techniques of hardening a chip against SEL, empirical testing of each structure can easily be done. The test structures will be based on the minimum inverter in order to make the structures as close to actual circuit design as possible, including mismatch and the edge effects. Because the purpose of this thesis is to characterize and compare different techniques and not to characterize the technology in it self, an inverter model was preferred in favor of large standardized structures.

In this thesis we will investigate the effects of placing nMOS and pMOS at difference distances from each other in order to reduce the gain of the parasitic thyristor and thereby making the inverter less susceptible against SEL [5] [37]. Several different guard ring options as majority and minority, P+ and N+ guard rings will be investigated. The guard rings may collect some of the injected charge induced by either a particle strike, transient on one of the outputs or a laserpulse [12] [41] [13]. Inverters with different distance from the pMOS/nMOS source to well-and substrate contacts respectively will be investigated. By increasing this distance, the resistance between the source and contacts will increase and the structure may be more susceptible to SEL as shown in [20] and [8]. The effect of different sizes of the N-well will be investigated as well as the size of the drain and source of the nMOS and pMOS. At last, the effect of increasing width of the nMOS and pMOS as well as the orientation of the nMOS and pMOS transistors relative to each other will be investigated.

The same test structures will be produced in two options of the AMS 0.35μm technology, one option with bulk (C35B4C3) and the other with an exitaxial layer (C35B4O1). Publications [5], [39], [31] have reported that the use of an epitaxial layer on top of the substrate will suppress latch-up, making the structures less susceptible to SEL.

Testing ASIC's for radiation tolerance is usually performed by using a particle accelerator and exposing the whole chip for radiation. High energetic laser pulses has shown in [26] [22] [16] and [29] to be an effective tool in SEL testing and mitigation techniques. In addition to the low costs of a laser module in comparison to a particle accelerator, the precision of the laser spot plays an important role. The selectable laser spot size and precision gives the possibility to either choose which structure to expose or to scan the entire chip.

The test structures will be exposed to high energetic infrared laser beam pulses and monitored for SEL occurrence and power consumption. By varying the energy of the laser pulses, the energy threshold for SEL occurrence can be found. By comparing the different SEL threshold, one can characterize the hardness of the different structures and conclude which technique is the best alternative to use in VLSI designs. The higher laser pulse energy the structure can withstand without going into latch-up, the less susceptible the structure is to SEL. If SEL is triggered, the power

consumption is monitored in order to decide if the SEL is hazardous to the circuit or if it just causes malfunction. By basing the test structures on the inverter, the results can be directly compared to each other and a designer can easily point out which structure he wants based on the SEL threshold, latch-up current and area.

Chapter 1

Single Event Latch-up theory and explanations

1.1 Space environments and electronics

In space, radiation is emitted by the sun, stars and other high energy objects outside the earth's atmosphere. The space radiation environment is of concern for earth-orbiting satellites and for missions to other planets because of the large amount of radiation from the Van Allen belt. The Van Allen belt consist of a radiation hazard environment of various particles that may collide with devices and circuits, causing transient and permanent damage in electrical properties of solid-state devices and integrated circuits. Particles of main concern are electrons, protons, photons, alpha particles and heavier ions. When these particles strike

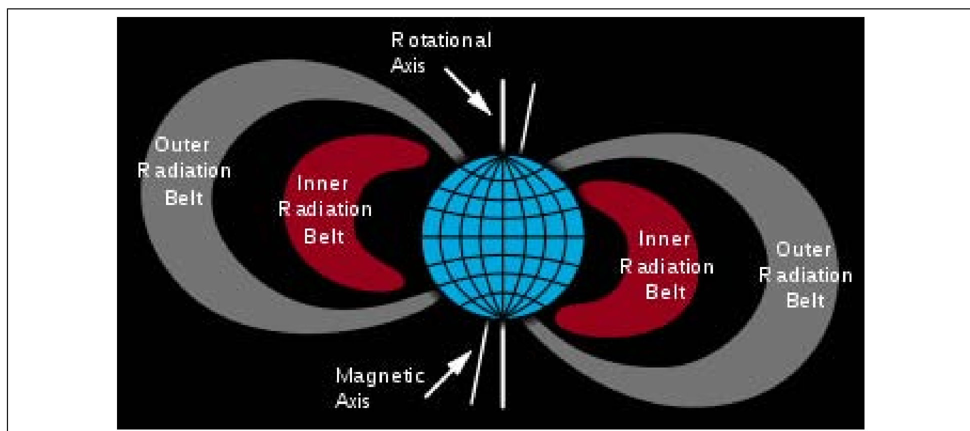

Figure 1.1: The Van Allen radiation belt [28].

the semiconductor, Single Event Effects (SEE) can occur, as well as semiconductor degradation and threshold voltage shifts. SEE is triggered by a single particle, while semiconductor degradation and threshold voltage shifts are obtained by trapped electrons and protons and continuous exposure to radiation. Because of the difficulties and high cost of repairing and replacing electronics in space, the components must be designed to withstand a certain amount of radiation.

Single Event Latch-up (SEL) is one of the SEE's triggered by a single particle and can be a destructive state. As feature sizes become smaller, the particle energies required to trigger SEL decreases, making the chip more susceptible for SEL.

1.2 Latch-up

1.2.1 Cause of latch-up

Latch-up is an undesired state where a semiconductor device undergoes a low-impedance state between power and ground as a result of interaction between a parasitic npn and pnp BJT. These two transistors occur when using both nMOS and pMOS-devices and are interconnected as a P-N-P-N structure. If a CMOS inverter is considered, this P-N-P-N-structure consists of the source (or drain) of the pMOS (P+), the N-well (N-), the P-substrate (P-) and the source (or drain) of the nMOS (N+) (figure 1.2).

Under normal operation, the middle junction of the P-N-P-N-structure is reverse biased, and the other two junctions are forward biased. Only a small leakage current will then pass trough this high impedance section. This parasitic structure forms a thyristor which functions as a bistable switch conducting when their gate receives a trigger current and conducts as long as they are forward biased. The middle pn-junction functions as the

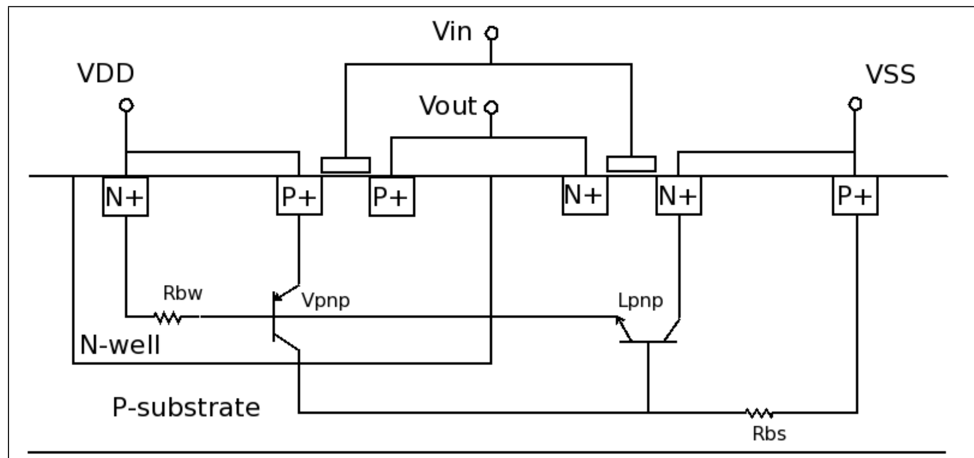

Figure 1.2: Cross section of an inverter.

thyristors gate, and is in its "off" state at normal operation. If a deviation from its normal operation causes the bipolar circuit to switch to its "on" state, a direct path between power and ground is created, allowing high currents to be established. Even if the source of the deviation is removed, the thyristor is still turned on and the circuit is still in latch-up. If these currents are not limited (by external resistors or a current-limiting power supply) they can reach orders of 0.3-3A for typical devices [23], resulting in system failure and potentially melting the device because of excessive heating. Only by powering down this thyristor (often resulting in powering down the whole chip) can normal operation be restored.

1.2.2 Description of the latch-up process

There are two ways of triggering latch-up, anode triggering and cathode triggering. The anode of the structure is the P+ source of the pMOS and by forward biasing the pn-junction formed by the P+ anode and the N-well, the vertical pnp (Vpnp) transistor within the N-well turns on. The cathode is the N+ source of the nMOS and by forward biasing the pn-junction formed by the N+ cathode and the P-substrate, the lateral npn (Lnpn) transistor that extends into the P-substrate turns on. Forward biasing of the pn-junctions is caused by a voltage drop between the anode/cathode and the N-well/P-substrate contacts respectively. This voltage drop can be caused by either transients at the different nodes (internal latch-up), or by a high energy particle strike or ESD (external latch-up) causing a current to be established. When the pn-junction is forward biased, a current is forced into the N-well/P-substrate, turning on these parasitic transistors.

The transient current needed to trigger latch-up is called the trigger current and is a way to characterize the device resistance against latch-up. The higher injected current a device can withstand without going into latch-up, the less susceptible the device is to latch-up. The trigger voltage and trigger currents are basically the same thing, the trigger voltage is the voltage induced by the trigger current over the parasitic resistance in the device. For latch-up to be sustained, a minimum voltage and current applied to the structure is needed to keep the gate of the thyristor forward biased and in a conducting state, this is called the holding voltage and holding current. Holding voltage is considered to be a good parameter in characterizing latch-up susceptibility [4]. Holding current is not so much used because most power supplies can deliver that amount of current. The higher holding voltage needed to maintain latch-up, the less susceptible the device is to latch-up. When the holding voltage exceeds the supply voltage, the design is said to be latch-up immune because latch-up cannot be maintained.

When a trigger current is applied to the structure, a negative impedance state is reached where it switches from a high resistance- low current state to a low resistance-high current state. Figure 1.3 shows the I-V characteristics between the P+ anode and the N+ cathode of a structure experiencing latch-up. Here you can see the triggering points (Vtrig, Itrig), the holding points (Vhold, Ihold) and the negative impendace region that occurs when the structure is triggered into latch-up. Here the trigger voltage is the minimum voltage needed at the anode in order to forward bias the base-emitter junction of the pnp transistor. Actually, any condition that leads to the low impedance region can trigger latch-up. The holding voltage is the minimum voltage needed at the anode in order to sustain latch-up, regardless of how latch-up was triggered.

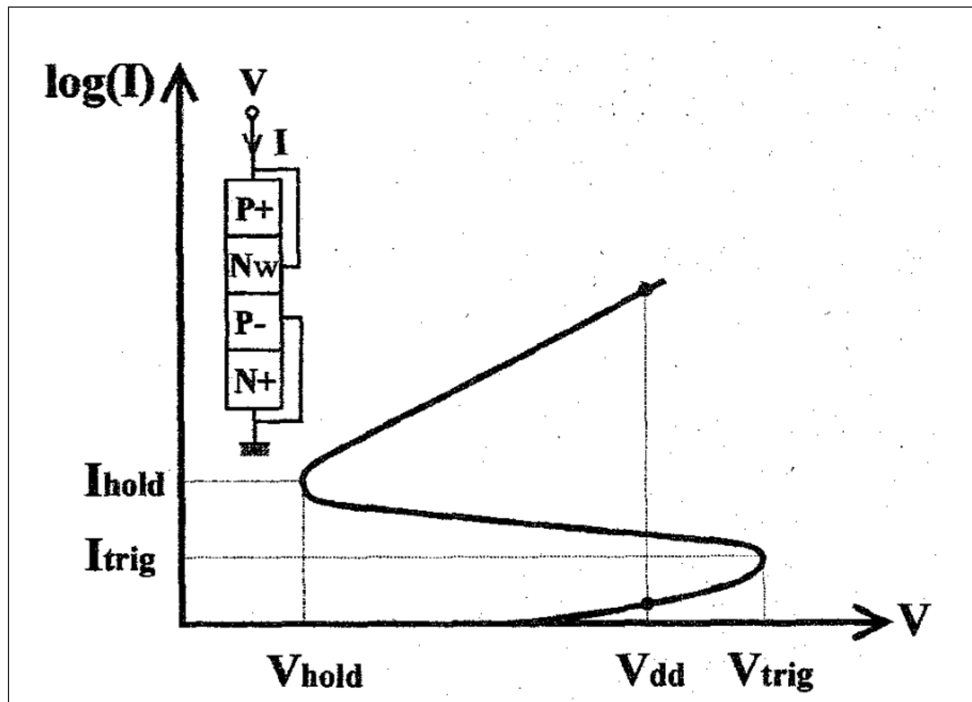

Figure 1.3: I-V characteristics of the latch-up incident[3].

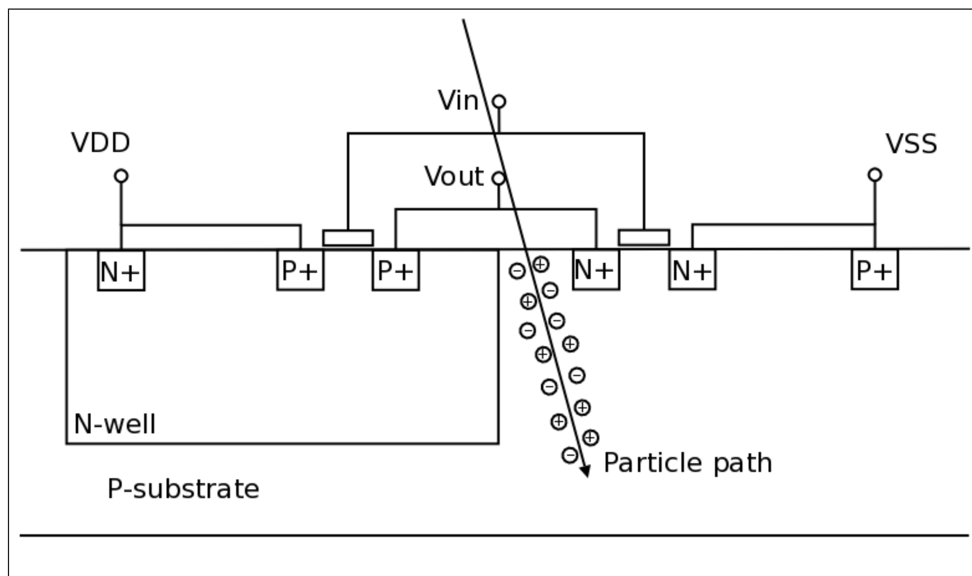

Figure 1.4: Cross section of an inverter experiencing a particle strike where free carriers are being generated.

1.2.3 Latch-up in space

In space, Single Event Latch-up (SEL) represents a major threat against integrated circuits and is triggered by a single-particle striking the semiconductor, creating free carriers. SEL can be initiated by heavy ions, cosmic rays or alpha particles creating a dense track of electron-hole pairs along a heavy ion path in silicon and is the primary reason why latch-up is a con-

cern in space applications [42]. The particle induces a transient current within the well-substrate junction flowing between the well contact and the substrate contact producing a voltage drop within the well and substrate. Depending on the location of the particle strike, the voltage drop will vary with the distance from the well contact. SEL is an external latch-up, meaning that it is caused by an external source as a particle strike, ESD occurrence or signal overshoot at the I/O pins. To avoid SEL the main object is to reduce the impact of the particle strike in the silicon or destroying the parasitic thyristor. Either by recombining or collection of the free carriers before they can reach the area of interest, or controlling the parasitic components contributing to initiate latch-up.

1.3 Two-transistor model

1.3.1 A simple latch-up model

To fully understand the latch-up phenomenon, a good point of view is the "two-transistor model". The two-transistor model is a schematic diagram of a thyristor which is obtained by bisecting the middle pn junction of the parasitic P-N-P-N-structure into two separate BJT's, the schematic can be seen in figure 1.5. The parasitic thyristor, also called a Silicon Controlled

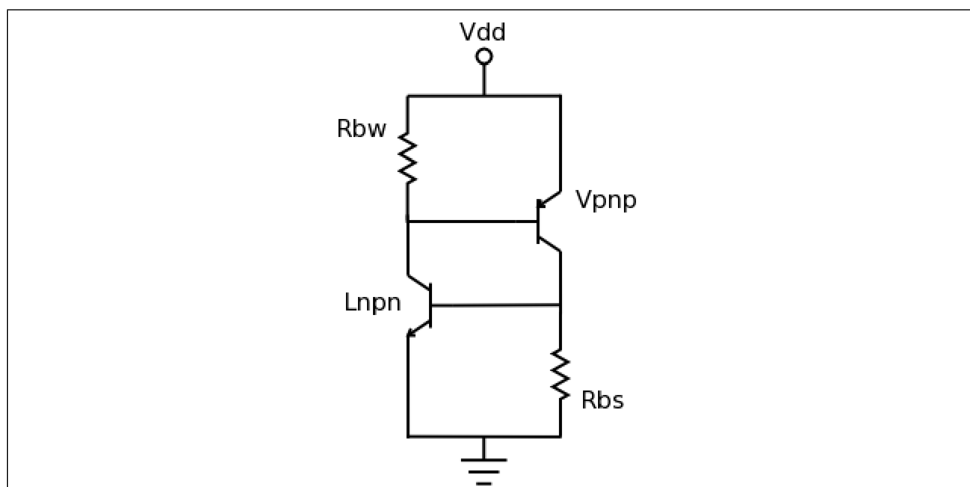

Figure 1.5: Two-transistor model

Rectifier (SCR), is consists of an npn and a pnp transistor. The npn is formed by the N+ source (or drain) of an nMOS within the substrate, the P-substrate and the N-well. The pnp is formed by the P+ source (or drain) of a pMOS within a N-well, the N-well and the P-substrate. The collector of the npn is interconnected with the base of the pnp and vice versa. If one of these BJT's gets a trigger pulse at the base node, latch-up can be initiated.

1.3.2 Triggering of latch-up

If the pnp BJT gets a trigger pulse at the base node, it starts conducting current from the P+ anode (transistor emitter) trough the N-well base

and into the P-substrate collector. If the magnitude of this collector current is high enough to create a voltage drop of about 0.7 V in the P-substrate, the base-emitter junction of the npn BJT is forward biased and starts conducting. The pnp transistor conducts current from the N+ cathode (transistor emitter) trough the P-substrate base and into the N-well collector. If the collector current of the npn transistor is high enough to maintain the forward biasing of the pnp transistor, the two BJT's are keeping each other in a conducting state. This is called a regenerative feedback loop which is the principle of a thyristor and cause of the negative impedance region in figure 1.3.

By looking at the first order equivalent model of the P-N-P-N-structure (Figure 1.5), a simplified schematic of the parasitic thyristor is presented. R_{bw} and R_{bs} models the resistance in the N-well and P-substrate respectively, and Lnpn and Vpnp models the lateral pnp BJT and the vertical npn BJT. R_{bw} and R_{bs} is determined by the distance between the anode/cathode and the N-well/P-substrate contacts respectively and how many contacts present. These resistances is shunting the base of the transistors to power and ground and is important to keep small so the transistors are kept in reverse biased conditions.

If an assumption is made that the pnp has a threshold voltage of $V_{th} = 0.7V$, the transistor cannot turn on until an injected current I_{Rw} trough the N-well resistance is high enough to create a forward voltage drop of 0.7 V. This establishes a condition given as [23]

$$I_{Rw} \cdot R_W \approx V_{th} \tag{1.1}$$

Where R_W is the resistance between the N-well contact and the location of the injected current. As mentioned, any condition or injected current that results in a negative impedance condition as shown in figure 1.3 can trigger latch-up, including ESD, signal-transients or particle strikes. The nearer the N-well contact the current is injected, the lower the voltage drop is and the less chance for latch-up to occur. The highest voltage drop occur when the current is injected near the anode (pMOS source).

1.3.3 Gain of the BJT's

The current gain (β_{pnp}) of the vertical pnp might be 50 to 100 and is determined by the thickness of the N-well [7]. The β_{npn} of the lateral npn is typically a much lower value, around 2 to 20 and is determined by the distance between the cathode and the N-well edge [23]. By keeping the gain product ($\beta_{pnp}\beta_{npn}$) of the two transistors below 1, one can achieve latch-up immunity. Because the collector current of the BJT's becomes too low to maintain a forward biased base-emitter junction of the opposing BJT, regenerative feedback cannot occur. However, with typically used spacings this product is normally greater than 1 because this assumption ignores the base-emitter resistances which impose a much higher gain product requirement. A more accurate criterion is shown in [23], assuming that a sufficient current must flow through the N-well and P-substrate to turn

on both structures;

$$\beta_{pnp}\beta_{npn} > \frac{I_A + I_{RS}\beta_{pnp}}{I_A - I_{Rw}} \tag{1.2}$$

Where I_A is the anode current, I_{RS} is the current through the P-substrate resistance and I_{Rw} is the current through the N-well resistance.

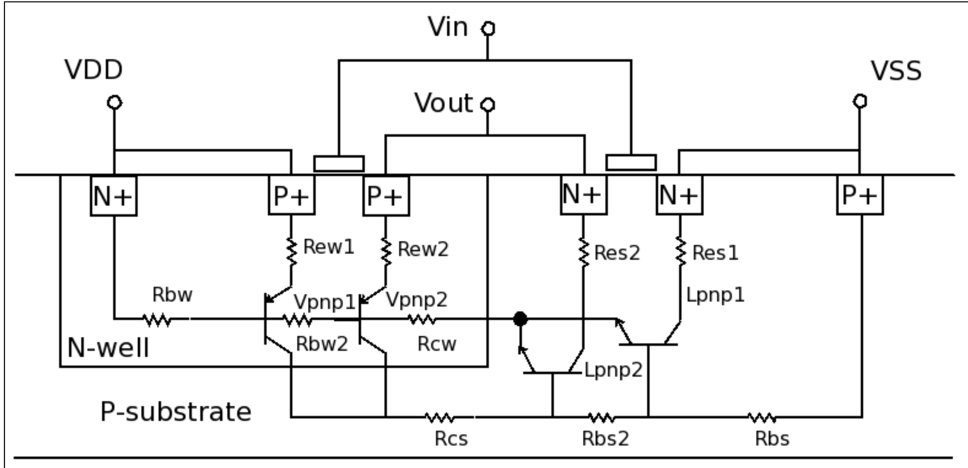

Figure 1.6: Detailed cross section of an inverter with parasitic components [3].

The current gain of a BJT is varying with emitter current (I_E) [38], in figure 1.7 you can see the normalized gain β increasing as a function of (I_E). This effect is due to recombination in the base-emitter depletion region which plays a smaller role as the current increases trough the transistor. The magnitude of (I_E) can vary between devices and can increase and decrease as structure sizes varies. When the circuit is in normal operation and the BJT's are turned off, there exists only a small leakage current trough the emitter. A large amount of this leakage current will recombine in the base-emitter depletion region, resulting in small values for β_{npn}/β_{pnp} or $\alpha_{npn}/\alpha_{pnp}$. If a high enough trigger current is applied, turning the transistors on, I_E is increased. This result in an increased β for the transistors, again resulting in an increased I_E (figure 1.7). Assuming that latch-up occurs, both the transistors are now fully turned on and their current gain is at their highest. Even if the trigger current source is removed, the structure will stay latched up because the β is now at a higher level than before they were turned on. The higher β allows the holding voltage to be significantly lower than the trigger voltage, still maintaining a low impedance high current path between power and ground. Actually, the current gain of the bipolar transistors only affects the trigger current of the structure slightly as mentioned in [18] and [36]. Only when the gain product ($\beta_{npn}\beta_{pnp}$) can be reduced below unity (or does not fulfill Eq. 1.2) a reduction in the gain is favorable when aiming for a high trigger current because of the high area penalty (see table 2.1).

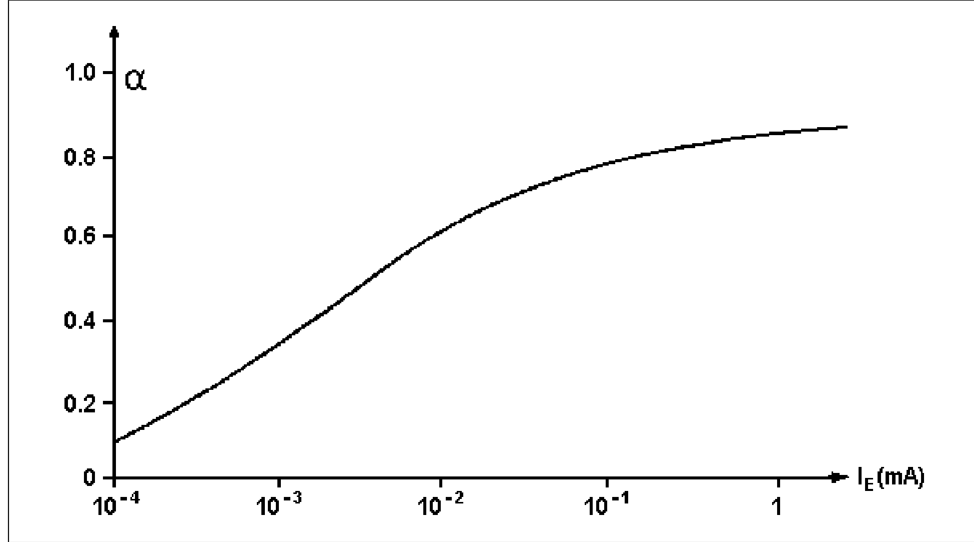

Figure 1.7: Transport factor as a function of emittercurrent[38], figure is only intended as an illustration.

1.3.4 A more accurate latch-up model

A more detailed figure of the parasitic structures arising from the inverter can be shown in figure 1.6 [3]. Here you can see that there are actually four parasitic BJT's, two pnp and two npn where one has the MOSFET drain as emitter and the other the MOSFET source as the emitter. You can also see additional resistors which represents the sheet resistance in the N-well and P-substrate. Latch-up susceptibility is dependent on all of these components which is the key to understand latch-up. The parasitic BJT's connected to the drain of the MOSFET exists only when the MOSFET is turned on, meaning that in the inverter V_{pnp2} and L_{npn2} never exists at the same time. Basically, the V_{pnp1} and V_{pnp2} as well as the L_{npn1} and L_{npn2} operates in parallel and can be simplified to one single transistor with a lower emitter resistance. When making a more detailed schematic of the cross section of a inverter, we leave out these two transistors as well as the R_{bw2}, R_{bs2} to ease some of the calculations. The resulting schematic is shown in figure 1.8, where $R_{ew} = R_{ew1} \parallel R_{ew2}$ and $R_{es} = R_{es1} \parallel R_{es2}$. Now with a more detailed figure of the parasitic components in the inverter, another way of defining the gain criterion can be derived using the transport factor (α) trough the transistors as done in [9]. The transport factor is defined as[38];

$$\alpha = \frac{\beta}{\beta + 1} \tag{1.3}$$

By using this transport factor, we can write the gain criteria as[9];

$$\frac{\alpha_{pnp} R_{bw}}{R_{bw} + R_{ew}} + \frac{\alpha_{npn} R_{bs}}{R_{bs} + R_{es}} > 1 \tag{1.4}$$

Where α_p and α_n is the transport factor of the pnp and the npn BJT respectively. Here you can see that the gain criteria can be affected by the

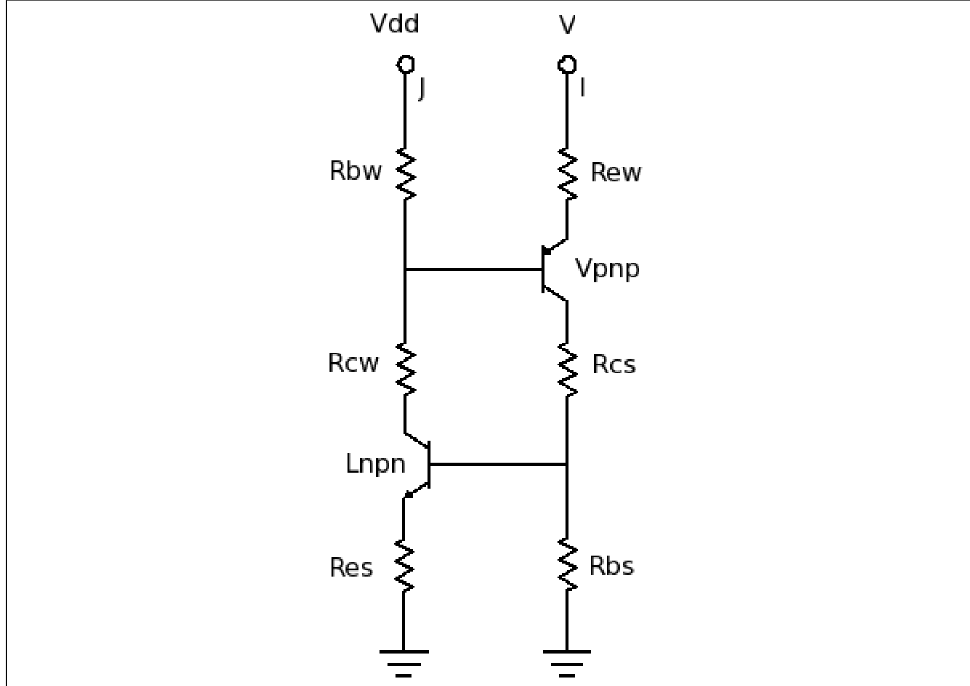

Figure 1.8: Detailed schematic of parasitic components in an inverter contributing to the latch-up malfunction [3].

parasitic resistances or the gain of the transistors. These gain criteria have to be fulfilled in order for latch-up to be sustained, if not, latch-up will die out after a period of time.

1.3.5 Triggering conditions for latch-up

Even though the gain criteria is fulfilled, latch-up still have to be triggered by an event, internal or external. Triggering of latch-up happens by turning on one of the BJT's by injecting a current to its sensitive nodes to forward bias the base-emitter junction. In order to turn on the V_{pnp} transistor, the current injected have to be high enough to create a sufficient voltage drop over R_{bw}. This current have to be higher than;

$$I_{on_{pnp}} = \frac{V_{th_{pnp}} + V_{Rew}}{R_{bw}} \tag{1.5}$$

where V_{Rew} is the voltage drop over the emitter resistance of the pnp BJT. This leads to a triggering voltage of [3]

$$V_{trig} = Vdd - V_{th_{pnp}}(1 + \frac{R_{es}}{R_{bw}}) \tag{1.6}$$

at the base node of the pnp BJT.

In order to start the regenerative feedback loop, the collector current of the V_{pnp} have to be high enough to forward bias the base-emitter junction of the L_{npn} transistor. The trigger current at the base of the V_{pnp} then have

to be higher than a critical value of [14]

$$I_{trig_{pnp}} \cong \frac{V_{th_{pnp}} + V_{Rew}}{R_{bw}} + \frac{V_{th_{npn}} + V_{Res}}{\beta_{pnp} R_{bs}} \tag{1.7}$$

to create a large enough collector current. In order to trigger latch-up by turning on the L_{npn} transistor, the same counts for the trigger current at the base of the L_{npn}. The trigger current at the base of the L_{npn} then have to be higher than a critical value of [14]

$$I_{trig_{npn}} \cong \frac{V_{th_{npn}} + V_{Res}}{R_{bs}} + \frac{V_{th_{pnp}} + V_{Rew}}{\beta_{npn} R_{bw}} \tag{1.8}$$

to reach a collector current large enough to forward bias the V_{pnp} transistor. Eq. 1.7 and 1.8 presents the trigger current needed to induce latch-up by turning on the pnp and npn transistor. The N-well sheet resistance is about 3 orders of magnitude higher than the P-substrate sheet resistance in the AMS 0.35μm technology, and the gain of the pnp is usually higher than the npn [7]. This will result in a lower trigger current for the pnp transistor even though R_{ew} is twice the magnitude of R_{es}. Eq. 1.4 - 1.8 shows the effect of the parasitic resistances and their effect on the trigger current and trigger voltage. By reducing these resistances in the well and substrate, the current needed to trigger latch-up is significantly increased. In addition to increasing the trigger current, a reduction in R_{bw} and R_{bs} as well as an increment in R_{ew} and R_{es} will increase the trigger voltage in some manner. But an increase in R_{ew} and R_{es} will also increase the source-resistance of the MOSFET, which is not desirable.

1.3.6 Holding conditions for latch-up

The holding current is also a parameter to take into account when designing for latch-up immunity, but has a minor effect on SEL because the circuit will often have a power supply that can deliver far greater currents than the holding current[23]. The holding current is often considered a measure for DC immunity and cannot account for the hardness against the triggering latch-up. For this reason the holding voltage is chosen as an additional measure for SEL immunity. The holding voltage (V_{hold}) is the minimum voltage needed across the P-N-P-N structure when latch-up is initiated and is a key metric to gain latch-up immunity[3], [23]. The holding voltage can be roughly calculated from the schematic in figure 1.8 [36];

$$V_{hold} = max(V_1, V_2) \tag{1.9}$$

$$V_1 \approx I_{Res}(R_{es} + \alpha_{npn} R_{cw}) + I_{Rew} R_{ew} + V_{th_{pnp}} \tag{1.10}$$

$$V_2 \approx I_{Rew}(R_{ew} + \alpha_{pnp} R_{cs}) + I_{Res} R_{es} + V_{th_{npn}} \tag{1.11}$$

Where I_{Res} and I_{Rew} is the current passing trough the respective resistances R_{es} and R_{ew} when the latch-up current is just above the holding current. Eq. 1.10 and 1.11 is only intended to be a simple illustration of which parameters the holding voltage depends on, the holding current is therefore not derived in this thesis, but can be found in [36]. Whether V_1 or V_2 is the larger of the two depends on the structure layout and the relationship between the different parasitic components. If V_1 is the largest, the npn transistor will be saturated while the pnp transistor will be in the active mode. If V_2 is the largest, the pnp transistor will be saturated and the npn will be in the active mode. The transistor in active mode typically saturates at a higher current level [36].

1.3.7 Latch-up current

When the latch-up condition is initiated, the total equilibrium current trough the structure is primarily determined by the external parasitic and the transport factor of the BJT's [23]. A rough approximation of this current can be drawn from figure 1.8;

$$I_{tot} = \frac{VDD \cdot \alpha_{pnp}}{R_{ew} + R_{cs} + R_{bs}} + \frac{VDD \cdot \alpha_{npn}}{R_{bw} + R_{cw} + R_{es}} \tag{1.12}$$

This approximation does not take into account the resistances of the external parts. This can be the resistance of the metal wiring on the chip, the bonding wires and the power supply.

1.4 nMOS and pMOS spacing, theory

The goal of increasing the nMOS-pMOS spacing is to increase the trigger current, making the inverter less susceptible to SEL. By placing the nMOS and pMOS a further distance from each other, the anode-cathode (pMOS source to nMOS source) distance is increased and the width of the diffusion (BJT base) is increased. As explained earlier, β_{npn} and β_{pnp} are decided (among other parameters) by the distance between the anode and the cathode of the P-N-P-N structure and the width of the diffusion. By decreasing the β (or the α) of the BJT's, the triggering current (see Eq. 1.7 and 1.8) will increase, but the holding voltage (see Eq. 1.9, 1.10 and 1.11) will actually decrease in a small manner. As a result of increasing anode-cathode spacing, the latch-up current will also decrease as can be seen in Eq. 1.12, making a latch-up event less dangerous for the circuit. If the distance is increased enough, the gain product of the transistors will eventually decrease to a level where it does no longer fulfill Eq. 1.2 and 1.4, making the structure immune to latch-up.

1.4.1 Manipulation of β

$$\beta = \frac{D_n N_D L_p}{D_p N_A W} \cong 2.5 \frac{N_D L_p}{N_A W} \tag{1.13}$$

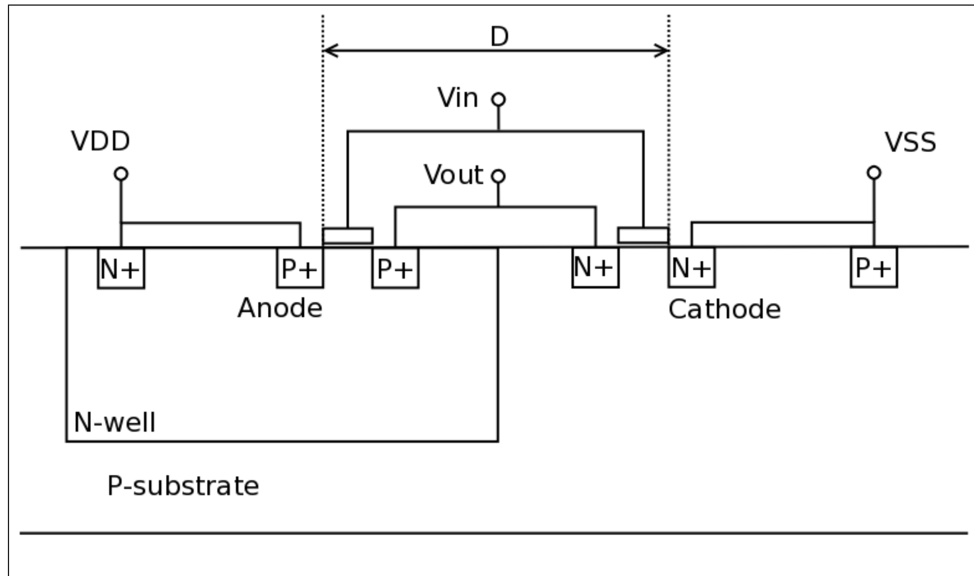

Figure 1.9: Cross section of an inverter, "D" pictures the distance between the anode and cathode of the parasitic thyristor.

N_D is the doping consentration in the donor, N_A is the doping concentration in the acceptor, D_n and D_p is the mobility to the N and P material respectively. L_p is the diffusion length of holes in the n-side, L_n is the diffusion length of the electrons in the p-side and W is the width of the base.

The derivation of β just presented [7] ignores many second-order effects that make β dependent of voltage and current [38], but the expression shows the dependence of length and width variations.

Because an ASIC-designer is not able to affect the doping concentration mobility of a process or the diffusion depth, the only parameters left to adjust is the length and width of the diffusion. To make diffusion length shorter, a possibility is to reduce the width of the nMOS and pMOS, but this is not preferred because it affects the circuit performance. By increasing the distance between the nMOS and pMOS, and thereby increasing the distance between the anode and cathode, the diffusion width of the BJT is increased and thereby decreasing the β. This is a safe and effective way to decrease the gain of the lateral npn transistor, but it has very little effect on the vertical pnp because the width of the pnp is basically decided by the N-well depth [23]. This technique is also very area demanding because of the empty space left in between the nMOS and pMOS. This area can be used to implement resistors and routing. It can not be used to implement any other nMOS or pMOS transistors because then you create a new anode or cathode closer to the anode/cathode already present.

1.4.2 Manipulation of α

In a BJT, the collector current is the minority carrier current injected into the base from the emitter, minus the any losses due to recombination

during diffusion [38]. The transport factor α is the relationship between the current injected into the base from the emitter and the current collected by the collector.

$$\alpha = \frac{\text{current collected by collector}}{\text{current injected by emitter}} = \frac{1}{\cosh\left(\frac{W}{L}\right)} = \frac{\beta}{\beta+1} \tag{1.14}$$

By studying Eq. 1.14 [38], one can see that α increases with increasing diffusion length L, and decreases with increasing diffusion width W. To avoid latch-up, the current traversing from the emitter of the parasitic transistor to the collector have to be kept to a minimum to avoid forward biasing of the other parasitic transistor and regenerative feedback to be induced. By this, the transport factor α have to be reduced because the collector current is decided by:

$$I_c = I_e \cdot \alpha \tag{1.15}$$

By increasing the anode to cathode spacing, we expect a small increase in SEL threshold ([18], [36]) as the spacing increases and total immunity as a result of the decreasing β product (Eq. 1.13) drops below unity (does not fulfill Eq 1.2). A decrease in latch-up current is also expected as a result of decreasing α in Eq. 1.14, see Eq. 1.12.

1.5 Guard rings, theory

The goal of inserting guard rings is to provide protection against SEL by collection of free carriers and biasing of the N-well/P-substrate.

Guard rings serve the purpose of providing electrical and spatial isolation between adjacent circuit elements, both preventing crosstalk between digital and analog circuits and interaction between devices and circuits that may undergo latch-up [41]. The guard rings collect the injected minority or majority carriers preventing them from interacting with the sensitive parts of a circuit, also called victims. They also prevent regenerative feedback from occurring between the pnp and npn because of the spatial separation, meaning a decrease in the feedback gain by reducing the parasitic current gain of the BJT's. When electron-hole pairs are generated in the silicon, the electrons (and holes) contribute to create a current (I_{inj}). Some of these electrons will recombine with holes before they do any harm, but the rest will be collected by the positively biased N-well. The more electrons collected by the N-well, the larger the current trough the N-well resistance I_{R_w}. If this current generates a sufficient voltage drop over R_w, the pn-junction between the P+ source of the pMOS and the N-well will forward bias and latch-up can be triggered (see Eq. 1.1.

1.5.1 Guard ring types

By placing an N+ Guard Ring (NGR) around the device located in the N-well, the guard ring will collect some of the free electrons (I_{inj}). By placing

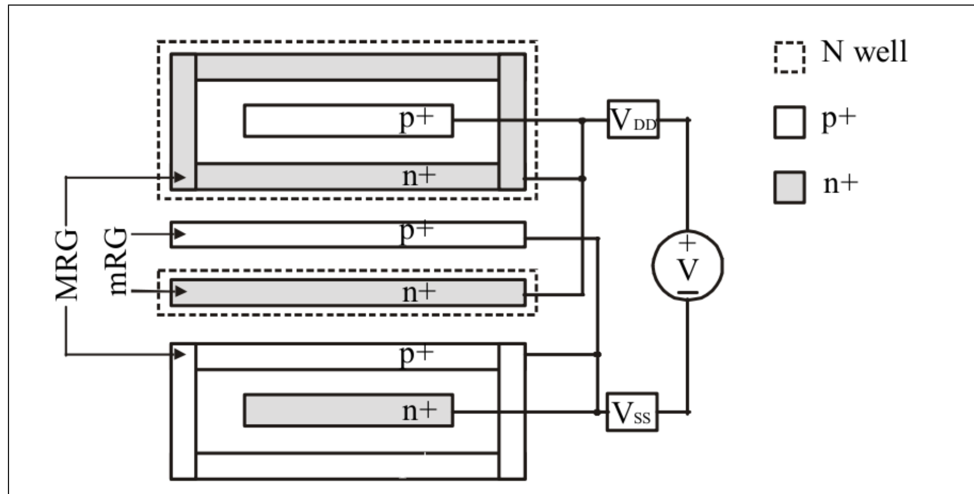

Figure 1.10: Majority (MRG) and minority (mRG) guard rings [15]

the NGR inside the N-well, making it a majority carrier NGR (MNGR), it will collect the electrons entering the N-well where they flow as majority carriers. By placing the NGR in a separate N-well surrounding the N-well device, it will collect the electrons flowing as minority carriers in the P-substrate before they are collected by the N-well, making it a minority carrier NGR (mNGR). The same apply for the P+ guard ring (PGR), placed around the device located in the substrate.

In a single N-well process the MPGR is placed at the border of the N+ device located in the substrate, while the mPGR is placed outside the border of the N+ device located in the substrate (figure 1.10)[15], or at the border of the P+ device. Majority carrier guard rings are also called integrated guard rings, while the minority carrier guard rings are called a separate guard ring [42].

When internal triggered latch-up is the problem, the main focus is to decrease the regenerative feedback between the parasitic pnp and npn transistors. By placing the guard rings in between the nMOS and pMOS the physical length between the structures increase, which lead to a decrease in the gain of the BJT's. The guard rings does not have to be actually rings, but they can take many shapes as long as they are placed in between the transistors and serve their purpose by electrically decoupling the BJT's.

When designing to protect against external triggered latch-up, the guard ring also acts as electrical isolation between the region of current injection and the sensitive region. When current injection is generated by a particle strike, the location of the injection is random and can be initiated at any place around and inside the P-N-P-N-structure. When minority carriers are injected into the semiconductor in the form of electron hole pairs generated by radiation, they diffuse to either VDD or VSS creating a current. This current has the potential to induce latch-up if the magnitude of the current is high enough to forward bias one of the parasitic transistors. The guard rings have to be placed around the sensitive regions or around an entire circuit to prevent the minority carriers from entering and inducing

latch-up. The guard rings are collecting the minority carriers before they can reach the sensitive regions of the circuit, and are biased to either power or ground depending on the sensitive region as explained earlier.

1.5.2 Guard ring design and effectiveness

For the guard rings to be effective in the collection of the extra injected carriers, it is important to reduce the resistance of the guard rings. The resistance has to be low enough to allow for large currents to be collected without loosing its effectiveness caused by the voltage drop. If the resistance is too high, the voltage drop within the guard ring can lead to a de-biasing of the guard ring [34].

The effectiveness of a guard ring depends on many variables, some the designers have control over and some are determined by the technology or process used. Which variables the designer have control over can vary between foundries and technologies. In the AMS 0.35μm technology, the designer can control the width of the guard rings, the shape and placement, the resistance from the guard rings to ground or power and guard ring contact densities. Variables the designer does not have control over (in AMS 0.35μm) are the depth of the guard ring, the sheet resistance of the guard ring and the substrate doping conditions. The effectiveness of a guard ring structure can be evaluated from a probability view. When electron-hole pairs are generated, the holes or electrons are either collected by the guard ring or they escapes and can be collected by the victims. The probability that an electron or hole escapes plus the probability that it is collected equals one [41].

$$P(collected)+P(escape) = 1 \tag{1.16}$$

The more electrons or holes collected by the guard ring the more efficient it is preventing the injected charge from reaching the sensitive parts of the circuit. Another way of defining the efficiency of the guard ring is the collection ratio metric [41].

$$F = I_{Collected} / I_{Injected} \tag{1.17}$$

If all the injected charge is collected by the guard ring, the collection ratio would equal unity, normalized to the injected charge. If the amount of collected charge decreases, the factor F decreases. This decrease is a measure of the efficiency of the guard ring to collect the charge trying to get pass and into the region of interest. In both cases the purpose of the guard rings are to reduce the effectiveness of charge carrier transport from the injection location to the nMOS or pMOS source by recombination, collection and spatial separation. This increases the maximum injected current before latch-up is triggered, even though the trigger current of the structures is the same. By dividing the trigger current with the collection ratio of the guard ring, the maximum injected current before latch-up is triggered can be calculated;

$$I_{Injected} = \frac{I_{trig}}{F} \tag{1.18}$$

The relationship between the injection of carriers and the collection of carriers can in general be seen as a bipolar transistor itself. There exists an emitter of carriers and a physical region which transports the carriers to a collector. A bipolar transistor is a minority carrier device, and there is an efficiency in the transport of the minority carriers between the emitter and collector (this is described earlier as the transport factor α). When a guard ring is present in CMOS, there exists two collectors, the guard ring it self and the source of the MOSFET. To prevent the source of the MOSFET to collect the carriers, the conductance of the guard ring have to be high in relationship to the MOSFET-source. Described in another way, the α between the emitter and the guard ring should be as high as possible, but the α between the emitter and the MOSFET-source should be as low as possible. To accomplish this, the resistance between the physical region (the base), trough the guard ring and to power or ground have to minimized as mentioned.

1.6 N-well and P-substrate contact placement, theory

By placing the N-well and P-substrate contacts a further distance away from the MOSFET source, SEL susceptibility is expected to increase as a function of increasing contact-source distance. The goal is to explore and characterize this effect.

When electron-hole pairs are generated from particle-strike, majority carrier currents flowing trough the well or substrate, causing voltage drops may forward bias the npn and pnp transistors. The resistance trough the N-well (R_{bw}) and the P-substrate (R_{bs}) seen in figure 1.2 and figure 1.5 must be reduced to reduce this voltage drop. Because when a sufficiently high potential drop is reached over one of these resistances, the corresponding transistor turns on. If the N-well potential drops more than approximately 0.7V beneath the anode of the structure (source or drain of pMOS), or the anode potential rises approximately 0.7V over the N-well the pnp transistor will be turned on. The same applies for the P-substrate, if the potential of the P-substrate is raised approximately 0.7V above the cathode of the structure (source or drain of the nMOS), or the cathode drops more than 0.7V beneath the P-substrate, the npn transistor will be turned on.

If the resistances of the substrate and wells are reduced, a higher transient current (trigger current) must be generated to cause a sufficient voltage drop and forward bias the emitter-base junctions of the npn and pnp transistors [31]. In Eq. 1.7 and 1.8 you can see that a decrease in R_{bs} or R_{bw} allows a higher trigger current (I_{trig}) and thereby (Eq. 1.18) a higher injection current I_{Inj}, before the threshold voltage between the base and the emitter of the BJT is reached.

1.6.1 Estimation of the shunting resistances

The resistance values of R_{bw} and R_{bs} are determined by the spacing ("D" in figure 1.11) between the anode/cathode and the contacts to power/ground respectively. The resistance value can be roughly estimated by counting the number of squares from the anode/cathode to their respective contacts. Sheet resistances are quoted in ohms per square (Ω/□). The "square" is used to denote that the resistance from one side of a square to the other will be the same regardless of the size because the width and length have compensatory effects on the resistance across. The fewer squares between the anode/cathode and the respective contacts, the lower resistance obtained.

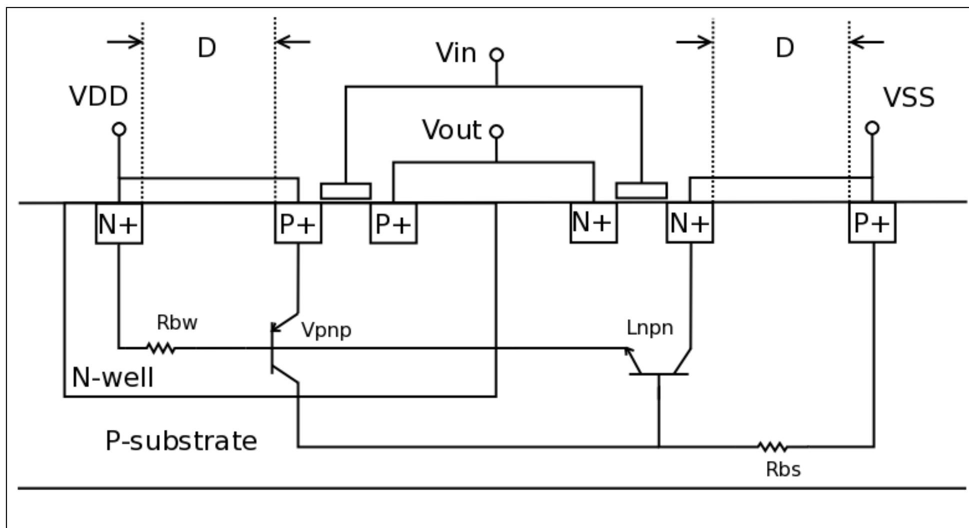

Figure 1.11: Cross section of an inverter with distance "D" between the transistor source and the respective contacts.

It is possible to calculate the maximum resistance allowable to withstand the highest transient current assumed to be generated by particle strikes, and calculate the maximum distance to the contacts. This, on the other hand, is a complex operation because the sheet resistance is a function of temperature and varies from wafer to wafer and the effects of current crowding. It is also difficult to control exactly where the transient currents move in the substrate and in the well.

1.6.2 Multiple contacts and butting

When multiple contacts are used, the resistance values are decreased because of the parallel coupling between anode/cathode and the contacts, decreasing the N-well and P-substrate resistance. In addition to the N-well and P-substrate resistance is the resistance in the contacts. The resistance of the contacts may be of high significance at short source-contacts distances, and the use of multiple contacts will reduce this resistance because of the parallel coupling between them. This is a way to

make the structure even less susceptible to SEL when the source-contacts distance is at a minimum.

It will always be an advantage to place the contacts as near the transistors as possible to obtain the best bias conditions. One technique is butting the respective contacts to the source of the transistors which reduces the resistance significantly. Butting is basically to place the contacts right next to the respective source without any N-well or P-substrate in between them as shown in figure 1.12. This technique shows

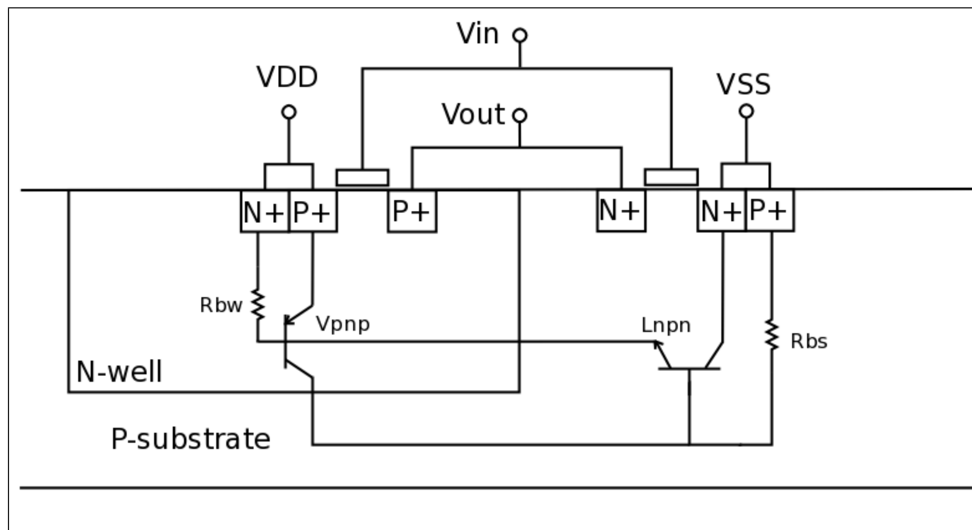

Figure 1.12: Cross section of an inverter were the transistor source is butted with the respective contacts ("D" is 0).

to be very effective in [20], but can be area consuming if every transistor are to be butted with a N-well or P-substrate contact.

1.7 N-well and diffusion size, theory

The goal is to explore and characterize the effect of increasing N-well and diffusion size on SEL susceptibility.

1.7.1 N-well size

The gain of the parasitic pnp BJT is mainly decided by the N-well depth [23], which is not possible for the designer to influence in the AMS 0.35μm technology. Though the area of the N-well is in the hands of the designer and the physical size of the N-well may play a role when designing for SEL resilience. Tests performed in [23] revealed that the laser-energy needed to induce SEL was almost constant as long as the laser spot remained inside the N-well region. Latch-up could still be triggered when the laser was outside the N-well, but higher laser energies was needed. This could imply that it can be an advantage to have the N-wells as small as possible to reduce the chance of a particle strike occurring inside the N-well.

As mentioned earlier, anode triggering is the easiest way to induce latch-up because of the pnp BJT's higher β and the high sheet resistance of the N-well. When a particle strike occurs inside the N-well, the electrons flow as majority carriers towards the pMOS source and N+ well contact. The larger the area of the N-well, the longer the electrons can flow as majority carriers, making it easier to induce SEL even from a distance from the actual structures. If a particle strike occurs outside of the N-well it would also be beneficial with a small N-well area. As mentioned in [10] and [11] the collection efficiency (α) is increasing with the size of the N-well, though not linearly. As mentioned in [26], the most sensitive region is at the edge of the N-well. When the size of the N-well is increased, the length of the N-well edge is increased, making the possibility of a particle strike at this location even higher.

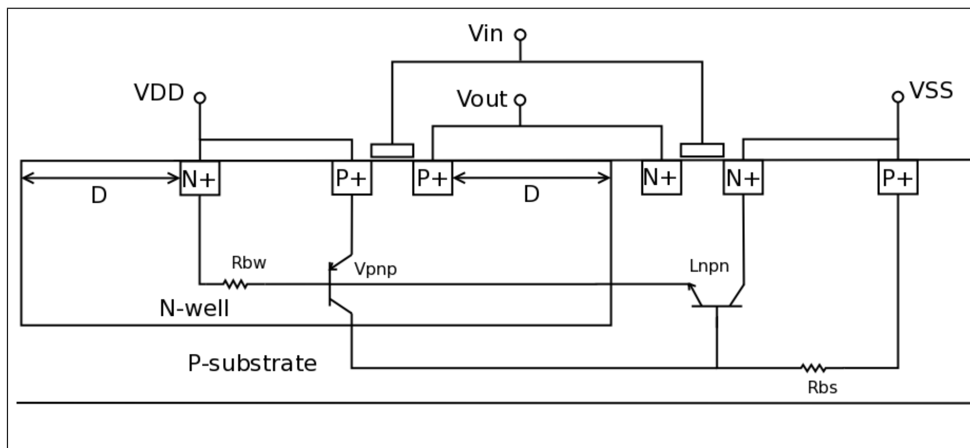

Figure 1.13: Cross section of an inverter were the N-well size is increased on both sides of the pMOS. Here, "D" is the new distance between the N-well edge and the source/contacts.

1.7.2 Diffusion size

The source and drain of the pMOS and nMOS function as the emitter of the parasitic pnp and npn BJT's, respectively. As can be seen in figure 1.8, there exists a resistance is series with the emitter of the BJT's (R_{ew} and R_{es}). This resistance has an effect on the latch-up current and the trigger voltage as can be seen in Eq. 1.6, 1.7 and 1.7. By decreasing this resistance the trigger voltage will decrease as well as the trigger current, making the structure more susceptible to SEL. As shown in Eq. 1.12, latch-up current will also increase as the R_{ew} and R_{es} decreases, making SEL more destructive on the circuit. This resistance is basically the resistance of the source N+/P+ contact. A way to decrease this resistance is to make the source and drain of the nMOS and pMOS larger to get a larger contact surface between the P+/N+ contacts and the P-substrate/N-well respectively.

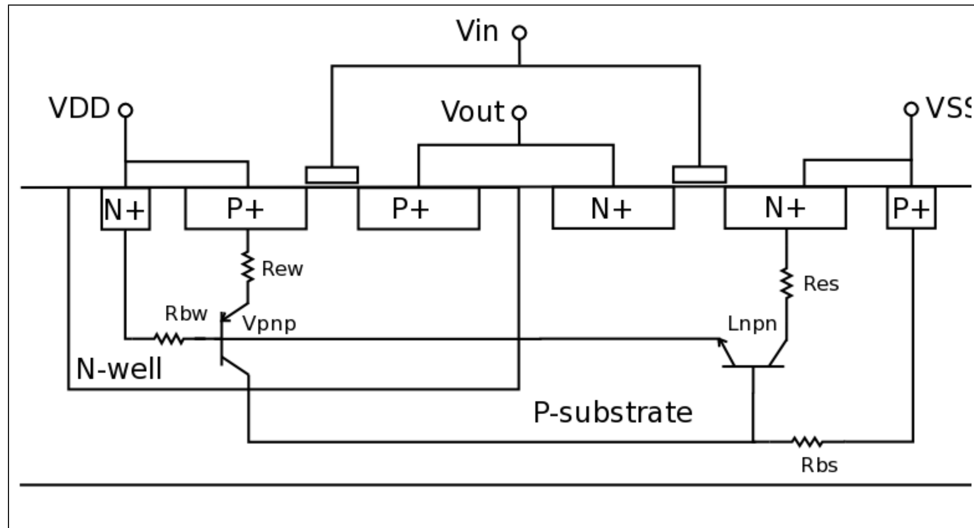

Figure 1.14: Cross section of an inverter were the source and drain areas of the nMOS and pMOS has been increased.

1.8 Transistor width, theory

The goal is to explore and characterize the effect of increasing nMOS and pMOS transistor width on SEL susceptibility. When designing large buffers in CMOS, wide transistors have to be used in order to produce the necessary output current. In this section we will investigate the effect of increasing the length (L) of the diffusion region by increasing the width of the nMOS and pMOS transistors. Eq. 1.13 shows how to roughly calculate the β of a BJT based on the doping consentration and the dimensions of the diffusion region. In section 2.2 we investigated the effect of manipulating the width (W) of the diffusion by increasing the distance between the nMOS and pMOS transistors. Eq. 1.13 shows that β increases linearly when the diffusion length (L) increases. Basically this means that when the nMOS transistor width is doubled, the gain of the parasitic npn BJT is doubled, resulting in increased SEL susceptibility because of reduced trigger current (Eq. 1.7 and 1.8.

1.9 Epitaxial layer

Epitaxial substrate wafers are often used to minimize latch-up occurrence in CMOS compared to bulk silicon wafers and is often preferred by digital designers. Analog designers often prefer bulk substrate with high bulk resistivity which acts a filter to attenuate high frequency noise, rapidly minimizing coupling to surrounding circuitry. Epitaxial layer is a low doped crystal layer deposited on top of the highly doped substrate such that both have the same structural orientation. Because the epi layer has a low resistivity layer beneath, the current required to turn on the lateral pnp increases, making the structure less susceptible to latch-up.

The use of guard rings are shown to be orders of magnitude more

efficient when fabricating on an epitaxial wafer than for bulk wafer [39]. The boundary between the low doped epi-layer and the highly doped substrate creates a very strong built-in electric field on a large P- epi/P++ substrate interface plane. This plane effectively directs majority carriers into the substrate, and also reflects the minority carriers (see figure 1.15) back into the epitaxial layer, making the guard rings more effective [19]. In a standard bulk process, the free carriers can dive deep into the substrate (see figure 1.16) avoiding the guard rings[17]. The epi-layer thickness is

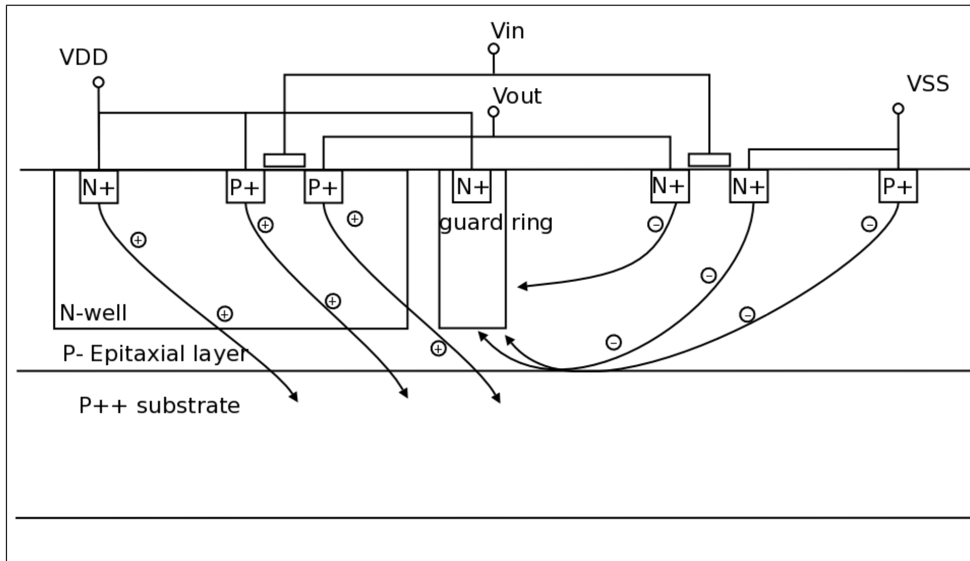

Figure 1.15: Cross section of inverter with minority carrier N+ guard ring fabricated *with* epitaxial layer

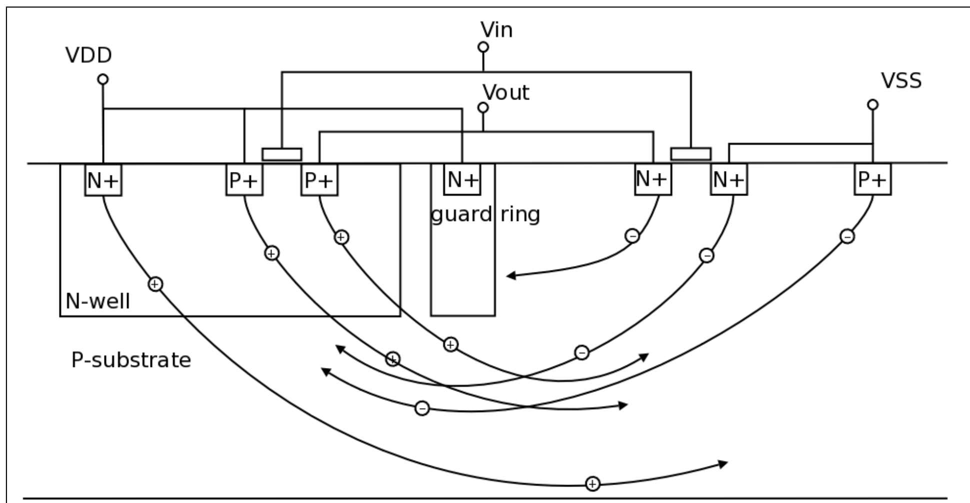

Figure 1.16: Cross section of inverter with minority carrier N+ guard ring fabricated *without* epitaxial layer

also of concern when trying to achieve the best results against latch-up. In [1], three different thickness of epi-layer was investigated, $2.3\mu m$, $4.0\mu m$ and $6.5\mu m$ where the epi-layer thickness of $2.3\mu m$ resulted in the highest

trigger current. Though, when increasing the the distance between the anode and the cathode of the structures, differing results appeared between the various epi-layer thickness. The dependence on the distance between the anode and cathode was much less for the epi-layer with $2.3\mu m$ thickness than for the thicker epi-layers.

Chapter 2

The test device

2.1 The test structures

2.1.1 Considerations

The scope of this thesis is to characterize different hardening techniques by physically testing them and analyze the results. In order to reach this goal, an ASIC designed with a number of test structures who hold these hardening techniques had to be made. In order to design an ASIC for SEL testing with laser light, many aspects have to be considered. The ASIC must have large metal power rails in order to withstand latch-up currents for a period of time. The metal routing around the structures had to be planned in order to avoid shadowing from the laser beam (see 3.1, avoiding all unnecessary metal at the sensitive nodes. Metal between the nMOS and pMOS, at the well and substrate contacts as well as source and drain have to be avoided. Because the contacts, source and drain have to be covered with a minimum of metal, it is of course impossible to have these regions completely free of metal. The test structures had to be placed a distance away from each other in order to minimize interactions between them leading to one structure triggering latch-up in the others. A pitch of 60μm was used when placing the structures. No packaging could be used because the laser beam would then be blocked, though a package without a lid could be used.

2.1.2 Inverter as a base

To characterize the different latch-up hardening techniques in the AMS 0.35μm process, several test structures based on the inverter were made. An inverter is basically the worst case device when latch-up is of concern because of the short distance between the nMOS and pMOS source (anode and cathode) leading to a low triggering current $I_t rig$ (see Eq. 1.7 and1.7). When several variations of the inverter are tested, the relevance to actual circuit design is easier to see and make use of. The use of inverters as the base structure is also a safe choice as it is an easy structure to analyze and many other publications use this component as a starting point ([42], [14], [3] and [25]).

Several authors ([23], [42] and [15]) prefer the use of large test structures build up from long P+ and N+ stripes inside the N-well and P-substrate. These stripes have to be much longer than they are wide (typical aspect ratio of 20:1) to suppress edge-effects and are placed in parallel to each other to form the P-N-P-N-structure as shown in figure 2.1. These structures are typical for latch-up studies and effective for benchmarking because they can be used to compare the different latch-up robustness of various technology nodes. The four-stripe structure represents a CMOS inverter circuit at the edge of the N-well and P-substrate regions, the gates and drains are not included because they are not directly involved in the latch-up process.

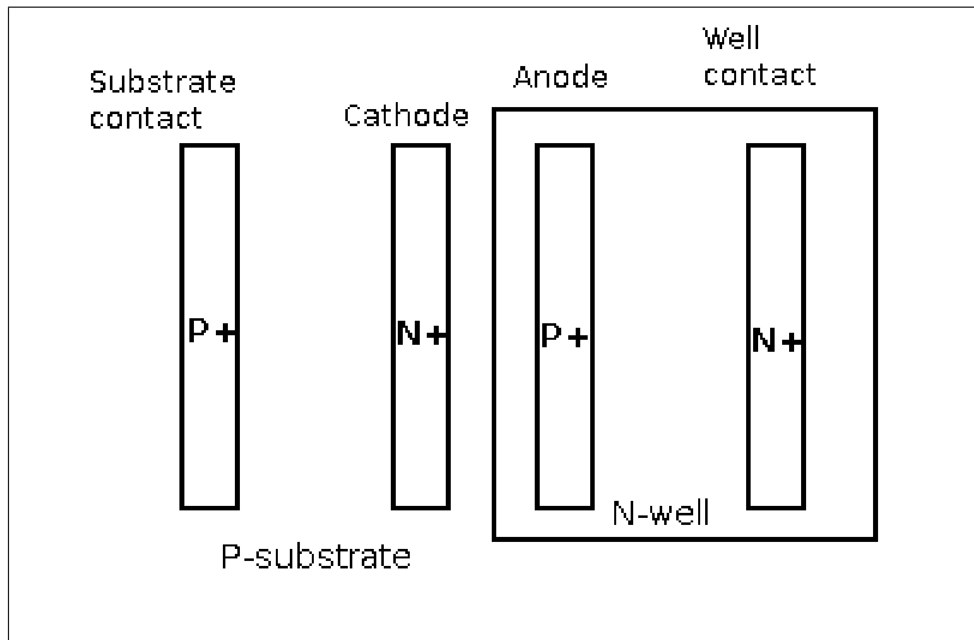

Figure 2.1: Long test structures consisting of anode, cathode and substrate-and well contacts.

2.1.3 The structures

In all, 80 different structures distributed over 5 columns were made using different hardening techniques or different versions of a hardening technique (see figure 2.2.

In column A you find GMI's standard minimum inverter, this inverter is used as a reference to relate the other structures to (see figure A.1 in Appendix A). The next 15 inverters are made to characterize the effect of increasing the distance between the nMOS and pMOS.

In column B, 16 inverters are used to characterize the effect of guard rings, both integrated and separate.

In column C, 16 inverters are used to characterize the effect of different well and substrate contact spacings and different placement of the contacts.

In column D, 8 inverters are used to characterize the effect of different sized N-well and 6 inverters to characterize the effect of different drain

and source area. One AND-gate and a NOR-gate were also implemented to characterize latch-up susceptibility on another device than the inverter.

In column E, 16 inverters are used to characterize the effect of nMOS and pMOS width and how this effect is impacted when the transistors are turned 90°.

Every column has its own digital powersupply (Dvdd), analog powersupply (Avdd) and digital ground connection (Dvss) as well as an analog ground connection (Avss) common to all structures and control logic. By using separate power connections we have the opportunity of measuring the current passing trough the N-well/substrate contacts or trough the source of the inverters. This is also a common design practice in order to avoid disturbance in the N-well or substrate from transients created by switching the transistors on and off.

2.1.4 Signal propagation

In order to confirm which one of the inverters is actually experiencing latch-up, a clock signal have to be propagated trough them and monitored. If the signal is not propagated trough the inverter, it is most likely experiencing latch-up (though another failure could occur). By implementing a network of tri-state inverters, the structure to be propagated to the output can be chosen manually (see figure 2.3). The structures are arranged as a matrix with 16 rows and 5 columns. One tri-state inverter is implemented at the output of each test-structure to create the possibility of choosing which row you want to be propagated. One tri-state inverter at the bottom of each column to choose which column you want to monitor. The tri-state inverters controlling the rows are controlled by a 4-16 MUX and the tri-state inverters controlling the columns are controlled by a 3-8 MUX (see figure 2.3. The inputs of the two MUX are controlled by the switches on the PCB.

2.1.5 Area penalty

The different inverter structures have different layout properties, functionality as well as area. In order to characterize the positive and negative sides to an inverter structure, the total area play an important role when designing large circuits. Table 2.1 presents the total area of the inverter structures as the smallest square that can contain the entire nMOS and pMOS including the N-well and P-substrate contacts (not including the metal routing). The areas presented does not show the minimum area for the respective structure, each structure can be optimized in order to save area, but the areas presented are the areas of the actual structures used in this thesis. Table 2.1 is intended to give a impression of the area penalty when using different latch-up hardening techniques.

Str.	Column A	Column B	Column C	Column D	Column E
1	$91.7\mu m^2$	$122.1\mu m^2$	$76.0\mu m^2$	$135.4\mu m^2$	$96.0\mu m^2$
2	$67.3\mu m^2$	$117.8\mu m^2$	$76.0\mu m^2$	$135.4\mu m^2$	$115.7\mu m^2$
3	$70.2\mu m^2$	$121.4\mu m^2$	$78.0\mu m^2$	$135.4\mu m^2$	$135.4\mu m^2$
4	$73.1\mu m^2$	$231.3\mu m^2$	$64.4\mu m^2$	$263.9\mu m^2$	$155.2\mu m^2$
5	$76.0\mu m^2$	$238.7\mu m^2$	$64.4\mu m^2$	$404.0\mu m^2$	$194.6\mu m^2$
6	$78.9\mu m^2$	$238.7\mu m^2$	$80.6\mu m^2$	$614.1\mu m^2$	$234.1\mu m^2$
7	$84.7\mu m^2$	$163.0\mu m^2$	$86.4\mu m^2$	$1057.3\mu m^2$	$272.5\mu m^2$
8	$90.5\mu m^2$	$211.5\mu m^2$	$92.2\mu m^2$	$3981.3\mu m^2$	$313.0\mu m^2$
9	$102.1\mu m^2$	$264.0\mu m^2$	$98.0\mu m^2$	$200.7\mu m^2$	$94.3\mu m^2$
10	$113.7\mu m^2$	$162.1\mu m^2$	$109.6\mu m^2$	$200.7\mu m^2$	$106.7\mu m^2$
11	$131.1\mu m^2$	$210.4\mu m^2$	$121.3\mu m^2$	$200.7\mu m^2$	$120.9\mu m^2$
12	$148.5\mu m^2$	$262.7\mu m^2$	$144.4\mu m^2$	$200.7\mu m^2$	$133.3\mu m^2$
13	$177.5\mu m^2$	$121.4\mu m^2$	$167.6\mu m^2$	$200.7\mu m^2$	$159.9\mu m^2$
14	$235.5\mu m^2$	$170.7\mu m^2$	$202.4\mu m^2$	$200.7\mu m^2$	$185.3\mu m^2$
15	$322.5\mu m^2$	$170.7\mu m^2$	$231.4\mu m^2$	$119.0\mu m^2$	$211.9\mu m^2$
16	$612.5\mu m^2$	$204.4\mu m^2$	$306.8\mu m^2$	$122.8\mu m^2$	$237.3\mu m^2$

Table 2.1: Total area of the inverter structures. The area is measured as the smallest square that can contain the entire nMOS and pMOS including the N-well and P-substrate contacts.

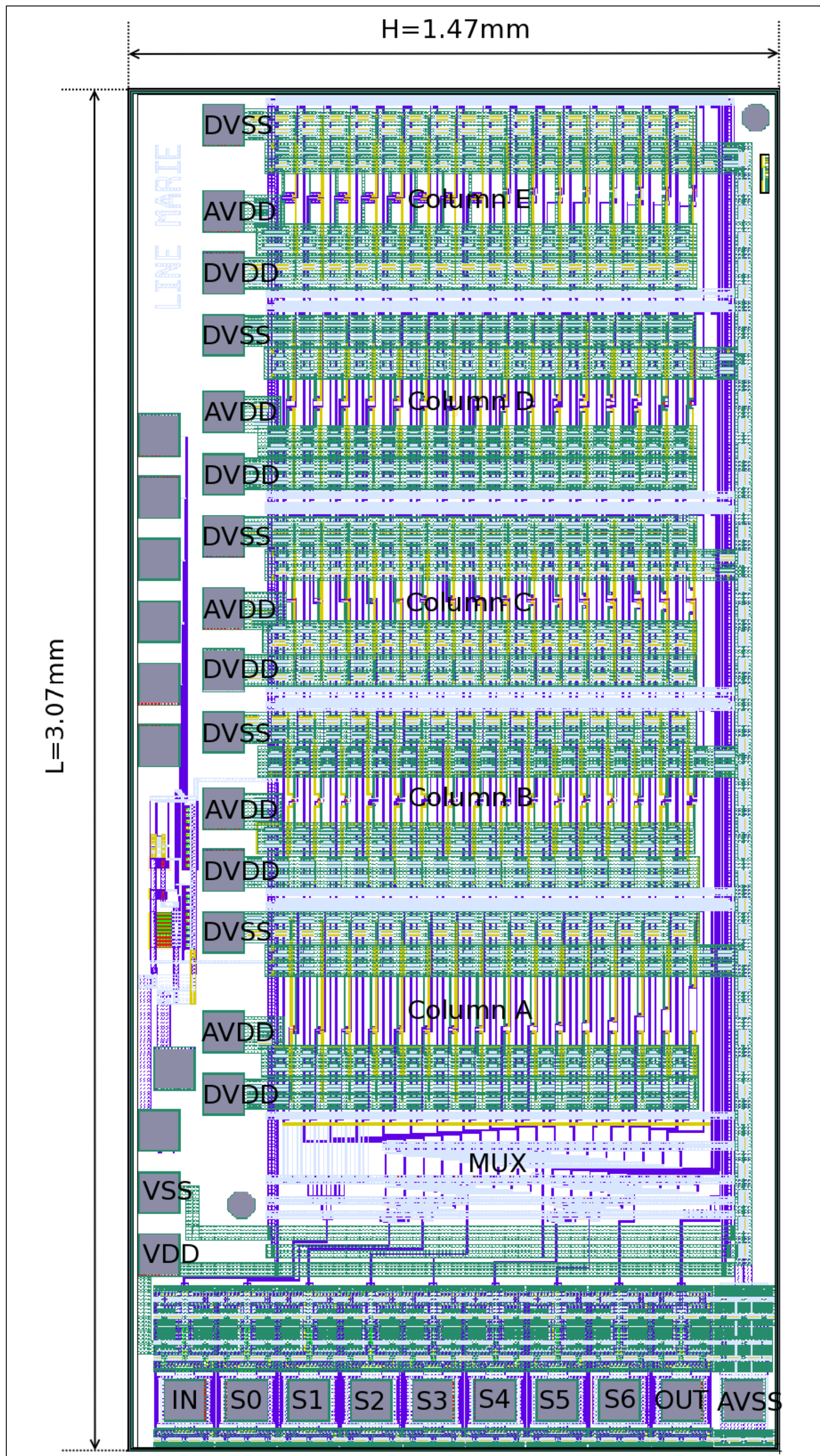

Figure 2.2: Layout of the entire ASIC before production.

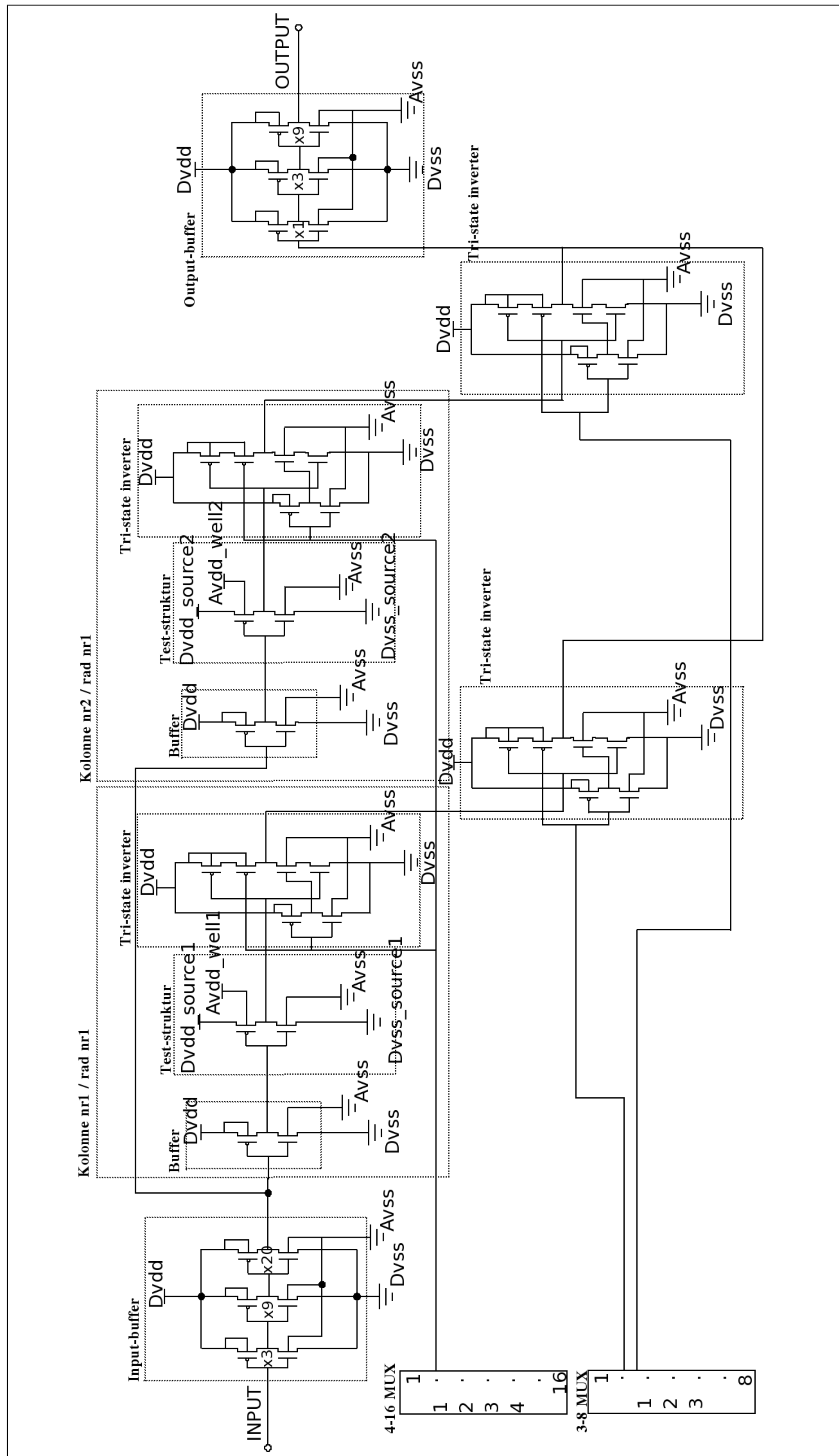

Figure 2.3: Simplified schematics of the entire ASIC.

2.2 nMOS and pMOS spacing

By making several standard minimum inverters with different distance between the nMOS and pMOS, an investigation on the impact of nMOS and pMOS spacing can be done by empirically testing each structure.

Each inverter is exactly the same except from the differing nMOS to pMOS distance. When designing the different inverters the purpose was to cover the range between minimum spacing to a spacing too long for consideration in an actual circuit design. The distances are measured between the source of the pMOS to the source of the nMOS and ranges from 5.4μm to 100μm. The drains of the transistors are always 1.4μm closer to the opposite transistor as can be seen in figure 2.4 and figure 2.5. The figures show only 2 of 15 layouts of the inverters with different transistor spacings, the rest can be seen in Appendix (A). The inverters were made with transistor source-source spacings of; A2=5.4μm, A3=5.9μm, A4=6.4μm, A5=6.9μm, A6=7.4μm, A7=8.4μm, A8=9.4μm, A9=11.4μm, A10=13.4μm, A11=16.4μm, A12=19.4μm, A13=24.4μm, A14=34.4μm, A15=49.4μm, and A16=99.4μm. By using Eq. 1.13, one can see the increase in source-source spacing from 5.4µm to 100µm decreases the β with a factor of 99.4μm/5.4μm=18.4.

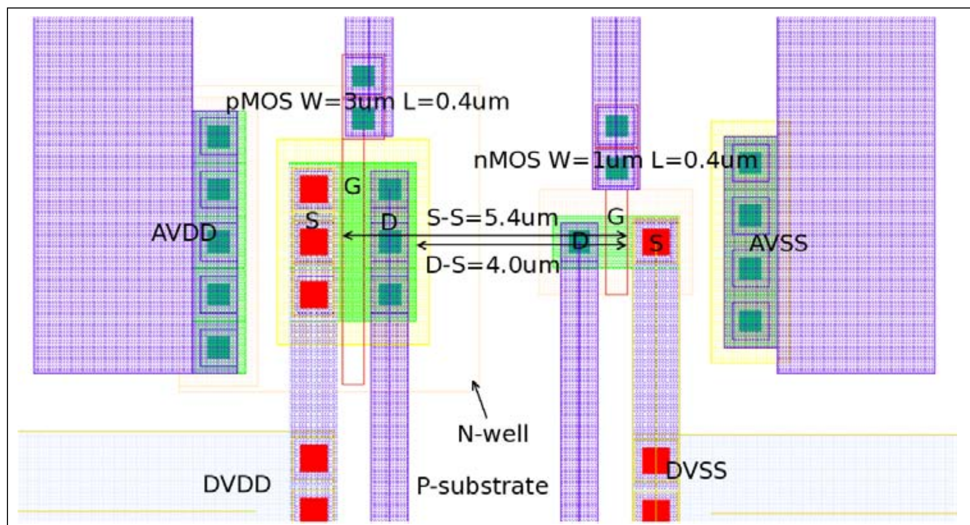

Figure 2.4: Inverter with nMOS-pMOS spacing of 5.4μm.

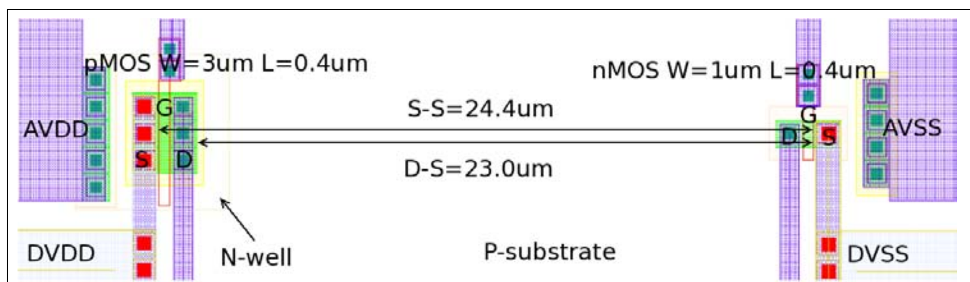

Figure 2.5: Inverter with nMOS-pMOS spacing of 25μm.

It is expected to see a marked decrease in the latch-up current as the anode-cathode spacing increases because of the lower transport factor (α) obtained (see Eq. 1.12). As demonstrated in [31], it is expected an increase in the trigger current as the nMOS to pMOS spacing (diffusion width W) is increased. The holding voltage is expected to increase linearly as a function of the anode to cathode spacing as explained in [19]. In the inverters with the longest transistor spacings, no latch-up is expected because of the low β product. Figure 2.6 roughly present the expected trigger current increment as the spacing between the nMOS and pMOS transistor increases based on Eq 1.7. The figure is only intended as an illustration of the source-source spacing effect on trigger current.

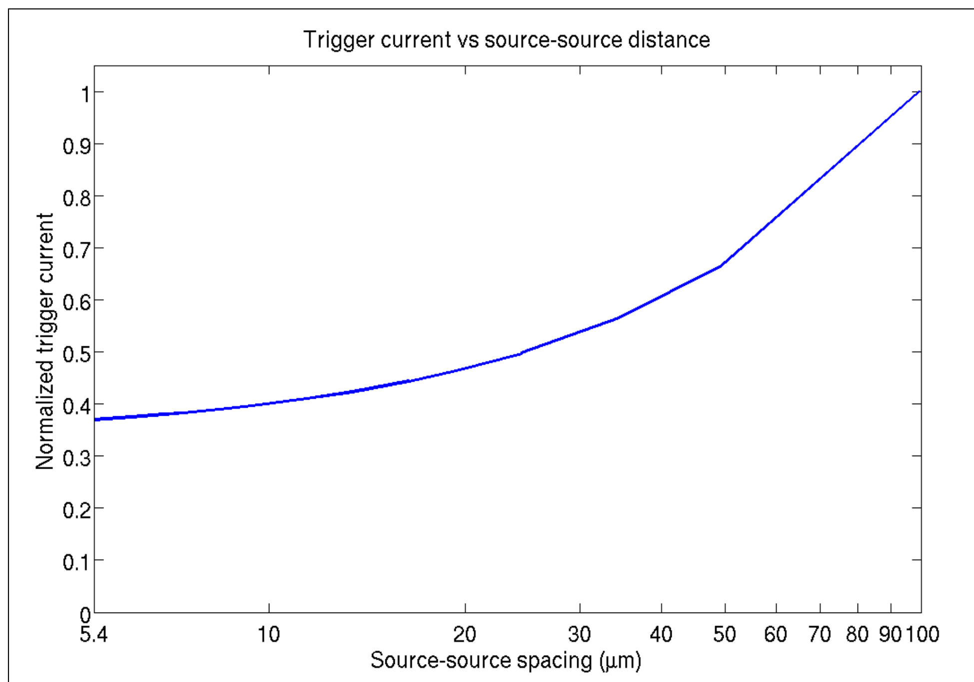

Figure 2.6: Latch-up trigger current as a function of source-source spacing of the nMOS and pMOS transistor. Normalized trigger current is shown as a function of the spacing between the N+ source of the nMOS and the P+ source of the pMOS in μm.

2.3 Guard rings

By the making of several inverter structures with different guard ring variations, we can determine the most effective structure by empirically testing the structures.

These structures are based on the minimum inverter used at Gamma Medica to get the most comparable results to this inverter and their technology. In all structures the nMOS source to pMOS source distance is set to be 9.250μm to eliminate this variable between the structures. When designing the guard rings, one of the goals were to place them as near to the transistors as the DRC rules allowed. Because of inattention when designing the structures, the inner edge of guard ring surrounding the pMOS was placed 0.1μm longer away from the source than the minimum allowed distance, this is pointed out in the figures. Because all the N+ guard rings are placed at the same distance from the pMOS source, this is not an issue. All the guard rings are biased with the highest contacts-densities possible and are connected to the power buses with a 3μm wide and about 40μm long metal 3 and 4 wire.

When using guard rings, it is obvious that it entails area penalty (see table 2.1 for the total area of the inverter structures). By using the total height and width of the transistors (including the guard rings and well - and substrate contacts) as a measure of area, a rough estimation of the area penalty of each transistor can be calculated. However, this should not be interpreted as a finite area penalty when designing large circuits, this is as mentioned just a rough calculation of the area of a single transistor including the guard rings. The nMOS and pMOS has an area of 33.3μm^2 and 21.6μm^2 respectively without guard rings.

Structure B1. With this structure we will investigate an N+ majority guard ring around the pMOS as shown in figure 2.7. The guard ring consists of a ring of N+ diffusion at the edge of the N-well, placed as near the pMOS transistor as possible to minimize the well resistance between the guard ring and the pMOS source. The longest and shortest distance between the source or drain of the pMOS and the guard ring is 1.1μm and 0.85μm respectively, this is limited by the DRC-rules of the AMS 0.35µm technology. The substrate contacts for the nMOS are placed as close to the nMOS as possible. The new area of the pMOS is now measured to be 52.4μm^2, an increase of 57%, the area of the nMOS is not changed.

When a particle strike occurs outside this guard ring, the current which then is generated will be collected by the guard ring before it is collected by the source of the pMOS. The current will have to pass the guard ring before it can be collected by the source, and because of the large area of the guard ring and low resistance, the guard ring is capable of collecting large currents. If a strike occurs inside the guard ring, then the generated current will not have to pass the guard ring to reach the source, but much of the current will still be collected by the guard ring because of its lower resistance and larger area. Even if the pMOS now is hardened against latch-up, the nMOS (or the parasitic npn) can theoretically still be triggered. Because

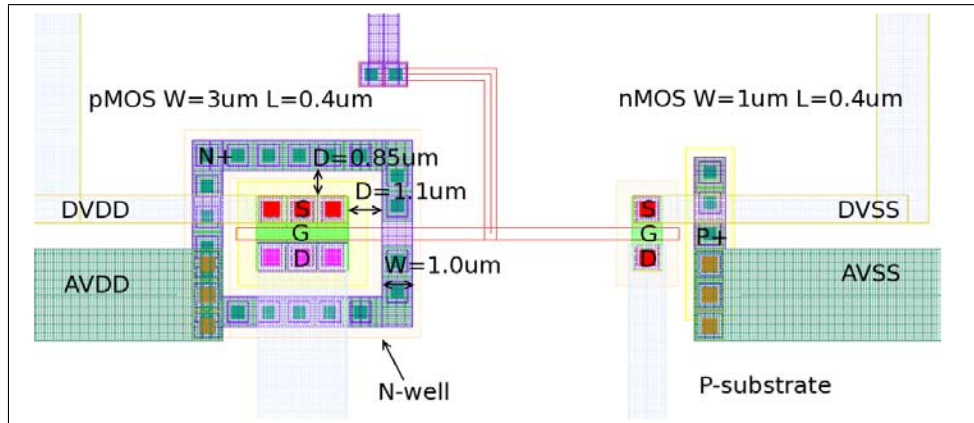

Figure 2.7: Majority N+ guard ring with a width of 1μm.

when a particle strike occurs, both free electrons and free holes are generated. Electrons are collected by the N+ guard ring and pMOS source and holes are collected by the nMOS source and the substrate contacts, meaning that the N+ guard ring will have no effect on the collection of free holes. Still, the inverter will be less susceptible to latch-up because the npn BJT now gets "less help" from the pnp BJT in its attempt to induce regenerative feedback.

Structure B2. With this structure we will investigate a P+ majority guard ring around the nMOS as shown in figure 2.8. The guard ring consists of a ring of P+ diffusion at the edge of the nMOS, placed as near the nMOS transistor as possible to minimize the substrate resistance between the guard ring and the nMOS source. The longest and shortest distance between the source or drain of the pMOS and the guard ring is 1.0μm and 0.85μm respectively, this is limited by the DRC-rules of the AMS 0.35μm technology. The substrate contacts for the nMOS are placed as close to the pMOS as possible. The new area of the nMOS is now measured to be 36.3μm^2, an increment of 68%, the area of the pMOS is not changed.

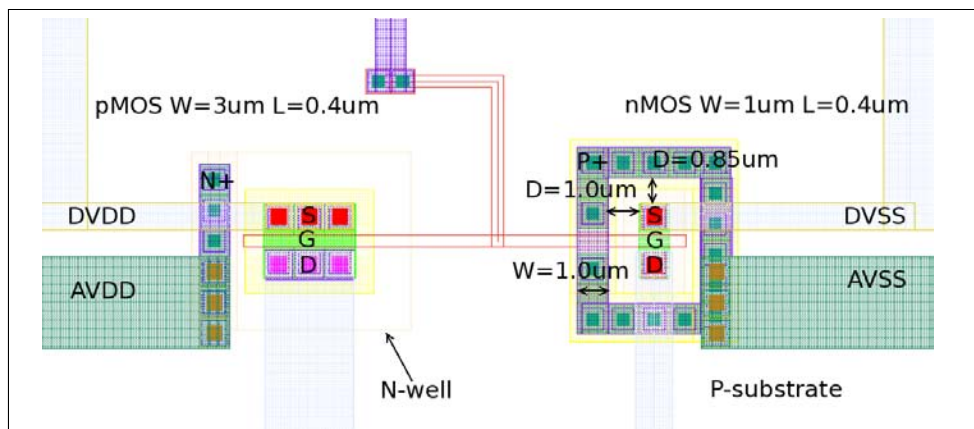

Figure 2.8: Majority P+ guard ring with a width of 1μm.

When a particle strike occurs outside the guard ring, the same situation

will appear here as for the previous guard ring structure (B1). The current will have to pass the guard ring in order to be collected by the nMOS source, and by this it will be significantly reduced depending on the guard ring efficiency. The same will also happen for a particle strike inside the guard ring, because of the low resistance, the larger part of the current will be collected by the guard ring. As mentioned, both free electrons and free holes are generated when a particle strike occurs. The P+ guard ring will collect only free holes and have no effect on the collection of free electrons. The pMOS (or parasitic pnp) will theoretically still be able to induce regenerative feedback, but it will get “less help” from the npn BJT. In comparison to the P+ guard ring surrounding the nMOS, a N+ guard ring surrounding the pMOS transistor is expected to show a greater effect on latch-up susceptibility because of the higher gain of the parasitic pnp transistor and the higher resistance in the N-well.

Structure B3. With this structure we will investigate both N+ and P+ majority guard rings surrounding the pMOS and nMOS respectively as shown in figure 2.9. The guard rings used have the same size, position and width as the ones in structure B1 and B2. Now when both guard rings are present, they can prevent both free electrons and free holes from being collected by the pMOS - and nMOS sources respectively. The area penalty of the pMOS and nMOS are the same as in B1 and B2, an increase of 57% and 68% respectively.

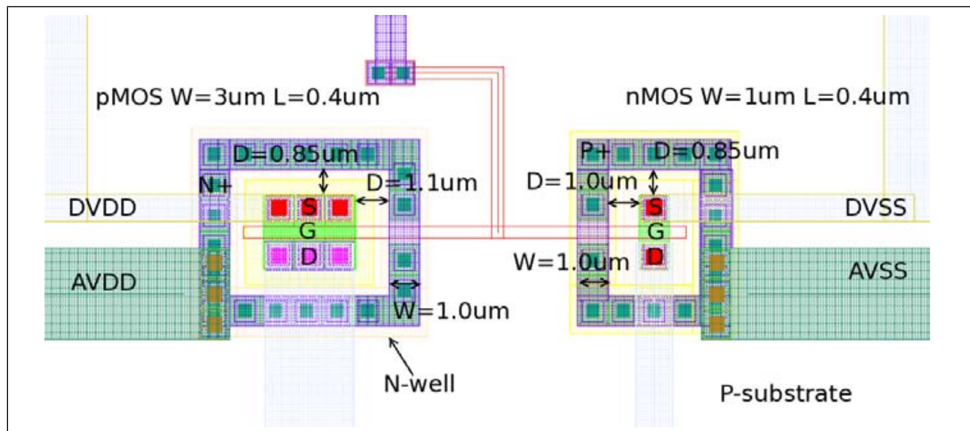

Figure 2.9: Both majority N+ and P+ guard ring with a width of 1μm.

When using both N+ and P+ guard rings, even better result are expected in comparison to using only one of the guard rings. Less current will reach the sources of the nMOS and pMOS resulting in a higher trigger current needed to trigger latch-up.

Structure B4. With this structure we will investigate the effect of using a N+ minority carrier guard ring around the pMOS transistor as shown in figure 2.10. The guard ring consists of a N+ diffusion ring placed in a separate N-well surrounding the pMOS. Both the inner N-well containing the pMOS and the guard ring are biased to VDD. The distance

between the inner N-well and the surrounding N-well is the minimum distance (according to the DRC-rules) of 1μm and is preferred to be small because of the area penalty and to minimize the chance of a particle strike inside the guard ring. The area penalty when using this type of guard ring on a pMOS of this size is measured to be 322% with an area of 140.6μm^2.

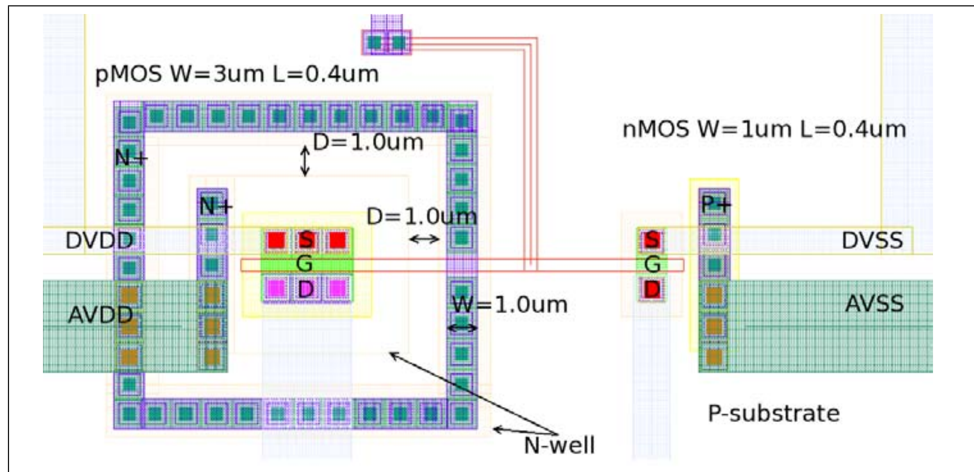

Figure 2.10: Minority N+ guard ring with a width of 1μm.

The purpose of this type of guard ring is to collect the minority carriers (in this case electrons) before they are collected by the N-well containing the pMOS where they flow as majority carriers. The effect of using a N+ minority guard ring is expected to be less than using a N+ majority guard ring. When using a N+ majority guard ring in a N-well, the guard ring also contributes in biasing the N-well and thereby lowering the well resistance.

Structure B5. With this structure we will investigate the effect of both P+ - and N+ minority carrier guard “rings”. Actually, the guards are not formed as rings with the purpose of saving area, they are formed as stripes and placed in between the nMOS and pMOS as shown in figure 2.11. In this case the guard does not protect directly against particle strikes that generate free carriers, but they degrade the β of the parasitic bipolar transistors by collecting the minority current passing between them. As a result of this, it is harder for the BJT’s to obtain regenerative feedback. The area penalty is measured to be 40% on the pMOS with a area of 46.8μm^2 and 22% on the nMOS with a area of 35μm^2.

As mentioned earlier, this type of guard “ring” is most used to prevent internal latch-up because it does not protect the sensitive part from charge injection. The effect of this structure is expected to be higher than structure nr B4 because both guard rings collect the free carriers. The current passing between the transistors will also be collected by the guard stripes, contributing to de-bias the BJT’s.

Structure B6. With this structure we will investigate the effect of N+ - and P+ majority guard rings and N+ - and P+ minority guard stripes as shown in figure 2.12. This structure takes the best from two techniques,

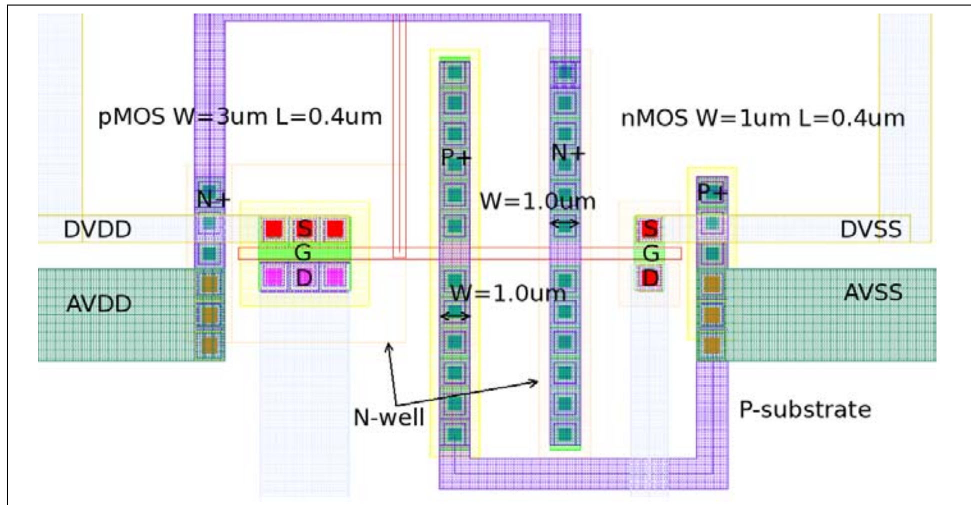

Figure 2.11: Minority N+ and P+ guard strips with a width of 1μm.

but the structures start to get "complicated" with four different guard rings and the area is also significantly increased. The nMOS and pMOS are now protected against particle strikes (charge injection) by the majority carrier guard rings, the β of the parasitic pnp and npn transistors are decreased as well as the current traversing between them is collected by both the minority and majority guard rings. The area penalty is measured to be 104% on the pMOS with a area of $68\mu m^2$ and 134% on the nMOS with a area of $50.7\mu m^2$.

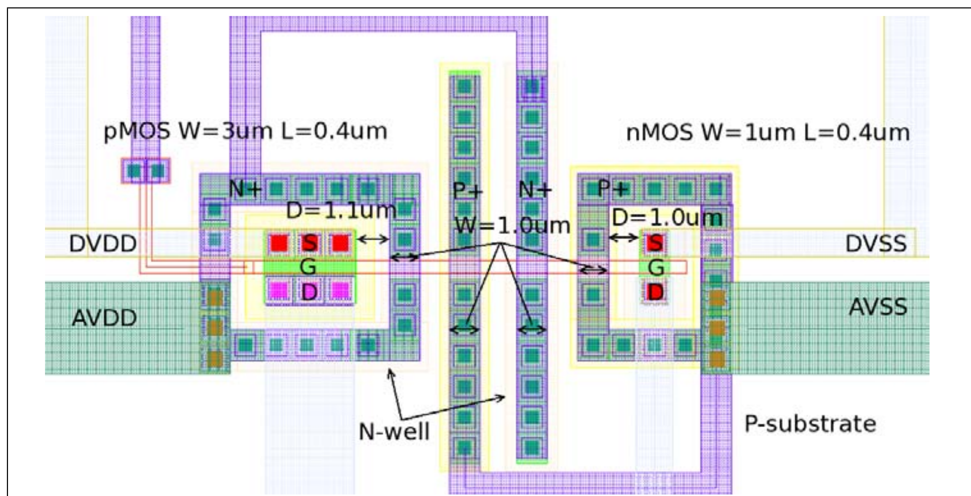

Figure 2.12: Both N+ and P+ majority and N+ and P+ minority guard strips with a width of 1μm.

This structure is expected to show greater effect than the previous structures because of the minority guard rings in addition to the majority guard rings. Now both the N-well and P-substrate have a good bias connection and the nMOS and pMOS are protected against both charge injection (external latch-up) and internal latch-up.

Structure B7, B8, B9. With these structures we will investigate the effect of a wider N+ majority carrier guard ring. This is basically the same structure as B1, but the width of the guard ring is increased from 1μm to 2μm, 3μm and 4μm (see Appendix A, figure A.23, A.24 and A.25). Now when increasing the size of the collector, and thereby decreasing the resistance from the injection source, even more of the injected charge will be collected by the guard ring. The resistance of the N-well is also significantly reduced because of the extremely good connection to VDD. The area penalty is of course increasing when the width of the guard rings are increasing. The area penalties for pMOS with N+ guard ring sizes of 2μm, 3μm and 4μm are; 150% with a area of 83.4μm^2, 272% with a area of 124μm^2 and 418% with a area of 172.6μm^2.

The effects of these guard rings are expected to increase as the width of the guard rings increase, though effect of increasing the width of the guard ring will decrease as it get wider.

Structure B10, B11, B12. With these structures we will investigate the effect of a wider P+ majority carrier guard ring. The width of the guard rings are increased from 1μm to 2μm, 3μm and 4μm (see Appendix A, figure A.26, A.27 and A.28 respectively. The area penalties for nMOS with these P+ guard ring sizes are; 198% with a size of 64.5μm^2, 366% with a size of 100.7μm^2 and 573% with a area of 145.5μm^2.

The effect of these guard rings are also expected to increase as the width of the guard rings increase for the same reason as for the N+ guard rings, but the effect will be lower due to the higher gain of the parasitic pnp BJT.

Structure B13, B14, B15. With these three structures we will investigate a butted MGR with a width of 1μm and 2μm, see figure 2.13 and 2.14. By butting the MGR with the source of the respective transistor, the resistance between the contacts and source (R_{bw} and R_{bs}) is decreased as well as the guard rings collect injected carriers and bias the N-well and P-substrate. Of all the structures made, these three are expected to show the lowest latch-up susceptibility.

In figure 2.15 you can see an inverter with the P+ and N+ contacts in between the transistors. In this way, the contacts function as a MGR, lowering the gain (β) of the parasitic BJT's and collecting majority carriers passing between them. The mNGR collects minority carriers in the P-substrate injected from the particle strike, protecting the pMOS transistor. This combination of contact placement and mNGR is expected to show very good results against latch-up.

Structure B16. With this structure we will investigate the effect of a butted MGR and a mNGR were the N-well and P-substrate contacts are placed in between the transistors (see figure 2.15). This structure is expected to show even higher latch-up resilience than B4 because of the N-well and P-substrate contacts are placed in between the transistors and function as guard stripes. The effect of placement of the N-well and P-substrate contacts will be further investigated in section 2.4.

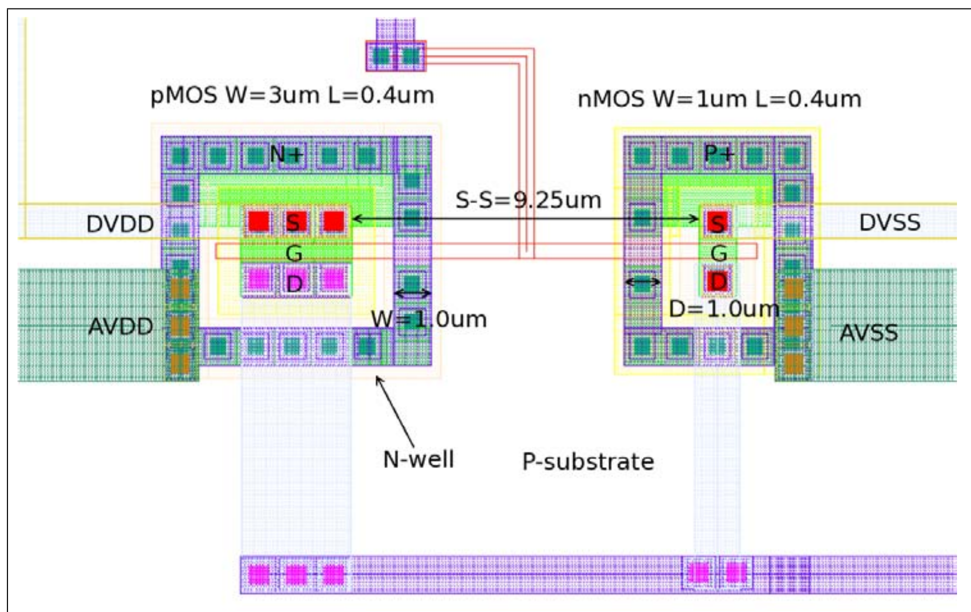

Figure 2.13: Inverter with N+ and P+ majority guard ring with a width of 1μm.

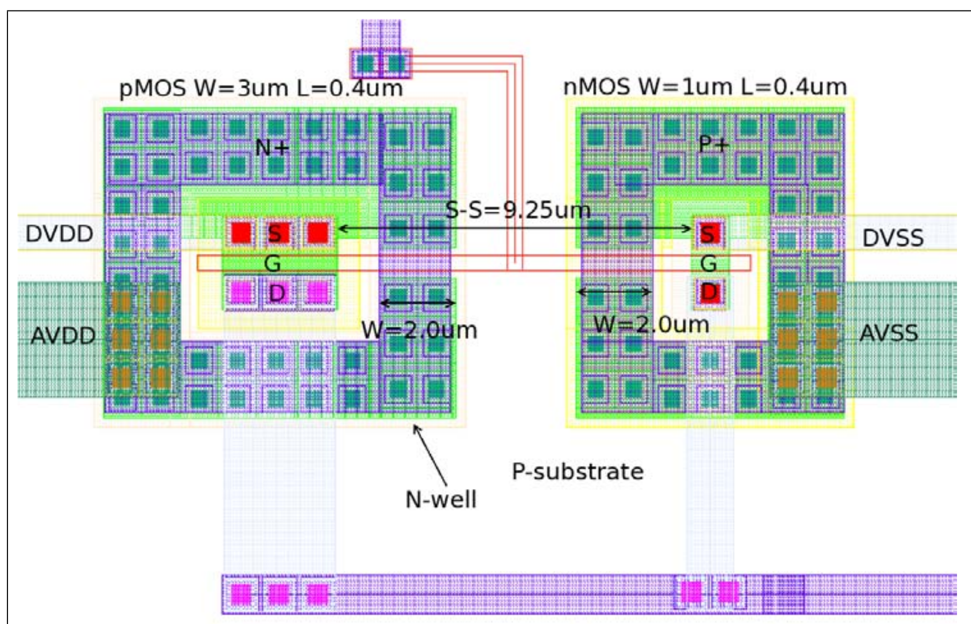

Figure 2.14: Inverter with N+ and P+ majority guard ring with a width of 2μm.

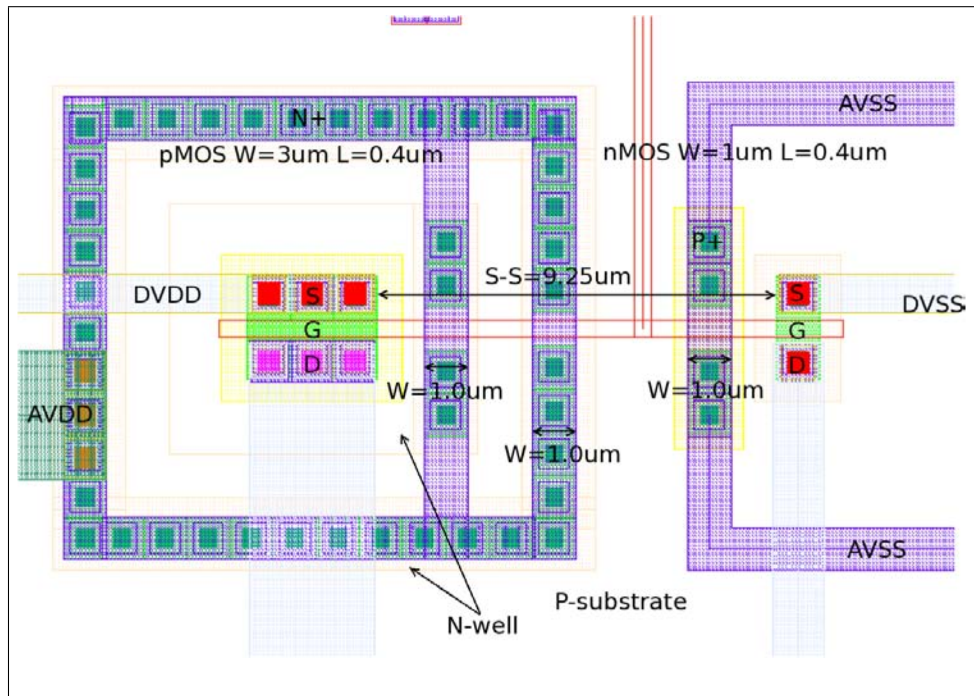

Figure 2.15: Inverter were the N+ and P+ contacts are placed in between the transistors and a minority N+ guard ring around the nMOS.

2.4 N-well and P-substrate contact placement

By making several standard minimum inverters with different placement of the contacts, an investigation of its effect can be done by empirically testing each structure.

Each inverter is exactly the same except from the different placement of the P-substrate and N-well contacts. The spacing between the nMOS and pMOS has been slightly increased to make room for all the different variations of contact placement. The distance between the nMOS and pMOS is set to be 7.4μm from source to source. 16 different structures were made, where the first one (structure C1) is a standard inverter with minimum contact to source distance of 0.6μm. Structure C2-C5 represent different placement of the contacts and butting of the contacts with the transistor terminals. Structure C6-C16cover the range from minimum contact-to source spacing, to a spacing too long for consideration in actual circuit design. These inverters were made with contact to source distances of; 0.6μm, 1μm, 1.5μm, 2μm, 2.5μm, 3.5μm, 4.5μm, 6.5μm, 8.5μm, 11.5μm 15.5μm, 20.5μm.

2.4.1 Different contact and diffusion location

Structure C1. The structure shown in figure 2.16 is the same one as investigated under "2.2 nMOS and pMOS spacing" and is only used as a reference to compare the result from the following test structures. As mentioned, the source-source distance is set to be 7.4µm to make room for the contact placement variations. This is not the minimum distance, but in order to sift out the effect of contact placement, a fixed distance between the transistors is necessary to eliminate variable gain of the parasitic BJT.

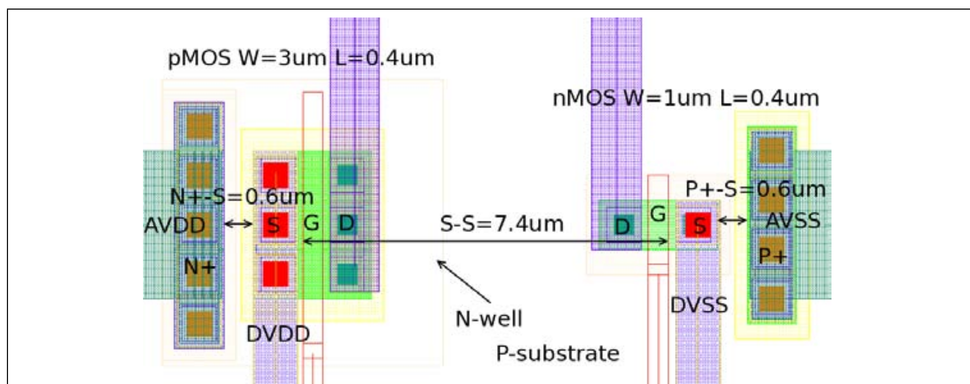

Figure 2.16: A standard inverter with source-source distance of 7.4μm and contact-source distance of 0.6μm.

Structure C2. In the structure figured in 2.17, the source and drain are on the opposite side of the gate compared to the first inverter figured in 2.16. A result of this change is an increase in the contact-source distance which leads to a larger shunting resistance in the N-well/P-substrate. The source-source distance is decreased as a result of this change, leading to a decrease in the parasitic BJT base width, increasing the gain of the BJT's.

It is expected that this structure will present a higher susceptibility against latch-up than the reference structure because of this increase in both shunt resistance and parasitic BJT gain.

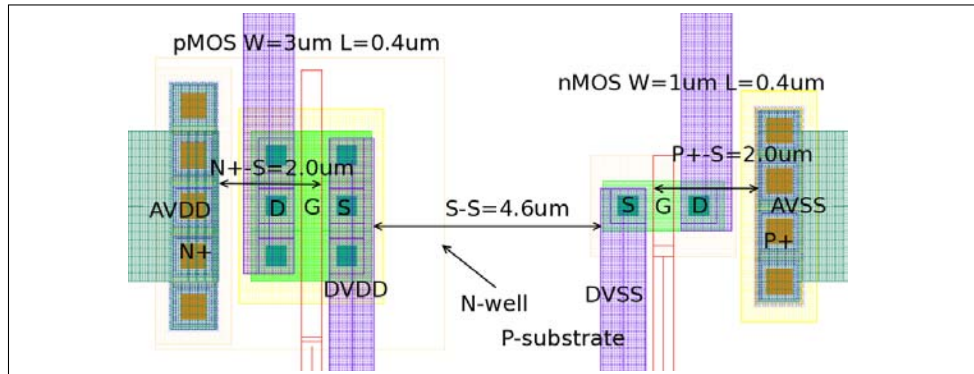

Figure 2.17: An inverter with source and drain on the opposite side of the gate compared to the standard inverter in 2.16, resulting in a source-source distance of 4.6μm.

Structure C3. In the structure figured in figure 2.18, the source and contacts are butted. This means that the N+/P+ diffusion of the contacts are directly connected to the P+/N+ source of the nMOS and pMOS respectively. This minimizes the shunting resistance between the contact and source because of the lower resistance in the diffusion compared to the N-well and P-substrate. This allows for a higher injection current before latch-up is triggered and improved susceptibility is expected against latch-up.

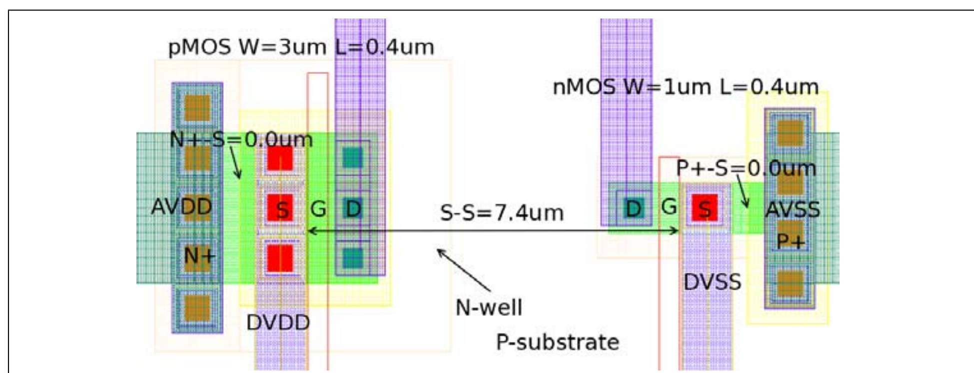

Figure 2.18: An inverter were the N-well/P-substrate contact and source are butted, resulting in a contact to source distance of 0.0μm.

Structure C4. In the structure figured in figure 2.19, the source and drain are on the opposite side of the gate and the N-well/P-substrate contacts are placed in between the transistors and butted with the source. As mentioned, placing the source on the opposite side of the gate increases the gain of the parasitic BJT's, but by placing the contacts in between the transistors they function as guard rings, lowering the transport factor of the BJT's and the current passing between them. At the same time the contacts can be butted with the source which reduces the shunt resistances,

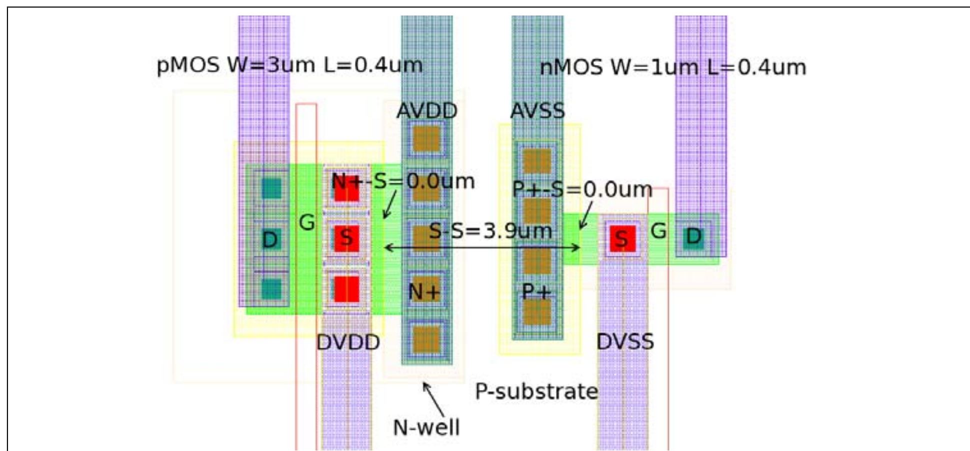

Figure 2.19: An inverter with source and drain on the opposite side of the gate compared to the standard inverter in figure 2.16, N-well/P-substrate contacts and source are butted and are placed in between the transistors. This results in a source- source distance of 3.9μm and a contact-source distance of 3.9μm.

making the structure less latch-up susceptible. It is expected to see very good results from this structure because of both the butting of the contacts and source and the use of the contacts as guard rings.

Structure C5. In the structure figured in figure 2.20, the N-well/P-substrate contacts are placed on the opposite side of the transistors and butted with the drain. By keeping the source of the transistors as far away from each other as possible, the gain of the BJT is kept as small as possible. As mentioned, by placing the contacts in between the transistors, they function as guard rings reducing both gain and current between the BJT's. By butting the contacts with the drain, the BJT's gain contribution from the drain is minimized, though butting of the source has a greater effect. It is expected to see good results against latch-up, but not higher susceptibility than structure C4.

2.4.2 Different contact-source spacing

Figure 2.22 and 2.23 shows two inverters with source to contacts spacings of 1.0μm and 20.5μm (see Appendix A to see all the structures).

If we assume a linear increase in resistance between the source and contact as the distance increases we can compare the two structures. The first structure, with a source-contact spacing of 1.0μm, and the second structure with source-contact spacing of 20.5μm differ with a factor of 20.5μm / 1.0μm = 20.5. This means that the resistance between the source and contact of the second structure is 20.5 times larger than the first structure. By using Eq 1.7 we can roughly present the effect of increasing source-contact distance. As seen in figure 2.21 Eq. 1.7 actually shows that when the resistance is lowered a factor of about 20, the trigger current is increased a factor of about 10.

Figure 2.21 is only intended to present an illustration of this effect on

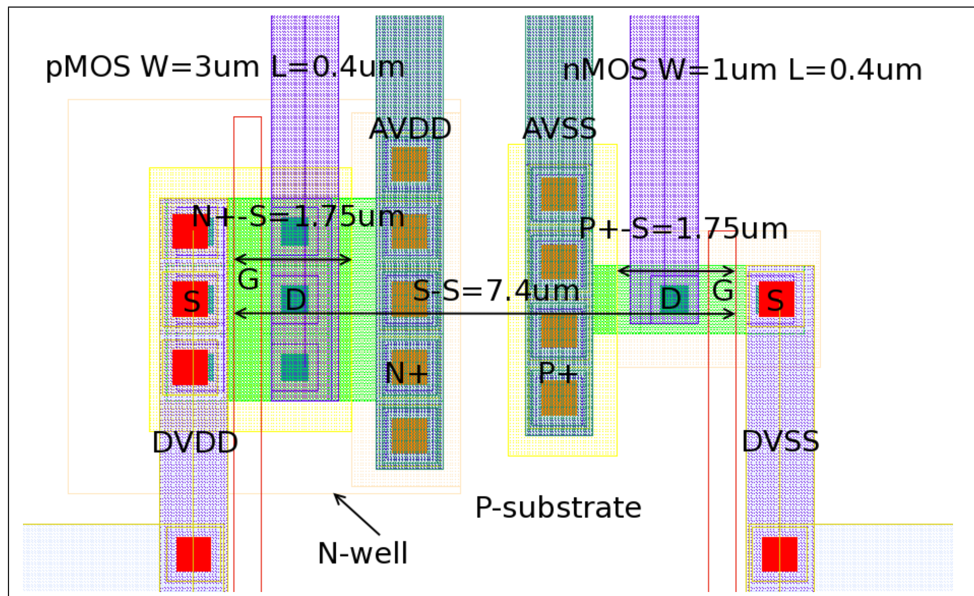

Figure 2.20: An inverter were the N-well/P-substrate contacts are placed in between the transistors and at the same time butted with the drain. This results in a contact-source distance of 1.75μm.

the trigger current of the pnp BJT, the shape and magnitude can vary with layout techniques and process parameters.

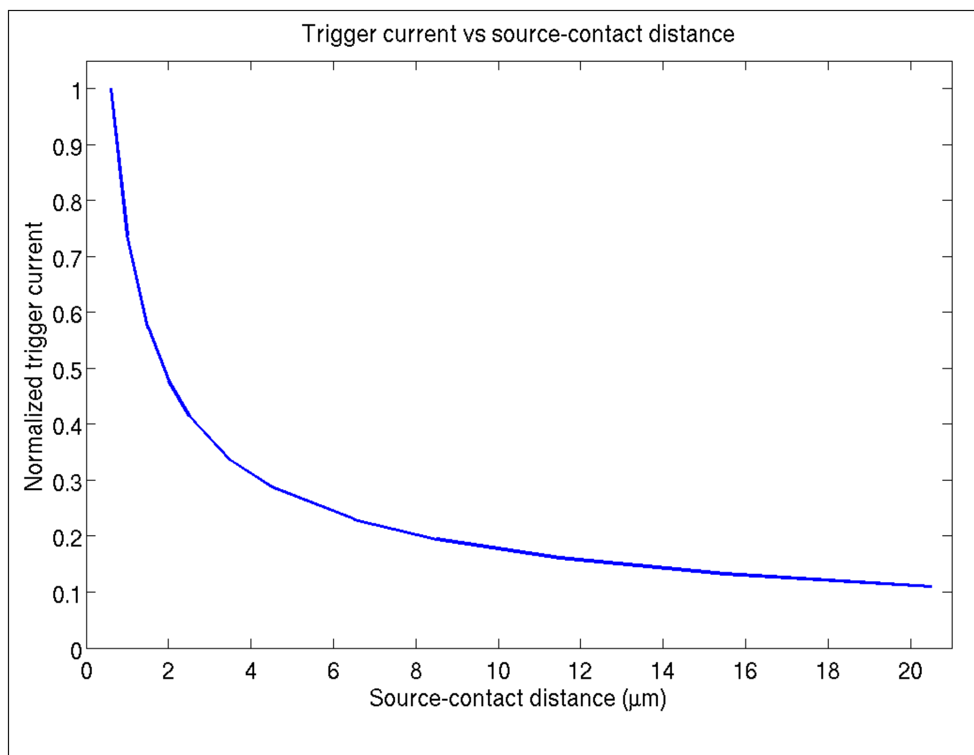

Figure 2.21: Normalized trigger current as a function of source-contact distance.

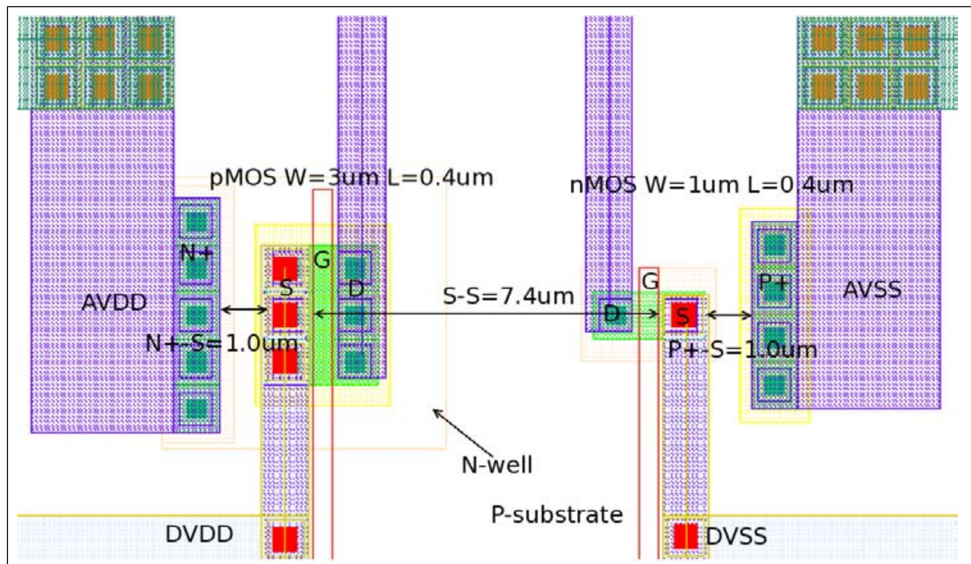

Figure 2.22: A standard inverter with N-well/P-substrate contact to source distance of 1.0μm.

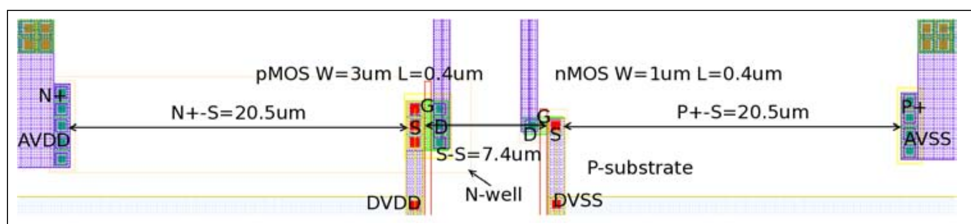

Figure 2.23: A standard inverter with N-well/P-substrate contact to source distance of 20.5μm.

2.5 N-well and diffusion size

2.5.1 Different N-well size

In order to investigate the effect of larger N-wells on SEL, 8 structures consisting of an inverter with varying N-well sizes are constructed. The N-well vary in both length and width between the smallest size of $L = 5.7\mu m, W = 5.8\mu m$ and the largest of $L = 53.4\mu m, W = 66.3\mu m$. The inverter that was used has a source-source distance of 16.4μm to make room for the different N-well sizes and the test result will be relative to the inverter with the same source-source distance and minimum N-well size. It is expected to see a vague increase in SEL susceptibility as the N-well size increases, but no marked differences between the structures.

In figure 2.24 and 2.25 you can see two inverters with different N-well size. Here you can see that a larger N-well involves a large area penalty, but this is not necessarily true since several pMOS transistors can be placed in the same N-well. Though, what the effect of several pMOS transistors in the same N-well has on SEL is not investigated in this thesis.

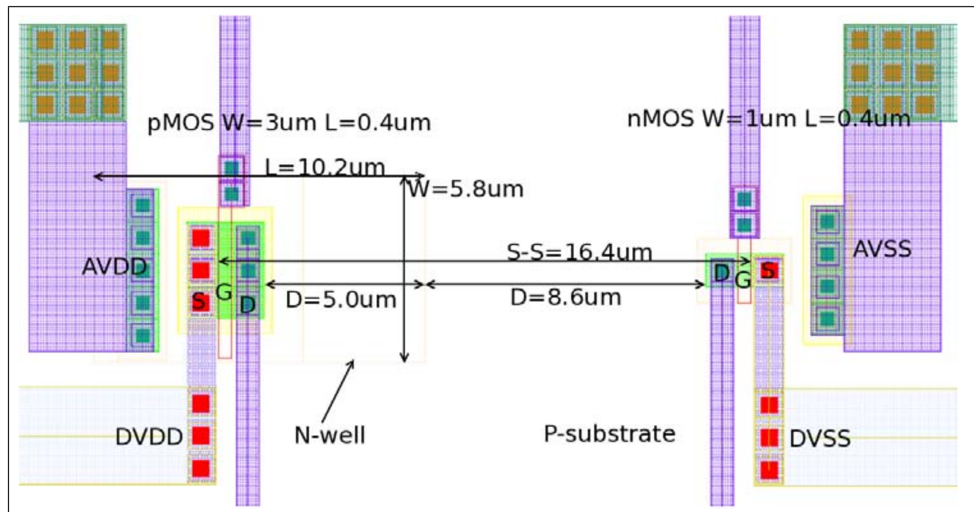

Figure 2.24: An inverter with the N-well increased in size along the X-axis towards the nMOS transistor. The new size is a length of 10.2μm and a width of 5.8μm.

2.5.2 Different diffusion size and contact placement

To investigate the effect of decreased R_{ew} and R_{es} resistance, 6 inverter structures with 3 different source and drain sizes are made to empirically test the latch-up susceptibility. The inverter with the largest source and drain size are made with 3 additional versions where different connection options are investigated. The source and drain areas are expanded only in one direction, relative to the standard inverter, as can be seen in figure 2.26 (see Appendix A for the other structures).

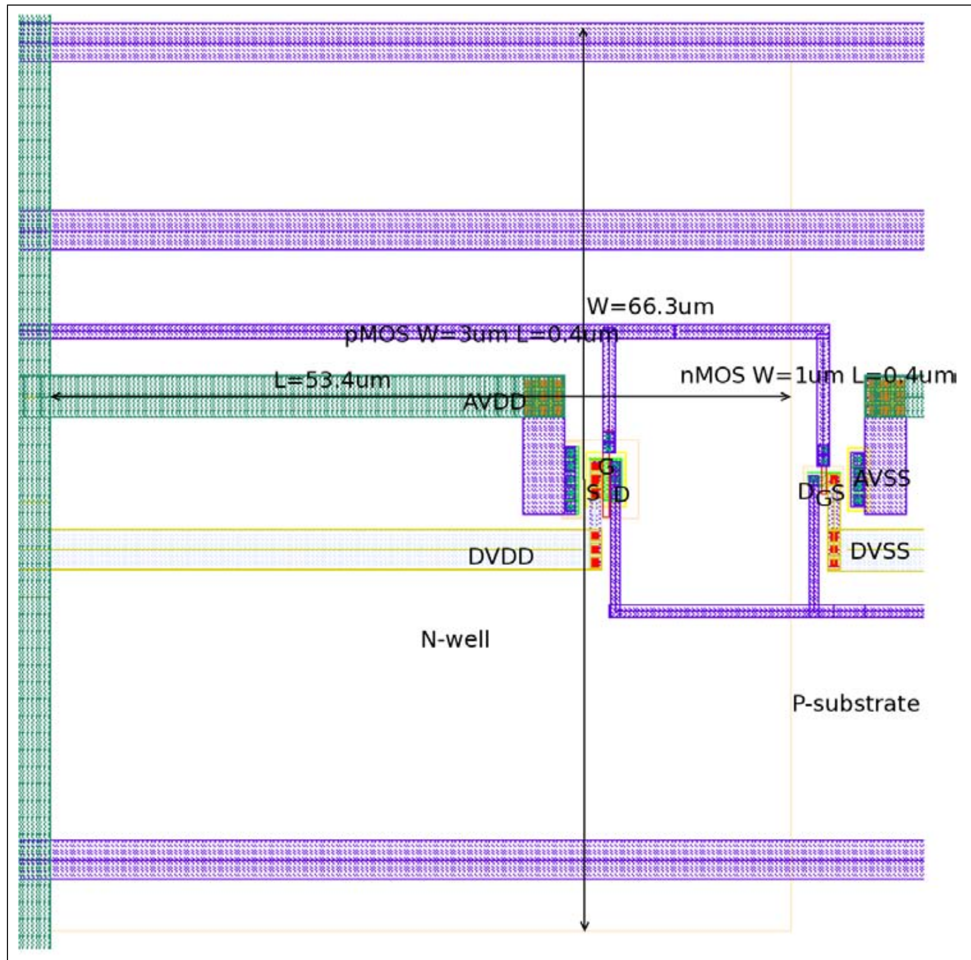

Figure 2.25: An inverter with the N-well increased in size along the X-axis and Y-axis in both directions. The new size is a length of 53.4μm and a width of 66.3μm.

The structures shown in figure A.56, A.57 and A.58 are expected to show a minor increase in latch-up susceptibility because of the decreased R_{ew} and R_{es} resulting in a lower V_{trig} (Eq. 1.6) and I_{trig} (Eq. 1.7 and 1.8). A downside with these test structures is the effect of decreasing P+/N+ contacts to source spacing and the drain to source distance as the source and drain area increases. When the source area increases, it expands in the direction towards the P+/N+ contacts decreasing the resistance R_{bw} and R_{bs}, this makes the circuit less susceptible to SEL and is explained in chapter 2.4. When the drain area increases, it expands in the direction towards the other transistor decreasing the distance between the drain and source of the two transistors. This results in a decreased width of the diffusion in the parasitic BJTs and a more latch-up susceptible circuit as explained in chapter 2.2. The effect of decreasing R_{ew} and R_{es} and the decreasing diffusion makes it difficult to sift out the effect of the increasing source/drain area. Though it is difficult to design test structures which explore only the effect of decreasing R_{ew} and R_{es}. The source/drain areas necessarily have to expand in some direction and the source-contact

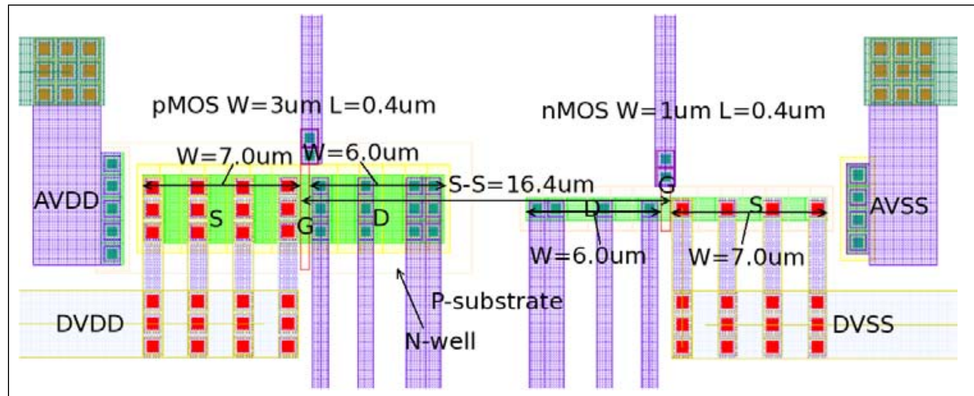

Figure 2.26: An inverter with source areas 7x and drain areas 6x the standard inverter.

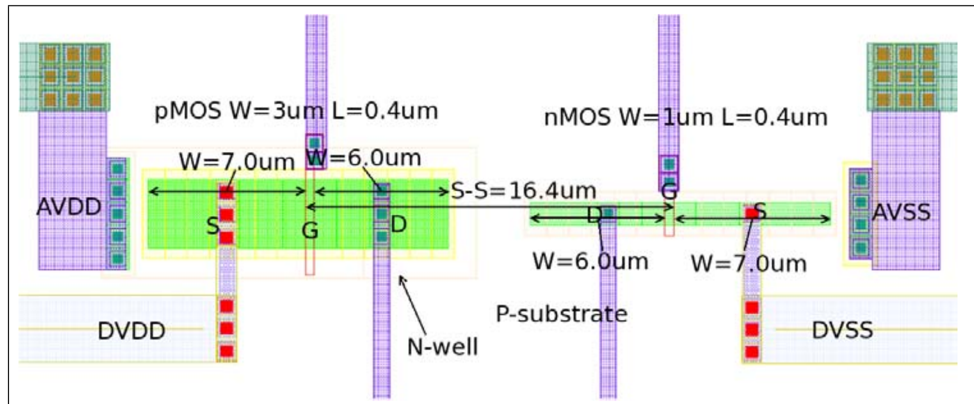

Figure 2.27: An inverter with source areas 7x and drain areas 6x the standard inverter, here with power/ground connection in the middle of the source/drain.

resistances R_{bw} and R_{bs} and the β of the BJT's will be affected by this in some manner.

The structure shown in figure 2.27 (see Appendix A for the other structures) is made to investigate different contact placement on a large source/drain area. Because of the sheet resistance in the diffusion of the source and drain areas are less than the N-well sheet resistance (but larger than the P-substrate sheet resistance), the contact placement may have some impact on the SEL threshold. If the source contact is placed far away from the P+/N+ contact, the source diffusion resistance may cause a larger voltage drop between them in comparison to a closer placement of the contacts. Depending on the sheet resistance of the diffusion the effect may be decisive or not. By comparing the SEL threshold of the different structures a conclusion wether the different contacts placement has an effect or not on SEL threshold.

2.6 Transistor width

To investigate the effect of transistor width on SEL, 16 different inverter structures are made with 8 different transistor widths. The source-source distance of the inverters are set to be 5.4μm, the minimum distance allowed by the design rules (DRC). The relationship between the width of the pMOS and the nMOS is set to be $W_{pMOS}/W_{nMOS} = 3$ to maintain the same “pull up” and “pull down” properties of the inverter. The different widths of the transistors can be seen in table 2.2.

Str.	W_{pMOS}	W_{nMOS}
E1	4.5μm	1.5μm
E2	6.0μm	2.0μm
E3	7.5μm	2.5μm
E4	9.0μm	3.0μm
E5	12.0μm	4.0μm
E6	15.0μm	5.0μm
E7	18.0μm	6.0μm
E8	21.0μm	7.0μm
E9	4.5μm	1.5μm
E10	6.0μm	2.0μm
E11	7.5μm	2.5μm
E12	9.0μm	3.0μm
E13	12.0μm	4.0μm
E14	15.0μm	5.0μm
E15	18.0μm	6.0μm
E16	21.0μm	7.0μm

Table 2.2: The transistor width of the different test structures in column E.

The inverters are made in 2 different versions, one version with the transistors placed in parallel along the Y-axis and one version with the transistors placed one after the other along the X-axis (see figure 2.28, 2.29, 2.31 and 2.32).

2.6.1 Wide nMOS and pMOS in parallel

When the transistors in the inverters are placed in parallel as shown in figure 2.28 and 2.29, the distance between the source of the transistors are fixed, but the drain of the first transistor is even closer to the source of the second transistor. This means that when one of the transistors are in a conducting state, the drain has almost the same potential as the source, making the base of the parasitic BJT shorter and wider, increasing its gain (β). Another disadvantage with this layout of the transistors is observed when the width of the transistors is increased. The width of the parasitic BJT’s increase proportionally with the width of the MOS transistors, increasing the gain of the BJT’s. When designing the structures, a choice was made to increase the number of N-well/P-substrate contacts

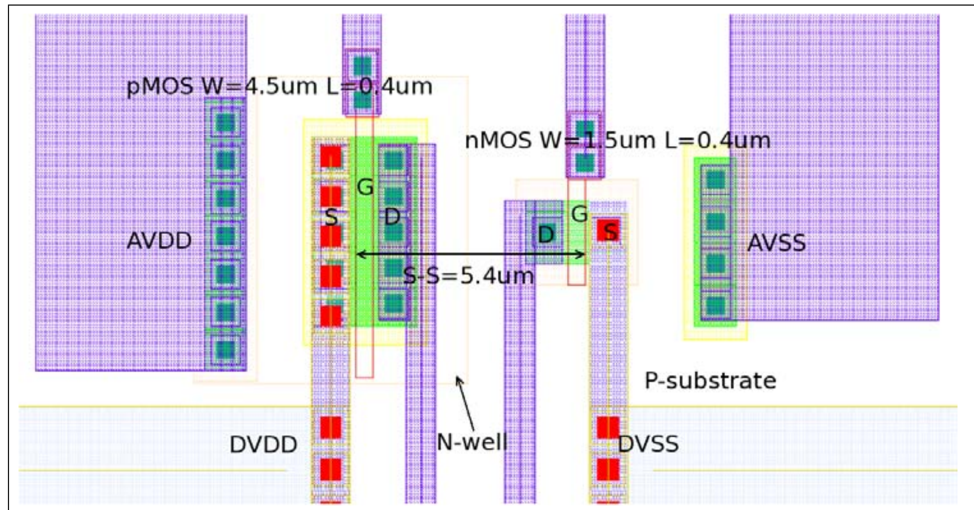

Figure 2.28: An inverter with transistor width of W_{pMOS} = 4.5μm / W_{nMOS} = 1.5μm. The transistors are placed in parallel along the Y-axis.

in accordance with the transistor width. This resulted in a decreasing R_{bw} and R_{bs} as the transistor width was increased. Figure 2.30 presents how the trigger current is affected by both increasing β and decreasing R_{bw} and R_{bs} when the transistors are placed in parallel, and is only intended as an illustration.

2.6.2 Wide nMOS and pMOS turned 90°

In structure E9-E16, the transistors are placed one after the other as shown in figure 2.31 and 2.32, both the drain and source is distanced from each other by the same distance. The drain still contributes to increase the gain of the parasitic BJT's because of the increased length of the diffusion region, but in a smaller manner because the source-drain distance is the same as the source-source distance. Increasing the width of the transistors when they are placed in this way has a smaller effect on the parasitic BJT's gain in comparison to the parallel layout of the transistors. When the width of the transistors is increased, the added area of source/drain is distributed over an increasing length away from the source/drain of the other transistor. This leads to a smaller increment of β in comparison to the parallel layout of structure E1-E8. These structures were also designed with increasing N-well/P-substrate contact in accordance with the transistor width. This resulted in a decreased R_{bw} and R_{bs} as the transistor width increased.

The area penalty of using this layout technique is initially zero because the same components are used, they are just placed at different angles (see table 2.1). However, it may be beneficial or non beneficial in terms of area to place the transistors in this way depending on the designer or the design to be implemented. Figure 2.33 presents how the trigger current is affected by both increasing β and decreasing R_{bw} and R_{bs} when the transistors is placed one after the other, and is only intended as an illustration.

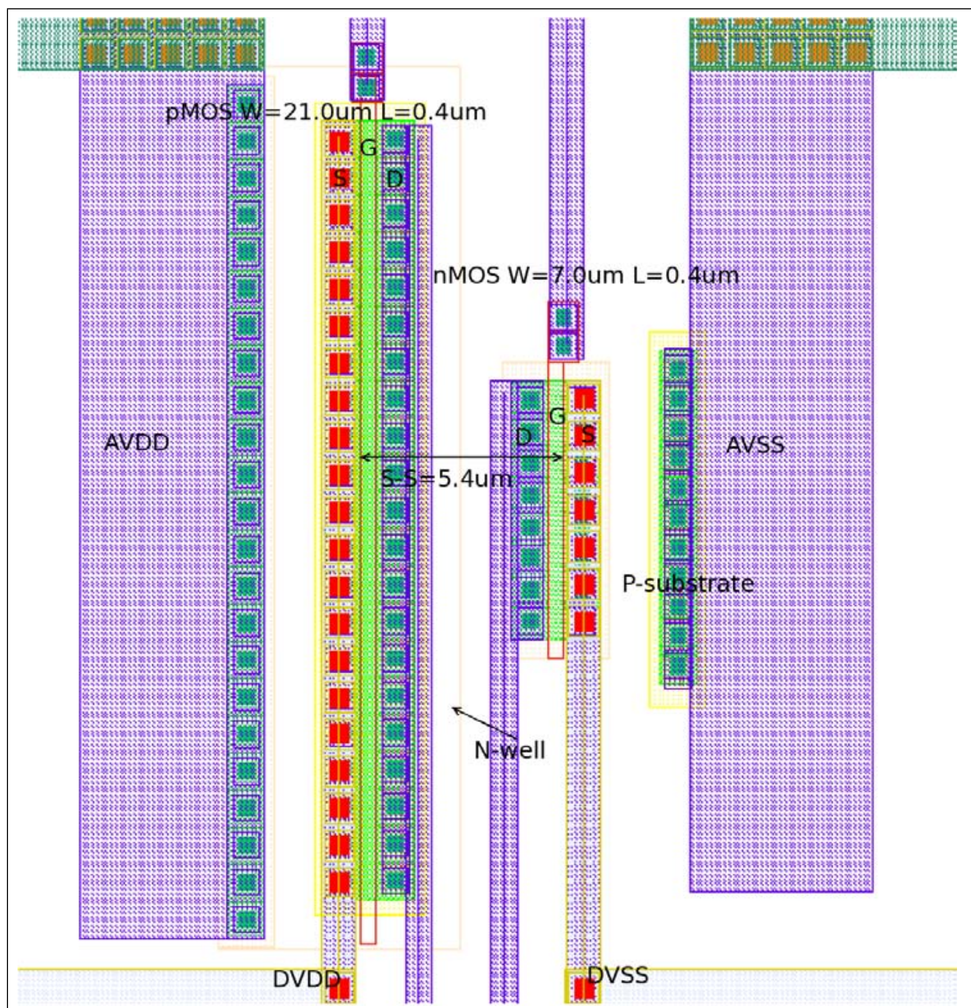

Figure 2.29: An inverter with transistor width of W_{pMOS} = 21.0μm / W_{nMOS} = 7.0μm. The transistors are placed in parallel along the Y-axis.

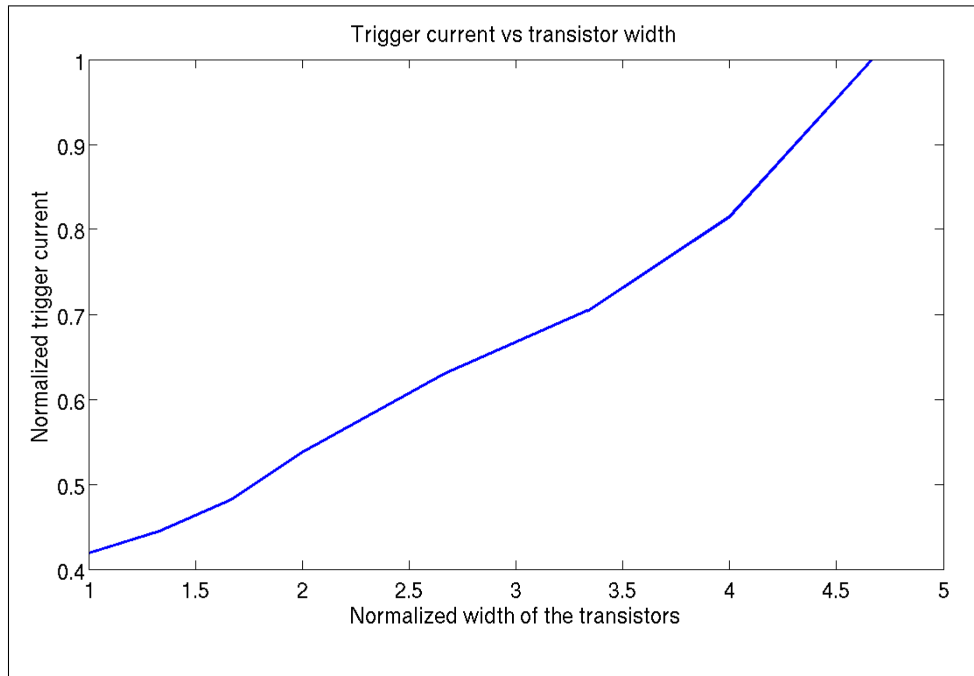

Figure 2.30: Normalized trigger current as a function of nMOS and pMOS width placed in parallel along the Y-axis. The curve follows Eq. 1.7 and is only intended as an illustration to show the effect of increased transistor width.

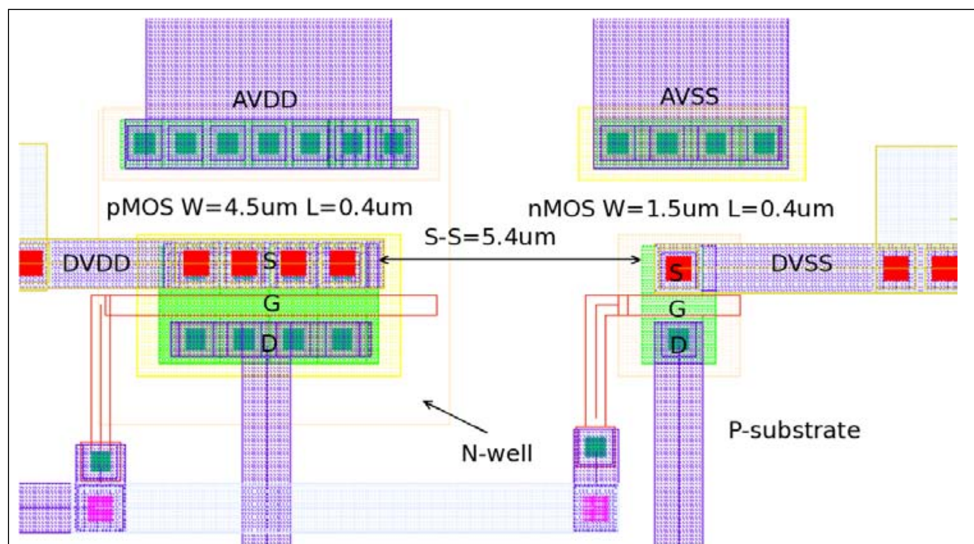

Figure 2.31: An inverter with transistor width of W_{pMOS} = 4.5μm / W_{nMOS} = 1.5μm. The transistors are placed one after the other along the X-axis.

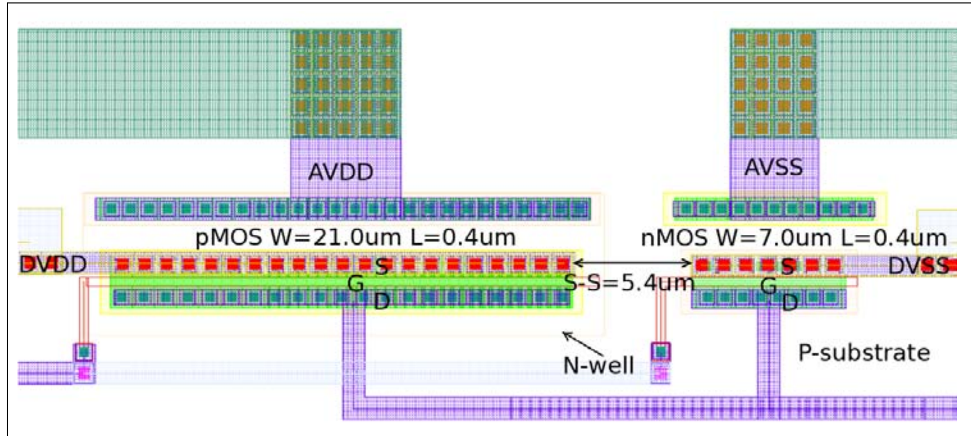

Figure 2.32: An inverter with transistor width of W_{pMOS} = 21.0μm / W_{nMOS} = 7.0μm. The transistors are placed one after the other along the X-axis.

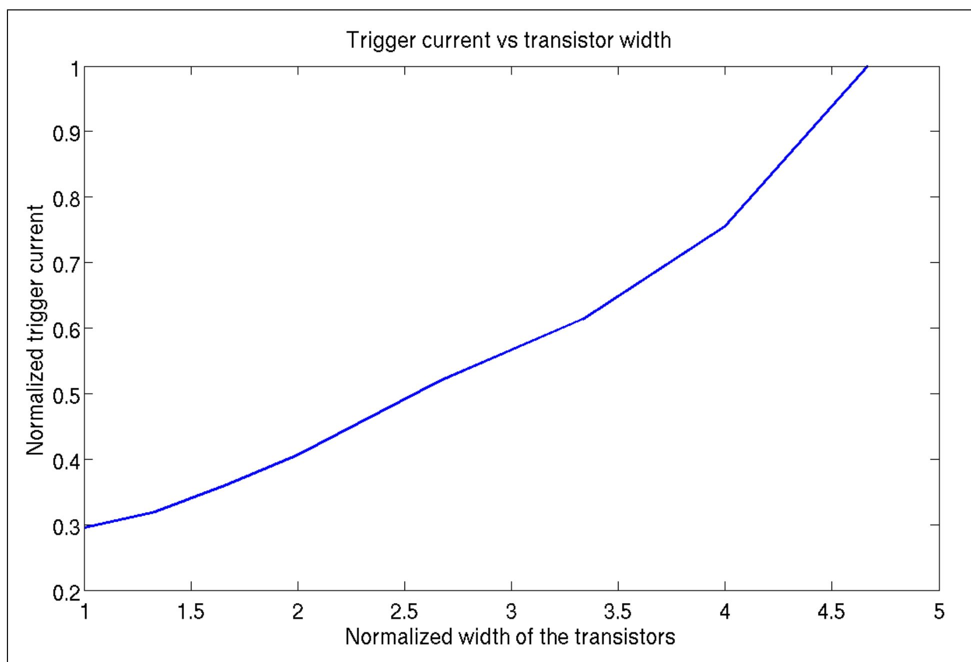

Figure 2.33: Normalized trigger current as a function of nMOS and pMOS width when the transistors are placed one after the other along the x-axis. The curve follows Eq. 1.7 and is only intended as an illustration to show the effect of increased transistor width.

Chapter 3

The test bench

3.1 The laser beam

3.1.1 Laser beam vs heavy particle

SEL threshold can be determined by exposing the device to radiation from a particle accelerator and characterized in terms of Linear Energy Transfer (LET). LET is a measure of the energy deposited from an ionizing particle traveling trough a material. The energy transferred from radiation into silicon in typically denoted in units of $MeV \cdot cm^2/mg$ of material, and arises from a combination of the energy transferred to the material per unit length (MeV/cm) divided by the materials density (mg/cm^3) [43]. Meaning that the higher LET level the device can handle before latch-up is induced, the more hardened it is. The drawback with performing these measurements in an accelerator or cyclotron is the enormous costs this causes. Using a cyclotron is also a very time-demanding procedure because of the safety procedures which have to be maintained at all times. As an alternative to a particle accelerator, one can use a pulsed laser-beam to initiate SEL. The absorption of a laser-beam that produces an electron-hole pair in the semiconductor material is quite similar to the interaction of a cosmic ray. Although the initial charge profile produced by the cosmic ray is somewhat different from the laser-beam, the interactions occur at a very short timescale, much shorter than of most microelectronic devices. Both events are capable of generating SEL in IC's because of the highly localized charge trail trough the semiconductor.

Testing with heavy ions from a cyclotron results in irradiating the whole device, making it impossible to locate the location of the latch-up, only indicating whether or not it happened. The pulsed laser-beam is focused trough a microscope down on the Device Under Test (DUT), and depending on the microscope the focused laser-dot can be as small as 1μm (but not smaller than the wavelength of the light). The advantage with a pulsed laser is the simplicity and price of the test module as well as the accuracy of the laser-beam. Using an x-y positioning board, the sensitive nodes in the design can be located by scanning the desired parts or the entire chip irradiating it with different laser pulse energies. Laser-beams can also be synchronized with external equipments,

providing temporal information that cannot be obtained with particle-beam testing. There are difficulties using a focused laser-beam in SEL testing because laser light cannot penetrate metal as particle-beams are able to, leaving shadowing beneath the metal lines. Also because of the optical effects like reflection, diffraction, absorption in polysilicon layers etc. the correspondence of incident laser energy to LET is violated [6]. These factors limit the quantitative comparisons between laser-beam and particle-beam irradiation.

In the case of pulsed laser incidence, charge carriers are generated by means of photoelectric absorption. Each laser photon generates one single electron-hole pair and according to [16] and [35] the deposited charge dependence on incident laser energy can be calculated;

$$Q_{dep_las} = T\frac{E_L}{E_P}\left(1 - e^{\alpha d}\right) \tag{3.1}$$

Where "T" is the energy transmission coefficient of the surface of the semiconductor, "E_L" is the incident laser energy, "E_P" is the amount of energy necessary to create a electron-hole pair (3.6eV in Silicon), "α" is the wavelength dependent optical absorption coefficient and "d" is the active absorption depth. In order to relatively compare the different structures, the structures have to be exposed to the pulsed laser at different energies. The higher laser energy needed to induce SEL, the less susceptible the structure is to SEL. Because it is a linear relationship between the laser energy and deposited charge into the silicon (Eq. 3.1), a conclusion of the effectiveness of the structures can easily be drawn. By using a laser with wavelength of 1.064μm the absorption depth (d) is about 700μm and is nearly ideal in comparison to a particle strike [22].

3.1.2 The laser module

The laser module used in this project is a "EzLaze 3 Nd:YAG Laser Cutting System"[33]. This module can deliver wavelengths of 1064nm(IR), 532nm(green) and 355(UV) with pulselengths of 3-4ns and energies up to 600μJ. As mentioned, the 1064nm(IR) wavelength is ideal for inducing SEL [3] and is the wavelength to be used on all tests. The laserspot size can be adjusted in X and Y directions and the smallest spot with the IR wavelength is 2x2μm and can be achieved using a 100x objective on the microscope. The maximum energy of 600μJ is achieved with the largest possible aperture of $27.6\mu m * 27.6\mu m = 762\mu m^2$, but in this project the minimum aperture of $2\mu m * 2\mu m = 4\mu m^2$ is used. Because the aperture size is adjusted by 2 blades moving in and out of the laser beam path, the maximum energy scales with the aperture area resulting in a maximum energy of $600\mu J \cdot 4\mu m^2 / 762\mu m^2 = 3.15\mu J$. The laser intensity could be adjusted with energy setting levels ranging from 0-100, though this is not percentages as can be seen in figure 3.1. The setting used in this project follows the "IR-UV Lo" slope which is a low energy setting used to attenuate the laser energy in order to gain a higher energy resolution at lower energies. If a structure is to be triggered into latch-up when the laser

energy setting is at 50, figure 3.1 shows that the laser energy is at 20% of the maximum energy.

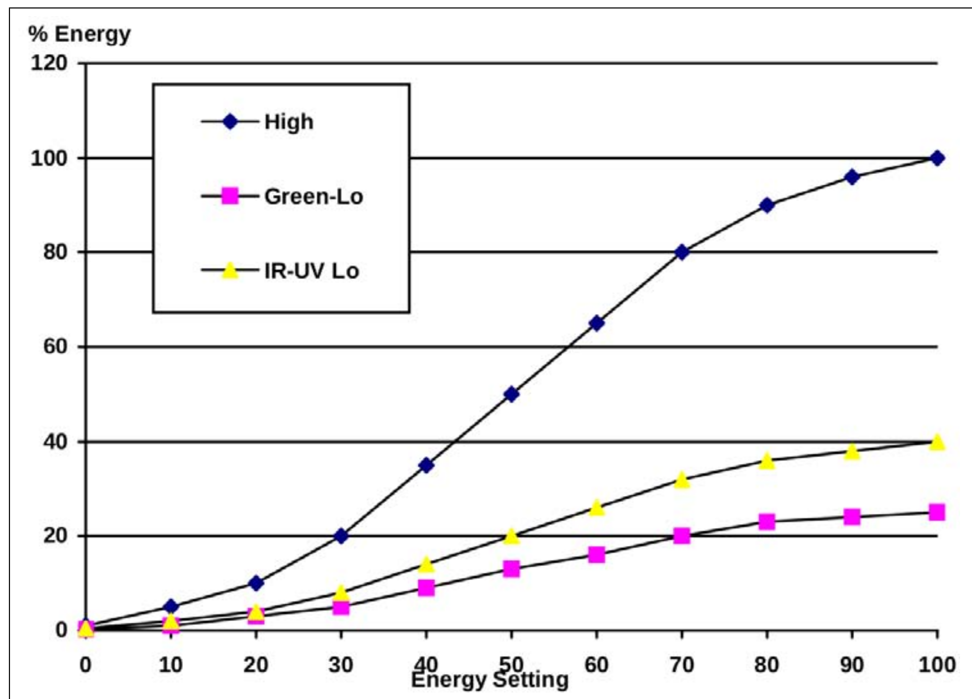

Figure 3.1: Laser energy slope. The setting used in this project was the ”IR-UV Lo“slope [33].

3.2 The printed circuit board

The test device had to be mounted to a Printed Circuit Board (PCB) to enable power connection and measurements as well as physical handling (see figure 3.2). When designing the PCB, some practical considerations had to be made with regards to the laser module. Because the exact dimensions of the laser module was not available at the time of PCB design, some assumptions had to be made. The focus distance of the microscope was known, but not the size of the lens. The microscope had a focus distance of 1.1cm so all the components were placed at the outer edge of the PCB while the ASIC was placed at the center to prevent the testpins and switches from bumping into the lens. When using microscopes with 100x zoom the focus rage becomes extremely narrow, a device to fasten the PCB was used in order to stabilize it. Decoupling capacitors were used to minimize noise, though they were placed far away from the chip so their effect are limited. A 0Ω resistance was also mounted in series with every power connection pin in case a series resistance was to be relevant. 7 Switches was mounted in order to control the input signals by hand in addition to the inputpins in case the inputs had to be controlled by a computer. The soldering pads and bonding pads were gold plated to ensure good connection, the testpins were hole mounted in order to withstand the physical stress and the decoupling

capacitors, resistances and switches were surface mounted in order to save space. 15 test cards were made with the opportunity to mount and test 2 test devices. The test devices were mounted and bonded on the PCB at Gamma Medica Ideas by their engineer. 10 PCB were mounted with the test device made in the AMS 0.35μm C35B4O1 option and 5 PCB were attached with the device made in the AMS 0.35μm C35B4C3 option.

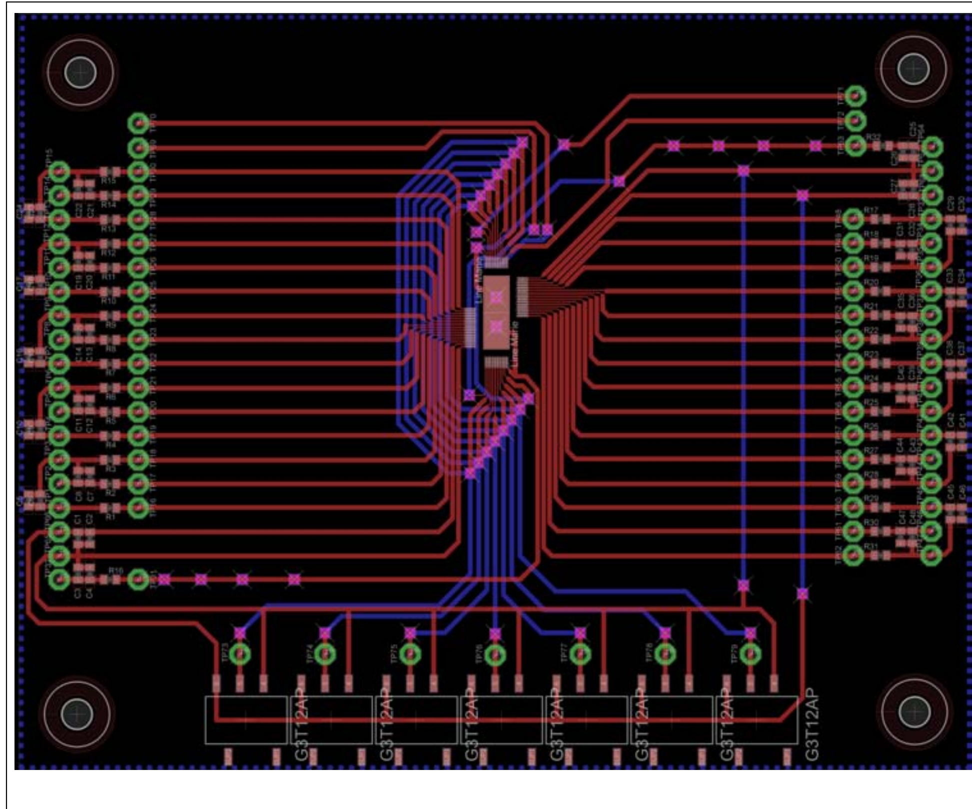

Figure 3.2: Layout of the PCB before production

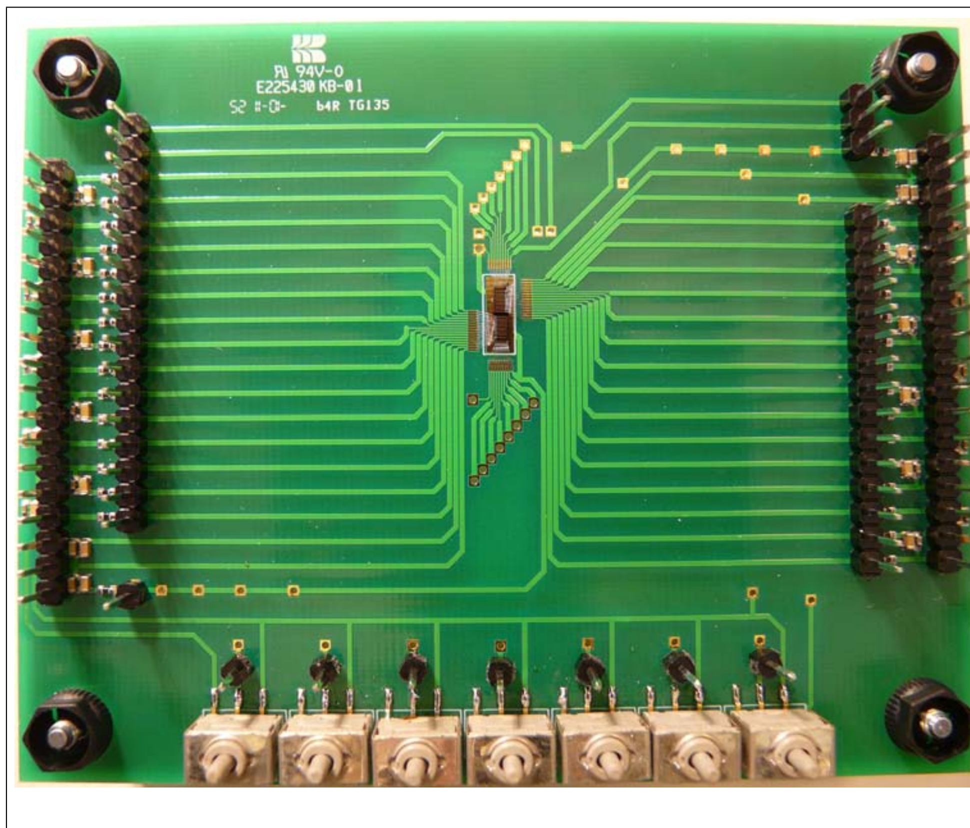

Figure 3.3: The finished PCB with the test device and all the other components mounted, ready to be used.

3.3 Measurement setup

The equipment needed to implement the tests:

- Agilent E3631A Power Supply.
- Agilent 33120A Signal Generator.
- Agilent 34401A Digital Multimeter.
- Agilent 54624A Oscilloscope.
- EzLaze 3 Nd:YAG Laser Cutting System.

The test device was supplied with a DC voltage of 3.3V and a digital input signal of 100kHz in order to emulate a realistic working environment. The multimeter was applied in series with the analog Vdd (Avdd) and digital Vdd (Dvdd) (see figure 2.2) input pins in order to measure the current delivered to the teststructures only and not the control logic. The oscilloscope was used to measure the output signal from the teststructures in order to determine which structure malfunction, in the sense that they experienced latch-up (see figure 3.4).

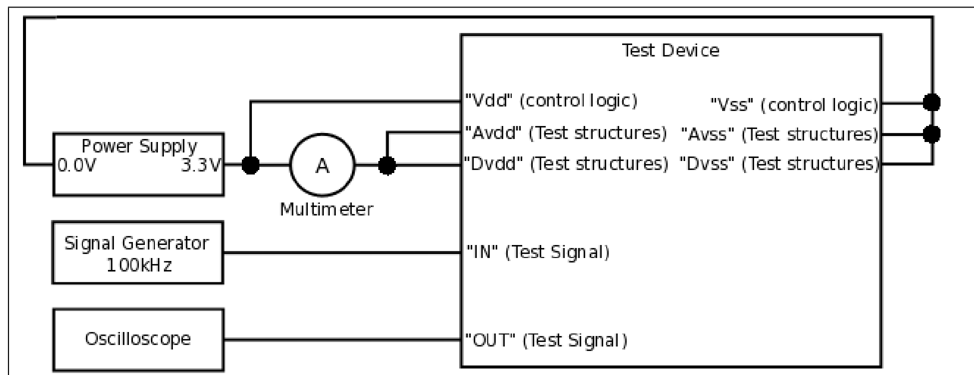

Figure 3.4: A schematic of the power supply, multimeter, signal and oscilloscope connection on the test device.

The PCB was fastened with a jig in order to gain stability and the microscope was manually focused down on the chip. The microscope held the possibility of using a camera and a external screen in order to see more detail and not have to look trough the goggles. The structures were found by moving the microscope in X and Y direction over the test device and by using a red light as the aiming dot for both the laser size, shape and position. The laser spot were first adjusted to the right size of 2x2μm and then positioned as accurate as possible in the middle between the two nMOS and pMOS of the inverter structure (see figure 3.5). Each structure were exposed to the same laser pulse energy 10 times with a frequency of 1Hz before the energy was increased to the next energy level in the attempt to initiate SEL. When SEL was successfully induced, the SEL current was promptly read out and the device was reset as quickly as possible in order to reduce the damage caused by the high currents. Because the temperature of the test device increased when latch-up was induced, a cooling period of 30 seconds was awaited before the next structure was exposed. The same

procedure was carried out for all the structures in 5 bulk devices and 5 epitaxial devices.

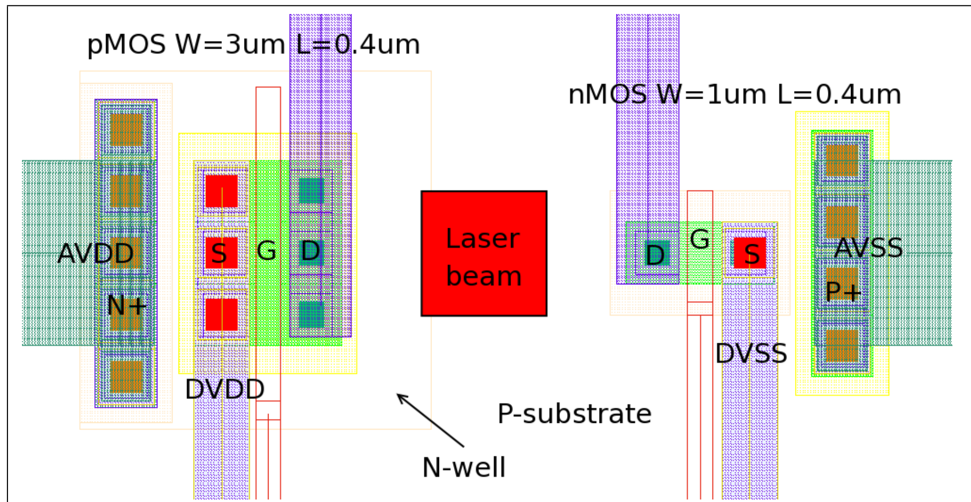

Figure 3.5: Location of the laser spot on structure C1, the same relative position (in the middle between the nMOS and pMOS) was used through all the structures.

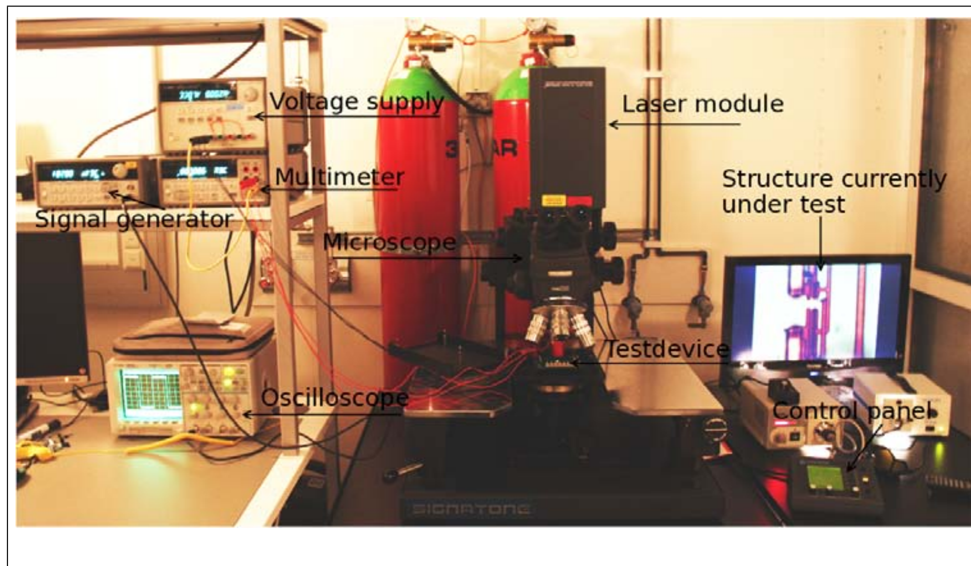

Figure 3.6: A picture of the testbench with the laser module, the test device and measurement equipment.

Chapter 4

Results

The test devices were designed with assistance from Gamma Medica Ideas at their facilities and were produced in two different options of the AMS 0.35μm technology, one option with exitaxial substrate (C35B4O1) and the other with bulk (C35B4C3).

The results are represented in tables, each column of its own. Some of the columns did not experience SEL and these structures are not presented in the results. Each table show both the SEL laser energy threshold (E_{th}) and SEL current (I_{SEL}) for all the structures in the column. Five devices were tested for SEL and all the data is presented in the tables. SEL current is denoted in mA and is the total current usage of the test device when experiencing latch-up, SEL energy threshold is presented in the energy setting displayed on the laser module. This energy threshold setting can be translated into a percentage of the maximum energy of 3.15μJ by using the "IR-UV Lo"slope in figure 3.1 (explained in chapter 3.1).

Comparisons between the measured energy trigger levels with the trigger current calculated with Eq. 1.7 and 1.8 is performed. The energy trigger levels measured, as well as the calculated trigger current, is normalized to the highest trigger level or trigger current respectively. By doing this, comparison between trigger energy level and trigger current can be done relatively, but it is not possible to tell if the measured energy level of one structure is high in comparison to the calculated level. Comparison between normalized trigger current and normalized energy trigger level can be done because it is a linear relationship between laser energy and the deposited current in the silicon (see Eq. 3.1.

Because the power usage of the test device is about 300μA (depending on which column is under test), this current can be neglected. The laser spot is the same size (2x2μm) under all the test, so are the laser wavelength.

Table 4.2-4.5 shows that there are relatively large differences between the thresholds of the same structures when a comparison between the different epitaxial and bulk test-devices are done. These differences can be caused by both mismatch and process variations between different devices as well as uncertainties in the testbench and measurements. A deviation of about 20% in the measured values can be expected. Though the same tendencies can be seen in both energy threshold and SEL current across

the 5 devices.

4.1 Column A bulk device, nMOS to pMOS spacing

Str.	E_{th} 1	E_{th} 2	E_{th} 3	E_{th} 4	E_{th} 5	I_{SEL} 1	I_{SEL} 2	I_{SEL} 3	I_{SEL} 4	I_{SEL} 5
A1	8.2	7.8	7.8	9.4	9.0	43.0	44.5	43.5	44.0	44.0

Table 4.1: Energy threshold (E_{th}) and latch-up current (I_{SEL}) measured after exposing column A on 5 different bulk devices. Latch-up current is denoted in mA and energy threshold is specified in the energy setting displayed on the laser module. This energy threshold setting can be translated into a percentage of the maximum energy of 3.15μJ by using the ”IR-UV Lo“slope in figure 3.1.

In column A (see figure 2.2), structure A1 (figure A.1) was the only structure to experience SEL by exposure of the laser pulse. Structure A1 is the standard minimum inverter used by GMI and is the reference structure used to compare with the other structures. Structure A2-A16 (figure A.2-A.16) did not experience SEL even with a laser energy high enough to burn the surface of the device. No useful useful data regarding anode-cathode spacing can be extracted from these results.

4.2 Column C epitaxial device, source-contact spacing

Structure C2-C5 explores different contact placement including butting of the contacts and transistor source (see Appendix A). Good results and useful data can be extracted from these measurements and clear tendencies can be seen (see Appendix B B, table B.2 for all the results). When comparing structure C1-C5, structure C2 stands out with a significantly lower SEL threshold and the highest SEL current, while C4 shows to have a slightly higher SEL threshold than all the other structures. Structure C6-C11 shows no clear correlation between source-contact spacing and SEL threshold, though a vague increment in the SEL threshold as the spacing increases can be seen. The last five structures with source-contact spacing of 6.5μm - 20.5μ m shows a dramatic decrease in SEL threshold from C11 to C12, as well as a consistent decrease in SEL threshold as the spacing increases.

4.3 Column C bulk device, source-contact spacing

Similar to what the results from column C with epi-layer shows, structure C2 has a significantly lower SEL threshold than the reference structure C1.

Str.	E_{th} 1	I_{SEL} 2
C1	28.3	46.2
C2	5.0	56.5
C3	28.5	46.3
C4	30.0	46.3
C5	27.6	46.3
C6	27.7	46.3
C7	28.3	46.3
C8	28.2	46.3
C9	28.1	46.3
C10	29.3	46.3
C11	29.3	46.3
C12	8.5	37.8
C13	7.2	40.9
C14	5.9	44.3
C15	5.4	44.8
C16	4.0	45.8

Table 4.2: Average energy threshold (E_{th}) and latch-up current (I_{SEL}) measured after exposing column C on 5 different epitaxial devices. Latch-up current is denoted in mA and energy threshold is presented in the energy setting displayed on the laser module. This energy threshold setting can be translated into a percentage of the maximum energy of 3.15μJ by using the ”IR-UV Lo“slope in figure 3.1.

Str.	E_{th} 1	I_{SEL} 2
C1	47.5	58.3
C2	6.2	56.5
C3	-	-
C4	-	-
C5	-	-
C6	-	-
C7	-	-
C8	-	-
C9	6.3	40.7
C10	4.6	46.9
C11	4.0	50.5
C12	2.0	53.8
C13	0.0	67.3
C14	0.0	67.3
C15	0.0	67.3
C16	0.0	67.3

Table 4.3: Average energy threshold (E_{th}) and latch-up current (I_{SEL}) measured after exposing column C on 5 different bulk devices. Latch-up current is denoted in mA and energy threshold is presented in the energy setting displayed on the laser module. This energy threshold setting can be translated into a percentage of the maximum energy of 3.15μJ by using the ”IR-UV Lo“slope in figure 3.1.

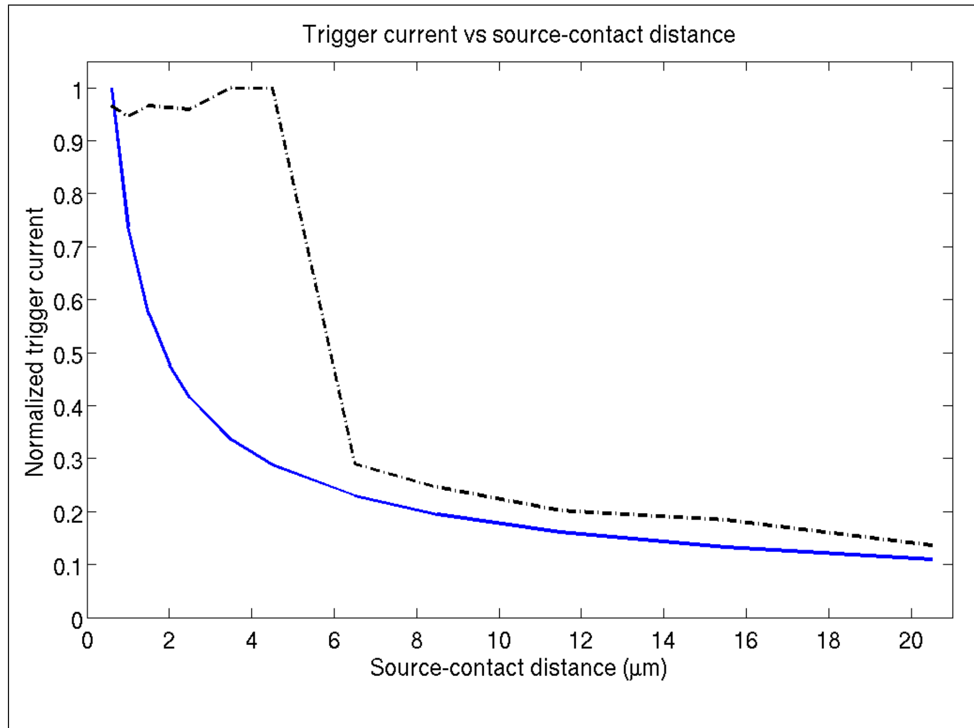

Figure 4.1: Normalized trigger current as a function of source-contact distance in the epitaxial device. The solid line represents Eq. 1.5 and the dotted line represents the average trigger setting level of C1 and C6-C16 over the 5 devices (see table 4.2).

The structures C3-C8 did not experience SEL at any laser energy levels. If one assume a too high threshold to experience latch-up in the structure C3-C8, a dramatic decrease in SEL threshold is shown in structure C9-C16 (as the contact-source spacing increases from 2.0μm to 2.5μm). An interesting tendency in the SEL current is that it increases from C9-C12 and that structure C13-C16 has a much higher SEL current than the other structures. The threshold of C13-C16 is at such a low level that they trigger each other when being exposed to the laser pulse. The output of all four structures malfunction and the SEL current measured is at a level about 4 times higher than the other structures (see Appendix B B, table B.3 for all the results).

4.4 Column D bulk device, N-well and diffusion size

Structure D1-D7 did not experience SEL at any laser energy levels. When structure D8 was exposed to the laser, SEL was triggered, but the output of D8 was still functioning. Though, the output of D9-D13 malfunctioned, which implies that structure D8 did not experience latch-up, but the laser pulse focused on D8 actually triggered structure D9-D13 because of their low SEL threshold. When exposing structure D9-D12 to the laser, structure

Str.	E_{th} 1	I_{SEL} 2
D1	-	-
D2	-	-
D3	-	-
D4	-	-
D5	-	-
D6	-	-
D7	-	-
D8	43.5	54.2
D9	6.4	54.2
D10	5.6	54.2
D11	6.0	54.2
D12	34.4	54.2
D13	36.	60.8
D14	-	-
D15	12.	56.5
D16	10.	42.4

Table 4.4: Average energy threshold (E_{th}) and latch-up current (I_{SEL}) measured after exposing column D on 5 different bulk devices. Latch-up current is denoted in mA and energy threshold is presented in the energy setting displayed on the laser module. This energy threshold setting can be translated into a percentage of the maximum energy of 3.15μJ by using the "IR-UV Lo"slope in figure 3.1.

D9-D13 experienced latch-up, but when exposing D13 to the laser, only D13 experienced latch-up. Structure D9-D11 shows no relationship between source/drain area and SEL threshold, except D10 which have a vague decrease in SEL threshold in comparison to D9 and D11. In D12-D14, a relationship between contact placement on a large source/drain area and SEL threshold is shown. The further away the contact is placed from the transistor gate, the higher SEL threshold. D15 and D16 is a NAND gate and a NOR gate respectively (see Appendix A). The results show that the SEL threshold and current are higher for the NAND gate (see Appendix B B, table B.4 for all the results).

4.5 column E bulk device, transistor width

Structure E1-E8 shows that the SEL threshold depends on transistor width, except E1 which only experienced latch-up on one device. SEL current shows a clearly dependence on transistor width. Even though the thresholds of the same structures differ between the devices in some manner, the results are fairly consistent and shows the same tendencies. Structure E9-E16 did not experience SEL at any laser energy levels (see Appendix B B, table B.5 for all the results).

Str.	E_{th} 1	I_{SEL} 2
E1	9.8	39.5
E2	9.9	56.4
E3	10.3	55.6
E4	10.6	73.3
E5	10.9	84.0
E6	11.1	94.5
E7	11.2	102.9
E8	11.4	112.2
E9	-	-
E10	-	-
E11	-	-
E12	-	-
E13	-	-
E14	-	-
E15	-	-
E16	-	-

Table 4.5: Average energy threshold (E_{th}) and latch-up current (I_{SEL}) measured after exposing column E on 5 different bulk devices. Latch-up current is denoted in mA and energy threshold is presented in the energy setting displayed on the laser module. This energy threshold setting can be translated into a percentage of the maximum energy of 3.15μJ by using the ”IR-UV Lo“slope in figure 3.1.

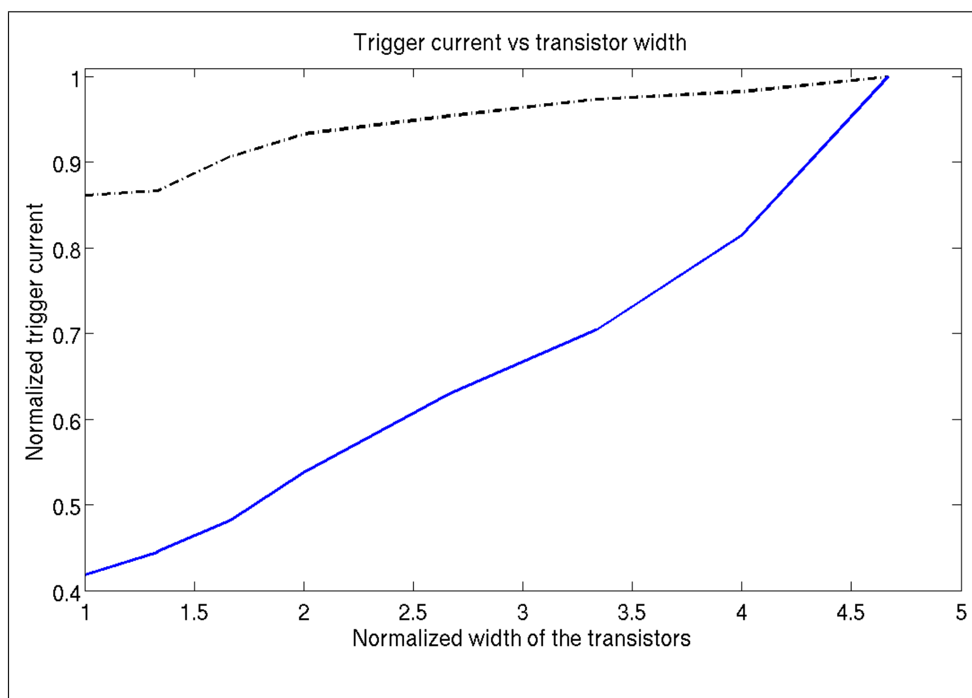

Figure 4.2: Normalized trigger current as a function of normalized nMOS and pMOS width. The solid line represents Eq. 1.5 and the dotted line represents the average trigger setting level of E1-E7 over the 5 devices.

Chapter 5

Discussion

In order to easily compare the results with the theory models, the most important equations are repeated here.

$$\beta = \frac{D_n N_D L_p}{D_p N_A W} \cong 2.5 \frac{N_D L_p}{N_A W} \tag{5.1}$$

$$\alpha = \frac{\beta}{\beta + 1} \tag{5.2}$$

$$I_{trig_{pnp}} \cong \frac{V_{th_{pnp}} + V_{Rew}}{R_{bw}} + \frac{V_{th_{npn}} + V_{Res}}{\beta_{pnp} R_{bs}} \tag{5.3}$$

$$I_{trig_{npn}} \cong \frac{V_{th_{npn}} + V_{Res}}{R_{bs}} + \frac{V_{th_{pnp}} + V_{Rew}}{\beta_{npn} R_{bw}} \tag{5.4}$$

$$V_{hold} = max(V_1, V_2) \tag{5.5}$$

$$V_1 \approx I_{Res}(R_{es} + \alpha_{npn} R_{cw}) + I_{Rew} R_{ew} + V_{th_{pnp}} \tag{5.6}$$

$$V_2 \approx I_{Rew}(R_{ew} + \alpha_{pnp} R_{cs}) + I_{Res} R_{es} + V_{th_{npn}} \tag{5.7}$$

$$I_{tot} = \frac{VDD \cdot \alpha_{pnp}}{R_{ew} + R_{cs} + R_{bs}} + \frac{VDD \cdot \alpha_{npn}}{R_{bw} + R_{cw} + R_{es}} \tag{5.8}$$

5.1 Column A, nMOS pMOS spacing - Difficult to induce SEL

In column A (see figure2.2 and Appendix A) the goal was to explore the effect of increasing distance between the nMOS and pMOS in an inverter structure.

With the laser module used in these tests, no SEL could be triggered in this column in the epitaxial device. An assumption can be made that these structures had too high SEL threshold to be triggered into latch-up with the actual laser module.

In the bulk device, structure A1 was the only structure that could be triggered into latch-up with the actual laser module. An assumption can also be made here that these structures had too high SEL threshold to be triggered into latch-up.

The average energy level to trigger structure A1 were 8.4 and the average SEL current were 44mA. This will be the reference energy level to compare the other structures up against.

The reason no of the other structures could be triggered into latch-up could be that the holding voltage (V_h) is to high (higher than Vdd of 3.3V), which means that the structure could theoretically be immune to SEL. Another reason could be that the SEL threshold is practically too high in order for the structures to be triggered by the laser beam without burning the silicon. Though a high energy particle could still manage to trigger SEL if the energy is high enough.

In [27] anode-cathode spacing was investigated in a 0.8μm technology and presented an increase in trigger current with a factor of 2 when the anode-cathode spacing was increased from 3μm to 9μm. In [31], the same tendencies are shown with a 250nm technology. These results show a more aggressive increase in trigger current as the anode-cathode distance increases than Eq. 5.3 and 5.4 shows in figure 2.6.

Possible future modifications

In order to gain results from these structures in a future device, some modifications could be made to lower the SEL threshold on all the structures. If the N-well/P-substrate contacts are placed further away from the transistor source, the SEL threshold and holding voltage may decrease enough to be able to induce latch-up in some or all of the structures. This implies that the contact-source distance must be constant through all the structures in order to measure the effect of increasing distance between the nMOS and pMOS. Though, because the contact-source distance now has been increased, the SEL threshold of these structures have been lowered in comparison to the current structures. This make the new structures invalid for direct comparison with the reference structure A1. Though, this is just a theoretical assumption and it would be both interesting and beneficial to put it to the test by actually making the structures and implement the tests.

5.2 Column B, guard rings - Unable to induce SEL

In column B (see figure 2.2 and Appendix A) the goal was to explore the effect of minority and majority N+ and P+ guard rings surrounding the MOS transistors.

In either the bulk or epitaxial device SEL could be triggered. As assumed in the previous section, the SEL threshold may be too high in order to trigger latch-up with the actual laser module.

Because SEL could not be triggered, either the SEL threshold, the holding voltage or both are too high for latch-up to be induced or maintained. In theory, this means that the structures are immune to SEL, but as mentioned a high energy particle could still manage to trigger SEL if the energy is high enough.

In [12] and [13] it is shown that the trigger current roughly increases with a factor of 2 when N+ guard rings are applied, and [13] shows that the trigger current is increased with a factor of roughly 5 when P+ guard rings are applied.

Possible future modifications

To enable implementation of the tests, the threshold and holding voltage of the test structures could be decreased by increasing the contact-source distance as explained in the previous section (5.1). Though this would be difficult because the majority guard rings also function as N-well/P-substrate contacts. Another option is to insert a resistance in series with the power or ground connection to the guard rings and contacts [8]. This would decrease the efficiency of both the guard rings and contacts, making the structure more susceptible to SEL, enabling latch-up to be triggered. Though some second order effects may impact the structures making the relative results invalid when removing the resistances. More information would have to be collected and evaluated in order to implement relevant tests with this procedure

5.3 Column C, contact placement - Clear correlation between contact placement and SEL

In column C (see figure 2.2 and Appendix A) the goal was to explore the effect of different N-well/P-substrate contact placement and contact-source spacings.

Productive and consistent results were obtained from both the bulk and epitaxial device. All the structures in the epitaxial device experienced latch-up, though only 10 of 16 structures in the bulk device could be triggered into latch-up. As assumed in the previous sections, the threshold of the structures which did not experience latch-up may have been to high in order to be triggered by the actual laser module.

5.3.1 The epitaxial device

In the epitaxial device, all the structures were triggered into latch-up and the same tendencies were shown through all the 5 test devices. Even though the results shown in 4.2 were not in complete compliance with the theory (see figure 4.1), it does not mean that something is wrong with either the theory nor the measurements performed. Second order effects may have a greater influence than expected and there are always uncertainties when it

comes to the testbench and the configuration, this will be discussed further down.

Structure C1 and C6-C16

Table 4.2 shows that the average trigger energy level of C1 and C6-C11 (see Appendix A figure A.32 and A.37-A.42) are at about 3 times higher than the reference structure A1 (see Appendix A figure A.1) and produce a 5% higher SEL current. The higher SEL current may be a result of decreased anode-cathode spacing, increasing the β/α and thereby the current (see Eq. 5.8.

The structures C12-C16 (see Appendix A figure A.43-A.47) shows a trigger level between 50%-100% of A1 and produces a SEL current +/- 10% of A1. The differing SEL current may be a result of differing R_{bw} and R_{bs} (figure 1.8) and second order effects.

In figure 4.1 the average trigger energy level of C1 and C6-C16 in comparison to the curve of Eq. 1.7 is shown. When the source-contact distance is shorter than 6.5μm the calculated trigger levels differ up to 70% from the measured trigger levels. But when the source-contact distance is longer than 6.5μm, the calculated levels only differ about 10% from the measured trigger levels. A decrease in measured SEL threshold of about 70% is discovered when contacts-source spacing increases from 4.5μm (structure C11) to 6.5μm (structure C12). But only a decrease of about 15% is discovered when contacts-source spacing increases from 6.5μm (structure C12) to 8.5μm (structure C13). As presented in figure 4.1, the distance between 4.5μm and 6.5μm acts like a "threshold" distance. If the contact-source distance is increased beyond this distance, a marked decrease in SEL hardness may occur.

An interesting tendency in the SEL current also shows when the contact-source distance is increased beyond this "threshold" distance. In the structures with a contact-source distance of 4.5μm or less, the SEL current measured an average of 46mA. In structure C12 (contact-source distance of 6.5μ) the SEL current measured an average of 38mA and in structure C13, C14, C15 and C16 the SEL current increased and measured an average of 41mA, 44mA, 45mA and 46mA respectively. A decrease in SEL current was expected as a function of increasing R_{bw} and R_{bs} (figure 1.8) in accordance to Eq. 5.8 when the contact-source distance was increased. But the increase in SEL current when the contact-source distance was increased above 6.5μm was unexpected. This can be explained by the voltage across the shunt resistances, when they increase, the voltage across them increases, leading to a higher voltage over the base-emitter junction of the BJT's.

Structure C2

Structure C2 (see Appendix A figure A.33) measured an average SEL threshold energy level of 5. This presents a 40% lower threshold in comparisson to the reference structure A1 with a threshold of 8.4. The lower threshold of C2 may be caused by the decreased source-source spacing (increased β) of the two transistors as indicated in Eq. 1.7 and 1.8. C2 shows a an average SEL current of 57mA, 20% higher than the reference structure A1. This may also be caused by the increased β (or α) (see Eq. 1.12).

Structure C3

Structure C3 (see Appendix A figure A.34), with a measured average SEL trigger energy level of 28.5 and current of 46mA, presented a 239% higher threshold and 5% higher current than the reference structure A1. This may be a result of the lower R_{bw} and R_{bs} (figure 1.8), resulting in an increased threshold in accordance to Eq. 5.3 and 5.4 and an increased current in accordance to Eq. 5.8.

Structure C4

Structure C4 (see Appendix A figure A.35), with a measured average SEL trigger energy level of 30 and current of 46mA, presented a 257% higher threshold and a 5% higher current in comparison to the reference structure A1. The higher threshold can be a result of the decreased contact-source spacing and the placement of the contacts in between the transistors, functioning as guard rings and decreasing the α of the BJT's. The small increase in SEL current may come from the decreased anode-cathode distance.

Structure C5

Structure C5 (see Appendix A figure A.36), with a measured average SEL trigger energy level of 27.6 and current of 46mA, presented a 228% higher threshold and a 5% higher current in comparison to the reference structure A1. The higher threshold may be a result of the contacts functioning as guard ring. The higher SEL current may be a result of the decreased anode-cathode spacing. Because the contact-source distance is longer than in structure C4, the threshold is 8% lower than in C4.

Possible future modifications

In order to further investigate the effect of both contact placement and contact-source distance, it could be beneficial to create a set of inverter structures with wider nMOS and pMOS or with increasing nMOS-pMOS distance. By varying the contact placement in these structures we can determine whether the same effect occurs when changing different features

of the parasitic BJT's. The same tests should also be done for the bulk device.

5.3.2 The bulk device

In the bulk device, structure C3-C8 (see Appendix A figure A.34-A.39) did not experience SEL at any laser energy level. As assumed in the section5.1 and 5.2, the SEL threshold may be too high in order to trigger latch-up with the actual laser module. Because the bulk device possess a reflective coating against light at the top level, the laser energy may have been attenuated to a level where the deposited energy is too low to induce SEL but still enough to physically damage the top layers.

Structure C1, C2 and C9-C16 (see Appendix A figure A.32, A.33 and A.40-A.47) did experience latch-up and the same tendencies were shown through all the 5 test devices (see table 4.3. When comparing the bulk device with the epitaxial device some of the same tendencies and can be seen across the two different device options as well. When the contact-source distance is 2.0μm or less, the SEL thresholds are too high in order to trigger latch-up, except for C1.

Structure C1

Structure C1 with a measured average SEL trigger energy level of 47.5 and current of 58mA, presented a 465% higher threshold and a 30% higher current in comparison to the reference structure A1. The higher threshold may be a result of the decreased contact-source spacing and the higher current may be a result of decreased anode-cathode spacing in comparison to A1.

Structure C9-C16

Structure C9-C16 had a SEL threshold ranging between 7.4 and down to 0.0 which is the lowest energy level setting of the laser module, meaning a decrease in threshold of 12% or more in comparison to the reference structure A1. Similar to what experienced with the epitaxial device, it seems to be a contact-source "threshold" distance. When the contact-source distance is 2.0μm or more, the threshold drops dramatically and the structures become much more susceptible to SEL. The "threshold" distance of the bulk device (2.0μm-2.5μm) seems to be at a shorter distance in comparison to the exitaxial device (4.5μm-6.5μm).

Based on these observations, it can be assumed that the epitaxial device hold an advantage over the bulk device when it comes to contact placement dencities. Using an epitaxial device, the contacts can be placed further away from the transistor, reducing the layout area without experiencing the observed threshold drop.

The SEL current of C9-C12 is increasing from an average level of 41mA to a level of 54mA as the contact-source distance is increasing. The

SEL current of structure C13-C16 cannot be determined because all the 4 structures were triggered into latch-up at once. The current measured was the total SEL current of these 4 structures, but if we split the average current measured on the 4 structures we get an average SEL current of 269mA/4 = 67mA on these structures. The reason for the current increment may be that the voltage applied to the base-emitter junction of the BJT's increases as a result of the increasing R_{bw} and R_{bs} (figure 1.8), increasing the α of the BJT's. The increment in SEL current can be explained by an increase in the voltage across the shunt resistances (R_{bw} and R_{bs} in figure 1.8) as these increases. This may forward bias the base-emitter coupling of the BJT's even more, resulting in a higher transport factor (α) and an increased latch-up current (see 1.12.

Possible future modifications

The same modifications should be done for this device as was explained under the epitaxial device. In addition to prevent latch-up from spreading, the structures should be placed even further away to minimize the interactions between them.

5.4 Column D, N-well and diffusion size - SEL dependent on diffusion size

In column D (see figure 2.2) the goal was to explore the effect of different N-well sizes, source/drain diffusion sizes and contact placement on a large source/drain area.

In the epitaxial device no SEL could be triggered in any of the structures, and in the bulk device no SEL could be triggered in the first 8 structures with different N-well sizes. In the bulk device, structure D8 (see Appendix A figure A.55) seemed to be triggered into latch-up, but the output of this structure did not malfunction. Though, the outputs of D9-D13 did malfunctioned, and it is therefore reason to believe that these were triggered by the high energy deposited by the laser beam at structure D8.

Structure D9-D11

Structure D9-D11 (see Appendix A figure A.56-2.26) explores different source/drain sizes and measures SEL threshold energy levels about 25% lower than the reference structure A1, even though the anode-cathode distance is increased with 80%. This decrease in SEL threshold may be a result of the decreasing emitter resistances R_{ew} and R_{eb} (see figure 1.8) in accordance to Eq. 5.3 and 5.4.

Because the source area increases toward the N-well/P-substrate contacts, this will affect the SEL threshold and the effect of increased source/drain area is hard to filter out. In order to minimize the effect of decreasing contact-source distance as the source/drain area increases, the area should be increased at a 90° orientation of the contact direction, not

towards it. When increasing the source/drain area, the emitter resistance decreases as the shunt resistance decreases and in Eq. 5.3 and 5.4 you can see that these two resistances counteracts eachother. This means that the increase of the source/drain areas may have a greater impact on SEL threshold than measured on these structures.

The SEL current of these structures are hard to measure because structure D9-D13 trigger each other when they are exposed to the laser beam. This means that the SEL current measured is the total SEL current of these 5 structures. But if we split the average current measured on the 5 structures we get an average SEL current of 271mA/5 = 54.2mA through these structures. The increase in SEL current of 23% in comparison to A1 may be a result of the decreasing emitter resistances in accordance to Eq. 5.8.

Structure D12-D14

Structure D12-D14 (see Appendix A figure A.59-A.61) explores different contact placement on large source/drain areas, and measures SEL threshold energy levels about 320% higher than the reference structure A1. Structure D14 did not experience latch-up and it can be assumed, as in section 5.1 and 5.2, that the SEL threshold may be too high in order to trigger latch-up with the actual laser module. The higher thresholds may be a result of the increased anode-cathode distance and the fact that the diffusion resistance is a 100 times lower than the N-well resistance, reducing the shunt resistance R_{bw}.

The SEL current of these structures are hard to measure because structure D9-D12 trigger each other when they are exposed to the laser beam. This means that the SEL current measured is the total SEL current of these 4 structures. But if we split the average current measured on the 4 structures we get an average SEL current of 271mA/4 = 68mA on these structures. This means that D12 may have a SEL current of about 68mA, while D13 is measured to an average of 61mA, 54% and 39% higher than the reference structure A1 respectively. The increase in SEL current in comparison to A1 may be a result of the decreasing emitter resistances in accordance to Eq. 5.8.

Structure D15 and D16

Structure D15 and D16 (see Appendix A figure A.62 and A.63) is a NAND and a NOR gate respectively and explores the difference in SEL susceptibility between them.

Structure D15 measures an average threshold 21% higher than D16 and a SEL current 33% higher than D16. The reason for this may be the the different connection of the source for the two structures. When the source of both PMOS transistors in the NAND (structure D15) gate are connected to DVDD (see figure 2.2), a lower emitter resistance is achieved in addition to a higher β because of the increased BJT diffusion length of the pnp BJT (see equation 5.1). Because the two sources are connected to DVDD, the

resistance between source and N-well contacts decreases, resulting in a increased SEL threshold. Because the pnp BJT has a higher gain than the npn BJT [23], reducing the shunt resistance of the pnp will have a greater effect on the SEL threshold in comparison to the npn. The NAND gate also has a lower emitter resistance compared to the NOR (structure D16) gate, resulting in a larger SEL current.

5.5 Column E, transistor width - SEL threshold proportional to transistor width

In column E (see figure 2.2) the goal was to explore the effect of increasing the MOS transistor width from the minimum width of 1μm to a width of 7μm on SEL susceptibility.

In the epitaxial device, no SEL could be triggered at any laser energy level. It is assumed that the threshold of these structures is to high to induce SEL with the actual laser module.

Structure E9-E16 (see Appendix A figure A.72-A.79) in the bulk device could not be triggered into latch-up. It is assumed that the threshold of these structures is too high to induce SEL with the actual laser module.

Structure E1-E8

Structure E1-E8 (see Appendix A figure A.64-A.71) in the bulk device were triggered into latch-up and gave satisfying results. As the nMOS/pMOS width was increased from 1.5μm/4.5μm (structure E1) to 7.0μm/21.0μm (structure E8), the SEL threshold increased about 20% and the SEL current increased about 180%. The SEL threshold of E1 was about 17% higher and the SEL current about 10% lower than the reference structure A1. The SEL threshold of E8 was about 35% higher and the SEL current about 155% higher than the reference structure A1.

The increased SEL threshold can be a result of the increasing contact and source area as the nMOS and pMOS transistors increase in width. As the contact and source area increases, the resistance between the terminals decreases (reducing R_{ew} and R_{eb} in figure 1.8), resulting in a increased SEL threshold (see Eq. 5.3 and 5.4).

When the BJT diffusion length increases as a function of the nMOS and pMOS transistor width, the β of the parasitic pnp and npn increases as shown in Eq. 1.13. The increased β and the decreased parasitic resistances (R_{ew} and R_{eb}) increases the SEL current as can be described by Eq. 5.8.

As can be seen in figure 4.2, the measured SEL threshold does not follow the expected trigger current curve of Eq. 5.3, but show the same tendency. The R_{ew} and R_{eb} resistances may behave differently than expected and is hard to calculate without advanced tools. The β of the BJT's may also behave differently than described in Eq. 1.13, this can contribute to the difference between the calculated and measured curve in figure 4.2.

Possible future modifications

Because structure E9-E16 was too resilient to SEL, the effect of turning the MOS transistors 90° could not be fully explored. In order to explore the effect of turning the MOS transistors 90°, the structures would have to be made more susceptible to SEL in a way that would not impact the transistor width and orientation. By placing the N-well/P-substrate contacts further away from the source, the SEL threshold would decrease, provided the same number of contacts placed at the same distance from the source on all 16 structures. By placing the contacts far enough from the source, the SEL threshold would be decreased enough to make all the structures susceptible to latch-up. In this manner, the structures could be relatively compared to each other and the effect of increased transistor width could be headed out.

Depending on the designer and available area, the number of N-well/P-substrate contacts can either increase in accordance with the transistor width or be set to a standard fixed number. In the structure E1-E16 the number of contacts increases in accordance with the transistor width resulting in a decreased contact-source resistance as the MOS transistor width increases. This design procedure is not wrong, but in this test case it does not isolate the effect of increased transistor width because both the SEL threshold and current will be affected by the increased number of contacts. In order to explore the isolated effect of increased transistor width, 8 additional structures should be made with a fixed number of contacts.

5.6 Other uncertainties

The energy setting resolution of the laser module is distributed over 240 steps. This means that if SEL is induced at an energy setting of 3.3, but not at 2.9, the actual SEL threshold could be anywhere in between 2.9 and 3.3 which gives rise to some uncertainties. If the resolution of the energy setting had been higher, a more accurate SEL threshold could be found.

Because the focus of the microscope and laserspot had to manually adjusted, some uncertainties could occur from bad focus or uncertain charge distribution into the silicon.

Latch-up susceptibility will be dependent on the laser pulse location on the test structures. To be able to compare the test structures against each other, they must be exposed to the same type of laser with the same intensity at the same location on the structure, though this can not be done with a 100% accuracy since the structures differ in both size and form. In [10] and [11] collection effeciency is affected by the collectors (source or contacts) orientation on the injection source (this may be relevant only when testing the structures with different width). The absorption factor is also changed as the doping consentration is changed, meaning that the absorption factor can be different at different locations on the semiconductor and is higher

with epitaxial layer [22].

Mismatch between the test devices as well as process variations is of concern and affect both the SEL threshold and current. An additional number of test devices should be tested in order to get more reliable results.

The two different AMS 0.35μm options C35B4C3 (bulk) and C35B4O1 (epitaxial) possess different top layers from the fabric. The C35B4O1 (epitaxial) option possess a anti reflective coating as the top layer which lets through a greater portion of the laser beam light than the C35B4C3 (bulk) option. The difference in light absorption of the two options is essential in order to compare the SEL laser energy threshold between them.

When SEL is initiated, high currents are passing through the ASIC and bonding wires. This may degrade the structures, metal wiring and bonding wires, resulting in higher resistance through them. This higher resistance may affect both the SEL threshold and current.

When latch-up was induced and a high current passing trough the structure, a certain temperature increment was expected. It was observed that under latch-up, the test device appeared out of the microscope focus because the device was twisting as a result of the temperature increment. When the device was reset and back to normal operation, the temperature decreased and the device appeared in focus again. For a period of about 5-10 seconds (depending on SEL current and the time period before the device was reset) after the device had been reset after latch-up the SEL threshold was measured about 20-30% lower that before SEL had been initiated. In the reference structure A1, the SEL energy threshold setting was initially 8.4, but after SEL had been initiated the threshold was measured as low as 6.6. According to [24], the resistance in the silicon increases as the temperature increases and at a temperature of 125° the N-well and P-substrate sheet resistance is doubled in relation to a temperature of 25°. Another effect of increasing temperature is the decrease in the the threshold voltage and the gain(β) of the BJT's. These three variables has a great effect on SEL trigger current and in some extent trigger voltage as can be seen in Eq. 1.6, 1.7 and 1.8.

Chapter 6

Conclusion

This thesis has discussed and explored several ways of hardening an ASIC design against Single Event Latch-up (SEL) in AMS 0.35μm. It is proved by empirically testing that different layout strategies in CMOS circuit design have a great effect on SEL susceptibility, though some of the structures appeared too resistant against SEL in order to be triggered. The use of a pulsed laser beam has also proved to be a helpful tool in the characterization, testing and comparing of SEL thresholds in CMOS.

In the epitaxial device, SEL threshold is clearly affected by contact-source distance. When the contact-source distance is below 4.5μm, the threshold is at a high and almost constant level, but when the distance is increased to 6.5μm the threshold drops about 70%. This means that in order to maintain a high SEL threshold, the contact-source distance should not exceed 4.5μm when using epitaxial substrate.

The bulk device shows the same tendency as the epitaxial device. When the contact-source distance is 2.0μm or less, the SEL threshold is too high to initiate latch-up with the actual laser module. When the distance is 2.5μm or more, the SEL threshold drops to a level 12% beneath the reference inverter A1. This means that in order to maintain a high SEL threshold, the contact-source distance should not exceed 2.0μm when using a bulk substrate.

If the drop in SEL threshold is distributed over the distance between 4.5μm and 6.5μm in the epitaxial device or between 2.0μm and 2.5μm in the bulk device can not be determined by these measurements. Structures with a higher resolution of contact-source distances have to be made in order to characterize this ”threshold“ drop more accurate.

Increasing source and drain diffusion sizes presents a SEL threshold 25% lower than the reference structure A1, even though the anode-cathode distance is increased, which should contribute to a increased SEL threshold. Based on this observation, large source and drain areas affect SEL threshold negatively.

Different contact placement on large source and drain diffusion areas show some effect. The SEL threshold increased about 5% when the contacts were moved from the edge beside the MOSFET gate (structure D12) to the middle of the diffusion area (structure D13). SEL could not be initiated

when the contacts were moved to the other side of the diffusion (structure D14), near the N-well/P-substrate contacts. The threshold of structure D12 and D13 is 310% and 330% higher in comparison to the reference structure A1 respectively. But it is hard to determine if the positive effect on SEL threshold in comparison to A1 is because of the contact placement or the increased anode-cathode spacing.

As the nMOS/pMOS width was increased from 1.5μm/4.5μm to 7.0μm/21.0μm, the SEL threshold increased about 20% and the SEL current increased about 180%. The SEL threshold of these structures were between 17% and 35% higher and the SEL current were 10% lower and up to 155% higher than than the reference structure A1 respectively. These observations present that increasing the width of the MOSFET in an inverter increase the SEL threshold as well as the SEL current.

Based on the measurements performed in this thesis, structure C4 (see figure A.35) is presented as the most effective way to implement an inverter in an epitaxial technology. Structure C4 has the lowest area usage (about 30% less than A1) of all the structures and possess the highest SEL threshold of the structures able to experience latch-up. 2.5% higher than second place and 87% higher than the structure with the lowest threshold.

In the bulk device, structure C1 is presented as the least susceptible structure against SEL of the structures able to experience latch-up. Structure C1 with a 17% decreased area, a 465% higher SEL threshold and a 30% higher SEL current in comparison to the reference structure A1.

The structures not able to experience SEL can be assumed to have a SEL threshold too high to be triggered by the actual laser module used in these measurements. This means that these structures can withstand more laser energy than the other structures before SEL is initiated. But because SEL is not initiated, the most effective structure can not be withdrawn from these tests.

However, theory [12] presents N+ majority guard rings (see figure A.17) as the least susceptible structure against SEL.

6.1 Further work

In order to characterize and learn more about SEL occurrence in the AMS 0.35μm technology, further work have to be done. Below are listed some pointers on how to continue this work further in order to gain more useful results:

- Investigate increment of R_{bw} and R_{bs} separately in addition to a higher resolution on the different contact-source spacings.
- Investigate the effect of several pMOS in the same N-well in contrast to several pMOS in separate N-wells.
- Investigate further the possibility of converting deposited laser energy to deposited radiation energy in silicon.
- Measure the laser energy out of the microscope in order to obtain accurate

energy levels.
- Investigate the difference in laser light absorption of the bulk and epitaxial option.
- Do measurements where the structures are exposed to the laser beam at different locations in order to localize the most sensitive areas of the structures.
- Find a way to measure the holding voltage of the different structures, and then measure them.
- Find or develop models for 3 dimensional calculation of the parasitic components present in the CMOS technology.

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Appendix A

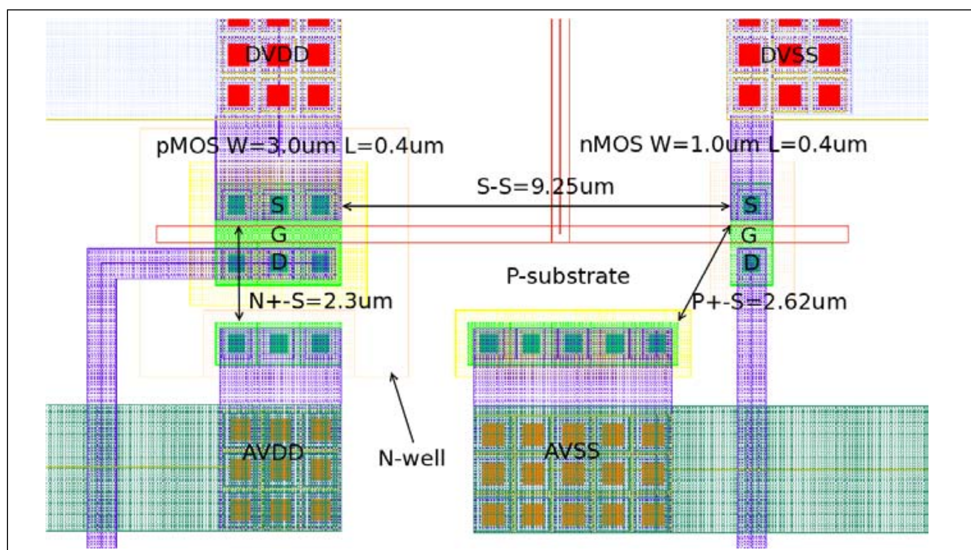

Figure A.1: Structure A1 - GMI's standard inverter.

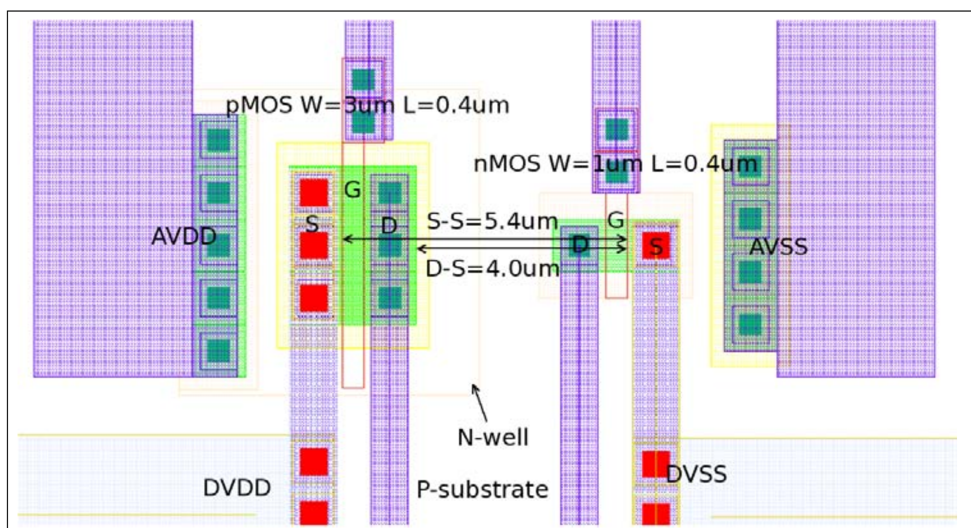

Figure A.2: Structure A2 - Inverter with nMOS-pMOS spacing of 5.4μm.

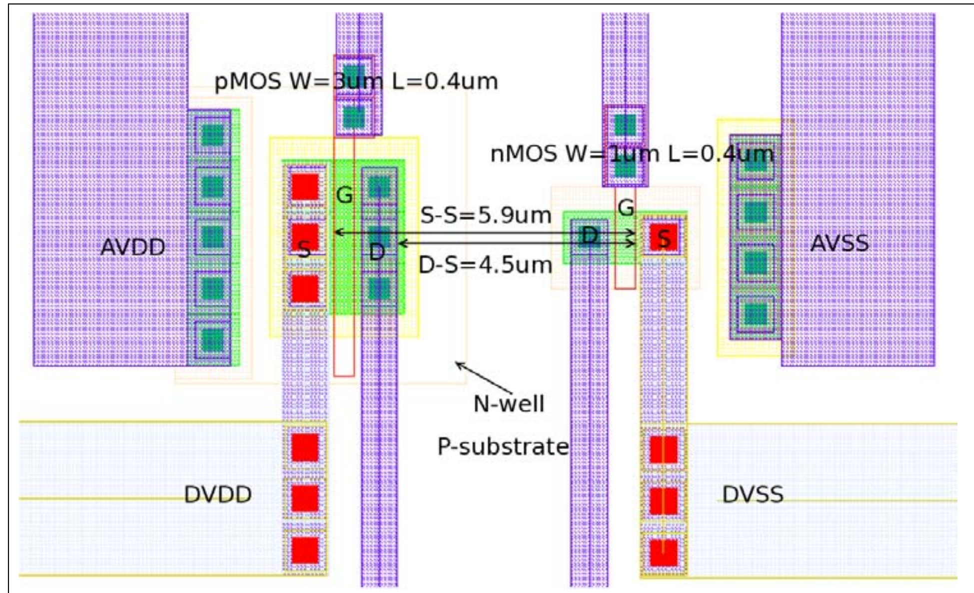

Figure A.3: Structure A3 - Inverter with nMOS-pMOS spacing of 5.9μm.

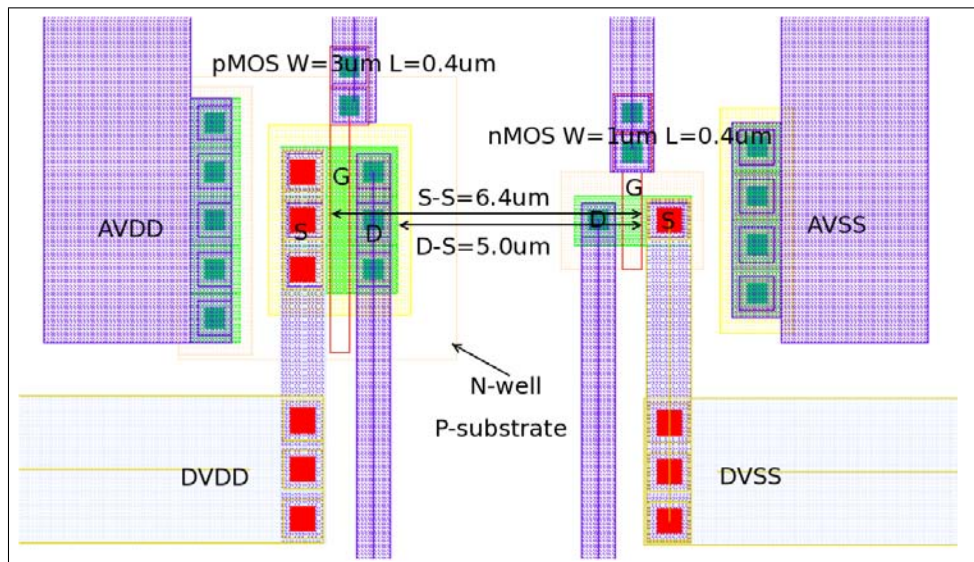

Figure A.4: Structure A4 - Inverter with nMOS-pMOS spacing of 6.4μm.

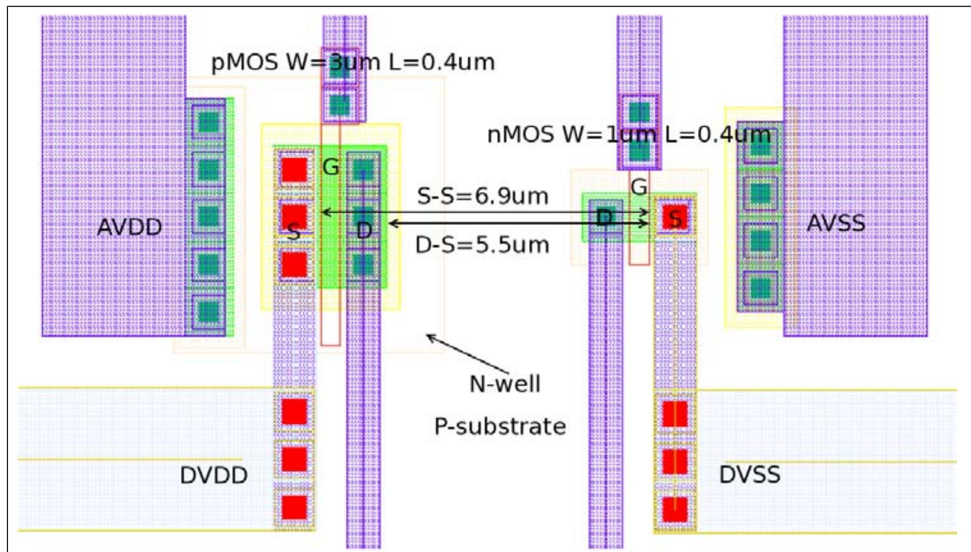

Figure A.5: Structure A5 - Inverter with nMOS-pMOS spacing of 6.9μm.

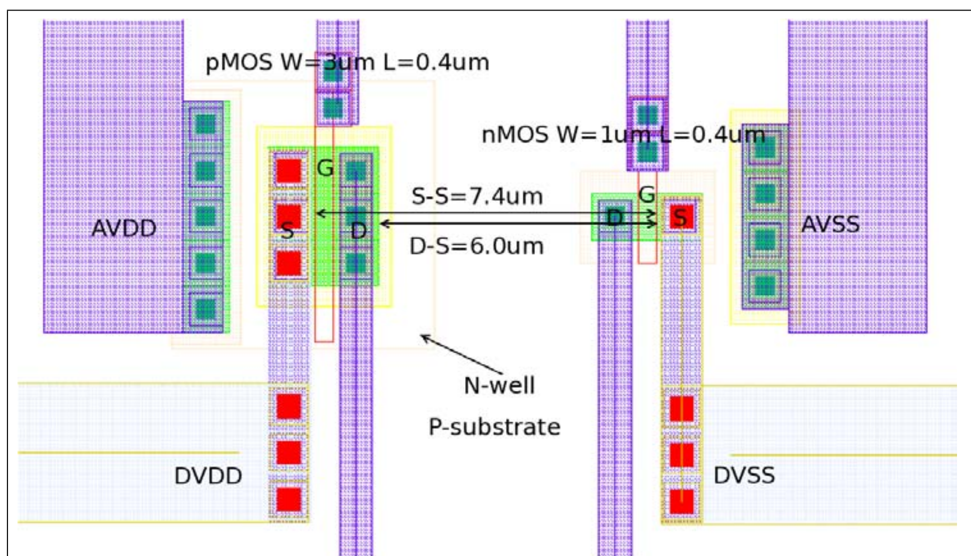

Figure A.6: Structure A6 - Inverter with nMOS-pMOS spacing of 7.4μm.

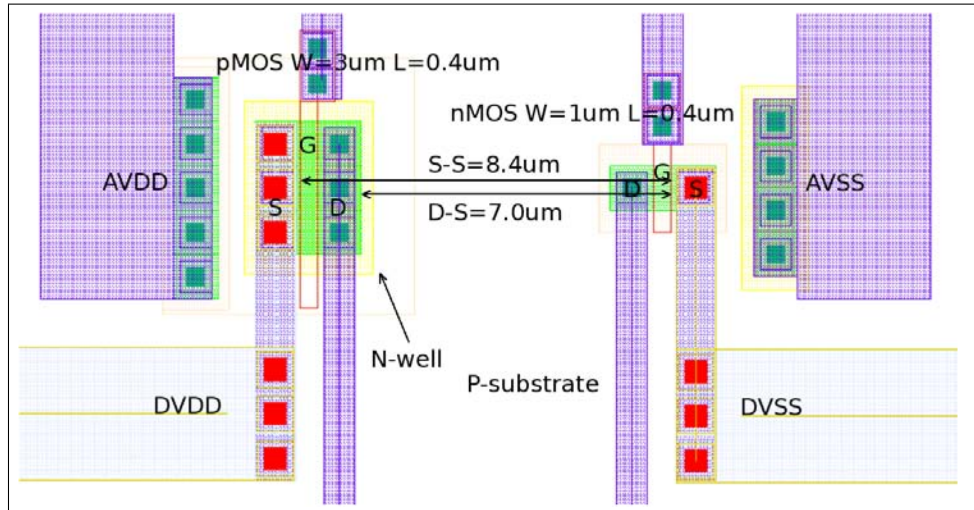

Figure A.7: Structure A7 - Inverter with nMOS-pMOS spacing of 8.4μm.

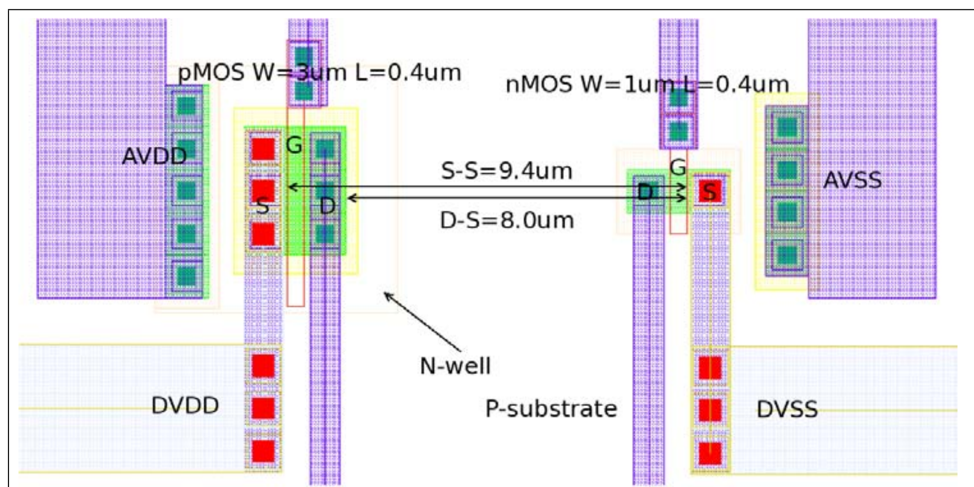

Figure A.8: Structure A8 - Inverter with nMOS-pMOS spacing of 9.4μm.

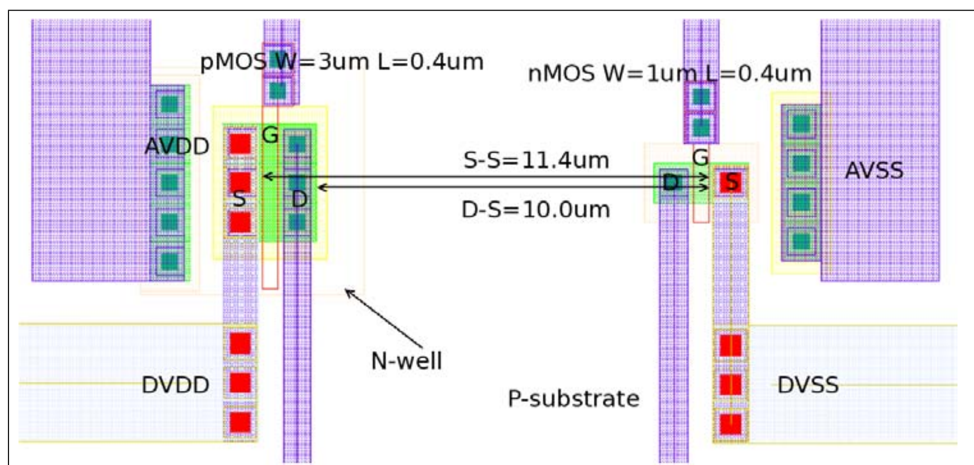

Figure A.9: Structure A9 - Inverter with nMOS-pMOS spacing of 11.4μm.

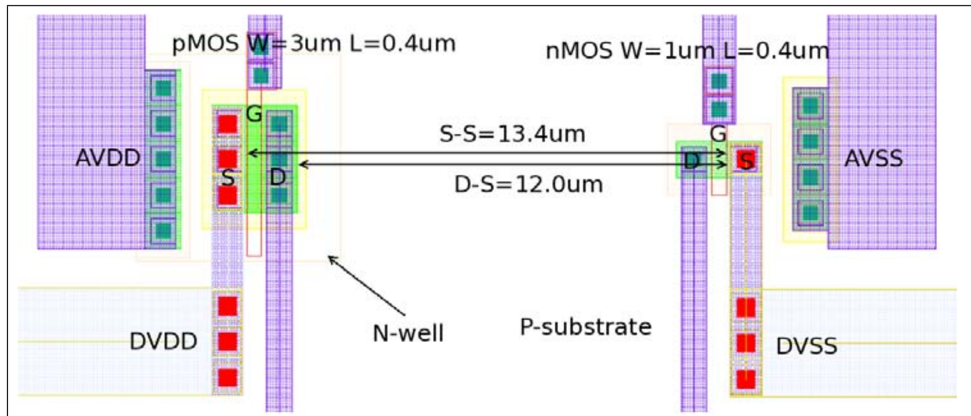

Figure A.10: Structure A10 - Inverter with nMOS-pMOS spacing of 13.4μm.

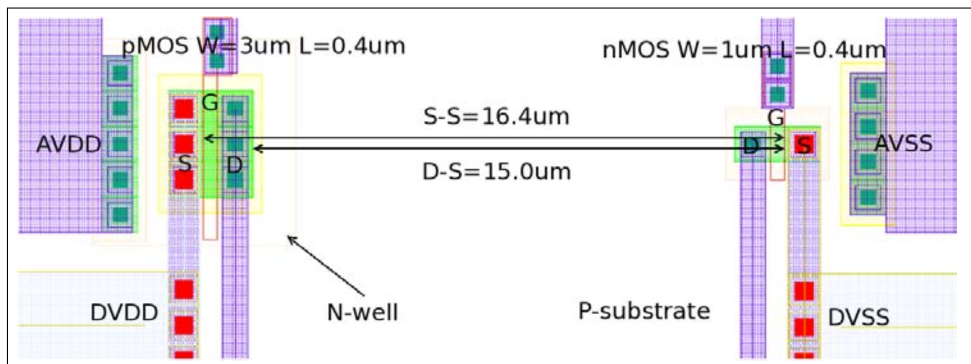

Figure A.11: Structure A11 - Inverter with nMOS-pMOS spacing of 16.4μm.

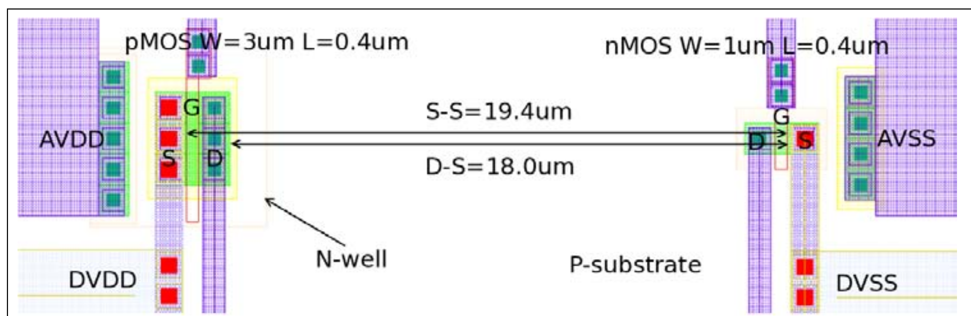

Figure A.12: Structure A12 - Inverter with nMOS-pMOS spacing of 19.4μm.

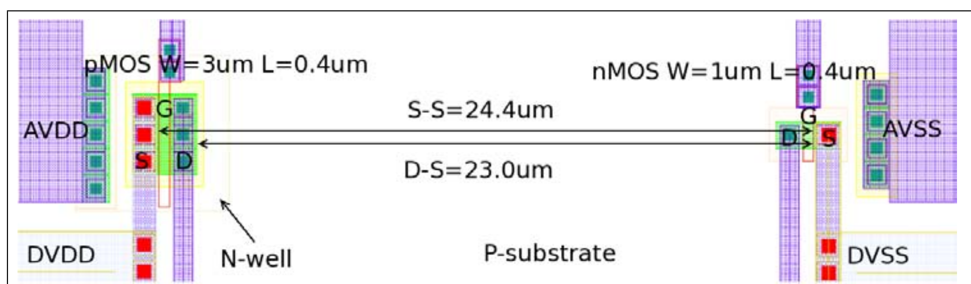

Figure A.13: Structure A13 - Inverter with nMOS-pMOS spacing of 24.4μm.

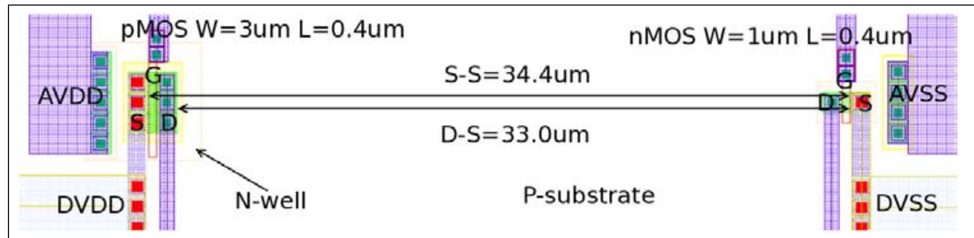

Figure A.14: Structure A14 - Inverter with nMOS-pMOS spacing of 34.4μm.

Figure A.15: Structure A15 - Inverter with nMOS-pMOS spacing of 49.4μm.

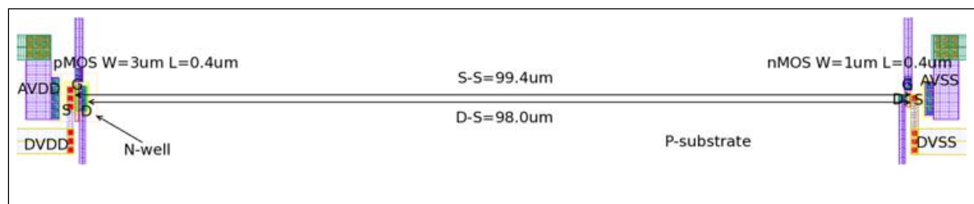

Figure A.16: Structure A16 - Inverter with nMOS-pMOS spacing of 99.4μm.

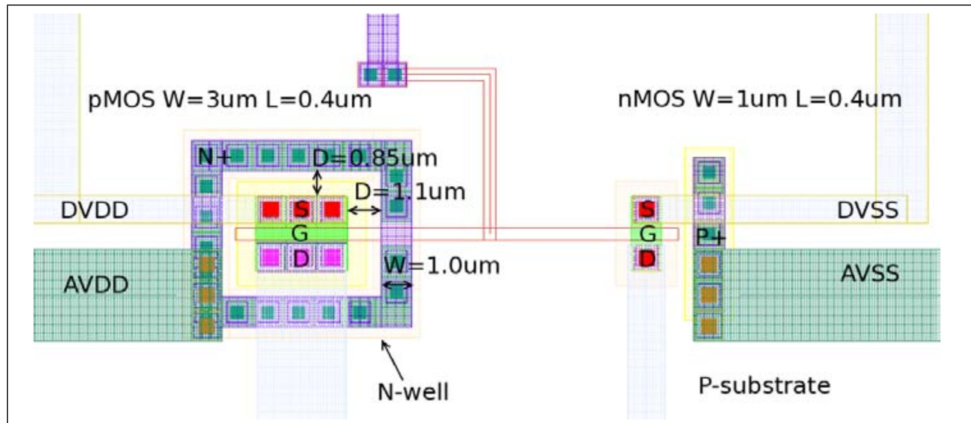

Figure A.17: Structure B1 - Majority N+ guard ring with a width of 1μm.

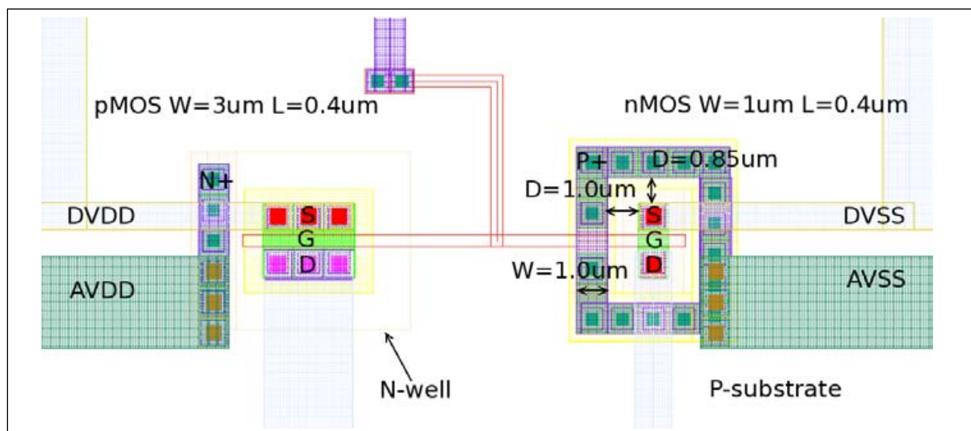

Figure A.18: Structure B2 - Majority P+ guard ring with a width of 1μm.

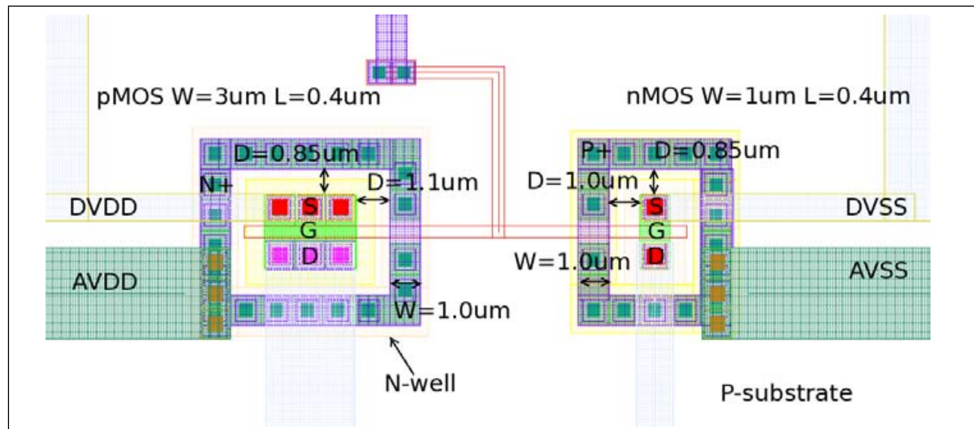

Figure A.19: Structure B3 - Both majority N+ and P+ guard ring with a width of 1μm.

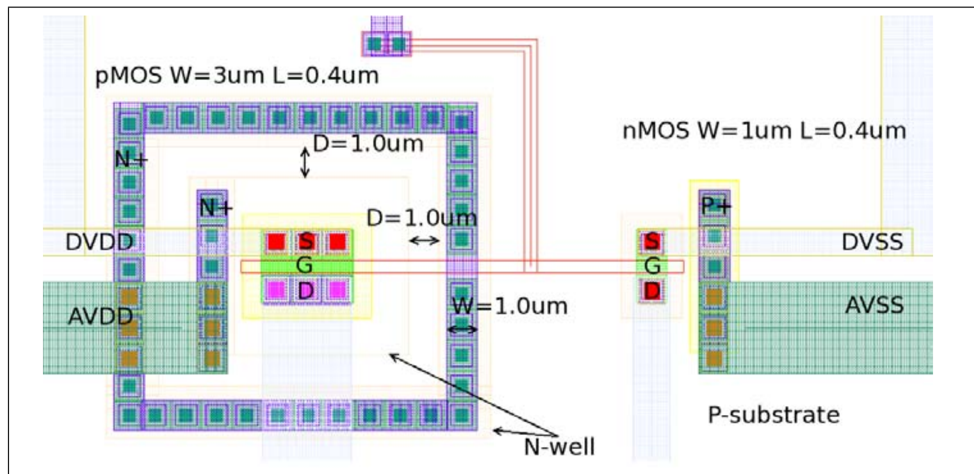

Figure A.20: Structure B4 - Minority N+ guard ring with a width of 1μm.

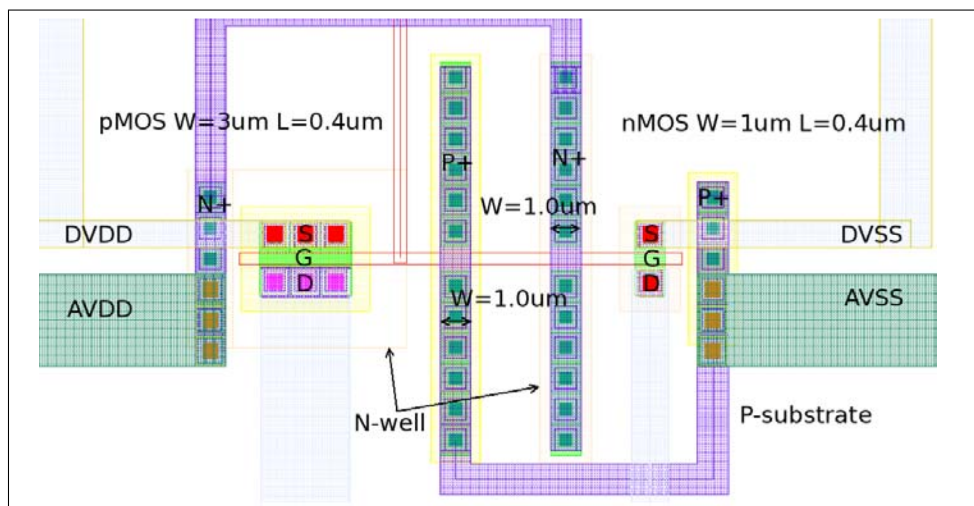

Figure A.21: Structure B5 - Minority N+ and P+ guard strips with a width of 1μm.

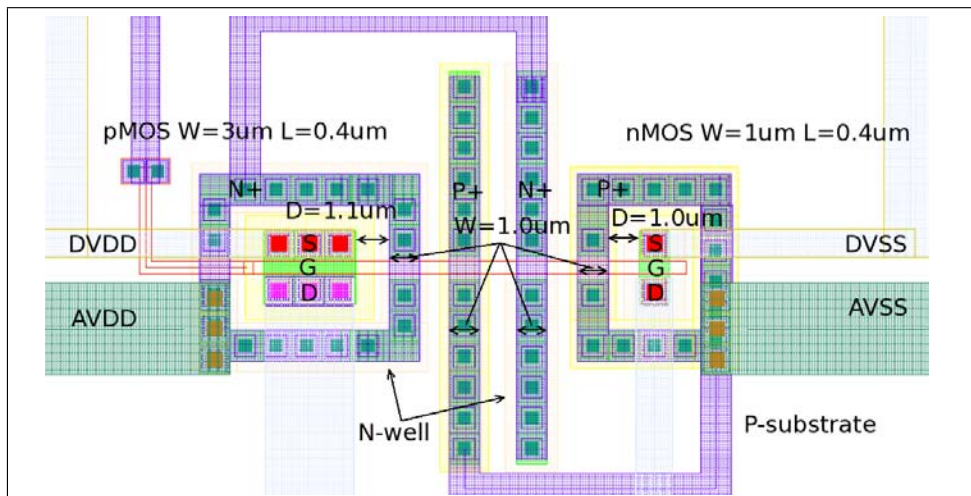

Figure A.22: Structure B6 - Both N+ and P+ majority and N+ and P+ minority guard strips with a width of 1μm.

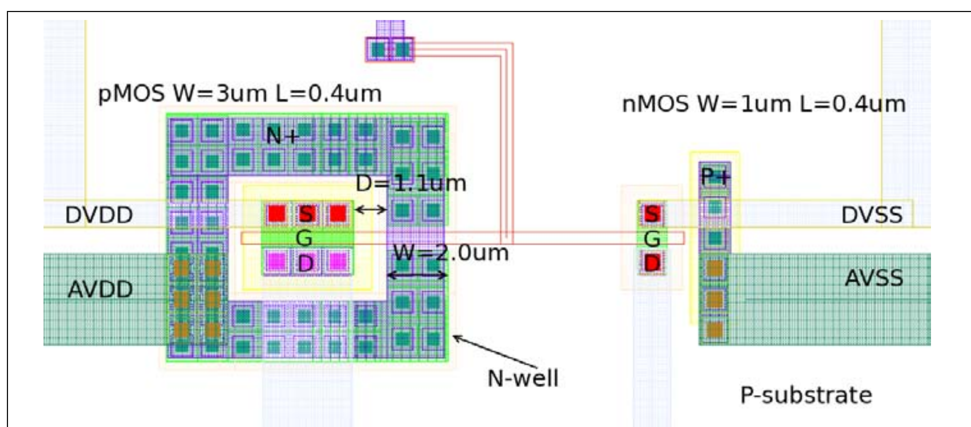

Figure A.23: Structure B7 - Majority N+ guard ring with a width of 2μm.

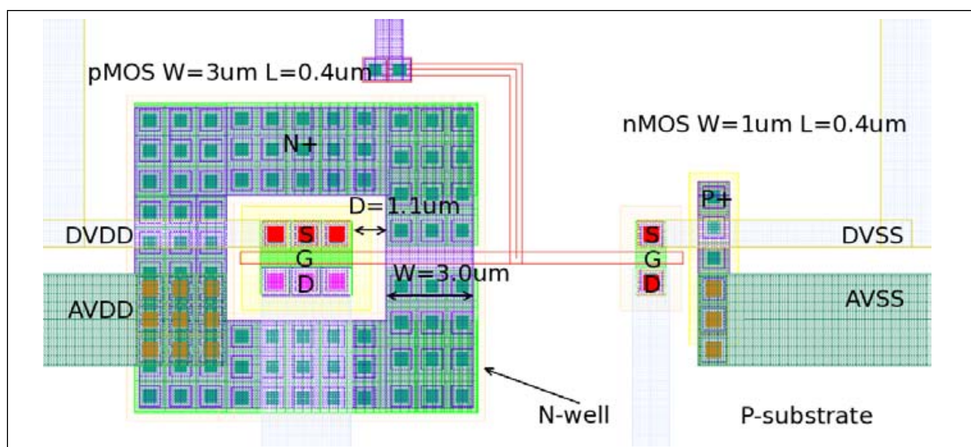

Figure A.24: Structure B8 - Majority N+ guard ring with a width of 3μm.

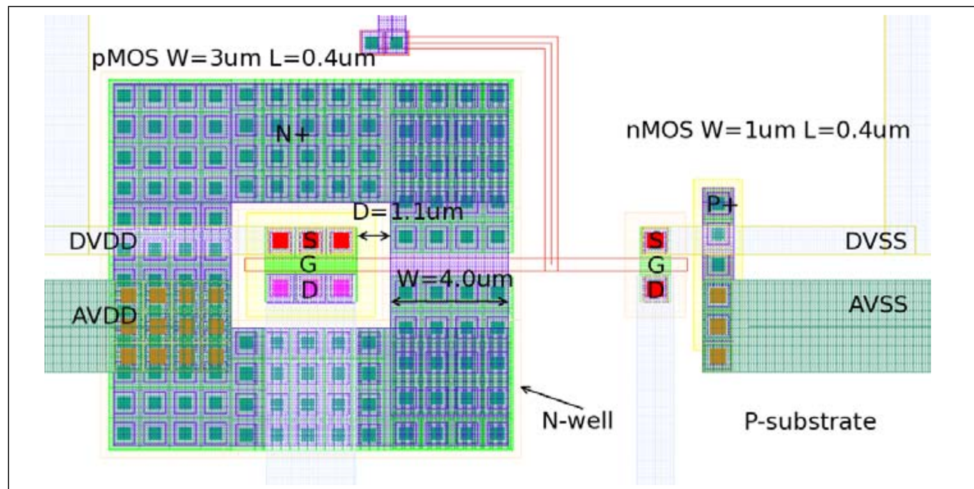

Figure A.25: Structure B9 - Majority N+ guard ring with a width of 4μm.

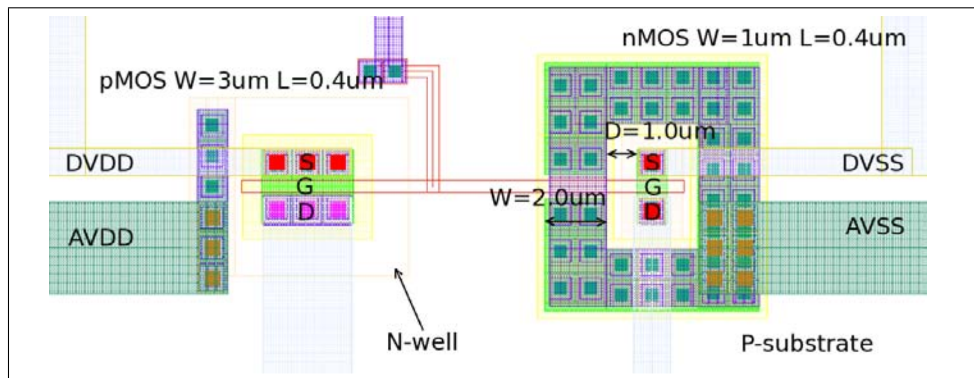

Figure A.26: Structure B10 - Majority P+ guard ring with a width of 2μm.

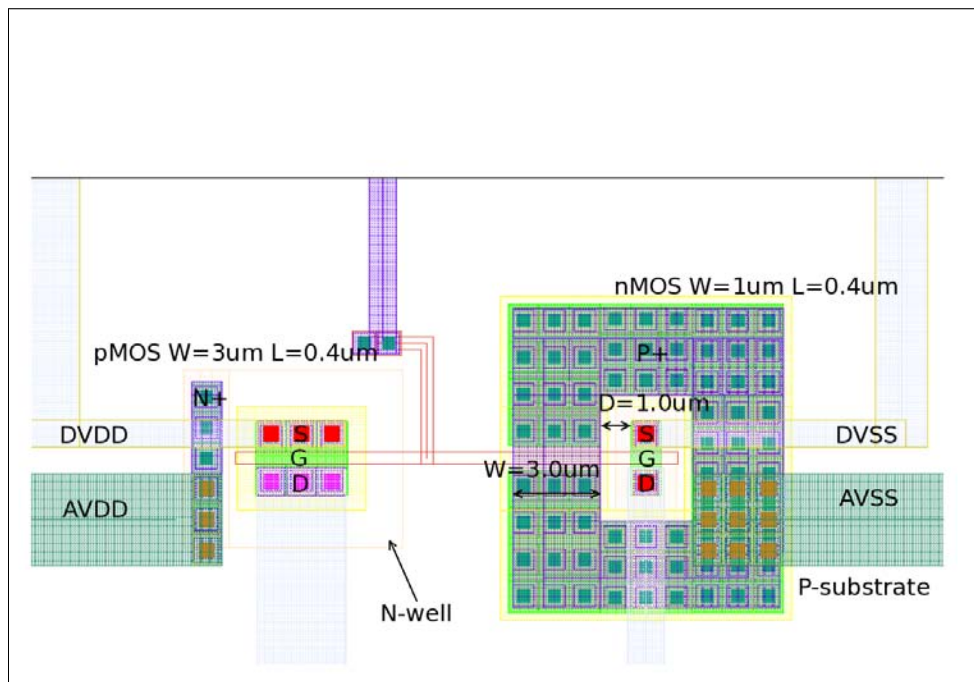

Figure A.27: Structure B11 - Majority P+ guard ring with a width of 3μm.

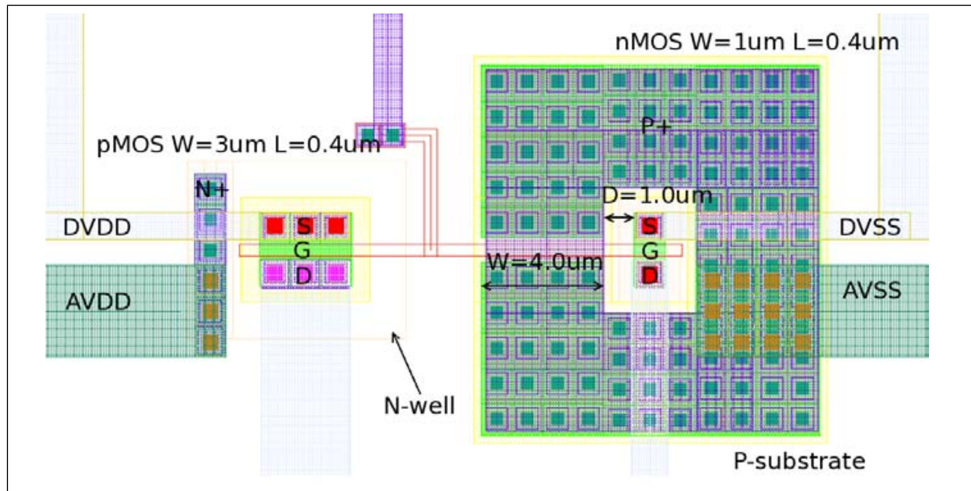

Figure A.28: Structure B12 - Majority P+ guard ring with a width of 4μm.

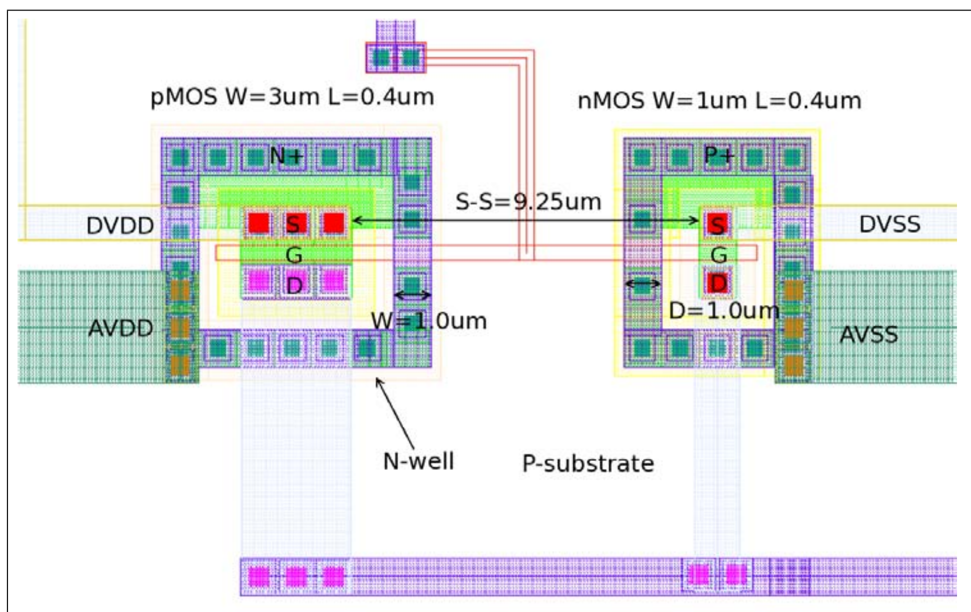

Figure A.29: Structure B13 - Inverter with N+ and P+ majority guard ring with a width of 1μm.

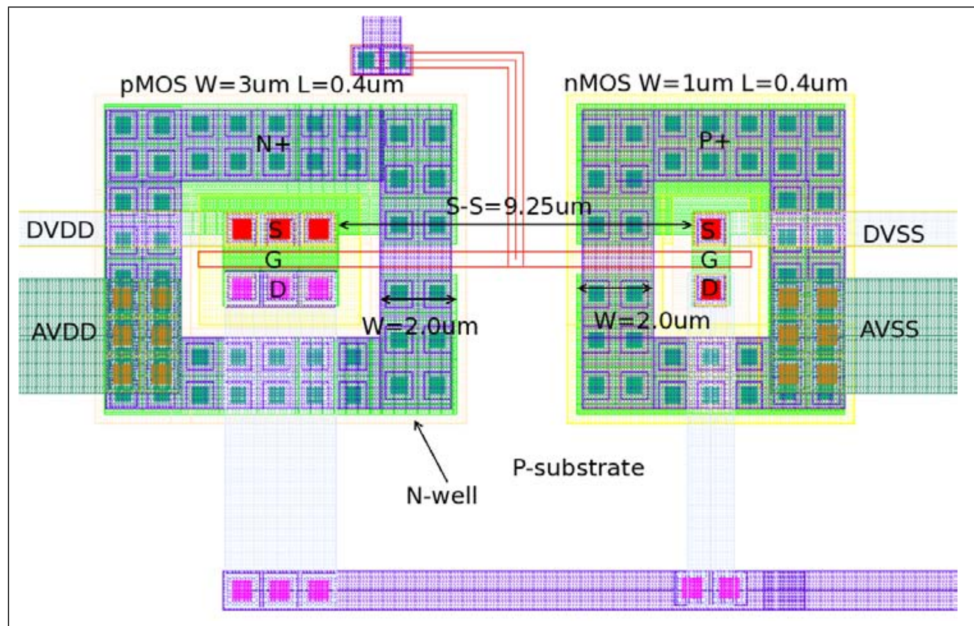

Figure A.30: Structure B14 - Inverter with N+ and P+ majority guard ring with a width of 2μm.

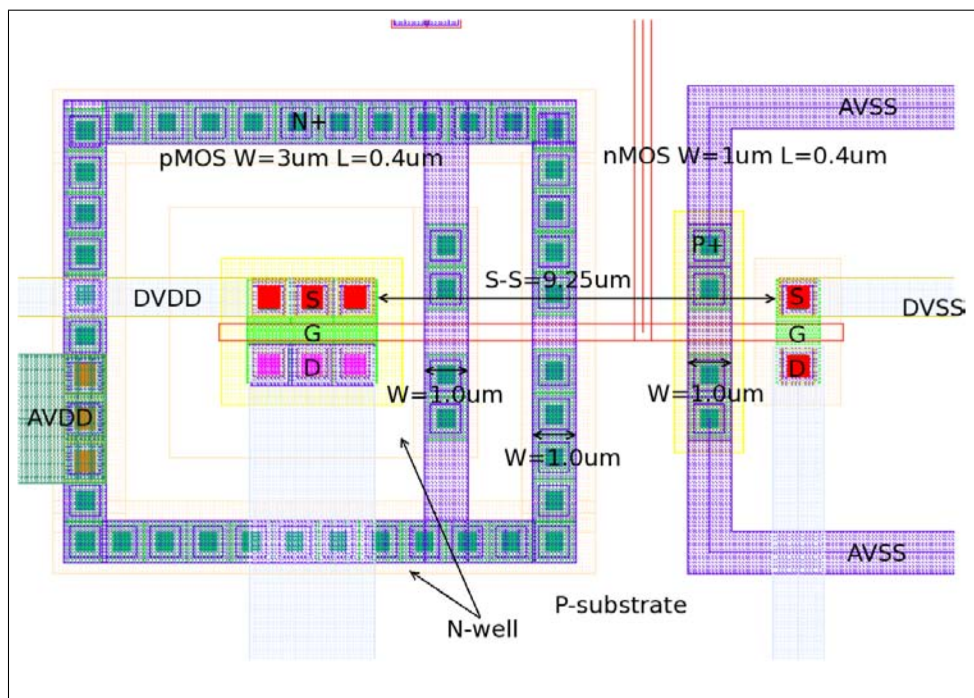

Figure A.31: Structure B15 - Inverter were the N+ and P+ contacts are placed in between the transistors and a minority N+ guard ring around the nMOS.

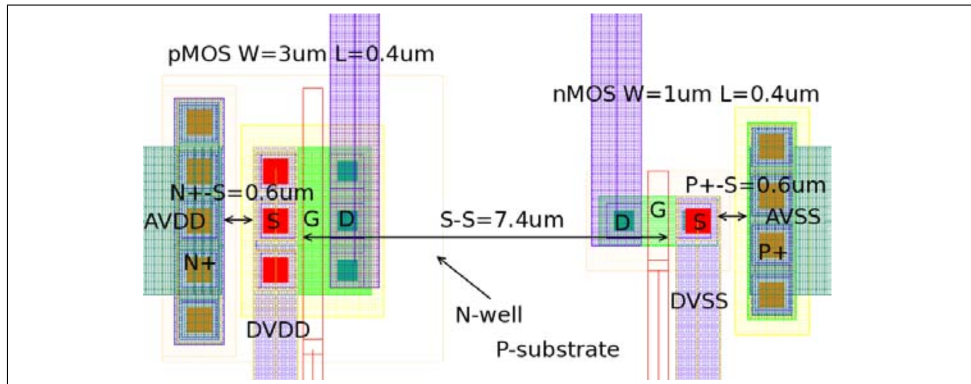

Figure A.32: Structure C1 - A standard inverter with source-source distance of 7.4μm and contact-source distance of 0.6μm.

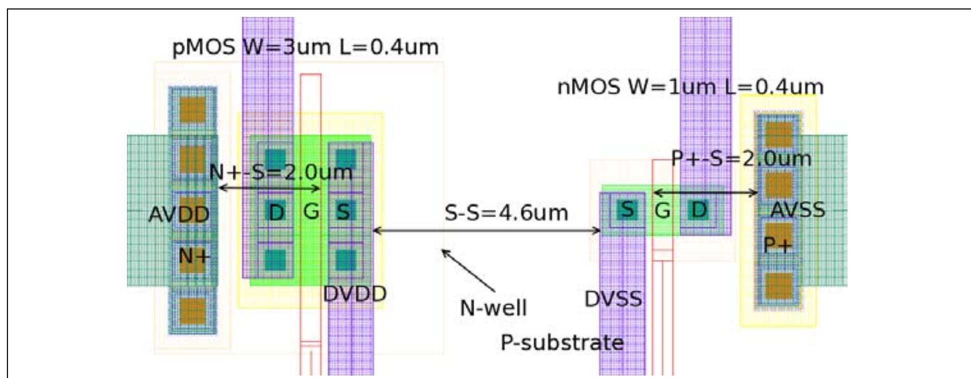

Figure A.33: Structure C2 - An inverter with source and drain on the opposite side of the gate compared to the standard inverter in A.32, resulting in a source-source distance of 4.6μm.

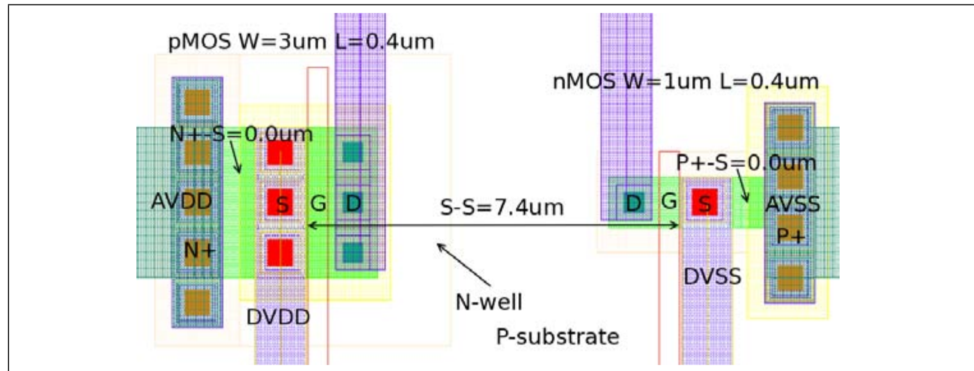

Figure A.34: Structure C3 - An inverter were the N-well/P-substrate contact and source are butted, resulting in a contact to source distance of 0.0μm.

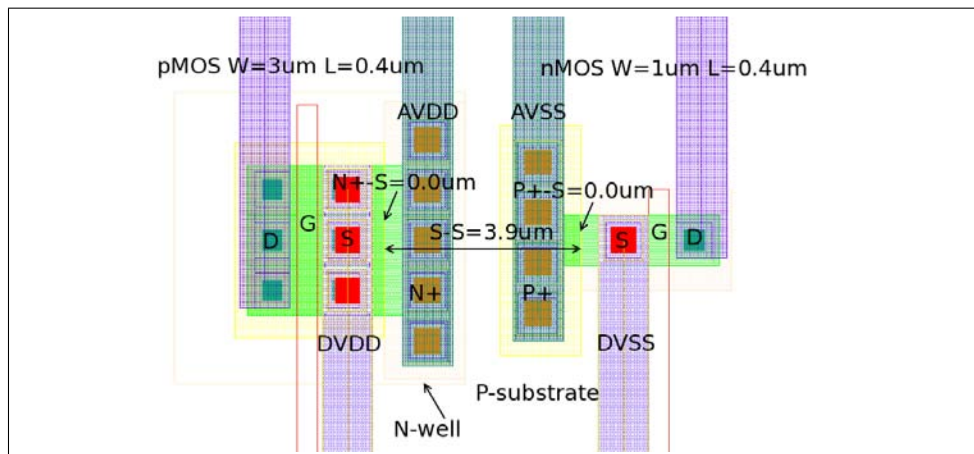

Figure A.35: Structure C4 - An inverter with source and drain on the opposite side of the gate compared to the standard inverter in figure A.32, N-well/P-substrate contacts and source are butted and are placed in between the transistors. This results in a source- source distance of 3.9μm and a contact-source distance of 3.9μm.

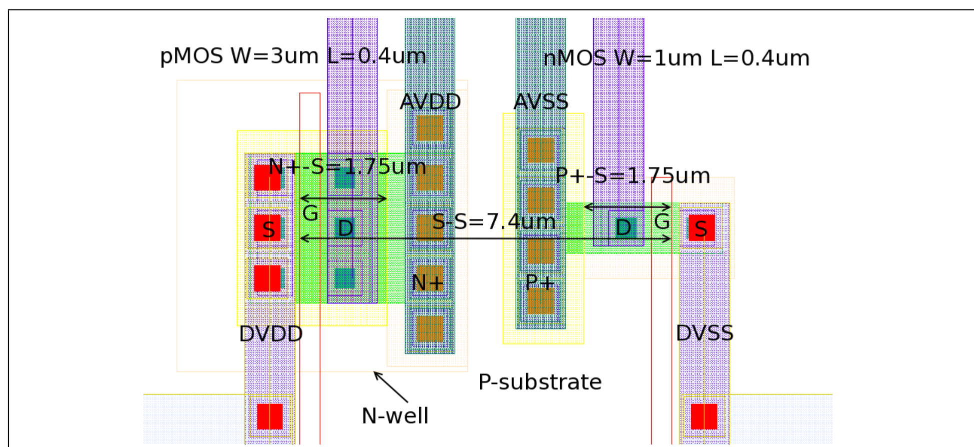

Figure A.36: Structure C5 - An inverter were the N-well/P-substrate contacts are placed in between the transistors and at the same time butted with the drain. This results in a contact-source distance of 1.75μm.

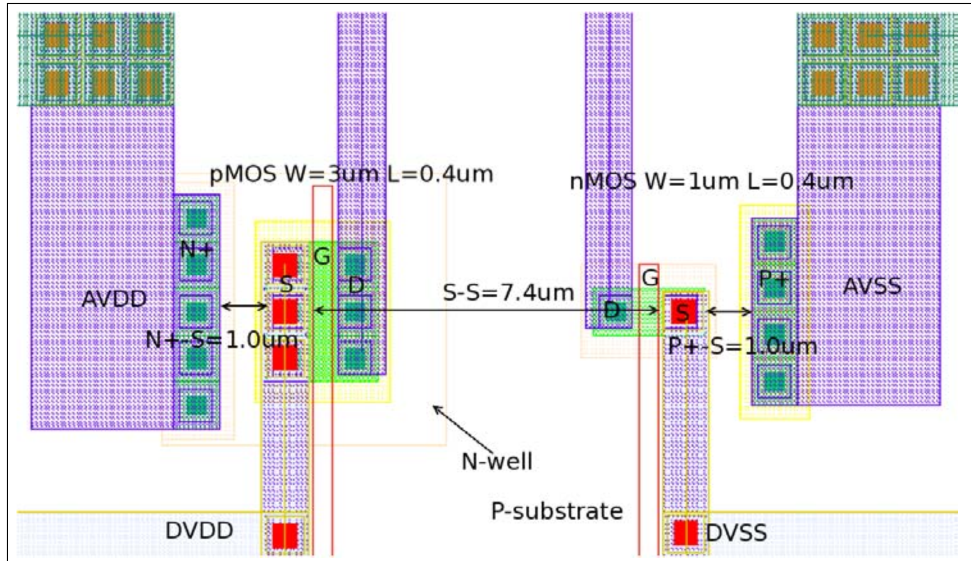

Figure A.37: Structure C6 - A standard inverter with N-well/P-substrate contact to source distance of 1.0μm.

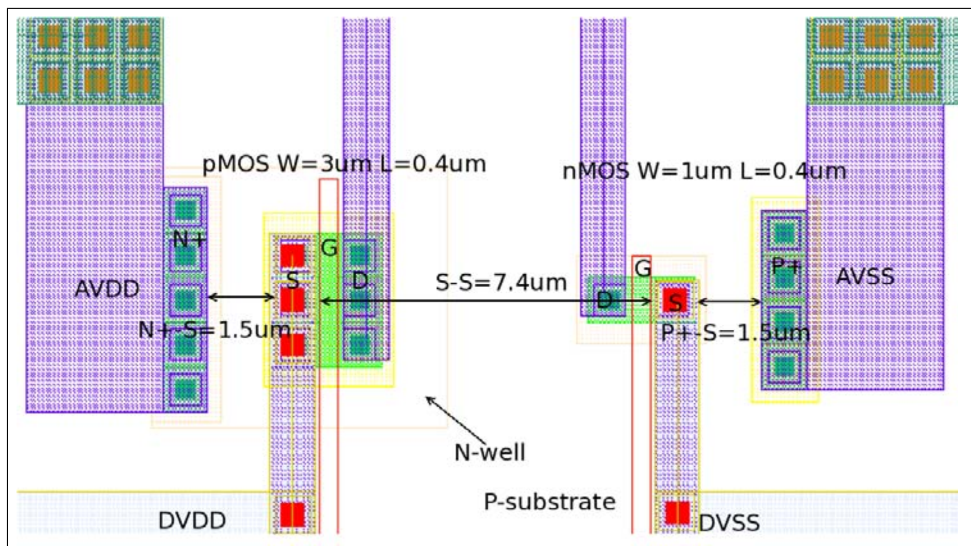

Figure A.38: Structure C7 - A standard inverter with N-well/P-substrate contact to source distance of 1.5μm.

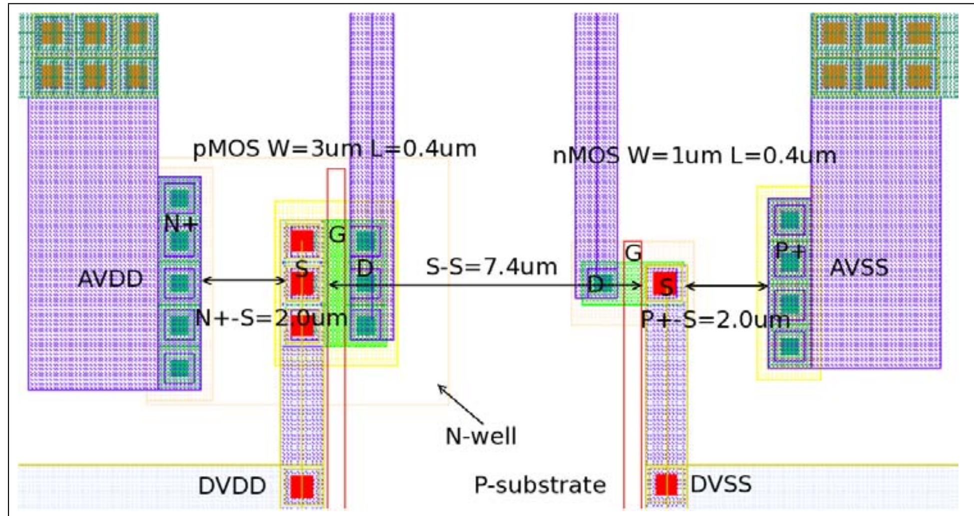

Figure A.39: Structure C8 - A standard inverter with N-well/P-substrate contact to source distance of 2.0μm.

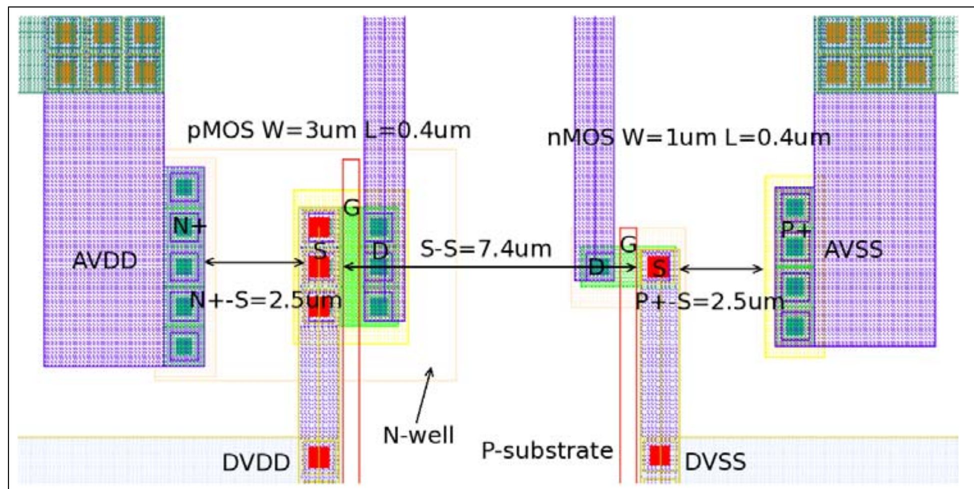

Figure A.40: Structure C9 - A standard inverter with N-well/P-substrate contact to source distance of 2.5μm.

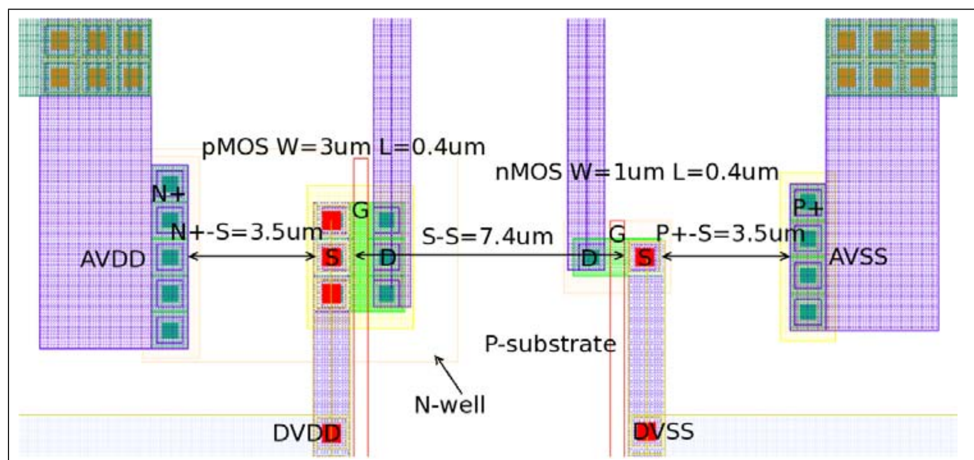

Figure A.41: Structure C10 - A standard inverter with N-well/P-substrate contact to source distance of 3.5μm.

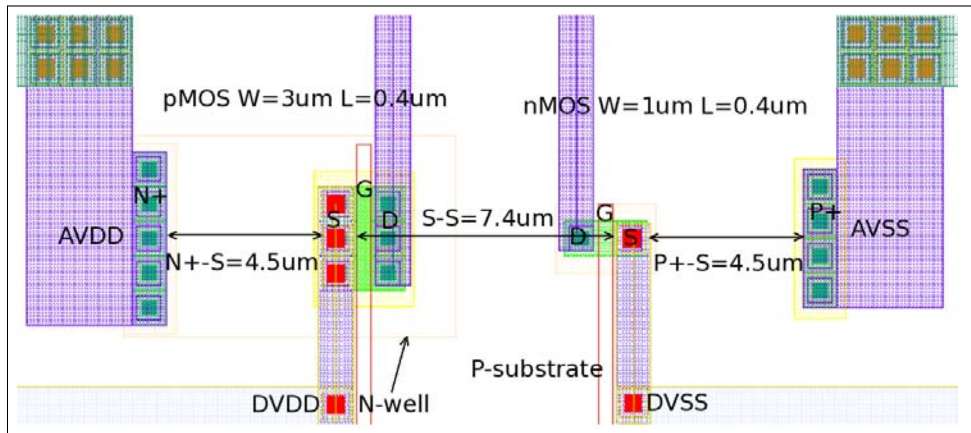

Figure A.42: Structure C11 - A standard inverter with N-well/P-substrate contact to source distance of 4.5μm.

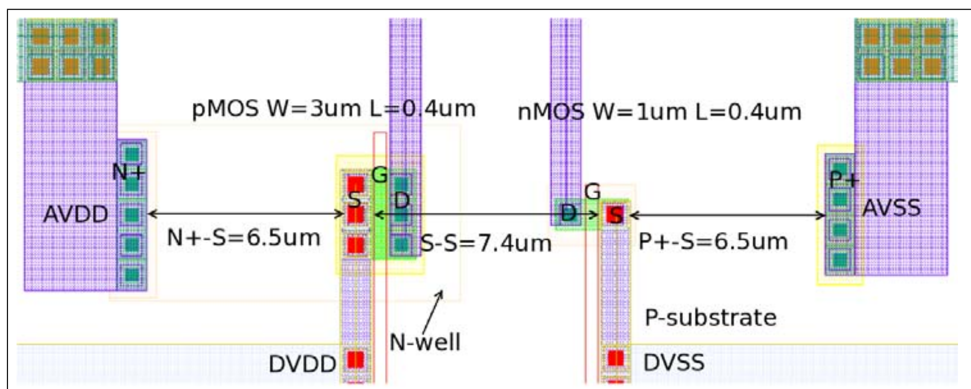

Figure A.43: Structure C12 - A standard inverter with N-well/P-substrate contact to source distance of 6.5μm.

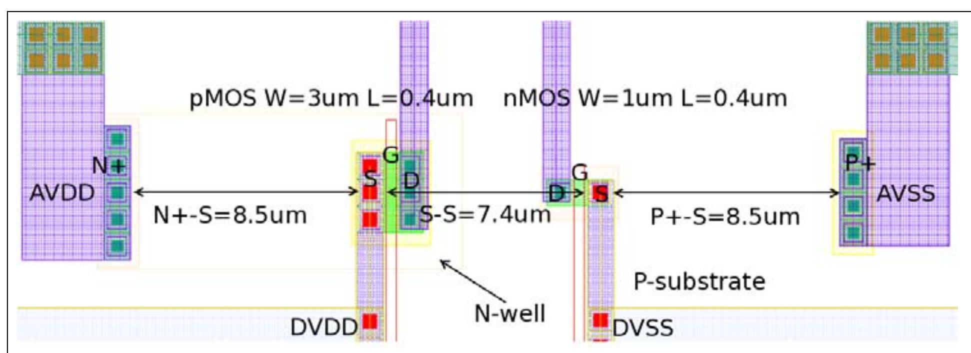

Figure A.44: Structure C13 - A standard inverter with N-well/P-substrate contact to source distance of 8.5μm.

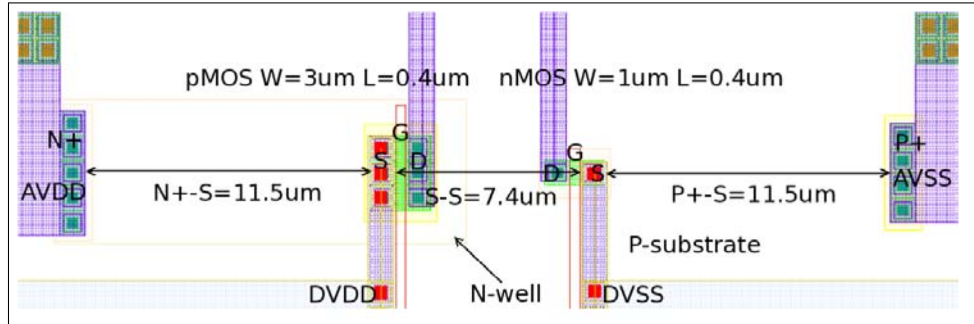

Figure A.45: Structure C14 - A standard inverter with N-well/P-substrate contact to source distance of 11.5μm.

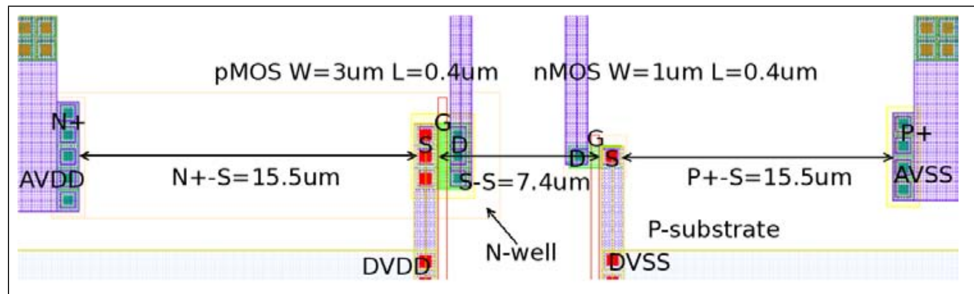

Figure A.46: Structure C15 - A standard inverter with N-well/P-substrate contact to source distance of 15.5μm.

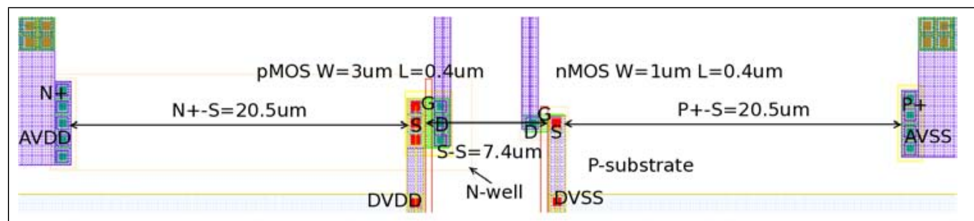

Figure A.47: Structure C16 - A standard inverter with N-well/P-substrate contact to source distance of 20.5μm.

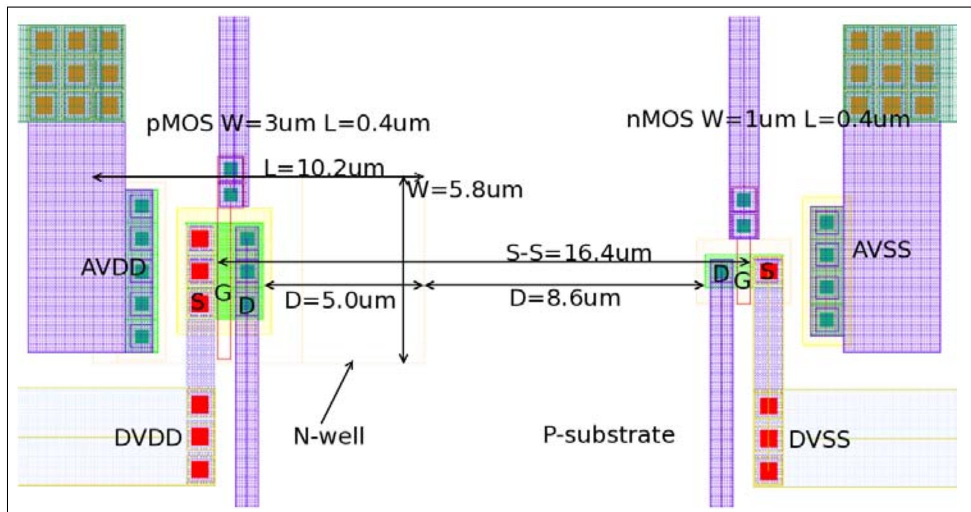

Figure A.48: Structure D1 - An inverter with the N-well increased in size along the X-axis towards the nMOS transistor. The new size is a length of 10.2μm and a width of 5.8μm.

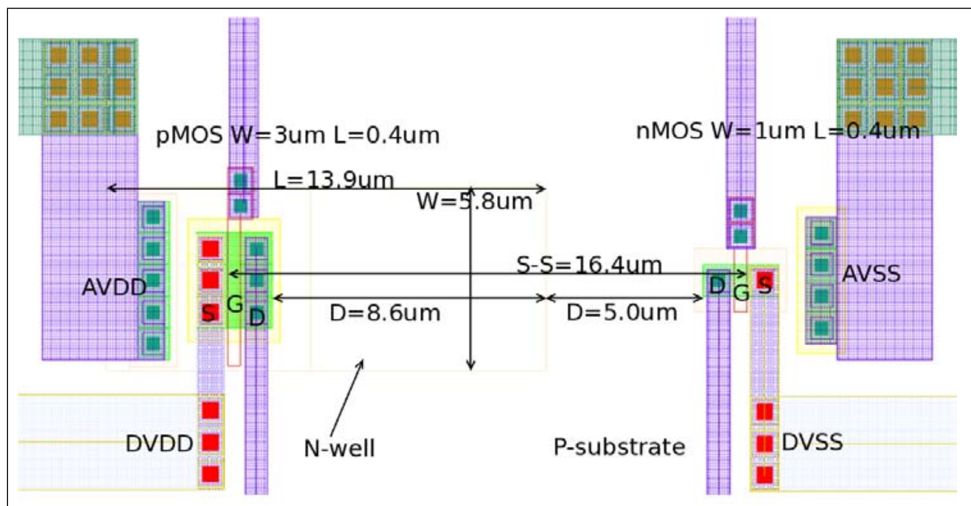

Figure A.49: Structure D2 - An inverter with the N-well increased in size along the X-axis towards the nMOS transistor. The new size is a length of 13.9μm and a width of 5.8μm.

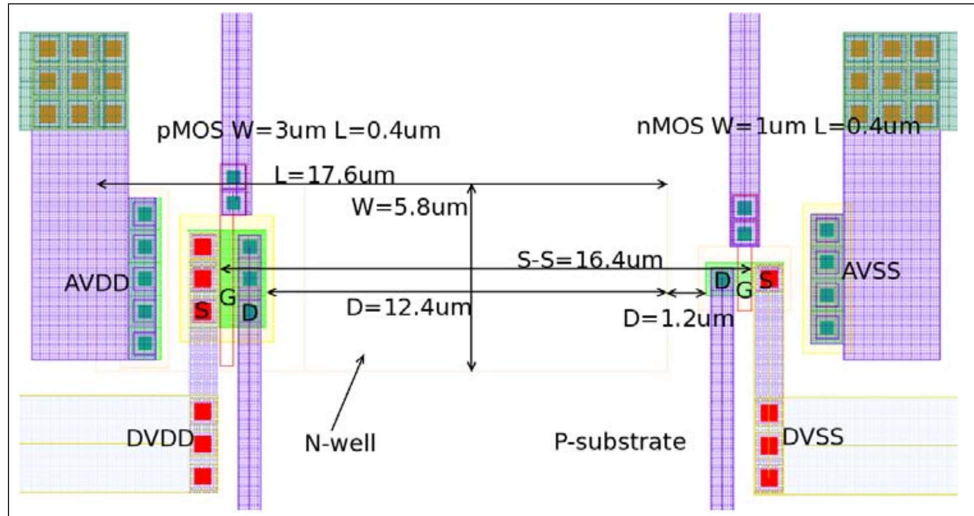

Figure A.50: Structure D3 - An inverter with the N-well increased in size along the X-axis towards the nMOS transistor. The new size is a length of 17.6μm and a width of 5.8μm.

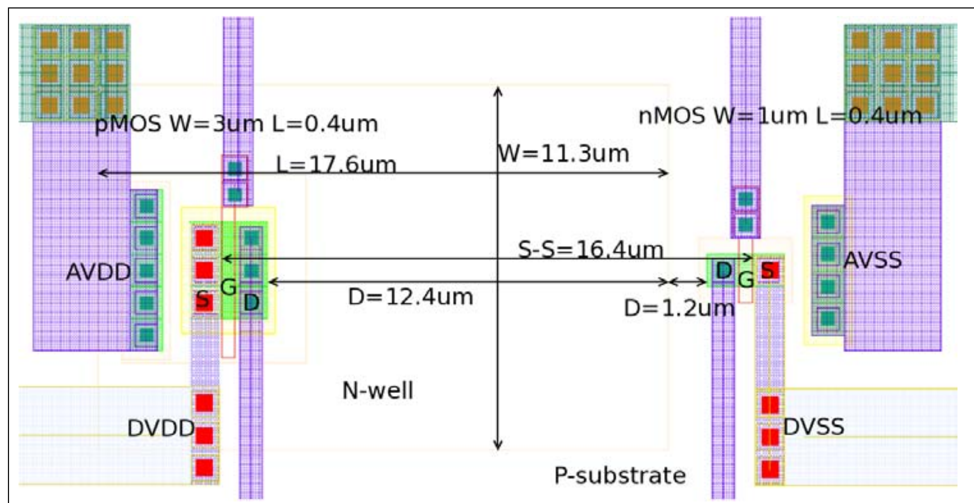

Figure A.51: Structure D4 - An inverter with the N-well increased in size along the X-axis towards the nMOS transistor and the Y-axis. The new size is a length of 17.6μm and a width of 11.3μm.

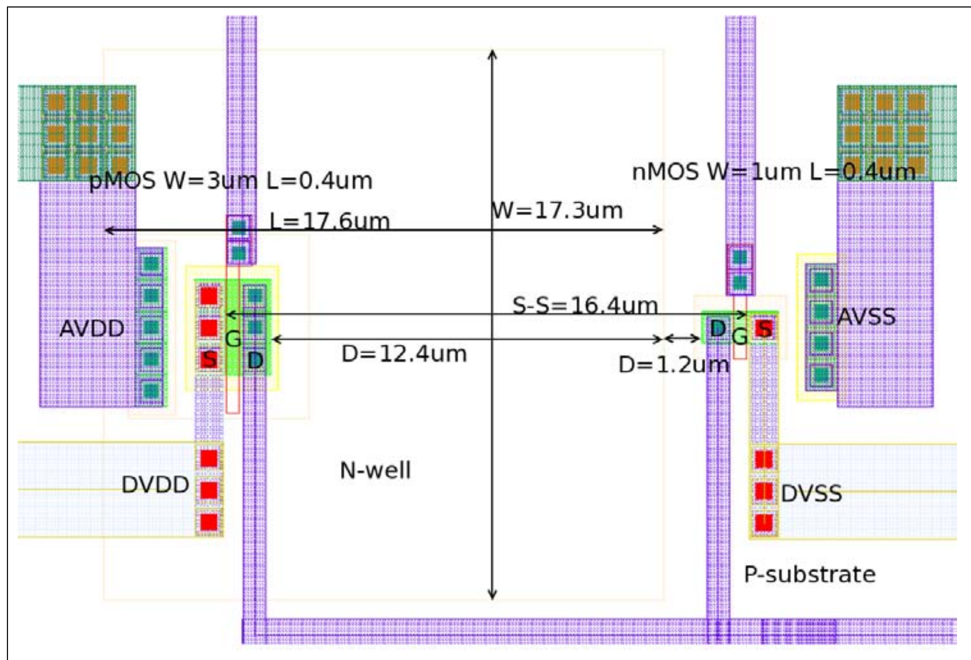

Figure A.52: Structure D5 - An inverter with the N-well increased in size along the X-axis towards the nMOS transistor and the Y-axis. The new size is a length of 17.6μm and a width of 17.3μm.

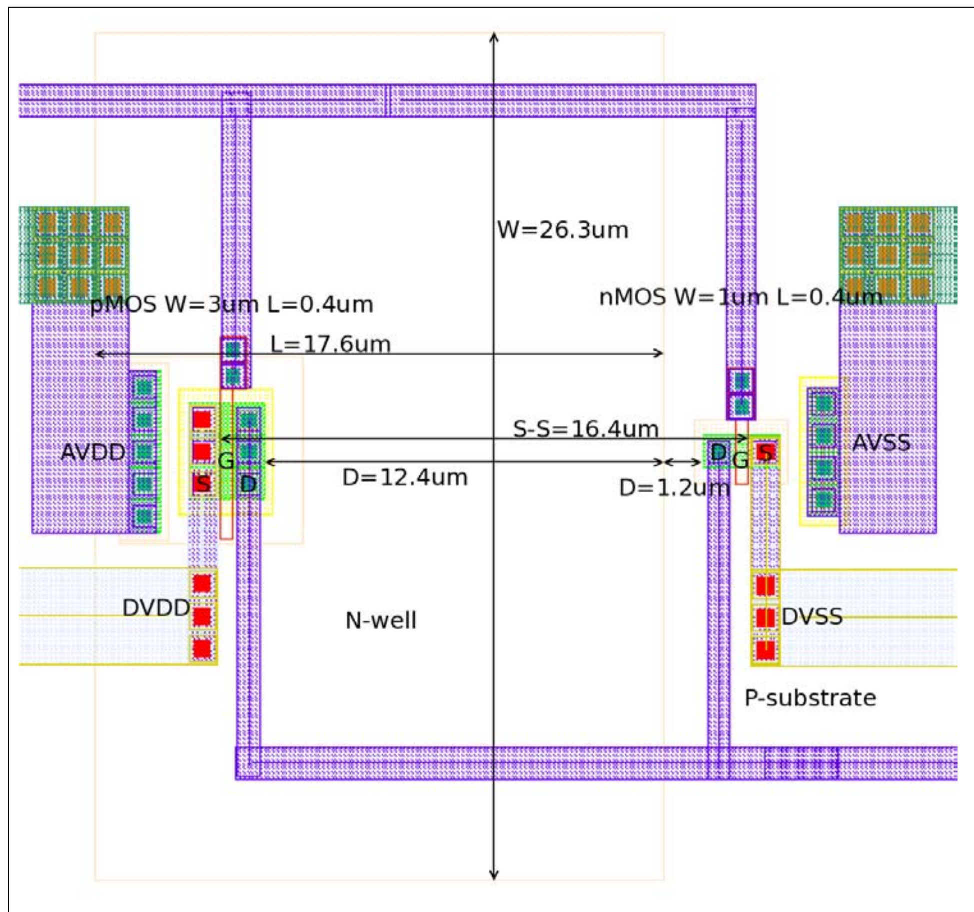

Figure A.53: Structure D6 - An inverter with the N-well increased in size along the X-axis towards the nMOS transistor and the Y-axis. The new size is a length of 17.6μm and a width of 26.3μm.

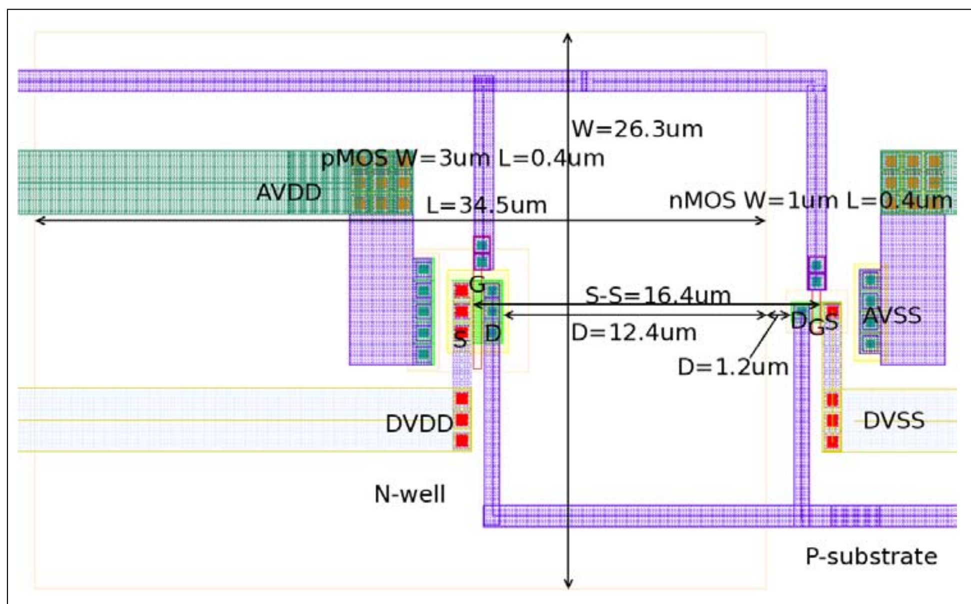

Figure A.54: Structure D7 - An inverter with the N-well increased in size along the X-axis and Y-axis in both directions. The new size is a length of 34.5μm and a width of 26.3μm.

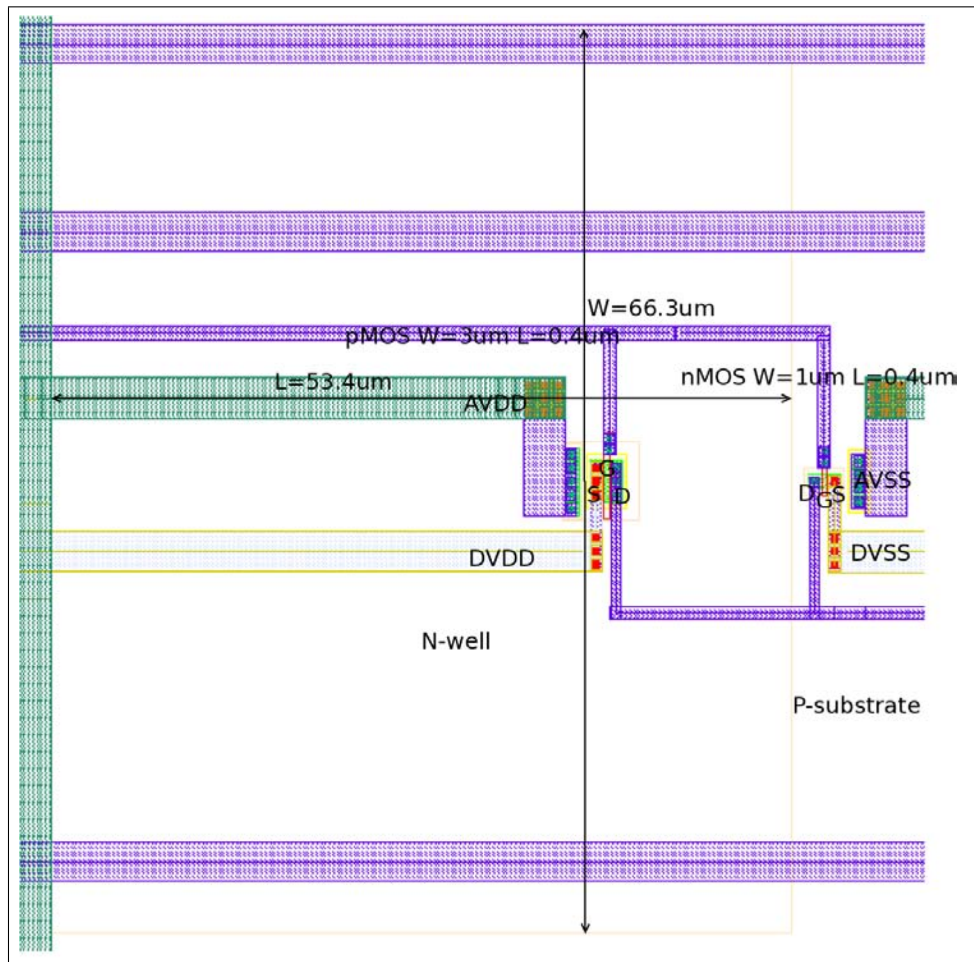

Figure A.55: Structure D8 - An inverter with the N-well increased in size along the X-axis and Y-axis in both directions. The new size is a length of 53.4μm and a width of 66.3μm.

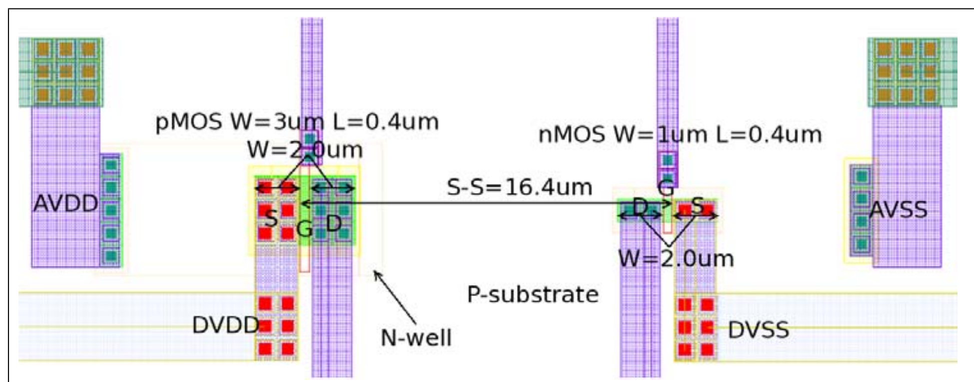

Figure A.56: Structure D9 - An inverter with source and drain areas 2x the standard inverter.

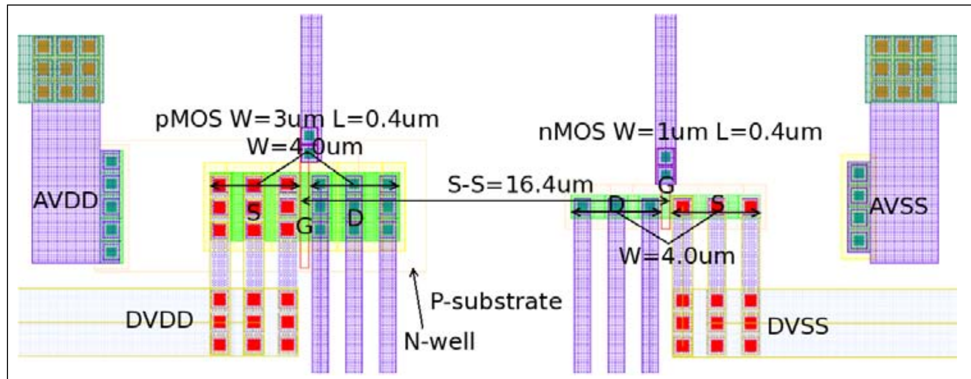

Figure A.57: Structure D10 - An inverter with source and drain areas 4x the standard inverter.

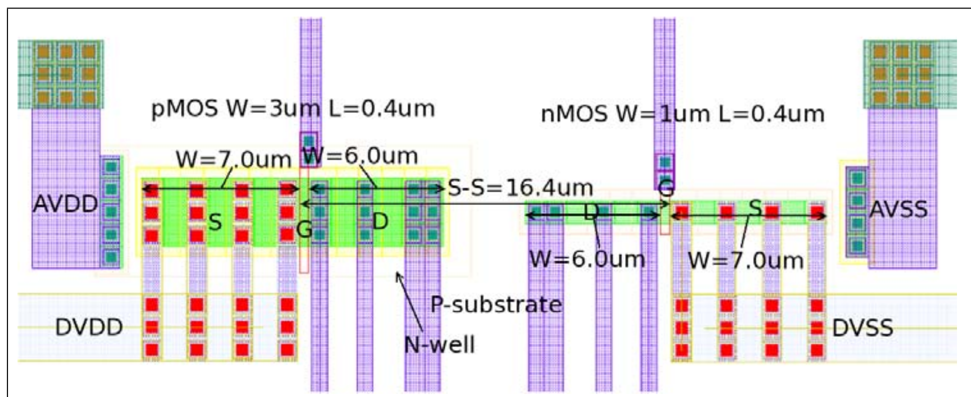

Figure A.58: Structure D11 - An inverter with source areas 7x and drain areas 6x the standard inverter.

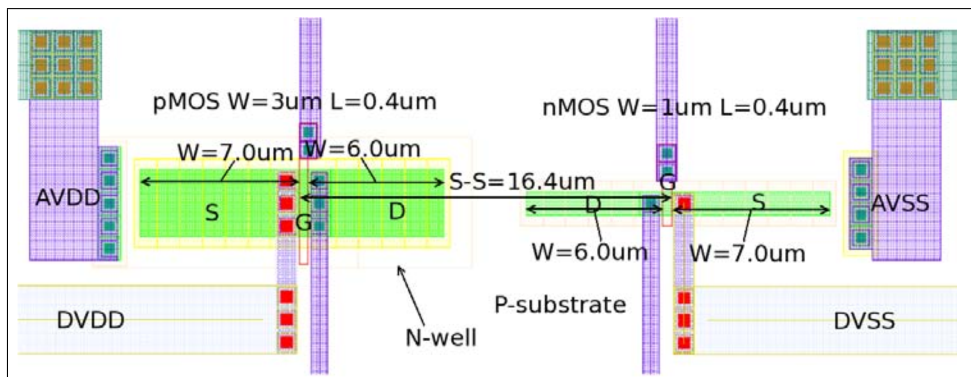

Figure A.59: Structure D12 - An inverter with source areas 7x and drain areas 6x the standard inverter, here with power/ground connection closest to the transistor gate.

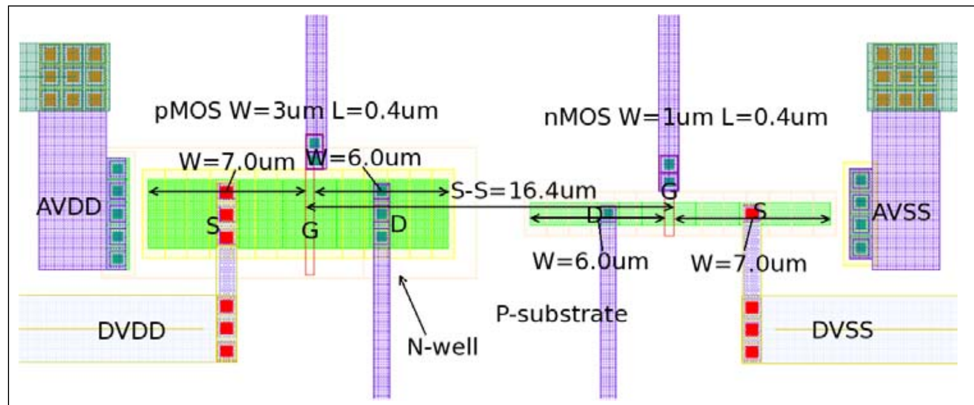

Figure A.60: Structure D13 - An inverter with source areas 7x and drain areas 6x the standard inverter, here with power/ground connection in the middle of the source/drain.

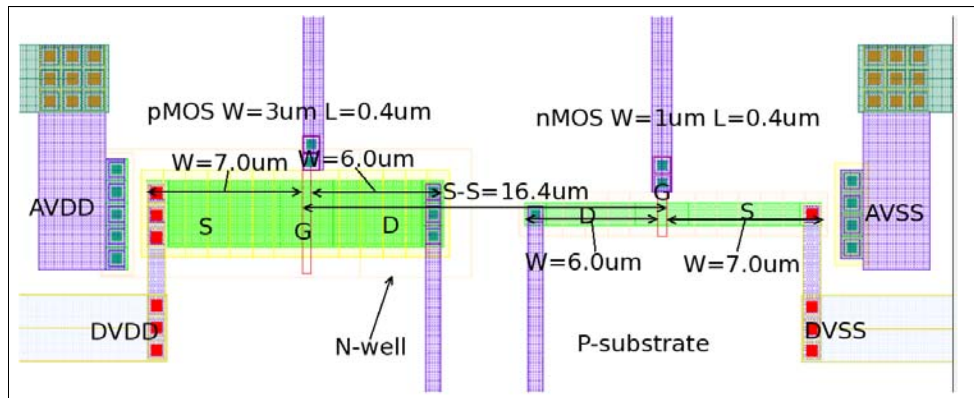

Figure A.61: Structure D14 - An inverter with source areas 7x and drain areas 6x the standard inverter, here with power/ground connection furthest away from the transistor gate.

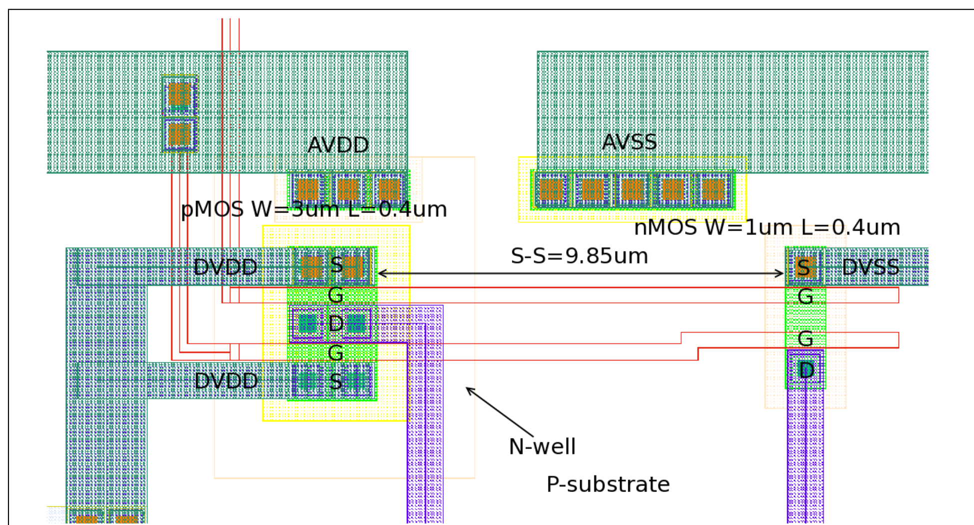

Figure A.62: Structure D15 - A standard GMI 2 input NAND gate.

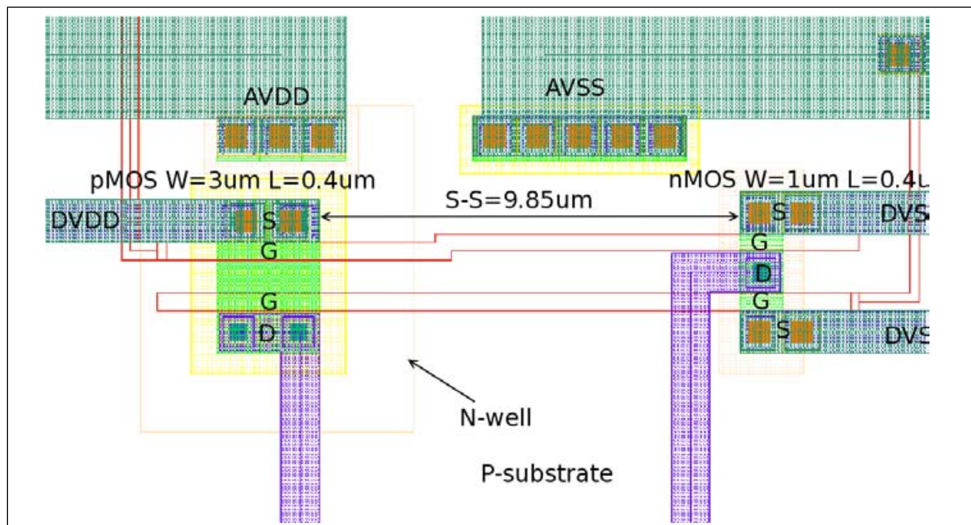

Figure A.63: Structure D16 - A standard GMI 2 input NOR gate.

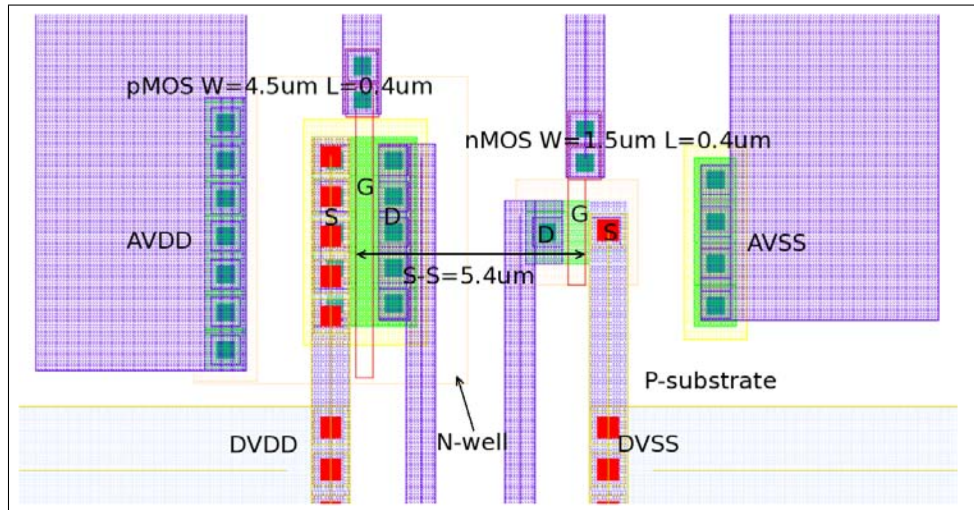

Figure A.64: Structure E1 - An inverter with transistor width of W_{pMOS} = 4.5μm / W_{nMOS} = 1.5μm. The transistors are placed in parallel along the Y-axis.

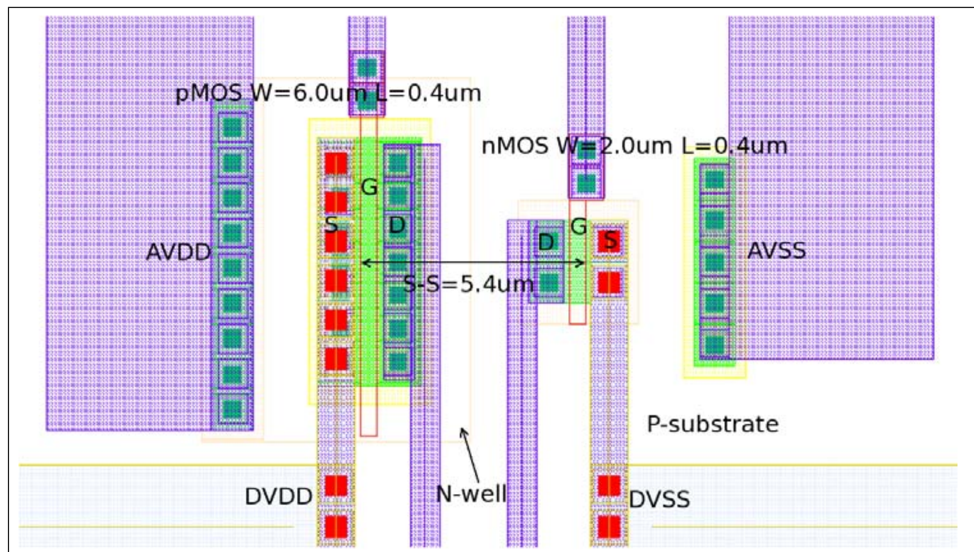

Figure A.65: Structure E2 - An inverter with transistor width of W_{pMOS} = 6.0μm / W_{nMOS} = 2.0μm. The transistors are placed in parallel along the Y-axis.

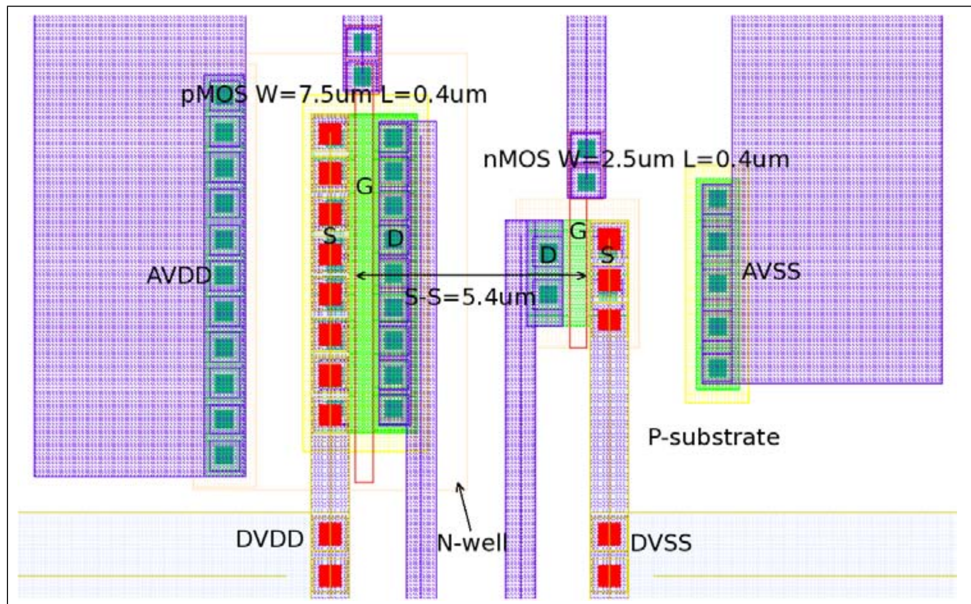

Figure A.66: Structure E3 - An inverter with transistor width of W_{pMOS} = 7.5μm / W_{nMOS} = 2.5μm. The transistors are placed in parallel along the Y-axis.

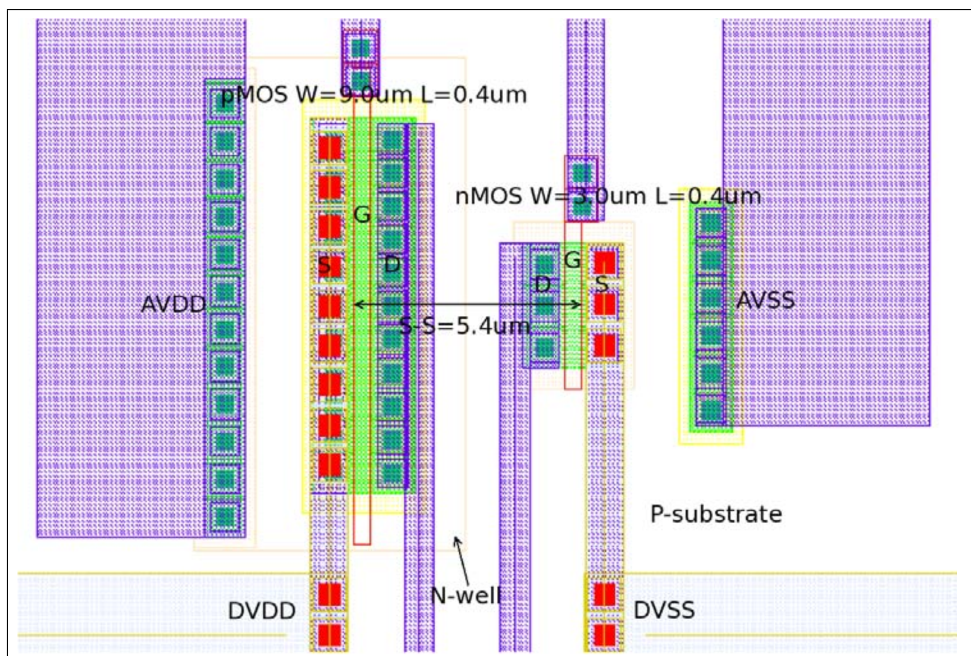

Figure A.67: Structure E4 - An inverter with transistor width of W_{pMOS} = 9.0μm / W_{nMOS} = 3.0μm. The transistors are placed in parallel along the Y-axis.

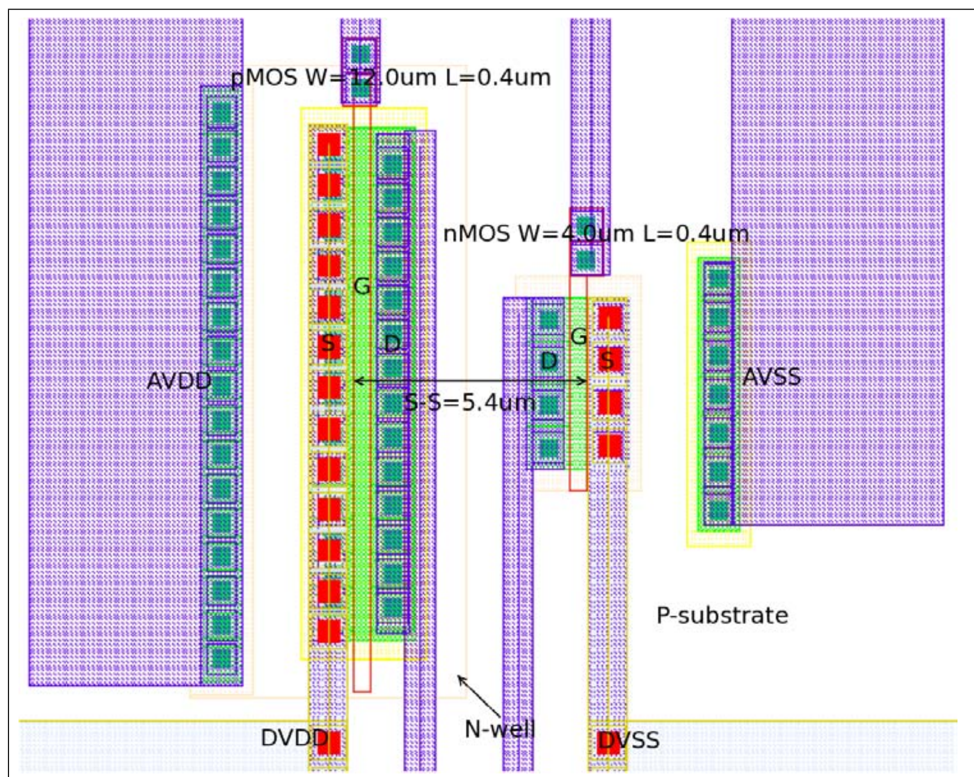

Figure A.68: Structure E5 - An inverter with transistor width of W_{pMOS} = 12.0μm / W_{nMOS} = 4.0μm. The transistors are placed in parallel along the Y-axis.

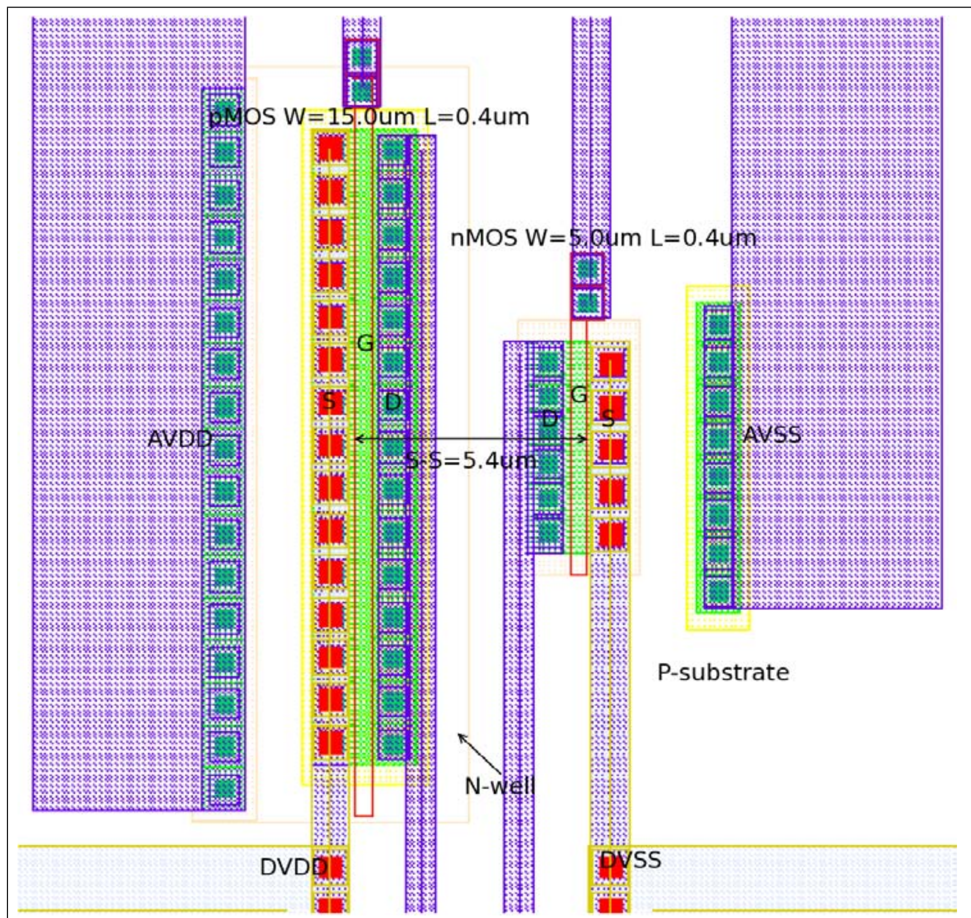

Figure A.69: Structure E6 - An inverter with transistor width of W_{pMOS} = 15.0μm / W_{nMOS} = 5.0μm. The transistors are placed in parallel along the Y-axis.

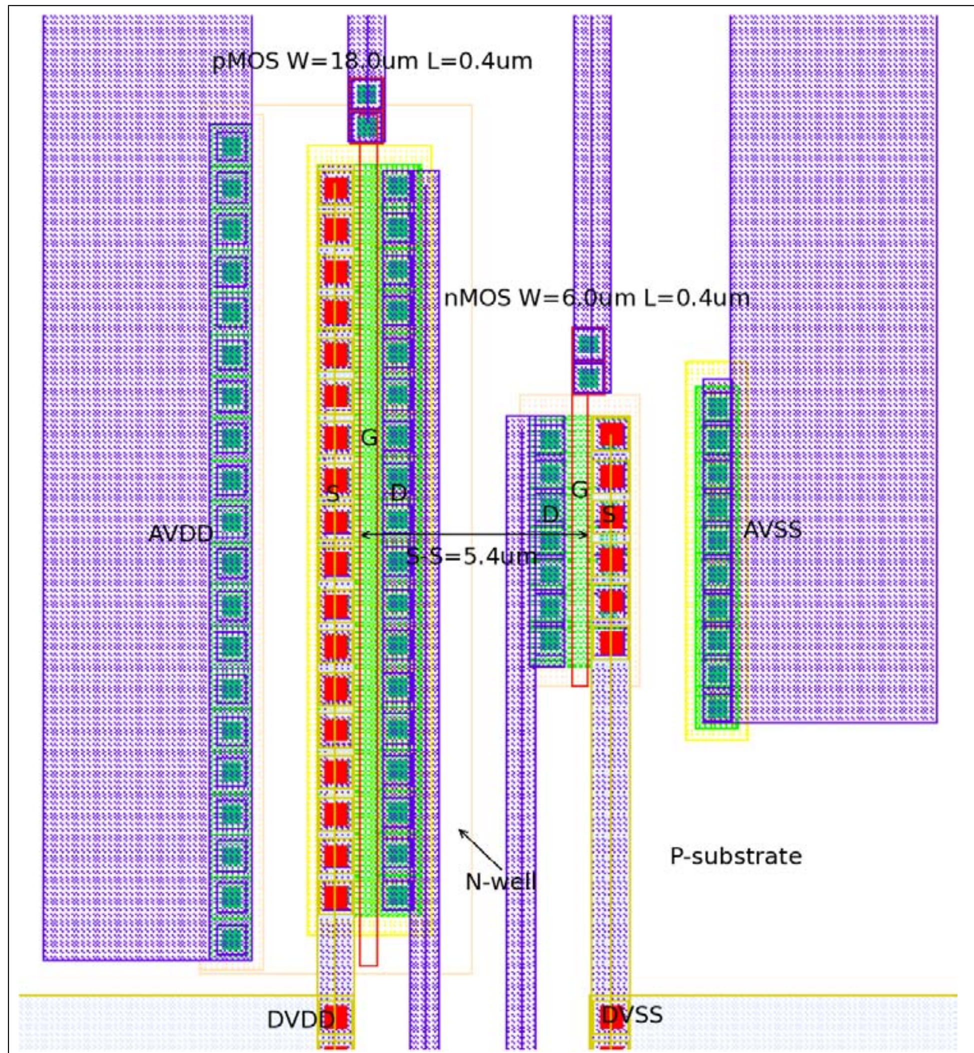

Figure A.70: Structure E7 - An inverter with transistor width of W_{pMOS} = 18.0μm / W_{nMOS} = 6.0μm. The transistors are placed in parallel along the Y-axis.

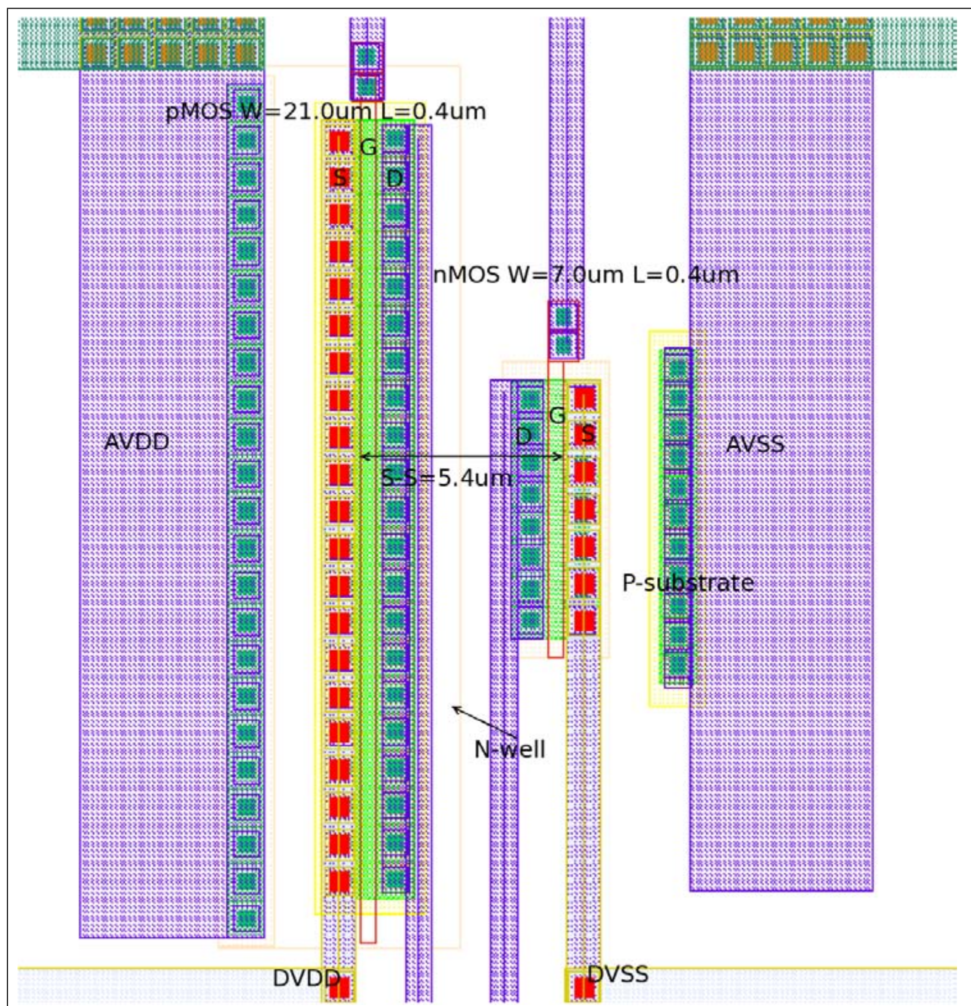

Figure A.71: Structure E8 - An inverter with transistor width of W_{pMOS} = 21.0μm / W_{nMOS} = 7.0μm. The transistors are placed in parallel along the Y-axis.

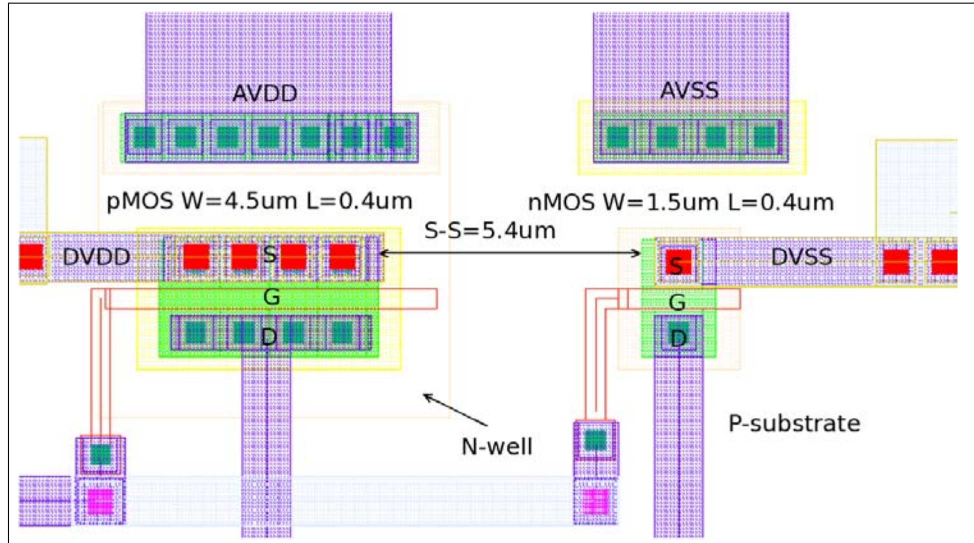

Figure A.72: Structure E9 - An inverter with transistor width of W_{pMOS} = 4.5μm / W_{nMOS} = 1.5μm. The transistors are placed one after the other along the X-axis.

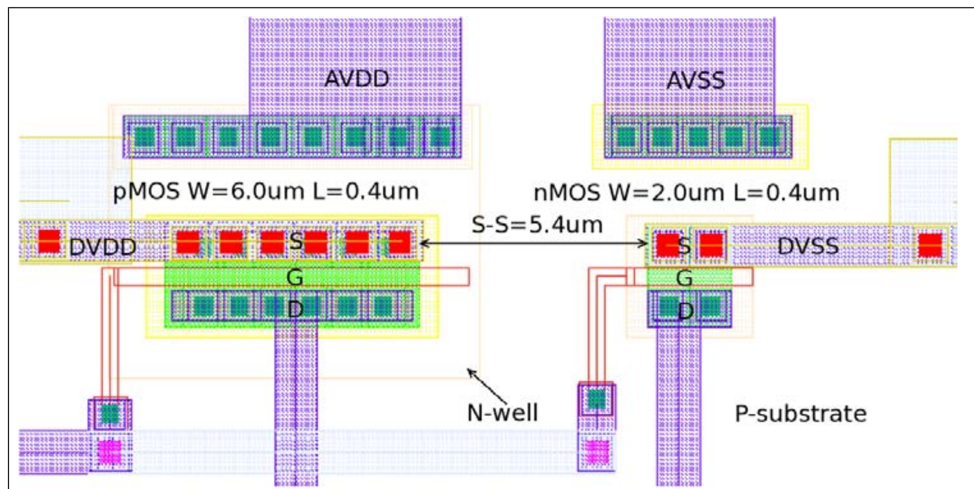

Figure A.73: Structure E10 - An inverter with transistor width of W_{pMOS} = 6.0μm / W_{nMOS} = 2.0μm. The transistors are placed one after the other along the X-axis.

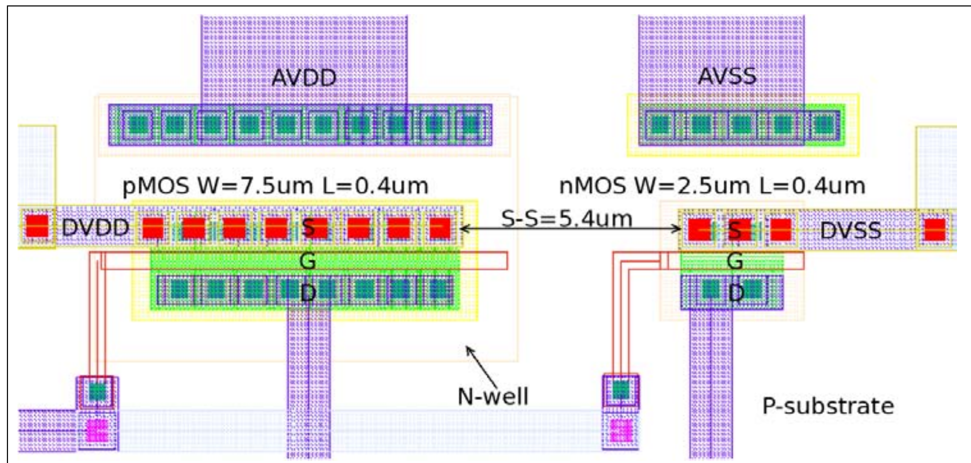

Figure A.74: Structure E11 - An inverter with transistor width of W_{pMOS} = 7.5μm / W_{nMOS} = 2.5μm. The transistors are placed one after the other along the X-axis.

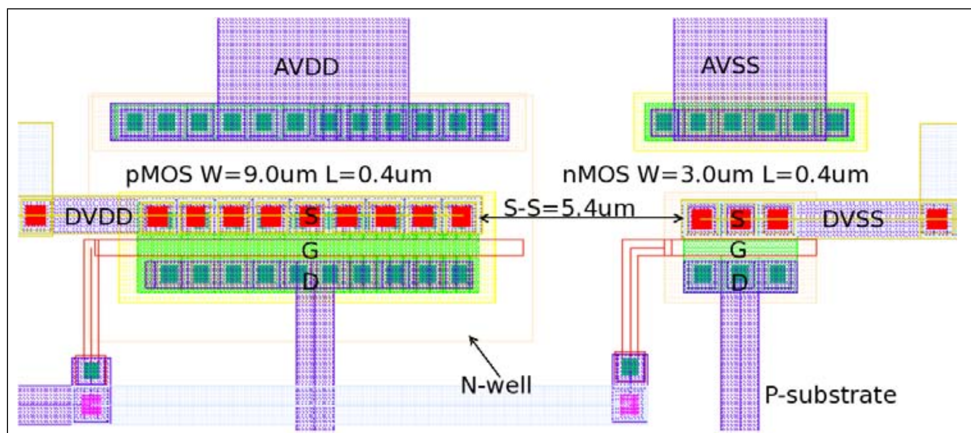

Figure A.75: Structure E12 - An inverter with transistor width of W_{pMOS} = 9.0μm / W_{nMOS} = 3.0μm. The transistors are placed one after the other along the X-axis.

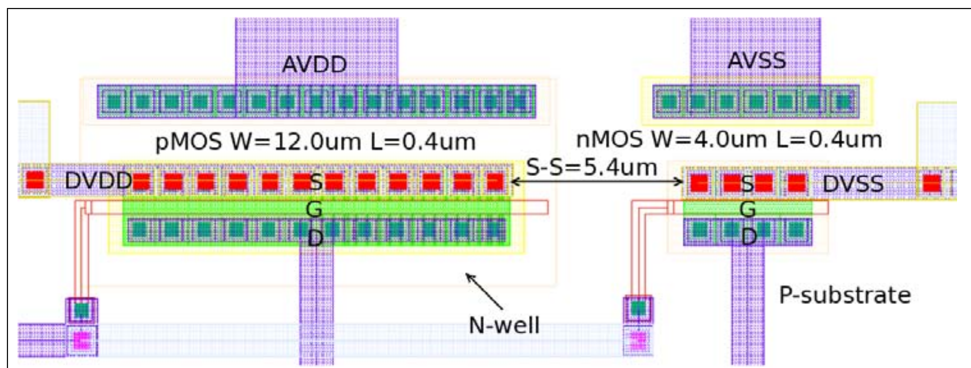

Figure A.76: Structure E13 - An inverter with transistor width of W_{pMOS} = 12.0μm / W_{nMOS} = 4.0μm. The transistors are placed one after the other along the X-axis.

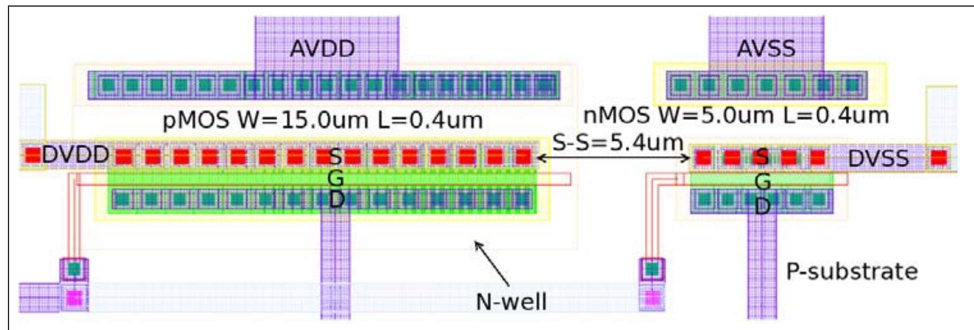

Figure A.77: Structure E14 - An inverter with transistor width of W_{pMOS} = 15.0μm / W_{nMOS} = 5.0μm. The transistors are placed one after the other along the X-axis.

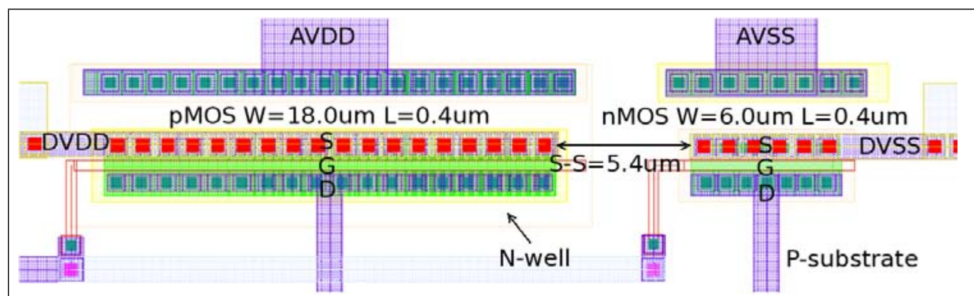

Figure A.78: Structure E15 - An inverter with transistor width of W_{pMOS} = 18.0μm / W_{nMOS} = 6.0μm. The transistors are placed one after the other along the X-axis.

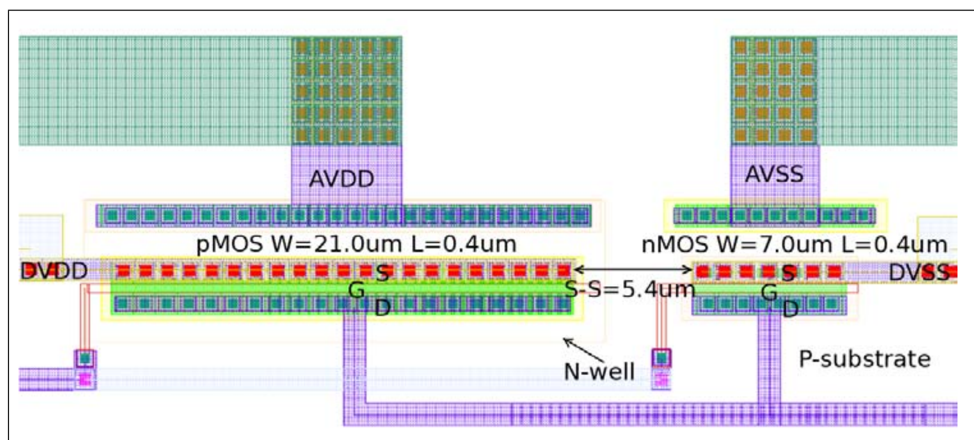

Figure A.79: Structure E16 - An inverter with transistor width of W_{pMOS} = 21.0μm / W_{nMOS} = 7.0μm. The transistors are placed one after the other along the X-axis.

Appendix B

Str.	Column A	Column B	Column C	Column D	Column E
1	$91.7\mu m^2$	$122.1\mu m^2$	$76.0\mu m^2$	$135.4\mu m^2$	$96.0\mu m^2$
2	$67.3\mu m^2$	$117.8\mu m^2$	$76.0\mu m^2$	$135.4\mu m^2$	$115.7\mu m^2$
3	$70.2\mu m^2$	$121.4\mu m^2$	$78.0\mu m^2$	$135.4\mu m^2$	$135.4\mu m^2$
4	$73.1\mu m^2$	$231.3\mu m^2$	$64.4\mu m^2$	$263.9\mu m^2$	$155.2\mu m^2$
5	$76.0\mu m^2$	$238.7\mu m^2$	$64.4\mu m^2$	$404.0\mu m^2$	$194.6\mu m^2$
6	$78.9\mu m^2$	$238.7\mu m^2$	$80.6\mu m^2$	$614.1\mu m^2$	$234.1\mu m^2$
7	$84.7\mu m^2$	$163.0\mu m^2$	$86.4\mu m^2$	$1057.3\mu m^2$	$272.5\mu m^2$
8	$90.5\mu m^2$	$211.5\mu m^2$	$92.2\mu m^2$	$3981.3\mu m^2$	$313.0\mu m^2$
9	$102.1\mu m^2$	$264.0\mu m^2$	$98.0\mu m^2$	$200.7\mu m^2$	$94.3\mu m^2$
10	$113.7\mu m^2$	$162.1\mu m^2$	$109.6\mu m^2$	$200.7\mu m^2$	$106.7\mu m^2$
11	$131.1\mu m^2$	$210.4\mu m^2$	$121.3\mu m^2$	$200.7\mu m^2$	$120.9\mu m^2$
12	$148.5\mu m^2$	$262.7\mu m^2$	$144.4\mu m^2$	$200.7\mu m^2$	$133.3\mu m^2$
13	$177.5\mu m^2$	$121.4\mu m^2$	$167.6\mu m^2$	$200.7\mu m^2$	$159.9\mu m^2$
14	$235.5\mu m^2$	$170.7\mu m^2$	$202.4\mu m^2$	$200.7\mu m^2$	$185.3\mu m^2$
15	$322.5\mu m^2$	$170.7\mu m^2$	$231.4\mu m^2$	$119.0\mu m^2$	$211.9\mu m^2$
16	$612.5\mu m^2$	$204.4\mu m^2$	$306.8\mu m^2$	$122.8\mu m^2$	$237.3\mu m^2$

Table B.1: Total area of the inverter structures. The area is measured as the smallest square that can contain the entire nMOS and pMOS including the N-well and P-substrate contacts.

Str.	E_{th} 1	E_{th} 2	E_{th} 3	E_{th} 4	E_{th} 5	I_{SEL} 1	I_{SEL} 2	I_{SEL} 3	I_{SEL} 4	I_{SEL} 5
C1	27.8	26.6	28.2	27.8	30.9	47.5	47.0	46.0	47.0	44.0
C2	4.7	5.0	4.7	5.0	5.4	56.0	58.0	56.0	56.5	56.0
C3	27.8	27.4	28.2	29.0	30.1	47.0	47.5	46.0	47.0	44.0
C4	29.4	28.2	29.8	29.8	32.9	47.0	47.5	46.0	47.0	44.0
C5	27.8	25.0	28.2	28.2	28.6	47.0	47.5	46.0	47.0	44.0
C6	26.6	25.0	29.8	27.8	29.4	47.0	47.5	46.0	47.0	44.0
C7	27.4	26.6	29.8	27.8	29.8	47.0	47.5	46.0	47.0	44.0
C8	27.0	25.8	29.0	28.6	30.5	47.0	47.5	46.0	47.0	44.0
C9	27.8	24.7	30.1	27.4	30.5	47.0	47.5	46.0	47.0	44.0
C10	28.6	25.8	31.7	29.4	30.9	47.0	47.5	46.0	46.5	44.0
C11	29.4	26.2	31.3	28.6	30.9	47.0	47.5	46.0	46.5	44.0
C12	8.2	7.9	9.0	7.4	9.8	39.0	39.5	36.0	38.0	36.5
C13	6.6	5.8	8.2	6.2	9.0	43.0	42.5	39.5	41.5	38.0
C14	5.8	4.7	6.2	5.8	7.0	45.0	45.5	42.5	46.5	42.0
C15	5.4	4.7	5.0	5.4	6.6	45.0	46.5	44.5	45.5	42.5
C16	0.0	4.7	4.7	5.0	5.4	47.0	47.5	45.0	46.0	43.5

Table B.2: Energy threshold (E_{th}) and latch-up current (I_{SEL}) measured after exposing column C on 5 different epitaxial devices. Latch-up current is denoted in mA and energy threshold is specified in the energy setting displayed on the laser module. This energy threshold setting can be translated into a percentage of the maximum energy of 3.15μJ by using the ”IR-UV Lo“slope in figure 3.1.

Str.	E_{th} 1	E_{th} 2	E_{th} 3	E_{th} 4	E_{th} 5	I_{SEL} 1	I_{SEL} 2	I_{SEL} 3	I_{SEL} 4	I_{SEL} 5
C1	-	44.3	42.3	56.0	-	0	59.0	60.0	56.0	0
C2	7.4	5.8	5.4	6.2	-	59.0	58.5	60.5	58.0	0
C3	-	-	-	-	-	0	0	0	0	0
C4	-	-	-	-	-	0	0	0	0	0
C5	-	-	-	-	-	0	0	0	0	0
C6	-	-	-	-	-	0	0	0	0	0
C7	-	-	-	-	-	0	0	0	0	0
C8	-	-	-	-	-	0	0	0	0	0
C9	7.4	5.8	7.0	6.6	4.7	42.0	41.5	40.0	40.0	40.0
C10	6.6	5.0	5.8	5.4	0.0	48.0	47.5	46.5	46.0	46.5
C11	5.8	4.3	5.4	4.3	0.0	51.0	50.5	50.5	50.0	50.5
C12	4.7	3.9	0.0	0.0	0.0	55.0	53.5	53.5	53.5	53.5
C13	0.0	0.0	0.0	0.0	0.0	275	265	265	270	270
C14	0.0	0.0	0.0	0.0	0.0	275	265	265	270	270
C15	0.0	0.0	0.0	0.0	0.0	275	265	265	270	270
C16	0.0	0.0	0.0	0.0	0.0	275	265	265	270	270

Table B.3: Energy threshold (E_{th}) and latch-up current (I_{SEL}) measured after exposing column C on 5 different bulk devices. Latch-up current is denoted in mA and energy threshold is specified in the energy setting displayed on the laser module. This energy threshold setting can be translated into a percentage of the maximum energy of 3.15μJ by using the ”IR-UV Lo“slope in figure 3.1.

Str.	E_{th} 1	E_{th} 2	E_{th} 3	E_{th} 4	E_{th} 5	I_{SEL} 1	I_{SEL} 2	I_{SEL} 3	I_{SEL} 4	I_{SEL} 5
D1	-	-	-	-	-	0	0	0	0	0
D2	-	-	-	-	-	0	0	0	0	0
D3	-	-	-	-	-	0	0	0	0	0
D4	-	-	-	-	-	0	0	0	0	0
D5	-	-	-	-	-	0	0	0	0	0
D6	-	-	-	-	-	0	0	0	0	0
D7	-	-	-	-	-	0	0	0	0	0
D8	38.4	42.7	42.7	44.3	49.4	270	270	270	270	275
D9	5.8	6.2	6.6	6.6	6.6	270	270	270	270	275
D10	5.4	5.8	5.8	5.0	6.2	270	270	270	270	275
D11	5.0	6.6	6.2	5.8	6.6	270	270	270	270	275
D12	31.3	30.9	38.8	33.7	37.2	270	270	270	270	275
D13	35.2	34.1	38.4	34.9	38.0	60.0	61.0	59.0	60.0	64.0
D14	-	-	-	-	-	0	0	0	0	0
D15	-	11.7	12.3	12.3	13.3	0	55.0	55.5	60.0	55.5
D16	-	9.8	10.1	10.1	10.9	0	42.0	42.5	42.0	43.0

Table B.4: Energy threshold (E_{th}) and latch-up current (I_{SEL}) measured after exposing column D on 5 different bulk devices. Latch-up current is denoted in mA and energy threshold is specified in the energy setting displayed on the laser module. This energy threshold setting can be translated into a percentage of the maximum energy of 3.15μJ by using the "IR-UV Lo"slope in figure 3.1.

Str.	E_{th} 1	E_{th} 2	E_{th} 3	E_{th} 4	E_{th} 5	I_{SEL} 1	I_{SEL} 2	I_{SEL} 3	I_{SEL} 4	I_{SEL} 5
E1	9.8	-	-	-	-	39.5	0	0	0	0
E2	9.4	13.3	7.8	9.4	9.4	56.0	55.0	56.0	57.5	57.5
E3	10.9	13.3	8.2	9.4	9.8	55.0	55.5	56.0	55.5	56.0
E4	10.9	13.7	8.2	9.8	10.5	73.0	72.5	73.0	74.5	73.5
E5	10.9	13.7	9.4	9.4	10.9	84.0	84.5	83.0	84.5	84.0
E6	10.9	14.1	9.4	10.1	10.9	94.5	94.5	94.0	95.0	94.5
E7	11.3	14.1	9.8	9.8	10.9	103.0	103.0	103.0	102.5	103.0
E8	11.3	14.5	10.1	10.1	10.9	112.0	113.0	112.0	112.0	112.0
E9	-	-	-	-	-	0	0	0	0	0
E10	-	-	-	-	-	0	0	0	0	0
E11	-	-	-	-	-	0	0	0	0	0
E12	-	-	-	-	-	0	0	0	0	0
E13	-	-	-	-	-	0	0	0	0	0
E14	-	-	-	-	-	0	0	0	0	0
E15	-	-	-	-	-	0	0	0	0	0
E16	-	-	-	-	-	0	0	0	0	0

Table B.5: Energy threshold (E_{th}) and latch-up current (I_{SEL}) measured after exposing column E on 5 different bulk devices. Latch-up current is denoted in mA and energy threshold is specified in the energy setting displayed on the laser module. This energy threshold setting can be translated into a percentage of the maximum energy of 3.15μJ by using the "IR-UV Lo"slope in figure 3.1.