Configurable Multiple Value Encoders using Semi Floating-Gate

Dr. Scient thesis

René Jensen

May, 16th
2008

ACKNOWLEDGMENTS

ABSTRACT

This thesis presents a new multiple-valued encoder with re-configurable radix. The proposed circuits utilize serial cyclic D/A conversion and semi floating-gate (SFG) inverters for compact design and a high functional capacity per device. A re-configurable radix is not supported by existing SFG inverter based multiple-valued encoders which make use of parallel binary weight D/A conversion. The study covers least significant bit-first (LSB), least significant bit-first with alternate bit inversion (LSB ABI) and most significant bit-first (MSB) digital input codes.

The serial cyclic D/A converters with LSB and LSB ABI input codes are implemented in a double-poly 0.35um AMS process. Measured results are provided and analyzed using standard static D/A converter performance measures. Circuits are tested using the practical radices 4, 8 and 16. Experimental results demonstrate that serial cyclic D/A converters using SFG inverters are feasible. Compared to related work on cyclic D/A conversion, the proposed circuits feature both a reduced number of devices and a reduction in the required die area.

Several new techniques are identified for extending the resolution beyond radix 4, 8 and 16 MVL applications. This includes an error correction algorithm called least significant bit-first with alternate bit inversion (LSB ABI), a sample and hold clock scheme and a Dual Data-Rate (DDR) mode of D/A converter operation. The techniques are implemented on a chip and measured results are provided.

The thesis also includes simulation work on several new SFG based circuits. A ternary serial D/A converter, a MSB-first serial D/A converter and a multiple-valued frequency divider which features re-configurable modulus.

Contents

ACRONYMS AND ABBREVIATIONS

ABI	Alternate bit inversion
A/D	Analog-to-digital
ADC	Analog-to-digital converter
ASIC	Application-specific integrated circuits
ATI	Alternate trit inversion
CFT	Clock feedthrough
CMOS	Complementary metal-oxide semiconductor
DAC	Digital-to-analog converter
D/A	Digital-to-analog
DC	Direct current
DNL	Differential non-linearity
DR	Dynamic range
DDR	Dual data-rate
EDP	Energy delay product
ENOB	Effective number of bits resolution
FDIV	Frequency divider
FG	Floating-gate
FoM	Figure of merit
GPIB	General purpose interface bus
INL	Integral non-linearity
LSB	Least significant bit
LST	Least significant trit
MOS	Metal-oxide semiconductor
MSB	Most significant bit
MST	Most significant trit
MVL	Multiple valued logic
MV	Multiple valued
NMOS	N-channel metal oxide semi-conductor
NOB	Number of bits
OTA	Operational transconductance amplifier
PDP	Power delay product
PMOS	P-channel metal-oxide semi-conductor
PSRR	Power supply rejection ratio
SC	Switched capacitor
SDR	Single data-rate
SFG	Semi floating-gate
S/H	Sample-and-hold

SNDR   Signal-to-noise-and-distortion ratio
T/H   Track-and-hold
ULSI   Ultra-high large-scale integration
VLSI   Very high large-scale integration
VM   Voltage mode

NOTATION AND NOMENCLATURE

Throughout the thesis, the multiple valued output voltages of serial D/A converters are denoted Y_n. Converters use bit-serial digital input codes. Each code or input word consists of n bit and is denoted B. The i-th bit of a code is referred to as b_i. In this thesis converters perform a bit-wise conversion of the codes, one bit per iteration. The intermediate multiple valued output voltages are denoted Y_i.

B	Digital input word
b_i	i-th bit of a bit-serial input code
D_i	Deviation
f_b	Bit-rate
f_N	Nyquist frequency, $f_N = f_{s/2}$
f_s	Sampling or update frequency
f_S	Symbol-rate
n	Number of bits resolution
R	Radix, $R = 2^n$
Y_i	Intermediate analog output voltage after the i-th bit
Y_n	Analog output voltage with n bit resolution
Φ	Recharge clock/Bit clock
Ψ	Reset clock/Output symbol or multiple value clock
V^-	Lower end of voltage swing
V^+	Upper end of voltage swing
V_{LSB}	Least significant bit voltage/Smallest voltage step

Chapter 1

INTRODUCTION

Digital computing has reached widespread use and digital (binary) logic circuits dominate the computer industry. The digital technological revolution is binary. Modern microelectronic fabrication processes and design tools are tailored to meet the demands of digital (binary) circuits.

The concept of how to represent information and information theory has deep roots. Already in 1948 Shannon introduced the idea of information entropy [1]. Intuitively it relates to the uncertainty about an event associated with a probability distribution. According to Shannon, binary signals have a very low entropy and are less efficient than alternate multiple-valued representations. However, a low entropy is often the most robust representation. For instance, digital (binary) VLSI circuits implement binary logic and have the best noise-margins.

In [2], Multiple-Valued Logic (MVL) is proposed as a possible alternative to the digital paradigm. MVL is an alternative with more than two logical values and a higher information entropy. In 1920 Lukasiewicz developed multiple-valued logic of more than two logical truth values. At the same time the American mathematician Emil Post introduced his many valued Post algebra. Post algebra is applicable for optimization of MVL. The MVL research community has its own IEEE organized conference called the "International Symposium of Multiple Valued Logic" (ISMVL). It has been held on an annual basis since 1971. In [3] Etiemble argues strongly that multiple-valued logic is restricted to a small niche. The feasibility of new paradigm MVL depends on the availability of devices constructed for MVL operations [4]. These devices are often associated with a higher functional capacity.

In todays binary world, radix converters have become an immediate concern [5]. Several radix converters are proposed. This includes LUT-cascades [6], arithmetic decompositions [7], iterated function systems [8] and linear coded weights [9]. Radix conversion is described as a complex task. The proposals

are modular but do not necessarily support runtime re-configuration of the radix. The most efficient binary to multiple-valued radix conversion utilizes radices corresponding to an integer number of bit resolution. This also allows implementation using a binary weighted digital to analog converter [10].

Practical radix converter implementations normally assume bit-parallel transmission of digital (binary) input. This means that the number of interconnections and number of bit resolution are fixed. A change in radix therefore requires a redesign of the circuit.

In many applications the cost of interconnection and synchronization makes bit-parallel transmission impractical. Interconnections are a limited resource in modern VLSI, in particular inter-chip connections. A common solution is the use of time multiplexed systems where digital data is communicated serially. In applications where digital input is transmitted serially, a single interconnect can be sufficient. Radix conversion by use of inherently parallel algorithms requires an initial serial to parallel conversion. This solution becomes a problem as it requires considerable chip area. Serial buses are becoming more common. This motivates the development of alternate serial D/A converters. A serial D/A converter is simple and cheap to implement.

Industrial use of floating-gate [11] has long traditions from initial use as EEPROM memories to portable flash memories. Today, FGMOS devices have reached applications [12] beyond memory technology. One example is semi floating-gate (SFG) devices – volatile floating-gate inverters recharged periodically by a recharge clock signal. In this thesis semi floating-gate (SFG) inverters, volatile floating-gate inverters recharged periodically by a recharge clock signal, are utilized for multiple-valued logic purposes. Another example is Field Programmable Gate Arrays (FPGA). Some FPGA implementations exploit floating-gates to create and break connections. Adaptive and reconfigurable circuits are known to reduce the time to market as well as increase the life span of circuits. The importance of configurable floating-gate circuits is emphasized by Aunet *et al.* in [13][14] and by Kelly *et al.* in [15].

This thesis will present the development of configurable serial D/A converters using semi floating-gate (SFG) devices. It introduces flexible/adaptive algorithms with runtime reconfigurable radix. The converters proposed are compact alternatives to traditional radix converters based on parallel binary weight D/A conversion algorithms[16][17][18].

1.1   Objectives

The most important aims of this PhD thesis are:

- To develop new and more compact radix converters based on the proposed semi floating-gate based configurable serial D/A converter.

- To bring additional knowledge into the field of volatile floating-gate design and multiple-valued logic by working with problems related to reconfigurable iterative algorithms. In particular the utilization of the semi floating-gate latch and the semi floating-gate inverter devices when using a non-overlapping two-phase clocking strategy.

- To demonstrate through physical implementations, that semi floating-gate devices can be used in a practical serial D/A conversion application.

- To characterize the linearity of the introduced converters and the associated effective radix using static D/A converter performance measures.

- To improve the effective radix of the SFG serial D/A converter using an error correction scheme referred to as alternate bit inversion (ABI).

- To develop a compact SFG MV frequency divider featuring asymmetrical output clock signal and reconfigurable modulus. The circuit is auxiliary to the D/A converter but applicable as bit-counter and reset signal generator.

- To improve the accuracy and conversion speed of semi floating-gate based memories (SFG Latch) by proposing new and alternate SFG S/H circuits. A physical implementation will demonstrate the concept.

1.2   Related work

The work in this thesis is possible thanks to the development of Semi Floating-Gate (SFG) Latches [19] by Mirmotahari *et al.* and SFG inverters [20] introduced by Berg *et al.* SFG inverters are recharged volatile floating-gate inverters exploiting multiple-input multiple-valued floating-gate transistors [21]. Multiple-valued encoders using SFG devices are presented in [17] and [16]. However these converters use a parallel binary weight D/A converter algorithm where binary weights and radix are design parameters. Also relevant for this thesis is clock-controlled neuron-MOS logic gates [22]. Further background on neuron-MOS circuits is given in [23] and [24] by Shibata and Ohmi.

Several modular radix converters for MVL exist. Recent advances in the field include converters using LUT-cascades [6], arithmetic decompositions [7], iterated function systems [8] and linear-coded weights [9][25]. Radix conversion is a complex task and converters tend to be larger circuits. In [26][27] a simple serial D/A converter with configurable radix is introduced. The circuit is passive and utilizes switched-capacitor techniques for reduced circuit complexity.

Advances have been made on active switched-capacitor D/A converters using operational transconductance amplifiers (OTA) and standard serial digital input codes. The simplest converters are cyclic D/A converters, also referred to as algorithmic or iterative. In [28] an active LSB-first serial D/A converter is presented. [29] introduces a different solution with support for MSB-first digital input codes. Several practical cyclic D/A converter implementations have been reported [26, 29, 30, 31, 32, 33, 34, 35]. Further references to algorithmic D/A conversion are also found in [36], [37] or [30].

1.3   Main contributions

This thesis presents research on configurable multiple-valued encoders using semi floating-gate devices. The main contributions are:

New circuits for configurable serial D/A conversion using semi floating-gate devices

The most important part of this thesis is the introduction of several new serial D/A converters using semi floating-gate (SFG) inverters. This includes support of the two main standard bit-serial digital input codes; the least significant bit (LSB) first and the most significant bit (MSB) first. In addition a least significant bit first converter using alternate bit inversion (LSB ABI) is introduced.

Error cancellation in semi floating-gate based serial D/A conversion by use of LSB ABI codes

Bit-weight errors in serial D/A converters using SFG devices are significantly reduced by introducing a LSB ABI mode of operation. This provides higher accuracy, increased effective radix or improved INL/DNL measures. The negative gain of SFG inverters is exploited for negative feedback in the converter. In each cycle the error of the previous iteration is subtracted due to the negative feedback. The successive generation of binary weights is preserved by introducing alternate bit inversion (ABI) input codes. The effectiveness of the algorithm is demonstrated by simulations in Cadence Spectre and by implementation on a chip. Analog SFG devices have non-linear gain and propagate level-noise. This makes the introduction of an error cancellation scheme in cyclic algorithms particularly important.

Implementation and analysis of converter linearity in LSB and LSB ABI serial D/A converters using semi floating-gate devices
The proposed SFG serial D/A converters using LSB or LSB ABI digital input codes were selected for implementation in CMOS. The multiple-valued output voltage levels are extracted from the measurements and analyzed in Matlab using standard D/A converter performance measures.

The use of difference equations to model serial D/A converter operation
The serial D/A converter algorithms are mathematically equivalent to the traditional parallel binary weight D/A converter. A set of difference equations modeling the converter operation is derived.

Increased speed in semi floating-gate circuits by use of Dual Data-Rate (DDR) operation
The speed of serial D/A conversion using semi floating-gate is significantly improved using DDR mode of operation. It is demonstrated that the maximum bit-rates are doubled using the proposed mode of operation. A traditional SDR SFG performs only one operation per recharge clock cycle. The proposed DDR mode of operation allows latching twice per recharge clock cycle, one on each of the clock edges.

A configurable serial D/A converter architecture
A complete architecture for configurable serial D/A conversion is provided. This includes a SFG MV FDIV for generation of the external reset clock signal, a SFG S/H read-out circuit, a modular level restoration circuit for removal of level-noise in multiple-valued input signals and serial D/A converter cores. Practical implementations are provided for all components except the SFG MV FDIV.

1.4   Thesis outline

Chapter 2 presents the fundamentals of cyclic D/A conversion. Simple difference equations modeling the operation are derived from the well-known algorithm for parallel binary weighted D/A conversion.

In chapter 3 the fundamentals of D/A conversion and static D/A converter performance measures are presented. This founds the basis of later linear analysis in chapter 4.

D/A converter circuits using SFG devices are proposed in chapter 4. An analysis and discussion of performance in terms of linearity and compact design is given. The main focus is on LSB and LSB ABI digital input codes. Measured results on practical chip implementations are provided for three converter candidates using LSB codes and one LSB ABI based converter

candidate. A comparison with related work on cyclic D/A conversion is given. The fifth D/A converter using MSB-first digital input codes is evaluated using simulation results from Cadence Spectre.

Circuits auxiliary to the D/A converter core are presented in chapter 5. This includes a SFG S/H Read-out circuit, a SFG MV FDIV with configurable radix and a SFG Ternary refresh circuit. Measured results on a chip implementation of the SFG S/H Read-in and Read-out circuits are provided. Additional measured chip results for the ternary switching element (Paper VIII) are provided.

Chapter 6 summarizes this thesis and gives proposals for further work.

Eight publications [38, 39, 40, 41, 42, 43, 44, 45] are selected for presentation in this thesis and are attached in chapter 7 as **[Papers I-VIII]**. All eight publications have been accepted and presented at international conferences with peer review. The articles are published in conference proceedings. These papers have been created and written as part of this Ph.D. thesis.

1.5 Summary of publications

In [38]**[Paper I]** configurable serial D/A conversion using SFG devices is introduced. It is shown how the ideal serial D/A converter model is mathematically equivalent to the well-known parallel binary weight D/A converter algorithm. A practical implementation using SFG devices requires sufficient accuracy in the SFG based adder and memory. A simple serial D/A converter using semi floating-gate devices is implemented on a 0.35um AMS chip. Cadence Spectre is used for tuning of parameters and preliminary simulation results. This paper focuses on the feasibility of configurable serial D/A conversion using SFG devices. The importance of accurate and linear SFG device operation is emphasized. In particular that of the included SFG Latch. The paper presents simulation results demonstrating sufficient accuracy of SFG devices to solve the serial D/A converter difference equation. Additional chip measured results are provided in this thesis in chapter 4.2. The converter supports standard least significant bit (LSB) first digital input codes. The proposed D/A converter is referred to as DAC-1.

Based on the experience from DAC-1, several techniques for increasing the effective radix are introduced. The effective radix or linearity is discussed and studied using standard static D/A converter performance measures.

[39]**[Paper II]** introduces a LSB alternate bit inversion (LSB ABI) error cancellation scheme for increased converter accuracy and effective radix. In each cycle the error of the previous iteration is subtracted due to the negative feedback. The successive generation of binary weights is preserved by

introducing alternate bit inversion (ABI) input codes. This allows the effect of symmetrical non-linear gain error in the SFG inverter transfer function to be compensated. The new peak error could be within one LSB for multiple-valued radices 2, 3 and 4. The proposed LSB ABI serial D/A converter is implemented on a chip and simulation results from Cadence Spectre are discussed and analyzed. Additional chip measured results are provided in chapter 4.3 of this thesis. The converter supports LSB ABI digital input codes and is referred to as DAC-2.

[40][**Paper III**] addresses problems associated with the existing SFG Latch based memory. Three practical converter applications are discussed; utilization as internal memory, as read-in circuit and as read-out circuit. Improved SFG S/H Read-in and Read-out circuits are introduced. A practical implementation on a chip demonstrates the concept. The linearity of the SFG S/H circuits is discussed and studied.

By integrating the SFG S/H memory proposed in [40][**Paper III**] into DAC-1 proposed in [38][**Paper I**], new converters with both improved linearity and reduced device count are made possible.

In [41][**Paper IV**] a new configurable serial D/A converter using SFG devices is introduced. This concept exploits SFG S/H circuits for improved linearity and reduced device count. It is referred to as DAC-3. A practical chip implementation is performed and chip measured results are provided.

[42][**Paper V**] addresses the troubling slow speed associated with all cyclic serial D/A converters. A new mode of operation referred to as Dual Data-Rate (DDR) is introduced. It allows a doubling of the conversion rate by utilizing both clock edges. The new mode of operation exploits SFG S/H circuits for improved linearity and reduced device count. In this paper a new configurable serial D/A converter referred to as DAC-4 is introduced. The converter implements DDR DAC operation. A practical implementation on a chip and chip measured results are provided. The results are discussed and studied in terms of converter linearity.

[43][**Paper VI**] presents a new serial D/A converter with support for standard MSB-first digital input codes. This alternative uses SFG devices and supports runtime reconfiguration of its radix. The converter is referred to as DAC-5.

In [44][**Paper VII**] an N-ary multiple-valued Frequency Divider (MV FDIV) using SFG devices is introduced. The proposal is applicable as a configurable bit counter in cyclic D/A converters. Simulation results demonstrate usage as reset clock signal generator in a SFG serial D/A converter. The MV FDIV circuit is compared with a digital bit-counter in terms of device count and functionality.

[45][**Paper VIII**] proposes a ternary switching element using SFG devices.

A practical implementation on a chip is done and simulation results are discussed. Additional chip measured results are provided in chapter 5.4 of this thesis.

Chapter 2

SERIAL D/A CONVERSION

In this chapter mathematical models for discussion of [38, 39, 41, 42, 43]**[Papers I, II, IV, V and VI]** are presented.

2.1 Introduction

In this thesis semi floating-gate devices for binary to multiple-valued conversion are introduced. A focus on compact and configurable SFG MVL devices motivates the use of cyclic D/A conversion algorithms. The proposed LSB-First SFG cyclic D/A converter allows on-chip conversion in a standard CMOS process.

In modern computers the digital (binary) number system is a base two system. The digits of this binary number system are referred to as bit and each position is associated with a binary weight, a power of two. D/A conversion is a multiplication problem in which the product of bits and their weights are added. An illustration is given in table 2.1 where weights (W), binary number (B) and normalized weights $(W/2^n)$ are included. It is common to denote the leftmost bit with the highest weight as the most significant bit (MSB). The rightmost bit of the lowest weight is the least significant bit (LSB).

B	b_n	...	b_i	...	b_2	b_1
W	2^{n-1}	...	2^{i-1}	...	2^1	2^0
$W/2^n$	2^{-1}	...	$2^{-(n+1-i)}$	...	$2^{-(n-1)}$	2^{-n}

Table 2.1: *The binary number system and its binary weights. Calculating the decimal values of a binary number is equal to a multiplication problem.*

A good overview of D/A converter architectures which focus on bit-serial and cyclic D/A conversion was given by J.W. Bruce in [46]. A bit-serial D/A converter is characterized by its bit-wise conversion of a digital input. Serial D/A converters are in general constructed with much simpler circuits than their bit-parallel counterparts. However, the speed of the serial D/A converter algorithm decreases linearly with the number of bit resolution. It is therefore associated with moderate speed at low resolutions (2-4 bit) and slow speed at high resolutions (10 or more bit). In a N bit cyclic D/A converter the result of each bit conversion is added to the result of the previous bits converted. After all N bit are clocked in, the accumulated result is at the analog output. It can easily be stored using a sample and hold circuit [47]. Because of their iterative nature the cyclic D/A converters are not only extremely compact, but also support a range of resolutions. D/A conversion is defined as a process of transforming a binary number B into an analog value Y given by

$$Y_n = \sum_{i=1}^{n} 2^{-i} b_i \ , \tag{2.1}$$

where the digital input B is the ordered set of bit $(b_1, b_2, \ ... \ , b_n)$. A cyclic D/A converter solves this process by using a first order difference equation generating the same sum. Traditional and better known bit-parallel binary weighted D/A converters solves it in one big parallel computation. It therefore outperforms bit-serial or cyclic D/A converters in speed, but provides only a fixed resolution. The design is however modular.

Three types of converters are covered. The LSB-First (LSB), LSB-First with Alternate Bit Inversion (LSB ABI) and the MSB-First cyclic D/A converter. These converter algorithms will be referred to as LSB, LSB ABI and MSB type respectively.

2.2 LSB-first D/A Conversion
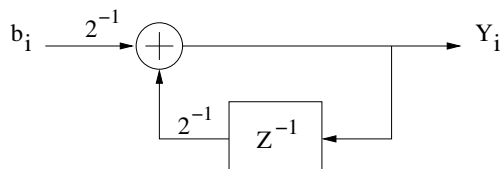

Figure 2.1: *Typical signal flow digram of LSB first type cyclic D/A converters.*

The LSB-First type cyclic D/A converter operation is modeled by the first

order linear difference equation

$$Y_i = \frac{1}{2}\left(Y_{i-1} + b_i\right) \tag{2.2}$$

with initial condition $Y_0 = 0$ and n iterations $i = 1, .., n$. One iteration for each bit resolution. The input is ordered with the least significant bit (LSB) b_1 first, and the most significant bit (MSB) b_n last. This gives input codes of the form

$$B = (b_1, b_2, \ ... \ , b_i, \ ... \ , b_n) \ . \tag{2.3}$$

After all n bits are clocked into the converter, the corresponding analog value

$$Y_n = \sum_{i=1}^{n} 2^{-i} b_i \tag{2.4}$$

results at the output. Equation 2.4 shows that a n-bit LSB-first digital code is converted into an analog value Y_n in the range from 0 to 1 . In figure 2.1 a signal flow diagram of the LSB first type cyclic D/A converter is shown.

2.3   LSB-first ABI D/A Conversion
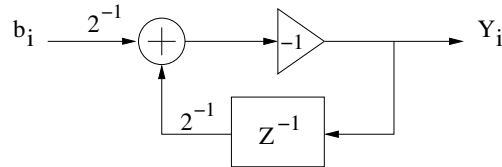
Figure 2.2: *Typical signal flow diagram of LSB ABI type cyclic D/A converters.*

A LSB-First Alternate Bit Inversion type cyclic D/A converter is a special case of the standard LSB-First type D/A converter. Alternate bit inversion (ABI) of intermediate analog values and digital input codes is utilized. This means that the intermediate analog voltage Y_i is inverted once per iteration. The inversion process works as a negative feedback subtracting non-linear errors of the previous iteration. A signal flow diagram of the LSB first type cyclic D/A converter is shown in figure 2.2. The algorithm will be referred to as LSB ABI conversion and is modeled by the equation

$$Y_i = 1 - \frac{1}{2}\left[Y_{i-1} + b_i'\right] \tag{2.5}$$

where $Y_0 = 0$ and n an integer $n >= 2$. The index i takes the values $i = 1, .., n$. A LSB ABI converter differs from a LSB converter by utilizing

alternate inversion of the binary input. When converting from a LSB to a LSB ABI code (B'), every second bit is inverted. If the length of the digital input code is an odd number, the inversion starts with the first bit. Otherwise inversion starts at the second bit.

$$
\begin{aligned}
B' = (b'_1, b'_2, \ ... \ , b'_n) \ &= (\overline{b_1}, b_2, \overline{b_3}, \ ... \ , \overline{b_n}), \quad n = odd \\
&= (b_1, \overline{b_2}, b_3, \ ... \ , \overline{b_n}), \quad n = even
\end{aligned}
\tag{2.6}
$$

The LSB ABI converter is particularly interesting in a SFG inverter implementation context. A SFG inverter is an analog device which propagates noise. It also has finite gain and parasitic effects which result in an error being added in each iteration. The LSB ABI conversion algorithm has the ability to reduce the effect of SFG inverter computation errors and improve overall linearity. After all n bits are clocked into the converter, the corresponding analog value

$$
\begin{aligned}
Y_n &= \quad \textstyle\sum_{i=1}^{n} 2^{-i} b_i, \qquad n = even \\
&= \ 2^{-n} + \textstyle\sum_{i=1}^{n} 2^{-i} b_i, \quad n = odd
\end{aligned}
\tag{2.7}
$$

has been generated. It was mentioned earlier that SFG inverters propagate noise. The devices are inherently analog and not level restoring. In the LSB-First cyclic D/A algorithm each iteration includes a divide-by-two of the previous intermediate result. This reduces the amount of level-noise or level-error propagated by a factor of $1/2$ and is often said to assure that the error lies within the least significant bit. Further, it is assumed that the error contributed or generated by SFG inverter computations is symmetrical around $V_{dd}/2$ and is of opposite signs. By using a LSB ABI algorithm the intermediate result tends to shift between the two regions of operation. The sign of the error contribution shifts with it. An error cancellation effect occurs. All-zero or all-ones codes benefit the most from this technique.

The overall conversion error when using LSB converters and analog SFG inverters can be estimated as

$$
E = \sum_{i=1}^{n} 2^{-(i-1)} e_i
\tag{2.8}
$$

Here, e_i denotes the error contributed by the i-th iteration. A LSB ABI algorithm is proposed, where the error of each iteration is subtracted in the next iteration. This reduces the accumulated error to

$$
E = \sum_{i=1}^{n} (-1)^{(n+i+1)} 2^{-(i-1)} e_i
\tag{2.9}
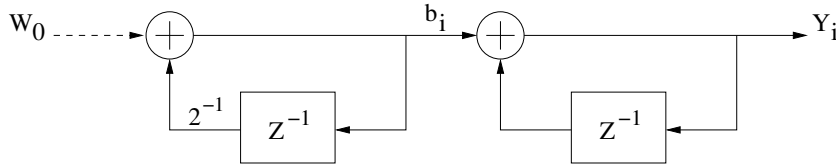$$

2.4   MSB-first D/A Conversion

Figure 2.3: *Typical signal flow diagram of MSB-First type cyclic D/A converters.*

In the MSB-First type cyclic D/A converter each iteration can be expressed as

$$Y_i = Y_{i-1} + 2^{n+1-i}b_{n+1-i} \tag{2.10}$$

where $Y_0 = 0$ and n iterations $i = 1, .., n$. The converter reads bit-serial codes

$$B = (b_n, b_{n-1}, \ ... \ , b_{n+1-i}, \ ... \ , b_1) \ , \tag{2.11}$$

ordered from MSB to LSB. The converter can easily be implemented using an accumulator and a divide-by-two counter. The accumulator provides memory between each iteration and the counter generates the binary weights. The digital input determines which weights are added to the intermediate result. After all n bits are clocked in, the analog value

$$Y_n = \sum_{i=1}^{n} 2^{n+1-i}b_{n+1-i} \tag{2.12}$$

is at the output. A weakness of this construction is that the most significant bit is read first in time. It is read and stored from analog memory n-1 times. This is n-1 times more than when using the LSB and LSB ABI algorithms presented earlier. This allows for a much higher error contribution in physical implementation. Although expected to be less accurate than a LSB-first converter, it is included for completeness and comparison. In figure 2.3 a typical signal flow diagram of the MSB-First type cyclic D/A converter is included.

It can be shown that the MSB, LSB and LSB ABI type converters all express the same normalized values. One exception is the LSB ABI type converter configured with an odd number of bit resolution. Its analog output is offset by 2^{-n} as indicated earlier. The converters span

$$Y_{range} = (Y_{max} - Y_{min}) = \frac{2^n - 1}{2^n} \tag{2.13}$$

portions of the full scale. The cyclic D/A converter algorithms can also be derived from the well-known and popular parallel binary weight D/A converter algorithm in equation 2.14.

$$
\begin{aligned}
Y_n &= \sum_{i=1}^{n} 2^{-i} b_{n+1-i} \\
&= 2^{-1}b_n + 2^{-2}b_{n-1} + \ ... \ + 2^{-i}b_{n+1-i} + \ ... \ + 2^{-n}b_1 \\
&= 2^{-n}\left(2^{n-1}b_n + \ ... \ + 2^{i-1}b_i + \ ... \ + 2^{0}b_1\right)
\end{aligned}
\tag{2.14}
$$

An alternative converter algorithm for MSB-first D/A conversion exists. By exploiting a multiply-by-two feedback the conversion process can be made less complex. However multiply-by-two calculations were considered less practical in a SFG context.

2.5 Summary

Fundamental background on configurable serial D/A converter algorithms has been presented. This includes signal flow diagram, difference equations and digital codes for least significant bit (LSB) first, least significant bit first with alternate bit inversion (LSB ABI) and most significant bit (MSB) first conversion.

For further background on serial D/A conversion readers are referred to [46]. The popular D/A converter textbooks include little or no information on cyclic D/A conversion in their surveys on D/A converter architectures [48] [49] [50] [51]. [52] by P. E. Allen covers switched-capacitor circuits and mentions cyclic D/A conversion. The article [53] covers various converter architectures and includes discussion of parameters, limitations and applications for serial cyclic D/A conversion. A brief description is also included in a textbook on CMOS circuits by Jacob Baker [54]. However, [54] covers only cyclic D/A converters using LSB-First bit-serial codes. In [55] professor A. Baschirotto gives a lecture on data converters and interfacing. The talk gives a good introduction to both cyclic MSB-first and LSB-first D/A converters. In [55] cyclic D/A conversion is referred to as serial D/A conversion, a process which generates the analog voltage serially bit by bit. The algorithms are grouped into active multiplication by two, passive multiplication by two and active division by two. Operational transconductance amplifiers are utilized as active component. Cyclic D/A conversion is also referred to as algorithmic D/A conversion. Original work on cyclic D/A converters are presented in [28],[29],[36],[35] and [32].

Chapter 3

D/A CONVERTER PERFORMANCE

In this chapter background information on notation and methods for analysis of SFG serial D/A converters is introduced. The material presented forms the basis of later performance characterization for practical implementations in chapter 4.

3.1   Introduction

This thesis introduces new D/A converter circuits utilizing compact analog SFG devices. The ideal operation is described using linear first order difference equations. Linear analog SFG based memory and SFG device transfer functions become a main concern. These non-linearities are analyzed using standard static D/A converter performance measures. SFG devices are compact circuits with a high functional capacity per device. However, the devices are analog and provide no form of level correction. Digital (binary) logic suppress level-noise and provide noise margins. A SFG device is inherently analog. In addition to propagating level-noise, the non-linear transfer functions and mismatch errors degrade performance of converters using SFG devices. This makes quantification of static distortion using standard metrics important.

3.2   Ideal D/A Conversion

In MVL applications using semi floating gate (SFG) inverters, we are primarily interested in encoding multiple valued signals of radix 4, 8 and 16. This means between two and four bit D/A converter resolution. In tables 3.1, 3.2

and 3.3 examples of LSB, MSB and LSB ABI codes of these resolutions are given as a summary of the three converter types presented.

The cyclic D/A converter algorithms are visualized by combining the digital test data from the three tables below and the LSB, LSB ABI and MSB algorithms in equations 2.4, 2.7 and 2.12. The resulting analog values are shown in figure 3.1. Both cyclic D/A algorithms and bit-parallel D/A converter algorithms presented map to the same points. The exception is the LSB ABI type converter with odd number of bit resolution. Its analog value is offset by 2^{-n} when in this configuration. A positive offset of $1/8$ when using the three bit codes corresponds to the unused portion of the output range.

MV	MSB		LSB		LSB ABI	
R=4	b_2	b_1	b_1	b_2	b_1	$\overline{b_2}$
0	0	0	0	0	0	1
1	0	1	1	0	1	1
2	1	0	0	1	0	0
3	1	1	1	1	1	0

Table 3.1: *LSB, LSB ABI and MSB digital input codes for radix four.*

MV	MSB			LSB			LSB ABI		
R=8	b_3	b_2	b_1	b_1	b_2	b_3	$\overline{b_1}$	b_2	$\overline{b_3}$
0	0	0	0	0	0	0	1	0	1
1	0	0	1	1	0	0	0	0	1
2	0	1	0	0	1	0	1	1	1
3	0	1	1	1	1	0	0	1	1
4	1	0	0	0	0	1	1	0	0
5	1	0	1	1	0	1	0	0	0
6	1	1	0	0	1	1	1	1	0
7	1	1	1	1	1	1	0	1	0

Table 3.2: *LSB, LSB ABI and MSB digital input codes for radix eight.*

3.3 Static D/A Converter performance measures

In this work low freqency MVL encoders are our main interest. INL and DNL are expected to give a good indication of the converter performance. This assumes operation within the limits of the building blocks. In SFG

MV	MSB				LSB				LSB ABI			
R=16	b_4	b_3	b_2	b_1	b_1	b_2	b_3	b_4	b_1	$\overline{b_2}$	b_3	$\overline{b_4}$
0	0	0	0	0	0	0	0	0	0	1	0	1
1	0	0	0	1	1	0	0	0	1	1	0	1
2	0	0	1	0	0	1	0	0	0	0	0	1
3	0	0	1	1	1	1	0	0	1	0	0	1
4	0	1	0	0	0	0	1	0	0	1	1	1
5	0	1	0	1	1	0	1	0	1	1	1	1
6	0	1	1	0	0	1	1	0	0	0	1	1
7	0	1	1	1	1	1	1	0	1	0	1	1
8	1	0	0	0	0	0	0	1	0	1	0	0
9	1	0	0	1	1	0	0	1	1	1	0	0
10	1	0	1	0	0	1	0	1	0	0	0	0
11	1	0	1	1	1	1	0	1	1	0	0	0
12	1	1	0	0	0	0	1	1	0	1	1	0
13	1	1	0	1	1	0	1	1	1	1	1	0
14	1	1	1	0	0	1	1	1	0	0	1	0
15	1	1	1	1	1	1	1	1	1	0	1	0

Table 3.3: *LSB, LSB ABI and MSB digital input codes for radix sixteen.*
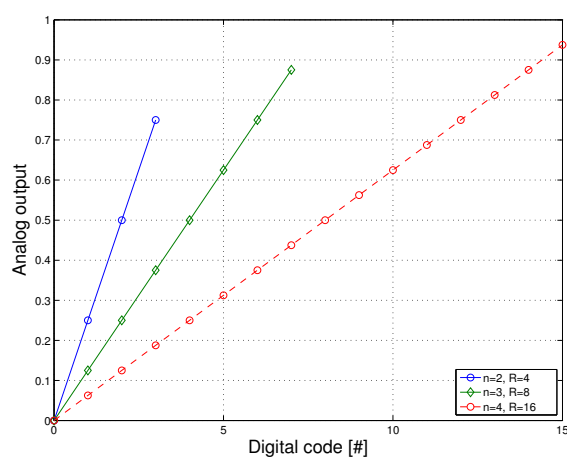
Figure 3.1: *Ideal transfer characteristic of a monotonic D/A converter. The three radices of interest, radix four, eight and sixteen, are illustrated.*

Inverters[20] the refresh rate is required to be below a certain frequency. Otherwise both leakage and refresh rate will affect performance.

A sweep of all digital input codes X is used as a test, producing the staircase transfer function shown in figure 3.2. The static performance measures are given by the converter deviation between the experimental output voltage levels and the ideal staircase transfer function of uniform steps. The set of ordered digital input codes used are denoted

$$X = (X_0, X_1, \ ... \ , X_{2^n-1}) \tag{3.1}$$

where X_0 normally is the all-zero code and X_{2^n-1} is the all-ones code. The codes are ordered ascending by their converter output voltages. In an ideal converter the distance between the output values of two adjacent input codes is $1LSB$. The LSB voltage is 2^{-n} of the full scale output swing V_{FS}.

The experimental output values Y_{real} and the ideal theoretical values Y deviate by an error

$$d_i = Y_{real}(X_i) - Y(X_i) \tag{3.2}$$

A set of standard static measures for characterization of D/A converters exists which can be grouped into linear and non-linear errors. In this thesis the focus is on linear errors such as gain and offset errors, and non-linear measures such as differential non-linearity (DNL) and integral non-linearity (INL) errors.
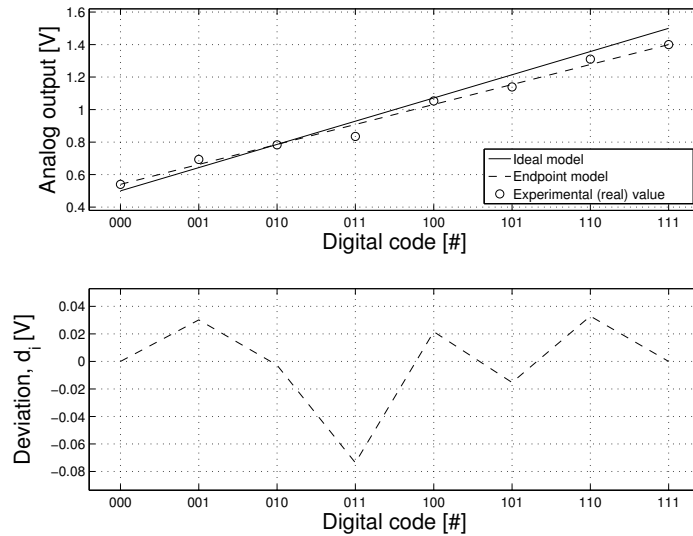
Figure 3.2: *Example of transfer characteristic and deviation measures of a D/A converter using three bit resolution.*

The gain is calculated using

$$A = \left[Y_{real} \left(X_{2^n-1} \right) - Y_{real} \left(X_0 \right) \right] / \left[Y \left(X_{2^n-1} \right) - Y \left(X_0 \right) \right] \tag{3.3}$$

Offset errors are the difference between experimental and ideal output voltages when using an all-zero input code X_0. All the digital codes in the transfer characteristic are offset by this value;

$$Y_{offset} = Y_{real} \left(X_0 \right) - Y \left(X_0 \right) = d_0 \tag{3.4}$$

The non-linear measures are often calculated after compensating for gain and offset errors. Experimental output values are compared with a straight line Y' going through its end-points $Y_{real} \left(X_0 \right)$ and $Y_{real} \left(X_{2^n-1} \right)$.

Differential non-linearity (DNL) is the maximum deviation in the output step sizes from the ideal values of one least significant bit (LSB). It can also be expressed as the change in deviation between to adjacent codes X_i and X_{i-1};

$$D_i = d_i - d_{i-1} \tag{3.5}$$

An increasing DNL indicates an increasing deviation from the ideal converter characteristics. The ideal DNL is $D_i = 0$ for all adjacent ordered code transitions. This gives an monotonic increasing transfer characteristic and an uniform distribution of the converter output voltage levels over the output voltage swing, V_{FS}. A DNL less than $\pm 1 LSB$ indicates a monotonic transfer characteristic.

The integral non-linearity (INL) describes the overall or maximum deviation from a wanted straight line. Before determining the INL it is common to compensate for the gain error and offset which are both linear components. The ideal converter model is adjusted using the end-point values $Y_{real} \left(X_0 \right)$ and $Y_{real} \left(X_{2^n-1} \right)$ of the experimental result. This form of INL is called end-point INL. It is defined as

$$I_i = \sum_{k=1}^{i} D_k = \left(d_i - d_0 \right) / V_{LSB} \tag{3.6}$$

An INL less than 0.5 LSB is analog with a monotonic D/A converter output [49].

In addition the converter resolution is often stated. It is given by the number of bits in the input code, n. It is also common to refer to the number of distinct analog output voltage levels, the radix R, of the converter. In binary weighted converters the radix of the analog output voltage is $R = 2^n$. A third option is to give the accuracy in voltage, often relative to the LSB-voltage V_{LSB}.

3.4   Summary

This chapter provides background for analysis of serial D/A converters using SFG devices. The standard non-linear static D/A converter performance measures, integral non-linearity (INL) and differential non-linearity (DNL), are introduced as figures of merit (FoM).

Further information on static D/A converter measures can be found in [48] [49][50][56]. Hoeschele [48] and Razavi [49] define analysis methods and provide popular reference material.

Chapter 4

SEMI FLOATING-GATE SERIAL D/A CONVERSION

This chapter summarizes the proposed new Semi Floating-Gate (SFG) serial D/A converters published in [38, 39, 41, 42, 43]**[Papers I, II, IV, V and VI]**. The converters are presented and discussed. In addition, previously unpublished measurements of practical chip implementations are included. A total of five new converter implementations using SFG inverters are presented.

The converters are presented in chronological order and referred to as DAC-1,.. ,DAC-5. The work covers Least Significant Bit-First (LSB), Least Significant Bit-First with Alternate Bit Inversion (LSB-ABI) and Most Significant Bit-First (MSB) type serial D/A conversion. Also, the algorithms can be described by the number of iterations per recharge clock cycle; Single Data-Rate (SDR) when using one iteration per recharge clock cycle and Dual Data-Rate (DDR) when using two. A measure of linearity is found using standard D/A converter measures as described in chapter 3. Finally, a summary of the converter linearity as a function of resolution and converter implementations is provided at the end of this chapter.

4.1 Introduction

In this chapter practical implementations of serial D/A converters using semi floating-gate (SFG) devices are presented. The proposed circuits exploit semi floating-gate inverters for a compact and configurable design. In [20] Berg *et al.* introduce the semi floating-gate (SFG) inverter for Multiple-Valued Logic (MVL) purposes. The inverter is a volatile multiple-input Multiple-Valued inverter recharged periodically by a recharge clock signal. Several techniques have been proposed for making this recharge clock surplus. Halvorsrød *et*

al. [57] propose an active floating-gate inverter. The leakage current of reverse powered diodes are utilized to create high impedance conductances between the floating-gate and two bias voltages. Another technique is pseudo floating-gate [58] which makes use of resistors for control of the floating-gate voltage. A different approach is to exploit the recharge switches for increased functional capacity per device. In [19] Mirmotahari *et al.* introduce a SFG Latch structure consisting of only two SFG inverters in series. The technique requires two perfectly matched and non-overlapping complementary clock signals.

Binary to multiple-valued radix converters using SFG devices have traditionally been implemented using bit-parallel D/A converter algorithms. In this thesis, work on new configurable serial D/A converters is presented. A total of five novel SFG based cyclic D/A converters are proposed. The converters out-perform the bit-parallel ones in terms of small die area requirement and ability to adapt through re-configuration. In this thesis, it is assumed that digital data are communicated bit-serially between the surrounding binary world and the multiple valued logic circuit. A cyclic D/A converter then offers a significant reduction in die area compared to bit-parallel D/A based MVL encoders. The latter requires an additional serial to parallel conversion for solving the problem of serial D/A conversion. These serial to parallel converters are typically implemented using a shift-register.

The functionality of the cyclic D/A converters is demonstrated through simulations in Cadence Spectre, chip measurements and study of D/A converter linearity. Two encoder properties are of primary concern; noise margins and monotonicity. Optimal noise margins are synonymous with equal spacing between the output values. This makes it important to characterize the linearity of the converters through simulations.

The construction of SFG based cyclic D/A converters is an interesting and challenging task for several reasons. First of all, a high precision SFG based memory is required. Offset, gain and linearity errors will have a huge impact on the overall performance. Second, the SFG memory will require that a multi-phase clocking strategy is selected. Modern designs tend to minimize the number of clock phases used. In this work two-phase clock signals are chosen as they allow a more compact memory, and thus more compact converters to be built. A problem with this choice is that it requires the clock signals to be perfectly matched, complementary and non-overlapping [19]. A third challenge is the analog nature of SFG inverters. The inverters are inherently level-noise propagating, which can make SFG based cyclic D/A conversion challenging. Its finite gain imposes further deviation from the ideal converter output values.

4.2   SDR LSB D/A Converter (DAC-1)
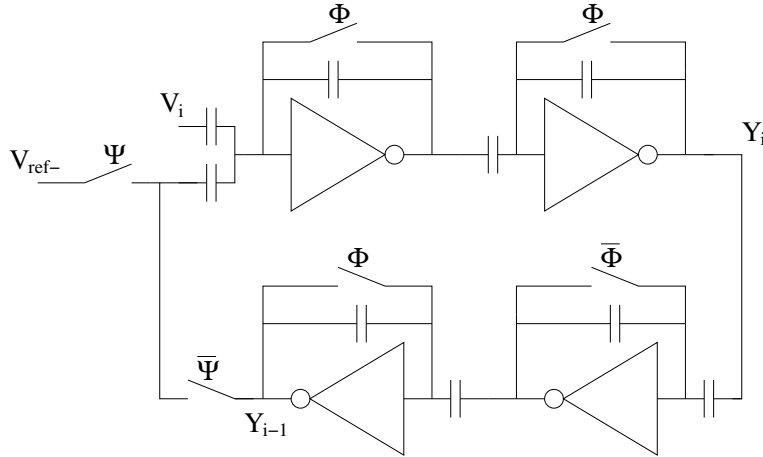
Figure 4.1: *Schematic diagram for DAC-1. Digital input voltage V_i, recharge signal Φ, reset signal Ψ and analog output voltage Y_i are shown.*

The circuit presented in figure 4.1 [38][**Paper I**] and described in equation 2.2 will be referred to as DAC-1. It implements LSB-First type D/A conversion. To the knowledge of the author, this converter is the first attempt to implement cyclic D/A conversion using SFG inverters. A two-phase clocking strategy referred to as "recharge and evaluation" is chosen. This requires perfect matching of the two complementary and non-overlapping clock signals Φ and $\overline{\Phi}$. The circuit consists of two logical components; a two-input SFG Adder and a SFG Latch.

The SFG Latch is the analog memory of the converter. It is required for storing the intermediate result between each iteration. The two one-input inverters with opposite clock signals (latch configuration) form the SFG Latch[19] capable of storing the analog values. A latching clock scheme gives unity gain in each inverter and a delay of half a clock period. The latch provides a one clock period delay as required by the cyclic D/A converter algorithm.

One iteration is computed per cycle using the SFG Adder. The $(n-1)$ first computations therefore involve four SFG inverter computations each. In the n-th cycle only two computations take place. This gives a total of $4(n-1)+2$ analog SFG inverter computations. SFG inverters operated in "recharge and evaluation" mode have gain -1. A second one-input inverter is connected in series to compensate for the negative gain. The two inverters form a two-input SFG Adder. In order to solve the difference equation in 2.2, linear operation and binary weights are required. A standard two-input SFG Adder is sufficient. First, the two input capacitors are chosen equally large. Second, in order to assert unity gain, the feedback capacitors and the sum of

the input capacitors are matched by layout simulation in Cadence Spectre. The weighted sum then equals the divide-by-two operation found in the LSB-First cyclic D/A algorithm (equation 2.2) of DAC-1. Note, according to simulations the parasitic capacitances are much smaller than the wanted capacitances. This reduces the effect of device variation (mismatch). Gate capacitance is dependent on V_{gs} and V_{ds}. In our circuits the effect of these gate-capacitance variations are smaller than in a single $pMOS$ or $nMOS$ transistor. The $pMOS$ and $nMOS$ sides will to some extent cancel each other out.

Analog SFG inverters have finite gain and it is necessary to limit their operation to an interval of voltages between V^- and V^+. In this study experiments are performed using $V^- = 0.5V$ and $V^+ = 1.5V$ due to increased non-linearity close to the rails. This gives a converter with a reduced output voltage swing; from $V_{dd} = 2V$ to $(V^+ - V^-)$. All input signals (except clock signals) are offset by V^-. The bit-serial digital input B_i needs to be encoded V^- when "0" and V^+ when "1".

A non-overlapping two phase clock Φ and a perfectly matched complementary clock $\overline{\Phi}$ drive the converter. The two phases $\Phi = 0$ and $\Phi = 1$ are referred to as the "evaluation" and "recharge" period respectively. During the "evaluation" period the digital input B_i is read and one iteration is computed by the SFG Adder. While in this mode the semi floating-gate of the SFG Latch is also recharged. In the "recharge" period the result of previous bits is latched into and stored in the SFG Latch. While in this memory phase, all other nodes are recharged using $V_{in} = V_{out} = V_{SFG} = V_{dd}/2$.

The converter is initialized by disconnecting the SFG Latch output voltage from the SFG Adder and replacing it with the all-zero code voltage $Y_0 = Y^- = 0.5V$.

Measured DAC-1 operation is illustrated in figure 4.2, figure 4.3 and figure 4.4. In the first illustration, figure 4.2, there are four traces. The first trace shows a radix four analog output voltage sampled from node Y_i. Trace two is a train of bit-serial input codes. This code sequence generates a staircase at the output node in trace one. Trace three is the reset clock applied in node Ψ. The last trace shows the recharge-clock (bit-clock) signal Φ. In the second and the third illustration the reset signal Ψ is omitted. This gives more room for the output voltage as the resolution is increased to three bit in figure 4.3 and four bit in figure 4.4. An additional illustration of the converter operation is shown in figure 4.5. Here, the multiple-valued output voltage levels are circled out.
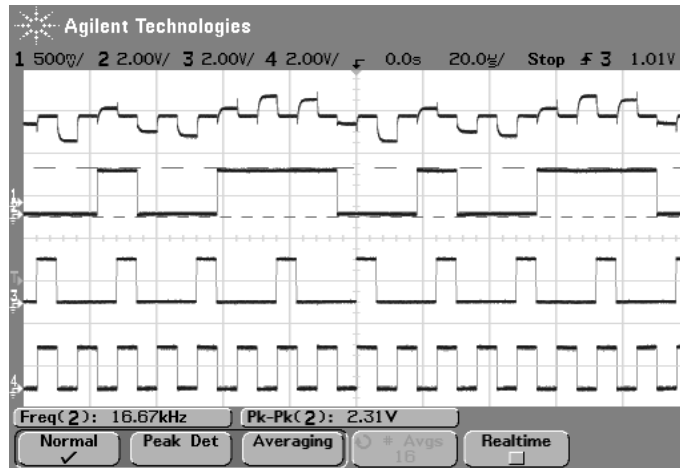
Figure 4.2: *Measured DAC-1 output voltages and timing of clock signals. Configured for radix R=4 using n=2, $f_\phi = 41.7kHz$, $f_\psi = 20.83kHz$. The four traces are; analog output voltage Y_i, bit-serial input code B_i, reset clock Ψ and bit-clock Φ.*
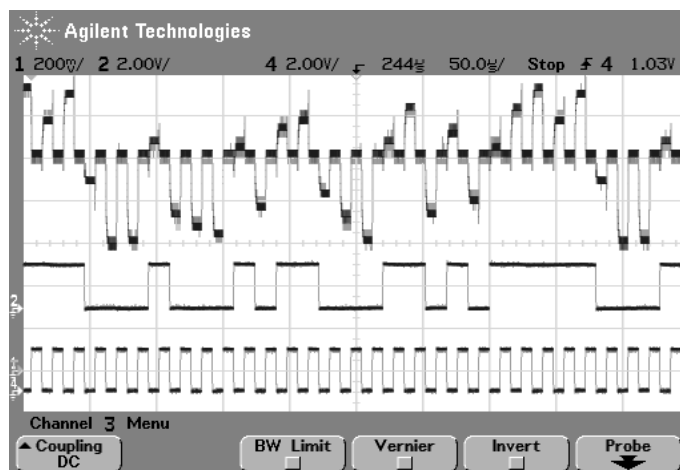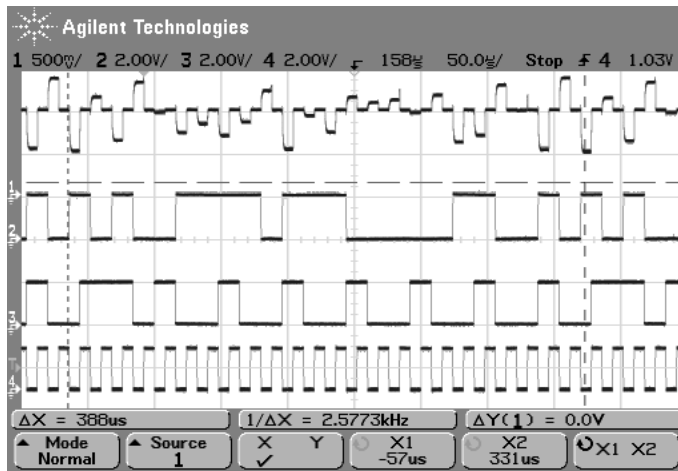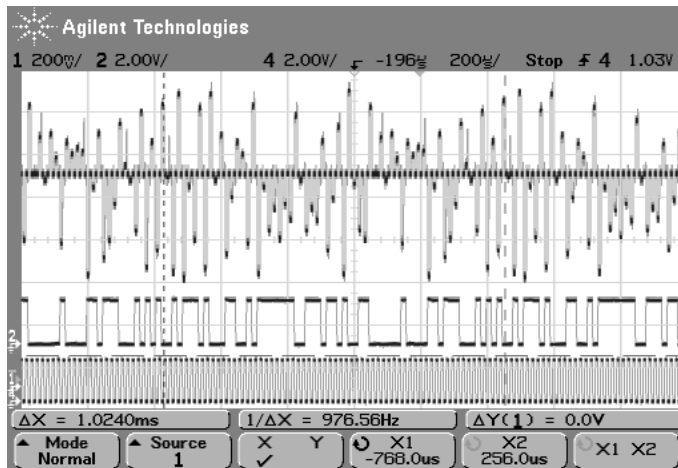

Figure 4.3: *Measured DAC-1 output voltages. Configured for radix R=8 using n=3, $f_\phi = 62.0kHz$, $f_\psi = 20.67kHz$. The three traces are; analog output voltage Y_i, bit-serial input code B_i and bit-clock Φ.*
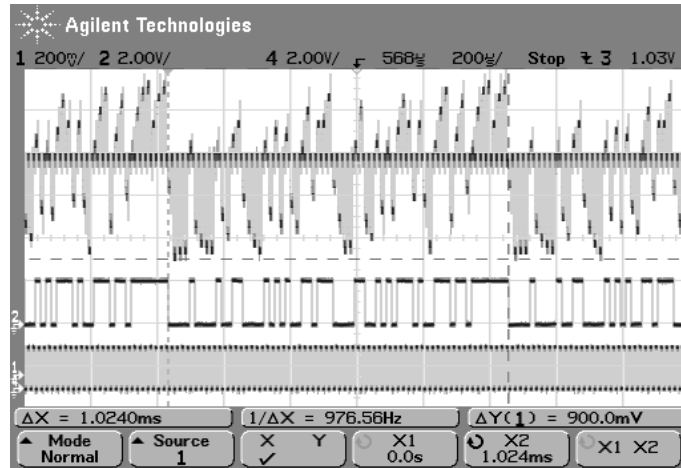
Figure 4.4: *Measured DAC-1 output voltages. Configured for radix R=16 using n=4, $f_\phi = 62.5kHz$, $f_\psi = 15.63kHz$. The three traces are; analog output voltage Y_i, bit-serial input code B_i and bit-clock Φ.*

Figure 4.5: *Illustration of LSB D/A conversion. Measurements using DAC-1 and three bit resolution are used as illustration data. The multiple-valued output voltage levels are circled out. Labels are included for the voltages representing the multiple-values (0-7) generated by the LSB-First input codes (000-111).*

4.3   SDR LSB ABI D/A Converter (DAC-2)

Figure 4.6: *Schematic diagram of DAC-2, a SFG inverter implementation of a LSB ABI type D/A converter algorithm. The digital input voltage V_i, recharge clock signal Φ, reset clock signal Ψ and analog output voltage Y_i are shown. The auto-zero circuit is built into the design using two switches.*

Figure 4.6 shows the SDR LSB ABI D/A Converter from [39][**Paper II**] called DAC-2. It implements the error correction algorithm referred to as LSB ABI presented in chapter 2.3 (equation 2.7). The proposed circuit is a modified version of DAC-1 [38][**Paper I**]. External input and output signals of DAC-1 and DAC-2 are mainly the same. Two global input signals, one for digital input codes b_i and one for the initial all-zero code voltage $Y_0 = Y^- = 0.5V$, are needed. The digital input b_i is recharged using two switches which allows the larger auto-zero circuit (AZC)[59] to be omitted. Removal of the AZC both eliminate a source of error and reduce power consumption. However, this requires the reset signal (Ψ) to be modified. The new reset clock signal has half the pulse-width of the original reset clock. There are two feedback wires. The upper wire interleaves the bit-serial input with a recharge voltage ($V_{dd}/2$). The lower wire provides a negative feedback of the intermediate analog output voltage Y_i.

Two sets of complementary clock signals synchronize the conversion process; bit-clock signals Φ and $\overline{\Phi}$, and reset clock signals Ψ and $\overline{\Psi}$. Again, both clock signals are required to be sets of perfectly matched, complementary and non-overlapping waveforms. The binary data are represented by a voltage of 0.5V for zeros and 1.5V for ones. The conversion process for DAC-2 requires three SFG inverter computations the first n-1 cycles, and only one computation the n-th (final) round. A total of $3(n-1)+1$ SFG inverter computations are involved, which is $(n-1)$ less computations than when using the circuit DAC-1.

There are mainly two goals for proposing the new circuit, DAC-2. First, the number of analog SFG inverter based computations per cycle is a limited resource. Compared to DAC-1 [38][**Paper I**], one inverter is omitted in the two-input SFG adder component. This gives a more compact LSB ABI type cyclic D/A converter and reduces the die area of practical implementations. In addition, each SFG inverter operation degrades the multiple-valued signal and propagates level-noise without any form of level correction. By omitting one SFG inverter, the overall converter linearity is improved. In figure 4.7 the SFG inverter transfer function is illustrated.
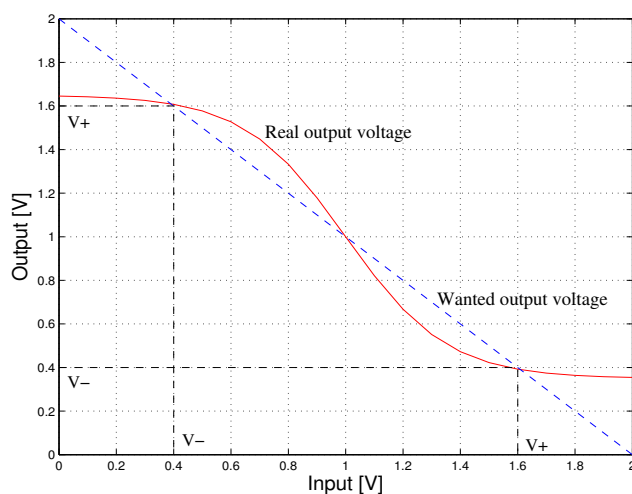
Figure 4.7: *Illustration of how errors are created in the converter. The slashed graph shows wanted output voltage and solid graph shows real output voltage of a SFG Inverter. $V^- = 0.4V$ and $V^+ = 1.6$ in this example.*

Second, the number of cycles can be extended by introducing the new error correction scheme. The circuit exploits negative inverter gain in the converter loop as negative feedback. This causes errors of previous iterations to be subtracted. By applying the same alternating inversion to digital input codes, only errors are subtracted. LSB ABI digital input codes were presented in more detail in chapter 2.3. Examples of 2, 3 and 4 bit codes are shown in the tables on pages 16 and 17. The codes are more complex than LSB and MSB codes which are standard binary numbers.

Measured DAC-2 operation is illustrated in figure 4.8, figure 4.9 and figure 4.10. In the first measurement in figure 4.8 there are four traces. The first trace shows a radix eight analog output voltage sampled from node Y_i. Trace two is a train of bit-serial input codes. This code sequence generates a staircase at the output node in trace one. Trace three shows the reset signal applied in node Ψ. The last trace shows the recharge clock signal Φ (bit-clock). In figures 4.9 and 4.10 the resolution is increased to radix 16 by

Figure 4.8: *Measured DAC-2 output voltages. Configured for radix R=8 using n=3, $f_\phi = 61.86kHz$, $f_\psi = 20.62kHz$. The four traces are; analog output voltage Y_i, bit-serial input code B_i, reset clock Ψ and bit-clock Φ.*

applying four bit input codes. An additional illustration of the converter operation is shown in figure 4.11.

Figure 4.9: *Measured DAC-2 output voltages. Configured for radix R=16 using n=4, $f_\phi = 62.5kHz$, $f_\psi = 15.63kHz$. The three traces are; analog output voltage Y_i, bit-serial input code B_i and bit-clock Φ.*
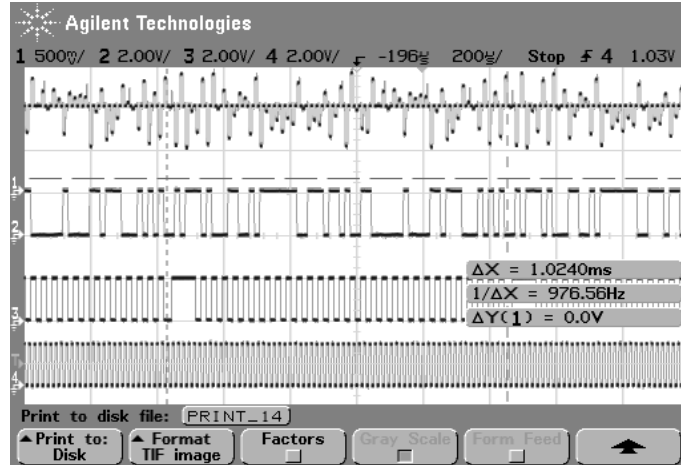
Figure 4.10: *Measured timing of clock signals for DAC-2. Configured for radix R=16 using n=4, $f_\phi = 62.5kHz$, $f_\psi = 15.63kHz$. The four traces are; analog output voltage Y_i, bit-serial input code B_i, reset clock Ψ and bit-clock Φ.*
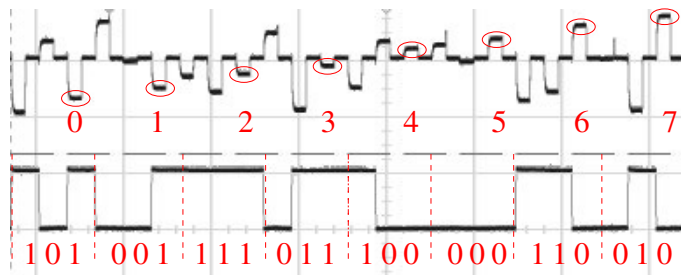
Figure 4.11: *Illustration of LSB ABI D/A conversion. A measurement using DAC-2 and three bit resolution is used as illustration data. The multiple-valued output voltage levels are circled out. Labels are included for the voltages representing the multiple-values (0-7) generated by the LSB-First input codes (000-111).*

4.4 Improved SDR LSB D/A Converter (DAC-3)
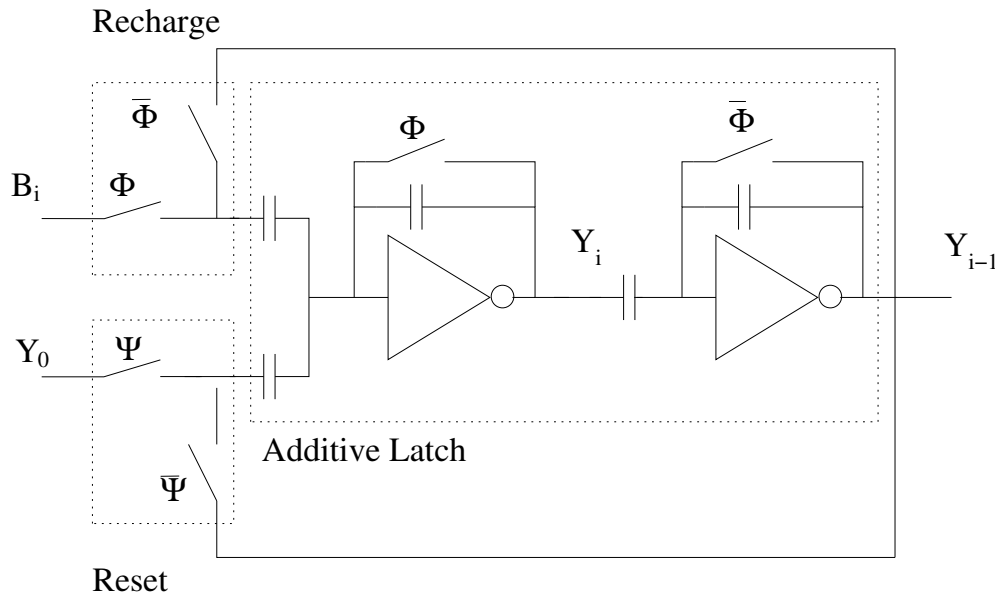
Figure 4.12: *Block diagram for latching serial-bit D/A converter with digital input B_i, recharge signal Φ, reset signal Ψ and analog output voltages Y_i and Y_{i-1}.*

Figure 4.12 shows a new SDR LSB D/A converter from [41]**[Paper IV]** called DAC-3. Compared to earlier work on DAC-1 in [38]**[Paper I]**, DAC-3 features a shorter multiple-valued signal path. This is made possible by use of sample and hold elements [40]**[Paper III]** which have an increased accuracy and a higher functional capacity per device than traditional SFG Latches.

The conversion process is synchronized by the perfectly matched and non-overlapping complementary clock signals Φ and $\overline{\Phi}$. Compared to DAC-1 [38] **[Paper I]** and DAC-2 [39]**[Paper II]**, the converter is latching. This means that the "recharge and evaluation" clock scheme is replaced by a "sample and hold" clock scheme [40]**[Paper III]**. In this scheme all input signals are sampled or latched into the converter. As a result the interleaved recharge voltages are shifted by 180 degrees compared to the "recharge and evaluation" clock scheme. The presented implementation makes use of switches for recharging of the input signals B_i and Y_0. There are two feedback wires. The upper wire interleaves the bit-serial input with a recharge voltage ($V_{dd}/2$). The lower wire provides a negative feedback of the intermediate analog output voltage Y_i.

In this circuit the critical number of analog SFG inverter based computations per cycle has been further reduced. The conversion process now requires two computations in each of the $n-1$ first cycles, and one computation for the n-th and final iteration. As a result, only $2(n-1)+1$ analog SFG inverter computations are involved. The converter supports one iteration of the SDR LSB D/A conversion algorithm (equation 2.4) per clock cycle.

Measured DAC-3 operation is illustrated in figures 4.13 and 4.14. In the first measurement there are four traces. The first trace shows a radix four analog output voltage from node Y_i. Trace two is a train of bit-serial input codes applied at node B_i. This code sequence generates a staircase at the output node in trace one. Trace three shows the reset signal applied in node Ψ. The last trace shows the recharge clock signal Φ. In figure 4.14 the three traces are shown. The first trace shows the 16 output voltage levels. The trace is a sampled from node Y_i. Trace two is the sampling clock signal and the last trace is the bit-serial input codes applied at node B_i.
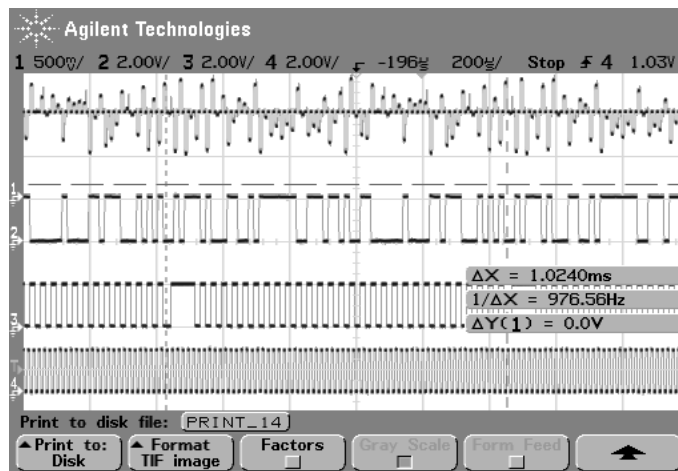
Figure 4.13: *Measured DAC-3 output voltages. Configured for radix R=4 using n=2, $f_\Phi = 82.98kHz$, $f_\Psi = 41.49kHz$. The four traces are; analog output voltage Y_i, bit-serial input code B_i, reset clock Ψ and bit-clock Φ.*
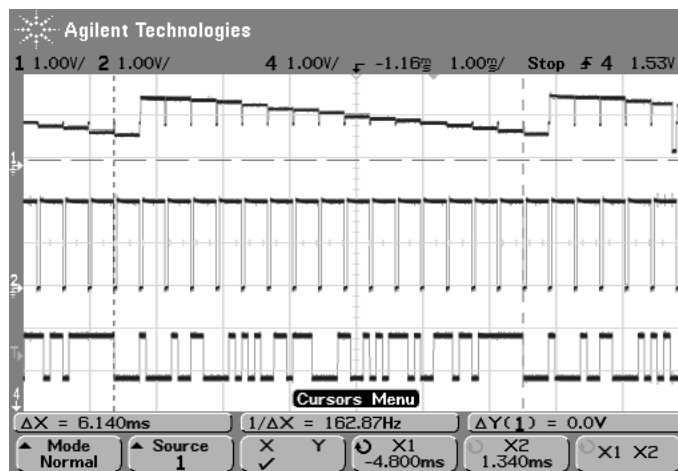
Figure 4.14: *Measured DAC-3 output voltages. Configured for radix R=16 using n=4, $f_\phi = 10.4kHz$, $f_\psi = 2.6kHz$. The three traces are; analog output voltage Y_i, sampling signal and bit-serial input code B_i.*

4.5 DDR LSB D/A Converter (DAC-4)
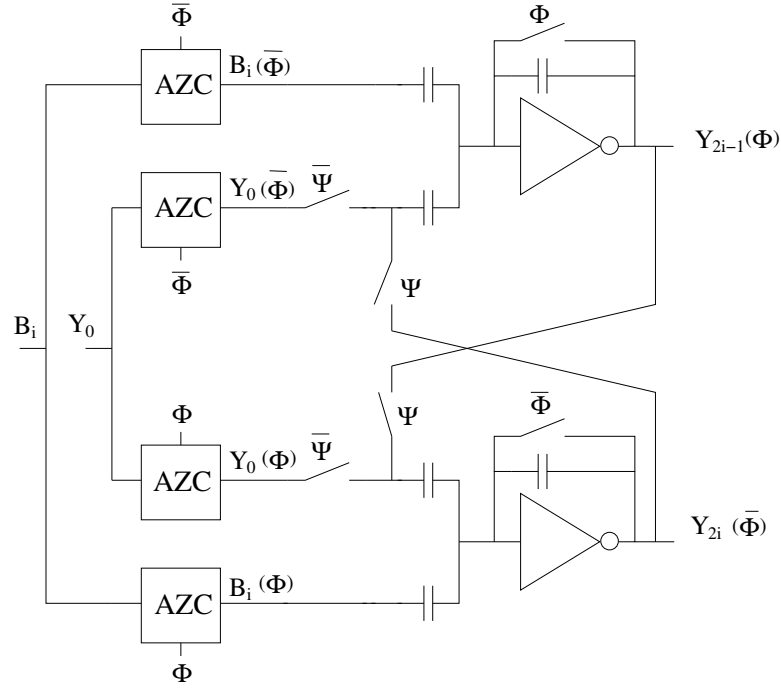
Figure 4.15: *Block diagram for DDR LSB serial-bit D/A converter with digital input voltage B_i, recharge signal Φ, reset signal Ψ, analog output voltage Y_{2i-1} and analog output voltage Y_{2i}.*

In figure 4.15 [42] **[Paper V]** a new and faster SFG serial D/A converter is presented. The converter supports two iterations per clock cycle compared to merely one in DAC-1 [38] **[Paper I]**, DAC-2 [39] **[Paper II]** and DAC-3 [41] **[Paper IV]**. This change is made possible by combining two SFG S/H elements from [40]**[Paper III]** in a loop.

A new Dual Data-Rate (DDR) clock scheme is introduced in which SFG operations are performed on both recharge clock edges. The remaining time is utilized as settling time and guard intervals. A reduced conversion rate is one of the main problems associated with cyclic D/A conversion [46]. Between each iteration the stored intermediate analog output voltage is delayed only half a clock period between each addition. As a result, by using this new scheme, bit-rates at twice the maximum SFG recharge rate are supported. Because of this property the converter will be referred to as a Dual Data-Rate (DDR) converter. DAC-4 [42]**[Paper V]** is the only converter in this work which supports bit-rates at twice the maximum SFG recharge rate. It is also the only converter presented to process data at a rate beyond the fundamental recharge rate limit. This allows the generation of radix four

signals using merely one recharge clock cycle which correspond to a radix of sixteen after only two recharge clock cycles.

Compared to the extremely compact DAC-3 [41][**Paper IV**], the size of DAC-4 is only marginally increased. However, four auto-zero circuits (AZC) [59] are utilized for generating input signals with an interleaved recharge voltage. These AZC's contribute noticably to the die area of DAC-4. The two SFG Inverters are in a looped SFG Latch configuration. This means that while resetting one SFG Inverter the other acts as an output buffer.

Again, two bias voltages Y^- and Y^+ are included, allowing the multiple-valued output voltage levels to be tuned. The initial value Y_0 is set to the smallest output Y^-, which corresponds to the all-zero code voltage. An initial condition, $Y_0 = Y^-$, is set by applying a high reset clock signal Ψ and low complementary reset clock signal $\overline{\Psi}$. The converter is also expected to function with initial voltage Y_0 set to $V_{dd}/2$. Note that each iteration is synchronized by the edges of the perfectly matched and complementary clock signals Φ and $\overline{\Phi}$.

Practical experiments use digital input b_i encoded as $Y^- = 0.5V$ when a '0' and $Y_+ = 1.5V$ when '1'. The input signal b_i is latched or sampled into the converter as in DAC-3. SFG inverter based latching requires input signals to be interleaved with a recharge voltage of $V_{dd}/2$. These voltages are denoted $b_i\left(\overline{\Phi}\right)$, $b_i\left(\Phi\right)$, $Y_0\left(\overline{\Phi}\right)$ and $Y_0\left(\Phi\right)$. In DAC-4 the recharging is done using AZC's as shown in figure 4.15. The introduction of AZC's is motivated by a reduction in clock signal complexity and their application as input buffers.

Measured DAC-4 operation is illustrated in figures 4.16 and 4.17. In the first measurement in figure 4.16 there are four traces. The first trace shows a radix 16 analog output voltage sampled from node Y_{2i}. The next trace shows a read-out clock signal controlling a sample and hold circuit. Trace three shows the reset signal applied in node Ψ. The last trace shows a train of bit-serial input codes applied at node B_i. In figure 4.17 only sampled output voltages and bit-serial input codes are traced. In figure 4.18 timing of clock signals is illustrated. Four traces are shown. These are recharge clock from node $\overline{\Phi}$, reset clock from node Ψ, a sample clock and the bit-serial input codes applied at node B_i.

In DAC-4 [42][**Paper V**] the number of analog SFG inverter based processing has been further reduced. Only n SFG inverter computations are required per conversion process. This means an optimal one computation per iteration or per bit resolution.
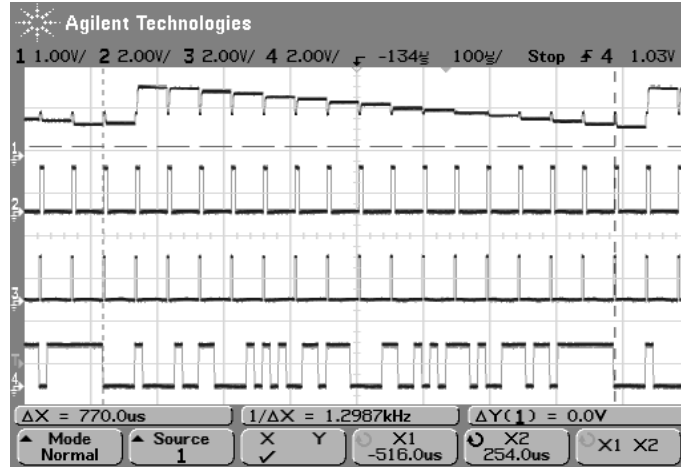
Figure 4.16: *Measured DAC-4 output voltages. Configured for radix R=16 using n=4, $f_\phi = 83.14kHz$, $f_\psi = 20.78kHz$. The four traces are; sampled analog output voltage Y_{2i}, read-out clock signal, reset clock Ψ and bit-serial input code B_i.*
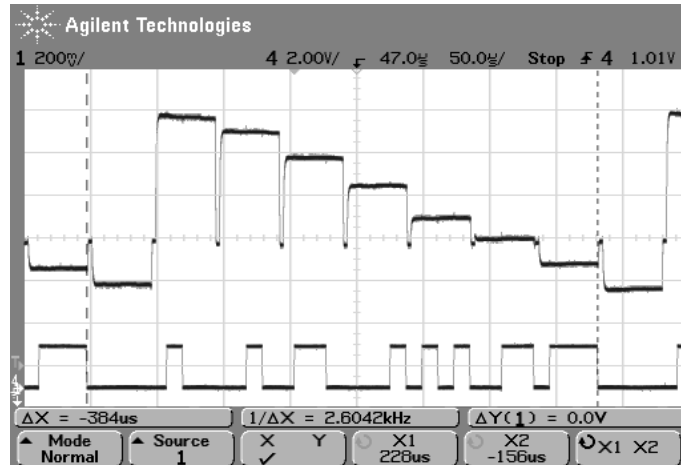
Figure 4.17: *Measured DAC-4 output voltages. Configured for radix R=8 using n=3, $f_\phi = 62.5kHz$, $f_\psi = 20.83kHz$. The two traces are sampled analog output voltage Y_{2i} and bit-serial input code B_i. The measurement setup was limited to an even number of bit. 3 bit resolution is therefore evaluated using 4 bit codes.*
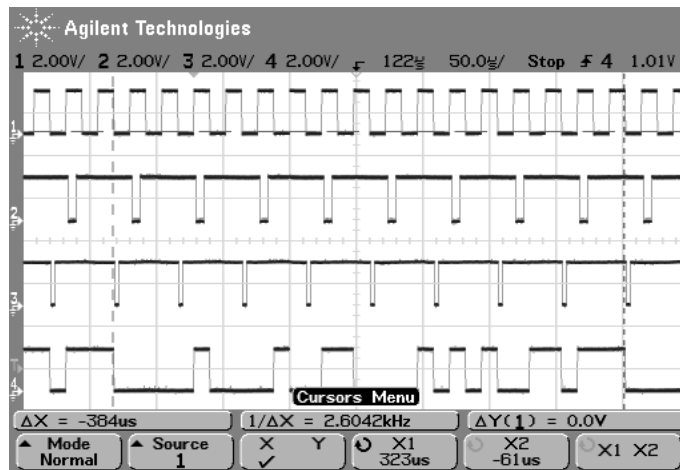
Figure 4.18: *Measured timing of clock signals for DAC-4. Configured for radix R=8 using n=3, $f_\phi = 62.5kHz$, $f_\psi = 20.83kHz$. The four traces are; recharge clock (bit-clock) $\overline{\Phi}$, reset clock Ψ, sample clock and bit-serial input code B_i.*

4.6   MSB D/A Converter (DAC-5)
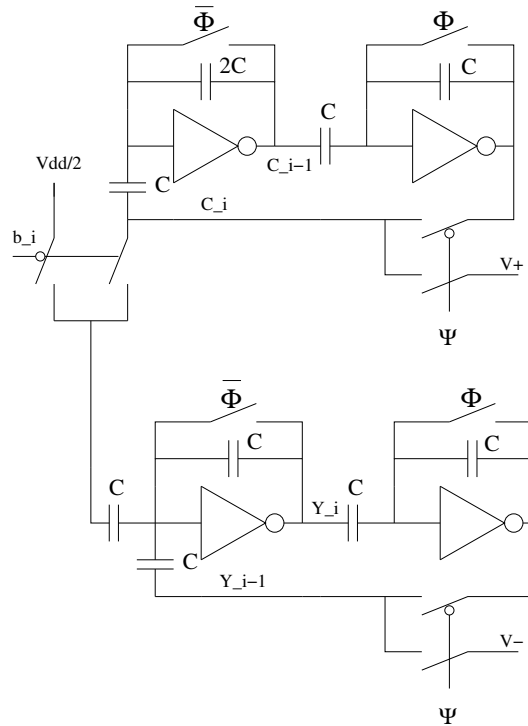
Figure 4.19: *Block diagram for MSB-first serial D/A converter using SFG devices.*

Figure 4.19 presents a new SFG MSB serial D/A Converter introduced in [43][**Paper VI**] called DAC-5. The converter supports runtime re-configuration of the output radix and Most Significant Bit-First (MSB) type digital input codes. MSB is the bit-order used by successive-approximation A/D converters. The development of a MSB-First serial D/A converter therefore becomes essential in multiple-valued encoder/decoder applications.

DAC-5 consists of two components, a SFG MV counter and a SFG MV accumulator, both modified versions of DAC-3 [41][**Paper IV**]. A high functional capacity per device is achieved by use of the SFG sample and hold clock scheme in [40][**Paper III**]. Note that the use of recharged input signals has been avoided in DAC-5. The presented MSB D/A converter therefore consists of only four SFG inverters.

The converter is clocked and biased using mainly the same input signals as in earlier work. A total of seven input signals are included; a serial MSB-first digital input (b_i), two recharge clock signals (Φ and $\overline{\Phi}$), two reset clock signals (Ψ and $\overline{\Psi}$), two bias voltages (V^- and V^+) and an additional voltage reference $V_{dd}/2$. Again, note that the input signals are not interleaved with a recharge
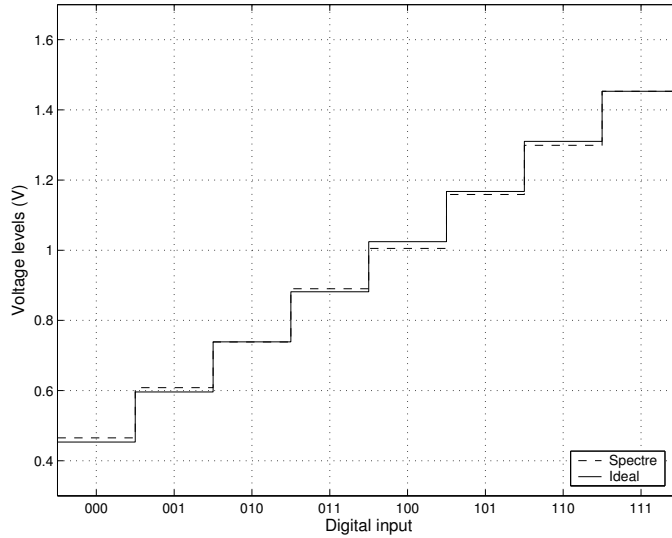
Figure 4.20: *Sampled output voltages of DAC-5. A stream of MSB-first digital input codes, 000_2-111_2, was used as test data.*

voltage. The analog output voltage results at terminal Y_i every n-th cycle and is easily retrieved using the SFG S/H circuit presented in [40]**[Paper III]**. The system is reset when Ψ is high. In this state the SFG MV accumulator is initialized with the all-zero code voltage, $Y_0 = Y(X_0) = V^-$, and the SFG MV Counter with the MSB-weight voltage $W_0 = V^+ = 1.5V$. These parameters assume a converter output swing between V^- and V^+.

SFG MSB-First serial D/A conversion was described earlier in chapter 2.4 (equation 2.12). Figure 4.19 showed a practical implementation. In the SFG MV counter, binary weights are generated successively in a descending order, starting with the weight of the MSB ($W_0 = V^+$). The voltages representing binary weights are offset by a voltage of $V_{dd}/2$. In each cycle a divide-by-two operation takes place. This is implemented using a feedback capacitor which is twice as large as the input capacitor.

The multiplication problem is solved using a set of switches. A switch selects the zero weight voltage $V_{dd}/2$ for a low digital input and its binary weight W_i for a high digital input bit. In the SFG MV accumulator the products are then added to the result of previous iterations. All capacitors of the SFG MV accumulator are chosen equally large.

In figure 4.20 extracted multiple-valued output voltages are shown as a function of digital MSB-first input codes. The data is based on simulation results from Cadence using process parameters for the $0.35\mu m$ AMS process. A bit-rate (Φ) of 10 MHz and a resolution (N) of three bit was utilized. Figure 4.21 shows a characterization of the converter linearity. The INL and DNL
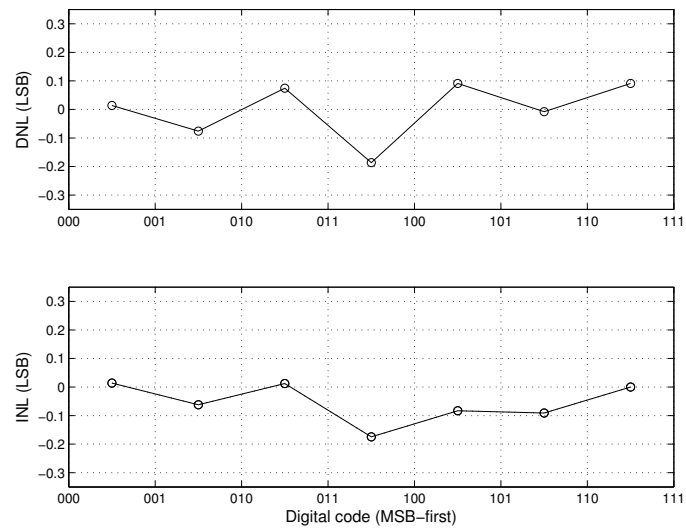
Figure 4.21: *DNL and INL figures of merit for DAC-5. Voltage levels were extracted from the simulation included in figure 4.20 where 3 bit resolution was used.*

values demonstrate a monotonic increasing D/A converter output with an offset voltage of 65 mV. The output voltages representing the largest and the smallest input codes were 0.98V apart.

4.7 Summary

Studies on five SFG based cyclic D/A converters have been presented. Three standards of codes are covered; MSB, LSB and LSB ABI. The main focus is on LSB codes. Chip design and measured results are provided on DAC-1 [38] **[Paper I]**, DAC-2 [39]**[Paper II]**, DAC-3 [41]**[Paper IV]** and DAC-4 [42]**[Paper V]**. DAC-1, DAC-3 and DAC-4 implement LSB D/A conversion. DAC-2 implements LSB ABI D/A conversion.

In figure 4.23 the measured analog voltages of D/A converters DAC-1,..,DAC-4 are summarized. It includes measured results of the three radices of interest in SFG MV encoders; 4, 8 and 16 levels. The converters are characterized by computing the non-linear measures DNL and INL. In figures 4.25, 4.26 and 4.27 the INL values for SFG converters using two, three and four bit resolution are included. The corresponding DNL values are shown in figures 4.28, 4.29 and 4.30. All chip measured results demonstrate monotonic output with sufficient accuracy and resolution for multiple value encoder applications.

One of the main objectives of the project is to provide a compact and linear SFG D/A converter by the use of cyclic D/A converter algorithms. The first converter, DAC-1, demonstrated SFG cyclic D/A conversion using LSB codes. The SFG inverters propagate level-noise. This makes the number of SFG inverter based computations per conversion an important parameter. Figure 4.24 shows a comparison of the number of SFG inverter computations per conversion, both as a function of each practical implementation and the number of bit resolution. The number of computations per iteration is reduced from four in DAC-1 to only one computation in circuit DAC-4. Measured results indicate that linearity improves with a decreasing number of computations per conversion.

Converters DAC-2 (SDR LSB ABI) and DAC-4 (DDR LSB) demonstrate the best linearity and the overall lowest DNL values. DAC-2 provides lower gain, but otherwise compete well with DAC-4. Each iteration in DAC-2 involves three level-noise propagating and generating SFG inverter computations, while in DAC-4 only one SFG inverter computation per iteration is needed. This demonstrates the power of the LSB ABI error correction algorithm.

DAC-3 has the most compact design, but provides half the maximum conversion rate of DAC-4. The die area requirement of the proposed circuits is mainly given by the inter-poly capacitors. An overview of the capacitor geometries is presented in table 4.1. This choice of device sizes is based on simulations in Cadence Spectre and extracted parasitic capacitance values. Peak INL/DNL values are summarized in figures 4.31 and 4.32. The number of SFG Inverter computations per iteration (k) are 4 in DAC-1, 3 in DAC-2, 2 in DAC-3 and 1 in DAC-4. A correlation between the number of compu-

Device	Geometry [m]	Area [m^2]
Capacitor of 18.8 fF	7.9u x 2.5u	1.97e-11
Capacitor of 24.5 fF	10u x 2.6u	2.6e-11
Capacitor of 28.6 fF	6.2u x 5u	3.1e-11
Capacitor of 48.7 fF	10.5u x 5.1u	5.35e-11
One-input analog inverter	23u x 21u	4.83e-10
Two-input analog inverter	28u x 21u	5.88e-10
Converter, D/A 1	120u x 21u	2.52e-09
Converter, D/A 2	100u x 21u	2.10e-09
Converter, D/A 3	90u x 21u	1.89e-09
Converter, D/A 4	77u x 50u	3.85e-09

Table 4.1: *Converter circuits and die area requirements from implementation on a 0.35μm ASIC. The device sizes were chosen based on simulations in Cadence Spectre.*

tations and peak INL/DNL values is observed when using three or four bit resolution. DAC-2 performs beyond the predicted INL/DNL values due to LSB ABI error correction.

The SFG Inverters have a lower leakage current and limited speed due to the use of minimum-size transistor geometries. In the introduction we assumed the wanted capacitor values to be much larger than the parasitic values. However, in order to reduce die area and settling times the wanted capacitor values are kept small.

Figure 4.22 shows a performance summary of the presented LSB-First cyclic D/A converters. This includes measured experimental results of DAC-1 [38], DAC-2 [39], DAC-3 [41] and DAC-4 [42]. In figure 4.22 results are also compared to related work on cyclic D/A converters reported in the following papers; Bell-2005 [31], Arnourah-2002 [29], Ogawa/Shibata-2001 [32], Moussavi-2001 [33], Cauwenberghs-1995 [30], Wang-1992 [34], Wang-1993 [35] and Suarez/Gray-1975 [26].

In [60][61], Robert Walden suggests a figure of merit (FoM) which includes the effective number of bits (ENOB) N, power dissipation P and sampling rate F_S.

$$F = \frac{2^N F_S}{P}$$

This FoM correctly includes the performance limitations of signal-to-noise-and-distortion ratio (SNDR) and still produces optimistic results for some low resolution converters.

Paper	#bit	#devices	Area [um²]	Tech. [um]	Power	Conversion rate	Vdd/range	#biases	Unit.cap.
Bell-2005	8-12	80	7875	-	5uA, 10V	66.7kSps/12bit	10V/4.6V	3 (6)	-
Arnourah-2002	8	1)	-	0.5	-	1 bit / cycle	5V/2V	1	-
Ogawa/Shibata-2001	8	36	530x22=11660	0.6	-	-	5V/1V	-	-
Moussavi-2001	12	-	0.22mm²	0.35	10mW	4.416MSps/12bit	3V/-	2	0.5pF
Cauwenberghs-1995	8	114	216x315=68040	2	100mW	25MSps/8bit	5V/4V	7	-
Wang-1993	10	3)	-	Discrete	-	1 bit / cycle	-/4V	1	-
Wang-1992	8(14)	2)	-	Discrete	-	1 bit / 2 cycles	-/2.5V	1	-
Suarez/Gray-1975	8	15	1.61mm²	-	-	74.07kSps/8bit	15V/-	2	-
DAC-4	4	22	77x50=3500	0.35	~250uW	1 bit / cycle	2V/1V	1 (2)	~20fF
DAC-3	4	17	90x21=1890	0.35	~250uW	1 bit / cycle	2V/1V	1 (2)	~20fF
DAC-2	4	23	100x21=2100	0.35	~375uW	1 bit / cycle	2V/1V	1 (2)	~20fF
DAC-1	4	29	120x21=2520	0.35	~500uW	2 bit / cycle	2V/1V	1 (2)	~20fF

1) 1 OTA, 4 capacitors, 8 switches
2) 3 OTA's, 5 capacitors and 15 switches
3) 2 OTA's, 4 capacitors, 8 switches

Figure 4.22: *A performance summary of the presented cyclic D/A converters. The experimental results are compared to the reported performance of converters in related work.*
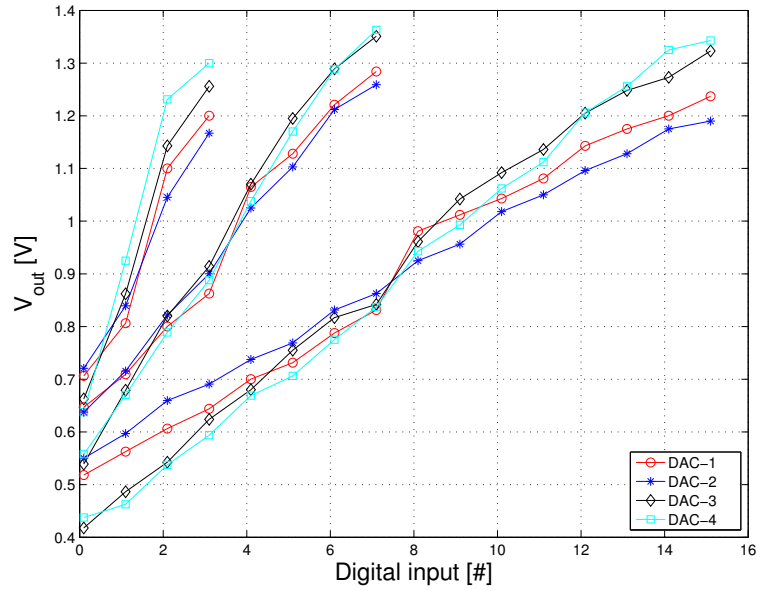
Figure 4.23: *Measured output voltages of SFG LSB D/A converters. Circuits are configured with 2, 3 and 4 bit resolution. Some of the measurements are subject to offset voltage correction.*
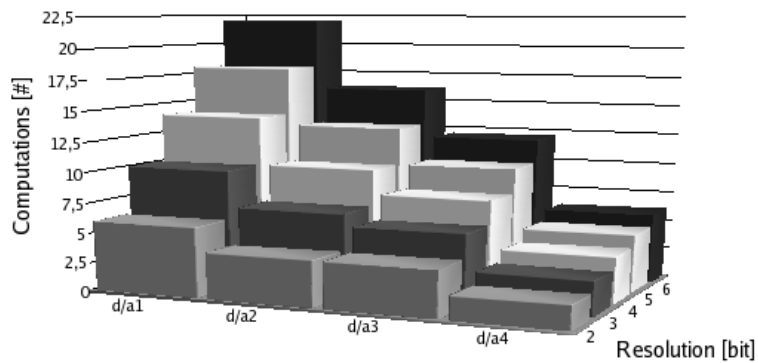
Figure 4.24: *Comparison of the number of SFG inverter computations per conversion as a function of D/A circuit and resolution.*
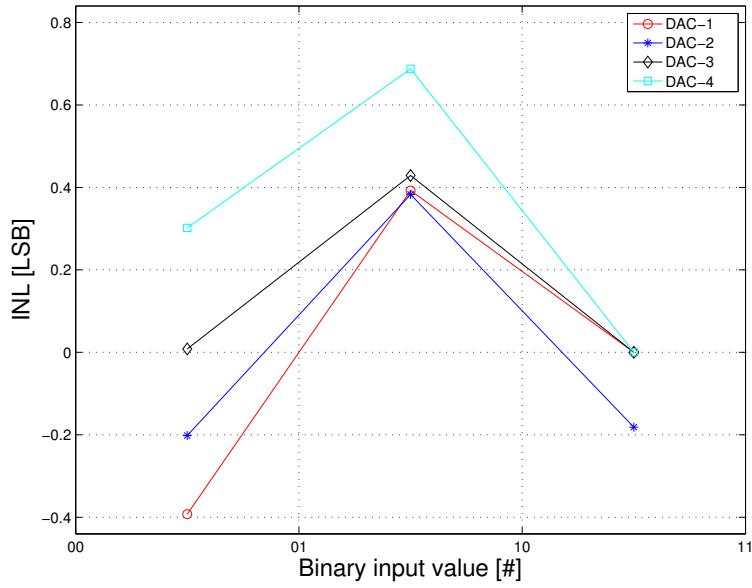
Figure 4.25: *INL for measured D/A converter output voltages, n=2.*
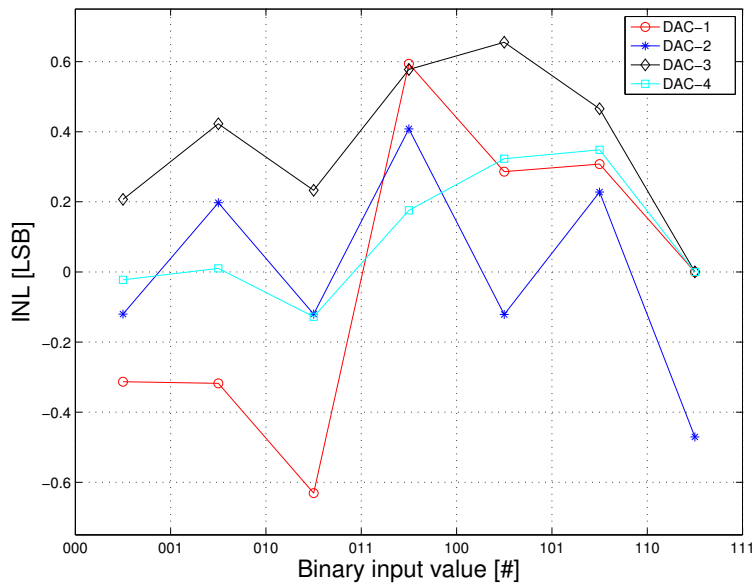
Figure 4.26: *INL for measured D/A converter output voltages, n=3. DAC-4 was measured using 4 bit codes.*
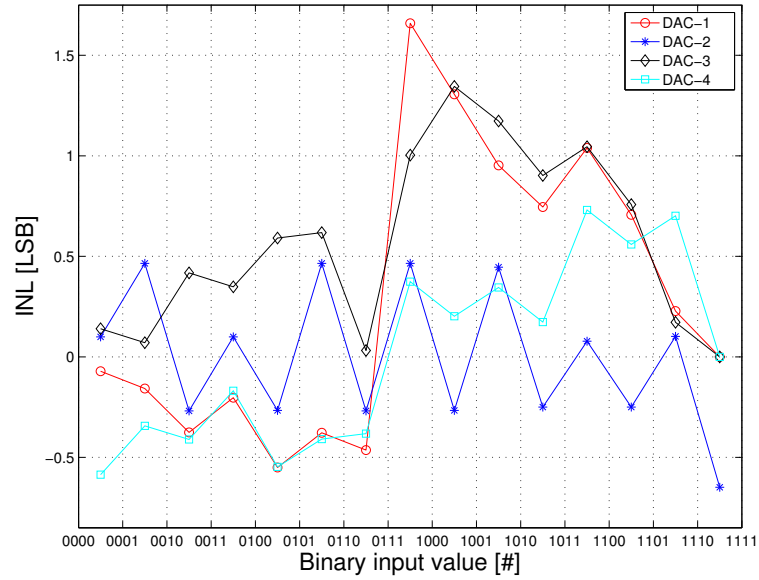
Figure 4.27: *INL for measured D/A converter output voltages, n=4.*
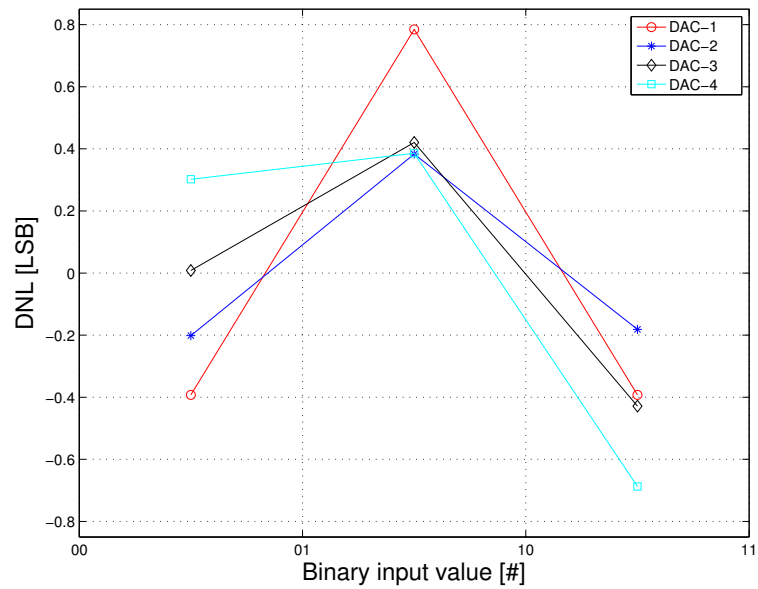
Figure 4.28: *DNL for measured D/A converter output voltages, n=2.*
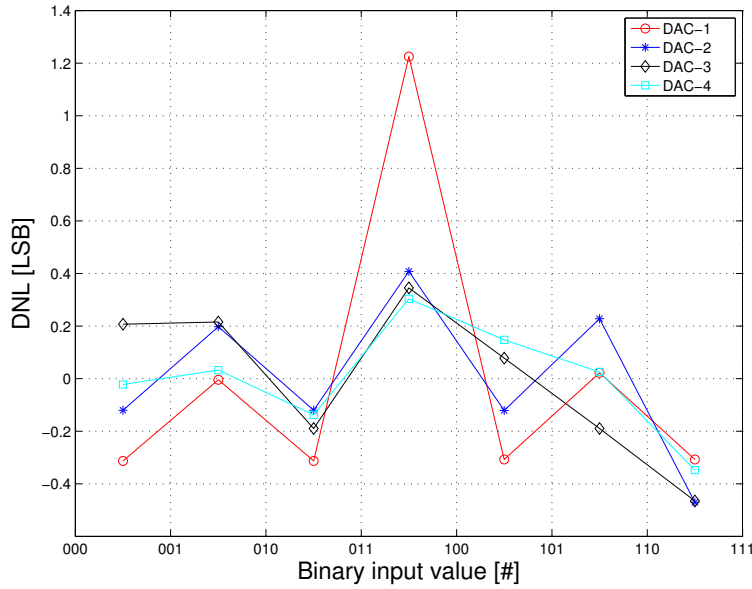
Figure 4.29: *DNL for measured D/A converter output voltages, n=3. DAC-4 was evaluated using 4 bit codes.*
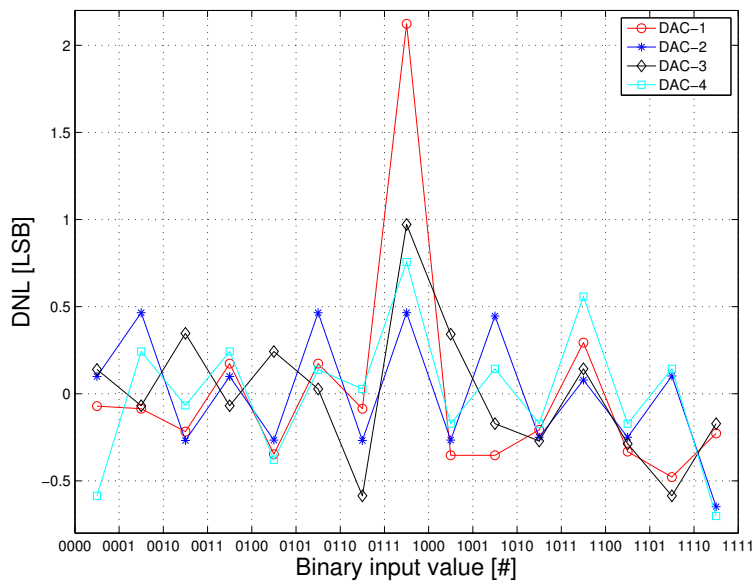
Figure 4.30: *DNL for measured D/A converter output voltages, n=4.*
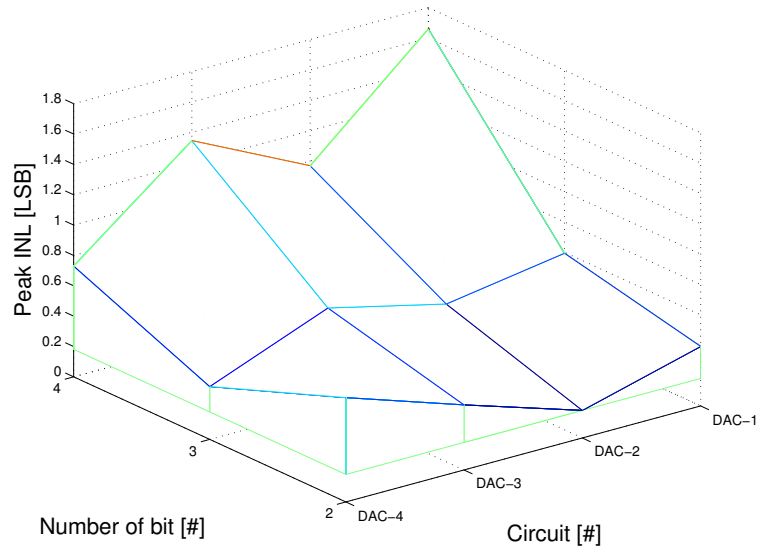
Figure 4.31: *Summary of INL values for measured D/A converter output voltages. The number of SFG Inverter computations per iteration (k) are 4 in DAC-1, 3 in DAC-2, 2 in DAC-3 and 1 in DAC-4. DAC-2 uses LSB ABI error correction and performs beyond the predicted INL values.*
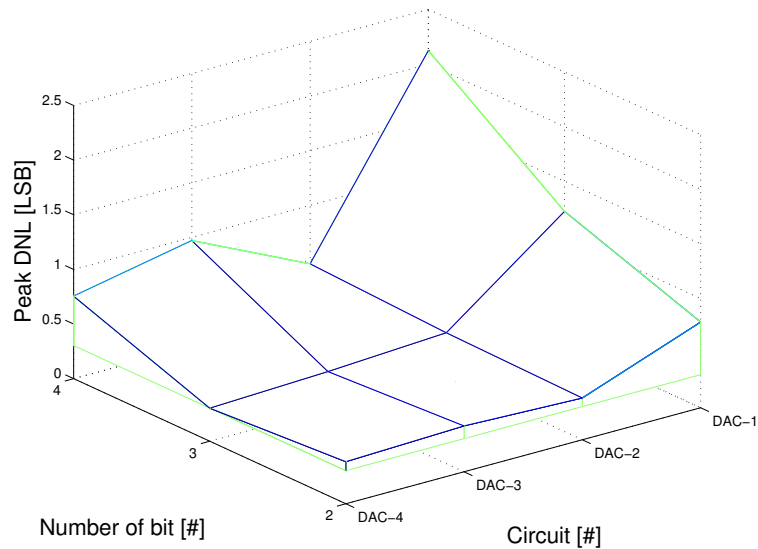
Figure 4.32: *Summary of DNL values for measured D/A converter output voltages. The number of SFG Inverter computations per iteration (k) are 4 in DAC-1, 3 in DAC-2, 2 in DAC-3 and 1 in DAC-4. DAC-2 uses LSB ABI error correction and performs beyond the predicted DNL values.*

Chapter 5

AUXILIARY CONVERTER CIRCUITS

This chapter summarizes work on auxiliary circuits [40, 44, 45]**[Papers III, VII and VIII]** of relevance for the SFG serial D/A converter. The ternary refresh element introduced in [45]**[Paper VIII]** is implemented on a chip and additional unpublished measured results are provided.

5.1 Introduction

A complete recharged cyclic D/A converter architecture using recharged SFG inverters is presented. Figure 5.1 shows a typical architectural view of the converter. It consists of a converter core (D/A), a frequency divider (FDIV) and a sample and hold (S/H) output stage. The FDIV counts the number
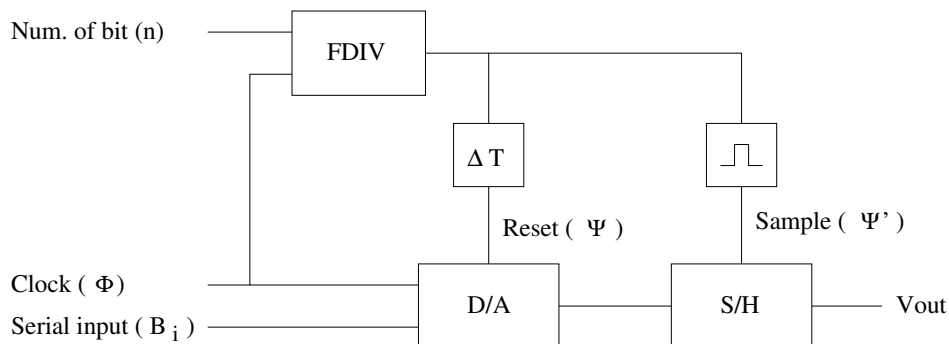
Figure 5.1: *A typical recharged cyclic D/A converter architecture. It consists of a recharged SFG cyclic D/A converter core (D/A), a recharged SFG frequency divider (FDIV) and a recharged sample and hold output stage (S/H).*

of bit converted and generates an initial reset pulse while processing the first bit of a digital input code. Each iteration is assumed to require a full clock cycle. After all the bit have been processed, the analog value is stored in the S/H component.

The LSB-First, MSB-First and LSB-First with ABI versions of the D/A converter core are presented in chapter 4. This chapter focuses on the remaining components, the S/H read-out circuit and the FDIV based bit counter.

5.2   SFG S/H Circuits

A problem with the traditional SFG Latch [19] based memory is its accuracy and the generation and removal of the SFG recharge voltage. Two SFG S/H circuits [40][**Paper III**] are introduced; one SFG S/H Read-in circuit shown in figure 5.2 and one SFG S/H Read-out circuit shown in figure 5.4. The first introduces a recharge voltage to input signals by interleaving sampled values by a voltage $V_{dd}/2$. Figure 5.3 shows an illustration of the two modes of operation. In the SFG Read-out circuit two SFG S/H Read-in components are combined. By using complementary and overlapping recharge clock signals as shown in figure 5.5, it is possible to remove an interleaved recharge voltage from the sample. Measurements are included in figures 5.6, 5.7, 5.8 and 5.9. The results demonstrate successful generation and removal of the interleaved recharge voltages.

In a SFG serial D/A converter application the analog output voltages can be stored using a S/H circuit. A cyclic D/A conversion usually requires one cycle per bit in the digital input code. In the n-th cycle the analog output can be sampled and stored in analog memory. In a recharged cyclic D/A converter, such as the proposed SFG inverter based converters [38, 39, 41, 42, 43][**Papers I-II,IV-VI**], the output is interleaved with a recharge voltage and is available for only half of the final cycle. This gives a window for sampling which lasts half the time period of one cycle, $2/f_\Phi$.
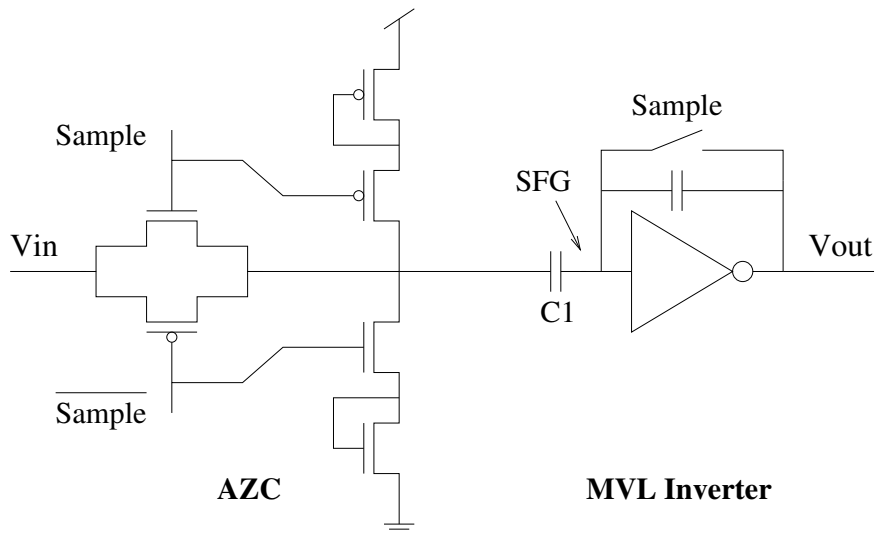
Figure 5.2: *Schematic diagram of a SFG S/H element. The circuit comprises of a Semi Floating-Gate Auto-Zero Circuit (AZC) and an analog SFG MV inverter.*
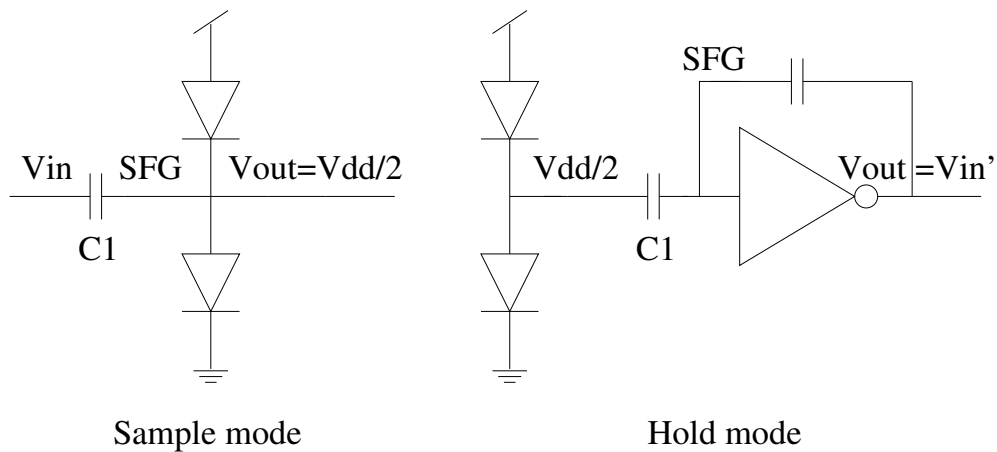
Figure 5.3: *Equivalent circuit diagrams for a SFG S/H Read-in circuit. The proposed circuit has two modes of operation; Sample and Hold.*
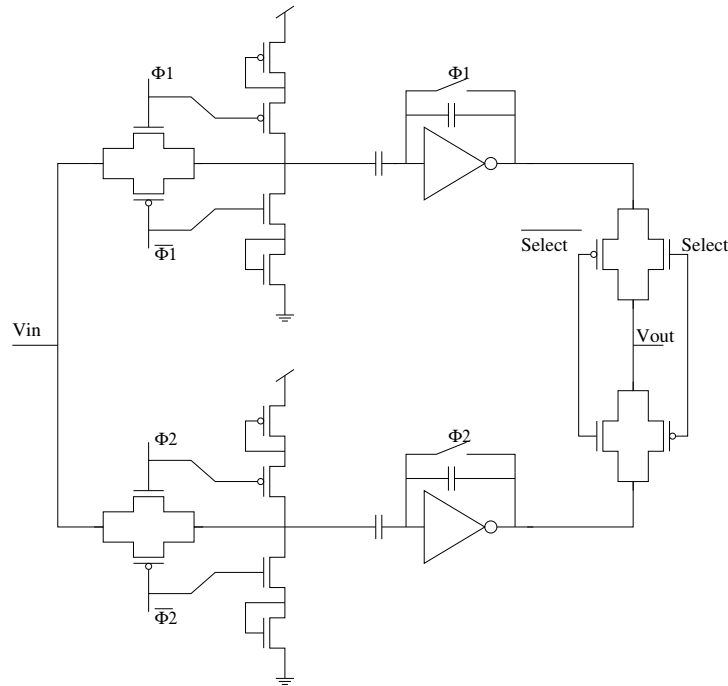
Figure 5.4: *Schematic diagram of a SFG S/H Read-out circuit. The circuit comprises of two SFG S/H elements and two pass-gate transistors. Three complementary external clock signals are required. One sample clock for each of the two S/H elements and a select clock for controlling the output switches.*
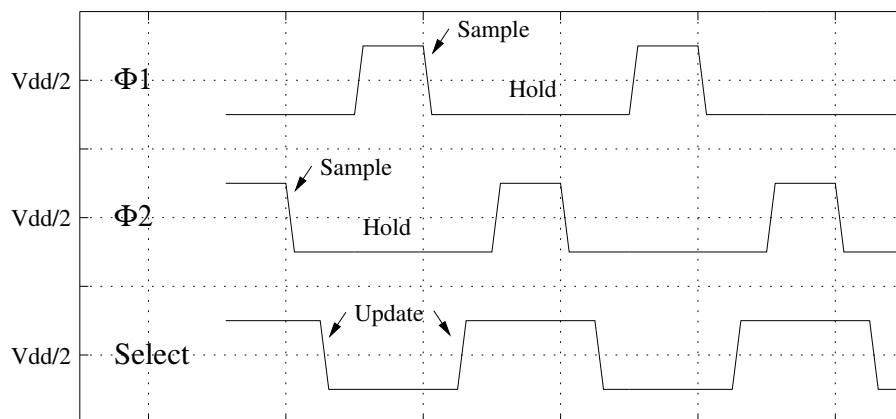
Figure 5.5: *Clock signal specification for the SFG S/H Read-out circuit shown in Figure 5.4. Asymmetric clock signals are utilized to give overlapping hold phases. The select signal updates the output voltage by swapping to the most recent sampled value.*
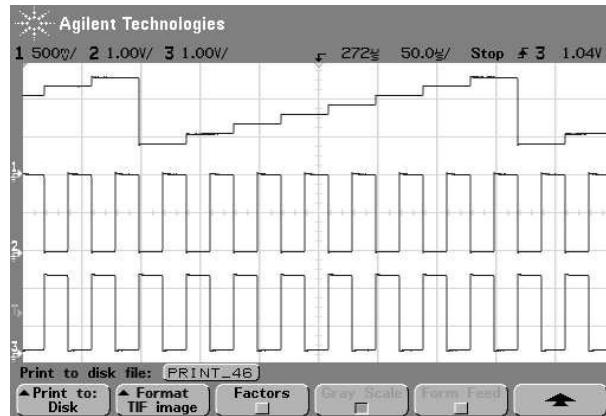
Figure 5.6: *Waveform describing test input signals in the SFG S/H Read-in measurement. Included is the multiple valued radix eight input signal and the two complementary sample clocks.*
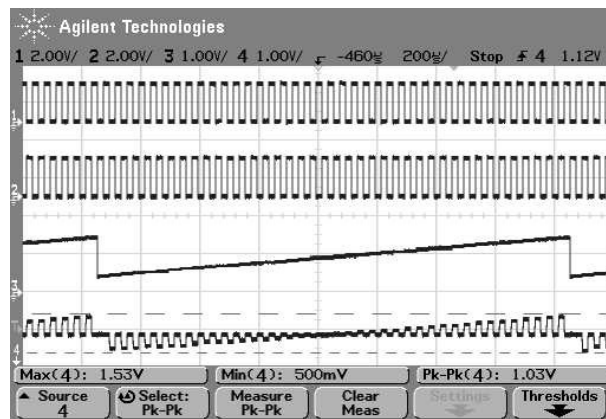
Figure 5.7: *Measured results for the SFG S/H Read-in circuit. The four traces are; sample clock Φ, complementary sample clock $\overline{\Phi}$, input waveform V_{in} and output voltage V_{out}.*
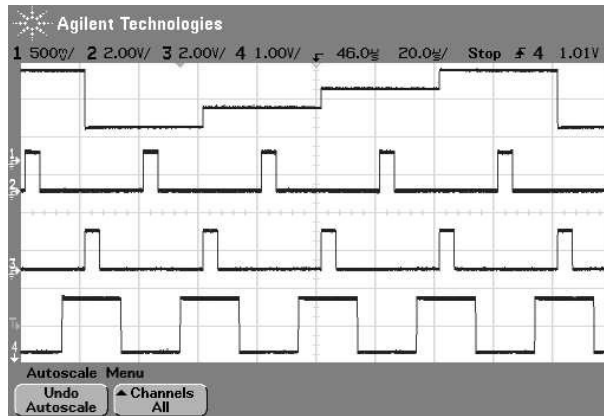
Figure 5.8: *Partial test input signals in SFG S/H Read-out measurement. Included in the oscilloscope plot are the two sample signals S/H_1 and S/H_2. A third Select signal is required, updating the output signal. Three additional complementary clock waveforms $\overline{S/H_1}$, $\overline{S/H_2}$ and $\overline{select}$ are also required. A radix 4 input wave is included for demonstration of the timing between the clock signals and the discrete time MV input waveform.*
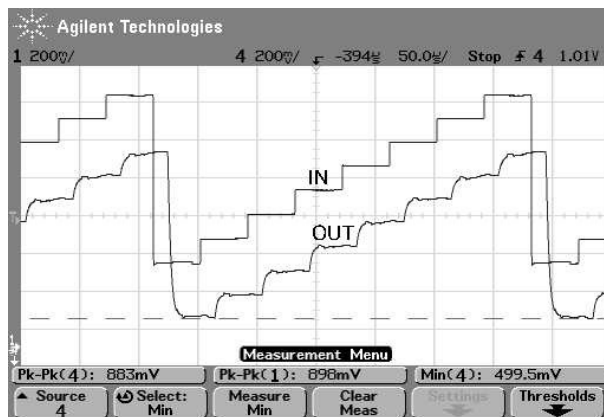
Figure 5.9: *SFG S/H Read-out measurement results. Measured result of a radix 8 input wave and corresponding sampled output waveform. The removal of the interleaved recharge voltage is observed.*

5.3   N-ary SFG MV FDIV
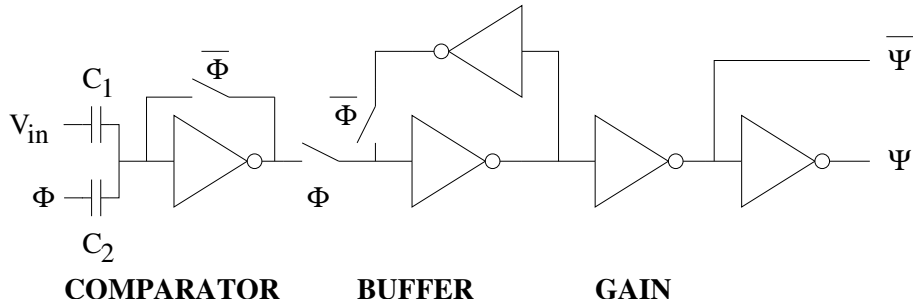
Figure 5.10: *Circuit diagram of a buffered SFG Comparator with removal of interleaved recharge voltages.*

Cyclic D/A converters often require a larger digital circuit for generation of control signals. Each conversion process is initiated by a clock signal which will be referred to as the reset clock signal. A common way to generate this clock signal is by use of a frequency divider. One cycle usually corresponds to one clock pulse. In recharged SFG cyclic D/A converters[38, 39, 41, 43]**[Papers I,II,IV,VI]** it is one recharge clock pulse (Φ). The frequency divider counts the number of clock cycles and generates a reset pulse after all digital input bits are clocked into the converter. The frequency dividers are often implemented using flip-flops which divide by two and create symmetrical output clock signals. The presented SFG cyclic converters however require an asymmetrical clock signal and support of divisors which are not a power of two. One example is SFG inverter based MVL where a radix of eight or three bit resolution is a common choice.

In [62] a digital counter of configurable resolution is described. The circuit is large and complex. This motivates the development of a configurable recharged SFG MV frequency divider [44]**[Paper VII]**. A compact MVL solution is made available by combining a recharged SFG MV counter and a recharged SFG Comparator [44]**[Paper VII]**. The proposed recharged SFG Comparator is illustrated by a circuit diagram in figure 5.10, an equivalent circuit diagram in figure 5.11 and a buffered output voltage in figure 5.12. Figure 5.13 shows the complete recharged SFG MV FDIV. In figure 5.14 and 5.15 generation of a reset pulse applicable as bit-counter in Single Data-Rate (SDR) SFG cyclic D/A converters [38, 39, 41, 43]**[Papers I,II,IV,VI]** is shown.

Comparator mode
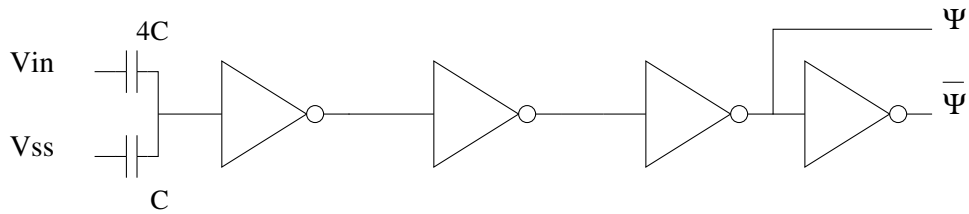
Hold mode
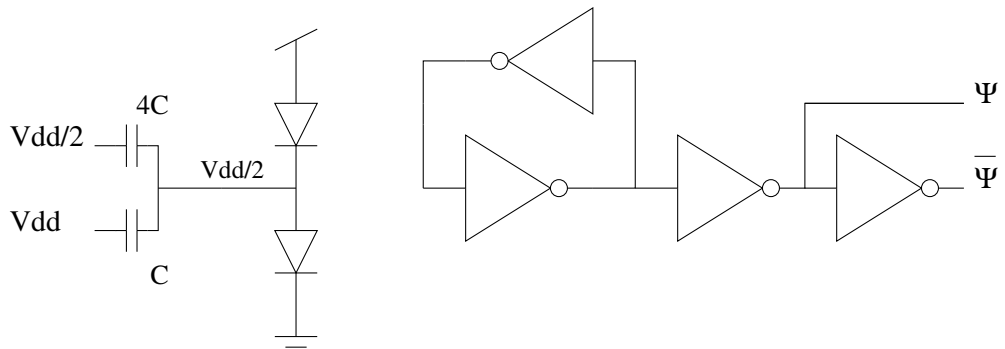
Figure 5.11: *Equivalent circuit diagrams for each of the two SFG Comparator modes of operation, "comparator" mode and "hold" mode.*
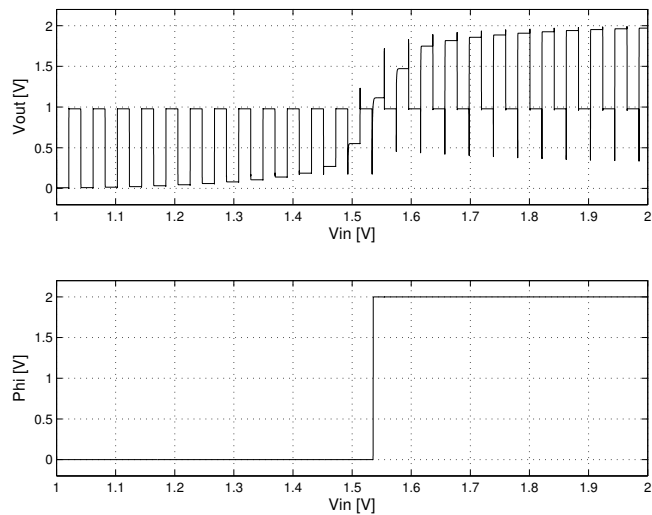
Figure 5.12: *Unbuffered and buffered output voltages of a recharged comparator. The comparator is configured with a switching point of 1.5V (3/4 V_{dd}).*
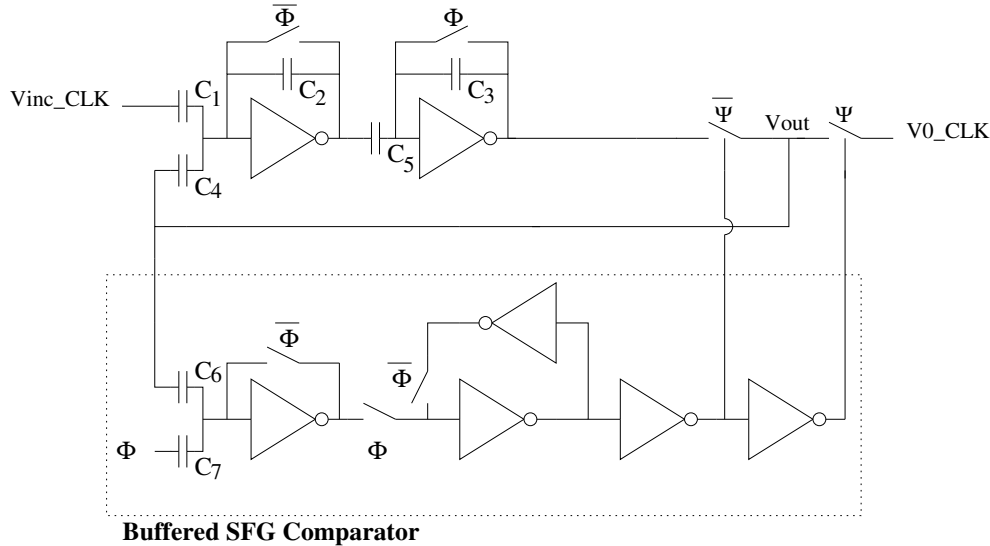
Figure 5.13: *Self-resetting multiple-valued counter using recharged inverters. The circuit consist of a recharged multiple-valued counter (upper section) and a buffered recharged comparator (lower section). The ideal or theoretical capacitor values are $C_4{=}C_5{=}C_7{=}C$, $C_2{=}2C$ and $C_6{=}4C$. These values implement the required scaling of the feedback signals.*
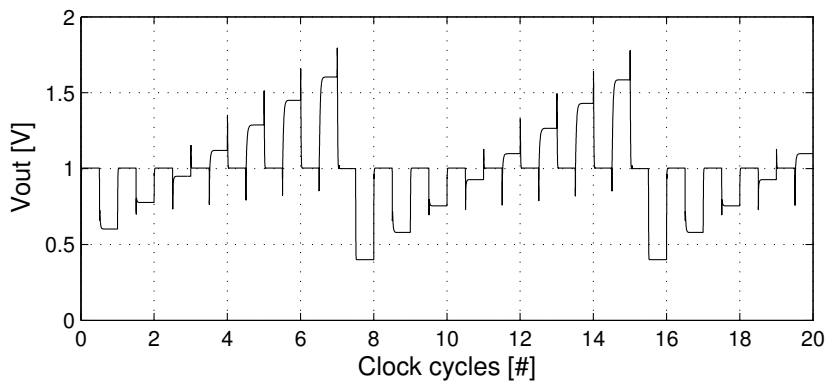
Figure 5.14: *Output voltage from internal multiple-valued counter with radix eight (N=8). The counter counts upwards from "0" to "7" before it is reset.*
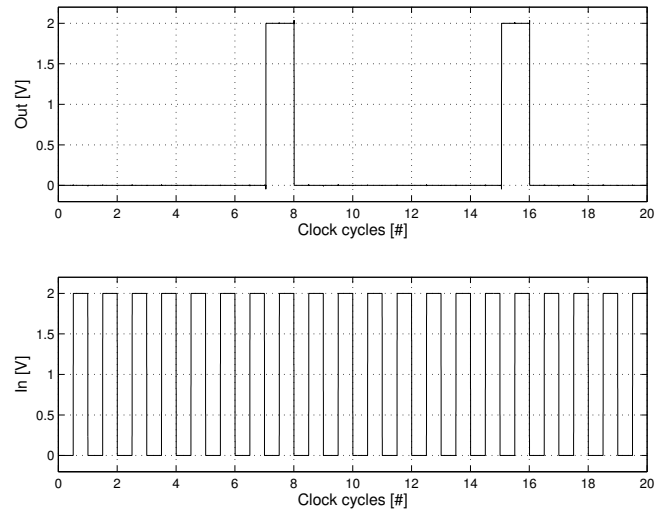
Figure 5.15: *Output and input clocks from frequency division with modulus 8. The output pulse has twice the pulse-width as that of the input clock.*

5.4 Ternary D/A conversion

The main focus of this thesis is on binary to multiple-valued radix conversion. However, based on the experience and knowledge gained on SFG serial D/A converters it can be useful to briefly discuss input signals of radices other than two. A natural place to start is ternary D/A conversion [63].

In [45][**Paper VIII**] a novel ternary switching element using SFG devices is presented. The proposed ternary refresh switching element is applicable as input stage in ternary LST-first SFG D/A converters. In this application level-noise/errors can be devastating. In the special case where digital (bi-nary) input codes are used it is sufficient to utilize two switches in a "select" configuration to suppress level-noise. The proposed ternary refresh element is modular and can be adapted to support input signals of other radices as well. In figure 5.16 the schematic diagram of the proposed ternary refresh element is included. Figure 5.18 shows an illustration of the ideal transfer function.

A practical implementation of the ternary refresh circuit in [45][**Paper VIII**] is not previously reported. Chip measured results are therefore included in figure 5.17. The measurement demonstrates suppression of level-noise in
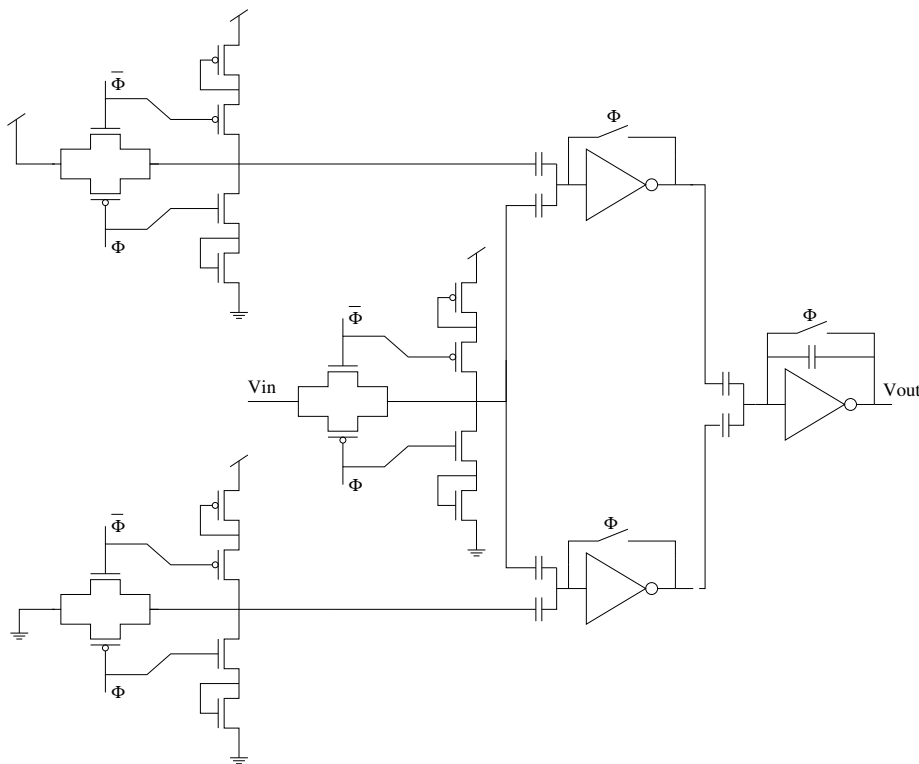
Figure 5.16: *Circuit diagram for ternary refresh element.*
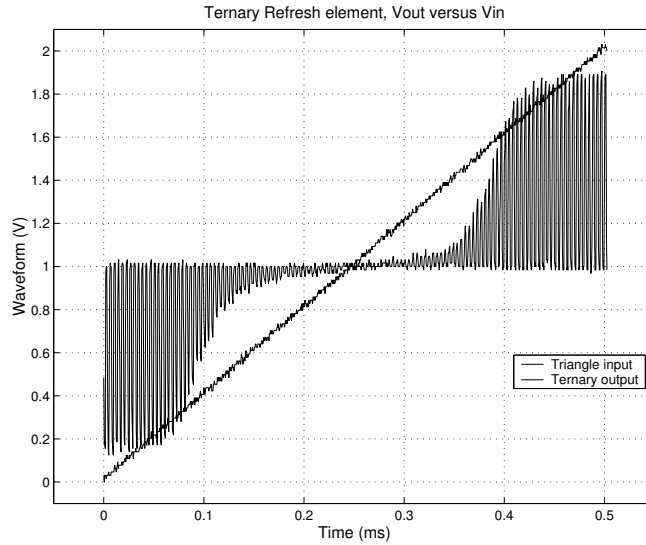
Figure 5.17: *Additional unpublished chip measurement for ternary refresh element. The measurement demonstrates suppression of level-noise and generation of an output voltage with radix three.*

ternary voltage-mode signals.

In chapter 4 it was concluded that the practical number of cycles in SFG serial D/A conversion is limited. Conversion with four bit resulting in equally many cycles was demonstrated with sufficient accuracy for MVL encoder applications. In cases where a higher resolution is required it can be interesting to increase the radix of the input signal. This may allow a higher resolution without an increase in deviation.

Ternary D/A converter circuits not previously published is briefly presented. Figures 5.19 and 5.21 shows the proposed Sschematic diagrams. The signal flow diagrams are included in figures 5.20 and 5.21. A ternary D/A converter uses least significant trit first (LST) input signals. An example of three trit codes is included in table 5.1. The ternary D/A converter has obvious advantages over the binary D/A converter. The main motivation is a reduced number of cycles. A resolution of 82 levels is possible using only four cycles, one per trit. This corresponds to a step size of $12.2mV$. In Practical implementation of ternary D/A converters is beyond the scope of this thesis.

Compared to the included work on binary SFG serial D/A converters [38, 39, 41, 42, 43][**Papers I-II,IV-VI**] capacitive weights are modified to allow a ternary input signal. In general a feedback capacitance of $Radix \cdot 0.5C$ and two inputs with capacitive weights $0.5C$ are needed. This means that earlier work on cyclic binary D/A conversion can be adapted to support ternary input signals by adding $0.5C$ to the feedback capacitance of the two-input
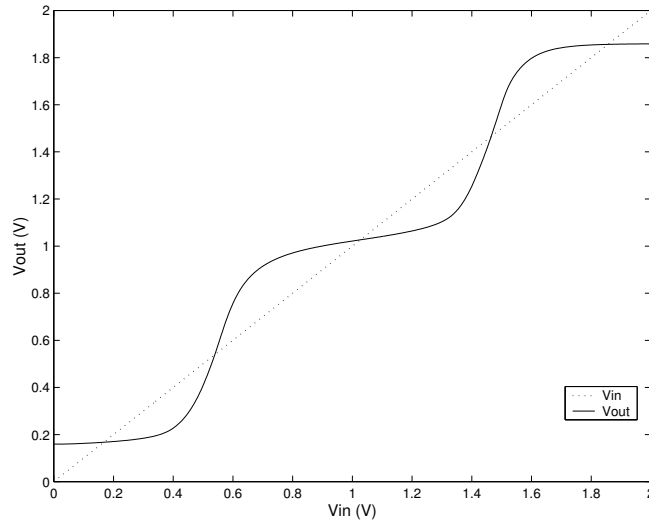
Figure 5.18: *Ideal ternary refresh element operation.*

additive SFG inverter. The result is shown in figure 5.19. Note that by expanding the general capacitor values by 3/2 we get the indicated values $C/3$, $C/3$ and C. Ternary D/A conversion is therefore modelled using the difference equation

$$Y_i = \frac{1}{3}t_i + \frac{1}{3}Y_{i-1}, \quad Y_0 = V^- = 0.5V, \ i = 1..n. \tag{5.1}$$

Also, for the ternary D/A converter to work input signals need to follow the specifications in table 5.1. Further, each trit (ternary digit) needs to be referred to the voltage $V^- + t(V^+ - V^-)$ where t is the unsigned trit and takes values 0, 1 or 2. The bias voltages $V^+ = 1.5V$ and $V^- = 0.5V$ are the same as when using binary input signals. This gives a ternary input signal referred to the voltages $0.5V$, $0.83V$ and $1.167V$. Note that the ternary switching element presented in [45][**Paper VIII**] was tuned for a different choice of voltage references.

MV	LST			LST ATI			Analog [V]
R=27	t_1	t_2	t_3	$\overline{t_1}$	t_2	$\overline{t_3}$	V_{out}/Y_3
0	0	0	0	2	0	2	0.0
1	1	0	0	1	0	2	0.0370
2	2	0	0	0	0	2	0.0741
3	0	1	0	2	1	2	0.1111
4	1	1	0	1	1	2	0.1481
5	2	1	0	0	1	2	0.1852
6	0	2	0	2	2	2	0.2222
7	1	2	0	1	2	2	0.2593
8	2	2	0	0	2	2	0.2963
9	0	0	1	2	0	1	0.3333
10	1	0	1	1	0	1	0.3704
11	2	0	1	0	0	1	0.4074
12	0	1	1	2	1	1	0.4444
13	1	1	1	1	1	1	0.4815
14	2	1	1	0	1	1	0.5185
15	0	2	1	2	2	1	0.5556
16	1	2	1	1	2	1	0.5926
17	2	2	1	0	2	1	0.6296
18	0	0	2	2	0	0	0.6667
19	1	0	2	1	0	0	0.7037
20	2	0	2	0	0	0	0.7407
21	0	1	2	2	1	0	0.7778
22	1	1	2	1	1	0	0.8148
23	2	1	2	0	1	0	0.8519
24	0	2	2	2	2	0	0.8889
25	1	2	2	1	2	0	0.9259
26	2	2	2	0	2	0	0.9630

Table 5.1: *LST and LST ATI input codes for 3 trit resolution. Analog voltages are calculated using Matlab.*
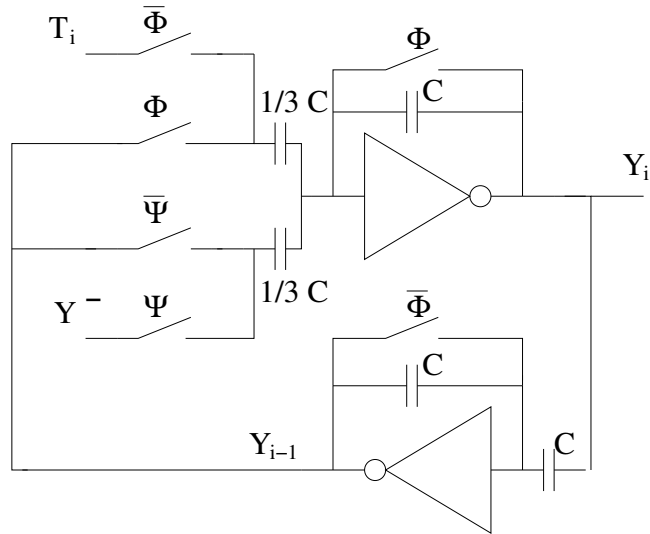
Figure 5.19: *Circuit diagram for ternary LST-first D/A Converter. The ternary input voltage T_i, initial condition Y^- and analog output voltage Y_i are shown.*
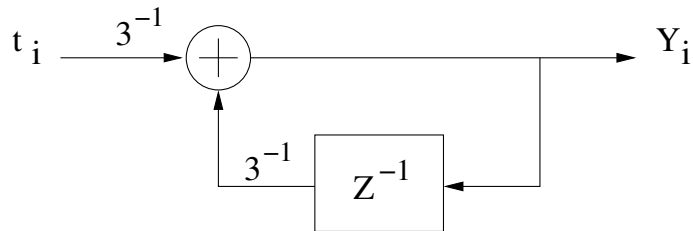
Figure 5.20: *Signal flow diagram for ternary LST-first D/A converter. Ternary input trit t_i and intermediate analog output voltage Y_i are shown.*
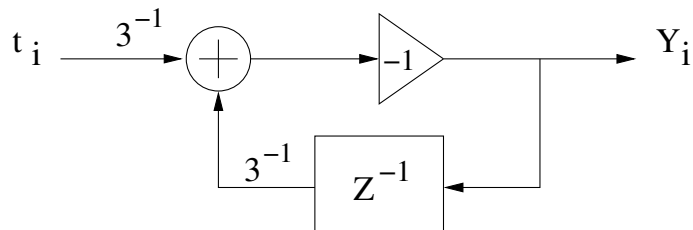
Figure 5.21: *Signal flow diagram for ternary LST-first ATI D/A converter. Ternary input trit t_i and intermediate analog output voltage Y_i are shown.*
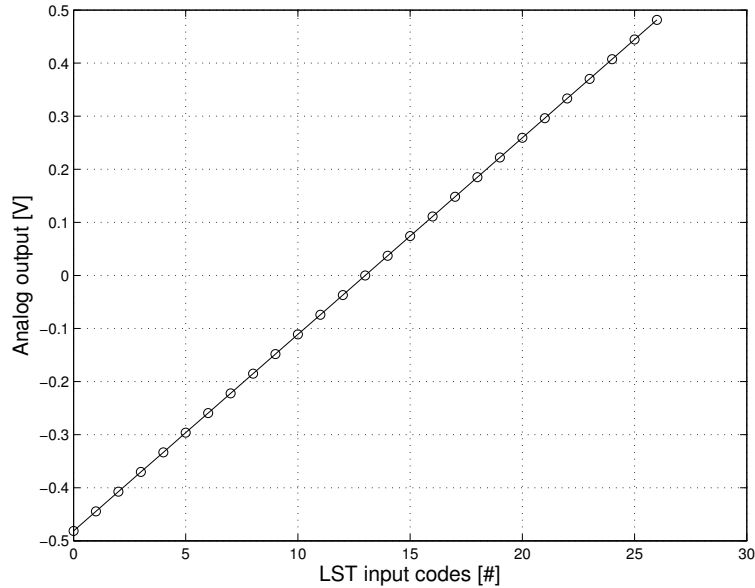
Figure 5.22: *Balanced Ternary LST-first D/A Converter using SFG devices.*

The proposed SFG based ternary D/A converters also support balanced ternary logic. This requires the initial condition $Y_0 = 0$. A balanced ternary representation is used for the LST ternary input signal: -1, 0 and 1. The application is illustrated in figure 5.22.

5.5 Summary

In this chapter a SFG serial D/A converter architecture and its components have been presented. The main focus of this thesis is the converter cores [38, 39, 41, 42, 43] **[Papers I-II,IV-VI]**. This has been presented in chapter 2 and 4. In this chapter three components, auxiliary to the converter core, are introduced: SFG MV FDIV [44] **[Paper VII]**, SFG S/H circuits [40]**[Paper III]** and SFG Ternary refresh element [45]**[Paper VIII]**. For more information on these components the reader is referred to the included publications. The measurement of the SFG ternary refresh element is included in this chapter as it has not previously been published.

Chapter 6

CONCLUSION

In this thesis it has been demonstrated that configurable multiple-valued encoders using semi floating-gate devices are feasible. Several new serial D/A converters and auxiliary circuits have been proposed for this purpose. The study of these circuits include both theoretical work using ideal Matlab models, circuit simulation in Spectre and practical implementations on a chip. SFG devices have insufficient gain to accommodate high accuracy and resolution. OTA based cyclic D/A converters are reported to have an accuracy of 10 bit or so resolution [37]. However, in this work sufficient accuracy for binary to multiple-valued conversion is demonstrated.

6.1   Configurable multiple-valued encoders

The main aim of this thesis was to introduce configurable multiple-valued encoders using semi floating-gate devices and is met in the following ways:

- by proposing new SFG serial D/A converter circuits for binary to multiple-valued radix conversion. To the knowledge of the author, this work is the first to combine SFG devices and cyclic D/A conversion algorithms. Difference equations modeling the operation and signal flow diagrams are made available.

- by developing support of standard least significant bit (LSB) first and most significant bit (MSB) first digital input codes. In addition conversion of a new LSB ABI code standard with error correction capabilities is demonstrated.

- by constructing practical implementations of the proposed LSB and LSB ABI converters. A standard digital AMS $0.35\mu m$ process was used for this purpose. The chip measurements demonstrated operation with sufficient accuracy for configurable multiple-valued encoding when using two, three

and four bit resolution. Measured results were analyzed using standard static
D/A converter performance measures.

- by proposing circuits auxiliary to the converter with performance enhancing
capabilities. A complete architecture for serial D/A conversion is provided.
This includes a configurable SFG MV FDIV for generation of the external
reset clock signal, a SFG S/H read-out circuit and a modular level restoration
circuit for suppression of level-noise in multiple-valued input signals. The
architecture supports runtime configuration of the converter output radix.
Practical implementations demonstrating the algorithms are made available
for the SFG S/H and the ternary level restoration circuits.

6.2   Optimization techniques

The range of applications for the serial D/A converter using SFG devices is
extended by improving the converter resolution and speed. These secondary
objectives are met by introducing several new techniques:

Reduction of length of MV signal path
The number of SFG device computations per conversion was found to be a
limited resource. Normally one bit resolution corresponds to one converter
cycle. A reduced number of SFG device computations per iteration therefore
means a higher accuracy or number of bit resolution. For this reason the
number of computations per iteration should be kept at a minimum. A strong
correlation was found between the INL/DNL converter measures and this
figure of merit. An optimal solution using a mere one inverter per iteration
is demonstrated. It is referred to as DAC-4 or DDR LSB D/A converter.

LSB ABI error correction
A method for reducing the gap in accuracy between SFG device based and
OTA based cyclic converters is introduced. The technique is called LSB
ABI serial D/A conversion. Converter DAC-2 demonstrates its effectiveness.
According to the chip measured results a significant improvement in accuracy
is demonstrated. DAC-2 or LSB ABI error correction competes well with the
optimal standard LSB D/A converter DAC-4, despite the fact that it uses
three non-ideal SFG computations per iteration and DAC-4 a mere one.

Dual Data-Rate (DDR) mode of operation
One problem with cyclic D/A converters is slow conversion rates. In this work
the speed of SFG D/A conversion is significantly increased by introducing a
new Dual Data-Rate (DDR) mode of operation. As a result two iterations
of the difference equation are calculated per recharge clock cycle. This is
a doubling of the speed. The method is applicable to other computational
problems as well. It is verified by chip measured results.

Improved internal memory using a SFG S/H circuit
Introduction of a new SFG S/H memory circuit with improved performance compared to the traditional SFG Latch. The SFG S/H memory was exploited in DAC-3, DAC-4 and DAC-5.

6.3 Concluding remarks

Configurable multiple-valued encoders using semi floating-gate devices are demonstrated. The circuits combine simple and compact cyclic D/A converter algorithms with compact SFG devices. As a result extremely compact solutions with minimum die area requirements are made possible. Compared to recent work in the field of radix conversion, the SFG serial D/A converters are simple, compact and support runtime configuration of the radix. Resent research on radix conversion includes LUT-cascades [6], arithmetic decompositions [7], iterated function systems [8] and linear coded weights [9]. Radix conversion is described as a complex task. Related work using semi floating-gate devices for radix conversion (D/A conversion)[16][17] utilizes the larger and less flexible parallel binary weighted conversion algorithm exclusively. Here, reconfiguration of the radix requires redesign of the converter. Slow speed is a problem with all serial D/A converters using cyclic algorithms. In this thesis a new DDR mode of operation is introduced, allowing approximately a doubling of the conversion rate. A study of converter accuracy and resolution for chip implementations has been an essential part of this work. It shows that configurable multiple-valued encoders using simple semi floating-gate devices indeed are feasible.

6.4 Further work

There are both obvious possibilities and practical boundaries emerging from this work. A brief list of topics for further work is given.

It was discovered that accuracy/resolution can be improved by use of DDR mode of operation (demonstrated in DAC-4) or the error correction scheme LSB ABI (demonstrated in DAC-2). A combination of the two algorithms has promise for even further improvement in accuracy. This new converter would have higher speed using DDR mode of operation, only two SFG inverters per iteration and LSB ABI error correction built-in. The cost in speed should be marginal compared to the fastest implementation, DAC-4, where only one SFG inverter per iteration is used. A disadvantage with this solution is the increased die area. The number of SFG inverters required for such an implementation would be four, a doubling compared to the presented

compact implementations DAC-3 and DAC-4.

Another interesting concept is the use of ternary input signals. The number of iterations is a limited resource. This motivates the use of non-binary input signals. By combining ternary input codes and the proposed converters, an increase in resolution can be achieved without increasing the number of cycles further. Recharged analog SFG inverters propagate level-noise and the number of SFG inverters in chains or number of loops in cyclic circuits should be kept at a minimum for best performance. By using a ternary input signal the resolution can be increased without adding more converter iterations. A resolution of 16 levels (4 bit) was demonstrated in this thesis. Using ternary input signals we aim at a resolution of 81 levels (4 trit).

This thesis has been mainly application and architecture oriented. From a critical perspective it should be noted that some important work remains to improve the robustness of the circuits presented. The proposals rely on the accuracy of the recharged SFG inverter [20]. It is evident that the basic building blocks[19][20] are sensitive to variations in power supply voltage and mismatch errors.

Compact circuit design was a focus in this thesis. Further reduction of the size of the converter motivates use of a more modern process. As part of further work it would have been interesting to investigate problems that occur in newer processes. This is not straightforward as analog design techniques have been utilized. It is a question of whether the reduction in supply voltage that follows is possible in a voltage-mode MVL application. It might impose an impossible strain on the noise-margins of MV signals.

Bibliography

[1] C.E. Shannon. A Mathematical Theory of Communication. *Bell System Technical Journal*, 27:379–423,623–656, July 1948.

[2] M. Kameyama. Towards the age of beyond-binary electronics and systems. *Twentieth International Symposium on Multiple Valued Logic (ISMVL)*, pages 162–166, May 1990.

[3] D. Etiemble. Why M-Valued Circuits are Restricted to a Small Niche? *Multiple-Valued Logic and Soft Computing*, 10:109–123, 2003.

[4] D. Etiemble. On the performance of Multiple-Valued integrated circuits: Past, present and future. *Proceedings of the 22nd IEEE International Symposium on Multiple-Valued Logic(ISMVL'92)*, pages 154–164, 1992.

[5] K.C. Smith. Multiple-Valued logic: a tutorial and appreciation. *IEEE Computers Vol. 21*, pages 17–27, 1988.

[6] T. Sasao. Radix Converters: Complexity and Implementation by LUT Cascades. *IEEE International Symposium on Multiple-Valued Logic (ISMVL'05)*, pages 256–263, May 2005.

[7] Y. Iguchi, T. Sasao, and M. Matsuura. On Designs of Radix Converters Using Arithmetic Decompositions. *International Symposium on Multiple Valued Logic (ISMVL)*, May 2006.

[8] J. Shimakawa and T. Saito. Cyclic D/A Converters Based on Iterated Function systems. *IEICE Trans. Fundamentals*, E.87-A(10):2811–2814, October 2004.

[9] J.J. Wikner and M. Vesterbacka. D/A conversion with linear-coded weights. *Southwest Symposium on Mixed-Signal Design (SSMSD)*, pages 27–29, February 2000.

[10] J.L. McCreary and P. Gray. All-MOS Charge Redistribution Analog-to-Digital Conversion Technique - Part I. *IEEE Journal of Solid-State Circuits*, SC-10(6):371–379, December 1975.

[11] D. Khang and S.M. Sze. A floating-gate and its application to memory devices. *The Bell System Technical Journal*, 46(4):1288–1295, 1967.

[12] P. Hasler, B.A. Minch, and C. Diorio. Floating-Gate Devices: They Are Not Just for Digital Memories Anymore. *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, 2:388–391, May 1999.

[13] S. Aunet. *Real-time reconfigurable devices implemented in UV-light programmable floating-gate CMOS.* PhD thesis, Norwegian University of Science and Technology, Norway, 2002.

[14] S. Aunet, Y. Berg, and T. Sæther. Real-Time Reconfigurable Linear Threshold Elements Implemented in Floating-Gate MOS. *IEEE Transactions on Neural Networks*, 14(5), September 2003.

[15] P.M. Kelly, T.M. Mcginnity, and L.P. Maguire. Re-Programmable MVL Circuits and Architecture to Enable Evolvable MVL Hardware. *Journal of Multiple-Valued Logic and Soft Computing*, 9(4), 2003.

[16] Y. Berg, S. Aunet, Ø. Næss, O. Mirmotahari, and M. Høvin. Binary to Multiple-Valued Recharge Converter for Multiple-Valued CMOS Logic. *IEEE European Conference on Circuit Theory and Design (ECCTD)*, September 2003.

[17] Y. Berg, Ø. Næss, S. Aunet, J. Lomsdalen, and M. Høvin. A novel floating-gate binary signal to multiple-valued signal converter for multiple-valued cmos logic. *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2:579–582, September 2002.

[18] A. Rantala, P. Kuivalainen, and M. Åberg. An 8-bit and a 10-bit low power high-speed neuron mos digital-to-analog converter in 0.04 mm2. *25th European Solid-State Circuits Conference (ESSCIRC)*, pages 310–313, September 1999.

[19] O. Mirmotahari and Y. Berg. A Novel Multiple-Input Multiple-Valued Semi-Floating-Gate Latch. *33rd International Symposium on Multiple-Valued Logic (ISMVL)*, May 2003.

[20] Y. Berg, S. Aunet, O. Mirmotahari, and M. Høvin. Novel recharge semi-floating-gate CMOS logic for multiple-valued systems. *IEEE Symposium on Circuits and Systems*, 2003.

[21] T. Shibata and T. Ohmi. A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations. *IEEE Transactions on Electron Devices*, 1992.

[22] K. Kotani, T. Shibata, M. Imai, and T. Ohmi. Clock-controlled neuron-mos logic gates. *IEEE Trans Circuits Syst II Analog Digital Signal Process*, 45(4):518–522, April 1998.

[23] T. Shibata and T. Ohmi. Neuron MOS binary-logic integrated circuits - Part I: Design fundamentals and soft-hardware-logic circuit implementation. *IEEE Transactions on Electron Devices*, pages 570–576, 1993.

[24] T. Shibata and T. Ohmi. Neuron MOS binary-logic integrated circuits - Part II: Simplifying techniques of circuit configuration and their practical applications. *IEEE Transactions on Electron Devices*, pages 974–979, 1993.

[25] M. Vesterbacka and J.J. Wikner. Design of encoders for linear-coded d/a converters. *IEEE ISCAS*, 1:524–527, May 2001.

[26] R. Suarez, P. Gray, and D. Hodges. An All-MOS Charge-Redistribution A/D Conversion Technique. *IEEE Journal of Solid-State Circuits*, XVII:194–195, 1974.

[27] R. Suarez, P. Gray, and D. Hodges. An All-MOS Charge-Redistribution Analog-to-Digital Conversion Technique – Part II. *IEEE Journal of Solid-State Circuits*, SC-10(6):379–385, December 1975.

[28] K. Watanabe, G.C. Temes, and T. Tagami. A new algorithm for cyclic and pipeline data conversion. *IEEE Transactions on Circuits and Systems*, 37(2):249–252, February 1990.

[29] M.M. Arnourah, S.Q. Malik, and R.L. Geiger. An MSB-first monotonic switched capacitor serial DAC. *Midwest Symposium on Circuits and Systems(MWSCAS)*, 1(45):I–571 – I–574, August 2002.

[30] G. Cauwenberghs. Bit-Serial Bidirectional A/D/A Conversion. *Proceedings of the 16th Conference on Advanced Research on VLSI (ARVLSI'95)*, pages 108–120, 1995. ISBN 0-8186-7047-9.

[31] M.J. Bell. An lcd column driver using a switch capacitor dac. *IEEE Journal of Solid-State Circuits (JSSC)*, 40(12):2756 – 2765, December 1005.

[32] M. Ogawa and T. Shibata. NMOS-based Gaussian-Element-Matching Analog Associative Memory. *European Solid-State Circuits Conference (ESSCIRC)*, pages 257–260, September 2001.

[33] M. Moussavi, R. Mason, and C. Plett. A differential bipolar quasi-passive cyclic digital-to-analog converter with 4.416 MSps conversion rate and -77 dB THD. *Proceedings of IEEE Custom Integrated Circuits Conference (CICC)*, pages 161–164, May 2001.

[34] S. Wang, B.B. Bhattacharyya, and M.O. Ahmad. A Novel Ratio-Independent Cyclic Multiplication D/A Converter. *Proceedings of the 35th IEEE Midwest Symposium on Circuits and Systems (MWSCAS)*, 1(35):72–75, August 1992.

[35] S. Wang, M.O. Ahmad, and B.B. Bhattacharrya. A Novel Cyclic D/A Converter. *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2:1224–1227, May 1993.

[36] H. Matsumoto and K. Watanabe. Switched-capacitor algorithmic digital-to-analog converters. *IEEE Transactions on Circuits and Systems*, CAS-33(7):721–724, July 1986. ISBN 0098-4094-86-0700-0721.

[37] H. Onodera, T. Tateishi, and K. Tamaru. A cyclic switched capacitor A-D, D-A converter. *Electronics and Communications in Japan*, 70(9):56–65, 1987.

[38] R. Jensen and Y. Berg. Serial Semi Floating Gate MOS D/A Converter With Configurable Resolution. *IEEE TENCON*, November 2004. Chiang-Mai, Thailand.

[39] R. Jensen and Y. Berg. Configurable Serial-bit D/A Converter for Multiple Valued Logic. *IEEE ICSES*, September 2004. Poznan, Poland.

[40] R. Jensen, Y. Berg, and J.G. Lomsdalen. Semi Floating-Gate S/H Circuits. *IEEE Norchip*, December 2005. Oulu, Finland.

[41] R. Jensen, J.G. Lomsdalen, and Y. Berg. Improved Serial SFG MOS D/A Converter with Configurable Resolution. *IEEE ECS*, September 2005. Bratislava, Slovakia.

[42] R. Jensen, J.G. Lomsdalen, and Y. Berg. Dual Data-Rate Cyclic D/A Converter Using Semi Floating-Gate Devices. *37th International Symposium on Multiple-Valued Logic (ISMVL'07)*, pages 37–41, May 2007. Oslo, Norway.

[43] R. Jensen, J.G. Lomsdalen, and Y. Berg. Configurable MSB-first Serial D/A Converter using Semi Floating-Gate Devices. *IEEE ICSES*, pages 697–700, September 2006. Lodz, Poland.

[44] R. Jensen, H. Gundersen, J.G. Lomsdalen, and Y. Berg. Recharged Comparator and Multiple-Valued N-ary Frequency Divider. *ULSIWS*, pages 51–54, May 2006. Nanyang, Singapore.

[45] H. Gundersen, R. Jensen, and Y. Berg. A Novel Ternary Switching Element Using CMOS Recharge Semi Floating-Gate Devices. *IEEE International Symposium on Multiple Valued Logic (ISMVL)*, May 2005. Calgary, Canada.

[46] J.W. Bruce. Nyquist-rate digital-to-analog converter architectures. *IEEE Potentials*, 2001.

[47] D.A. Johns and K. Martin. *Analog Integrated Circuit Design*. John Wiley & Sons, New York, USA, 1997. ISBN 0-471-14448-7.

[48] D.F. Hoeschele. *"Analog-to-Digital and Digital-to-Analog conversion techniques"*. John Wiley & Sons, 1994. ISBN 0-471-57147-4.

[49] B. Razavi. *"Principles of data conversion system design"*. IEEE Press, 1995. ISBN 0-7803-1093-4.

[50] P.G.A. Jespers. *Integrated Converters - D to A and A to D Architectures, Analysis and Simulation*. Oxford University Press, New York, 2001.

[51] R. Plassche. *"Integrated analog-to-digital and digital-to-analog converters"*. Kluwer international series in engineering and computer science. Analog circuits and signal processing, 1994. ISBN 0-7923-9436-4.

[52] P.E. Allen and E. Sanchez-Sinencio. *Switched capacitor circuits*. Van Nostrand Reinhold, February 1984. ISBN 0-442-20873-1.

[53] B.M. Gordon. Linear electronic Analog/Digital Conversion Architectures, Their Origins, Parameters, Limitations, and Applications. *IEEE Transactions on Circuits and Systems*, CAS-25(7):391–418, July 1978.

[54] R.J. Baker. *CMOS Circuit Design, Layout, and Simulation, Second Edition*. John Wiley & Sons, 2005. ISBN 0-471-70055-X.

[55] A. Baschirotto. Data converters and interfacing: A/d and d/a converters. Lecture at DTU, Copenhagen, Denmark, November 2002. (http://www2.imm.dtu.dk/courses/02911/lecture-plan.htm).

[56] J.J. Wikner. *CMOS Digital-to-Analog Converters for Telecommunication Applications*. PhD thesis, Department of Electrical Engineering, Linköping University, Sweden, August 1998.

[57] T. Halvorsrød, Ø. Næss, and T.S. Lande. Active floating gate circuits. *2004 IEEE International Workshop on Biomedical Circuits and Systems*, 1:13–16, December 2004.

[58] Ø. Næss, S. Aunet, and Y. Berg. Low-voltage pseudo floating-gate reconfigurable linear threshold elements. *Proceedings of IEEE International Joint Conference on Neural Networks (IJCNN)*, 2:675–680, 31 July-4 Aug. 2005.

[59] H. Gundersen and Y. Berg. A novel ternary more, less and equality circuit using recharged semi-floating gate devices. *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2006. Kos, Greece, ISBN 0-7803-9390-2.

[60] Robert H. Walden. Analog-to-digital converter technology comparison. *IEEE GaAs IC Symposium, Technical Digest*, pages 217–219, October 1994.

[61] Robert H. Walden. Analog-to-digital converter survey and analysis. *IEEE Journal on Selected Areas in Communication*, 17(4):539–550, April 1999.

[62] M.M. Mano. *Digital Design*. Prentice Hall, New Jersey, 1984. pp 282.

[63] S. Nooshabadi, G.S. Visweswaran, and D. Nagchoudhurhi. Current mode ternary d/a converter. *Eleventh International Conference on VLSI Design*, pages 244 – 248, January 1998.

List of Figures

List of Tables