Optimisation of $CdTe_{(1-X)}Se_X$ and $Mg_XZn_{(1-X)}O$ layers for CdTe PV devices

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Abstract

This thesis presents a study on the optimisation of $CdTe_{(1-X)}Se_X$ and MZO layers for CdTe PV applications. The first part of this work focused on the formation of the $CdTe_{(1-X)}Se_X$ layers using CdSe layer and its impact on solar cell performance. Initially the incorporation of CdSe layer into conventional CdS/CdTe devices was investigated. This approach was found to be detrimental to all device parameters particularly J_{SC} due to the formation of a $CdS_{(1-X)}Se_X$ phase at the CdTe/CdSe/CdS interface. This phase increased the amount of parasitic absorption observed at short wavelength, reduced PV performance, and resulted in excessive void formation at the CdTe device interface. Replacement of CdS with SnO_2 as the junction partner layer was found to increase the device photo response at both short and long wavelength due to removal of the CdS and efficient formation of the $CdTe_{(1-X)}Se_X$ phase. This resulted in increased device performance of > 13% with notably high J_{SC} values of > 29 mA cm^{-2}. However, removal of CdS did result in a reduced V_{OC} and interface voids were still present. Focus was then placed on alternative oxides to SnO_2 which could act as the device window layer but simple binary oxides tested, ZnO, TiO_2 and FTO were all found to reduce performance compared to SnO_2. The second part of this work therefore investigated MZO layers for CdTe PV. Two approaches were studied, co-sputtering from ZnO and MgO targets or sputtering from a single MZO target. The use of co-sputtered MZO layers was found to be detrimental to performance, due to the high resistivity of the layers and the formation of S-shaped *JV* curves related to interface charge accumulation. Initially use of single target MZO layers similarly resulted in S-shaped curves and poor performance however, post-growth annealing of the MZO converted the material from amorphous to crystalline and enhanced conductivity of the MZO, removing the charge accumulation. Despite the reduced overall performance compared to SnO_2, 11.3% and 13.5% respectively, the MZO devices had an improved V_{OC} demonstrating that with further optimisation of the device junction interface further improvements to performance could be achieved.

Declaration

I declare that with the exception of the procedures listed below all the work presented in this thesis was carried out by the candidate. I also declare that none of this work has previously been submitted for any degree and that it is not being submitted for any other degree.

EBIC, EBSD and STEM measurements were undertaken by Leon Bowen at the Department of Physics, University of Durham, Durham, DH1 3LE, UK.

SIMS measurements were undertaken by Dr Guillaume Zoppi at the Department of Mathematics, Physics and Electrical Engineering, Northumbria University, Ellison building, Newcastle upon Tyne, NE1 8ST, UK.

XPS measurements were undertaken by Huw Shiel at the Stephenson Institute for Renewable Energy, Physics Department, University of Liverpool, L69 7XF, UK.

Some of the work presented in this thesis has been published previously in the following publications:

- Baines, T; Durose, K; Major, J. D. Co-sputtered $Mg_{(X)}Zn_{(1-X)}O$ window layers for $CdTe_{(1-X)}Se_X$ solar cells. *in 45th IEEE specialist photovoltaics conference in Hawaii,* 2018.
- Baines, T.; Papageorgiou, G.; Hutter, O. S.; Bowen, L; Durose, K.; Major, J. D. "Self-catalysed CdTe wires" *Nanomaterials, 8,274*, 2018.
- Baines, T.; Zoppi, G.; Bowen, L.; Shalvey, T. P.; Mariotti, S; Durose, K; Major, J. D. "Incorporation of CdSe layers into CdTe thin film solar cells" *Solar Energy Materials and Solar Cells, 180, 196-204,* 2018.
- Baines, T.; Shalvey, T. P.; Major, J. D. "CdTe Solar Cells" book chapter in *A Comprehensive Guide to Solar Energy Systems,* 2018.
- Baines, T.; Zoppi, G.; Durose, K.; Major, J.D. "Use of CdS:O and CdSe as window layers for CdTe Photovoltaics" *in 44th IEEE specialists photovoltaics conference in Washington*, 2017.

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Abbreviations

AZO	Aluminium doped zinc oxide
AFM	Atomic force microscopy
V_{bi}	Built in voltage
CV	Capacitance voltage
CL	Cathodoluminescence
CBD	Chemical bath deposition
CSS	Close space sublimation
CB	Conduction band
JV	Current voltage
W	Depletion width
EBSD	Electron back scatter diffraction
EBIC	Electron beam induced current
EDX	Energy dispersive X-ray
EQE	External quantum efficiency
FF	Fill factor
FTO	Fluorine doped tin oxide
FIB	Focussed ion beam
HRT	Highly resistive transparent
IQE	Internal quantum efficiency
PV	Photovoltaic
MOCVD	Metal organic vapour deposition
MZO	MgZnO
PVD	Physical vapour deposition
QE	Quantum efficiency
SEM	Scanning electron microscopy
SIMS	Secondary ion mass spectrometry
R_S	Series resistance
R_{SH}	Shunt resistance
SLG	Soda lime glass
TCO	Transparent conducting oxide
ITO	Tin doped indium oxide
TEM	Transmission electron microscopy
VB	Valence band
XRD	X-ray diffraction
XPS	X-ray photoelectron spectroscopy

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1. Introduction

In 2017 it was estimated that ≈155000 TWh of energy was consumed globally with more than 70% of the world's energy demand coming from fossil fuels such as coal and natural gas[1]. It was also estimated that global energy demand grew by over 2% in 2018, with an increase in the amount of energy produced by fossil fuels[2]. In addition to this the amount of global CO_2 emissions increased by 1.7%, far above those required to meet the objectives set by the Paris agreement on climate change in 2015[3,4], where it was negotiated that by 2020 the average global temperature shouldn't rise by more than 2°C. In order to meet the Paris agreement requirements there needs to be a substantial reduction in global carbon emissions and fossil fuels need to be replaced with cleaner more sustainable alternatives. The use of renewable energy has continually risen with over 20% of the world's energy[2] now coming from renewable sources such as solar, wind and hydroelectric. However, for the worlds energy supply to become completely carbon neutral the use of renewable energy, particular solar, needs to be increased.

Solar cells or photovoltaics (PV) have the potential to meet a large proportion of the world's energy needs as the total energy from solar radiation reaching the Earth is over 7000 times the planet's total energy consumption. In 2010 it was estimated that covering 1% of the land area on the Earth's surface with 10% efficient solar cells would produce twice the energy currently needed[5]. As a result, solar is seen as one of the most promising forms of renewable energy. Traditionally the price of solar held back its mass scale adoption but, in recent years the price has dropped significantly, to the point where it is now competitive with more established technologies like coal and natural gas[6]. For PV to become the "go to" technology for energy production, further reductions in price are still required.

1. Introduction

Currently the PV market is heavily dominated by silicon solar cells with over a 95% global market share[7]. Silicon has established itself as the market leader primarily due to Si manufacturing being well established in the electronics industry and the abundance of Si. Currently Si solar cells have reached lab and module efficiencies of 26.7% and 24.4% respectively[8]. Despite achieving this high performance Si has a number of inherent technological limitations such as an indirect bandgap, low absorption coefficient and the expensive purification costs required for a high PV performance[9]. Due to the limitations of Si a range of alternative technologies have been investigated as a replacement. In particular thin film technologies such as CdTe have been heavily investigated in the last 30 years. Currently CdTe solar cells represent a 4% PV market share but with a single company, First solar accounting for the majority of that, CdTe solar cells have now recorded lab and module efficiencies of 22.1% and 18.6% respectively[8].

The key advantage of CdTe as a PV absorber compared to Si is that it has a direct bandgap at approximately 1.5 eV[9], enabling a high optical absorption coefficient coupled to a near optimal bandgap[9]. This means that unlike in Si significantly less material is required for sufficient optical absorption in CdTe PV devices, < 2 μm compared to 200 μm for Si, significantly reducing material and cell production costs. The performance of CdTe devices remains significantly lower than the theoretical maximum, ≈ 30%, and in order for CdTe devices to have a larger market share further improvements to device performance will be required.

In the past 6 years the performance of CdTe PV devices has improved significantly from 16.5% to 22.1%, this improvement was after a prolonged period of stagnation[8,10]. This increase in efficiency has been largely due to the incorporation of Se into the CdTe layer forming the $CdTe_{(1-X)}Se_X$ phase and the removal of CdS as the device window layer. Both of these led to substantial increases to device photocurrent which is now close to the optimal value. This thesis will focus on aspects of how improvements to device photocurrent have

been achieved and investigate the development of new device architectures for CdTe PV. The use of selenium in CdTe PV devices remains relatively unexplored and its exact role in the current enhancement in CdTe device requires further investigation, it will be demonstrated that the use of Selenium can improve device photocurrent however, a reduction to device photovoltage was also observed. It has also proven challenging to replace CdS as the device window layer without compromising performance, particularly voltage. Whilst there have been a few reports of a high device performance achieved using MgZnO (MZO) as the partner layer, replication of these results has proven challenging. In this thesis the optimisation process for device quality MZO, along with the optimisation process for $CdTe_{(1-x)}Se_x$ layers will be presented and an improvement to both device photocurrent and voltage will also be presented. This thesis will present the complete optimisation study of what at the start of this work was a novel device structure, $MZO/CdTe_{(1-x)}Se_x$, and is now becoming the adopted device structure in the CdTe PV community. The work on Selenium and MZO incorporation into CdTe devices was at the start of this work novel and a lot of the work presented in this thesis was conducted in parallel with other research groups and helped contribute to the growing body of work on these topics.

1.1. References

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2. Photovoltaic devices

2.1. Introduction

Solar cells or PV devices, convert solar radiation into electrical energy, via the photovoltaic effect. The photovoltaic effect was first demonstrated in 1839 by Becquerel[1], who observed a photocurrent produced by light incident upon an electrolyte solution. However, the first modern solar cell wasn't developed until 1954, when a 6% efficient silicon based device was produced by Chapin, Fuller and Pearson at Bell labs[2]. Today the world record for single and multi-junction solar cells stands at 29.1% and 46%, respectively[3].

The photovoltaic effect is a process that generates power in a photovoltaic device when exposed to solar radiation. It principally involves two steps: firstly, an incident photon excites an electron from the valence band across the bandgap to the conduction band, creating an electron-hole pair. In order for electron-hole pairs to be generated, the incident photon's energy must be larger than the semiconductor's bandgap ($hv > E_g$). The second part of the process involves the generated electron-hole pairs being separated by an electric field and collected before they recombine, for a photocurrent to be produced.

The focus of this thesis is on the fabrication and characterisation of PV devices. Therefore, this chapter will outline some of the theoretical aspects that are essential for understanding PV devices. The basic principles of semiconductors will also be briefly discussed, for a more in-depth discussion on semiconductor physics the reader is directed towards the textbooks by Sze and Lee[4] and Yu and Cardena[5]. Section 2.2 will discuss the types of semiconductor junctions that are commonly present in CdTe solar cells and the fundamentals of solar cell devices including device characteristics and performance losses (Section 2.4). The different types of solar cell technologies will also be presented (Section 2.5).

2.2. Semiconductors and semiconductor junctions

2.2.1. Semiconductors

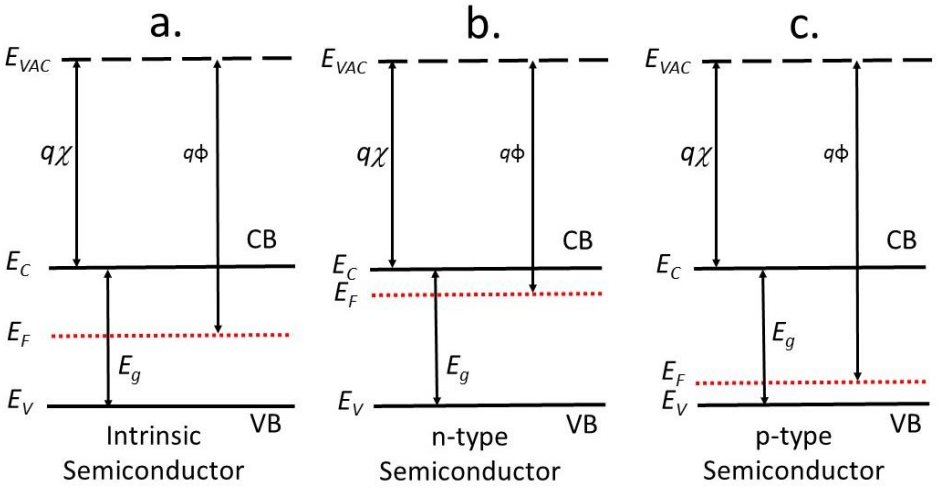

Figure 2.1: *Electronic band diagram for an intrinsic (a), n-type (b) and p-type (c) semiconductor. Where ϕ is the work function, χ is electron affinity, E_{VAC} is the vacuum level, E_F is the Fermi level, E_g is the bandgap energy, E_C is the conduction band minimum and E_V is the valence band maximum.*

Semiconductors are a class of materials which have electrical conductivity and resistivity properties which lie between those of a conductor and an insulator. The conductivity of a semiconductor material depends on the impurities and/or dopants, in principle there exists three basic types of semiconductors, intrinsic, n-type and p-type. The electronic band diagram for the three different types of semiconductors is shown in Figure 2.1, where ϕ is the work function, χ is electron affinity, E_{VAC} is the vacuum level, E_F is the Fermi level, E_g is the bandgap energy, E_C is the conduction band (CB) level and E_V is the valence band (VB) level. In an intrinsic semiconductor the concentration of electrons in the CB and holes in the VB is equal.

There exists two different type of dopants in semiconductors native and extrinsic. Dopants can act as either acceptor where holes are added to the VB, shifting the Fermi level towards the VB introducing p-type conductivity or donors where electrons are added to the CB, shifting the Fermi level to the CB introducing n-type conductivity (Figure 2.1b).

Native doping arises from point defects in the material such as vacancies and interstitials and extrinsic dopants arises when impurities are added to semiconductor such as boron into silicon. For example, the addition of donor impurities into the material, e.g. group 5 elements like phosphorus are used for doping Si, leads to the formation of donor levels (E_D) close to the CB and shifts the Fermi level closer to the conduction band making the material n-type (Figure 2.1b). Conversely, the addition of acceptor impurities, e.g. group 3 elements like boron are used for doping Si, leads to the formation of acceptor levels (E_A) close to the VB and shifts the Fermi level closer to the valence band, making the material p-type (Figure 2.2c).

2.2.2. Semiconductor junctions

For photo generated carriers to be separated in a solar cell, an electric field must exist in the device. An electric field is typically established by the formation of a semiconductor junction. In a CdTe solar cell there typically exists three basic types of semiconductor junctions, metal-semiconductor junctions (Schottky and Ohmic), homojunctions and heterojunctions, these junctions will be discussed in the following sections. The basic properties of semiconductor junctions will be presented in this thesis. For more in-depth discussion, the reader is directed to the books by Sze and Lee[4] and Nelson[6].

2.2.2.1. Metal-semiconductor junction

A metal semiconductor interface can behave either as an Ohmic contact or as a Schottky junction, depending on the electronic properties of the materials. Figure 2.2a shows a metal and a p-type semiconductor band structure before contacting, the Fermi levels are independent of each other. When the two materials are brought into contact the Fermi levels must line up so that no transfer of charge exists under equilibrium and an electric field is established, as a result the vacuum levels also shift because the vacuum level and electron affinity for a material is always constant (Figure 2.2b). The amount the

vacuum level and Fermi level shift is dependent on the difference between the work function values of the metal and semiconductor.

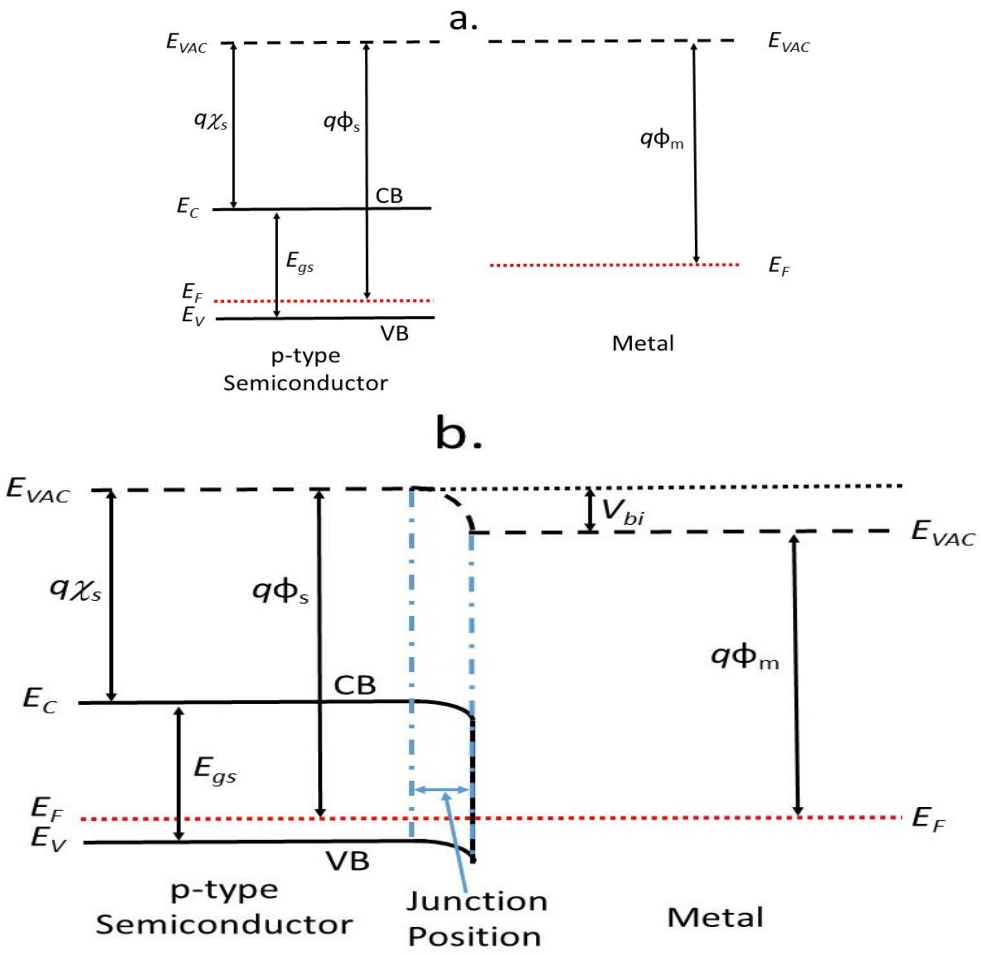

Figure 2.2: *Electronic band structure for a p-type semiconductor and metal before (a) and after contacting (b), showing a Schottky junction. V_{bi} is the built-in potential. Where $\phi_m < \phi_s$.*

In order for a Schottky barrier to be produced, the work function of the metal must be lower than the work function of the p-type material, $\phi_m < \phi_s$. When the materials are brought into contact, electrons flow from the metal to the semiconductor, leaving a positive charge on the metal and a negative charge in the semiconductor. This process continues until a sufficient charge gradient is established and equilibrium is reached. The energy of the valence band in the semiconductor bulk is higher than at the metal-semiconductor interface meaning an electrostatic field is generated. The variation in electrostatic potential is represented by the change in E_{VAC} and the electrostatic field by the

gradient of E_{VAC}. Due to metals much higher conductivity, screening length and dielectric constant compared to the semiconductor, virtually all the potential difference is dropped across the semiconductor, until equilibrium is reached, and the potential difference and electric field become zero.

The region where the potential difference occurs carries a net charge, this space-charge region of the junction is assumed to be depleted of carriers and is generally referred to as the depletion region. The depletion region relates to the area where E_{VAC} is changing and because the electron affinity and bandgap in the semiconductor are constant, the conduction and valence bands must change in parallel with E_{VAC}. This is referred to as band bending. The total amount of band bending in the semiconductor is related to the differences in work function between the metal and semiconductor and gives the built-in potential in the junction (V_{bi}), see Figure 2.2b.

The field created when these materials are brought into contact will drive holes to the left and electrons to the right, presenting a lower restive path for electrons from the semiconductor to the metal, a Schottky barrier. The Schottky barrier in Figure 2.2.b is designed to promote the transfer of electron across the junction. However, it provides an extraction barrier to hole transport. Therefore, this kind of junction would not be beneficial for solar cells as it only promotes the transfer of one type of carrier. An equivalent situation applies when contacting an n-type material to a metal however, the metals work function should be larger than the work function of the semiconductor (i.e. $\phi_m > \phi_S$).

It is possible to design a metal-semiconductor junction that promotes the transport of majority carriers across the junction i.e. holes in a p-type material. If a p-type material is contacted to a metal with a higher work function, $\phi_m < \phi_P$, now the semiconductor bands will bend upwards so as to encourage the transport of majority carriers across the interface (Figure 2.3). This means that current can pass easily in both directions establishing a low resistive contact for majority carriers known as an Ohmic contact.

An Ohmic contact is desirable for high efficiency devices, However for p-type materials with high electron affinities and work functions like CdTe (≈ 4.4 eV and 5.7 eV respectively) it can be particularly challenging as no low cost metal exists with such a high enough work function[7,8]. A pseudo-Ohmic contact can be created by heavily doping the semiconductor at the near interface region, so that carriers can tunnel through the barrier. In CdTe devices Ohmic contacts are usually made by heavily doping the back surface typically with Cu, more information on the formation of an Ohmic contact in CdTe devices can be found in Section 3.3.4[9].

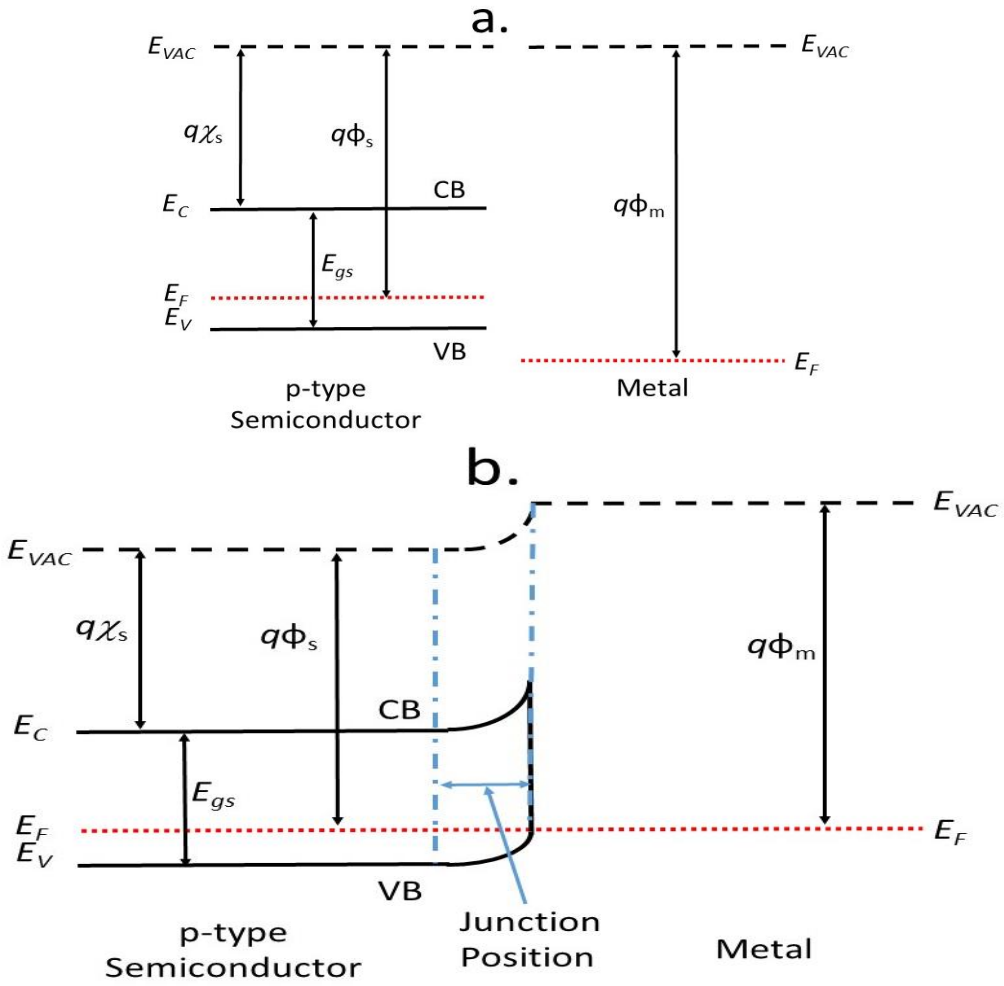

Figure 2.3: *Electronic band structure for a p-type semiconductor and a metal before (a) and after (b) contacting showing an Ohmic contact. Where* $\phi_m > \phi_s$.

2.2.2.2. Homojunction

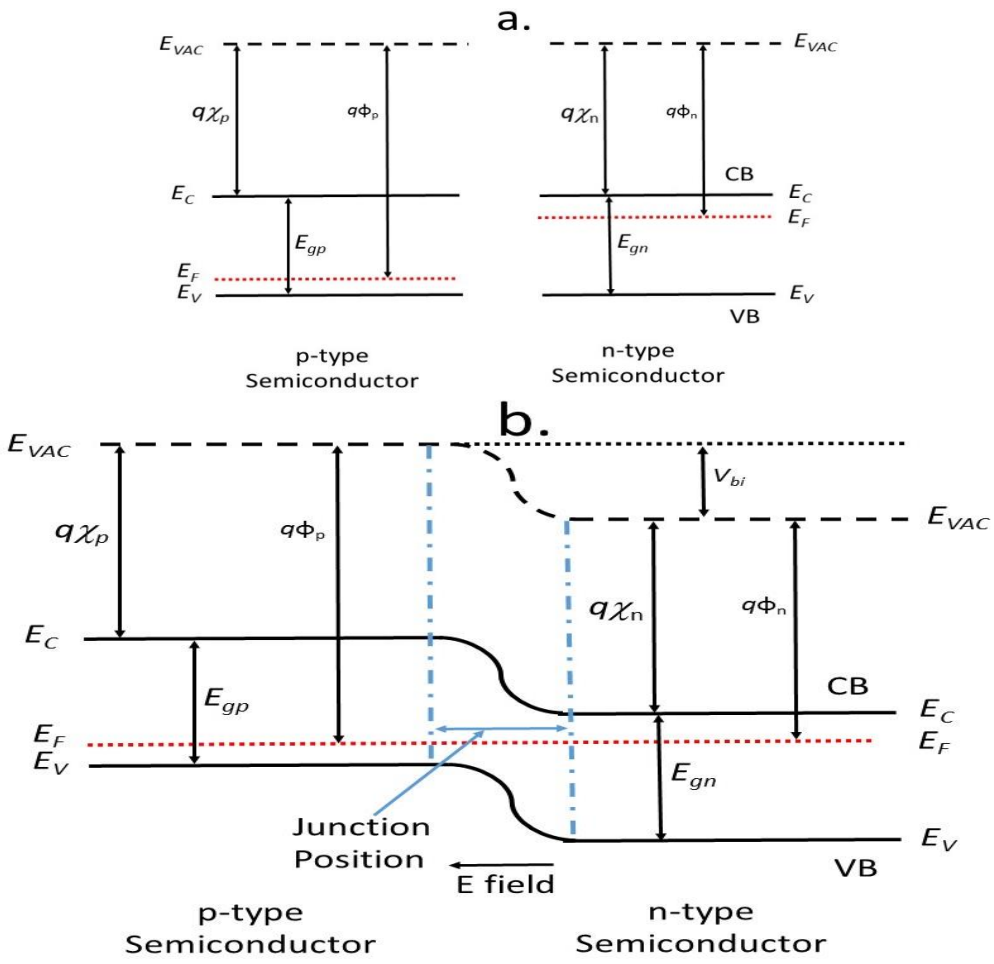

Figure 2.4: *Electronic band structures for p and n type semiconductor before (a) and after (b) contacting, showing a typical homojunction.*

A p-n junction is the most common type of junction in PV devices. The junction is formed when a p-type and an n-type material are brought into contact and the Fermi levels are aligned. A p-n homojunction is the simplest type of junction to form as it is created by doping the same semiconductor (e.g. silicon) differently, both p and n-type. As a homojunction is formed between materials with the same bandgap no barrier will exist to minority carrier transport which is beneficial for solar cell applications. When the junction is formed, an electrostatic potential is created which drives the collection of minority carriers, i.e. photo generated electrons are driven towards the n-type side and holes towards the p-type side due to the electric field that has been established where a positive

charge exists on the n-type side and a negative charge exists on the p-type side of the junction. Similar to the Schottky junctions the junction, region is depleted of carriers and provides a barrier to majority carrier transport.

Due to its ease of doping and indirect bandgap, a p-n homojunction is the basis of Si solar cells, the most widely used PV technology. However, the use of a homojunction for materials with higher absorption coefficients is challenging. In direct bandgap materials most of the absorption is close to the surface and homojunctions produced using these materials suffer from excessive surface recombination. Therefore, materials with high absorption typically utilise a p-n heterojunction structure.

2.2.2.3. Heterojunction

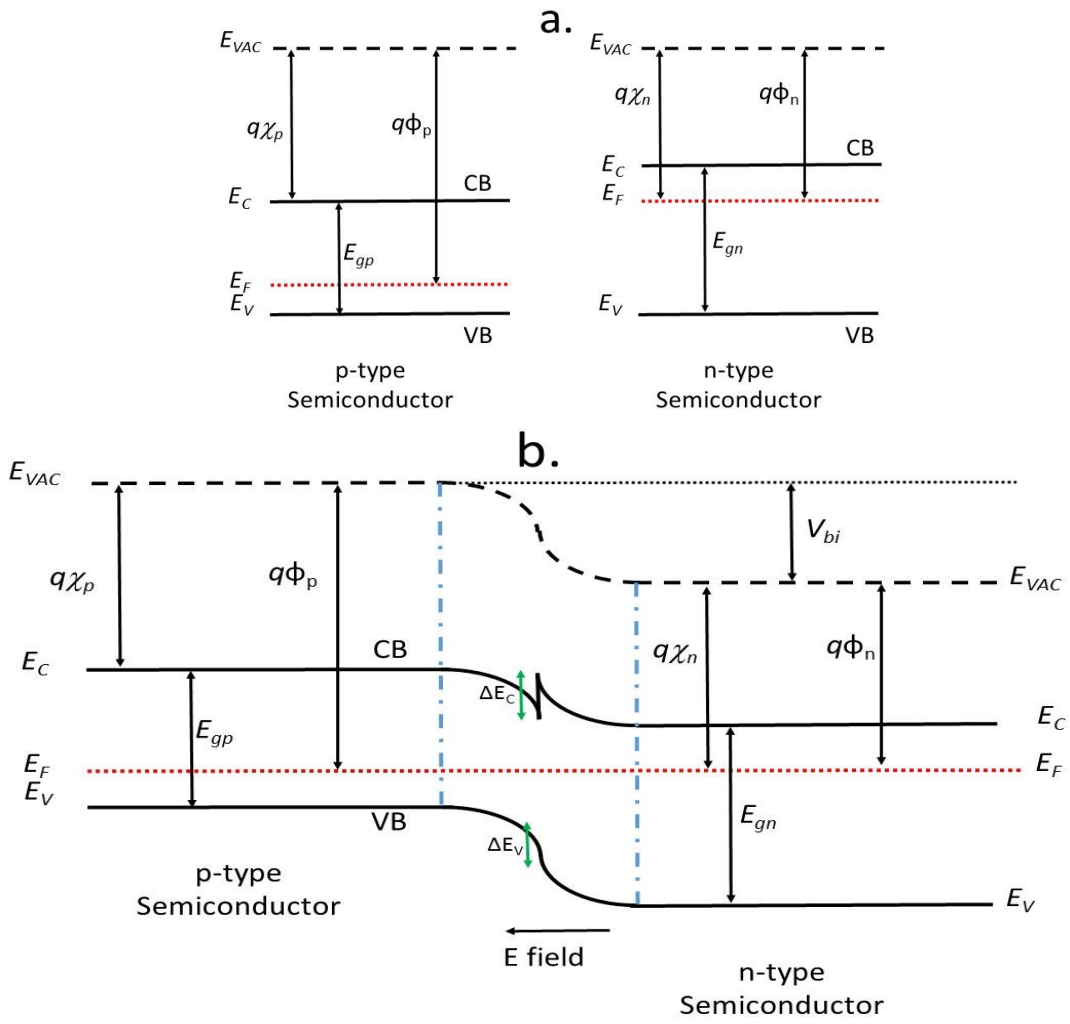

Figure 2.5: *Electronic band structure of a p-type and n type semiconductor before (a) and after (b) contacting demonstrating a typical heterojunction.*

Heterojunctions are formed between separate p and n-type semiconductor materials that typically have different bandgaps. The energy band alignment is determined by the Anderson model[10], where the vacuum level of the materials is aligned then the difference in Fermi level, conduction band minimum and valence band maximum are then evaluated. Due to the difference in bandgap when the Fermi levels are aligned there will be discontinuities in the conduction band and valence band, known as the CB or VB offsets[11]. Figure 2.5 shows the electronic band diagram for a typical heterojunction. In the example presented in Figure 2.5, the heterojunction enhances the field driving holes to the p-type side and opposes the field for electrons as a barrier has been introduced in the conduction band. Barriers are common in solar cell heterojunctions and can lead to an enhanced recombination. However, by carefully selecting the right partner layers, the barrier height can be small. The exact band alignment and barrier heights will depend on the materials' electron affinities, work function and bandgap[11].

When heterojunctions are used in solar cells there is typically an n-type window layer through which illumination occurs, with a large bandgap Eg_n and p-type absorber layer Eg_p, with a lower bandgap. This structure allows incident photons with energy below that of the window layer bandgap ($hv < E_{gn}$), to reach the absorber layer generating carriers near the junction region. This eliminates the need for the junction to be positioned near the surface and avoids surface recombination.

2.2.2.3.1. Band alignments in heterojunctions

As mentioned previously, in a PV heterojunction when the materials are brought into contact and the Fermi levels align, a CB and VB offset will exist at the interface. It is important when designing this kind of interface to consider what impact these offsets will have on the interface and how they will affect carrier transport[11]. The CB and VB offset can be designed in such a way so that the interface is either 'cliff' like (Figure 2.6a), where no

barrier exists to carrier transport or 'spike' like (Figure 2.6b) where a small barrier exists in the CB or VB.

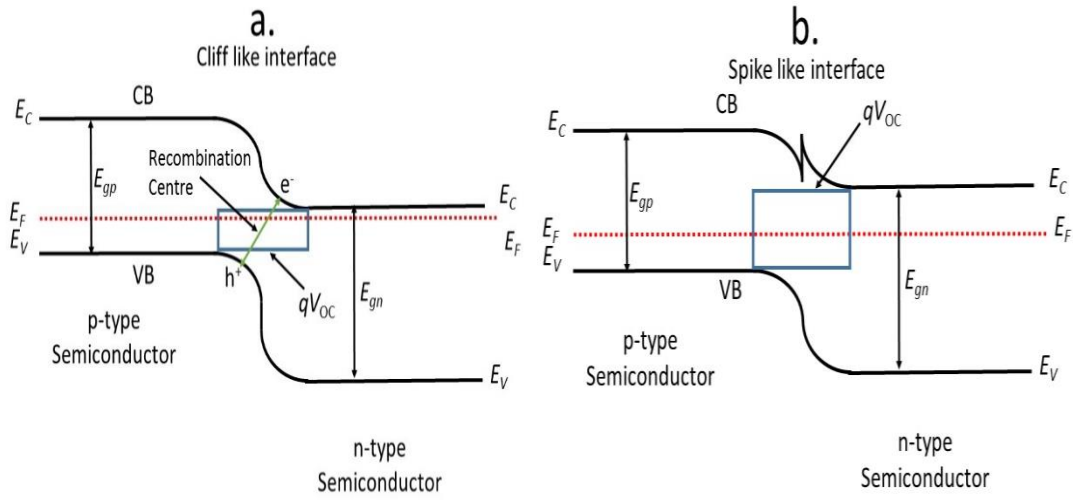

Figure 2.6: *Band diagram for a p-type and n-type heterojunction showing (a) cliff like and (b) spike like interfaces.*

Initially it would seem that the cliff like interface would be more ideal for PV devices as this presents no barrier to carrier transfer. However, it has been observed that for a p-type absorber such as CdTe, a spike offset in the CB such as the one shown in Figure 2.6b gives the best PV device performance provided the CB offset is within the range of 0.1 - 0.3 eV[11–14]. The small electron barrier means that the electrons can either tunnel across the interface or will have enough thermal energy to overcome the barrier.

It has also been observed that a cliff like interface reduces the built in potential and reduces the gap between the VB of the p-type material and CB of the n-type material increasing recombination and reducing device voltage[13]. It has also been demonstrated that a spike in the CB increases the amount of band bending at the near interface region compared to a cliff interface which provides a barrier to holes at the interface and creates an inversion layer at the near interface region in a p-type material[13]. This inversion layer means that minority carriers now become majority carriers and the recombination rate is significantly reduced leading to an increased device voltage. However, if the CB offset becomes too high, > 0.4 eV, electrons can no longer overcome it and device photocurrent

will be significantly reduced[11]. Figure 2.7 shows a modelled CdTe interface that shifts from a cliff like interface to a large spike like interface[12]. It is essential to choose the optimal partner layer when designing a heterojunction solar cell otherwise a low performance will be achieved.

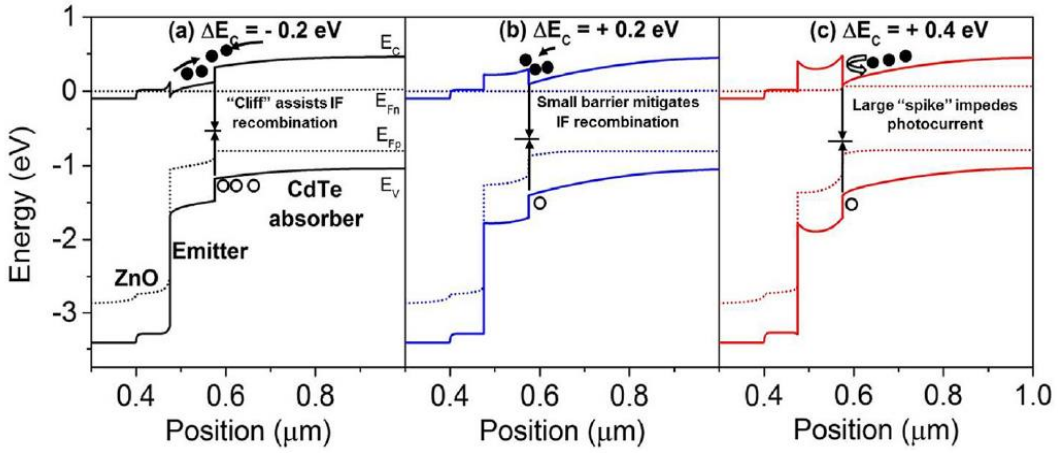

Figure 2.7: *Simulated band diagram for a CdTe heterojunction with a (a) cliff interface, (b) a small spike interface and a (c) large spike interface taken from ref[12]. Where IF is the interface recombination.*

2.3. Depletion region capacitance and capacitance-voltage analysis

Assessing the solar cell junction capacitance is important to analyse the junction quality electrostatic potential and the V_{bi}. As well as this a capacitance-voltage (*CV*) measurement is also a key characterisation tool for PV devices, using *CV* analysis a number of properties of a solar cell can be identified such as V_{bi}, doping density (N_A) and depletion width. This section will outline the basic principles of a p-n junction capacitance, *CV* analysis and the *CV* characteristics for a CdTe solar cell[15].

A p-n junction, comprises of p-type, n-type and depletion regions that can be assumed to act as a parallel-plate capacitor due to the opposite charge separated by the junction. In order for this to be valid a number of assumptions needs to be made:

i. The depletion region is entirely depleted of mobile carriers,

ii. The bulk region is electrically neutral; and

iii. The boundary between these two regions is sharp (i.e. no band bending) and therefore defines the boundary of the depletion width (W_d).

In addition to this, the charge distribution across the junction is assumed to be linearly graded. For an abrupt junction (i.e. no band bending), solving Poisson's equation allows for determination of the depletion region width (W) in relation to the doping level and permittivities of the semiconductor using Equation 2.1:

$$W = W_n + W_p = \left[\frac{2\varepsilon_0 V_{bi}(\varepsilon_n N_D + \varepsilon_p N_A)}{q\varepsilon_n N_A N_D}\right]^{\frac{1}{2}} \quad \textbf{Equation 2.1.}$$

where ε_0 is the free space and ε_n and ε_p are relative permittivities of the n and p-type materials respectively, q is the electronic charge, W_n and W_p is the depletion width on the n-and p-type sides respectively, N_A and N_D are the doping concentrations in p and n-type sides of the junction respectively and V_{bi} is the built in voltage. In equation 2.1, is it assumed that the depletion region is two sided (i.e. in the n-type and p-type components). However, it is often the case that in a solar cell junction one side is doped much higher than the other, meaning a one-sided depletion region will form as the net charge must be equal on both sides of the depletion region[16]. Therefore, the potential difference across the more highly doped material is negligible compared to the lower doped material. In CdS/CdTe solar cells for example, the doping concentration of CdS is orders of magnitude higher than in the CdTe layer, ≈ 10^{17}-10^{18} cm^{-3} and 10^{14}-10^{15} cm^{-3} respectively[17]. In this case, we may use a one-sided junction approximation where it is assumed the depletion region exists solely in the CdTe layer, allowing Equation 2.1 to be approximated to:

$$W = \left[\frac{2\varepsilon_p \varepsilon_0 V_{bi}}{qN_A}\right]^{\frac{1}{2}} \quad \textbf{Equation 2.2.}$$

If an external voltage, *V*, is applied to the junction the depletion width is varied and calculated as follows:

$$W = \left[\frac{2\varepsilon_p\varepsilon_0(V_{bi}-V)}{qN_A}\right]^{\frac{1}{2}} \quad \textbf{Equation 2.3.}$$

If a forward bias, + ve, is applied to the junction, carriers are injected into the depletion width, which lowers the depletion width. The opposite it true under reverse bias, - ve, where the depletion width increases. The junction's capacitance is related to the depletion width and calculated using Equation 2.4:

$$C = \frac{\varepsilon_p\varepsilon_0 A}{W} \quad \textbf{Equation 2.4.}$$

where *A* is the area of the device. Using Equation 2.3 and 2.4 the junction capacitance can be calculated in relation to the applied external bias using the equation:

$$C = \left[\frac{\varepsilon_p\varepsilon_0 A q N_A}{2(V_{bi}-V)}\right]^{\frac{1}{2}} \quad \textbf{Equation 2.5.}$$

By rearranging Equation 2.5 to Equation 2.6 and measuring the capacitance as a function of applied voltage, both N_A and V_{bi} can be determined from the slope and intercept of the line resulting from a $1/C^2$ vs external voltage (*CV*) Mott-Schottky plot.

$$\frac{1}{C^2} = \frac{2(V_{bi}-V)}{\varepsilon_p\varepsilon_0 A q N_A} \quad \textbf{Equation 2.6.}$$

Using Equation 2.4, it is also possible to calculate the depletion width from the measured capacitance. It is also possible to calculate the doping density and depletion width as a function of applied voltage to see how the doping density changes by varying the width of the depletion layer. More information on depletion capacitance and *CV* can be found in the book by Blood and Orten[18].

In order for the *CV* measurement to accurately measure doping density profile a number of assumptions must be satisfied:

i. The space charge in the depletion region originate only from ionised shallow levels and there is a negligible contribution to the space charge from deep levels;

ii. Only one junction exists in the device, in a p-n junction the contacts must be Ohmic; and

iii. The semiconductor must be thicker than the depletion region so that a quasi-neutral region exists.

In solar cells based on Si, the above condition can be easily satisfied. In thin film technologies violation of these assumptions occurs more often and deviations from the expected *CV* behaviour can occur. This is particularly true in the case of CdTe devices for several reasons. i) In CdTe, a large amount of deep levels may exist and contribute to the space charge region, ii) forming an Ohmic contact at the back contact can be particularly challenging due to CdTe high work function and low doping density and iii) CdTe devices can be sufficiently thin so that the entire layer may be fully depleted, making analysis of the junction complex in the reverse bias as the depletion region approaches film thickness[16,17,19].

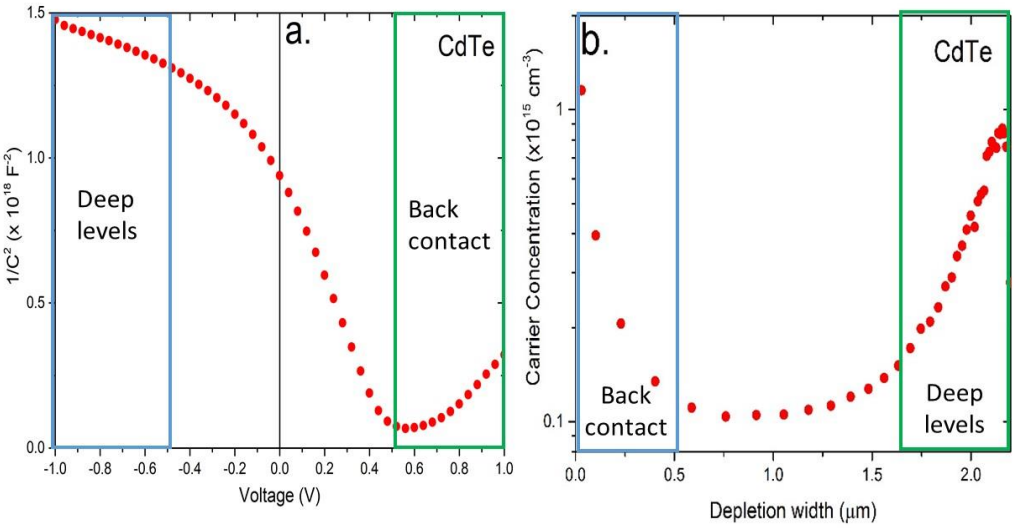

Figure 2.8: *(a) Shows a typical $1/C^2$ vs V (CV) plot for a typical CdTe devices and (b) doping density – depletion width plot for the same CdTe device.*

Figure 2.8a shows a typical $1/C^2$ as a function of V plot generated for a CdTe device and Figure 2.8b shows a typical doping density – depletion width profile generated for a typical CdTe device. In an ideal situation where no deep levels exist in the semiconductor and the contacts are assumed to be Ohmic. The $1/C^2$ should be linear in the forward and reverse bias regions and the doping density profile should be constant throughout or should show gradual changes independent of bias level throughout the entire depletion region regardless of the applied potential. However, in CdTe devices a characteristic "U-shape" is widely observed (Figure 2.8b), indicating the CdTe device is not following the assumptions made[17]. The left branch of the U-shape corresponds to the high forward bias regime however, the apparent doping increase is due to capacitance changes due to the non-Ohmic back contact (Schottky junction). As a forward bias is applied to the p-n junction a reverse bias is applied to the back contact junction therefore, as the device p-n junction narrows the back contact junction widens. As the back contact field widens the voltage drop across the back contact becomes non-negligible, compared to the voltage drop across the p-n junction, causing a voltage sharing effect and reducing the overall measured capacitance leading to the false increase in the doping profile[17,19]. The right branch of the U-shape (Figure 2.8b) corresponds to the high reverse bias regime. CdTe has a large amount of deep levels which are less efficiently ionised than shallow levels due to their high activation energy. Consequently, the Fermi level sits lower in the bandgap than the deep level, leaving them unoccupied. In the quasi-neutral region little band bending occurs and the separation between the Fermi level and valence band is constant. In the depletion region however, a large amount of band bending occurs which increases the separation between the valence band and the Fermi level. This results in the deep levels' position falling below the Fermi level and becoming occupied meaning the apparent doping density is greater than the actual doping density. At even higher reverse biases, the amount band bending increases, as the depletion region increases resulting in more deep levels

becoming occupied and further increases in the apparent doping density. It also worth noting that, as the reverse bias increases, the depletion region approaches the CdTe film's thickness and the CdTe layer becomes fully depleted and contacts the metal. Due to the large carrier density of the metal (≈ 10^{23} cm^{-3}), any further increases in the reverse bias will cause the depletion region to extend into the n-type side. Due to the higher carrier concentration of CdS and transparent conducting oxide (TCO) (≈ 10^{17}-10^{20} cm^{-3}), the apparent doping density will increase sharply as the depletion width approaches the film thickness[16]. More information of CV profiling in CdTe devices can be found in Refs 18 and 19[16,17].

2.4. Fundamentals of solar cells

In this section the equivalent circuit of an ideal solar cell will be presented, along with the current voltage behaviour and losses due to non-ideal devices. For additional discussion on PV device physics, the reader is directed to the books by Nelson[6] and Würfel[20].

2.4.1. Current density-voltage characteristics

Current density-voltage (*JV*) analysis is the standard characterisation technique used to determine a solar cell's efficiency. The current produced by the solar cell is measured as a function of applied bias in either the dark or under illumination. In addition to the device efficiency, the standard device performance parameters such as fill factor (*FF*), open circuit voltage (V_{OC}) and the short circuit current density (J_{SC}) are determined from the *JV* measurement under standard illumination (1000 W m^{-2}, AM 1.5 spectrum at 25°C). This section will describe an ideal device and how the device parameters from the *JV* curve are determined.

2.4.1.1. Ideal device

The equivalent circuit diagram for an idealised solar cell is shown in Figure 2.9. The circuit consists of a diode representing the pn junction (J_D), a current source equivalent to illumination connected in parallel (J_L) and series and shunt resistances, R_S and R_{SH}, to account for resistivity of the layers and leakage current respectively. In an ideal device, the resistances are assumed to have no impact on device performance and therefore that R_S = 0 and $R_{SH} = \infty$.

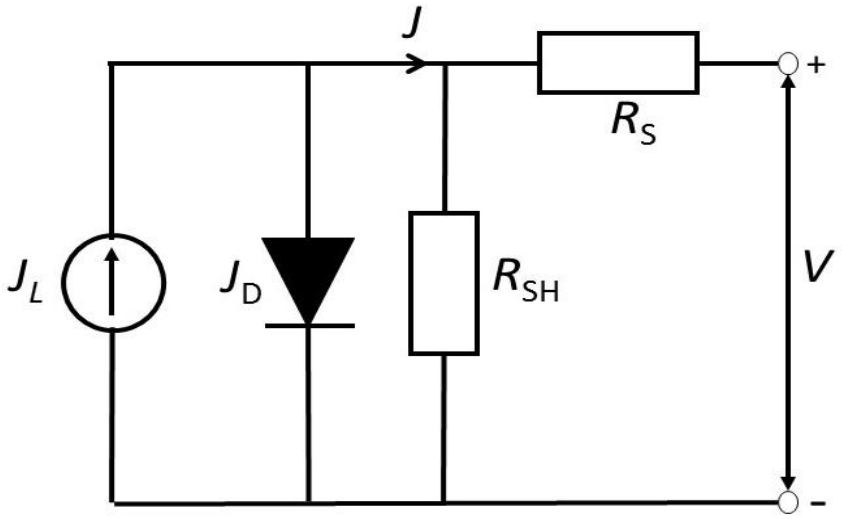

Figure 2.9: *Equivalent circuit for an ideal solar cell, where J_D is the dark current diode, J_L is the light generated current, R_{SH} is the shunt resistance and R_S is the series resistance.*

For an ideal device under dark conditions, the diode current, J_{dark}, may be determined and its *JV* response is described by the Shockley diode equation:

$$J_{dark} = J_0(e^{\frac{qV}{nKT}} - 1) \qquad \textbf{Equation 2.7.}$$

where J_0 is the reverse saturation current, *V* is the voltage applied across the diode, *k* is Boltzmann's constant, *T* is the temperature and *n* is the diode ideality factor. The ideality factor is a measure of the junction and device quality and is related to the current transport mechanism in the junction and in the bulk of the device and has a value between 1 and 2. When the device is placed under illumination, a light generated term (J_L) is added to Equation 2.7:

$$J = J_{dark} - J_L \qquad \textbf{Equation 2.8.}$$

$$J = J_0(e^{\frac{qV}{nKT}} - 1) - J_L \qquad \textbf{Equation 2.9.}$$

Typical light and dark *JV* curves for a solar cell device are shown in Figure 2.10 which can be represented by plots of Equations 2.7 and 2.9. The standard device performance parameters are marked on the light curve, J_{SC} and V_{OC}, along with the maximum power points, P_{MP}, J_{MP} and V_{MP}.

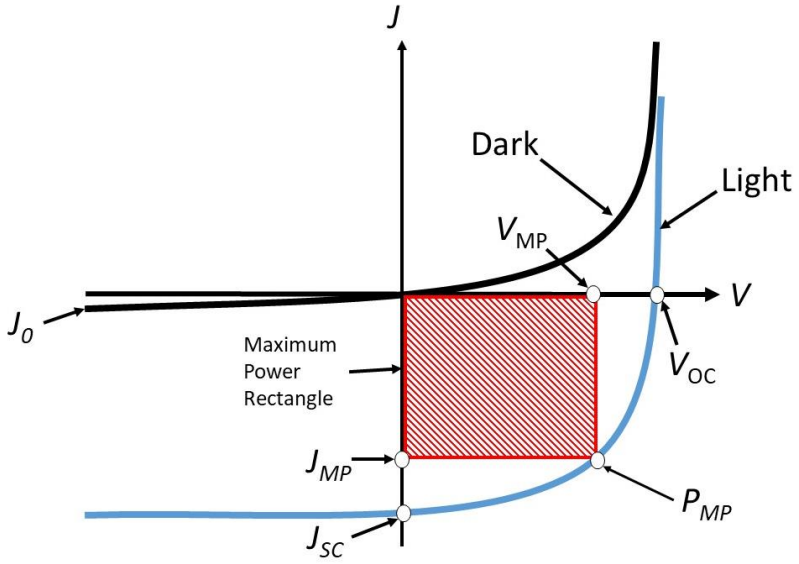

Figure 2.10: *JV curves produced by PV devices under dark and under illumination conditions. Where J_{SC} is the short circuit current density, J_0 is the dark saturation current and V_{OC} is the open circuit voltage. P_{MP} is the maximum power point with J_{MP} and V_{MP} the current and voltage values at the maximum power point.*

2.4.1.2. Solar cell parameters

Assessment of *JV* curves both in the dark and under illumination is a key test of cell quality. Several performance parameters can be extracted from the *JV* curves which are discussed below. Losses associated with these parameters are discussed in Section 2.4.3.

a) Short circuit current density

J_{SC} is the current density generated by the device in mA cm^{-2} when no bias is applied and is the intercept of the y-axis in Figure 2.10. Using Equation 2.8 when no bias is applied (V = 0) the J_0 term equals zero and the short circuit current density is equal to the J_L term.

b) Open circuit voltage

The open circuit voltage (V_{OC}) is the value of the applied voltage when no current flows through the circuit, measured in volts, and is the maximum voltage the device can deliver. It can be determined from the x-axis intercept in Figure 2.10. The V_{OC} is the point at forward bias where the light and dark generated currents cancel out and it can be calculated using Equation 2.10.

$$V_{OC} = \frac{nKT}{q} \ln\left[\frac{J_L}{J_0} + 1\right] \qquad \textbf{Equation 2.10.}$$

c) Fill Factor

The fill factor (*FF*) is a measure of the "squareness" of the *JV* curve, with 100% indicating a square response and low values tending towards more of a straight line. The fill factor is defined as the ratio of the maximum power rectangle to the power rectangle (shown in Figure 2.10) and can be calculated using Equation 2.11.

$$FF = \frac{P_{MP}}{J_{SC}V_{OC}} = \frac{J_{MP}V_{MP}}{J_{SC}V_{OC}} \qquad \textbf{Equation 2.11.}$$

d) Efficiency

The device efficiency (η) is defined as the ratio of the maximum power generated by the device (P_{MP}), to the incident power upon the device (P_I) and can be calculated using Equation 2.12. Efficiency values are typically determined using AM 1.5 illumination (see Section 2.4.2), where P_I = 1000 W m^{-2}.

$$\eta = \frac{P_{MP}}{P_I} = \frac{J_{MP}V_{MP}}{P_I} = \frac{V_{OC}J_{SC}FF}{P_I} \qquad \textbf{Equation 2.12.}$$

2.4.2. Solar spectrum

It is important to consider the solar spectrum when designing a solar cell as it is used to calculate the ultimate efficiency that can be achieved by a solar cell. The standard AM1.5 solar spectrum used to characterise PV devices is shown in Figure 2.11.

The solar spectrum may be approximated by a black body emitting at a temperature of 6000 K. However, there are a number of factors which can lead to variations in the solar

spectrum, such as temperature across the Sun's surface but of particular importance for PV is the effect of the Earth's atmosphere, shown by the absorbance troughs in Figure 2.11. The path length of the light through the atmosphere is described in terms of the air mass (AM) where AM0 corresponding to the solar spectrum outside the Earth's atmosphere and AM1 represents the solar spectrum incident at the equator. For temperate climates the AM1.5 solar spectrum corresponds to the spectrum intensity is reduced and attenuated by the Earth's atmosphere at a 37° tilt towards the equator. For device testing in this work, a standard power density of 1000 W m^{-2} was used to approximate the AM1.5 spectrum at 25°C.

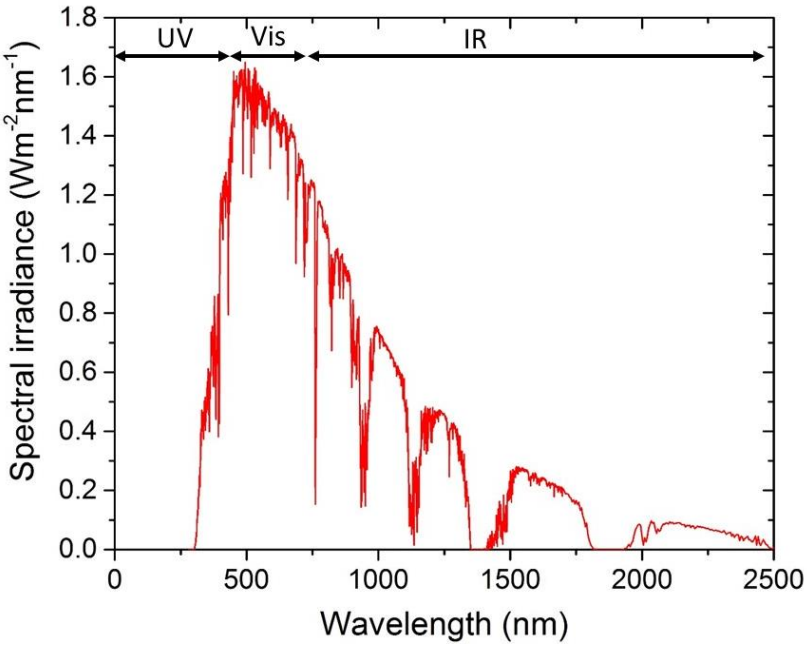

Figure 2.11: *Reference AM1.5 spectrum plotted from the ASTM G173-03 tables*[21].

2.4.3. Fundamental losses in a solar cell

There are several fundamental limitations that mean solar cells can't reach 100% power conversion efficiency. These include:

i. Radiative recombination: As the absorbed photon flux increases the emitted photon flux increases;

ii. Thermalisation: Photons with energy greater than the semiconductor's bandgap ($h\nu > E_g$) excite carriers into states above the conduction band edge,

the hot carriers will then relax to the conduction band edge through scattering interactions with phonons and the carriers will have the same energy as the bandgap. Due to this effect the maximum efficiency that can be achieved by a solar cell is directly related to the bandgap of the absorber layer; and

iii. The limit of the PV performance of a is described by using the Schockley-Queisser limit, shown in Figure 2.12[22]. There are several assumptions made when the Schockley-Queisser limit is calculated:

1) Each incoming photon generates an electron-hole pair;
2) The photovoltaic material consists of a single bandgap energy;
3) Photon with energy lower than the bandgap are not absorbed and all photons with greater energy are absorbed;
4) Loss of electron-hole pairs is through radiative recombination only; and
5) The illumination of the solar cell is via standard AM1.5 test conditions.

iv. The upper performance limit of a single junction solar cell is described by its bandgap, whilst it would be intuitive to use a material with a narrow bandgap as this would maximise the amount of the solar spectrum that is absorbed and achieve the maximum possible J_{SC}. However, the maximum V_{OC} that can be achieved by a solar cell is related to the V_{bi} and bandgap, with narrow bandgap materials yielding a low V_{OC} value and performance. Consequently, there is a trade-off between the maximum voltage the PV device is capable of producing and the fraction of the solar spectrum that is can absorb.

The Schockley-Queisser limit is calculated from the amount of electrical energy that is extracted per photon of incoming sunlight and is dependent on a number of parameters such as the solar spectrum and recombination. Combining these processes means that the maximum conversion efficiency that can be achieved for a single junction solar cell is 33%

using a semiconductor with a bandgap of around 1.4 eV. Figure 2.12 shows the Schockley-Queisser limit for a variety of semiconductors with different bandgaps.

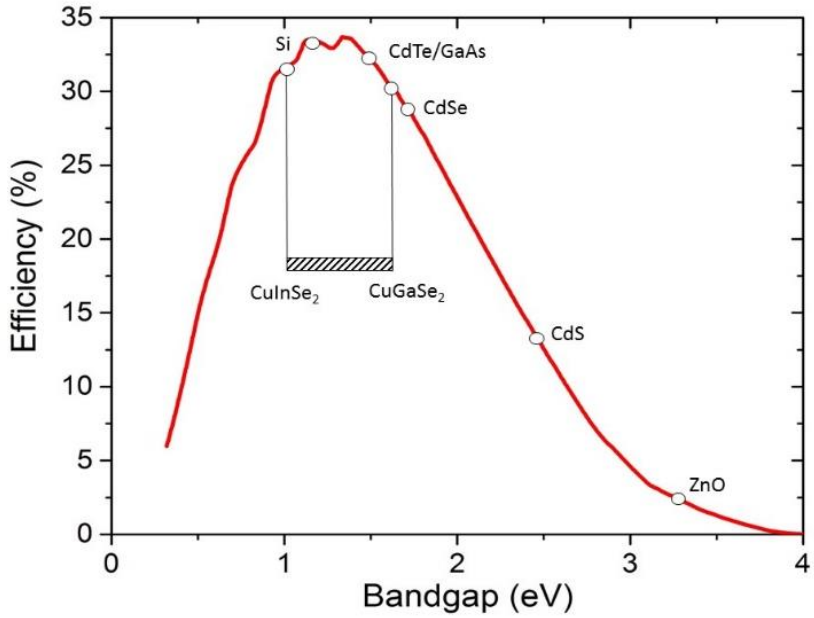

Figure 2.12: *Maximum theoretical conversion efficiency as a function of bandgap under AM1.5 spectrum, Schockley-Queisser limit. Bandgaps for materials that are commonly used in photovoltaics are also marked*[22,23].

In real devices, it can be difficult to achieve anywhere near to the Schockley-Queisser predicted maximum efficiencies due to additional loss mechanisms such as non-radiative recombination, including Auger and Shockley Reed Hall (SRH) recombination. Recombination causes significant losses in solar cells particularly to J_{SC} and V_{OC}. Under high recombination the carriers diffusing across the junction increases, which increase the saturation current, therefore, reducing device V_{OC}. As a result, under high rates of recombination the V_{OC} can be significantly reduced, thus J_0 and V_{OC} values are essentially a measure of the amount of recombination present in the device structure.

SRH is often the dominant type of non-radiative recombination in most semiconductor devices, occurring via trap states found in the band gap, which arise due to native and impurity defect states present in the semiconductor[24,25]. Energy states found in the band gap are a problem in compound semiconductors, such as CdTe due to the number of impurities and defects present in the material. In this type of recombination carriers are

captured from either the conduction or valence bands via trap states. For a single trap state there are four possible processes[26]:

i. Capture of an electron from the conduction band to the trap;

ii. A filled trap can emit an electron in the conduction band;

iii. An empty trap can emit a hole in the valence band i.e. an empty trap will attract an electron from the valence band; and

iv. A trap filled with an electron can trap a hole i.e. a trap will emit an electron into the valence band.

So far, we have only treated fundamental material losses. There are additional losses associated with cell construction and design (resistive losses). In the equivalent circuit diagram for an ideal device (Figure 2.9) the series and shunt resistances were defined as 0 and ∞ respectively. Clearly in a real device this would not be the case. Non-trivial R_S and R_{SH} values can have a significant impact on solar cell performance, particularly the *FF*[6].

R_S arises from movement of current through the device and contact resistance between the device's layers for example overly thick absorber layers or poor contacts between the layers will increase R_S and in extreme situations the series resistance can also reduce the J_{SC}. R_{SH} is a reflection of alternative current pathways present in the device, typically due to grain boundaries and pinholes. A large number of conductive grain boundaries or poor uniformity leading to pinhole formation will decrease R_{SH} and in extreme cases will reduce the V_{OC} of the device. Figure 2.13a and b shows effect of R_S and R_{SH} on the *JV* characteristics of a PV devices. The resistance terms may be incorporated into Equation 2.9 to produce Equation 2.13:

$$J = J_0(e^{\frac{qV-JR_S}{nKT}} - 1) + \frac{(V-JR_S)}{R_{SH}} - J_L \qquad \textbf{Equation 2.13.}$$

a) Series Resistance

Figure 2.13a shows that R_S dominates the shape of the *JV* curve under forward bias conditions, with a decrease to R_S leading to a steeper gradient in the forward bias regime.

R_S may be estimated from the gradient of the straight line portion of the curve under forward bias, the slope is approximately equivalent to $1/R_S$ if it is calculated using *I* vs *V* and R_S as a function of contact area, Ω cm^{-2}, can be calculated using *J* vs *V*.

b) Shunt resistance

Figure 2.13b shows that R_{SH} dominates the shape of the *JV* curve in the reverse bias regime and leads to an increase in the gradient. R_{SH} may be estimated from the gradient of the straight line portion of the curve under reverse bias, the slope is approximately equal to $1/R_{SH}$ if it is calculated using *I* vs *V* and R_{SH} as a function of contact area, Ω cm^{-2}, can be calculated using *J* vs *V*.

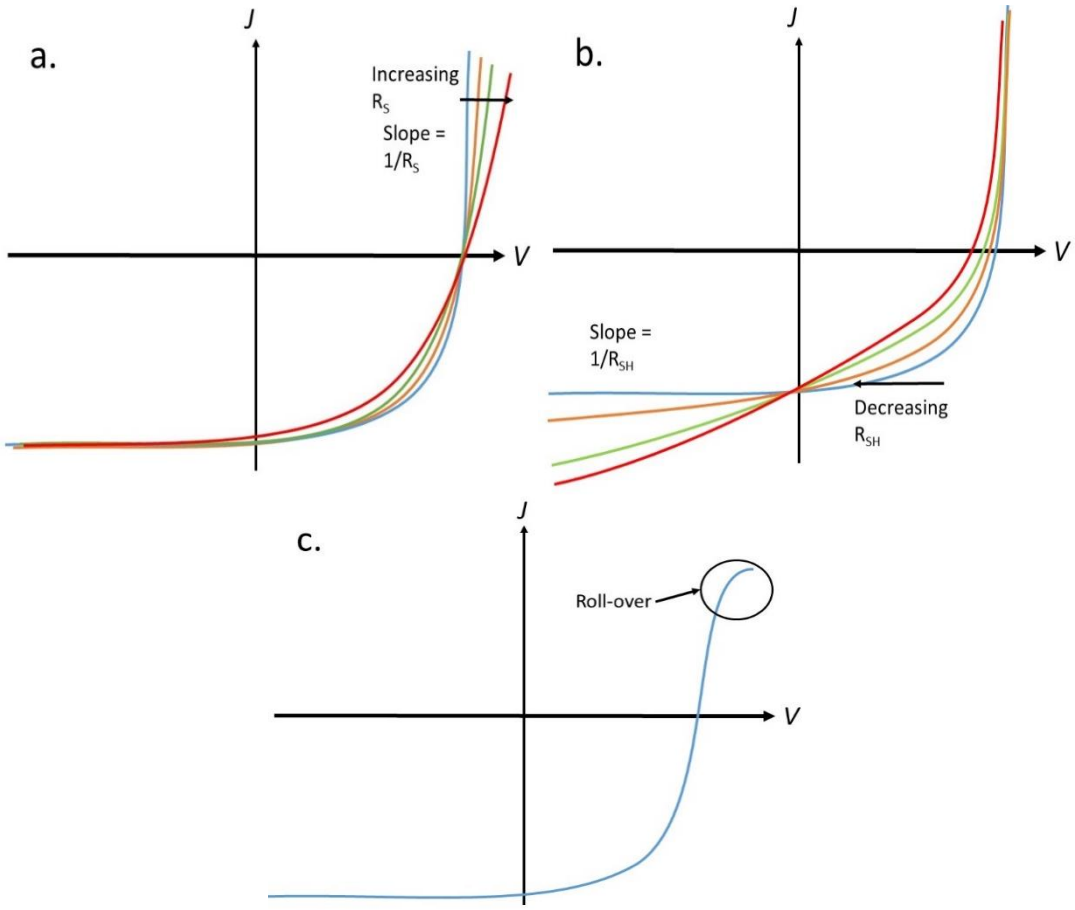

Figure 2.13: *Effect of (a) series resistance (R_S), (b) shunt resistance (R_{SH}) and (c) roll-over on JV characersitics.*

c) Non-Ohmic contacts

In addition to the influence of R_S and R_{SH} if a non-Ohmic contact is formed between the semiconductor and metal, the *JV* curve for the device will exhibit "roll-over" at high forward bias. Figure 2.13c shows a JV curve with a device that demonstrates roll-over. The level of roll-over observed depends on the Schottky barrier height at the semiconductor-metal interface, cells that have a higher Schottky barrier will exhibit a stronger roll-over. Roll-over is produced by the back contact diode which produces a current opposing that of the main junction diode, leading to a reduction in device V_{OC} and *FF* if the barrier is sufficiently large. Roll-over is commonly observed in CdTe devices due to its high work function and electron affinity (see Section 3.3.4).

2.4.4. Quantum efficiency

Quantum efficiency (QE) measurements are one of the most widely used characterisation tools in PV devices for quantifying the conversion efficiency of light into electricity. It is also widely used in thin film PV to analyse the junction properties, junction position and to determine loss mechanisms in complete devices. QE is defined as the ratio of light generated carriers collected to the number of incident photons as a function of wavelength (λ). There are two types of QE: 1) External Quantum Efficiency (EQE), which is the number of carriers extracted from the device compared to the total incident photons, calculated using Equation 2.14; and 2) Internal quantum efficiency (IQE), which only takes into account absorbed light therefore, excluding reflection (R) and transmission (T) losses, calculated using Equation 2.15[27].

$$EQE = \frac{Electrons/s}{photons/s} = \frac{current/q}{total\ photon\ power/h\nu} \qquad \textbf{Equation 2.14.}$$

$$IQE = \frac{EQE}{1-R-T} \qquad \textbf{Equation 2.15}.$$

It is also possible to calculate the J_{SC} from an EQE curve by integrating the whole spectrum over all wavelengths using Equation 2.16[28].

$$J_{SC} = -q \int_{\lambda_1}^{\lambda_2} EQE(\lambda) \Phi_{ph,\lambda}^{AM1.5} d\lambda \qquad \textbf{Equation 2.16.}$$

where λ in the wavelength in nm and $\Phi_{ph,\lambda}$ is the spectral photon flux.

The bandgap of the absorbing material can also be estimated by extrapolating the EQE cut-off back to the x-axis and then using equation 2.17.

$$E(eV) = \frac{1}{q} \times \frac{hc}{\lambda} \qquad \textbf{Equation 2.17.}$$

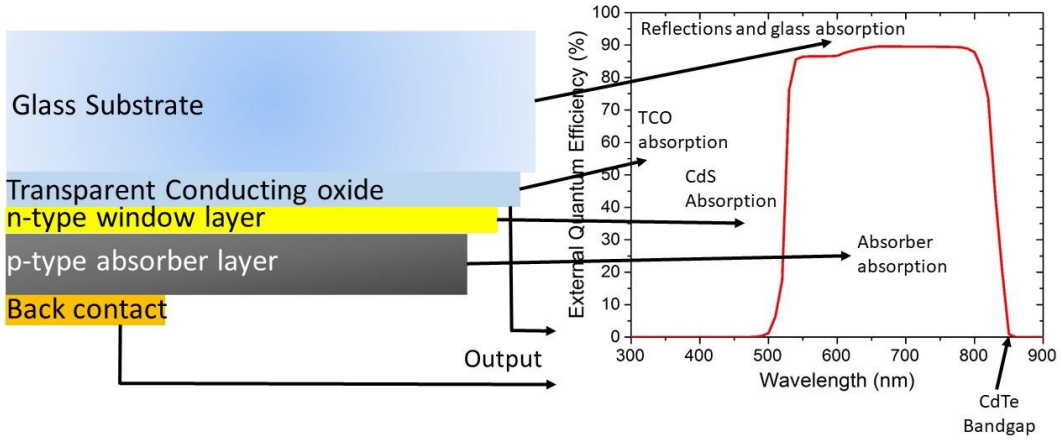

Figure 2.14: *Typical EQE curve generated for CdS/CdTe PV device, showing losses that are observed for this device[29].*

Figure 2.14 shows a typical EQE curve generated for a CdS/CdTe devices. Optical losses are observed across all wavelengths due to reflections from the glass substrate and TCO. These losses can be corrected for by taking an IQE measurement. Losses at long wavelength, > 840 nm, are observed as the energy of the incident photons is lower than CdTe bandgap and therefore are not absorbed[30]. A characteristic feature of a CdS/CdTe based EQE is the losses observed at short wavelength, (< 550 nm), due to parasitic absorption in the CdS layer[29]. CdS has a bandgap of approximately 2.5 eV and due to the doping density difference between the CdS and CdTe layers the depletion region lies entirely in the CdTe layer, (See Section 2.3), meaning any absorption in the CdS layer is lost

as photo generated carriers in this region cannot reach the p-n junction before they recombine[31]. This essentially means that the CdS region of the CdS/CdTe devices is photoinactive and doesn't contribute to the photocurrent unless intermixing between the CdS and CdTe layers has occurred[32]. By taking the intercept of the x-axis at long wavelength the bandgap of the absorber layer can also be estimated.

2.5. Solar cell technologies

Table 2.1: *Best efficiencies achieved for a variety of PV technologies*[3].

Material	Efficiency (%)
Crystalline Si	26.7
Multicrystalline Si	22.3
GaAs	29.1
InP	24.2
CIGS	22.9
CdTe	22.1
CZTSSe	12.6
Perovskite	23.7
Organic	15.6

There are numerous materials commonly used in solar cells, this section will give a brief description of the most common solar absorbers being produced. Table 2.1 shows the maximum efficiencies achieved by the various PV technologies[3].

2.5.1. Silicon

Silicon is the most established and widely used PV technology and dominates the PV market with over a 95% share[33]. Silicon is widely used due to its abundance and because it is widely used in the electronics industry, meaning the technology is highly developed and

benefits from the large scale production of silicon. Silicon solar cells were first developed in 1954 at Bell labs with an efficiency of 6%, since then extensive research and industrial development has been undertaken and an efficiency of 26.7% has now been achieved for single crystal Silicon solar cells[2,3]. Despite this high performance Silicon has an indirect bandgap of approximately 1.1 eV and therefore has a low absorption coefficient, meaning a comparatively thick layer is required for efficient light absorption, ≈ 200 μm. Due to this thickness a long minority carrier diffusion length is required to ensure extraction, meaning a highly pure material is required. Therefore, devices are typically based around single crystal silicon which is energy intensive and expensive to produce. A lower cost alternative is to use multicrystalline (polycrystalline) Silicon, whilst this approach is cheaper the efficiency is lower, 22.3%, due to the effect associated with grain boundaries[34].

2.5.2. III-V compound semiconductors

III-V technologies commonly used for PV applications are gallium arsenide (GaAs) and indium phosphide (InP). They have a direct bandgap and high optical absorption coefficients, both GaAs and InP have a near optimal direct bandgap of approximately 1.4 eV. The highest conversion efficiencies for these materials are 29.1% and 24.2% for GaAs and InP respectively. The disadvantages of using III-V materials is for high performing devices single crystal materials are required meaning, they have very high production costs[30]. Therefore, these devices have niche applications such as space solar cells where cost is less important than performance[35].

2.5.3. Thin Film Solar cells

Thin film solar cells utilise materials with a direct bandgap meaning they can absorb incident photons more efficiently as a result much thinner PV absorbers can be used, around 1 μm. In addition to this, as the layers are now thinner, significantly lower carrier lifetimes are required and therefore, the materials used can be less pure. The thinner layer

and lower purity materials means that thin films solar cells have the potential to be cheaper than other technologies such as silicon.

2.5.3.1. Chalcopyrite materials

Chalcopyrite solar cells were first developed using copper indium diselenide (CIS) due to its direct bandgap at around 1 eV, however, it was found that through incorporation of gallium into the film the bandgap can be controlled from 1.0 eV to 1.7 eV meaning the bandgap can be tailored to the ideal position for PV applications. Substituting gallium onto indium sites leads to the formation of copper indium gallium diselenide (CIGS), a high PV performance can be achieved with up to 22.9% being reported[3]. CIGS devices are typically produced in the "substrate" configuration using the device structure of a metal back contact (Mo), absorber layer (CIGS), window layer (typically CdS), buffer layer (ZnO) and TCO (AZO) with illumination occurring via the TCO side[35].

Due to the scarcity and cost of indium and gallium extensive research has been undertaken to replace these elements with earth abundant alternatives, leading to the development of copper zinc tin sulphide (CZTS) solar cells. However, to date the performance of PV device using CZTS remains significantly lower than the CIGS equivalent, 12.9%, due primarily to the formation of secondary phases[36].

2.5.3.2. CdTe

CdTe is a material that has been extensively investigated as a thin film PV material. Due to its near optimal bandgap of approximately 1.5 eV and its high optical absorption coefficient, only a few microns are needed to absorb most of the incident photons[35]. The PV potential of CdTe was first observed in 1959 by Rappaport *et al* [37], who fabricated homo-junction CdTe cells with 2% efficiency, via In diffusion into p-type CdTe in order to create a n-type layer.

CdTe PV devices are produced in the 'superstrate' configuration with glass acting as the substrate and the transparent front surface of the device, with CdS acting as the n-type

layer. CdTe device utilising this structure were first prepared in 1964 by Muller *et al*.[38], producing a conversion efficiency of 5%. Since then there has been a substantial development in the fabrication and refinement of devices, which have led to a significant improvement in performance. By the 1990s, 16% had been achieved for CdS/CdTe devices but, in the following 20 years there was little progress. Since 2011 there has been significant increases which has meant a performance of 22.1% has now been achieved for CdTe devices[3,39]. This improvement has largely been realised through the removal of CdS as the n-type partner layer resulting in an optimised J_{SC}.

The fabrication and characterisation of CdTe PV devices is the focus of this thesis and full details on the CdTe device structure, as well as a review of the state-of-the-art research is present in Chapter 3.

2.5.3.3. Perovskite solar cells

Perovskite solar cells utilise materials which adopt a perovskite structure, ABX_3, most commonly using a hybrid organic-inorganic lead halide-based material such as, methylammonium lead iodide (MAPI). Perovskite solar cells have attracted a lot interest due to their rapid performance increase, increasing from 3.8% to 23.7% since 2009 and relative ease of fabrication[3,40]. This rapid increase is due to a number of attractive materials properties such as, strong absorption, low recombination rates and a high carrier mobility. A typical perovskite solar cell structure consists of ITO as the TCO, TiO_2 as the electron transport layer, Perovskite layer such as MAPI as the absorber layer, Spiro-OMeTAD as the hole transport material and Au as the metal back contact. Despite their advantages there remains some fundamental questions about perovskite long term stability and lead toxicity, extensive research is being undertaken trying to address these problems.

2.5.4. Organic

Organic solar cells typically consist of polymer thin films of organic semiconductors (≈ 100 nm) such as, pentacene or copper phthalocyanine. The advantages of organic PV

materials are ease of fabrication, mechanical flexibility and strong optical absorption of sections of the solar spectrum meaning semi-transparent PV devices can be used. Typically, the device structure consists of glass or flexible substrate, ITO front contact, a conducting polymer, photoactive polymer and finally a back contact layer (Al, Ag). A performance of 15.6% has been achieved for organic PV devices however, questions over stability and ability to mass produce the active layers still require answering[3,34].

2.5.5. Summary

In summary there is a number of different types of PV technologies all of which have their advantages and disadvantages. For example, the dominant PV technology Si has an indirect bandgap meaning a thick, very pure layer is required for a high efficiency to be achieved. More novel PV technologies such as perovskite and organic solar cells suffer from inherent stability issues. CdTe PV offers a viable alternative to Si as the dominant technology as it has a number of advantages such as, a direct bandgap and less pure starting materials can be used reducing the material costs, in addition to this a high performance and stability has been achieved. CdTe PV currently has a 5% PV market share however, with further developments to the technology improvements to device efficiency and reductions to module cost can be achieved. This thesis will outline and demonstrate the research that is currently being undertaken in order to try and improve CdTe PV beyond the 22% already achieved.

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3. CdTe Solar cells

3.1. Introduction

As mentioned in Section 2.5.3.2 CdTe is a material that has been extensively investigated as a thin film PV material due to it attractive material properties. CdTe solar cells currently offer one of the lowest cost per watt in the PV market[1]. CdTe PV have improved significantly over the years from 2% in 1959 to 22.1% in 2019, Figure 3.1 shows the efficiency of CdTe solar cells over time[2–4]. This improvement is largely down to the CdTe research community moving away from the conventional CdS/CdTe structure such as Se alloying with the CdTe layer and investigating alternatives to CdS such as, CdZnS, MZO and SnO_2[5,6].

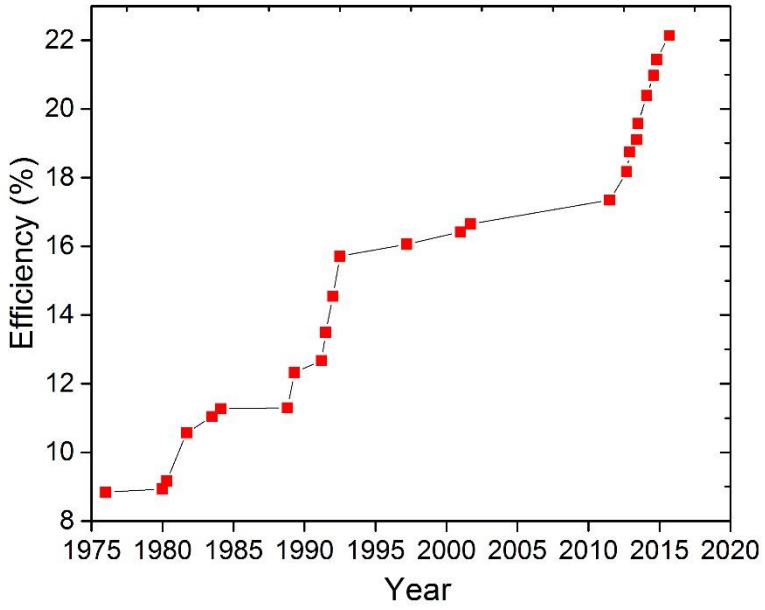

Figure 3.1: *Technological development of CdTe thin PV devices since 1976. Replotted from the NREL efficiency chart [4].*

In this chapter, the structure of CdTe solar cells will be discussed including the "traditional" CdS/CdTe structure, which is used in a large fraction of current CdTe research and was considered as the standard for comparison in the work presented in this thesis. The limitations of the CdS/CdTe structure will be discussed in Section 3.3. Recent

developments to the device structure with a particular focus on Se incorporation into the CdTe layer and use of MZO as the window layer will be discussed in Section 3.4.

3.2. CdTe device structure

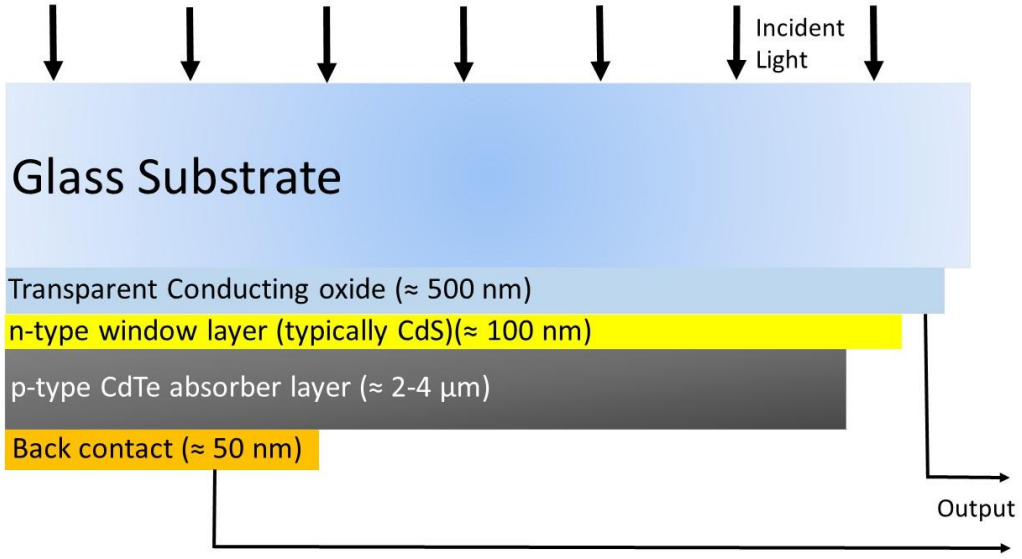

Figure 3.2: *Structure of a standard CdTe solar cell in the 'superstrate' configuration.*

CdTe can be produced in two different orientations the 'substrate' and 'superstrate' configuration[2,7,8] however the superstrate structure has established itself as the optimal approach. CdTe solar cells reported in this work were all prepared in the superstrate configuration. Figure 3.2 shows a schematic representation of a CdTe superstrate solar cell. In this configuration all depositions occur on a glass substrate, which also acts as the transparent front surface. The fabrication of a superstrate CdTe device can be divided into a number of distinct sequential steps, which are as follows:

i. A TCO layer which acts as the device front transparent contact.

ii. A "window layer" is then deposited onto the TCO acting as the n-type heterojunction partner layer, typically this is a CdS layer.

iii. The p-type CdTe absorber layer is then deposited, forming the p-n heterojunction.

iv. The device stack is then treated to a chlorine activation step. Typically, this is performed using $CdCl_2$. However, in this work it was performed using $MgCl_2$.

v. And a back contact is then added to the device to complete the cell structure.

In the following sections these device layers or processing steps will be explored in more detail from the more traditional approach to state-of-the-art new approaches. For each the benefits and potential limitations will be discussed.

3.2.1. Glass substrate and transparent conducting oxide

Low cost soda lime glass (SLG) is the most commonly used glass substrate for PV devices as this is the industry standard and can be produced on a large scale by a float process[9]. For more niche applications where a higher temperature or a reduced Na content is required aluminosilicate or borosilicate glass can be used[10], use of these bespoke glass types adds to fabrication costs significantly and is not industrially scalable. Hence for this work only SLG was used as the glass substrate, in addition to this, a lot of work has been undertaken on barrier layers to negate the impact of Na diffusion.

TCO layers are essential for achieving a high-quality device performance as they offer a transparent electrically conducting front contact. A good quality TCO is required to be both highly optically transparent (> 80%) and highly conductive (< 10 $\Omega\ \square^{-1}$)[11]. The most commonly used TCOs for PV applications are fluorine doped tin oxide (FTO), tin doped indium oxide (ITO) and aluminium zinc oxide (AZO)[11–13]. ITO and AZO are known to be thermally unstable at high temperatures suffering from loss of conductivity and therefore, are not suitable for CdTe PV due to the high temperature device processing[14]. The more thermally stable FTO layer is typically used as the TCO in CdTe PV and is the industry standard due to its reliability, low cost and ease of production[9,15]. FTO is the TCO that was used throughout this work.

3.3. Traditional CdTe approaches

Despite the CdTe community starting to move away from the conventional CdS/CdTe heterostructure, it is still widely used as the standard to compare any new cell development against. In this work CdS/CdTe device structures were used as the comparison by which new device architectures could be evaluated. The following sections review the key aspects of this reference structure.

3.3.1. CdS as the window layer

CdS was the first n-type window layer established for CdTe PV in the 1960s by Muller *et al*[16]. and subsequently became the default n-type partner layer. CdS is an attractive choice as the n-type material as it is naturally n-type due to sulfur donor vacancies, has a relatively wide bandgap (≈ 2.5 eV) and has a favourable band alignment with CdTe meaning a high V_{OC} can be achieved[17,18]. CdS layers can be fabricated via an array of methods such as close space sublimation (CSS)[19], chemical bath deposition (CBD)[20], sputtering[21] and metal-organic chemical vapour deposition (MOCVD)[22]. In general, sputtering and CBD are the chosen routes for fabricating CdS layers as they produce films with smaller grain sizes meaning less pinholes for a higher V_{OC} and *FF*[20].

As previously mentioned in Section 2.3, due to the different doping levels of the CdS and CdTe the depletion region lies entirely in the CdTe layer, meaning any photon absorption in the CdS will not contribute to photocurrent i.e. parasitic absorption (see Figure 2.14)[23,24]. Incident light with energy greater than CdS bandgap is predominately absorbed by the CdS and as the minority carrier lifetime is low, the photo generated carriers recombine before they can reach the junction in the CdTe layer[2,20]. Therefore, to try and minimise the amount of absorption in the CdS layer the thickness of the CdS layer is reduced. Figure 3.3 shows EQE data which demonstrates the effect of decreasing the CdS layer thickness modelled using solar cell capacitance simulator (SCAPS). The influence of CdS thickness reduction is apparent when comparing the devices short wavelength

response i.e. < 550 nm when the photon energy exceeds the CdS bandgap energy, the enhanced EQE response at short wavelength due to reduction in CdS thickness leads to an improved device J_{SC}. Whilst decreasing the thickness leads to the expected gains in J_{SC} it can also leads to the formation of pinholes and leads to losses in V_{OC} and *FF*. Therefore, the CdS thickness has to be finely controlled so that a maximum J_{SC} can be achieved without comprising V_{OC} and ultimately efficiency[25].

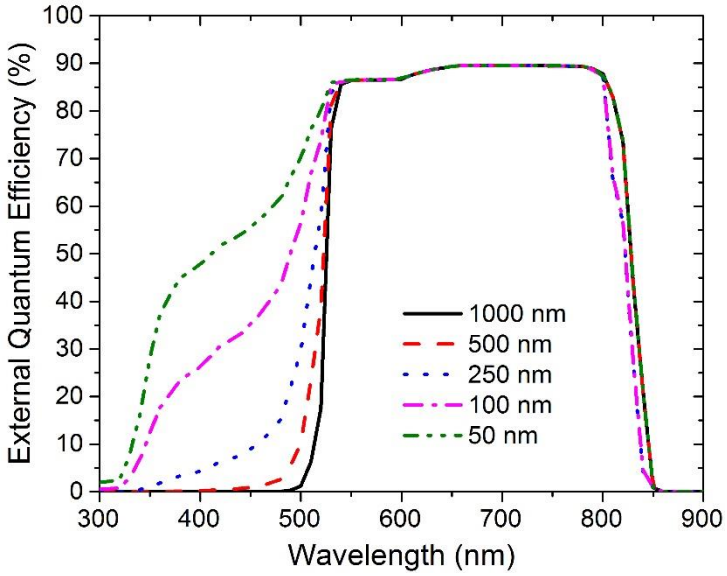

Figure 3.3: *The effect of increasing CdS thickness on CdS/CdTe devices (SCAPS). Where thinner CdS layers enables more light to reach the CdTe absorber layer.*

A number of strategies have been explored to try and improve the performance of CdS/CdTe based devices[26,27]. The inclusion of a 'high resistive transparent' (HRT) buffer layer has been used between the TCO and CdS layers. This HRT layer has a wider bandgap than CdS so no losses due to optical absorption are observed and it acts as a pinhole blocker meaning a thinner CdS layer can be used leading to enhanced J_{SC} without having the detrimental impact of increased pinholes and device shorting[27]. The choice of HRT layer is essential, as a favourable HRT layer can also improve the band line ups in solar cell and result in further improvements to device performance[26]. Common HRT layers that have been used are ZnO, SnO_2 and MZO[26,28,29]. An alternative to the HRT approach is to increase the bandgap of CdS. Wu *et al*[30]*.* demonstrated incorporating oxygen into the CdS layer leads

to a greatly reduced grain size and quantum confinement effects which results in significantly increasing its bandgap. The increased bandgap CdS:O phase led to an improved device J_{SC} and performance. Some losses at short wavelength were still observed due to the CdS:O layer reverting back to lower bandgap CdS at the CdS/CdTe interface [31]. CdS:O layers for CdTe PV were investigated in this work and more information about their impact on device performance can be found in Section 5.2.

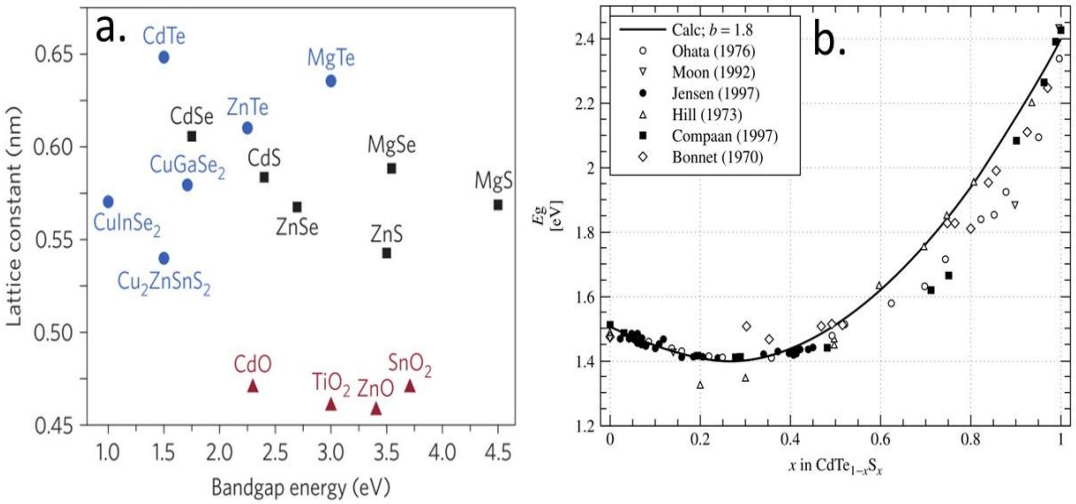

Figure 3.4 *a) Lattice constant and bandgap of common materials used in PV devices taken from ref[32]. b) Bandgap change with increasing S in the CdTe showing the bandgap bowing effect taken from ref[2].*

Both the HRT and CdS:O approaches still result in some parasitic absorption in the CdS layer, hence the maximum J_{SC} and thus performance remained limited. Significant recent work has, therefore, been undertaken to try and completely replace CdS as the window layer[28,33,34]. Replacing CdS as the window layer is not trivial however, as CdTe has a high lattice constant and, as a result, most common PV window layer materials such as, TiO_2 and ZnO require a high bandgap and a good lattice match with CdTe[32,35]. Figure 3.4a shows the lattice constants of materials that are commonly used in PV devices. A large lattice mismatch leads to strain and dangling bonds at the interface, reducing V_{OC} and device performance[36,37]. Although the lattice mismatch with CdS is still significant, 10%, during device processing, the CdTe and CdS layers intermix. Te diffuses into the CdS layer and S diffuses into the CdTe layer, leading to the formation of $CdS_{(1-Y)}Te_Y$ and $CdTe_{(1-X)}S_X$ regions

at the interface[35,38]. Intermixing between the layers helps to alleviate some of the strain at the interface, improving its quality and ultimately device performance. It has also been demonstrated that S diffusion into the CdTe layer results in a bowing effect where the bandgap of CdTe is reduced to a minimum of 1.39 eV following Vegard's law increasing the amount of photocurrent that can be produced by the device, Figure 3.4b shows how the S diffusion into CdTe affects its bandgap[2,38,39]. The amount of intermixing that occurs is dependent on a number of factors such as processing temperature and CdS grain size and is considered essential in producing a high quality interface[39,40]. This means replacing the CdS layer is difficult as other alternatives, such as ZnO and SnO_2, will have a higher lattice mismatch and potentially won't have the luxury of extensive intermixing to help reduce the strain at the device interface.

3.3.2. CdTe absorber layer

CdTe is the p-type absorber layer in CdS/CdTe devices, due to it high absorption coefficient only ≈ 2 µm is required to absorb 99% of the incident above bandgap energy photons[41]. CdTe thin films can be deposited via a number of different techniques such as sputtering[42], CSS[43], MOCVD[22], thermal evaporation[44] or electrodeposition[45]. The performance of polycrystalline CdTe devices depends on a number of different factors such as, grain size, grain boundary density and the doping density of the CdTe layer. This section will discuss some of the key points related to the CdTe layer for PV devices such as grain boundaries and doping, the current limitations of the CdTe layer will also be discussed.

3.3.2.1. Grain boundaries

As the CdTe is typically a polycrystalline material it has grain boundaries which are commonly considered detrimental to performance. The boundary regions are assumed to act as recombination centres due their increased defect density or act as shunting pathways. In as-deposited CdTe layers it has been shown that grain boundaries act as recombination centres and limit device V_{OC}[46], therefore, it is presumed beneficial to reduce

the grain boundary density, large grains are produced by high temperature methods such as CSS, meaning the majority of high efficiency devices utilise CdTe layers deposited via high temperature methods[19,47]. Nowell *et al*[47]. demonstrated that sputtered CdTe device efficiency increased with increasing CdTe grain size.

However, even in large grained CdTe layers, a chlorine activation step is always required in order for a high performance to be achieved. Cathodoluminescence (CL) imaging has demonstrated that grain boundaries still act as recombination centres even after the chlorine step but the recombination velocity is significantly reduced suggesting that the chlorine is electrically passivating the grain boundaries and reducing their impact[48]. Grain boundary passivating effects have also been observed for other elements such as, Se, S and O[49]. The CL imaging also indicated that the grain boundaries are still ultimately deleterious to recombination and thus performance, meaning the maximum V_{OC} achievable may always be compromised in polycrystalline CdTe. This is potentially demonstrated by single crystal CdTe devices, i.e. no grain boundaries, demonstrating a greater V_{OC} than thier polycrystalline counterparts, 1.04 V compared to 0.88 V[32].

There have however been a number of reports implying positive effect of grain boundaries in CdTe devices and it should be mentioned that polycrystalline CdTe devices outperform their single crystal counterparts. Some reports suggest that the chlorine is segregating along the grain boundaries, creating junction regions in the grains enhancing the carrier collection between the grain boundary and grain interior. This has been supported by electron beam induced current (EBIC) and scanning probe analysis[50,51]. For a comprehensive review on the effects of grain boundaries, the reader is directed to the review by Major[49].

Despite the large amount of work conducted on trying to understand the exact role of grain boundaries, there is still significant scope in order to evaluate their exact role in CdTe PV devices.

3.3.2.2. Doping of CdTe

Doping is of critical importance in solar cell layers since it determines the strength of the field and junctions' position. Some native doping of CdTe is possible, but, to achieve sufficiently high doping for device applications, extrinsic dopants are required.

CdTe can be doped via native defects either p or n-type. At high temperatures and in Te rich conditions the vapour pressure of Cd exceeds that of Te. This creates an excess of positively charged Cd vacancies ($V_{\mathrm{Cd}}^{\bullet\bullet}$), which is an acceptor in CdTe and makes the material inherently p-type[52]. However, in an excess Cd environment, doubly negatively charged Te vacancies ($V_{Te}^{//}$) begin to dominate promoting n-type conductivity[52,53]. Interstitial defects will also be present, Cd_i and Te_i which can additionally act as donors or acceptors respectively. Increasing the temperature of the CdTe fabrication can lead to an increase in the concentration of $V_{\mathrm{Cd}}^{\bullet\bullet}$ and $V_{Te}^{//}$ however, there is a limit to the achievable doping level as compensating defects form and lower the materials doping level[53]. The maximum doping density for CdTe that can be achieved by native defects is approximately 10^{14} cm^{-3},[54] low when compared to other semiconductors such as, silicon and GaAs[55].

Given the limitations of native defects, extrinsic (impurity) dopants have been widely explored in the aim of increasing the carrier concentration in CdTe. For II-VI semiconductors group III and VII elements are potential substitutional donors while group I and V are potential acceptors. Cl and In are some of the most well studied n-type dopants in single crystal CdTe layers[56] and Na, Cu and Ag are some of the most studied p-type polycrystalline CdTe dopants[57,58]. Cu is by far the most widely studied p-type donor for CdTe PV as it acts as a substitutional dopant on a Cd site ($Cu_{Cd}^{\bullet}$)[52]. The incorporation of Cu leads to an increased hole density (10^{15} cm^{-3}) and a significant improvement to device performance[59]. However, Cu doping has to be finely controlled as Cu is a fast diffuser, particularly along the grain boundaries and can lead to device instability. It has been demonstrated that Cu_i act as donors in CdTe layers, significantly lowering the doping density significantly and

reducing device performance[60]. As a result, Cu doping is typically applied post CdTe growth as it allows for finer control of the Cu diffusion. Group V dopants such as, P and As have demonstrated p-type doping capabilities and have shown a higher doping density (10^{16} - 10^{17} cm^{-3})[32,61] and producing CdTe devices using these dopants is currently an extensive area of research in the CdTe community (see Section 3.4.3).

As previously mentioned, chlorine is essential for a high PV performance to be achieved, yet the inclusion of chlorine seems somewhat counterintuitive as it would be expected to act as an n-type dopant. However, it has been shown that chlorine forms the A-centre defect complex,$(V_{Cd}^{\bullet\bullet} - Cl_{Te}^{/})^{\bullet}$, and is a single acceptor[62], it has also been demonstrated by scanning transmission electron microscopy (STEM) and atom probe tomography that chlorine segregates along the grain boundaries and electrically passivates them, reducing the level of recombination[61]. As with the grain boundaries, the exact role chlorine plays in doping CdTe devices is still a much debated topic and requires further investigation.

3.3.3. Chlorine activation step

The chlorine activation step is essential in order for high performance to be achieved and is used universally across the CdTe PV community in one form or another. The chlorine activation step for CdTe solar cells was developed by Basol in 1985[63]. Al-Allak *et al*.[64] demonstrated that as-grown devices had an efficiency of ≈ 1%, while heating in the presence of chlorine resulted in an efficiency of ≈ 10%. This performance increase is controlled by several factors such as, treatment temperature, treatment time, annealing atmosphere and chlorine source. Under or over treatment will result in losses to performance[2,17,64].

Conventionally, the chlorine treatment is performed post CdTe growth using $CdCl_2$[2]. As $CdCl_2$ is toxic, a variety of alternatives have been investigated, such as $MgCl_2$[65], NaCl and NH_4Cl[66], to varying degrees of success. In this work, $MgCl_2$ was used for the chlorine

treatment as this achieves a high performance and is non-toxic[65]. The annealing is usually performed under atmospheric conditions and the temperature is usually in the temperature range of 390 - 450°C.

The exact role the chlorine treatment plays has been widely studied and it has been suggested that the improvements in performance result from a number of factors such as:

i. Promoting recrystallization and grain growth: Depending on the technique used as-deposited CdTe often has a sub-micron grain size and a high density of stacking faults. Following the chlorine step, the CdTe layer undergoes recrystallisation and grain sizes of up to 10 microns can be achieved, reducing the grain boundary density and thus improving performance[2,67]. However, films deposited via high temperature methods, such as CSS, have large grain sizes, >1 μm, as deposited and the energy required to recrystallize then is too high. As a result, little grain growth occurs during the chlorine treatment but in order for a high performance to be achieved a chlorine step is still required, suggesting more factors are at play than just recrystallisation[40],

ii. Enhancing intermixing of the CdTe and CdS layers: In small grained CdTe layers, the chlorine treatment has been shown to enhance the amount of intermixing between the CdS and CdTe layer essential to alleviate interfacial strain and achieve optimal performance[39]. Again in large grained CdTe layers and high temperature deposition techniques it has been demonstrated that the majority of CdS and CdTe intermixing occurs during the CdTe film growth and not during the chlorine activation step[40]. This is suggestive that the chlorine treatment is affecting more than just the intermixing,

iii. Optimising the device junction position: EBIC analysis has been used to show that as grown devices demonstrate a buried CdTe homojunction response

however, after undergoing a chlorine treatment an optimised CdS/CdTe heterojunction is formed, achieving a higher performance[68],

iv. p-type doping of CdTe: It has been suggested that the chlorine plays a role in stabilising the p-type doping of CdTe forming the A-centre, $(V_{Cd}^{\bullet\bullet} - Cl_{Te}^{/})^{\bullet}$. This A-centre acts as a single acceptor and removes the mid bandgap $V_{Te}^{//}$ states which acts as a recombination centre[62],

v. Enhancing carrier collection: Scanning probe microscopy has been used to show that chlorine preferentially diffuses along the grain boundaries. EBIC has demonstrated that grain boundaries after the chlorine treatment become bright suggesting they have enhanced current collection compared to the grain interior. Therefore, using these two techniques it has been suggested that when the chlorine segregates along the grain boundaries it dopes the CdTe at the grain boundaries n-type, creating junctions regions that exist between the grain boundaries and grain interiors in chlorine treated devices, where n-p-n junctions exist and contribute to enhanced carrier collection from grain interior to grain exterior[50,51]. However, it should be mentioned that the techniques observing this can be highly surface sensitive and large amount of surface recombination may be dominating these measurements[49], and

vi. Grain boundary passivation: Luminescence measurements, particularly CL perhaps offer the most insight into the exact role of the chlorine treatment as they are less sensitive to surface effects. CL imaging has demonstrated that in the untreated CdTe devices the grain boundaries show a high level of non-radiative recombination compared to the chlorine treated CdTe devices. Following chlorine treatment grain boundaries still display a higher rate of non-radiative recombination when compared to the grain interior. However, the grain boundary recombination velocity was much lower compared to the

untreated equivalent. This supports the theory that chlorine segregation at the grain boundaries electrically passivates them, negating a lot of the deleterious effects of the grain boundaries[48].

There is growing consensus in the CdTe research community that the grain boundary passivation effect is the most important role of the chlorine treatment. Investigating the exact role of the chlorine step still remains challenging as in general it is difficult to separate the number of simultaneously occurring effects in real devices, such as oxygen content, processing temperature, grain growth and sulfur diffusion from the influence of the chlorine.

Currently the highest V_{OC} achievable even in the state of the art devices is approximately 880 mV, which is significantly lower than the theoretical limit approximately 1.2 V[69]. This could indicate that a better understanding of how the chlorine treatment works or how to passivate the grain boundaries more effectively could result in an enhanced V_{OC} and device performance.

3.3.4. Device back contacting

The formation of an Ohmic contact in CdTe devices is not trivial[41]. Due to CdTe high electron affinity and work function, a metal with a work function of higher than CdTe is required to form an Ohmic contact (see Section 2.2.3.1)[17]. As most of the metals don't possess a work function greater than 5.7 eV, the metal will usually form a Schottky barrier with CdTe. This will lead to the formation of a diode opposing the CdS/CdTe junction, resulting in a reduced performance[2,21]. As gold has a high work function it is often used as a simple metal back contact in research labs as this results in a low Schottky barrier. However, cell produced using gold still have significant rollover (see Section 2.4.3) in thier *JV* responses and gold is also very expensive[70].

A number of different strategies have been utilised in order to facilitate the formation of a pseudo-Ohmic contact in CdTe devices:

i. Te-rich back surface: Use of a Te rich back surface has been reported to create an Ohmic back contact by chemically etching the CdTe back surface. The p-type conductivity is enhanced by selectively etching the Cd, creating cadmium vacancies at the back surface, creating a heavily p-doped region at the back surface and allowing carriers to tunnel through the contact barrier[71]. A number of different etchants have been used such as, bromine-methanol[17] and nitric-phosphoric (NP) etch[17]. The NP etch yields the highest performance and is the most commonly used etchant,

ii. Doping: The use of Cu to form a heavily doped p^+ region at the back surface is by far the most commonly used way of forming a pseudo-Ohmic contact in CdTe PV devices[11,60]. This is usually achieved through the addition of 1-5 nm Cu layers between the CdTe and Au layers[72]. It has been shown that the Cu doping can be stabilised by adding a Cu doped ZnTe layer at the back surface, as this stops excess Cu diffusing into the CdTe layer and facilitates the formation of a p^+ region at the back surface[73,74]. Arsenic has also been used to create a heavily p doped CdTe:As region at the back surface to facilitate the formation of an pseudo-Ohmic contact.

iii. Interfacial layers: Interfacial or buffer layers have been incorporated between the CdTe and contact layer to try and improve the band alignment between the layers and lower the Schottky barrier[75]. A variety of different layers have been investigated as potential buffer layers such as, Te[75], Sb_2Te_3[11], ZnTe[76], MoO_3[77], WO_3[21] and a variety of organic polymers[78].

3.4. Recent CdTe device development

As previously mentioned the efficiency of CdTe devices has improved significantly since 2011 from 16.5% to 22.1%[3,79]. This has largely been due to new approaches to the CdTe device architecture. The next section will outline some more recent research developments

made in CdTe PV devices, including alloying the CdTe layer with Se and new alternatives to CdS as the device window layer. Currently the maximum V_{OC} achievable in polycrystalline CdTe is 0.88 V. However, the theoretical V_{OC} achievable for CdTe is approximately 1.2 V[32,69]. Therefore, a large amount of research is being undertaken to try and reduce the voltage deficiency in CdTe PV devices this has mainly focused on increasing the dopant density of the CdTe layer by using group V dopants primarily in single crystal CdTe layers but with a view to polycrystalline devices.

Many of the topics presented in this section were investigated and published during the course of my PhD therefore, a lot of the work presented in this thesis was done in parallel with others. As a result, I have achieved several publications related to selenium incorporation and the use of MZO in CdTe PV devices. Therefore, a lot of the work presented in this section will overlap with themes presented in results chapters 5 and 6 and will include references to my own work.

3.4.1. CdSe layers and selenium incorporation

Use of n type CdSe layers in CdTe PV was first reported in 2014, Paudel *et al*[80]. investigated the use of n-CdSe to replace CdS as the device window layer. Initially the use a narrow bandgap material, 1.7 eV compared to 2.5 eV, seems somewhat counterproductive as one would expect the amount of parasitic absorption to be enhanced[6]. However, the rate of solubility of CdSe into CdTe is significantly higher than CdS, due to Se and Te being similar in size[81,82]. The large interdiffusion of CdSe and CdTe forms a $CdTe_{(1-X)}Se_{(X)}$ phase resulting in a band bowing effect similar but larger to that of CdS. A lower bandgap can be achieved compared to CdTe (≈ 1.32 eV), the intention being that the reduced bandgap would result in an enhanced device response at long wavelengths[83]. Figure 3.5 shows the influence of Se diffusion into the CdTe layer on the bandgap of the resulting $CdTe_{(1-X)}Se_{(X)}$[83,84].

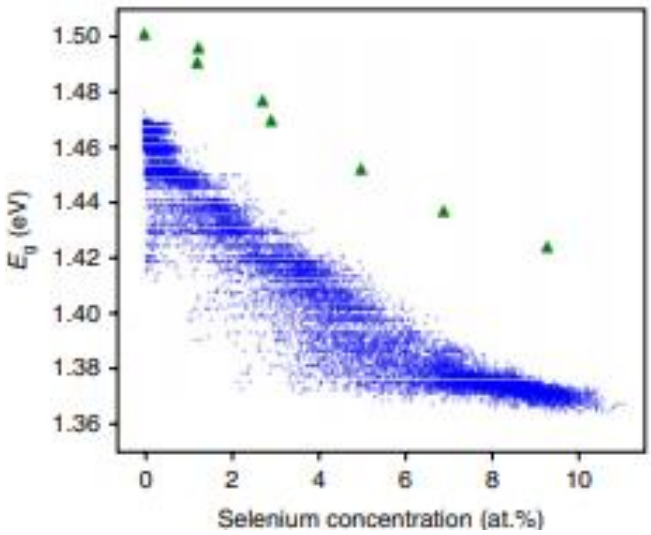

Figure 3.5: *Influence of Se concentration on CdTe bandgap calculated using CL and* secondary ion mass spectrometry (*SIMS) taken from ref*[84]*.*

Paudel *et al*[80]. demonstrated the expected gains at long wavelength, Figure 3.6a shows the EQE response for CdTe devices using a variety of different window layers such as, FTO, CdS/CdSe and CdSe. The devices produced using CdSe to form the $CdTe_{(1-X)}Se_X$ phase showed an effective bandgap of approximately 1.35 eV, estimated from EQE cut-off, and associated improvements to device J_{SC}. It was also found that when CdSe was used as the device window layer significant enhancement to device photo response at both short and long wavelengths, leading to a substantial increase to device J_{SC}. This improvement is only possible if the CdSe layer completely dissolves into the CdTe layer as any residual CdSe left in the device structure would contribute to enhanced parasitic absorption as the CdSe layer is photoinactive in CdTe devices similar to CdS[33,85,86]. Therefore, a key focus for optimisation is to ensure the CdSe layer has been completely consumed during device processing in CdTe devices.

This is exemplified by Figure 3.6b which shows how the CdSe thickness influences the CdTe device photo response. A thick CdSe layer result in significant amounts of parasitic absorption at low wavelength, implying there is a limit to amount of Se that can be effectively incorporated into the CdTe layers, with 100 nm demonstrating the best performance[80,87].

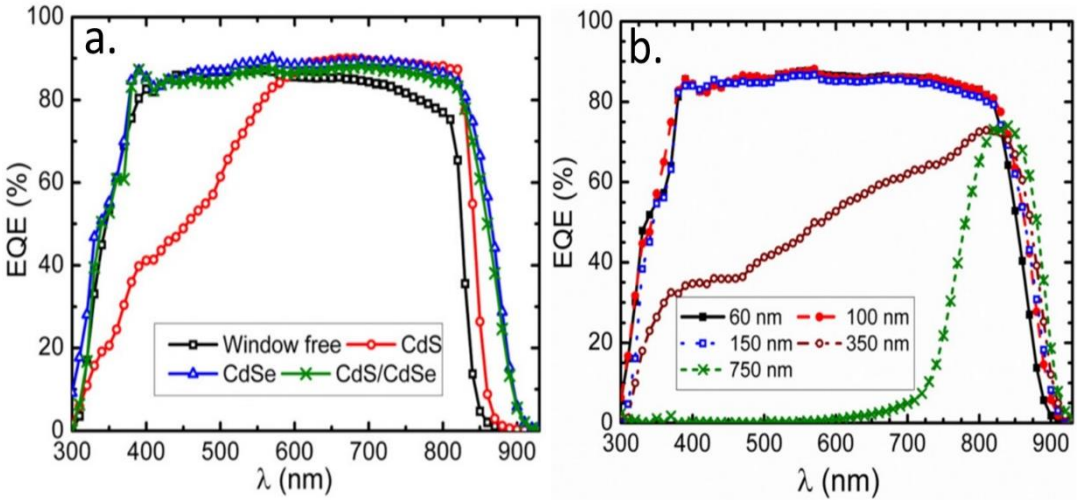

Figure 3.6: *a) CdTe device EQE response using a variety of different window layers and b) CdTe device EQE as a function of CdSe thickness in CdSe/CdTe devices taken from ref*[80].

As mentioned in Section 3.3.1, the removal of CdS as the device window layer is typically coupled with a significant reduction to both device V_{OC} and *FF*. It has however, been found that when CdSe layers are diffused into the CdTe layers forming the $CdTe_{(1-x)}Se_{(x)}$ phase the V_{OC} is largely retained in FTO/CdSe/CdTe devices, with only small reductions observed to the V_{OC} and *FF*[80,87]. This suggests that not only is the Se reducing the bandgap, it is also enhancing the material properties of the CdTe layer such as band alignment[84], interface strain alleviation[88] and carrier lifetime[89] and contributing to enhanced V_{OC} when compared to the FTO/CdTe devices. This opens up to the possibility of producing CdTe devices without the need for a CdS layer and achieving the maximum possible photocurrent[84].

Typically in order for no V_{OC} losses to be observed a thin CdS layer is still required, typically 10-15 nm thick, as this retains the device V_{OC} to beyond 800 mV and limits the amount of CdS parasitic absorption observed[29,80,88,90]. The use of thin CdS does still compromise *FF* as it can be difficult to achieve a uniform film at that thickness and therefore, often results in the formation of pinholes and reduction in device shunt resistance.

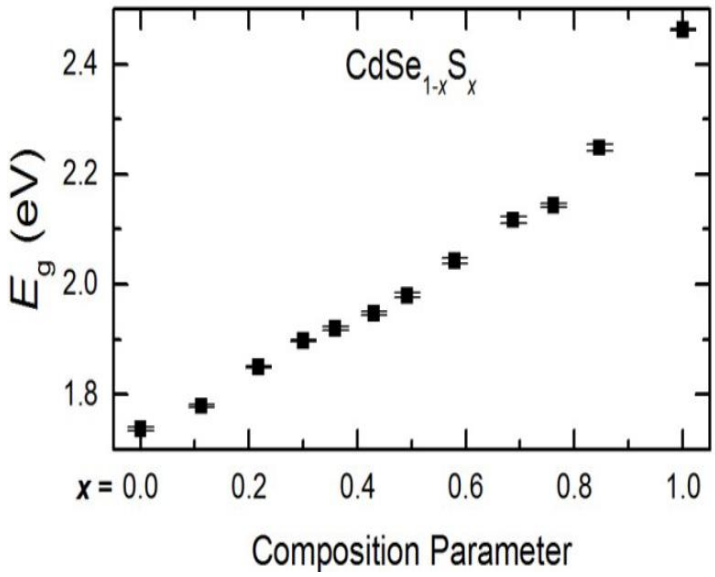

Figure 3.7: *Effect of increasing S content on CdSe bandgap taken form ref*[91].

However, it has been demonstrated that CdSe is also soluble in CdS, Junda *et al*[91]. demonstrated that the bandgap of CdSe increases roughly linearly with increasing S content from 1.7 eV to 2.5 eV with no bandgap bowing effect being observed. Figure 3.7 shows the influence of S content on the bandgap of $CdS_{(1-X)}Se_X$. Grice *et al*[90]. produced a variety of CdTe PV devices using co-sputtered $CdS_{(1-X)}Se_X$ window layers and a significant enhancement to the parasitic absorption at short wavelengths was observed for higher Se content, the $CdS_{(1-X)}Se_X$ is of a lower bandgap than CdS and isn't as readily soluble in CdTe as CdSe[90,92].

The exact role of Se in the CdTe layer is still unclear and device results have outpaced the fundamental understanding of the process. Poplwasky *et al*[87]. used EBIC and TEM to

demonstrate that when thick CdSe layers where used (> 200 nm) in the CdSe/CdTe device stack there was a photo inactive region at the front of the device due to remnants of the wurzite CdSe phase resulting in a buried junction response. When 100 nm CdSe layer were used the junction was at the interface as the CdSe layer had entirely converted from the wurzite phase to the photoactive $CdTe_{(1-X)}Se_{(X)}$ zincblende structure[87]. It was also demonstrated by atom probe tomography that the Se content was graded, with a high Se content at the near interface and a low Se content in the bulk (Figure 3.8a)[87,89]. It was suggested that this grading was responsible for the associated enhanced device V_{OC} from 0.70 V to 0.77 V, as a similarly graded band structure is used in other PV technologies such as CIGS to enhance carrier lifetime, reduce recombination and improve device performance[93].

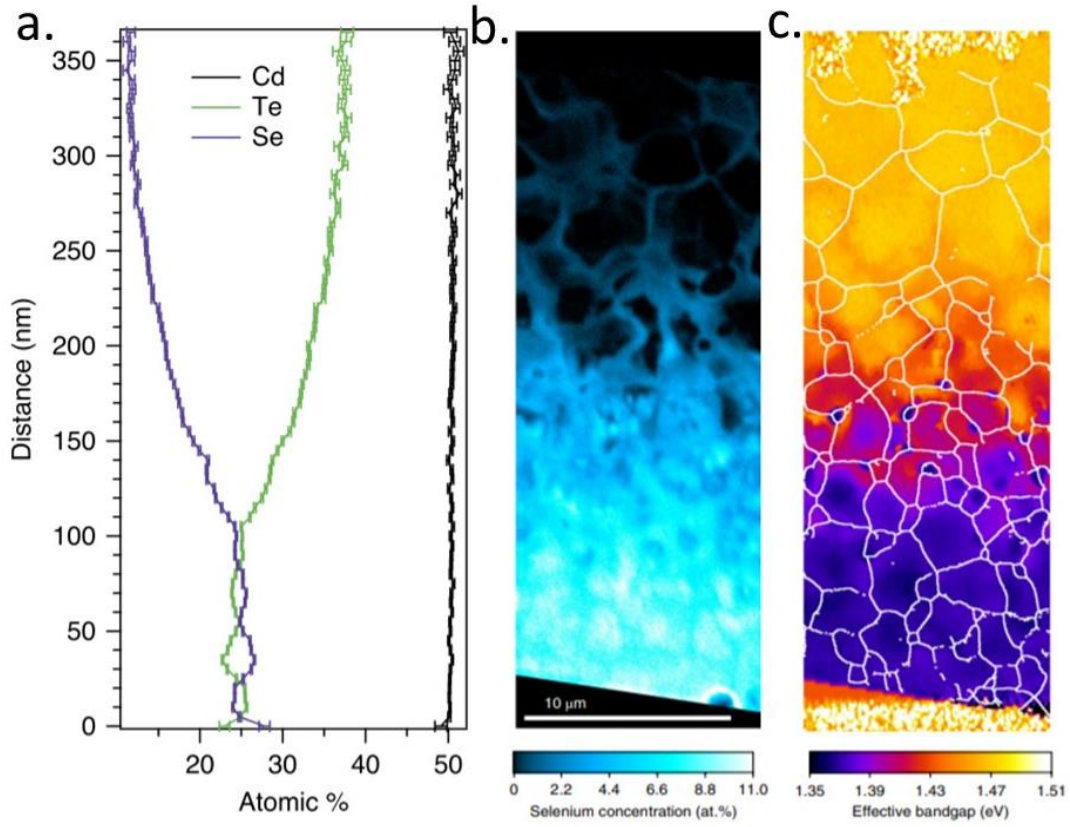

Figure 3.8: *a) Atomic probe spectroscopy showing the Se distribution away from the from CdSe/CdTe interface taken from ref*[87]*. b) SIMS mapping of the Se content in a* $CdTe_{(1-X)}Se_{(X)}$ *layer, c) CL mapping showing the effective bandgap of different regions of the* $CdTe_{(1-X)}Se_{(X)}$ *layer taken from ref*[84]*.*

Fiducia *et al*.[84] similarly reported a graded Se content using secondary ion mass spectrometry (SIMS) mapping. It was also shown that the Se diffused predominately along and accumulated at the grain boundaries in much the same fashion as chlorine[84]. PL and CL imaging showed that the grain boundaries had a reduced level of recombination and increased carrier lifetime, the inference being that Se was having a similar passivating effect as chlorine and that the reduced recombination was contributing to the enhanced carrier lifetime and performance. Figure 3.8b and c show the SIMS and CL maps generated for $CdTe_{(1-x)}Se_{(x)}$ based devices[84].

Currently the most common way of incorporating Se into the CdTe device is to use sputtered CdSe layers and rely on thermodynamic diffusion to produce the desired $CdTe_{(1-x)}Se_{(x)}$ phase[6,29,94,95]. An alternative and arguably more successful route to form the $CdTe_{(1-x)}Se_{(x)}$ phase is to use the co-sublimation of CdTe and CdSe. This creates a large grained $CdTe_{(1-x)}Se_{(x)}$ layer and offers more control of the $CdTe_{(1-x)}Se_{(x)}$ phase, yielding a higher performance. Munshi *et al*[96]*.* have demonstrated a performance of over 19% utilising this method with J_{SC} values of over 28 mA cm^{-2} in CdS free devices. This demonstrates the high performance that can be achieved using this method, however, a bespoke dual CSS system was required, where the $CdTe_{(1-x)}Se_{(x)}$ and CdTe can be deposited separately and the Se content in $CdTe_{(1-x)}Se_{(x)}$ layer can be controlled. This makes it difficult for other groups to replicate this level of performance. However, it demonstrates the level of performance that can be achieved by optimising the Se content. Other techniques that have been used to deposit CdTe could potentially also be used for producing $CdTe_{(1-x)}Se_{(x)}$ devices, such as MOCVD and MBE.

There is significant scope for further research in the exact role of Se in CdTe devices, whether a more controllably graded band structure can be achieved, resulting in further improvements to performance and if the passivating effects of Se can be adopted to the entire device stack.

3.4.2. Alternative window layers

As previously mentioned use of CdS as the device window layer will always have its limitations due to parasitic absorption, meaning the maximum attainable J_{SC} will always be reduced. The incorporation of Se into CdTe led to the realisation that a high V_{OC} can be achieved in CdS free devices and has led to significant research and development into the design of new window layers and architectures for CdTe PV devices. A number of different layer have thus far been investigated such as, ZnS[97], ZnO[98], TiO_2[99], SnO_2[100] and in particular MZO[101].

Use of CdS was long thought to be essential as the use of alternatives led inferior device interfaces, a reduced V_{OC} and performance. The reduced performance is due to a number of factors such as poorer band alignments and an enhanced lattice mismatch. Use of TiO_2 and ZnO resulted in a conduction band offsets with CdTe of - 0.6 eV and - 0.1 eV respectively and resulted in a reduced *FF* and performance[98,99]. Oladeji *et al*[97]. demonstrated a reduced level of performance when ZnS was used as the window layer rather than CdS, it was suggested that this was due to the enhanced lattice mismatch of ZnS/CdTe compared to CdS/CdTe, 16% and 10% respectively.

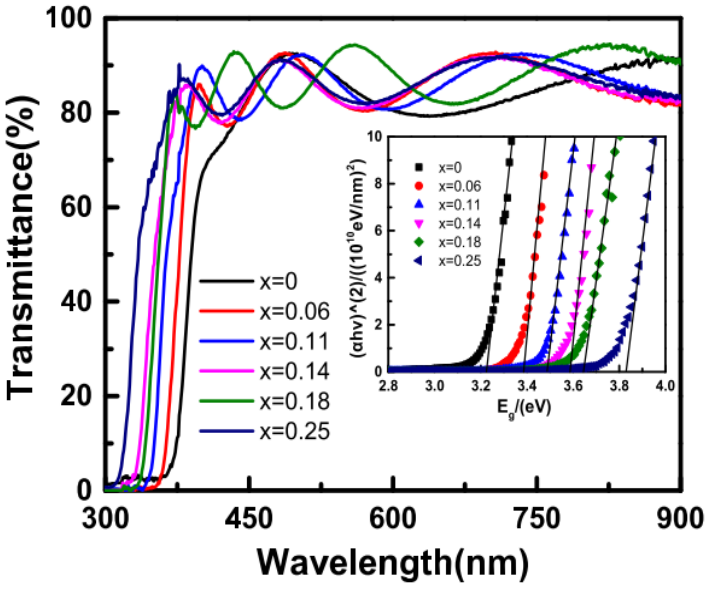

Figure 3.9: *Optical transmission curves demonstrating the effect of an increasing Mg content in MZO films, insert shows the bandgap shift as a result of Mg content taken from ref* [102].

In recent years MZO has emerged as a potential window layer for CdTe PV and a high performance has been achieved, over 19% in MZO/$CdTe_{(1-X)}Se_X$ devices[96]. However, the performance of MZO based devices depends on a number of parameters such as, Mg content[102,103], O content[28,101], conductivity[95] and thickness making MZO more challenging than CdS to optimise[28,29]. MZO is an attractive choice as a potential window layer because depending on the Mg content in the film the bandgap can be tailored between the ZnO and MgO bandgaps from approximately 3 eV to over 7 eV, Figure 3.9 shows the influence of Mg content on MZOs bandgap measured by optical absorption[102,104,105]. This means that, theoretically, the band alignments can be controlled and optimised so that the band structure can be tailored and thus result in superior performance. MZO layers are typically fabricated by sputtering from either a single target[33] or from ZnO and MgO targets[103] although they have also been produced using solution methods such as sol-gel[106].

Initially MZO was developed as a HRT layer in much the same fashion as ZnO and SnO_2, and used effectively in both MZO/CdS/CdTe and MZO/CdS/CdSe/CdTe devices. It has been demonstrated that MZO improves the band alignments in CdS/CdTe devices, enhancing carrier transport between the CdS and TCO layers. However, the conductivity of the MZO layer needs to be finely controlled[28,95]. Ren *et al*[29,95]*.* demonstrated that the addition of Mg into the ZnO increased the resistivity of the films and resulted in "S-shape" *JV* curves. It was also found that post growth annealing enhanced the film's conductivity and led to removal of the S-shape which enhanced device performance.

S-shaped *JV* curves indicate a barrier to extraction has formed at the device interface (see Section 2.2.2.3.1), when either i) the band alignment between the two layers has not been optimised resulting in a spike like barrier or ii) when the resistivity of the device layers becomes too high reducing carrier lifetime and enhancing recombination[107]. Therefore, to remove the S-shape *JV* curves, either the band structure needs to be improved and/or the device layers need to be more conductive so photo generated carriers can overcome the

barrier[108]. S-shaped *JV* curves are rarely seen in the CdTe PV. This is primarily because until recently CdS was used almost exclusively as the device window layer. As the research community investigates and optimises new window layer structures more S-shaped *JV* responses can be expected. S-shaped JV curves are commonly seen in organic PV as a number of contact layers are commonly investigated meaning extraction and injection barriers are more routinely seen until the optimal partner layer is found and several arguments for extraction barriers used in this thesis are based on work conducted on organic PV devices. The presence and removal of S-shaped *JV* curves will be discussed in more detail in Chapter 6.

Whilst the MZO has effectively been used as a HRT buffer layer, due to the fact that its material properties can be tailored, it has also been investigated as a direct replacement for CdS. This approach eliminates parasitic absorption and the bandgap allows the band alignment to CdTe to be optimised. However, work on MZO as a window layer is in its infancy. Munshi *et al.*[109] reported a performance over 18% in MZO/CdTe based devices, perhaps most remarkably is that these demonstrated a large V_{OC}, > 860 mV. Kephart *et al.*[28] identified that a Mg content of 23 atomic % is needed to produce a near optimal band alignment to CdTe and performance, as this composition results in only a small spike in the conduction band of approximately + 0.3 eV. A small spike in the conduction bands has been shown to be beneficial for device performance as this reduces recombination and increases the V_{bi} (see Section 2.2.2.3.1)[110,111]. Bittau *et al.*[112] demonstrated that for an optimal performance to be achieved, both the deposition conditions and Mg content need to be carefully controlled and optimised. Figure 3.10 shows how increasing the MZO sputtering deposition temperature effects V_{OC} and device performance.

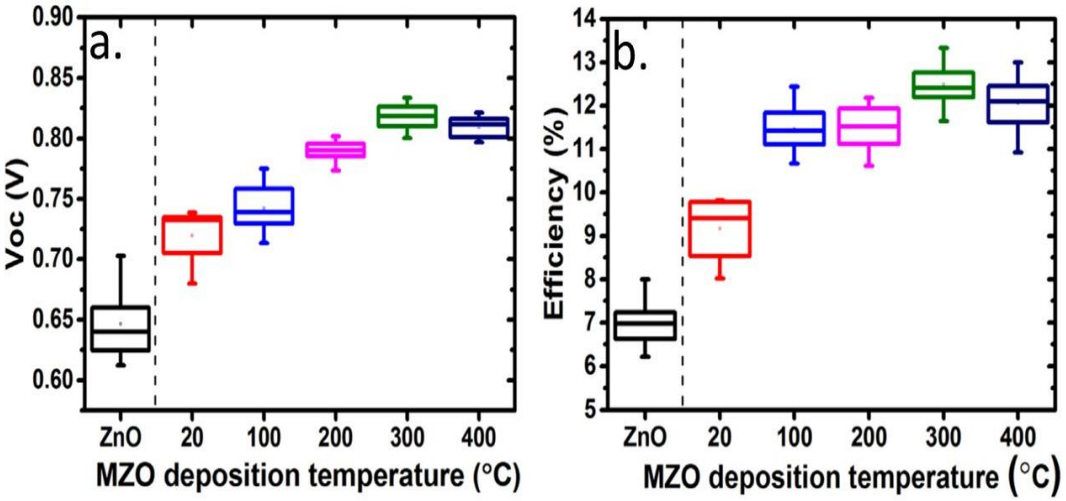

Figure 3.10: *Demonstrates the influence of MZO deposition temperature on device V_{OC} (a) and efficiency (b) taken from ref*[112].

Despite the early high performance that has been achieved there still remains significant questions about MZO based devices and because of the large number of parameters that require optimising the production of device quality MZO remains a challenge. The exact band structure produced by the MZO/ CdTe interfaces still requires evaluating, in particular how it changes with varied Mg content. There also remains only a few studies on the use of MZO in $CdTe_{(1-X)}Se_X$ devices. Munshi *et al.*[96] demonstrated a performance of over 19%. However, the focus of this study was the optimisation of the $CdTe_{(1-X)}Se_X$ layer rather than optimisation of the MZO layer. The MZO layer that was used had the same composition as for the CdTe based devices. However, due to the different bandgap of the $CdTe_{(1-X)}Se_X$ layer, a different composition may be required. Further investigations are clearly required in order for the MZO to be optimised in this device structure and Chapter 6 will present an in-depth study on the optimisation of MZO for $CdTe_{(1-X)}Se_X$ devices.

3.4.3. Group V doping and single crystal devices

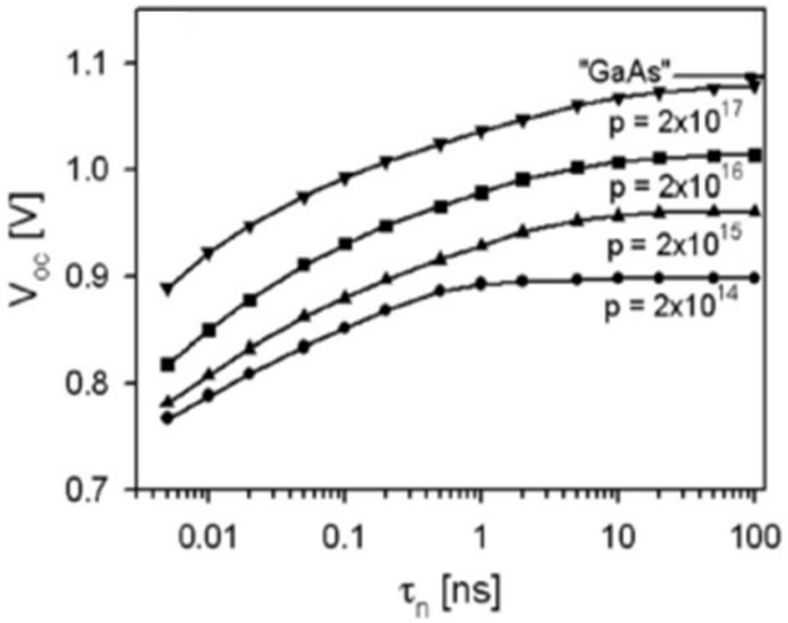

Figure 3.11: *Shows how increasing the doping density of CdTe impacts device V_{OC} taken from ref*[69]*.*

As mentioned previously CdTe suffers from a low doping density of (< 10^{15} cm^{-3}) and the presence of deleterious grain boundaries means that the level of recombination in CdTe devices is high and carrier lifetime is low, typically on the order of a few ns, this accounts for the low device V_{OC}. Figure 3.11 shows modelling predictions for how the CdTe doping density and carrier lifetime effects V_{OC}[69]. This model implies that in order for a higher V_{OC} than the current 880 mV limit to be achieved the doping density and/or minority carrier lifetimes of the CdTe layer needs to be increased[54,60].

Group V dopants have demonstrated a high doping density in CdTe, with P[32], As[61] and N[113], demonstrating a doping density of 10^{16}-10^{17} cm^{-3}. It has been shown that for P and As doping on a Te site has a higher rate of activation of up to 50%, Figure 3.12a shows the doping density achieved with P and the activation rate of the doping[32].

To date, the majority of the work undertaken on group V dopants has been on single crystal CdTe layers, as this has been found to be an easier way to incorporate toxic elements like P and As into the CdTe layer[32,57]. Whilst high doping densities have been

achieved for single crystal devices, the use of group V dopants in polycrystalline CdTe PV devices remains relatively unexplored, with only a few groups demonstrating a high performance. MOCVD CdTe devices have regularly demonstrated high doping using As. However, the V_{OC} and carrier lifetimes produced by these devices were similar to those achieved using Cu as a dopant[22,61]. As Figure 3.11 suggests increasing the doping density will only be beneficial to V_{OC} if the carrier lifetime can be maintained or increased i.e. increasing carrier density in isolation is not enough.

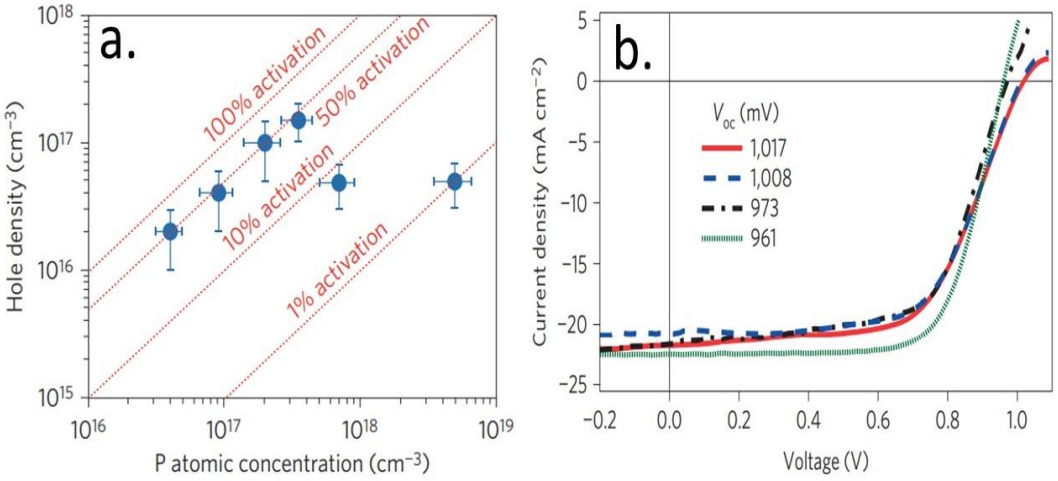

Figure 3.12: *a) Hole density as a function of P atomic concentration and b) JV curves produced for the single crystal P doped CdTe device, images taken from ref*[32].

One likely reason for the low carrier lifetimes is the negative impacts of grain boundaries. Therefore, there has been development work on single crystal CdTe with alternatives dopants to try and test the impact of grain boundaries. Duenow *et al.*[57] fabricated Na doped single crystal CdTe devices using the Bridgman method and showed a V_{OC} greater than 900 mV with enhanced carrier lifetimes, 10 ns. The inference from the high V_{OC} was that grain boundaries in polycrystalline CdTe are indeed detrimental to device recombination, particularly given that the doping density was still low (10^{15} cm^{-3}). Burst *et al.*[32] fabricated single crystal CdTe devices doped with P and achieve a high doping density (10^{17} cm^{-3}), showing large enhancement of the carrier lifetime (up to 400 ns) and a V_{OC} > 1 V. Figure 3.12b shows the device *JV* produced by the p doped single crystal devices. This

result was particularly significant for the field as it was the first time a V_{OC} of > 1 V had been reported. This highlighted the potential performance gains possible if it could be transferred to thin films.

It should be mentioned that the performance of single crystal device is still lower than the polycrystalline alternatives 15.2% compared to 22.1%. The reduced performance is primarily due to the reduced *FF* and enhanced R_S of the single crystal devices. Nonetheless the properties of heavily p-type doped single crystal devices does indicate that grain boundary recombination and low doping densities are potentially the limiting factors in polycrystalline CdTe and it remains to be seen whether these properties can be transferred to polycrystalline CdTe PV devices.

3.5. Summary

This chapter has outlined the current state of research in CdTe PV devices, from the traditional CdS/CdTe to the more novel device architectures being currently developed. The fundamental properties and device fabrication considerations of CdS/CdTe devices has also been discussed as well as the limitations of this device structure such as parasitic absorption in CdS and the low doping density of CdTe.

An overview of recent attempts to try to overcome these limitations was also presented such as Se incorporation into the CdTe layer forming the lower bandgap $CdTe_{(1-X)}Se_X$ phase, replacing CdS as the window layer with alternatives, particularly focussing on MZO and attempts to increase the doping density by doping the CdTe layer with group V dopants.

Overall this chapter demonstrates that despite the relative age of the CdTe technology and amount of research undertaken over the years there still remains significant scope for further development. This indicates understanding the exact role of grain boundaries in the CdTe layer, the role of Se in the $CdTe_{(1-X)}Se_X$ devices, window layer/$CdTe_{(1-X)}Se_X$ interface

optimisation and increasing the doping density and minority carrier lifetimes so polycrystalline device V_{OC} can be enhanced.

3.6. References

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4. Experimental techniques

4.1. Introduction

During this work a range of experimental techniques were used to grow and characterise thin films and photovoltaic devices. In this chapter the techniques used will be described in three sections. In Section 4.2 the thin film growth techniques and processing methods used to produce the solar cells will be discussed. Section 4.3 will present the thin film characterisation techniques used to determine the structure, morphology and chemical composition of the films. Finally, Section 4.4 will describe the electrical characterisation techniques used to determine CdTe device performance.

4.2. Thin film growth techniques and device processing

This section will describe the methods used to grow and process the thin films and solar cells produced in this work. Details of "typical" growth and processing conditions will be described. However, where alternative conditions were used then they will be given in the result chapters.

4.2.1. Physical vapour deposition techniques (PVD)

4.2.1.1. Thermal evaporation

Thermal evaporation is one of the most common physical vapour deposition (PVD) techniques as it can be used to deposit a variety of materials, such as metals and metal oxide thin films[1–3]. The technique works by heating a resistive heat source to a desired temperature under high vacuum (5×10^{-4} Torr) until a vapour flux is generated, a high vacuum is required because a long mean free path length is necessary in order to reduce the number of collisions and increase the rate of deposition. Figure 4.1a shows the schematic diagram of a typical evaporation chamber, where the material to be evaporated is placed in an evaporation boat at the base of the chamber. The vapour then condenses onto the chosen substrate mounted with line of sight to the evaporation source. Working distance variations can lead to non-uniformities. This can

be improved by turning the substrate rotation on. The choice of evaporation boat material is dependent on source material to be deposited, as some materials alloy with boat materials (typical boat materials are Mo, Ta and W).

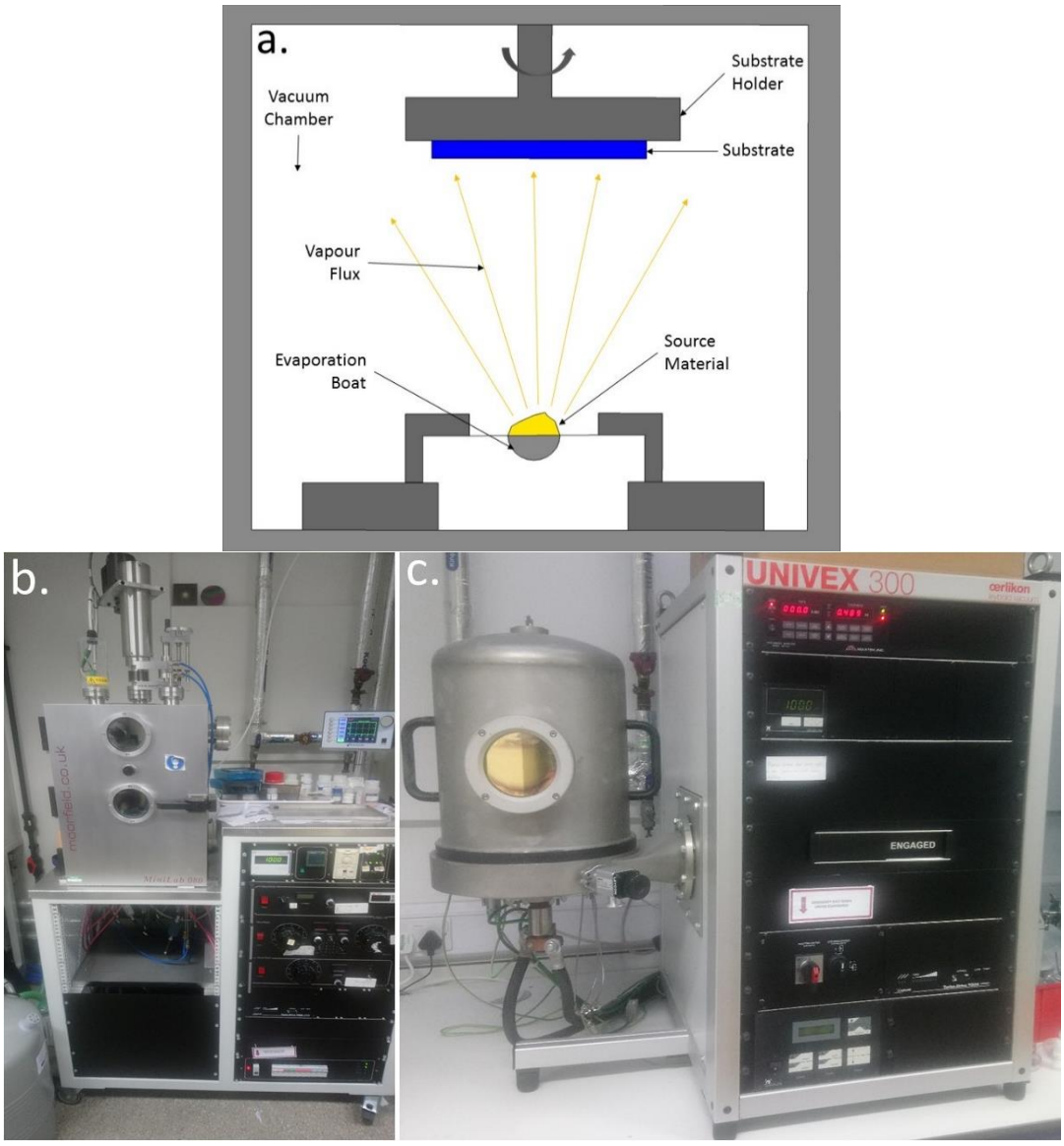

Figure 4.1: *a) Schematic diagram of a typical thermal evaporation chamber. b) Moorfield Minilab 080 evaporated used to deposit Cu and c) Oerlikon UNIVEX 300 thermal evaporator used to deposit Au in this work.*

For this work, a Moorfield MiniLab 080 thermal evaporation system was used for evaporation of 5 nm Cu using a Mo evaporation boat and an Oerlikon UNIVEX 300 was used for deposition of 50 nm Au for back contacting using a Mo or W evaporation boat, all depositions were carried out at room temperature. Figure 4.1b and c shows photographs of the evaporators used during this work.

4.2.1.2. Sputtering deposition

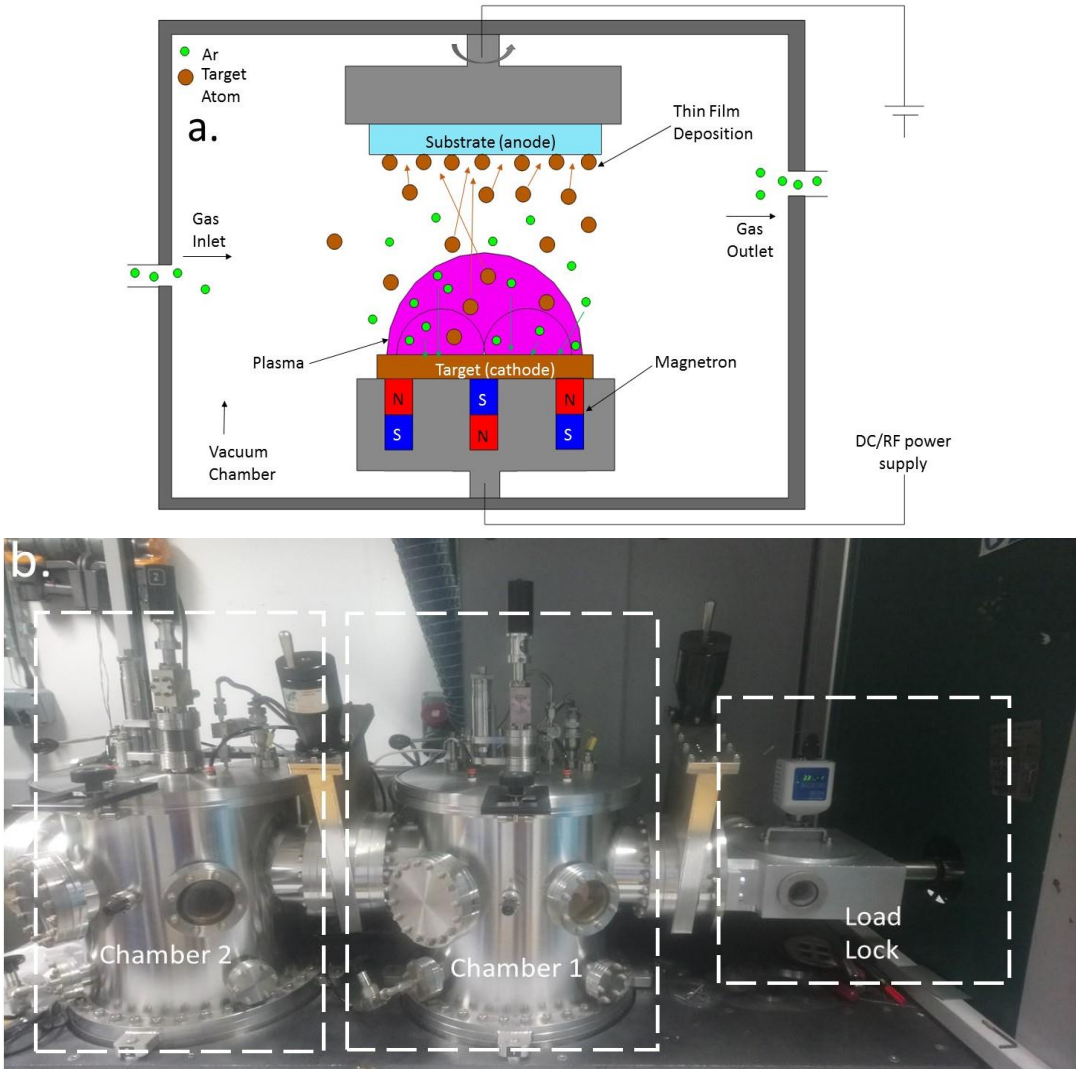

Figure 4.2: *a) Schematic representation of a typical sputtering process, b) Orion chamber system from AJA international Inc.*

Sputtering is a thin film deposition process that is used to produce a wide range of semiconductor and optical devices, on both laboratory and industrial scales. Sputtering can be used to produce high quality, homogenous and pure thin films such as, CdTe, CdS and ZnO[4–6]. Sputtering can also be used to deposit materials with very high melting points such as Pt and Mo where evaporation of these materials using resistance thermal evaporators would be difficult or impossible.

Figure 4.2a shows a schematic representation of a typical sputtering process. Briefly, the sputtering process works by firstly applying a potential to the target material, a gas

usually inert (typically Argon), is then ionised to form the plasma source. the generated ions are then accelerated towards the target. The potential applied is dependent on the target material, direct current (DC) or radio frequency (RF) can be used. DC is typically used for conductive targets, such as metals, and RF is used for more insulating materials, such as semiconductors and oxides.

The bombardment of these ions onto the target's surface causes the material of choice to be ejected from the target, which is then deposited onto the desired substrate. The number of atoms emitted from the targets surface is called the sputter yield. The sputter yield depends on several properties such as, target material, chamber pressure, potential to the target and temperature of the substrate.

One of the drawbacks of sputtering is it tends to be slow, ≈ 5-10 nm/min, and the bombardment of the target can lead to overheating of the target, potentially damaging the target material or sputtering guns. To combat this, the targets are water cooled to prevent the targets from overheating. To increase the sputter yield, magnetron sputtering can be used, where magnets are used to trap electrons in the magnetic field, enhancing both the efficiency of the ionisation process and allowing the plasma to be generated at lower chamber pressures, increasing the mean free path length of the ejected material. For more details on the sputter process, the reader is referred to references[7–9].

In this work, AJA international Inc. ATC Orion chambers (see Figure 4.2b for a photograph of the equipment used in this work) were used for the deposition of a variety layers such as, CdSe, CdS, ZnO, MgO and MZO. All layers in this work were deposited via RF sputtering. The base pressure in the chamber is $1x10^{-6}$ Torr. If required, the substrate can be heated to a desired temperature. Specific deposition temperatures will be described in the relevant chapters. The substrates can be rotated to produce a uniform film. All depositions in this work were carried out at 5mTorr. The working gas during this work was either pure argon or a mixture of argon and oxygen. See specific results chapters for specific

deposition parameters. Each deposition chamber contains more than one sputtering gun. This enabled production of co-sputtered materials. The co-sputtered approach was used to produce MZO films from MgO and ZnO targets in Section 6.2. See the relevant experimental sections of each results chapter for a more detailed description of the growth parameters used in this work.

4.2.1.3. Close space sublimation

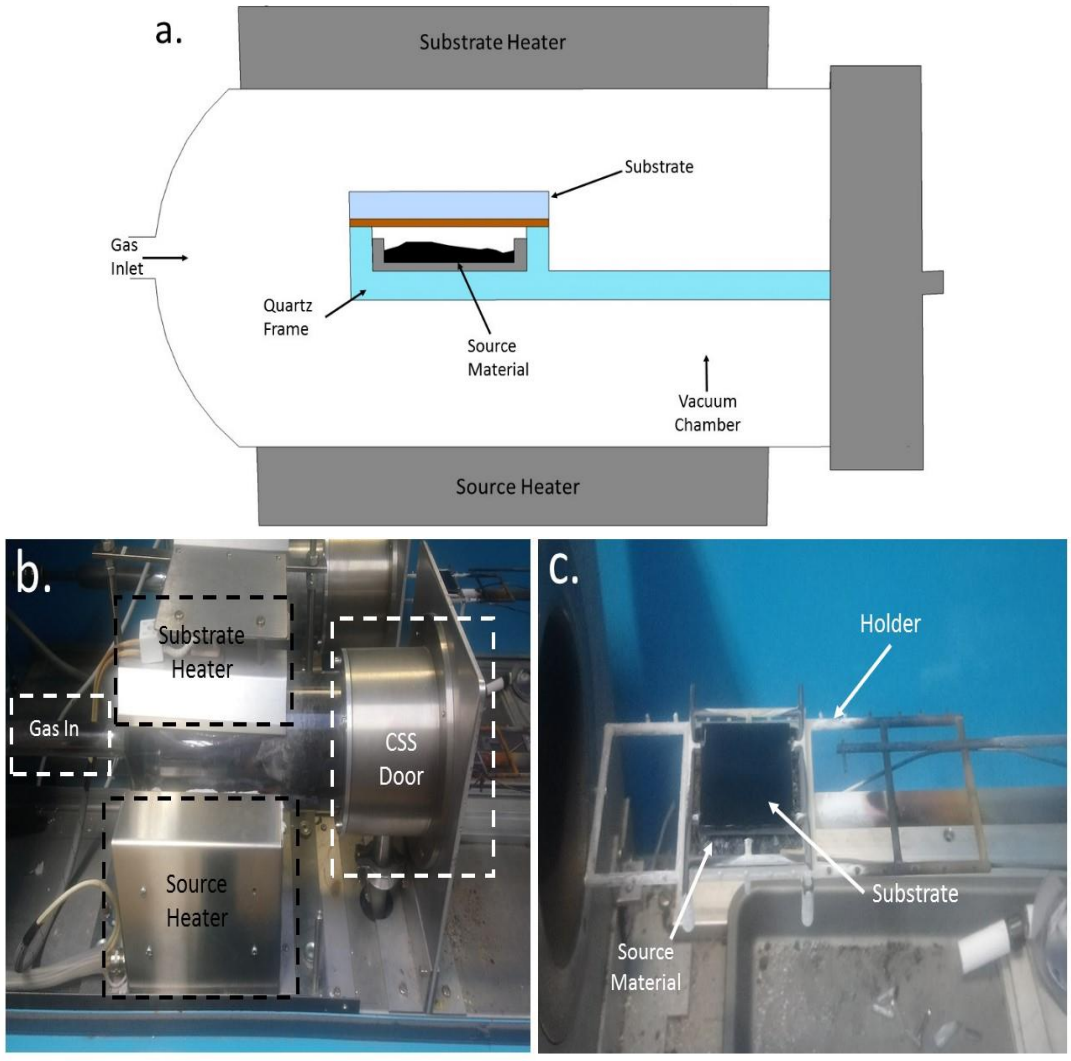

Figure 4.3: *a) Schematic representation of the CSS chamber used in this work. b) Shows the heaters and chamber of the Electro-Gas System Ltd. CSS system used in this work and c) source and substrate arrangement for this system.*

Close space sublimation (CSS) is a PVD technique used for depositing materials with high melting points typically > 1000°C[10]. Rather than being evaporated, the chosen material

sublimes, forming a vapour density suitable for deposition at a temperature far below the material's melting point. However, due to a relatively rough vacuum (0.1-1 Torr), CSS results in a very low vapour density and so the substrate must be placed near to the source material (5-10 mm). To ensure good film uniformity, the source tray is typically larger than the chosen substrate. Figure 4.3a shows a schematic representation of the CSS chamber used in this work.

CSS has been used to successfully deposit a wide range of materials, such as CdS, CdSe, CdTe and Sb_2Se_3 which have melting points of 1750°C, 1240°C, 1041°C and 611°C, respectively[11–14]. CSS is widely used for the deposition of CdTe in CdTe thin film solar cells, as it has a number of advantages, such as high deposition rates and production of a large grained material (typically microns in size)[4,15].

CSS growth of CdTe usually takes place between 500°C and 600°C (source temperature) and at pressure on the order of tens of Torr. Under these conditions, a CdTe vapour pressure can be produced which results in the direct sublimation of CdTe and the reversible dissociation to it component elemental vapours (see Equation 4.1) before condensing on the substrate due to temperature gradient between the source and substrate (< 100°C) and recombining to form a CdTe thin film. The temperature gradient can be controlled by monitoring the temperature of the source and substrate temperatures independently.

$$\boldsymbol{2CdTe_{(s)} \leftrightarrow 2Cd_{(g)} + Te_{2_{(g)}}} \qquad \textit{Equation 4.1.}$$

Figure 4.3b and c shows a photograph of the custom-built CSS system by Electro-Gas Systems Ltd. used in this work. The chamber, source tray and substrate holder are made of high purity quartz glass[16]. The base pressure reached in the chamber is 10^{-1} Torr. The source temperature is controlled by a tungsten coil heater and the substrate temperature was controlled by an infrared ceramic heater. Although both heaters can be controlled

independently, due to the close proximity of the source and substrate, the temperature gradient in this work was provided by only the source heater. The temperature was monitored via thermocouples. Furthermore, a range of gas ambient conditions can be utilised during deposition, including gas flows of N_2, O_2, H_2 or a mixture of N_2/H_2 and N_2/O_2. In this work, CSS was used to deposit 5-6 μm of CdTe at a source and substrate temperature of 610°C and 510°C respectively. The CdTe growth was, in general, performed via a two-stage process: 1) a 'high pressure' growth at 30 Torr (3.99 KPa) in a nitrogen atmosphere, and 2) a 'lower pressure' growth at 1 Torr (133.2 Pa). The growth at a 'higher pressure' facilitates larger grain growth. However, to overcome the possible formation of pinholes, the deposition is completed by growth at a lower pressure to aid pinhole blocking[15]. Specific deposition parameters will be described in the relevant results chapters.

4.2.2. Spin coating

Spin coating is a simple and a relatively easy process that can be used to deposit a wide range of materials, such as semiconductors, metal oxides and nanomaterials. As a result, the spin coating technique is used in semiconductor and nanotechnology research & development (R & D)[17,18]. However, the disadvantage of spin coating is that as a single substrate process, it has a relatively low throughput compared to other techniques such as roll-to-roll manufacture. The material usage is also very low (around 10%), with the rest being wasted, whilst this is not issue for R & D, it clearly not suitable for large scale manufacture. Despite its disadvantages, spin coating remains the usual starting point for many academic and R & D processes.

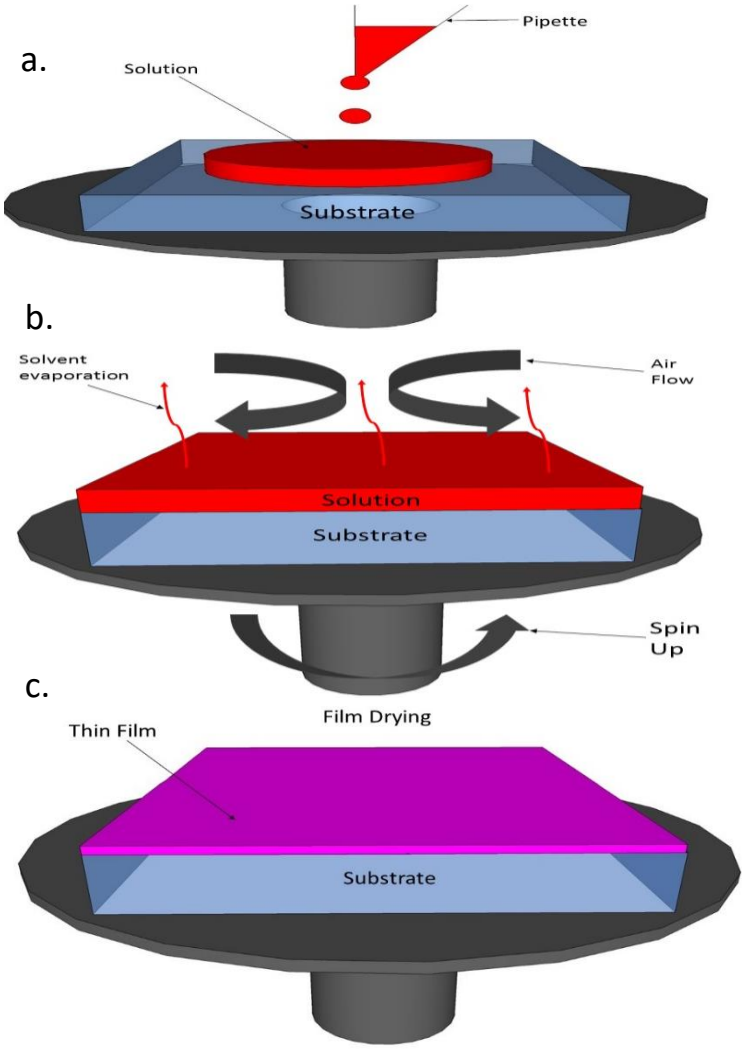

Figure 4.4: *Schematic representation of a typical spin coating process. a) Solution dropping, b) sample rotation and the removal of excess solvent, c) evaporation of solvent and formation of thin film.*

A typical spin coating process is done in three stages. Firstly, the substrate is coated in the solvent containing the dissolved molecules. Then the film is rotated at high speeds typically 1000 rpm to 6000 rpm, with most of the solution being thrown off the side and the airflow drying the solvent. Lastly, when the film has fully dried typically using a curing step, a uniform thin film is left on the substrate surface. The thickness of the film is controlled by a number of factors, such as concentration of the solvent, boiling point of the solvent and is inversely proportional to the spin speed squared, as shown in the following equation.

$$t \propto \frac{1}{\sqrt{\omega}}$$ ***Equation 4.2.***

where t = thickness and ω = angular velocity.

Figure 4.4 shows a schematic representation of a typical spin coating process. An Ossila spin coater was used in this work to deposit TiO_2. TiO_2 was deposited in a glove box in a nitrogen atmosphere via a two-step process at 3000 rpm^{-1} for 30s from titanium isopropoxide in ethanol. The first stage was the deposition of a 0.15 M solution which was then annealed at 110°C for 10 mins, followed by a second deposition of a 0.3 M solution which was again annealed at 110°C for 10 mins. The bilayer was then treated at 550°C for 30 mins in air[18].

4.2.3. Post growth treatment of CdTe device

In this work, the chlorine treatment of CdTe devices was performed using $MgCl_2$ rather than the conventional $CdCl_2$[19]. The $MgCl_2$ treatment was performed via spray deposition of a 1M $MgCl_2$ solution in H_2O, samples were then annealed in a tube furnace in an air ambient. Due to the varied device structures used in this work, re-optimisation was often required, meaning a range of temperatures was used to produce efficient devices. The specific chlorine treatment temperature will be described in the results chapters, but was typically in the range of 410°C and 430°C. The annealing time was also varied. Again, the specific annealing time will be described in the relevant results chapters but was in the range of 20 mins to 120 mins. Following the annealing step, excess $MgCl_2$ was rinsed from the back surface using de-ionised water. Prior to the back contact assembly, the CdTe back surface was nitric-phosphoric (NP) acid etched by submerging the sample in the NP solution for 15s to facilitate the formation of a Te-rich surface. The etching solution was a mixture of 1% nitric acid, 70% phosphoric acid and 29% de-ionised water[20].

4.2.4. Device fabrication

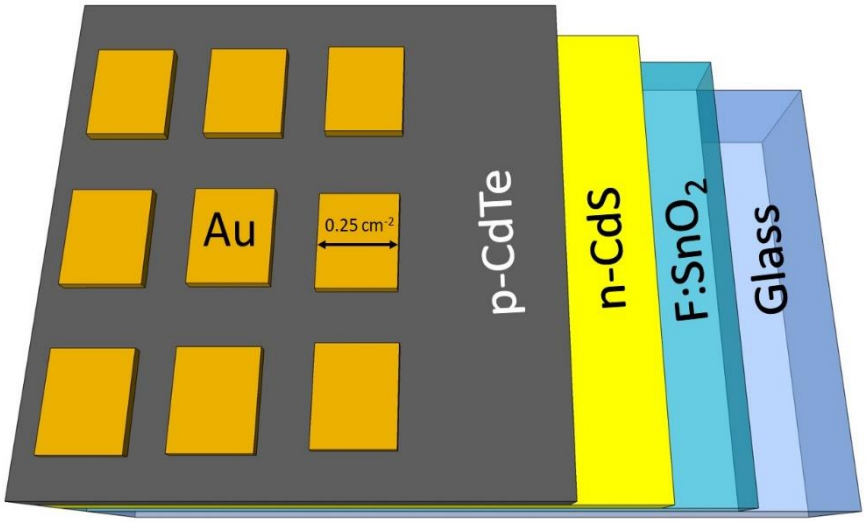

Figure 4.5: *Shows a schematic representation of the standard CdTe PV devices fabricated in this work.*

The CdTe devices produced throughout this work were fabricated in the conventional 'superstrate' configuration, Figure 4.5 shows a schematic representation of standard CdTe PV device fabricated in this work. All devices were deposited on NSG^{Ltd} soda lime TEC^{TM} 15 glass (F doped SnO_2 (FTO) coated glass). CdS was deposited via RF sputtering at room temperature, using a chamber pressure of 5mTorr using Ar as the working gas and a power density of 1.32 W cm^{-2}. CdTe was deposited via CSS as described in Section 4.2.1.3. All samples were then treated with $MgCl_2$ at 430˚C for 20 mins in an air ambient[19], samples were etched with a NP solution for 15s. All cells were completed by thermally evaporating 50 nm of gold to form the back contact, all cells had an active area of 0.25 cm^{-2}.

4.3. Material characterisation

4.3.1. Film thickness measurements

The thickness of the deposited films was determined using an Ambios XP-200 plus surface profiler. In surface profilometry, a probe moves along the surface of the sample in contact mode with a specified force. A constant force is maintained between the probe and substrate as the probe scans across the sample and any change in height is measured by

an optical deflection measurements system. Surface profilers can measure film thicknesses in range of nanometres to millimetres. Film thicknesses were determined by measuring step height difference between the film and the substrate surface, see Figure 4.6. The steps were made by either mechanically scribing, etching or masking the sample during fabrication.

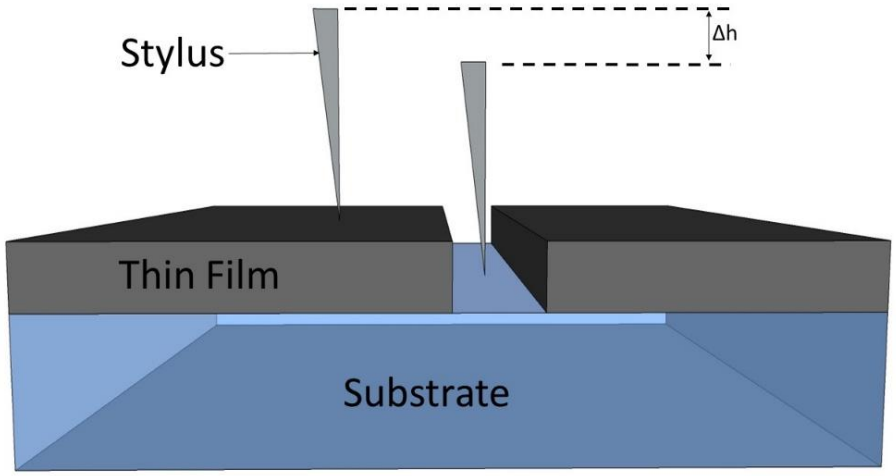

Figure 4.6: *Surface profiler measurement of sample thickness.*

4.3.2. Optical spectroscopy

Optical spectroscopy is a technique commonly performed on liquids and solids that undergo electronic transitions, where an electron jumps from lower energy state to a higher energy state. In the case of thin films optical measurements are typically performed using a monochromated light source in order to detect the films absorbance, transmission and reflectance properties [21]. The absorption coefficient can be calculated from transmittance and reflectance data using the following equation:

$$\alpha = \frac{1}{t} ln \left[\frac{1-R^2}{T}\right] \qquad \textbf{\textit{Equation 4.3.}}$$

where, α = absorption coefficient, t = film thickness, T = transmittance, R = Reflectance.

From the absorption coefficient, the material's bandgap (E_g) can be evaluated by using the Tauc method and Equation 4.4[22], where hv is the photon energy in electron volts, A is a constant and n is the exponent of the electronic transition.

By plotting the absorption coefficient as a function of photon energy ($\alpha h\nu$) of measured data against the photon energy ($h\nu$), the E_g is then evaluated by performing a linear extrapolation and measuring the intercept of the x-axis. If the material has a direct E_g then $n = \frac{1}{2}$ meaning $\alpha h\nu^2$ is plotted, whereas if the E_g is indirect then $n = 2$ then $\alpha h\nu^{\frac{1}{2}}$ is evaluated. In this work a Shimadzu SolidSpec – 3700 UV-Vis-IR spectrophotometer was utilised for transmission and reflection measurements.

$$\alpha(h\nu) = A\left(h\nu - E_g\right)^n \qquad \textbf{Equation 4.4.}$$

4.3.3. X-ray diffraction

X-ray diffraction (XRD) is a technique that is widely used for the phase determination and structural characterisation of crystalline materials. A number of parameters can be drawn from a material's XRD pattern such as lattice spacing, grain size, strain and texture[23].

Monochromatic X-rays are incident upon a crystal and are diffracted depending on the material's lattice spacing. The diffraction conditions are described by Bragg's law (Equation 4.5), which relates the constructive and destructive interference to the X-ray wavelength and angle of scattering from the lattice spacing d_{hkl} of the material. Figure 4.8 shows the interaction of incident photons with a material's lattice spacing.

$$n\lambda = 2d_{hkl}\,sin(\theta) \qquad \textbf{Equation 4.5.}$$

where, λ is the X-rays' wavelength, θ the angle between lattice plane and the reflected beam, d_{hkl} the spacing between the lattice planes and n is the order of diffraction, usually assumed to be 1.

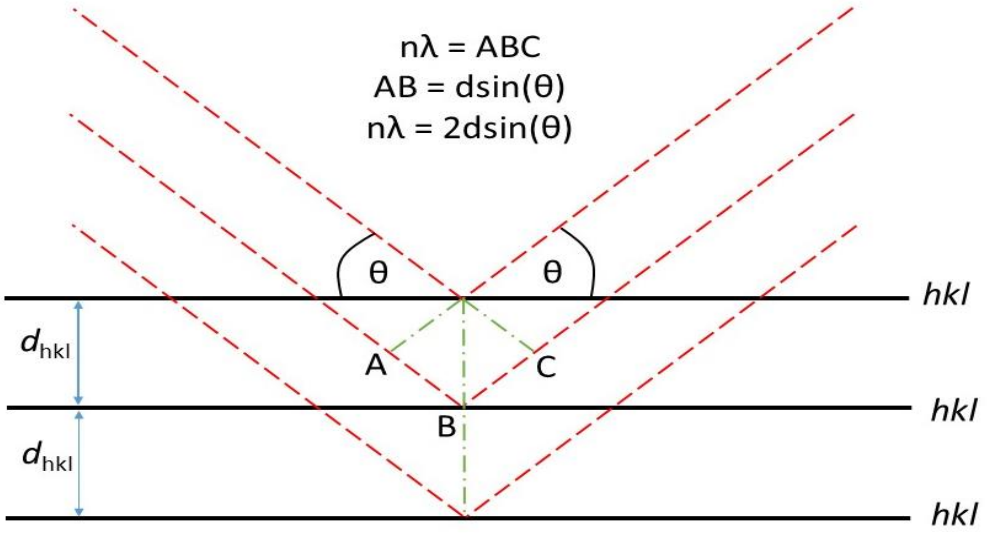

Figure 4.8: *Diffraction of X-rays by a crystal structure following Bragg's law.*

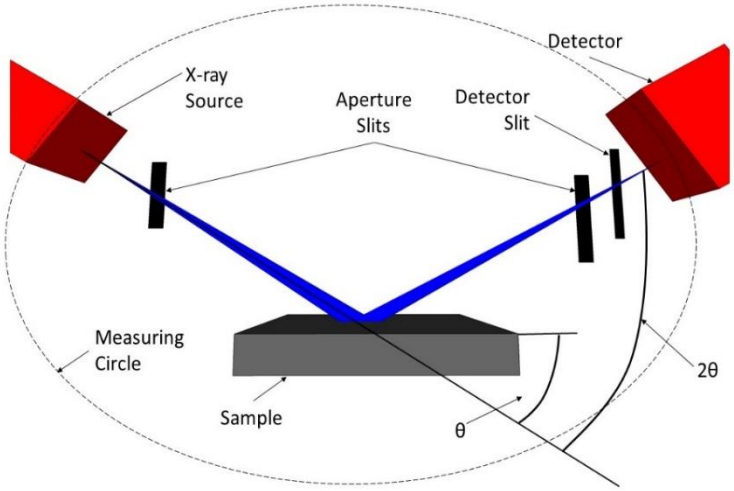

Figure 4.9: *Schematic representation of an X-ray diffractometer in the Bragg-Brentano geometry.*

For this work, a powder diffraction XRD method was used, with a monochromatic X-ray beam in the Bragg-Brentano mode as shown in Figure 4.9. X-rays are directed at a sample at an angle of θ, the X-ray beam is then diffracted at an angle of 2θ. Peaks are observed for angles that satisfy the Bragg conditions (Equation 4.5) and diffracted peak intensity corresponds to particular *hkl* plane for that material. The generated diffraction pattern can be used as a characterisation 'fingerprint' for the crystalline materials identification and structural determination. In this work, a Rigaku SmartLab XRD was used, with the emission at the Cu Kα (1.5406 Å) line, X-ray settings were 45kV and 200 mA.

From the calculated d_{hkl} values and crystallographic phase identified, the lattice parameters can be evaluated by using the appropriate equation. In this work, the lattice parameters were calculated for cubic and hexagonal structures using Equation 4.6 and Equation 4.7 respectively.

Cubic Structure: $$d_{hkl} = \frac{a}{\sqrt{h^2+k^2+l^2}}$$ **Equation 4.6.**

Hexagonal Structure: $$\frac{1}{{d_{hkl}}^2} = \frac{4}{3}\left(\frac{h^2+hk+k^2}{a^2}\right) + \frac{l^2}{c^2}$$ **Equation 4.7.**

where a,b and c are the lattice parameters.

In the Bragg Brentano mode, for a given angle θ, the planes orientated parallel to the substrate are diffracted, thus allowing for the preferred orientation, also known as texture, to be determined. Preferred orientation arises when there is a strong tendency for a crystalline powder or thin film to be oriented in one direction compared to other directions. The preferred orientation can be evaluated by using the Harris method, where the texture coefficient, C_{hkl} is estimated for a particular *hkl* plane, using Equation 4.8[24,25].

$$C_{hkl} = \frac{\frac{I_{hkl}}{I_{r,hkl}}}{\frac{1}{n}\sum_{n=1}^{n}\frac{I_{hkl}}{I_{r,hkl}}}$$ **Equation 4.8.**

where I_{hkl} is the measured intensity for the diffraction from a given *hkl* plane, with $I_{r,hkl}$ being the intensity of the diffraction from the same plane but for a randomly orientated sample and *n* is the number of peaks present.

A standard deviation, *σ* of the C_{hkl} values provides a measure of the overall spread of the data and thus the overall preferred orientation of the film. σ is calculated using Equation 4.9. Comparison of the *σ* values for different samples allows the level of preferred orientation to be compared, with a higher *σ* indicating a greater level of preferred orientation.

$$\sigma = \sqrt{\sum \frac{1}{n}(C_{hkl} - 1)^2}$$ **Equation 4.9.**

From the shape and position of the diffraction peaks, information on the grain size and strain can be obtained. The width of the diffraction peak is linked to grain size by the Scherrer equation, shown in Equation 4.10. A narrower diffraction peak typically results from a larger grain size than a broader peak[23,26].

$$L = \frac{k\lambda}{BCos(\theta)} \qquad \textbf{Equation 4.10.}$$

where, L is the grain size, λ is the X-ray source wavelength, B is the width of the peak at half maximum (FWHM) in radians, θ is the Bragg angle and k is the Scherrer constant which depends on the shape of the crystal and size distribution with a typical value 0.9.

4.3.4. Scanning electron microscopy (SEM) and secondary electron imaging

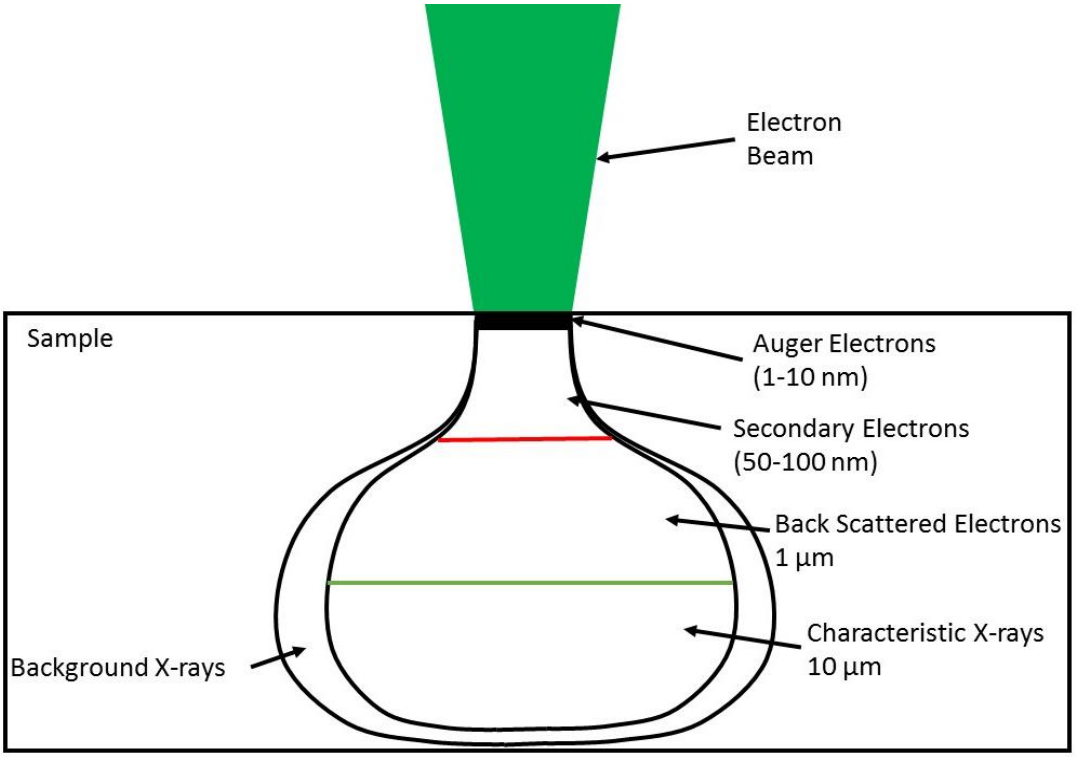

Figure 4.10: *Schematic diagram of the type of interactions produced when an electron beam is accelerated at a solid samples surface.*

Scanning Electron Microscopy (SEM) is a characterisation technique that allows microstructure to be visualised at a high level of magnification up to a few nanometres resolution [27]. It principally involves scanning an electron beam over a samples surface and detecting the electron and photon signals that are emitted. SEM is carried out under

vacuum and electrons are generated by an electron source, such as a tungsten filament. The electrons are accelerated at typically 5 – 30 kV and focussed towards the sample. Signals are then emitted from sample and are detected by a number of different detectors and the signal is then used to produce an image. Typical beam interactions with a sample are shown in Figure 4.10[28], a number of different techniques can be used to analyse the type of interactions produced by the sample form the electron beam.

The signals produced by the electron beam can be utilised in a number of characterisation techniques, such as electrons imaging; secondary electron, electron back scatter (Section 4.3.6), electron back scatter diffraction (EBSD) (Section 4.3.6), X-ray analysis; energy dispersive X-rays (EDX) (Section 4.3.8) and photon interactions and cathodoluminescence.

Secondary electron microscopy is the most common type of sample imaging used in the literature. In this work, the topological SEM images were taken using a JEOL JSM-7001F SEM and the cross-sectional SEM images were carried out using a Hitachi SU70 SEM.

4.3.5. Focussed ion beam

Focused ion beam (FIB) is a technique used in the semiconductor industry and materials science. The FIB set-up is similar to SEM. However, while the SEM uses a focused beam of electrons to image the sample, a FIB set-up uses a focused beam of ions instead, usually Ga ions. FIB systems can be operated at low beam currents for imaging or at high beam currents for site specific milling. The FIB can modify or mill the sample's surface. This milling can be controlled with nanometre precision. By controlling the energy of the ion beam, it is possible to perform nanomachining or the removal of unwanted material. FIB is typically coupled with an SEM in a dual system (FIB_SEM), as this allows for both high resolution imaging and accurate ion beam milling.

FIB milling is a commonly used to prepare samples for transmission electron microscopy (TEM), as TEM typically requires very thin samples (100 nm or less). The

nanometre scale resolution of FIB-SEM allows for the exact region of interest to be chosen and selectively milled away. The FIB beam voltage needs to be finely controlled in order to avoid surface damage[29]. Focussed ion beam (FIB) cross sections for SEM and STEM analysis were prepared using an FEI Helios MK2 Nanolab Dual Beam system.

4.3.6. Electron back scatter Diffraction (EBSD)

Electron back scatter diffraction (EBSD) is an SEM based characterisation technique that can be used to study crystalline materials. EBSD can identity individual grain orientations, local texture, strain, twin boundaries, phase identification and grain size. Back scattered electrons (see Figure 4.10) diffracted by atoms in a crystalline material are accelerated to a phosphor detection screen and generate Kikuchi lines, which produce a Kikuchi plot. A Kikuchi plot is a projection of the geometry of the crystal, meaning crystalline structure and orientation can be obtained for each grain imaged[28]. More information on EBSD can be found in the books by L.Reimer *et al.* and A. Schwartz *et al.*[28,30].

For EBSD images to be undertaken, a polished sample is placed in an SEM and then tilted approximately 70° relative to the electron beam. The EBSD detector is a camera fitted with an integrated phosphor screen. The camera is placed several mm from the surface of the sample. The Kikuchi lines on the phosphor screen are processed in order to produce a Kikuchi pattern. These patterns are used to identify the phase and orientation of the sample. Figure 4.11 shows a schematic representation of a typical EBSD set up.

In this work, EBSD samples were prepared by low broad ion beam milling using a Model 691 Gatan precision ion polishing system (PIPS) until the surface became mirror like. EBSD analysis of the plan-view and cross sectional samples was performed in a FEI Nano Helios Mk2 dual beam system, equipped with an Oxford instruments EBSD high sensitivity Nordlys S and Aztec acquisition software 2.2. The Kikuchi patterns were generated at 15 keV, 5000x magnification and 5.5 nA, with a working distance of 11 mm and EBSD step size of 0.2 μm.

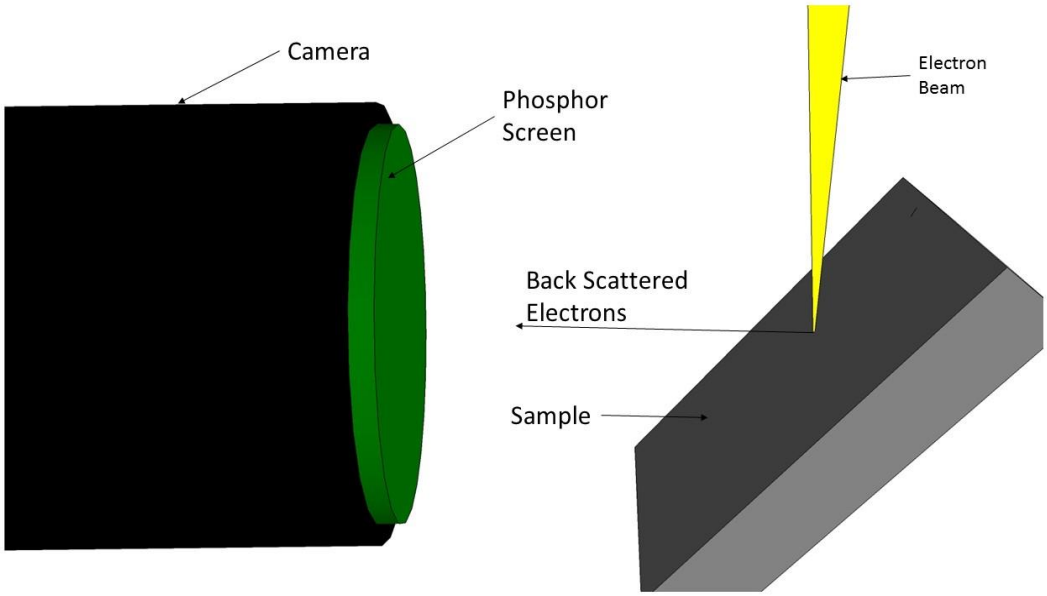

Figure 4.11: *Schematic* representation of a typical EBSD set up.

4.3.7. Transmission electron microscopy

Transmission electron microscopy (TEM) is a microscopy technique where an electron beam is transmitted through a sample and the interactions between the electrons and the atoms can be used to produce an image. TEM can be used to observe features such as crystal structure, dislocations and grain boundaries.

TEM operates on the same principle as light microscopy but uses electrons rather than light. As the size of electrons is much smaller than that of light. The wavelength of electrons has been measured to be on picometre scale (10^{-12}) compared to nanometres (10^{-7}) for visible light. Therefore, electron microscopy can resolve samples hundreds of thousands of times smaller than optical microscopy meaning an optimal resolution of less than a nanometre (0.2 nm) can be achieved. An image is formed from the interaction of the electrons transmitted through a specimen. The image is magnified and focused onto an imaging device, such as a phosphor screen or by a sensor such as a CCD camera[31]. In order for TEM to work, the sample must be very thin, typically less than 100 nm. In this work, TEM images were undertaken using a JEOL 2100F FEG TEM.

4.3.8. Energy dispersive X-ray analysis (EDX)

Energy dispersive X-ray (EDX) analysis uses the characteristic X-rays (see Figure 4.9) produced by a material when it interacts with the SEM and TEM electron beam. When the electron beam is incident on the sample, core electrons from the atom are ejected and the atoms will become ionized. This vacancy is then filled by an electron from the outer shell of the atom and a characteristic X-ray is emitted. The energy of the X-ray is the energy difference between the inner and outer electronic shells, this means the X-rays are characteristic of a particular element[31]. EDX may therefore be used to determine the composition of the material. In this work, the EDX spectra was undertaken using a JEOL JSM-7001F SEM and a JEOL 2100F FEG TEM using an energy dispersive X-ray spectrometer.

4.3.9. X-ray photoelectron spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) is a surface-sensitive quantitative technique that can be used measure the elemental composition, chemical state and electronic states present in a sample. XPS is a powerful technique as, not only can it identify the elements present in the sample, it can give information about the bonding and oxidation states present. XPS can also be used to probe the sample's Fermi level and valence band position relative to the vacuum level. However, XPS is highly surface specific, able to at most analyse only the first 5 - 10 nm of the sample. For an XPS spectrum to be obtained, an X-ray beam is incident onto a sample and the kinetic energy and number of electrons that are ejected from the samples surface are measured. XPS requires an ultra-high vacuum (UHV), 7.5×10^{-10} Torr, for an efficient spectrum to be taken. More information on XPS can be found at Ref[32].

In this work, XPS measurements were performed inside an ultra-high vacuum chamber operating at a pressure less than $1.5\text{x}10^{-9}$ Torr. Samples were secured to a sample plate using double sided carbon tape and a narrow strip of tantalum connecting the surface to the plate, to help prevent charging. Core-level electronic structure was probed using XPS

with a Mg Kα x-ray source (hv = 1253.6 eV) operating at 200 W and analysed with a hemispherical SCIENTA SES200 electron energy analyser comprised of a double channel plate and phosphor screen with a CCD camera. The resolution was determined from the full width at half maximum (FWHM) of an Ag $3d_{5/2}$ peak to be 0.6 eV, allowing binding energy determination with a precision of 0.1 eV.

4.3.10. Raman Spectroscopy

Raman spectroscopy is a technique used to observe the vibrational and rotational modes present in a sample, allowing analysis of the structural properties. Raman spectroscopy uses inelastic scattering from a monochromatic light laser source. The laser interacts with the vibrations or phonons in a molecule or compound which results in the energy shifting either up (Stokes) or down (anti-Stokes) in energy. These vibrational modes are then used to generate the structural fingerprint for that sample. One of the major drawbacks of Raman spectroscopy is that Raman scattering is a very weak phenomenon, 1 in 10 million photons are Raman scattered. Therefore, it can be difficult to separate Raman scattered light from Rayleigh scattered (elastic scattering) light[33]. In this work, Raman spectra were collected using a Horiba Xplorer Plus Raman microscope, utilising a 532 nm laser.

4.3.11. Secondary Ion Mass Spectroscopy (SIMS)

Secondary Ion Mass Spectroscopy (SIMS) is a widely used technique for semiconductor analysis[34]. It can be used to analyse the spatially resolved elemental composition throughout the thickness of a solid sample or thin film. SIMS involves a focused primary ion beam which sputters away surfaces of a sample. The primary ion beam interacts with the sample, resulting in some of the atoms being emitted and ionised. If the ion beam is positively charged, the resultant secondary ions produced are predominantly negatively charged and the reverse is true if the ion beam is negatively charged. Only a small amount of the ion's produced are ionised, with the majority being neutral. The secondary ions

kinetic energy can range anywhere from 0 to hundreds of electron (volts). The secondary ions that are produced are accelerated and focused towards a mass spectrometer, to measure the ratios of the emitted secondary ions which provides the elemental composition. The rate of secondary ions can be monitored as a function of sputtering time, thus providing a depth profile of an elemental composition throughout the sample. A stylus profile is typically used to measure the sputtering depth[34].

In this work secondary ion mass spectrometry was performed using Hiden Analytical gas ion and quadrupole detector. An O^{2-} ion gun was used to sputter the sample using a beam energy of 5 keV at a current of 300 nA, and the depth profiles were then normalised.

4.4. Electrical characterisation of devices

In this section, the characterisation techniques used to analyse the CdTe solar cells produced in this work will be described. See Section 2.4 for the theory behind these techniques when used for photovoltaics applications.

4.4.1. Current density – Voltage (*JV*)

JV analysis is the standard technique used to test a solar cell's performance. It is used to extract the principal device parameters such as, η, FF, J_{SC} and V_{OC}. Device performance is measured by being placed under a simulated AM1.5 spectrum, and the current produced in measured as a function of applied bias. The device parameters are then extracted from the produced *JV* curve using Equation 2.9 in Section 2.4.1.1. From further analysis of the *JV* curves other parameters can be produced such as, R_S, R_{SH} and n (see Section 2.4.3.2).

In this work *JV* measurements were performed using a TS Space Systems solar simulator at room temperature under AM1.5 illumination with an intensity of 1000 W m^{-2}. The calibration of the solar simulator was carried out using a GaAs reference cell. The external voltage was swept from -1 to +1 V and the current measured using a Keithley 2400 source meter.

4.4.2. External Quantum Efficiency (EQE)

EQE is one the most widely used characterisation techniques when analysing CdTe photovoltaics for quantifying how efficiently light is being converted to electricity. In this work, EQE measurements were taken using a Bentham PVE300 EQE system which was calibrated using a Si photodiode. Cells were illuminated in the 300 – 950 nm spectral range by a monochromatic light using Xenon and halogen light sources using a diffraction grating. The photo generated current was amplified using a lock-in amplifier. See Section 2.4.4 for more details on the theory of EQE and how to analyse EQE device response.

4.4.3. Capacitance – Voltage (*CV*)

CV measurements were utilised to determine the built-in voltage (V_{bi}), acceptor density (N_A) and depletion width for CdTe solar cells, see Section 2.3 for more detail on the theory of *CV* and how to analyse *CV* response. *CV* measurements were performed in the dark using a Solartron SI 1260 impedance analyser using an interface SmartLab software applying a frequency of 100 kHz and external DC voltage sweep from -1V to +1V.

4.4.4. Electron beam induced current (EBIC)

EBIC is an SEM based semiconductor characterisation technique used for measuring the current that flows in a semiconductor when it is exposed to an electron beam. When the electron beam is incident onto the semiconductor's surface, an electron-hole pair is generated. If this generated pair diffuse to a region with a built-in electric field, such as a *p-n* junction in a solar cell, a current will be generated[28]. To analyse a *p-n* junction, different geometries EBIC can be utilised, such as cross section and plan view. In the plan view geometry, the incident directed normal to the junction. The EBIC signal produced can reveal any localised variations in performance and recombination centres. In cross sectional EBIC the electron beam is scanned parallel to the *p-n* interface and will reveal the position of the device junction[35,36].

In this work, EBIC was performed with samples in the cross-sectional geometry. The samples were transferred to a Hitachi SU70 SEM for imaging and for EBIC analysis via a Matelect ISM5 specimen current amplifier set to a 200 nA measurement range. The beam conditions used for the EBIC analysis were 8 keV with a beam current of 0.92 nA. Figure 4.12 shows a schematic representation of EBIC analysis performed on a devices cross section.

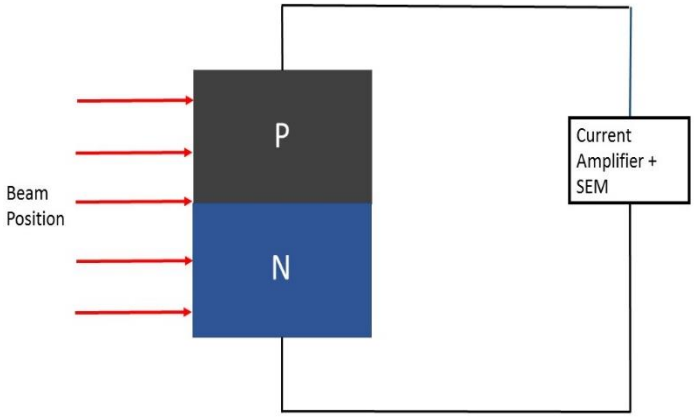

Figure 4.12: *A schematic representation of the sample preparation required for EBIC. a) Shows the FIB milling sample preparation and b) shows the EBIC measurement of the sample.*

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5. Selenium incorporation into CdTe layers and PV devices

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T. Baines, G. Zoppi, L. Bowen, T.P. Shalvey, S. Mariotti, K. Durose and J.D. Major, Incorporation of CdSe layers into CdTe thin film solar cells, Solar energy materials and solar cells, 180, 196 (2018). DOI: https://doi.org/10.1016/j.solmat.2018.03.010.

5.1. Introduction

The focus of this chapter is on routes to improving the J_{SC} in CdTe photovoltaics by modifying the window layer interface. This was initially investigated through the addition of oxygen to the CdS layer forming the wider bandgap CdS:O (Section 5.2.2). However, it was found that the use of CdS:O had fundamental limitations which reduced device J_{SC}. This led to the primary investigation of this chapter which was the addition of CdSe into the CdTe devices structure, as it has been shown that incorporation of Se into the CdTe devices and the removal of CdS improves device photo response at both short and long wavelengths[1,2].

The effect of incorporating CdSe layers into the CdS:O/CdTe device structure was investigated in Section 5.2.2. In Section 5.3 the addition of CdSe layers to the conventional CdS/CdTe photovoltaics was studied, with particular focus on the CdSe layer thickness, post CdTe growth treatment and formation of $CdS_{(1-X)}Se_X$ phase. Section 5.4 will focus on the removal of CdS from the device structure and using CdSe and SnO_2 as the device window layers. This section will again focus on the CdSe layer device thickness, post growth

annealing conditions and the addition of Cu to the device structure. In Section 5.5 alternative partner window layers for the $CdTe_{(1-x)}Se_x$ were investigated such as TiO_2, ZnO and fluorine doped tin oxide ($F:SnO_2$).

5.2. Use of CdS:O/CdSe as the window layer for CdTe photovoltaics

Due to parasitic absorption in the CdS layer of above bandgap (2.4 eV) energy photons, losses at short wavelength (< 550 nm) occur in CdS/CdTe devices, resulting in a significant reduction in performance (see Section 3.3.1). However, removal of CdS as the device window layer in order to improve short wavelength collection without compromising other device parameters such as open circuit voltage (V_{OC}) and fill factor (*FF*) is challenging[3]. The primary reason replacement of CdS layer is challenging is due to CdTe lattice mismatch with most materials. This, to an extent, includes CdS (10 %). However, the lattice mismatch can be reduced by the S-Te interdiffusion which somewhat eases the interfacial strain and improves performance. When wide bandgap oxides such as SnO_2 are used, they do not have the luxury of this decreased lattice mismatch and thus have reduced interface properties and performance due to high levels of interface recombination or unfavourable band alignments[3,4].

An alternative approach that has been developed by Wu *et al*[5]. is the use of nanostructured CdS grown in an oxygenated atmosphere (CdS:O), to controllably increase the bandgap from 2.5 eV to > 4 eV due to quantum confinement effects induced via oxygen incorporation. Integration of CdS:O into CdTe device structure has been reported to lead to an improvement in device J_{SC} and performance[6].

Recent work has demonstrated that incorporation of CdSe into the CdTe device structure leads to the formation of $CdTe_{(1-X)}Se_X$ phases which have a lower bandgap than CdTe[2]. The reduction of the bandgap leads to an enhanced EQE response at long wavelength. However, in order to retain a high V_{OC}, it is often still the case that a thin CdS layer is required[2,7]. Whilst the cells still show a high V_{OC}, the *FF* is significantly reduced for

cells with a thin CdS layer due to formation of unfavourable CdTe/TCO interface regions due to voids in the thin CdS layer[2,8].

This section will compare the device performance i) when an oxygenated CdS layer with varying oxygen content is incorporated into a CdS/CdTe device structure (Section 5.2.2) and ii) when varied thicknesses of CdSe is added to the CdS:O/CdTe device structure (Section 5.2.3). The intention was to investigate whether, by using a CdS:O layer the device response at short wavelength could be enhanced and the favourable CdS/CdTe interface qualities could be retained. Prior to combining that with the addition of a CdSe layer to improve the device response at long wavelength due to reduced bandgap of the $CdTe_{(1-x)}Se_x$ phase. Use of CdS:O should allow for a thicker window layer to be used than compared top CdS without compromising device J_{SC} and *FF* and retaining device voltage [5]. It was hoped that by combining the effects of both the CdS:O and CdSe the device performance would be enhanced, primarily though enhanced J_{SC}.

5.2.1. Device fabrication

Figure 5.1 shows a schematic representation of the CdTe device structure used in this section. General device fabrication procedures can be found in the relevant experimental sections (See Chapter 4). Unique device conditions used in this section are as follows:

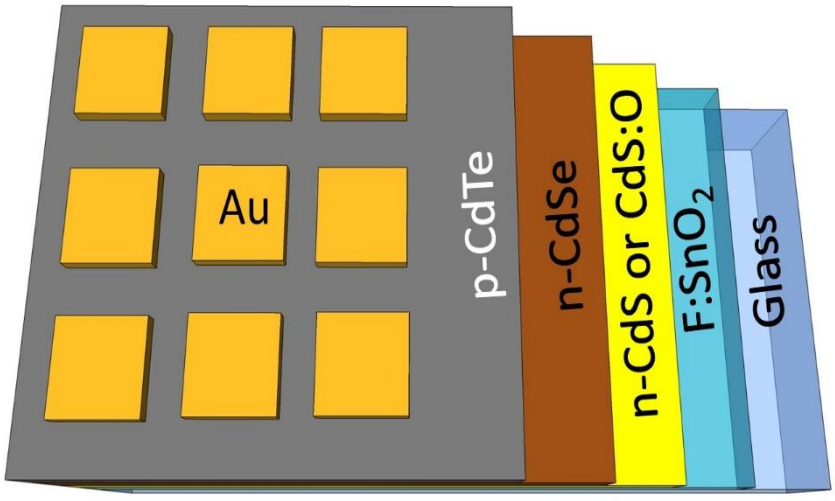

Figure 5.1: *Schematic representation of the as-deposited CdS:O/CdSe/CdTe device structure used in Section 5.2.*

120 nm of either CdS or CdS:O with varying oxygen concentration in the sputter ambient as specified in the text, was deposited at room temperature, using a power density of 1.32 W cm^{-2}. CdS:O layers with a 0%, 3%, 5% and 10% were fabricated by varying oxygen content, the oxygen content was controlled via the argon/oxygen flow rates in the sputtering chamber. CdSe layers were also deposited at room temperature using a power density of 1.32 W cm^{-2}. All samples were then $MgCl_2$ treated at 430°C for 20 minutes in an air ambient unless otherwise stated [9].

5.2.2. Effect of oxygen content in CdS:O layer

Initially the influence of the oxygen content on the CdS:O layers was investigated. A series of CdS:O layers with a varied oxygen content were deposited by adjusting the Ar/O_2 ambient in the chamber from 0% to a 10 % oxygen content. Figure 5.2 shows how the optical transmission of CdS changes as a function of oxygen content and the extrapolated bandgaps calculated from the Tauc method when deposited on soda lime glass (SLG). This shows that by increasing the oxygen content in the sputtering chamber the bandgap of CdS can be increased from 2.5 eV for no oxygen content (i.e. CdS layer) to beyond the transmission cut-off for SLG (≈ 4 eV) for a 10% ambient, the cut-off observed is due to the glass rather than the 10% CdS:O film. In addition to this, depending on the oxygen content, the bandgap of CdS:O can also be somewhat controlled. It has previously been shown by Wu *et al*[6]. that the bandgap shift in CdS due to oxygen content is due to quantum confinement effects. Quantum confinement effects relate to changes in the atomic structure as a result of an ultra-small length scale on the energy band structure. Quantum confinement effects will only occur if the electronic wave function in comparable to the particle size. When the particles size approaches Bohr exciton radius, quantum confinement effects result in an increase to the excitonic transition energy and blue shift in the absorption occurs and a widening of the materials' optical bandgap[10]. The oxygen causes a significant reduction in the grain size of CdS and causes the bandgap to increase

to beyond that of glass. The bandgap shift observed in CdS confirms successful formation of the CdS:O phase and these layers were then taken forward to replace conventional CdS as the window layer in CdTe devices.

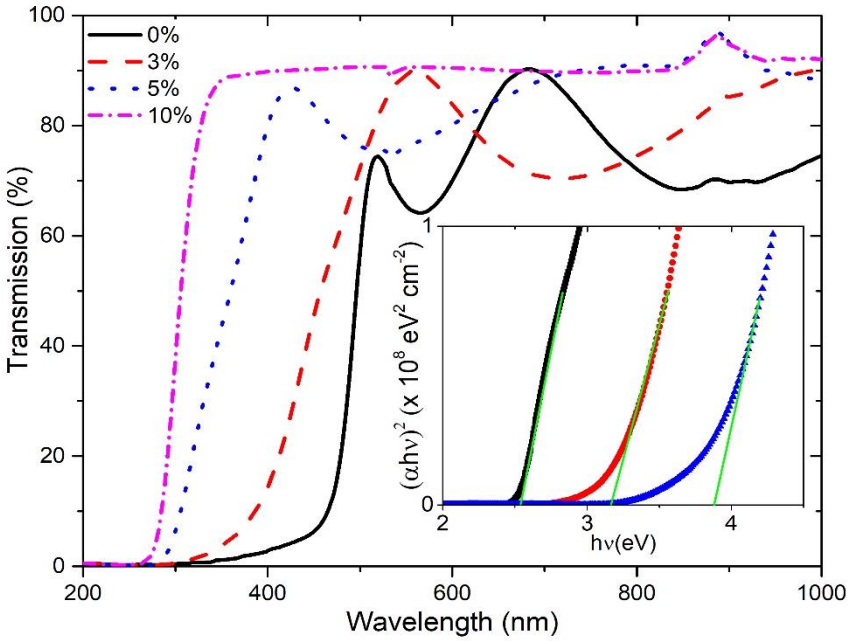

Figure 5.2: *Transmission data as a function of oxygen content in the 120 nm CdS layers grown on Soda lime glass (SLG). Insert, Tauc plots showing how CdS bandgap shifts with oxygen content.*

A series of cells were prepared with varying amounts of oxygen in the sputtering chamber during the CdS:O deposition, ranging from 0% to 7%, as it was found that 7% was beyond the limit to which oxygen could be effectively incorporated and the 10% CdS:O layers were more unstable, as they would visibly degrade back to the yellow CdS layer, CdS:O/CdTe devices with a 10% oxygen content were not fabricated.

To determine the influence of the CdS:O layer on device performance, all other cell deposition and processing conditions were kept identical, which are described in the relevant experimental Chapter 4. Figure 5.3a-d shows the average device performance parameters, the minimum and maximum values are also shown. The accompanying champion *JV* and EQE curves are shown in Figures 5.4a and b respectively.

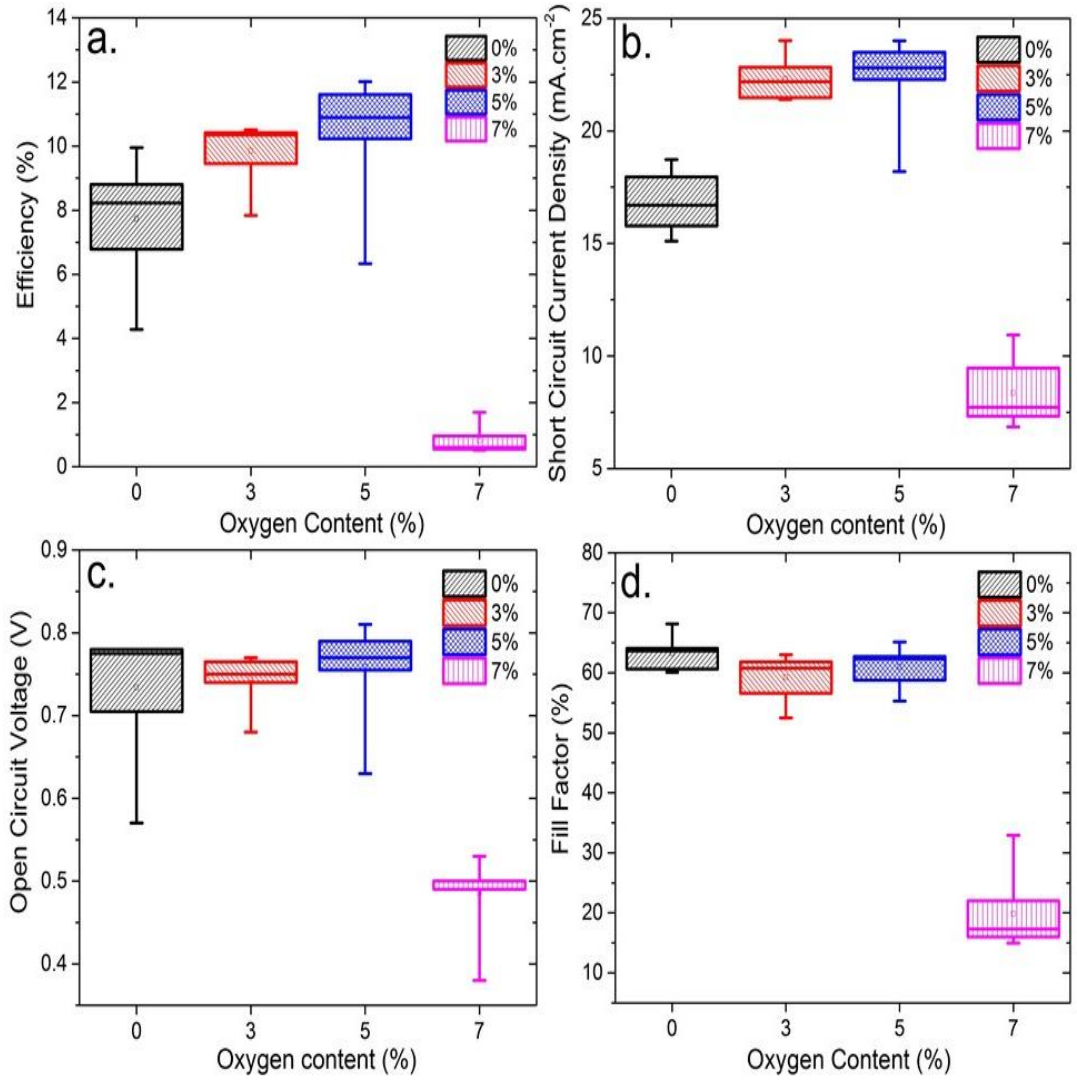

Figure 5.3: *CdS/CdTe device performance parameters, a) efficiency (η), b) short circuit density (J_{SC}), c) open circuit voltage (V_{OC}) and d) fill factor (FF), as a function of oxygen content in the CdS sputtering ambient. The box plots show the median, min, max and the 25%-75% percentiles. Number of samples (N) =8.*

Figure 5.3b shows that incorporating only a small amount of oxygen into the CdS film, and the resultant bandgap shift can have a dramatic impact on the J_{SC}. CdS:O with a 3% oxygen content improved the average J_{SC} from 16.84 mA cm^{-2} to 22.48 mA cm^{-2} which resulted in an average performance increase of over 2%. From the EQE data shown in Figure 5.4b, the increase in J_{SC} is due to an enhanced photo response at short wavelength resulting from the increased CdS bandgap as it converts to the CdS:O structure. However, there still seem to be losses which would be associated with CdS in the short wavelength (< 500 nm) region of the spectrum, possibly due to transformation of the CdS:O layer back

to CdS at the CdS/CdTe interface[6,11], meaning parasitic absorption in this CdS layer starts to occur.

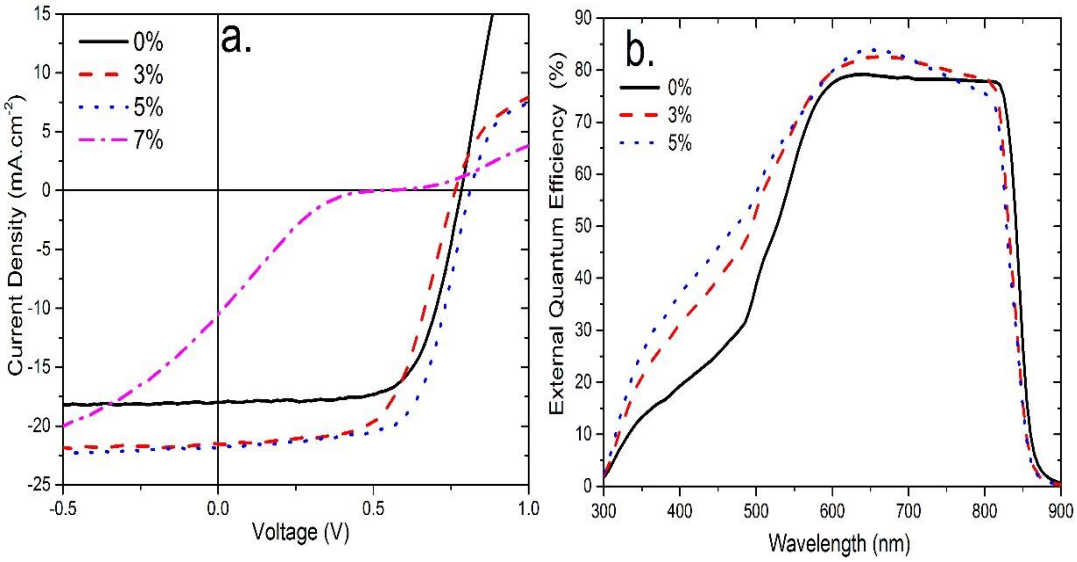

Figure 5.4: *a) Current – voltage (JV) and b) external quantum efficiency (EQE) responses for highest efficiency CdS:O/CdTe devices as a function of oxygen content in the CdS sputtering ambient.*

Whilst the J_{SC} is not significantly improved by increasing the oxygen content to 5% the V_{OC} was improved reaching a peak value of 0.81 V and the series resistance (R_S) was also reduced when compared to the 3% CdS:O film, shown in Figure 5.5. This indicates that CdS:O with a 5% oxygen content may have better interfacial properties with CdTe, possibly due to a better band alignment between the CdTe and CdS:O layers when compared to the CdTe and CdS layers. The increase to the device photo voltage led to improved cell efficiency with peak value increasing to 12.01% when a 5% oxygen content was utilised. It should be noted however, that the *JV* curves produced for the 3% and 5% CdS:O devices show an enhanced roll-over effect or the onset of the formation of an S-shaped *JV* response. This is possibly due to a growing extraction barrier now forming at the device interfaces due to the increased CdS bandgap, which has enhanced the device resistive losses when compared to CdS based devices as shown for the 7% CdS:O based devices (Figure 5.5)[12].

Adding a higher, 7% oxygen content into the film leads to a dramatic loss in performance with average efficiency decreasing to 0.72%, with all parameters being affected. The *JV* curves produced for devices with 7% CdS:O exhibit an uncharacteristic S – shape, suggesting a large extraction barrier has formed at the CdS:O/CdTe interface which is limiting the extraction of generated carriers [13,14]. Whilst the S - shaped curve is a relatively uncharacteristic feature in CdTe PV, this effect has been seen extensively in other PV fields such as in organic PV, where a wide range of interface band alignments are typically investigated. S-shaped *JV* curves originate from a misalignment of the devices band structure therefore, it is not surprising that this is a relatively unseen phenomenon in CdTe, as the CdS/CdTe device structure has been used almost exclusively for the last 20 years. As the field moves away from this structure, we can expect S-shaped curves to become a more prominent feature of CdTe PV literature. The S – shaped curves produced by CdS:O based devices could either be due to the formation of CdO phases owing to the high oxygen concentration, degradation of the 7% CdS:O layer or the potential creation of a spike in the conduction band due to its increased bandgap[12,13].

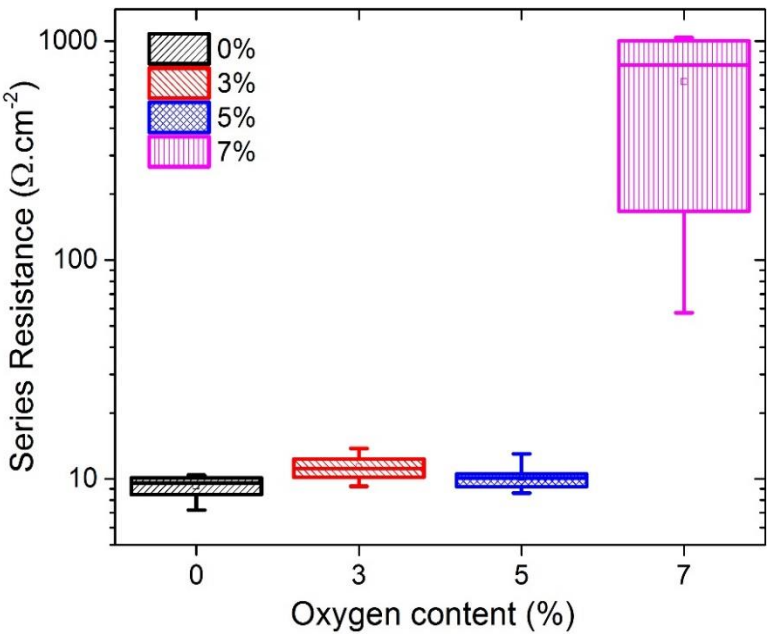

Figure 5.5: *Effect of increasing oxygen content in the CdS sputtering ambient on CdS:O/CdTe device series resistance (R_S). R_s values where calculated from the JV curves forward bias response. N=8.*

The device EQE spectrum is not shown for 7% CdS:O devices as they exhibited a very low response and was mainly electronic noise particularly when the measurement switched between the halogen and xenon lamps (700 nm). This is again suggestive that the limit of oxygen incorporation has been reached. Device *FF* (Figure 5.3d) remained relatively unaffected when 3% and 5% CdS:O layers were incorporated. However, it dropped significantly (< 30 %) for 7% CdS:O/CdTe devices, primarily due to substantial increase to device R_S (Figure 5.5).

This data confirms that, by increasing the bandgap of the window layer, the current produced by the device can be improved without having a detrimental effect on other device parameters, as V_{OC} and *FF* values were largely retained. However, this data would also seem to suggest that while the use of CdS:O can improve the devices photo response at short wavelength (< 500 nm) the response still seems fundamentally limited by recrystallisation of the CdS and thus will limit cell J_{SC}. Therefore, achieving an optimal device photo response across all wavelengths will require finding an alternative to CdS or CdS derivatives.

5.2.3. Addition of CdSe layers into CdS:O/CdTe devices

5.2.3.1. Effect of CdSe layer thickness in CdS:O/CdTe devices

Following initial optimisation, CdS:O with a 5% oxygen deposition ambient was identified as the most suited to device fabrication. A series of cells with a 5% CdS:O layer were then fabricated with the addition of varying thickness of CdSe ranging from 0 nm to 100 nm deposited between the CdS:O and CdTe layers. Figure 5.6a-d shows the influence of varying the CdSe layer thickness on the average and peak device performance. Figure 5.7a and b show the *JV* curves and EQE spectra for the champion devices for each CdSe thickness.

From these results incorporation of CdSe into the device structure has had a detrimental effect on device performance regardless of thickness. Device J_{SC} is particularly

affected, falling from 22.42 mA cm^{-2} for the cells with no CdSe to < 16 mA cm^{-2} for CdSe thicknesses > 40 nm. This can be explained by analysing the EQE spectra produced (Figure 5.7b), where the overall EQE response, particularly the short wavelength response at < 650 nm, is significantly reduced with increasing CdSe thickness.

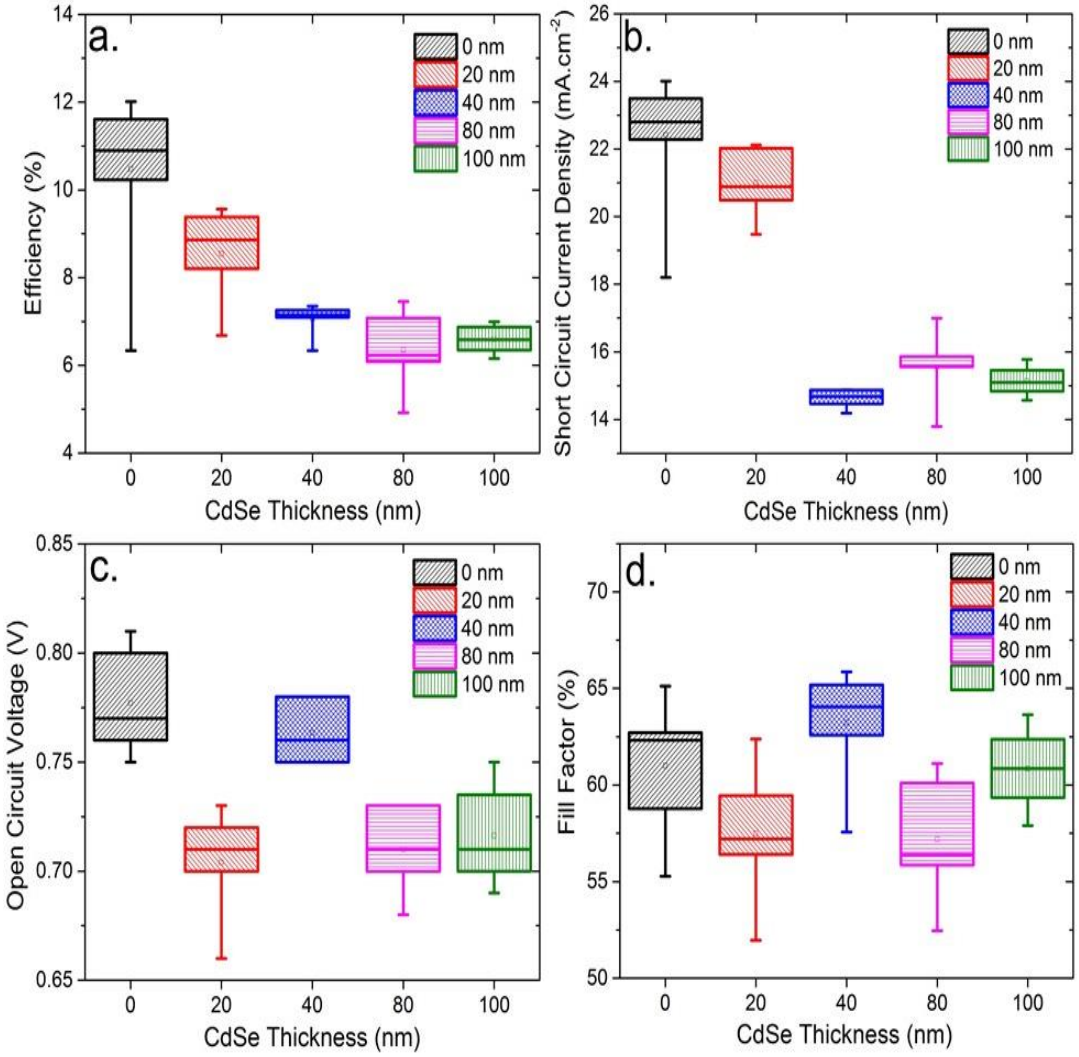

Figure 5.6: *CdS:O/CdSe/CdTe device performance parameters, a) η, b) J_{SC}, c) V_{OC} and d) FF where the CdSe thickness has been varied from 0 to 100 nm.N=9.*

This would appear to be evidence of a remaining CdSe layer which has not been intermixed with the CdTe during either the CSS deposition or the $MgCl_2$ treatment, due to CdTe one sided depletion region, any residual CdSe left in the device stack would result in enhanced parasitic absorption. Device series resistance (see Figure 5.8) also increases with increasing CdSe thickness, this would also appear to suggest that a CdSe layer is still present

post CdTe deposition and is contributing to the enhanced resistive losses. Ideally, the CdSe layer should be completely absorbed by the CdTe converting from the non-photoactive wurzite phase to the photoactive $CdTe_{(1-X)}Se_X$ zincblende structure which has a lower bandgap than CdTe due to the band bowing effect and thus enhance device photocurrent[8,15].

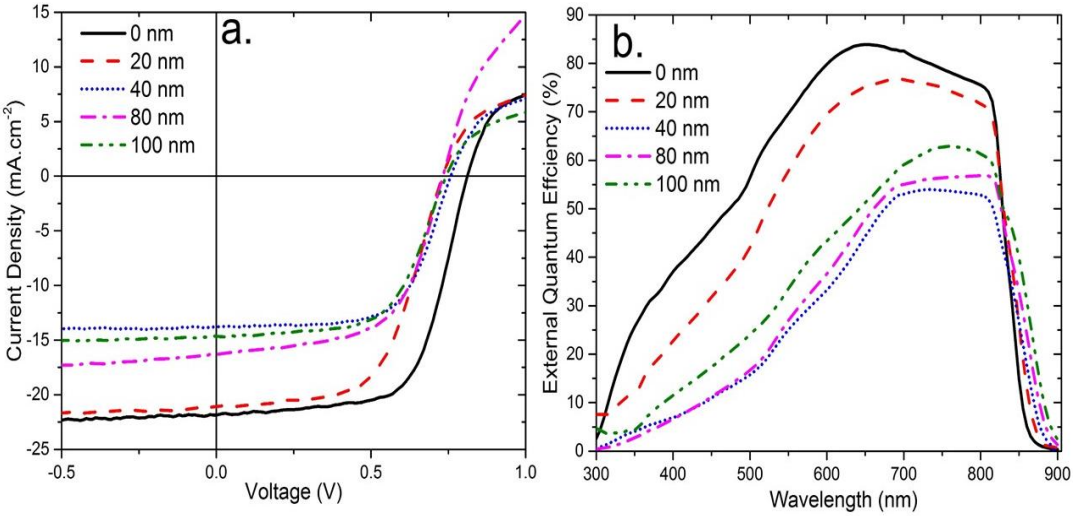

Figure 5.7: *a) JV and b) EQE responses for the highest efficiency CdS:O/CdSe/CdTe devices where the CdSe thickness has been varied from 0 to 100 nm.*

The EQE data does show enhanced absorption at long wavelength regions (> 850 nm), indicating a $CdTe_{(1-X)}Se_X$ intermixed region has indeed been formed. The decrease in bandgap follows a trend with increasing CdSe thickness. 100 nm of CdSe demonstrates the most absorption at long wavelengths and therefore has the lowest bandgap (1.39 eV) by estimation from the EQE absorption cut-off. From the EQE curves, it is clear that CdSe thicknesses > 40 nm lead to a significant enhancement to parasitic absorption with increased losses at 700 nm. This is distinctly different from losses observed for CdS (520 nm). This suggests that a residual CdSe layer is still present in the device structure and contributing to the enhanced parasitic absorption observed.

In addition to this, although there is no definitive thickness related trend the inclusion of CdSe into the device structure has a detrimental effect on the V_{OC} of the device with it being reduced for all CdSe thicknesses. This could be due to a number of factors, such as

poorer interface quality, a shift in the band alignment or introduction of defect states, all of which would limit V_{OC}. From these initial results it was apparent that some modification to the typical CdS/CdTe solar cell fabrication process would be required for devices which incorporated CdSe layers.

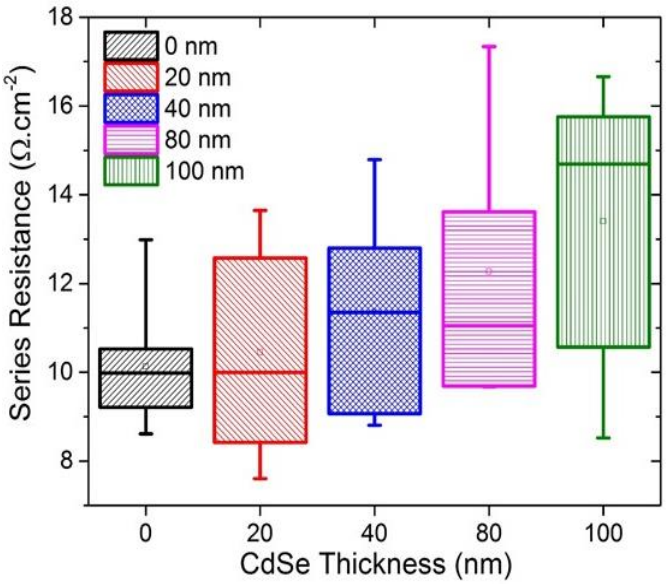

Figure 5.8: *CdS:O/CdSe/CdTe device series resistance (R_S) as a function of CdSe thickness. N=9.*

5.2.3.2. Influence of chlorine treatment time

It has often been suggested that the chlorine treatment step has a large influence on interdiffusion of CdS and CdTe layers[16–18]. This however, seems to be less pronounced for high temperature deposition techniques such as CSS[16]. In order to investigate whether CdSe intermixing could be similarly controlled via the chlorine treatment, the $MgCl_2$ activation step was varied from 20 mins to 120 mins for cells containing 100 nm CdSe layer. The idea being the additional treatment time would allow the CdSe to convert from the non-photoactive wurzite phase to the photoactive $CdTe_{(1-X)}Se_X$ zincblende structure [1], with the aim of improving the collection loss observed in Section 5.2.3.1.

Figure 5.9a-d shows how the device parameters change with increased chlorine treatment time using a CdS:O/CdSe/CdTe device structure with a 100 nm thick CdSe layer, 100 nm layers were chosen because it been demonstrated in previous work that it results

in the most efficient devices. Figure 5.10a and b show the *JV* curves and EQE spectra produced for the highest efficiency contacts. These results show that cells produced with a CdSe layer have a relatively high level of robustness to the chlorine step with similar peak performance being achieved after a 60 min treatment time. By comparison devices, with a CdS/CdTe structure show a significantly reduced performance with equivalent annealing time typically due to degradation of the CdS/CdTe layer.

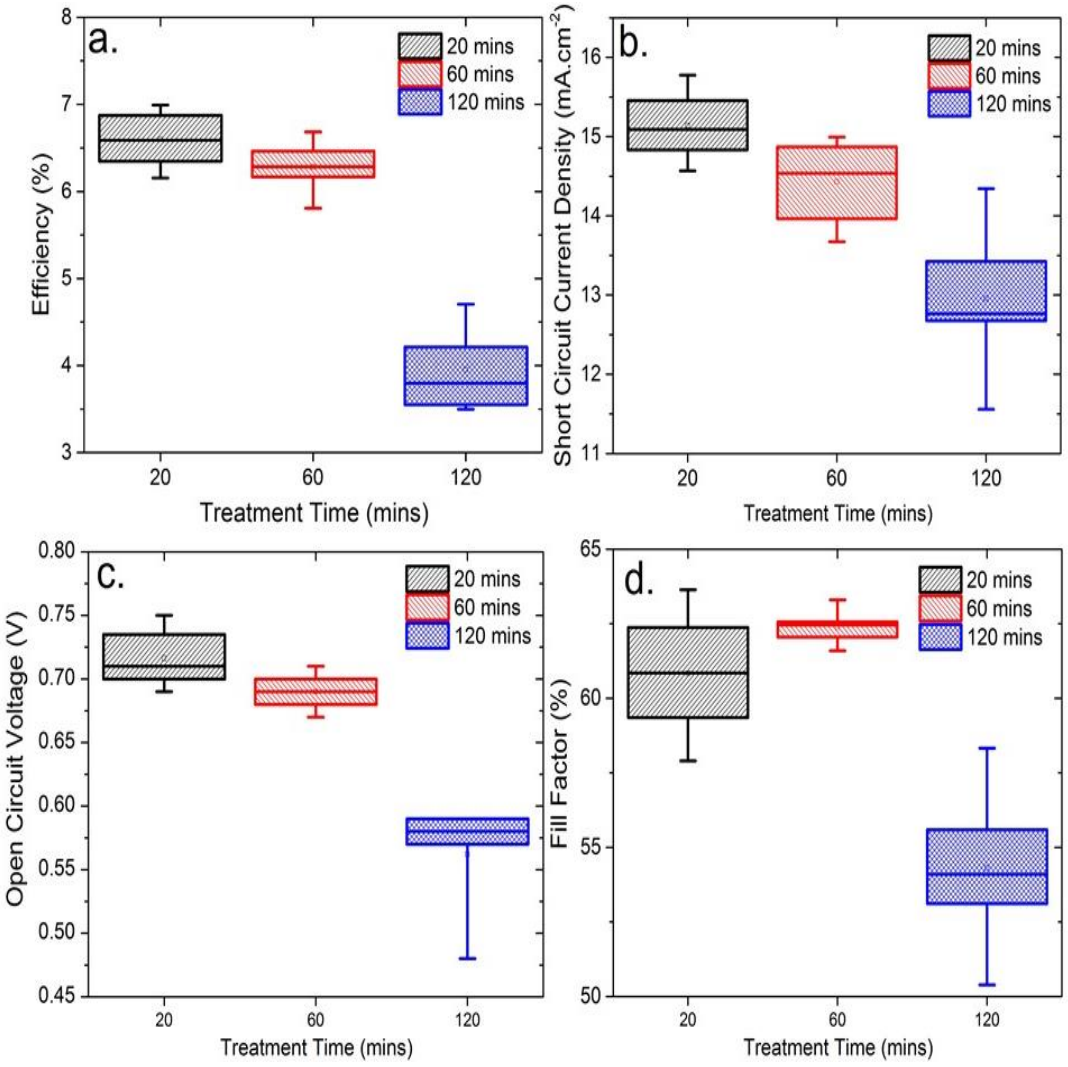

Figure 5.9: *CdS:O/CdSe (100 nm)/CdTe device performance parameters, a) η, b) J_{SC}, c) V_{OC} and d) FF as a function of chlorine treatment time. N=8.*

It is only after a long treatment time of 120 mins that the performance starts to deteriorate noticeably with losses in both the V_{OC} and R_{SH} (1220.18±88.90 Ω cm^{-2} and 671.65±90.08 Ω cm^{-2} for the 20 mins and 120 mins devices), indicating the cells have

become over treated and shunting pathways have been created in the CdS:O/CdSe. The J_{SC} however, has largely been retained even though the cells have been over treated, peak J_{SC} drops from 15.26 mA cm^{-2} to 14.34 mA cm^{-2}. The *JV* and EQE data presented in Figure 5.9b indicate little change in either Se diffusion or junction position as no enhancement to the devices short wavelength response was observed. Cells produced for treatment times of 20 mins and 60 mins show near identical EQE curves and the cells treated for 120 mins show similar cut-offs at short and long wavelengths, with enhanced losses in the long wavelength region (550-800nm).

The lack of change to the shape of the EQE curve would seem to suggest that the increased chlorine treatment time has not substantially increased the amount of Se diffusion into the CdTe and that the non-photoactive CdSe is still present. The lack of Se diffusion during the chloride treatment could be because CdTe deposited via CSS is large grained and typically does not recrystallize during the chlorine step, which in turn could limit the amount of Se diffusion. This effect has been observed for S diffusion in CSS grown CdTe PV, where very limited S diffusion occurred during the chlorine step. Instead the diffusion is primarily determined by the CdTe growth conditions[16]. Therefore, further optimisation of the CdTe deposition is likely to be required in order to control the Se diffusion as it is unable to be remedied by the post growth treatment.

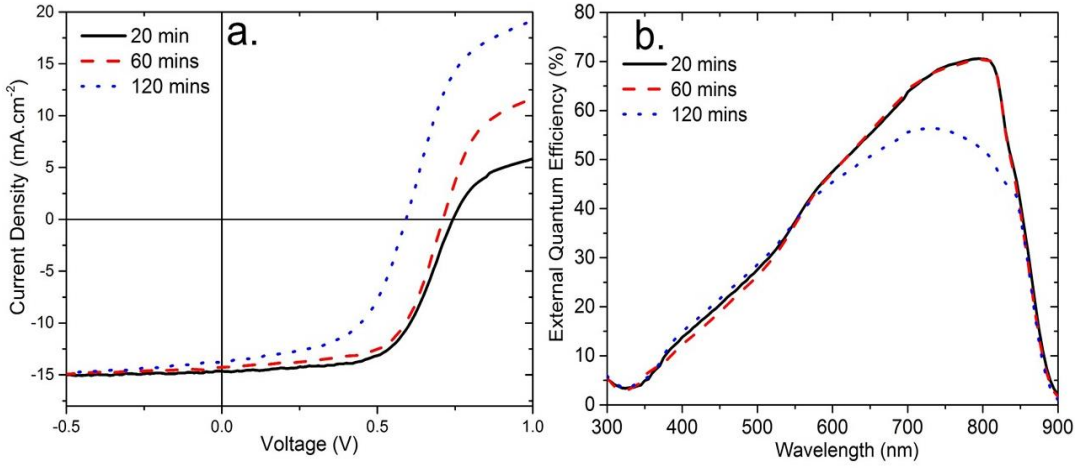

Figure 5.10: *a) JV and b) EQE responses for the highest efficiency CdS:O/CdSe (100 nm)/CdTe devices as a function of chlorine treatment time.*

An alternative explanation though is that the Se could also have diffused into the CdS layer during high temperature CdTe deposition, leading to the formation of $CdS_{(1-X)}Se_X$ phases. Such phases would be of a lower bandgap than CdS:O and cause enhanced losses at short wavelengths and would not be removed via additional chlorine treatment. The formation of $CdS_{(1-X)}Se_X$ phases will be explored in greater detail in Section 5.3.

5.2.4. Discussion

In this section, it has been demonstrated that integrating oxygen into CdS films increases the optical bandgap of CdS, thus leading to an increase in device J_{SC} and performance. However, adding too much oxygen into the CdS films will eventually result in a significant reduction to device performance and the formation of an uncharacteristic S–shaped *JV* curve due to the production of an energy barrier at the interface. It was found that there are limits to the device improvements that could ultimately be achieved due to partial transformation of CdS:O to a standard CdS layer.

The additional incorporation of CdSe into the devices to generate bandgap grading proved challenging, with even a thin layer of CdSe having a detrimental effect on device performance, in particular on device J_{SC}. The EQE data presented suggests either that a CdSe layer is still present or else a $CdS_{(1-X)}Se_X$ phase was formed in the device structure and contributed to losses to device response at wavelengths < 700 nm, ultimately leading to a reduction to device photocurrent, voltage and performance.

Altering device processing to account for CdSe incorporation was investigated by increasing the chlorine treatment step from 20 mins to 120 mins to examine its influence on Se diffusion. The EQE data presented suggested little effect on diffusion of the Se into the CdTe layer and as a result increasing the chlorine step also had very little influence on device J_{SC}. In addition to this, the overall device performance was reduced due to enhanced resistive losses as a result of over treatment of the devices.

It was determined that further investigations of the CdTe growth was required in order to understand how the Se diffusion could be controlled and whether the unwanted formation of $CdS_{(1-X)}Se_X$ could be avoided. Section 5.3 will explore the Se diffusion into the CdS layer in more detail and report on attempts to optimise the CdTe deposition process.

5.3. CdSe incorporation into CdS/CdTe devices

This section investigates i) the limitations of the CdS/CdSe/CdTe device structure with particular focus on the unwanted $CdS_{(1-X)}Se_X$ phase (Section 5.3.2.1 and 5.3.2.2) and ii) how the Se distribution can be controlled via device processing (Section 5.3.2.3). CdS was used in this section rather than CdS:O because it is a more stable, reliable and well-known material, allowing the role of Se incorporation to be more relatively studied.

5.3.1. Device fabrication

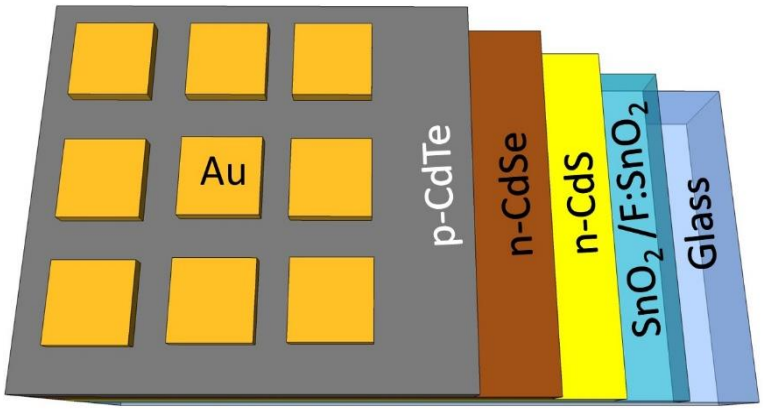

Figure 5.11: *Shows a schematic representation of the as-deposited CdS/CdSe/CdTe device structure used in Section 5.3*

Figure 5.11 shows a schematic representation of the CdTe device structure used in this section. General device fabrication procedures can be found in the relevant experimental sections (See Chapter 4). Unique device conditions used in this section are as follows

Undoped SnO_2 layers (100 nm) were deposited by chemical vapour deposition (CVD) at 600°C by NSG[Ltd]. 100 nm CdS was deposited via sputtering at room temperature, using a power density of 1.32 W cm^{-2}. Varying thicknesses of CdSe were deposited at room

temperature using a power density of 1.32 W cm^{-2}. All samples were then treated with $MgCl_2$ at 430 °C for 20 mins in an air ambient unless stated otherwise.

5.3.2. Limitations of CdS/CdSe/CdTe device structure

5.3.2.1. CdS/CdSe/CdTe device performance

Initially the impact of incorporating a CdSe layer into the conventional SnO_2/CdS/CdTe device structure (i.e. between the CdS and CdTe) was investigated, with SnO_2 acting as the traditional HRT or 'buffer' layer[19], SnO_2 was chosen as it has a wide bandgap and can be reproduced by NSG^{Ltd} easily. The HRT was used in this case because it allowed for a direct comparison to be made if the CdS layer was removed from the device structure. Initially both CdS and CdTe deposition conditions were kept the same as for our standard CdSe-free cell structure (see Section 5.2). This was done to determine the influence of Se incorporation in comparison to a baseline device. Figure 5.12a-d gives peak and average performance parameters extracted from the *JV* data for cells with either a 0 nm, 50 nm or 100 nm thick CdSe layer. The *JV* and EQE curves for the highest efficiency contacts are shown in Figure 5.13a and b respectively.

From this data it is again clear that including the CdSe layer has a detrimental effect on performance, particularly by reducing J_{SC} from 18.7 mA cm^{-2} to 15.6 mA cm^{-2} and *FF* from 61.5% to 55.1% (for 100 nm of CdSe). The progressive reduction in *FF* is caused by an increase in R_S from 7.1 Ω cm^{-2} to 8.6 Ω cm^{-2} and 12.6 Ω cm^{-2} with the inclusion of 0 nm, 50 nm and 100 nm CdSe layers respectively. R_{SH} values are unaffected by the CdSe incorporation. EQE curves again show the origin of the J_{SC} losses: for devices that have 100 nm CdSe layers, absorption was increased at long wavelengths, indicating the formation of a $CdTe_{(1-X)}Se_X$ phase with a bandgap of ≈ 1.38 eV. However, there were significant losses at short wavelengths, with the absorption cut-off starting to occur at ≈ 700 nm compared to ≈ 550 nm for a devices with CdS only. Inclusion of CdSe has increased the wavelength range over which harmful parasitic absorption takes place. This is the result one would expect in

the absence of significant interdiffusion as the bandgap of CdSe is 1.7 eV, which is lower than CdS, and would therefore, increase the range over which parasitic absorption would occur. However, in the ideal case, the CdSe should completely convert to the photoactive $CdTe_{(1-x)}Se_x$ zincblende phase, lowering CdTe bandgap and inducing bandgap grading to increase carrier lifetime[20].

There are therefore two possible explanations for the observed losses either, a) the CdSe layer is still present post CSS deposition and chlorine treatments, or b) in addition to intermixing with the CdTe, the CdSe also intermixes with the CdS layer forming a $CdS_{(1-x)}Se_x$ phase. A mixed S-Se phase would be of a lower bandgap than CdS (ranging from 2.4 eV to 1.7 eV depending on the Se content) and any absorption in this layer would be parasitic[21,22].

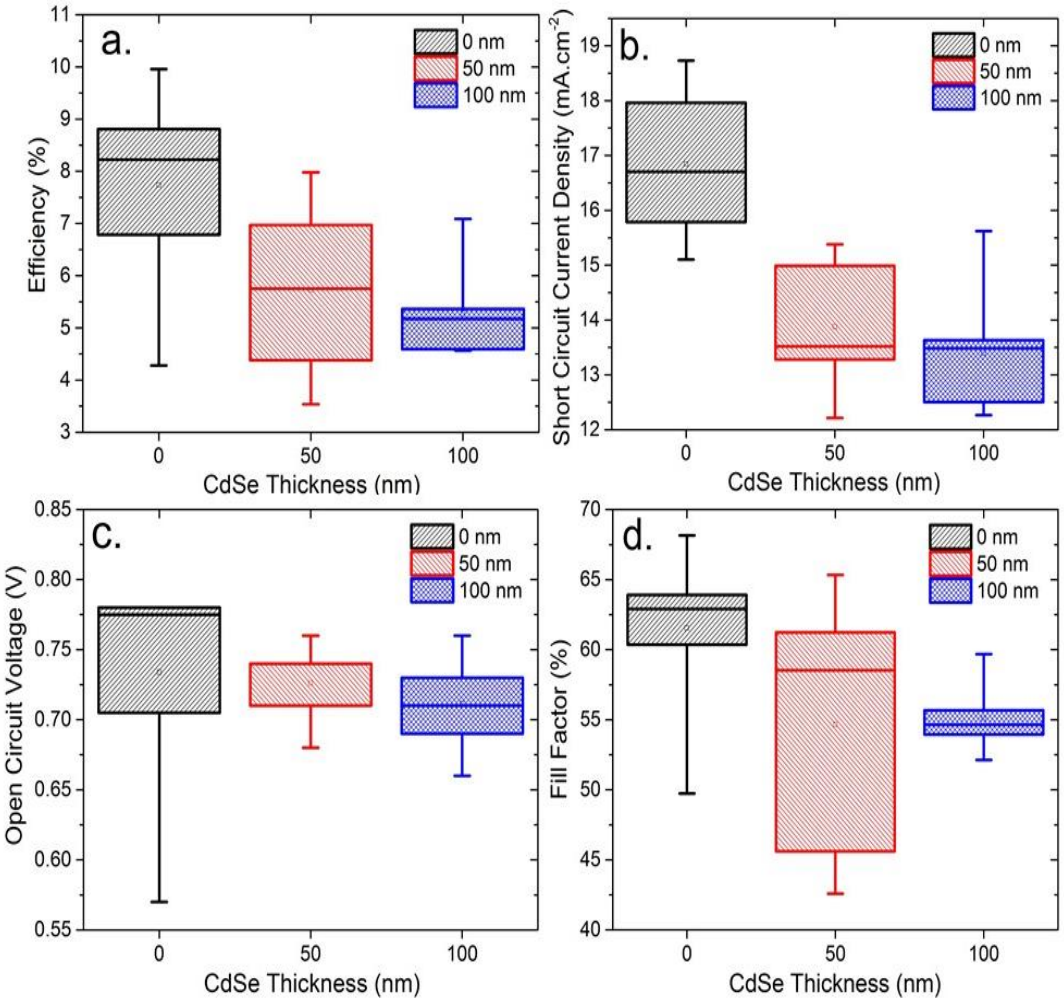

Figure 5.12: *SnO_2/CdS/CdSe/CdTe device performance parameters, a) η, b) J_{SC}, c) V_{OC} and d) FF where the thickness of the CdSe layer is varied from 0 to 100 nm. N=9.*

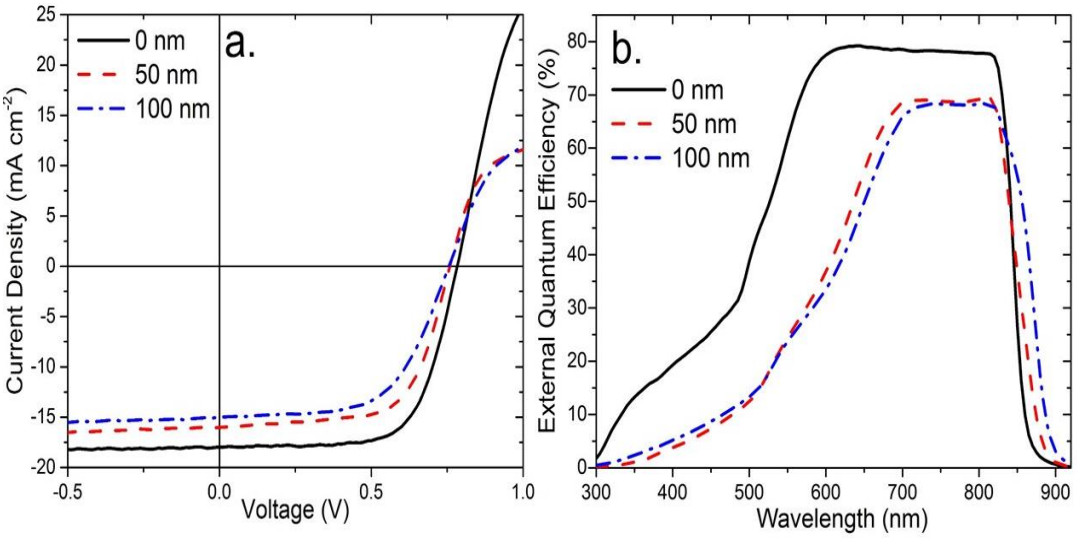

Figure 5.13: *a) JV and b) EQE responses for the highest efficiency SnO_2/CdS/CdSe/CdTe devices where the thickness of the CdSe layer is varied from 0 to 100 nm.*

It is notable that for a 50 nm layer of CdSe, the EQE data shows a very similar short wavelength cut-off to that of the 100 nm layer, but a lesser bandgap shift at long wavelengths (≈ 1.41 eV). The inference here is that for the 50 nm layer there appears to be a lower Se content in the $CdTe_{(1-X)}Se_X$ layer, but there is the same level of parasitic absorption to the 100 nm layer (i.e. reduced EQE in the 550-700 nm region). If the observed losses were due to a residual CdSe layer, it is anticipated that parasitic absorption would be more pronounced for the 100 nm layer, hence this suggests the issue is the formation of a $CdS_{(1-X)}Se_X$ phase. Paudel *et al*.[2] reported no such J_{SC} losses when CdS and CdSe were incorporated into their CdTe device structure, possibly due to the differences in deposition conditions with the conditions utilised here favouring intermixing between the CdS and CdSe. Previous work has shown that the majority of the intermixing occurs during our CdTe deposition[16]. This is consistent with the results presented in Section 5.2.3.1 for CdS:O based devices.

5.3.2.2. Structural analysis of CdS/CdSe/CdTe devices

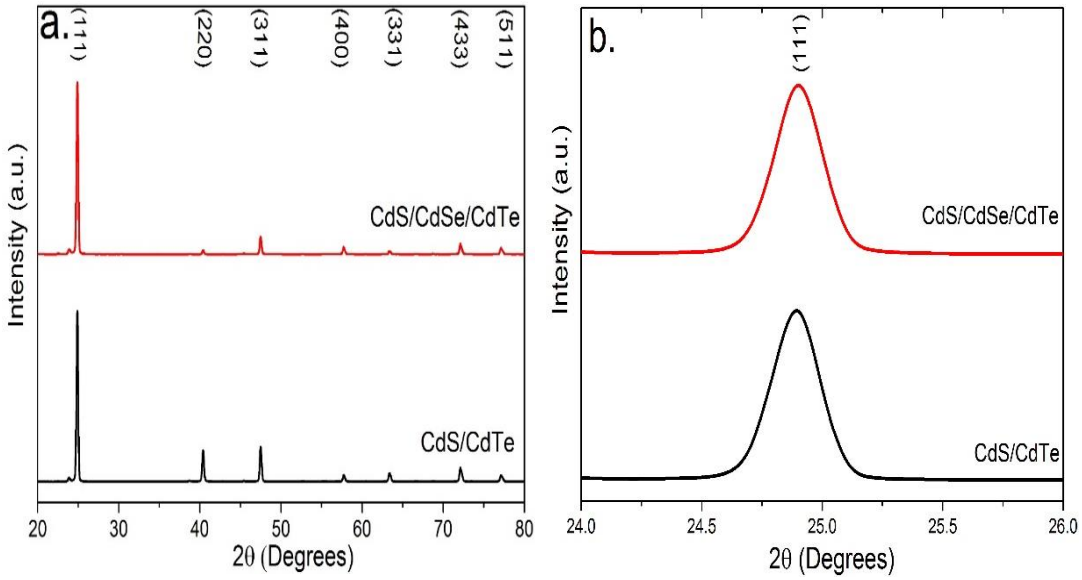

Figure 5.14: *a) X-ray diffraction (XRD) patterns of CdTe grown via CSS deposited on CdS/CdSe (100 nm) and CdS. b) Zoomed in image if the (111) CdTe diffraction peak.*

Table 5.1: *Calculated texture coefficients and standard deviation for CdTe grown on CdS and CdS/CdSe (100 nm) layers.*

Device structure	C_{111}	C_{220}	C_{311}	C_{400}	C_{331}	C_{422}	C_{511}	σ
CdS/CdTe	4.60	0.82	0.87	0.162	0.193	0.357	0.153	1.48
CdS/CdSe/CdTe	5.98	0.08	0.37	0.10	0.07	0.30	0.12	2.03

In order to assess the Se distribution in the sample we needed to first determine whether the CdTe layer had completely converted to the $CdTe_{(1-X)}Se_X$ phase, as in the ideal case the back surface should be entirely CdTe and a single $CdTe_{(1-X)}Se_X$ should not be forming. This was done by performing X-ray diffraction (XRD) measurements of the CdTe back surface when deposited on either CdS/CdSe or CdS, shown in Figure 5.14. Swanson *et al.*[21] demonstrated a shift to higher angles in the XRD pattern for $CdTe_{(1-X)}Se_X$ films compared to CdTe. From Figure 5.14b, it is clear that no such shift is observed as there is very little difference between the CdTe films with both exhibiting a highly (111) orientated zincblende CdTe film[23,24]. However, the CdTe films grown on CdS/CdSe do show a higher

degree of (111) orientation when compared to CdTe films grown on CdS. Table 5.1 shows the calculated texture coefficients and overall spread for the data presented in Figure 5.14a[25,26].

The XRD data would indicate that at the very least, Se is not diffusing though the entirety of the CdTe film, forming a continuous $CdTe_{(1-X)}Se_X$ phase. From the XRD it would also appear that Se is doing little to the CdTe layer however, when paired with EQE data previously shown it is clear that some Se is diffusing in to the CdTe. The thick CdTe layer (5 – 6 µm) and position of the CdSe interface being away from the back surface means the measurement is unable to probe the Se content at the near interface. Therefore, given the geometry of the measurement, analysing the interface is difficult and samples designed specifically to measure the interface properties may not be representative of the actual device interface produced during cell processing.

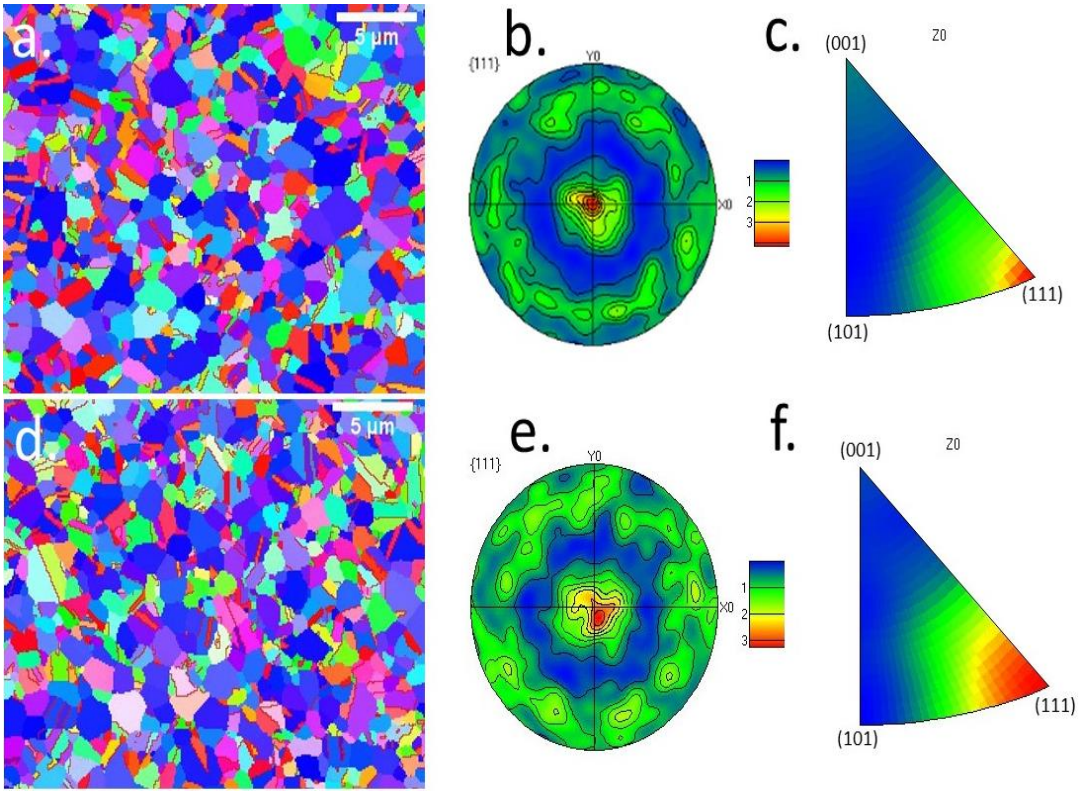

Figure 5.15: *Planar electron back scattered diffraction (EBSD) inverse pole figure map, (111) pole figure and inverse pole figure for CSS grown CdTe on CdS (a,b,c) and CdS/CdSe (100 nm) (d,e,f). The colours represent different grain orientations and the misorientation between adjacent grains, with blue representing 111 orientated grains.*

The film structure was investigated on a grain to grain level via the use of EBSD. Figure 5.15a-f shows the planar EBSD inverse pole figure maps, (111) pole and inverse pole figures for the back surface of CSS grown CdTe on CdS and CdS/CdSe, respectively. The colours represent different grain orientation and the misorientation between adjacent grains, the misorientation shows how close neighbouring grains are to each other in term of their preferred orentation. This data again shows that the CdTe films are highly orientated in the (111) direction regardless of whether it is deposited on CdS or CdS/CdSe[24,27,28]. Looking at the two EBSD images one could infer that changing the device window layer is having little impact on the back surface of the CdTe. This would again indicate that very little, if any Se is diffusing towards the back surface of the CdTe.

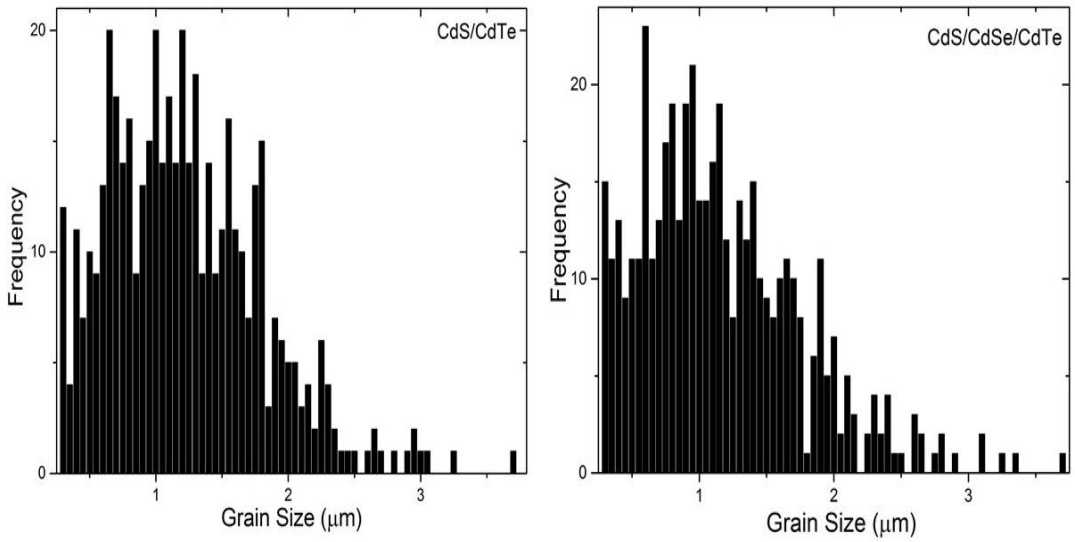

Figure 5.16: *Grain size distribution for EBSD images shown in Figure 5.15. Left panel CdTe grown on CdS and right panel CdTe grown on CdS/CdSe (100 nm). Grain sizes were taken from the EBSD maps shown in Figure 5.15a and d.*

The (111) pole figures are a contour stereographic representation of the inverse pole figure map and represents the orientation of each grain shown in the image. As the pole figures shown in Figure 5.15 are for the (111) projection, any grain orientated in the (111) direction will be shown in the centre of the map. It can clearly be seen that in Figures 5.15b and 5.15e that a high density of the grains are (111) orientated and therefore indicate that the CdTe film is predominantly (111) oriented. The inverse pole figure is also a contouring

representation of the number of grains that have a different orientation and from data presented in Figures 5.15c and f it is again clear that the CdTe films presented in Figures 5.15a and d are highly (111) orientated.

The grain size distribution for the CdTe layer when grown on CdS and CdS/CdSe was also investigated using the EBSD maps (Figures 5.15a and d) and is shown in Figure 5.16, to establish if the inclusion of Se had any impact on the CdTe grain size. From this data, it would appear that the Se incorporation has little influence on the grain size, with the average grain size being 1.20±0.58 µm and 1.14±0.59 µm for CdTe grown on CdS and CdS/CdSe respectively.

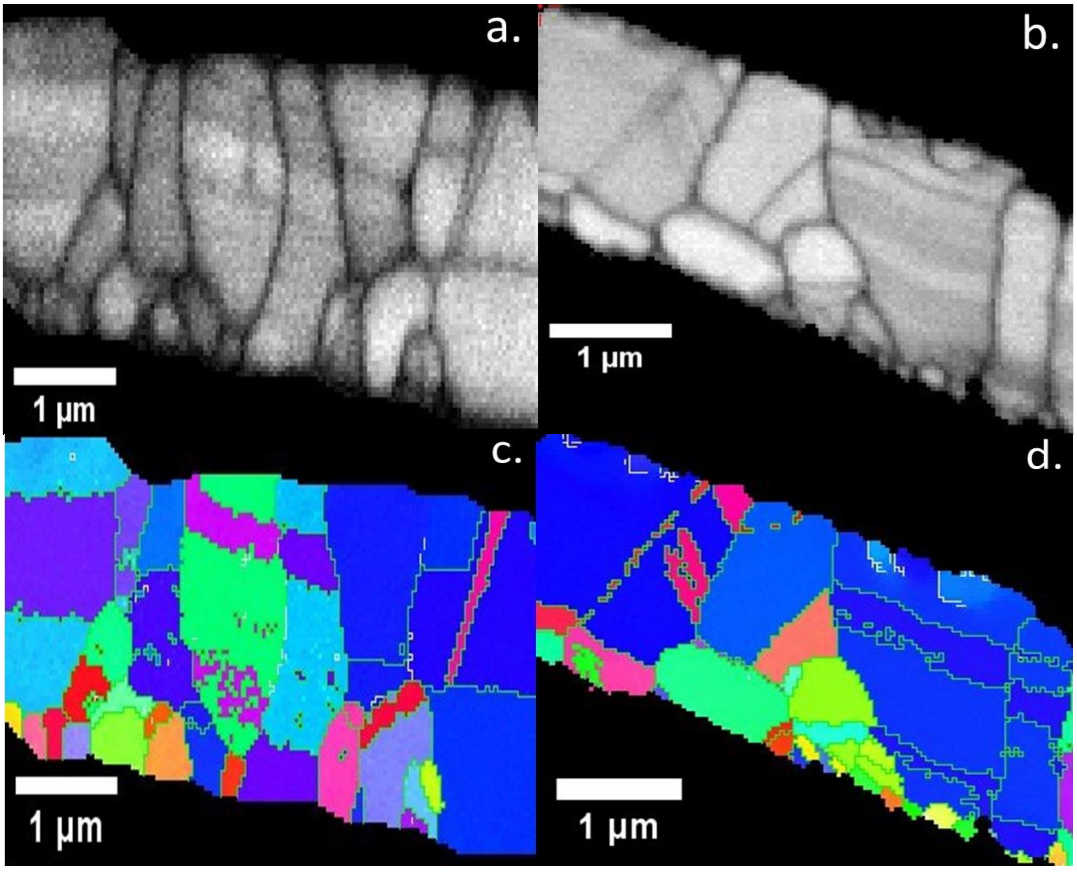

Figure 5.17: *Cross sectional EBS image of CSS grown CdTe deposited on a) CdS and b) CdS/CdSe window layer structures. The (111) cross sectional EBSD inverse pole figures for CdTe grown on CdS and CdS/CdSe are shown in c and d respectively.*

XRD and EBSD analysis indicated that depositing CdTe onto CdS or CdS/CdSe layers had no discernible effect on CdTe grain structure, orientation and size. However, it should be

noted that these techniques are preferentially probing the CdTe back surface and, as the device front interface is being altered, it is understandable that the back surface should be relatively unaffected by changing from a CdS window layer to a CdS/CdSe window layer.

It is also likely that, if any changes are to occur in the CdTe grain structure, it will be primarily at the CdTe/window layer interface. Therefore, in order to examine this, cross sectional EBS and EBSD of the CdTe layer grown on CdS and CdS/CdSe was undertaken (Figure 5.17a-d). From this data we can again see that the change of window layer is having little influence on the CdTe grain structure, with both structures demonstrating large columnar grains that in some cases extend the entire thickness of the CdTe layer. Again, the colours represent different grain orientations and misorientation between adjacent grains. From the EBSD images shown in Figure 5.17c and d, it can clearly be seen that both films demonstrate similar grain sizes and preferred orientations. In both EBSD images, a large amount of horizontal lines can clearly be seen. These horizontal lines represent twin boundaries present in the CdTe layer.

Therefore, using the data presented, the change in device window is having little influence on CdTe grain structure and preferred orientation throughout the film, including the near interface and back surface regions. This is probably to be expected as the underlying film for growth remains CdS in both the window layer structures which could be dictating the seed growth of the CdTe layer and resulting in little change to the CdTe layer.

Additional structural and chemical analysis was performed using scanning transmission electron microscopy (STEM) of focussed ion beam milled CdTe lamellas, Figure 5.18a and b shows cross sectional STEM images for CdS/CdTe and CdS/CdSe/CdTe device, respectively. From this data we can clearly see that incorporation of CdSe layers into CdS/CdTe devices has led to the formation of large voids, appearing as bright spots in the STEM image, can be seen at the front interface. One possible explanation for the void formation, is that excessive intermixing has occurred in this region between the CdS, CdSe and CdTe layers.

The intermixing has caused excessive diffusion of the CdS and CdSe layers, leading to the formation of voids which will be detrimental to device performance via the formation of $CdTe_{(1-x)}Se_x/SnO_2$ junction regions which would contribute to the observed reduction in V_{OC}. In addition to this, it has been previously demonstrated that voids present in the device structure would limit device V_{OC}, as has been reported for other PV architectures such as, CIGS and $Ag_2ZnSnSe_4$[29,30]. Avancini *et al*[31]*.* demonstrated that voids present in the device structure significantly reduced device performance, particularly affecting device V_{OC} and *FF*. It was found that voids introduced a high amount of unpassivated, highly recombinative free surfaces at the interface which increased the recombination velocity and reduced the V_{OC}. In contrast, the CdS/CdTe samples show a thin uniform CdS layer with no such voids at the interface, indicating a superior interface and possibly the reason for the enhanced device V_{OC}[29,30].

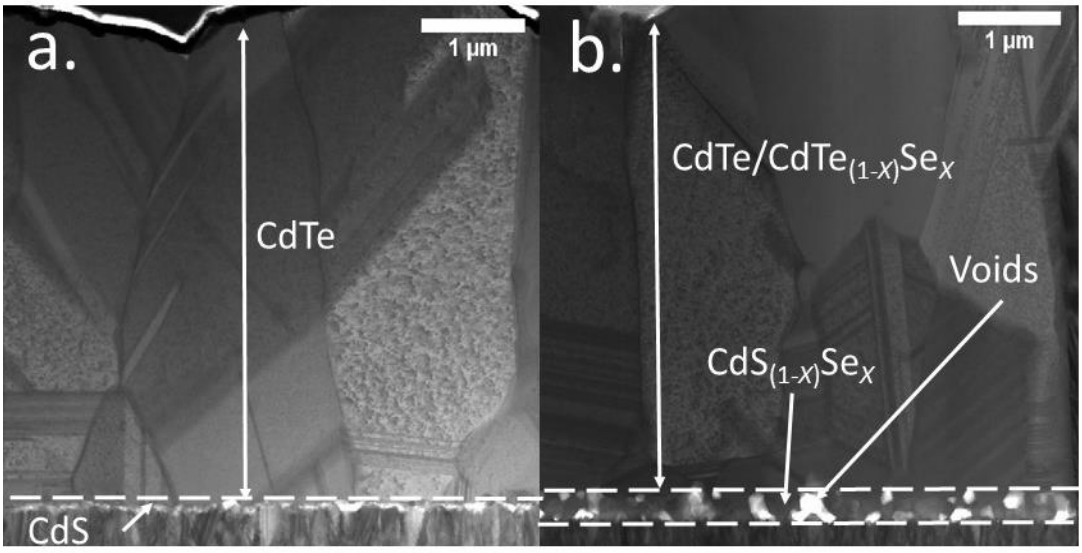

Figure 5.18: *FIB milled Cross sectional STEM of a) CdS/CdTe and b) CdS/CdSe (100 nm)/CdTe devices.*

From EQE analysis, it was believed that intermixing between the CdS and CdSe layers has also led to the formation of a large $CdS_{(1-x)}Se_x$ region at the front interface, the formation of this intermixed phase being the cause of the short wavelength losses observed in the device EQE response and resulting in the reduced device performance. To assess the formation of $CdS_{(1-x)}Se_x$ phases, elemental composition maps of the sample

interface using EDX analysis were undertaken (Figure 5.19). Figure 5.19b-e shows the Cd, S, Se and Te EDX map profiles for a CdS/CdSe/CdTe device with extracted EDS line scans from the front SnO_2 interface for all the elements is shown in Figure 5.19f. Voids in the sample can clearly be seen in the Cd and Te profiles with large gaps visible in the maps. Te can be seen in the glass sample because it can be difficult for the EDX measurement to distinguish between Sn and Te signals.

The intention behind the CdSe incorporation is that it should not diffuse into the CdS but should instead be consumed during the deposition of the CdTe layer. The Se content would be graded though the CdTe layer, resulting in a bandgap grading effect, with a high Se content at the near interface region and low Se content towards the back surface which would in theory, lead to an enhanced carrier lifetime[8]. From the Se profile (Figure 5.19d and f), it is clear that this is not the case with the Se and S showing nearly identical distributions, with Se heavily diffused into the CdS layer forming a $CdS_{(1-X)}Se_X$ phase. Despite the high temperature CdTe deposition conditions, the formation of this $CdS_{(1-X)}Se_X$ phase seems to have suppressed Se and S out diffusion into the CdTe layer. This can clearly be seen in the Te profiles (Figure 5.19e and f) with a large dark region at the front interface where the $CdS_{(1-X)}Se_X$ is still present. However, there is evidence of some Se out diffusion into the CdTe layer. The data presented here would seem to suggest that either a CdS/CdSe dual window layer is not suitable for CdTe PV applications or that the CdTe deposition needs to be significantly adjusted for this device structure to work efficiently. Further work will need to be carried out in order for this to be investigated, such as lower temperature for deposition or changing the pressure for CdTe growth to see whether the Se diffusion can actually be controlled by changing deposition conditions. It has previously been demonstrated that the $CdS_{(1-X)}Se_X$ phase is of a lower bandgap than CdS[22], therefore, by confirming the presence of this phase in the device structure it is therefore the likely cause of the losses observed in the short wavelength regions in the devices EQE response[32].

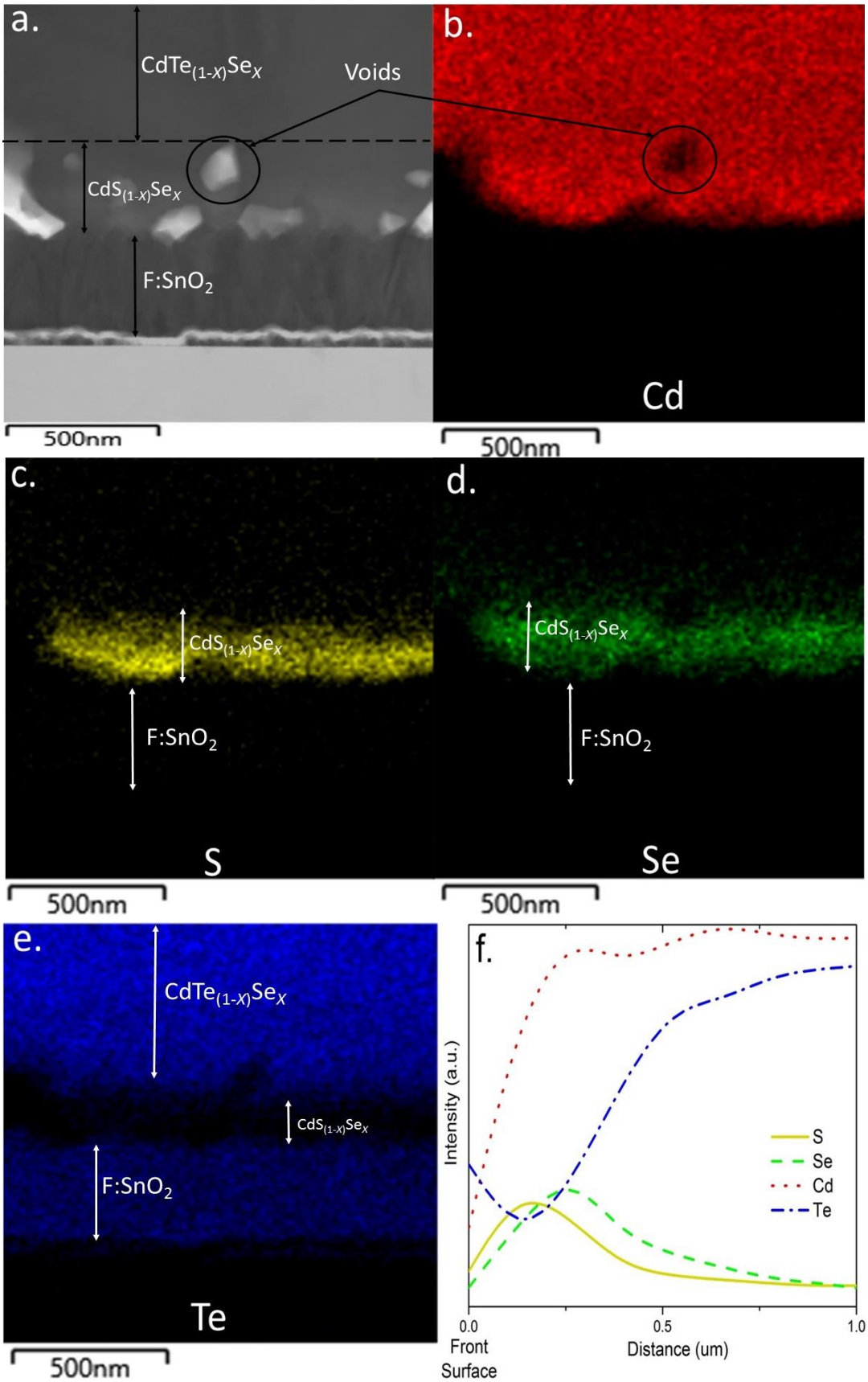

Figure 5.19: *EDX of the CdS/CdSe (100 nm)/CdTe cross sectional TEM image (a). The EDX is shown for the Cd (b), S (c), Se (d), and Te (e) profiles. The line scan for all the profiles is shown in f), the front surface represents the $SnO_2/CdS_{(1-X)}Se_X$ interface.*

The nature of the short wavelength losses observed by EQE (Figure 5.13b) can be spatially resolved via the use of EBIC analysis, with a high EBIC signal indicating regions of efficient carrier collection[33]. EBIC allows for direct visualisation of areas of high and low carrier collection efficiency on a solar cell cross section prepared by FIB milling. Using this information, the devices' junction position can be analysed (See Experimental section 4.3.5)[33,34]. Figure 5.20a and b shows overlaid secondary electron image (red) and EBIC signal (green) of CdS/CdTe and CdS/CdSe/CdTe device cross sections. The junction position was evaluated by extracting line scans from the EBIC signals and is shown in Figure 5.20c, with the marked front and back surfaces representing the SnO_2/CdS interface and the CdTe back surface respectively. The extracted line scans were normalised to 1 to allow direct comparison of the junction positions. There are distinct differences in the collection for the two cells structures: The cell with no CdSe layer shows a more "typical" p-n junction response with high collection at the CdS/CdTe interface and a poor collection towards the back surface of the cell (i.e. bright EBIC contrast)[34].

In contrast, the CdS/CdSe/CdTe cell shows little response at the region near to the CdS interface, but collection occurs throughout the remaining thickness of the cell. This EBIC data is again suggestive of a photoinactive region due to the $CdS_{(1-X)}Se_X$ phase being present at the near front surface. This is in accordance with EQE data presented in Figure 5.13b. High energy photons are predominately absorbed in the near interface region. Hence a photoinactive region would result in a greatly reduced EQE response at short wavelengths. The presence of this unwanted interfacial layer has effectively buried the junction and is the cause of the reduced J_{SC} observed[35]. The EBIC line scan (Figure 5.20c) also shows a degree of similarity to Te EDX profiles shown in Figure 5.19f, again an indication that the $CdS_{(1-X)}Se$ phase has resulted in a buried junction. The improved deep collection for the Se containing device could be an indication of enhanced carrier lifetime via bandgap grading[8]. This potential benefit is though undermined by the formation of $CdS_{(1-X)}Se_X$ phases which

may ultimately be a fundamental limitation of incorporating a CdSe layer when using a CdS layer and a high temperature CdTe deposition.

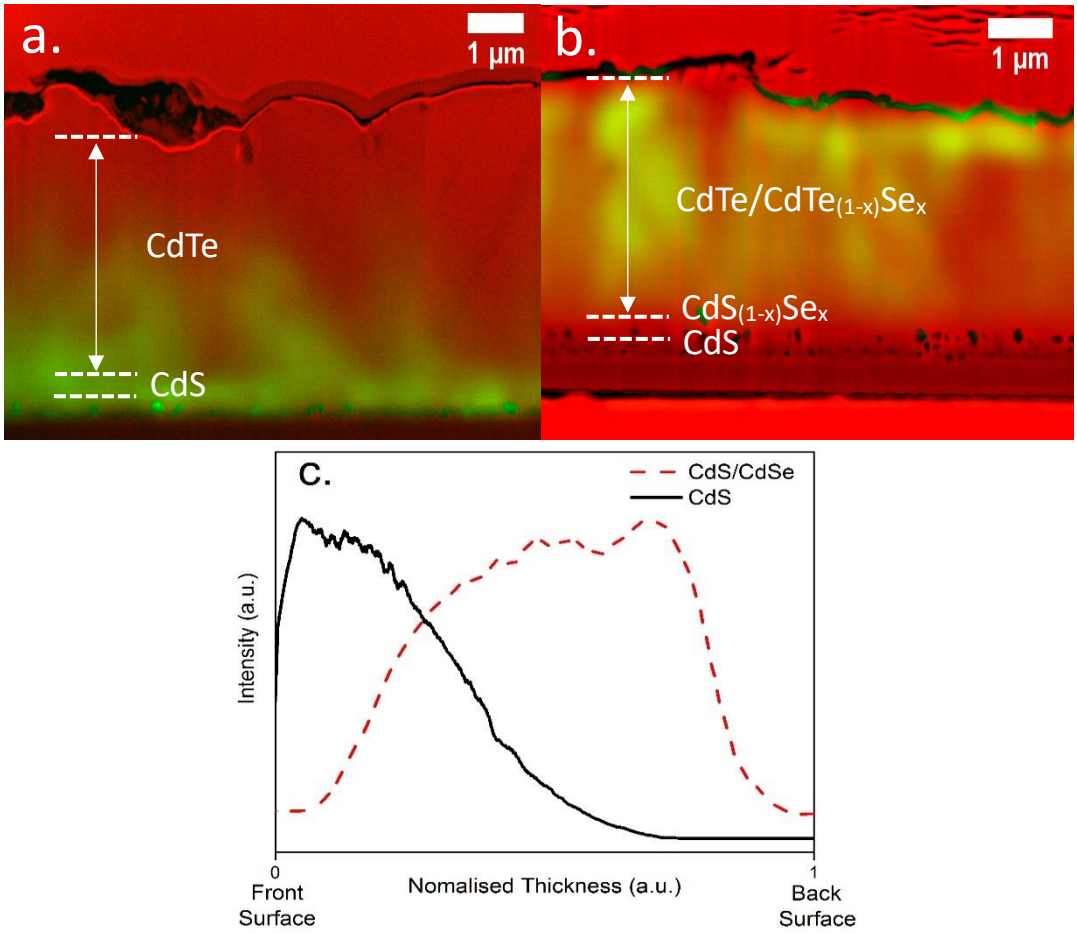

Figure 5.20: *Overlaid secondary electron (red) and EBIC output (green) for a) CdS/CdTe devices and b) CdS/CdSe (100 nm)/CdTe devices. The EBIC signal is overlaid on the SEM image to highlight the junction position. c) Shows the EBIC signal indicating the junction position with 0 representing the SnO_2/CdS interface and 1 representing the cells back surface, the line scan have been normalised to 1 so a direct junction comparison could be made.*

5.3.2.3. Post growth treatment of CdS/CdSe/CdTe devices

This section will report on efforts to try and control the Se diffusion by altering the CdTe deposition and device processing. The level of intermixing between CdTe and CdSe layers is liable to be controlled by two main factors: i) the CdTe deposition conditions; and ii) the post-growth chlorine treatment. In Section 5.2.3.2 it had been established that whilst the chlorine activation step was having some influence on device performance, it did not correct the issues associated with chlorine diffusion. It was established that the EQE

response was unaffected by the chlorine treatment and it was inferred form this that it was having little influence on the Se distribution. A similar effect was observed for Se diffusion when CdS was used rather than CdS:O, with there being little notable change in device performance and photo response when increasing the $MgCl_2$ annealing time from 20 mins to 120 mins (Figure 5.21, insert table shows highest efficiency contacts performance parameters). As previously discussed this is due to the large as-deposited grain size of CSS deposited CdTe. The chlorine step does not induce significant recrystallisation and therefore does not affect the amount of intermixing observed. Instead, the level of intermixing is primarily controlled by the higher temperature CdTe deposition step[11,16].

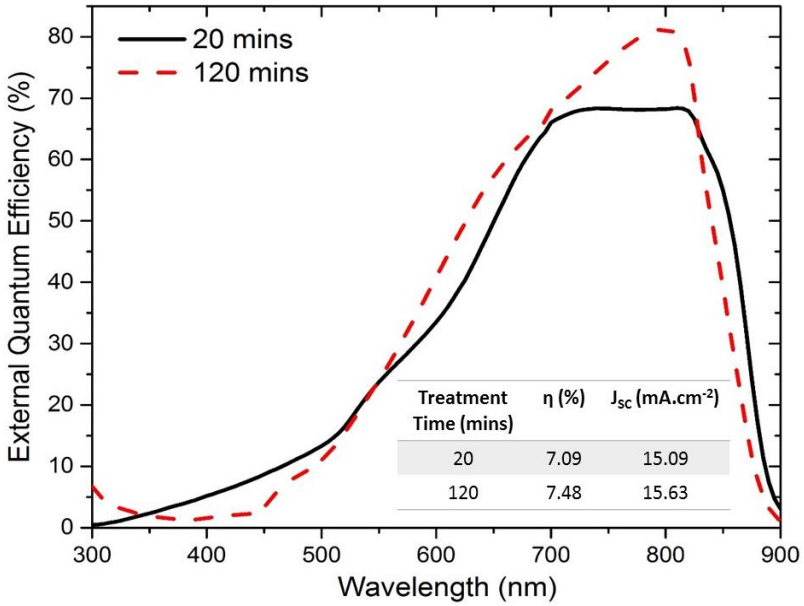

Figure 5.21: *The EQE curves generated for CdS/CdSe (100 nm)/CdTe cells using different chlorine treatment times at 430°C. Insert table includes the device η and J_{SC} values for highest efficiency contacts.*

In Section 5.3.2.2 it was shown that the CdS layer was effectively "capturing" Se and forming a $CdS_{(1-X)}Se_X$ phase which contributed to a reduced device performance. In order to improve device performance, different routes were required to preferentially diffuse the Se into the CdTe layer.

As it had been established the deposition step primarily controlled Se diffusion, to enhance the amount of Se-Te inter-diffusion occurring, post growth annealing was

performed in-situ in the CSS chamber at the growth temperature (610°C). Following completion of CdTe deposition, the source and substrate temperature were maintained at 610 °C and 510°C respectively, but an elevated N_2 pressure of 200 Torr was used to suppress further CdTe sublimation. A series of cells was produced with such post growth annealing ranging from 0 mins to 60 mins, with all other device processing conditions kept constant. Figure 5.22a-d shows the average performance parameters for devices with varying annealing times, with the *JV* and EQE responses for the highest efficiency contacts shown in Figure 5.23.

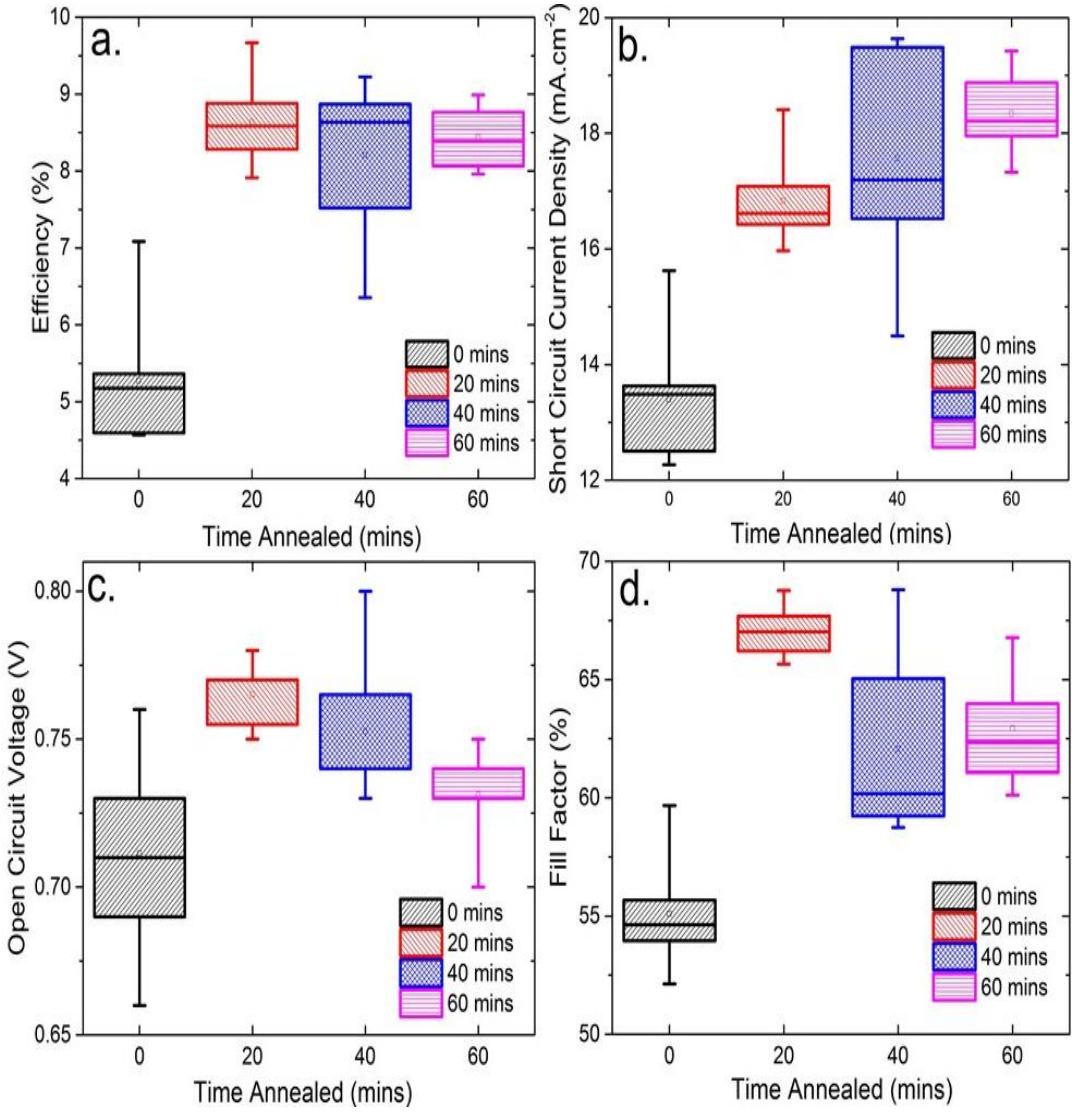

Figure 5.22: *SnO_2/CdS/CdSe (100 nm)/CdTe device performance parameters, a) η, b) J_{SC}, c) V_{OC} and d) FF as a function of in-situ post CdTe growth annealing times at 610°C.N=9.*

The post growth annealing showed some capacity to improve device performance, with all performance parameters being improved. J_{SC} was increased from 13.1 mA cm^{-2} to 18.3 mA cm^{-2} following a 60 mins anneal, with peak performance occurring following a 20 mins anneal; the EQE (Figure 5.23b) shows that the annealing resulted in some enhanced collection at short wavelengths[1]. If no further intermixing had been undertaken then EQE cut-off at short wavelength would have remained unchanged however, it is difficult to quantify the exact amount of intermixing that has occurred. This improvement in J_{SC} could be attributed to an increase in the availability of Se from the $CdS_{(1-X)}Se_X$ which has resulted in enhanced Se-Te intermixing. It can be inferred from this EQE response, that while some additional Se-Te inter-diffusion has occurred during annealing, as result of Se diffusing out of the $CdS_{(1-X)}Se_X$ phase, the performance was still limited.

The collection at wavelengths close to the CdTe band-edge was also enhanced which could indicate increased carrier lifetimes. Alternatively, it could indicate that a better-quality junction has been formed via recrystallisation or improved inter-diffusion at the interface. It should also be noted that the $CdTe_{(1-X)}Se_X$ absorption cut-off didn't change with increased annealing, suggestive of no significant change in the Se-Te intermixing, or at least no increase in the Se/Te ratio. The Se could have diffused further into the CdTe layer meaning a thicker $CdTe_{(1-X)}Se_X$ region but the bandgap has not been reduced any further. Whilst the average J_{SC} improves by annealing the devices for 60 mins, the overall cell performance is reduced due to a reduction in *FF* and V_{OC}, indicating the post growth treatment has become too intensive and is over treating the cells.

It would appear that while annealing helped somewhat with the Se-Te intermixing, it has not eliminated the issue of the $CdS_{(1-X)}Se_X$ phase as it appears to still be present in the device structure. It would therefore seem that the extent to which device processing can controllably affect interdiffusion is fundamentally limited.

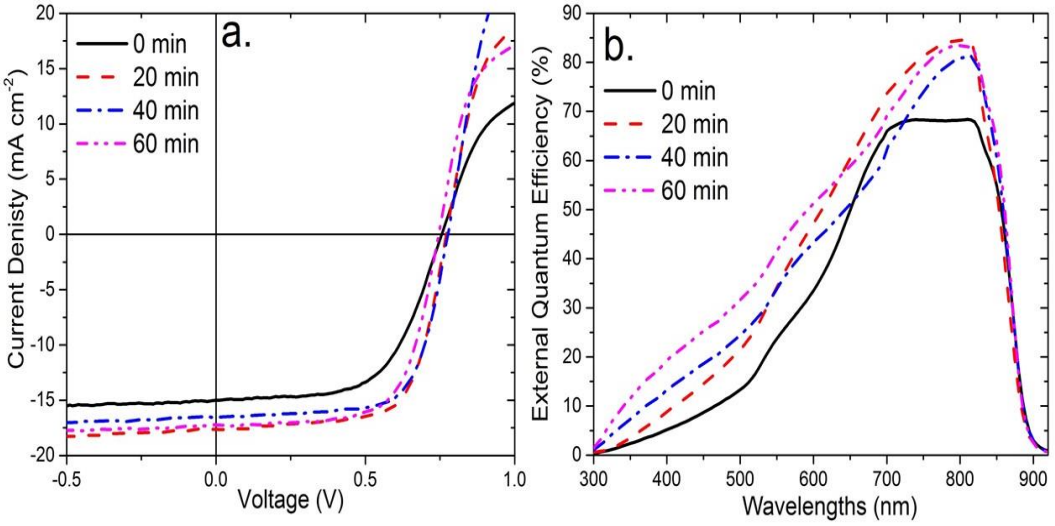

Figure 5.23: *a) JV and b) EQE responses for the highest efficiency SnO_2/CdS/CdSe (100 nm)/CdTe devices using different in-situ post CdTe growth annealing times at 610°C.*

5.3.3. Discussion

In this section the CdS/CdSe/CdTe device structure was investigated. It would appear that this structure is fundamentally limited due to enhanced optical losses at short wavelength due to the formation of a $CdS_{(1-X)}Se_X$ phase during CdTe deposition. This is supported by STEM data which suggests Se is diffusing into the CdS layer rather than into the CdTe layer during device processing. It also indicated that the intermixing of the CdS and CdSe layers was leading to the formation of voids at the interface which further limit cell performance. EDX and EBIC analysis confirmed that the presence of this $CdS_{(1-X)}Se_X$ phase was effectively resulting in a buried device junction, causing enhanced losses at short wavelength and the reduced device J_{SC}.

It has also been shown that the level of Te diffusion into the $CdS_{(1-X)}Se$ can be controlled to a point by adding an in-situ post CdTe growth anneal. This anneal did improve the device photo response at short wavelength, but, there still seemed to be a fundamental limitation to the level of Se incorporation into the CdTe layer that can be achieved. Results presented in this section and in Section 5.2 seem to strongly indicate that the CdS layer was the limiting factor to CdSe incorporation through the formation of a $CdS_{(1-X)}Se_X$ phase. Therefore, it was deemed that removing the CdS layer was essential in order to maximise

device J_{SC} and efficiency. Investigating the removal of the CdS layer will be the focus of the next section.

5.4. SnO_2/CdSe/CdTe devices: Removal of the CdS layer

In this section the hypothesis presented in Section 5.3.3 will be investigated; that replacing the CdS layer with an oxide layer in CdSe/CdTe based devices will lead to more effective Se incorporation and improved cell efficiencies. The CdS layer was initially replaced as the n-type window layer with a 100 nm SnO_2 layer. SnO_2 was chosen due to its wide bandgap (3.6 eV) and stability thus intermixing with CdSe should be negligible[36]. Previous work has shown that the use of a CdSe layer without CdS leads to the gains in J_{SC}, but losses in both *FF* and V_{OC}. It was hoped, that by incorporating the SnO_2 layer, such losses could be minimised[2]. The metal oxide is required because it has been previously shown that CdTe/TCO interfaces are of an inferior quality and therefore have a reduced V_{OC} and thus performance[37].

5.4.1. Device fabrication

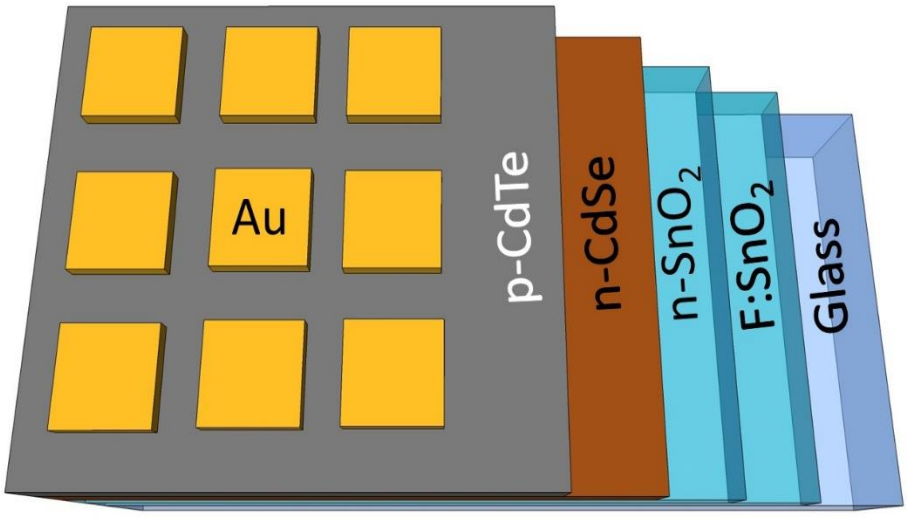

Figure 5.24: *Shows the schematic representation of the as-deposited SnO_2/CdSe/CdTe of the device structure used in Section 5.4.*

Device fabrication is similar to that previously described in Section 5.3.1. Figure 5.24 shows a schematic representation of the CdTe devices structure used in this section where the CdS layer has been replaced with SnO_2. In specified samples, a 5 nm Cu layer was also

deposited via thermal evaporation at the back surface to facilitate the formation of an Ohmic contact[38]. Cu was included in the device structure to overcome the roll-over problems that are observed in CdTe devices, no anneal was performed post Cu deposition.

5.4.2. SnO_2/CdSe/CdTe device and structural analysis

5.4.2.1. Comparison of CdS and n-SnO_2 layers in CdSe/CdTe devices

JV and EQE curves of the highest efficiency contacts for SnO_2/CdSe and comparative CdS/CdSe devices are shown in Figure 5.25a and b respectively, with extracted average and peak performance parameters shown in Figure 5.26. All CdTe growth conditions were kept identical, including the 20 mins post growth anneal at 610°C as this was shown to produce the best device response in Section 5.3.2.3 for CdS/CdSe based devices.

SnO_2 based devices yielded a slightly higher peak efficiency (10.05% compared to 9.67%) but a significant improvement in J_{SC} with peak value increasing from 18.4 mA cm^{-2} to 28.4 mA cm^{-2}. EQE analysis (Figure 5.25b) of the SnO_2/CdSe device shows a near optimal shape, with minimal losses and significantly higher collection at short wavelengths. It was expected that no cut-off related to the CdS would be observed but there appears to be no evidence of parasitic absorption from a residual CdSe layer. In addition to this the EQE response being enhanced at short wavelengths it has also been extended to longer wavelengths, indicating higher Se incorporation into the $CdTe_{(1-X)}Se_X$ compared to the CdTe growth on CdS. From this result, it is clear that the CdS was indeed the key limiting factor, again presumably due to the formation of $CdS_{(1-X)}Se_X$ phases which was limiting the Se out diffusion into the CdTe. The switch to a SnO_2 layer does however result in a drop in V_{OC}, with peak values decreasing from 0.77 V to 0.73 V. The device *FF* was also impacted falling from 68.1% to 48.5%, driven primarily by an increase in R_S which more than doubled from 6.6 Ω cm^{-2} to 13.5 Ω cm^{-2}. This increase in R_S and lower V_{OC} suggests that the SnO_2/$CdTe_{(1-X)}Se_X$ interface is of a lower quality than the CdS/CdTe or CdS/$CdTe_{(1-X)}Se_X$ interfaces, this could be due to a number of issues, such as a poorer band alignment and the lattice

mismatch being enhanced leading to a higher number of defect states at the interface. The calculated lattice mismatch between CdS/CdTe is approximately 10% whereas for SnO_2/CdTe it is approximately 40%. The high lattice mismatch between the layers will create a large amount of strain at the interface and is liable to result in a reduced device performance[21].

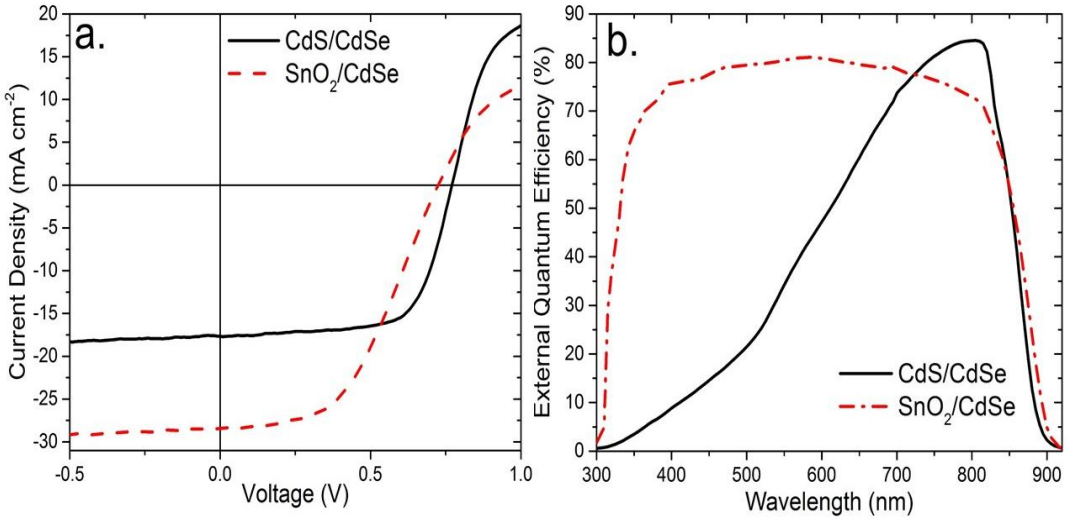

Figure 5.25: *a) JV and b) EQE data for cells produced using SnO_2 as the n-type window rather than the conventional CdS for CdSe (100 nm)/CdTe devices. Cells were produced with a 20 min in-situ post growth anneal at 610 °C.*

It also worth mentioning the large performance variation in the SnO_2/CdSe based devices compared with the CdS/CdSe devices, 4.4% to 10.1% for the SnO_2/CdSe devices and 7.91% to 9.66% for the CdS/CdSe. One possible explanation for this is the performance of SnO_2/CdSe devices is likely to be controlled by Se diffusion into the CdTe layer. Variations in temperature across the substrate are liable to cause variations in Se diffusion rate and thus lead to fluctuations in performance. As S diffusion is slower it is less likely to be affected variations in composition and performance.

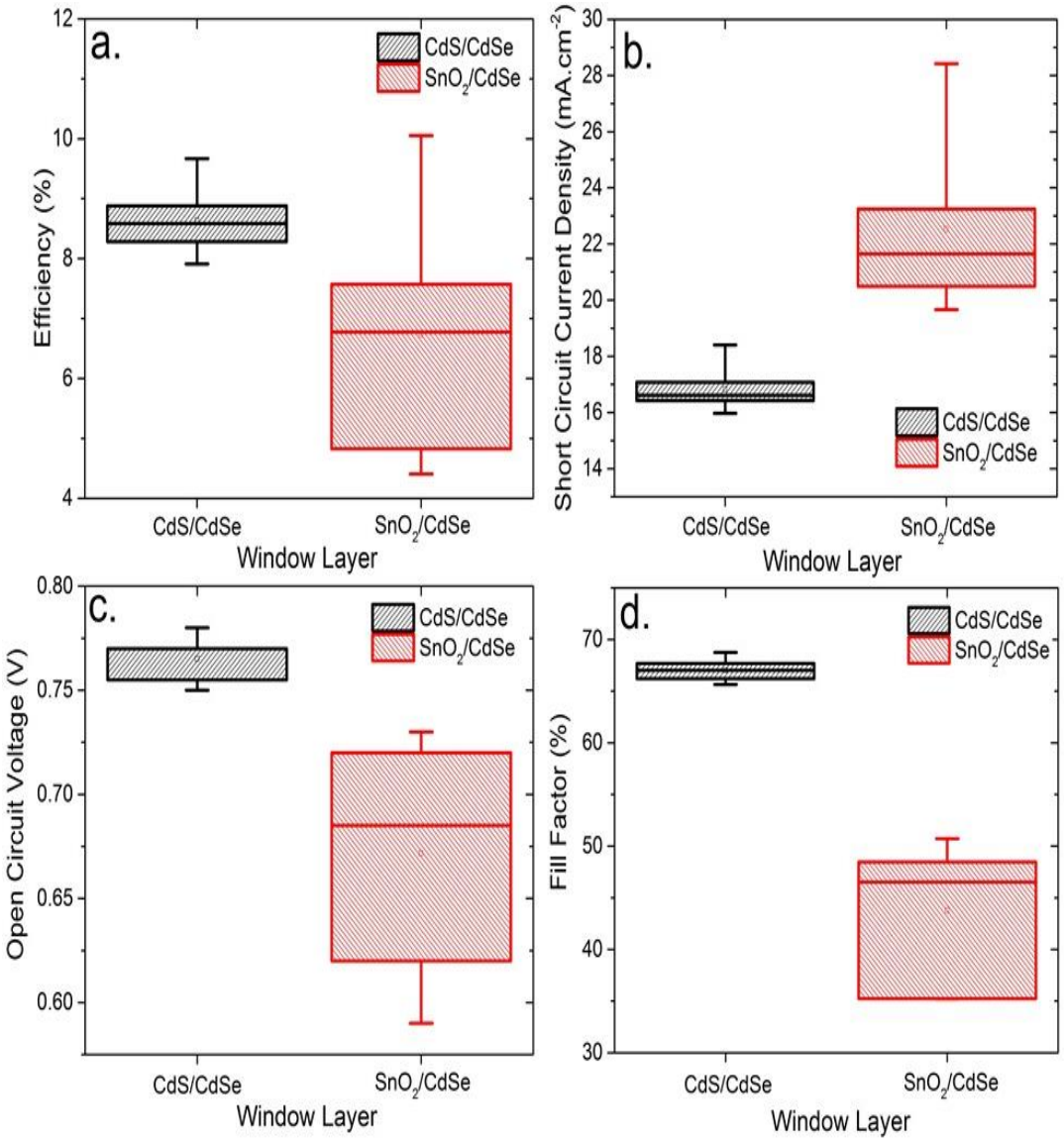

Figure 5.26: *Device performance parameters, a) η, b) J_{SC}, c) V_{OC} and d) FF for cell using CdS or SnO_2 as the device window layer in CdSe (100 nm)/CdTe devices. Cells were produced with a 20 mins in-situ post growth anneal at 610°C.N=8.*

5.4.2.2. Structural analysis of SnO_2/CdSe/CdTe devices

EBIC analysis was performed to analyse the junction position of the SnO_2/CdSe based devices. Figure 5.27a shows a cross sectional SEM image of a SnO_2/CdSe/CdTe device with an overlaid EBIC output signal in Figure 5.27b. It is worth noting that from the cross sectional SEM image there is still void formation at the front SnO_2 interface similar to that observed for CdS/CdSe devices, again this could be due to intermixing and recrystallization of the CdSe layer which is creating these voids at the interface during CdTe deposition.

The EBIC signal for the SnO_2/CdSe based devices now show more typical p–n junction characteristics, with the majority of the collection occurring at the front SnO_2 interface and relatively little collection at the back surface. This would seem to confirm the removal of the CdS layer has effectively removed the buried junction and this is the reason for the enhanced J_{SC} in the SnO_2/CdSe based devices when compared to the CdS/CdSe devices.

The improvement in junction position can be most clearly seen in the EBIC line scans shown in Figure 5.27c, where the junction position for CdS/CdSe/CdTe and SnO_2/CdSe/CdTe devices are directly compared. Samples thicknesses have been normalised with respect to 1, with 0 representing the front device interface and 1 representing the CdTe back surface. The SnO_2/CdSe based devices show a much higher photo response near the front interface compared to the CdS/CdSe based devices where the junction was effectively buried.

In order to correlate the EBIC signal with the Se distribution, secondary ion mass spectrometry (SIMS) was undertaken. Figure 5.27d shows the normalised Se profiles for both CdS/CdSe/CdTe and SnO_2/CdSe/CdTe devices, Se counts and sample thickness have been normalised to 1, with 0 representing the front SnO_2/CdS or SnO_2/CdSe interface and 1 representing the CdTe back surface. From this data it is clear that the Se has diffused much further into the sample in the CdS free devices with a significant Se content being detected further into the CdTe layer This would seem to support the EDS and TEM data presented in Figure 5.19 where the Se distribution was limited due to the presence of the CdS layer. The data presented in Figure 5.27 further supports the hypothesis that a dual window layer containing CdS/CdSe is detrimental to device performance, with a more ideal device response occurring in the CdSe based devices without a CdS layer.

It is also apparent that the Se distribution in the SnO_2/CdSe shows little sign of a graded Se content and therefore a graded bandgap. Instead we see a high Se content at the near interface, then a large region with a negligible Se content. From this data it would appear as if device processing needs to be re-optimised in order to try to control the Se distribution throughout the sample. It should be noted that sharp increases observed at the back surface are an artefact of the measurement, due to a change in the ion yield in the pre-equilibrium region during the early stages of the sputtering process.

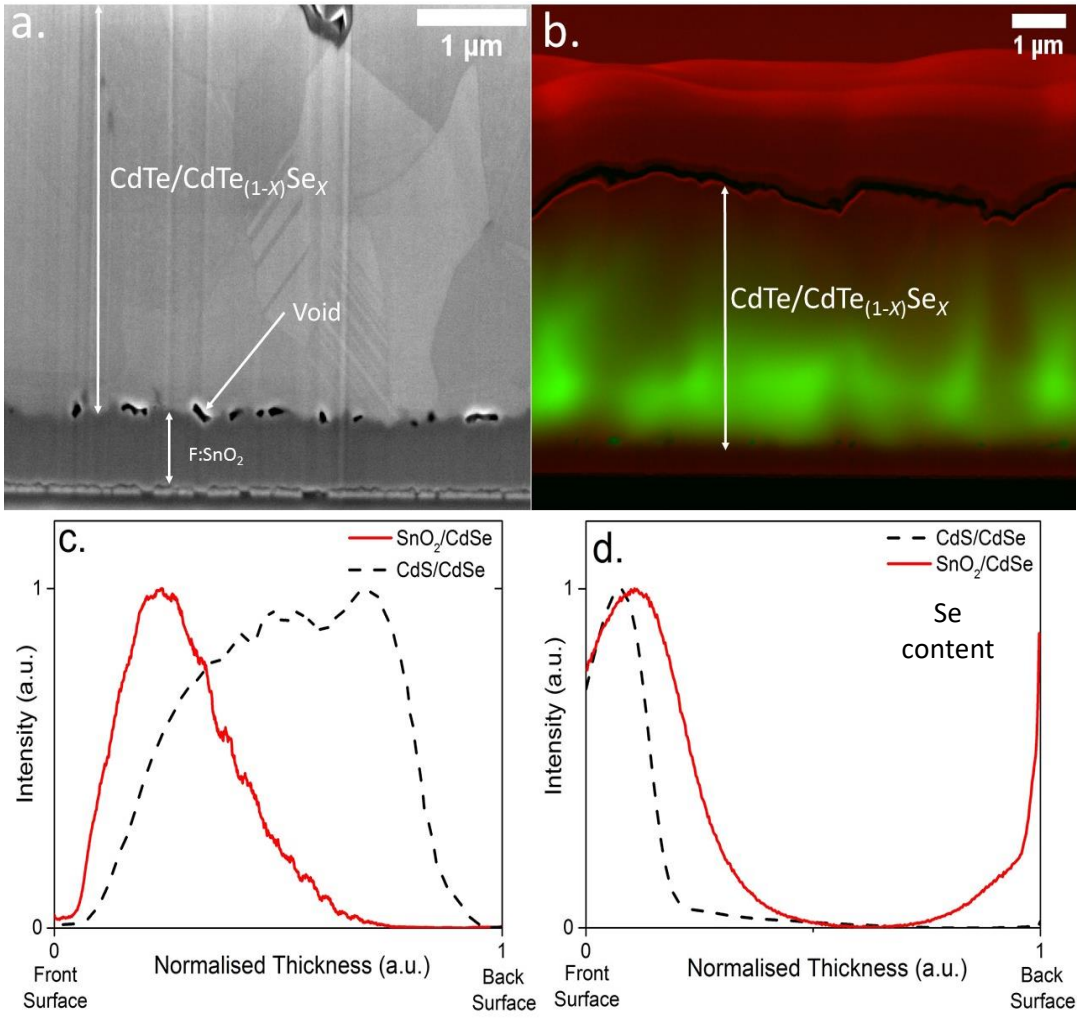

Figure 5.27: *a) Cross sectional SEM image and b) secondary electron image (red) with overlaid EBIC output (green) for SnO_2/CdSe/CdTe devices. c) extracted EBIC line scans showing device junction position EBIC signal representing the junction position and d) secondary ion mass spectrometry (SIMS) data showing the Se distribution through the sample for CdS/CdSe/CdTe and SnO_2/CdSe/CdTe devices, Se counts have been normalised to 1. For the normalised thicknesses 0 represents the front device interface and 1 represents the cells back surface.*

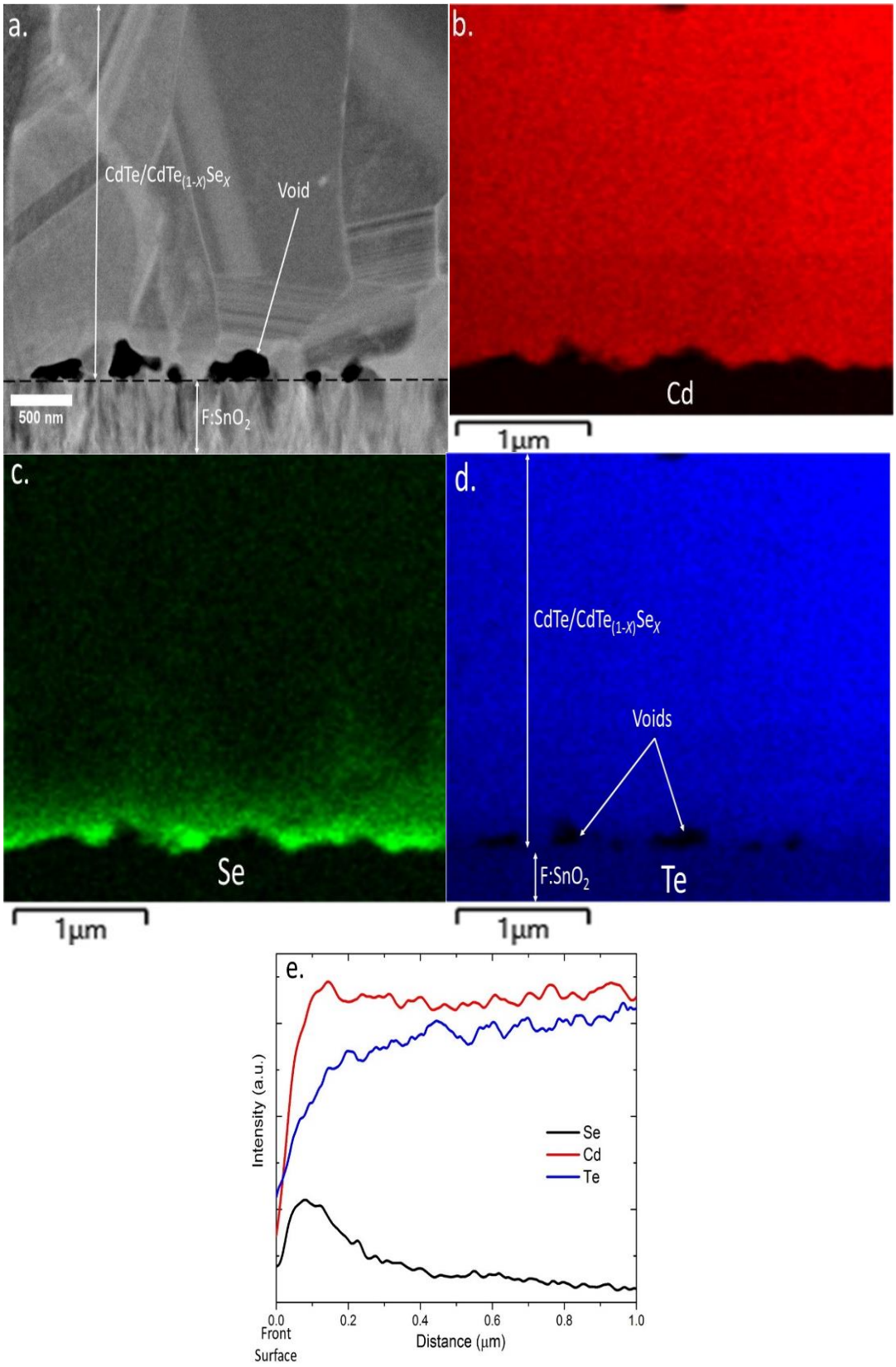

Figure 5.28: *STEM image the SnO_2/CdSe/CdTe FIB cross section (a). EDX are shown for the Cd (b), Se (c) and Te (e) profiles. The EDX line scans for all the maps are shown in f). The front surface represents the SnO_2/CdSe interface.*

Figure 5.28a shows a cross sectional TEM image of a SnO_2/CdSe/CdTe based device with extracted Cd, Se and Te profiles from EDX shown in Figure 5.28b, c and d respectively. The extent of voids present at the interface can be seen much more clearly in this TEM image compared to SEM analysis (Figure 5.27a). They can also be seen in the Cd and Te profiles. Again, the presence of void formation is an indication that CdSe and CdTe intermixing is leading to excessive void formation at the device front interface and removal of the CdS layer has not helped eliminate this problem. The CdTe layer structure seems unaffected by being deposited onto CdSe as the grain structure looks relatively similar to the CdTe deposited on CdS and CdS/CdSe (Figure 5.18).

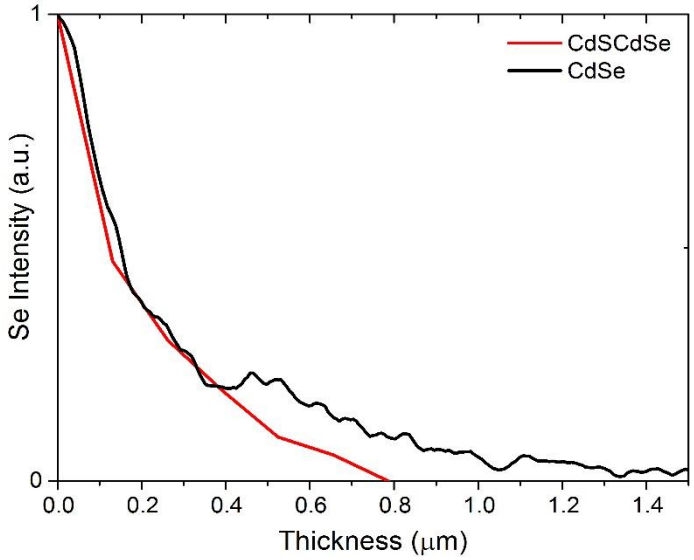

Figure 5.29: *Shows the extracted Se profiles from the EDX line scan for CdS/CdSe/CdTe stacks (Figure 5.19f) and SnO_2/CdSe/CdTe stacks (Figure 5.28e).*

The Se EDX profile (Figure 5.28c) shows a high Se content within 200 nm of the SnO_2/CdSe interface with relatively limited diffusion towards the back surface, however, it does demonstrate that some grading has been achieved in first 500 nm. Figure 5.29 shows a comparison of the Se EDX line scans produced for the CdS/CdSe and SnO_2/CdSe based stack. Se does appear to have diffused further into the CdTe layer when compared to the CdS/CdSe based structure, this supports the SIMS data shown previously (Figure 5.27d). The Te profile (Figure 5.28d) however, looks very different to the CdS/CdSe device structure

with Te now diffusing all the way to the SnO_2 front interface forming the $CdTe_{(1-X)}Se_X$ phase, as the Te signal can now be seen throughout the entire device stack compared to the Te signal produced for CdS/CdSe/CdTe stacks where relatively little Te can be seen at the near interface region. The Se map and the EDX line scan again do little to suggest that a graded Se content and thus a graded bandgap has been achieved, this is in accordance with the SIMS data shown previously.

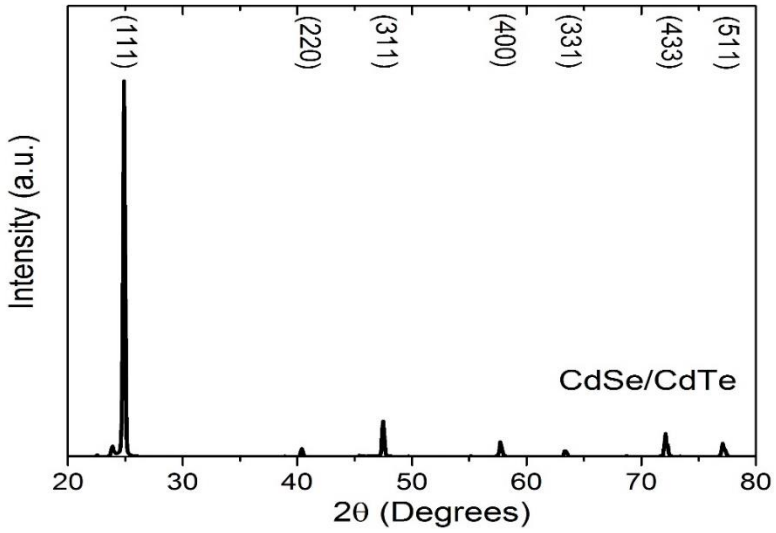

Figure 5.30: *XRD pattern of CdTe grown via CSS deposited onto SnO_2/CdSe (100 nm) layers*

Figure 5.30 shows the XRD pattern for CdTe deposited onto SnO_2/CdSe, Table 5.2 shows that calculated texture coefficients. The XRD pattern produced is very similar to the one presented for CdTe grown on CdS/CdSe layers (Figure 5.14a), where the CdTe film is highly orientated in the (111) direction. The standard deviation for data is 1.85 compared to 2.03 for CdTe deposited on SnO_2/CdSe and CdS/CdSe respectively, this indicates that the CdTe films grown on CdSe have a slightly reduced (111) preferred orientation compared to those grown on CdS/CdSe[26,28].

Table 5.2: *Calculated texture coefficients and standard deviation for CdTe grown on CdSe (100 nm) layer.*

Window layer	C_{111}	C_{220}	C_{331}	C_{400}	C_{331}	C_{433}	C_{511}	Σ
SnO_2/CdSe	5.53	0.12	0.52	0.22	0.08	0.34	0.19	1.85

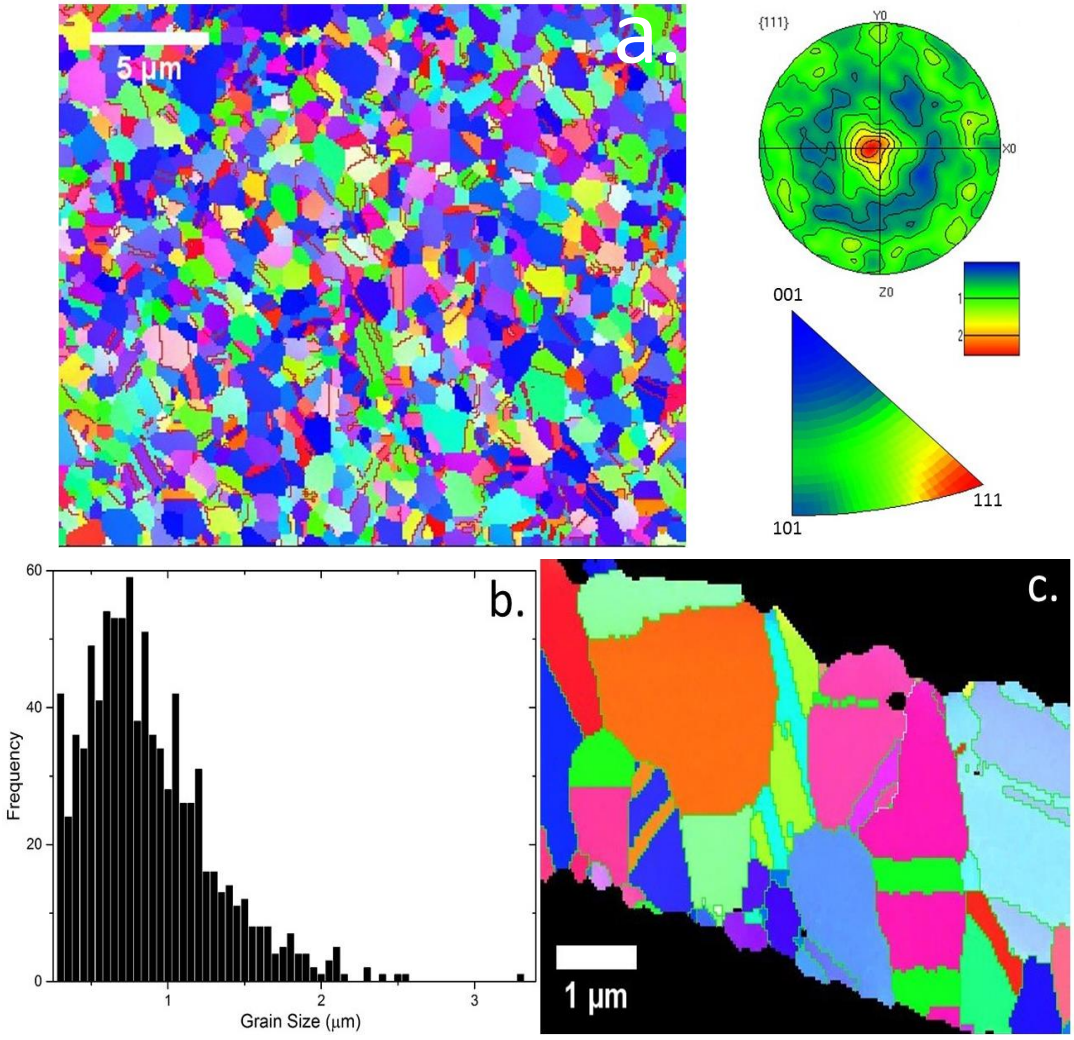

Figure 5.31: *a) Planar EBSD inverse pole figure map for CSS grown CdTe on CdSe (100 nm) layers, the (111) pole and inverse pole figure are also shown. b) Grain size distribution in the EBSD image and c) a cross sectional EBSD map for CSS grown CdTe on CdSe layers. The different colours represent the different orientations and the misorientation angle between adjacent grains.*

Figure 5.31a shows the planar EBSD inverse pole figure maps produced for a SnO_2/CdSe/CdTe based structure, the (111) pole and inverse pole figures are also shown, along with the grain size distribution in Figure 5.31b. The CdTe again exhibits a clear (111) preferred orientation and it appears CdTe deposited via CSS is highly orientated in the (111) direction irrespective of the window layers structure used. However, changing the window layer from CdS to CdSe has had a significant impact on the grain structure (Figure 5.31b), as CdTe grown directly on CdSe has a much lower average grain size compared to the CdTe

grown on CdS and CdS/CdSe[24,27]. The average grain size produced for SnO_2/CdSe/CdTe structure is 0.84 ±0.41 μm this is smaller than for the other structures where the majority of the grains were > 1 μm (Figure 5.16). At present, it is unclear if this reduced grain size is having a significant impact on the device performance. Further studies on the growth of the CdTe layer via CSS and its impact on device performance will need to be investigated.

Figure 5.31c shows a cross sectional EBSD image for a SnO_2/CdSe/CdTe device. Depositing CdTe on CdSe seems to have slightly effected the preferred orientation throughout the CdTe film with a more random orientation being observed at the front device interface and in the bulk when compared to the back surface image (Figure 5.30a). This would seem to confirm that whilst depositing CdTe on SnO_2/CdSe rather CdS is having a slight influence on the CdTe grain structure, the overall difference in the grain structure and preferred orientation, when compared with data presented in Figures 5.15 and 5.18 for the CdS and CdS/CdSe window layer structures is relatively minor.

5.4.2.3. Copper contacting of SnO_2/CdSe/CdTe devices

Prior to this point in the project, back contacting had been via a simple Au contact. Whilst it was appreciated this would likely lead to a non-ideal contact it was felt exclusion of Cu removed an additional factor from the processing. However, due to the persistent high degree of back contact related rollover observed for prior device sets (see for example Figure 5.25a), a Cu contacting step was included at this point in the project. To minimise rollover and improve the *FF* a 5 nm layer of Cu was thermally evaporated onto the CdTe back surface following $MgCl_2$ treatment but prior to gold back contact being applied[39]. Initial sample sets had not included Cu so the effect of Se could be investigated without being influenced by Cu. However, it was always anticipated that the optimal SnO_2/CdSe/CdTe would likely require Cu inclusion. Figure 5.32 shows the *JV* curves for the highest efficiency contacts when a 5 nm Cu layer is included into the SnO_2/CdSe/CdTe device structure. The inclusion resulted in a significant increase to the device *FF* improving

from 48.5% to 63.3% and has resulted in 3% improvement to device efficiency, improving from 10% to > 13%. Because of the significant performance improvement, the Cu contacting step was adopted, and devices discussed from this point include Cu in the device structure.

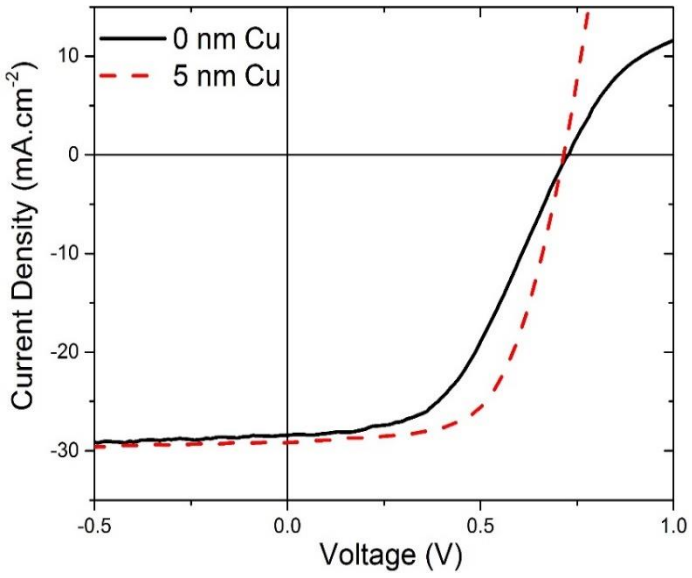

Figure 5.32: *JV curves produced for SnO_2/CdSe/CdTe devices with and without a 5 nm Cu layer added to the device structures back contact.*

5.4.2.4. Post growth annealing of SnO_2/CdSe/CdTe devices

Following the switch from a CdS to a SnO_2 layer and analysis of initial test devices, it was apparent a degree of process re-optimisation was required. In-situ annealing post-CdTe deposition had been observed to have the largest impact on CdS/CdSe devices (see section 5.3.2.3). Hence this process was re-assessed for SnO_2/CdSe based cells. As before devices were annealed following CdTe deposition in the CSS chamber at 610 °C for either 0 mins, 20 mins or 40 mins, with the influence on device performance being shown in Figure 5.33a-d. The *JV* and EQE curves for the highest efficiency contacts are shown in Figure 5.34a and b, respectively. The large variation observed in performance is likely due the lack of control of the Se distribution and the non-uniformity of the CSS deposition.

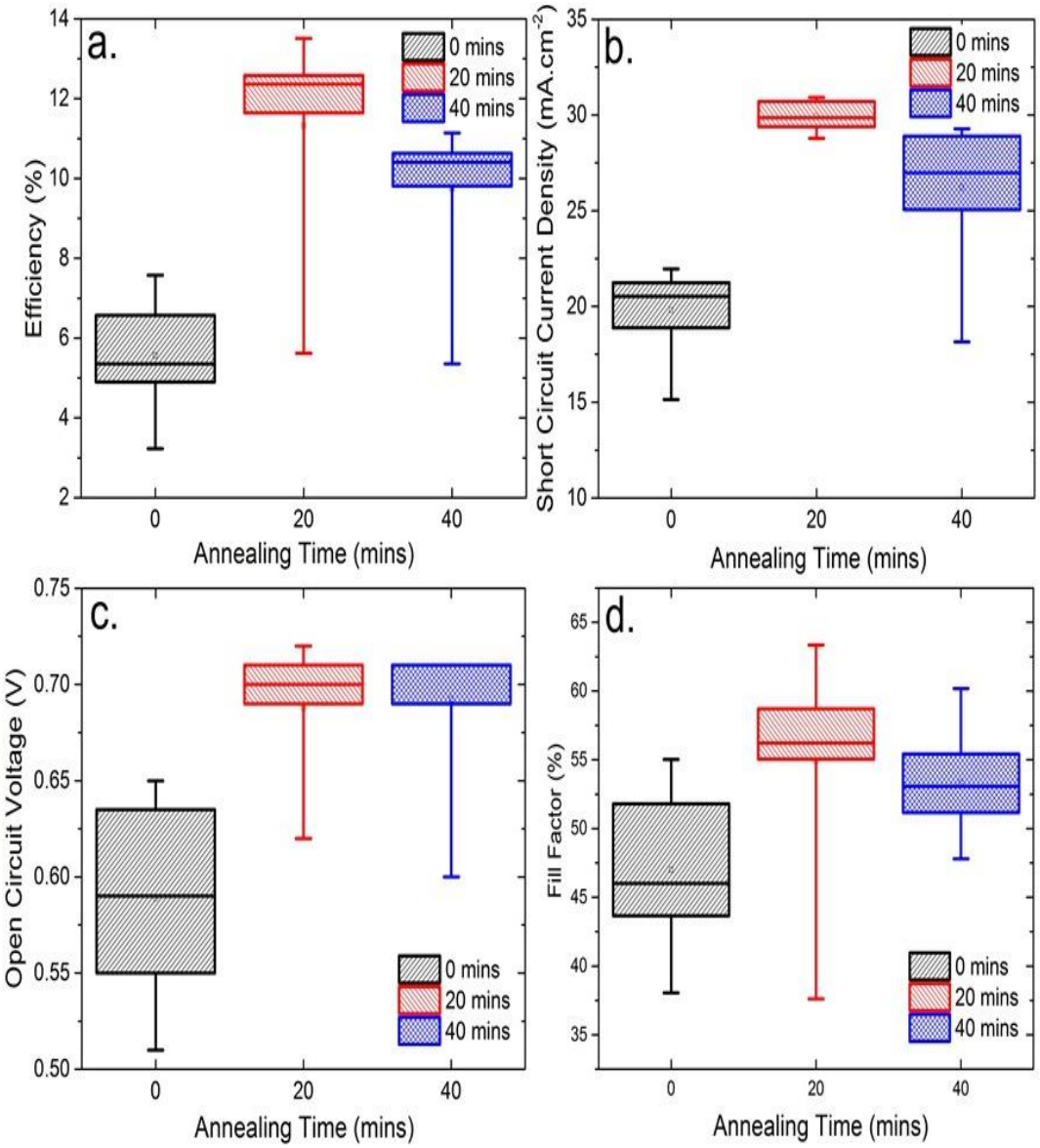

Figure 5.33: *SnO_2/CdSe (100nm)/CdTe device performance parameters a) η, b) J_{SC}, c) V_{OC} and d) FF for cells produced using different in-situ post CdTe growth annealing times at 610 °C. A 5 nm layer of Cu was added to the back contact. N=8.*

Devices with no post growth annealing (0 mins) had low performance, with an average efficiency of only 5.5%. In-situ annealing the devices for 20 mins significantly improved the performance, with all device parameters being increased and giving an average performance of 11.3%. EQE analysis (Figure 5.34b) shows an improvement at short wavelengths, indicating this post-growth annealing is influencing the near interface region, and results in a J_{SC} improvement from 21.6 mA cm^{-2} to 29.6 mA cm^{-2}, approaching the theoretical limit for this device structure. Average device V_{OC} improved significantly

increasing from 0.58 V to 0.70 V, following a 20 mins anneal. This could be due to the removal of the residual CdSe layer at the SnO_2/CdSe/CdTe interface forming a complete SnO_2/$CdTe_{(1-X)}Se_X$ interface, which it has been shown to be a superior interface and results in the observed enhanced device V_{OC}. The improvement to device *FF* is driven by an improvement to the device resistive properties with R_S decreasing from 9.1 Ω cm^{-2} to 4.4 Ω cm^{-2} and R_{SH} increasing from 502.7 Ω cm^{-2} to 1117.3 Ω cm^{-2} following a 20 min anneal.

Annealing the devices for 40 mins leads to a loss in performance with the average dropping to 9.7%, with J_{SC} and *FF* dropping but with V_{OC} being maintained. The EQE response is uniformly reduced across the entire spectral range which is resulting in the J_{SC} loss. The drop in *FF* is due to R_S increasing from 4.4 Ω cm^{-2} to 6.0 Ω cm^{-2} and R_{SH} decreasing from 1117.3 Ω cm^{-2} to 592.0 Ω cm^{-2} following a 40 min anneal. This suggests that the devices have now become over treated due to the enhanced device treatment and this is resulting in the lower performance.

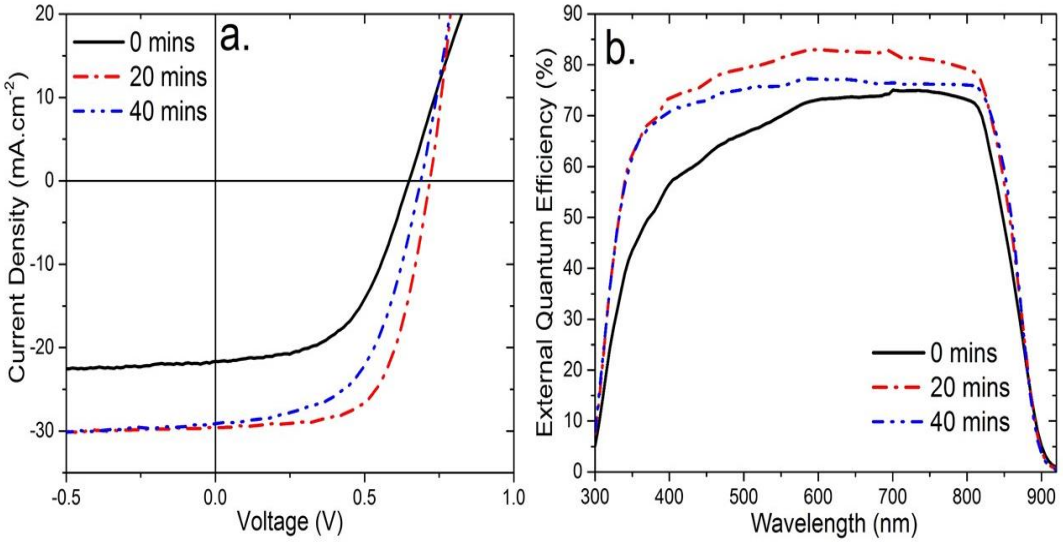

Figure 5.34: *a) JV and b) EQE data for highest efficiency contacts from cells produced using different post CdTe growth in-situ annealing times at 610 °C on SnO_2/CdSe (100 nm)/CdTe based devices. A 5 nm layer of Cu was added at the back contact.*

It has been suggested by Poplawsky *et al*[3]. from analysis of EBIC and atom probe tomography that the CdSe wurzite phase is photoinactive whereas the $CdTe_{(1-X)}Se_X$ zincblende structure is photoactive[8,15]. It may be postulated then that the unannealed

samples retain some of the unconverted CdSe phase, resulting in a lower performance. Annealing may have the effect of fully converting the remaining CdSe to the $CdTe_{(1-X)}Se_X$ phase hence the improved collection at the near interface observed in EQE. It should also be noted that annealing the films does not change the apparent EQE bandgap cut-off at long wavelength, suggesting that the further Se out-diffusion is not resulting in a further reduction to the bandgap This could indicate that rather than the Se/Te ratio being increased, the Se is diffusing into the CdTe layer or that Te is diffusing further into the CdSe region. The general improvement in device performance parameters would also suggest that the residual CdSe layer has been removed from the device structure, as the resistive losses have decreased and the V_{OC} has increased, indicating a reduced level of recombination and the more favourable $SnO_2/CdTe_{(1-X)}Se_X$ interface has now formed, rather than the less than ideal $SnO_2/CdSe/CdTe_{(1-X)}Se_X$ interface[40].

5.4.2.5. Influence of CdSe thickness on SnO_2/CdSe/CdTe devices

In addition to optimisation of the post growth annealing, the thickness of the CdSe layer in CdS free devices was also investigated ranging from 0 - 400 nm. Figure 5.35a-d shows the influence of CdSe thickness on device performance parameters for SnO_2/CdSe/CdTe cells, with the accompanying *JV* and EQE responses for the highest efficiency contacts shown in Figure 5.35e and f respectively. From this data it is clear that there appears to be a limit to the amount of CdSe that can be incorporated into the device structure, as thicknesses greater than 100 nm lead to losses in J_{SC} due to parasitic absorption visible at short wavelength in the device EQE response. In addition to this, the bandgap shift also seems to become saturated with increasing CdSe layer thickness, Table 5.3 shows the calculated bandgaps as estimated by the long wavelength EQE cut-off, i.e. the lowest

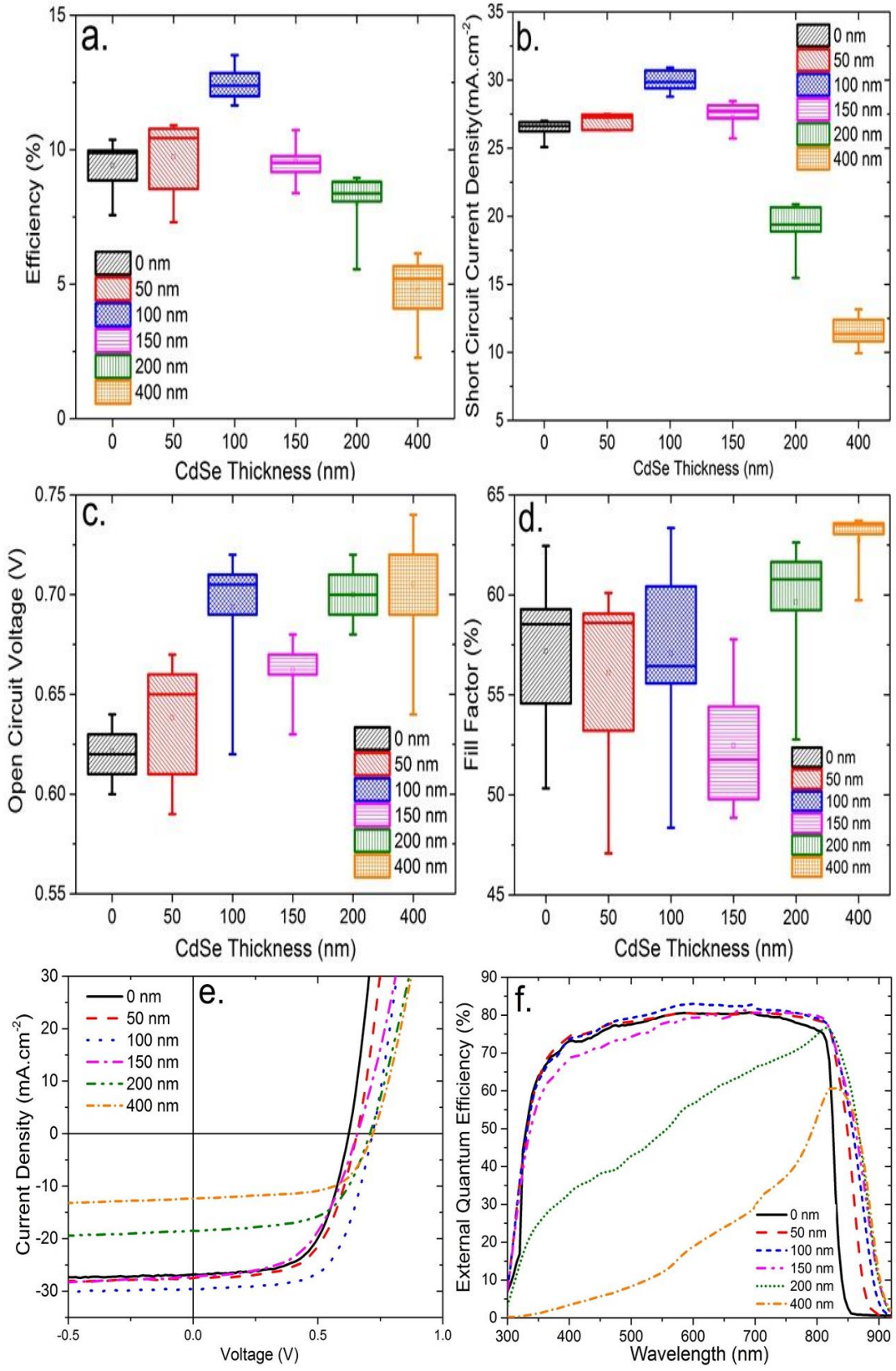

Figure 5.35: *Influence of CdSe thickness on device performance parameters of SnO_2/CdSe/CdTe cells, a) η, b) J_{SC}, c) V_{OC} and d) FF. N=9.. e) and f) show the JV and EQE data for the highest efficiency contacts. All devices were treated with a 20 mins in-situ post CdTe growth anneal at 610°C and a 5 nm Cu layer at the back contact.*

bandgap region present in the EQE response. The effective bandgaps ranged from 1.49 eV to 1.36 eV when 0 nm and 400 nm CdSe layer were incorporated, however the bandgap reduction has effectively saturated at 1.36 eV following 150 nm of CdSe. The device V_{OC} initially improves with CdSe incorporation increasing from an average of 0.62 V to 0.70 V when 0 nm and 100 nm CdSe layers are incorporated into the device structure, indicating that the $SnO_2/CdTe_{(1-X)}Se_X$ interface is of a superior quality compared to the SnO_2/CdTe interface. However, increasing the CdSe layer further has little influence on device V_{OC}[4], whilst the *FF* seems relatively unaffected by increasing the thickness of the CdSe layer.

Table 5.3: *The effective bandgaps of the $CdTe_{(1-X)}Se_X$ absorber as a function of CdSe layer thickness. Bandgaps were estimated from the external quantum efficiency cut-off.*

CdSe thickness (nm)	**0**	**50**	**100**	**150**	**200**	**400**
BandGap (eV)	1.49	1.41	1.38	1.36	1.36	1.36

For the thicker films, it was anticipated that longer annealing times post CdTe deposition may be required, given that the annealing time had to be optimised when 100 nm CdSe layers were utilised. Table 5.4 shows the peak and average performance parameters for SnO_2/CdSe/CdTe devices when a 200 nm CdSe layer is incorporated and post CdTe growth annealing time was varied from 20 mins to 60 mins. Figure 5.35a and b shows the *JV* and EQE responses for the highest efficiency contacts these devices.

It can be seen that by increasing the device annealing time, device J_{SC} and EQE response at short wavelength can be significantly improved. This is probably due to a reduction of the residual CdSe layer. However, the performance of these devices still remained significantly lower than an equivalent device with a peak efficiency of 9.9% and 13.5%, for the 200 nm and 100 nm CdSe layers respectively with losses due to a lower J_{SC} and *FF*. The assumption is that a residual CdSe layer is still present even after a 40 mins treatment. The performance drops slightly when the devices were annealed for 60 mins, 9.89% to 9.36% for 40 mins and 60 mins. However, the J_{SC} did improve slightly, from 24.51 mA cm^{-2} to 25.33

mA cm^{-2} for the 40 mins and 60 mins devices respectively, which again indicates that there has been a further reduction to the residual CdSe layer, shown by the enhanced device EQE response (Figure 5.36b). The reduced performance for 60 mins annealed device is primarily driven by losses to V_{OC} and *FF* which is an indication the device processing has become too intensive and the devices are now over treated.

The results for the 200 nm CdSe layer devices supports the suggestion that annealing the films post CdTe deposition is converting the photoinactive CdSe phase to the photoactive $CdTe_{(1-X)}Se_X$ phase via Se diffusion i.e. a thicker CdSe layer requires a longer annealing step to achieve full conversion to the $CdTe_{(1-X)}Se_X$. The data presented in Figures 5.35 and 5.36 would also seem to suggest that under these conditions there is a limit to amount of CdSe that can effectively be incorporated into the CdTe films as no bandgap shift has been observed in the device EQE response despite the enhanced annealing times. By varying the post growth annealing times, this limit can be increased to a point before device performance ultimately starts to become affected. This demonstrates that the CdSe thickness has to be optimised in tandem with the post annealing step, otherwise an optimal performance cannot be achieved.

Table 5.4: *Peak and average ± (in brackets) SD device parameters as a function of post growth annealing time at 610 °C for CdSe/CdTe cells with a 200 nm CdSe layer.*

Annealing times	**η (%)**	**J_{SC} (mA cm^{-2})**	**V_{OC} (V)**	***FF* (%)**
20	7.95 (7.13±0.46)	18.55 (16.98±0.71)	0.71 (0.70±0.01)	59.64 (60.40±1.45)
40	9.89 (9.43±0.10)	24.51 (22.82±0.73)	0.72 (0.72±0.01)	56.02 (57.46±1.78)
60	9.36 (8.27±0.22)	25.33 (23.09±0.33)	0.69 (0.67±0.01)	53.51 (53.06±0.70)

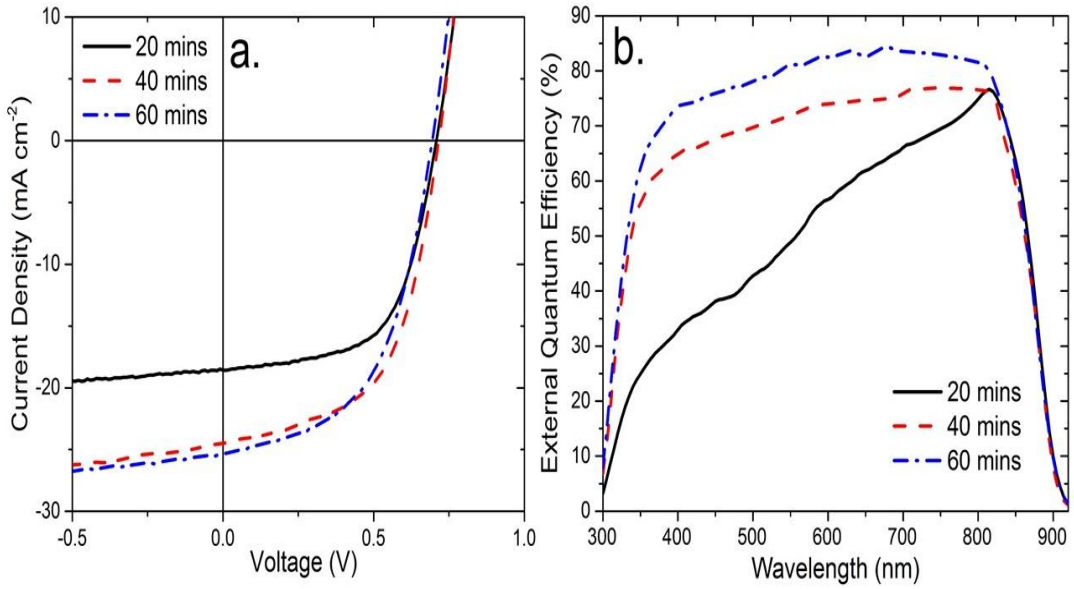

Figure 5.36: *a) JV and b) EQE data for highest efficiency contacts from cells produced using different post growth anneal times at 610°C on SnO_2/CdSe (200nm)/CdTe based devices. Cells had a 5 nm Cu layer at the back contact.*

5.4.2.6. Se and Te diffusion analysis in post growth annealed SnO_2/CdSe/CdTe devices

To assess the role the post CdTe growth annealing is having on the elemental distribution we used SIMS analysis for a series of devices with a 100 nm CdSe layer which were annealed for various times. Figure 5.37a and b shows the normalised Se and Te spectra for the 0 mins, 20 mins and 40 mins post growth annealed devices. The Se and Te signals were normalised with respect to 1 and the sample thickness was also normalised to 1, with 1 representing the back surface and 0 representing the front SnO_2 device interface so a direct comparison could be made.

The addition of the annealing stage induced some additional Se diffusion into the CdTe layer. All samples show a high Se content at the near interface region, but the 20 mins and 40 mins anneals show a higher Se content throughout the CdTe layer. The 40 mins sample also shows a more uniform distribution than the 20 mins anneal. However, there is little suggestion of Se grading despite the longer annealing times. In the ideal scenario, the Se will be graded with higher content at the near interface, thus a lower bandgap, with a decreasing Se content towards the back surface. Instead we see high Se content at the near

interface then a reasonably linear content in the bulk[8]. This agrees with the EDX data shown in Figure 5.28 where a high Se content was observed at the front device interface. Again, it should be noted that sharp increases observed at the back surface are an artefact of the measurement, due to a change in the ion yield in the pre-equilibrium region during the early stages of the sputtering process.

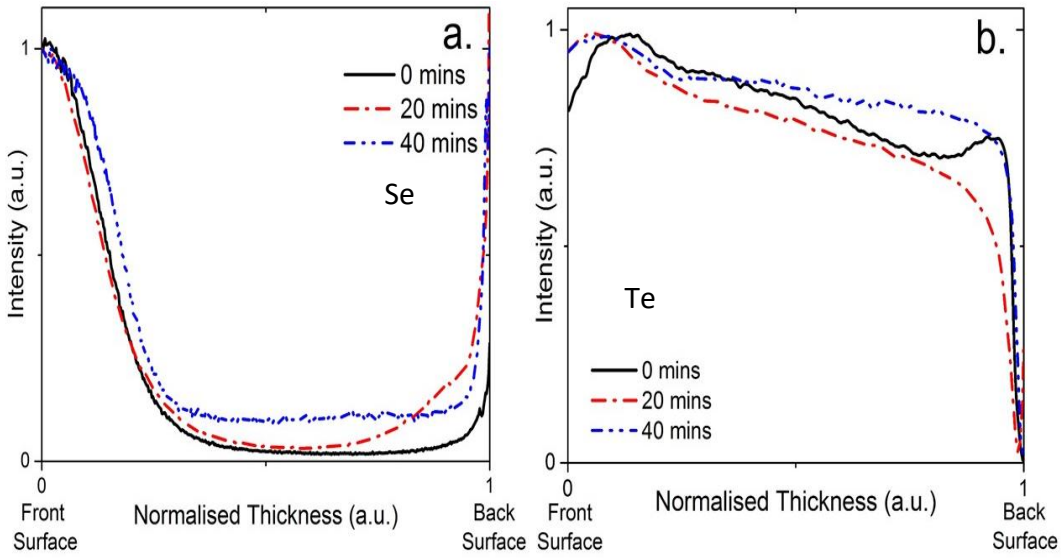

Figure 5.37: *Secondary ion mass spectrometry (SIMS) data showing (a) Se and (b) Te distribution through the sample as a function of annealing time. Sample thickness has been normalised with 0 representing the front SnO_2 interface and 1 representing the back surface. Counts have been normalised to 1 with respect to the Se content at the SnO_2 interface to allow direct comparison between the profiles.*

The Te distribution shown in Figure 5.37b demonstrates that post CdTe growth annealing the devices has some influence on Te diffusion, particularly at the $SnO_2/CdTe_{(1-X)}Se_X$ interface. The Te content at the $SnO_2/CdTe_{(1-X)}Se_X$ interface of the device is lower for the unannealed devices when compared to the 20 mins and 40 mins annealed samples, the Te distribution at the SnO_2 interface for 20 mins and 40 mins is relatively similar indicating again that the post growth annealing is having an impact on the Te diffusion in the sample. The SIMS data presented indicate that there is some Se diffusion into the CdTe, but a high Se content at the interface and that Te is diffusing into the CdSe layer forming the $CdTe_{(1-X)}Se_X$ phase.

From the data presented, it is evident that post-growth annealing may alter both the Se and Te content in the CdTe/$CdTe_{(1-X)}Se_X$ phase. In order to achieve an ideally graded bandgap though, some greater refinement in control of the Se diffusion may be required or else a more ideal way of incorporating the Se needs to be explored, e.g. co-sublimation to form $CdTe_{(1-X)}Se_X$ layers, as has been demonstrated by others[21,36].

5.4.2.7. Comparison between CdS/CdTe and SnO_2/CdSe/CdTe devices

It is clear from the data presented in this chapter that SnO_2/CdSe based CdTe devices can act as a viable alternative to the conventional SnO_2/CdS based devices. It is worth making a comparative assessment with the performance achieved from a conventional CdS/CdTe junction. Table 5.5 shows the peak and average performance parameters for comparative devices from the developed SnO_2/CdSe/CdTe structure with a standard SnO_2/CdS (100 nm)/CdTe devices. *JV* and EQE curves for the highest efficiency contacts are shown in Figure 5.38a and b respectively. For comparative purposes, the CdS based devices also underwent a 20 mins in-situ post CdTe growth anneal and a 5 nm Cu layer has been added to the back surface in both devices. The peak performance of both devices is similar being 13.5% for the CdSe device and 14.0% for the CdS. The CdSe based device showed a very high J_{SC} of 29.6 mA cm^{-2}, with primary losses associated with reflection from the glass substrate and TCO, compared to 25.6 mA cm^{-2} when CdS was used. From the EQE it was clear where the additional photocurrent arose from with enhanced response at both the short and long wavelength regions due to in the CdS layer being removed and the formation of the lower bandgap $CdTe_{(1-X)}Se_X$ phase extending collection at long wavelength.

The devices with CdSe have a significantly lower V_{OC} of 0.72 V compared to 0.82 V for CdS based devices, whilst the CdS based devices also have a marginally higher *FF*. The loss in V_{OC} could be due to a number of reasons: a) for the CdSe based device, the bandgap of the absorber layer $CdTe_{(1-X)}Se_X$ has been lowered (≈ 1.38 eV from EQE estimation) which in turn means the maximum attainable V_{OC} has been reduced, as both CdSe and CdS

structures show a similar voltage deficiency relative to their bandgap (52.8% and 54.6% respectively[31,32]); b) the SnO_2/$CdTe_{(1-x)}Se_x$ interface is of a lower quality due to poor energy band alignment between the SnO_2 and $CdTe_{(1-x)}Se_x$ layers which results in a high interfacial recombination rate and thus a reduced V_{OC}[31] or ; c) the switch to a SnO_2 and $CdTe_{(1-x)}Se_x$ interface has enhanced the lattice mismatch, resulting in an increased defect density and strain at the interface which will limit device V_{OC}.

Table 5.5: *Peak and average ± SD device parameters (in brackets) for cells using SnO_2/CdSe (100 nm) and SnO_2/CdS (100 nm) with a 5 nm Cu layer at the back contact and a 20 min in-situ post growth anneal at 610 °C.*

Window Layer	η (%)	J_{SC} (mA cm^{-2})	V_{OC} (V)	*FF* (%)
SnO_2/CdSe	13.5 (11.3±0.8)	29.6 (29.5±0.8)	0.72 (0.69±0.01)	63.3 (54.9±2.6)
SnO_2/CdS	14.0 (13.1±0.2)	25.6 (24.4±0.4)	0.82 (0.81±0.01)	66.4 (66.5±0.9)

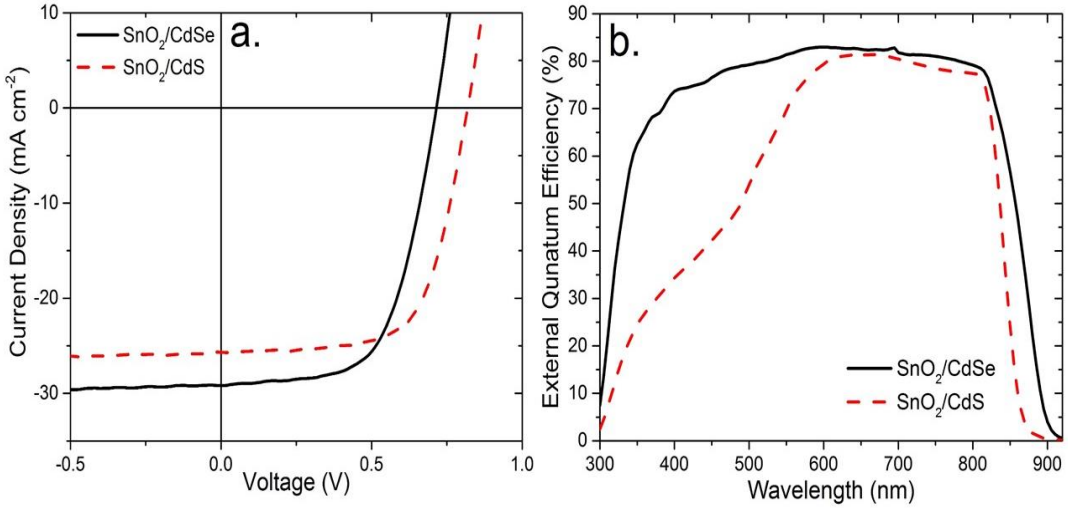

Figure 5.38: *a) JV and b) EQE data for highest efficiency contacts from cells using SnO_2/CdSe (100 nm) or SnO_2/CdS (100 nm) as the device window layers with a 5 nm Cu layer at the back contact and a 20 min in-situ post growth anneal at 610 °C.*

5.4.3. Discussion

In this section SnO_2/CdSe/CdTe devices were investigated. It was found that removal of CdS from device structure led to the gains in device photocurrent due to a significant improvement to device response at short wavelength. This verified the earlier findings that

the CdS layer and specifically the formation of a $CdS_{(1-X)}Se_X$ phase, is detrimental to CdSe incorporation in CdS/CdTe based devices. Without the CdS layer, EDX and SIMS analysis was used to show that Se was able to diffuse much further into the CdTe layer and Te was also shown to diffuse into the CdSe layer during CdTe deposition forming the desired $CdTe_{(1-X)}Se_X$ phase. EBIC analysis was performed to show that the formation of the $CdTe_{(1-X)}Se_X$ phase and removal of CdS led to the creation of a more conventional p-n junction position, resulting in an improved performance with over 13% being achieved for CdS free devices. The data presented in this section confirm that when CdSe is used in conjunction with a CdS layer, it is detrimental to device performance, under these processing conditions.

It was also shown that the Se and Te diffusion could be controlled to an extent by in-situ post CdTe growth annealing. This annealing led to the partial conversion of CdSe from the photoinactive wurzite phase to what is presumed to be the photoactive $CdTe_{(1-X)}Se_X$ phase. This annealing step resulted in a dramatic improvement to device performance due to a shift in junction position and a reduction in parasitic absorption shown in the EBIC and EQE data.

However, it was also found that SnO_2/CdSe/CdTe devices still had a number of issues that require further investigation. SIMS and EDS analysis showed little evidence of a graded Se content, implying a graded bandgap structure was not achieved. In addition to this, SEM and TEM images also showed the presence of large voids at the interface possibly due to excessive CdSe and CdTe intermixing. This suggests that; i) further optimisation of the device processing to control Se distribution is required and ii) that the use of a sputtered CdSe may not be the ideal way to incorporate Se in the CdTe layer. An alternative approach to Se incorporation may be required such as using a co-sublimated $CdTe_{(1-X)}Se_X$ layer.

Direct comparison between SnO_2/CdSe/CdTe and CdS/CdTe devices showed that the CdSe based devices had higher photocurrents. However, the device V_{OC} and *FF* were

reduced, suggestive of an inferior interface due to a poor band alignment or the reduced bandgap has resulted in a reduction to the built in field and therefore the V_{bi}.

5.5. Alternatives to SnO_2 as the device window layer

A potential route to improving cell efficiency will likely come from improving the device front interface by replacing the SnO_2 window layer with feasible alternatives. This section will report on efforts to try and improve the voltage produced by $CdTe_{(1-X)}Se_X$ based devices by replacing the device n-type window layer SnO_2 with a number of different alternatives. By replacing the window layer, a more suitable band alignment may be found leading to an improved device V_{OC}. The layers that will be compared are 100 nm SnO_2, FTO (i.e. no SnO_2 layer), 100 nm ZnO, 50 nm TiO_2 and thin (15 nm) CdS. 100 nm ZnO was chosen as we have previously demonstrated it to be the highest performance for CdTe devices and 50 nm TiO_2 was chosen as this was demonstrated to be the highest performing for our perovskite solar cells.

By replacing the n-type window layer in the p-n structure we can investigate its influence on device performance with a focus on device V_{OC} and *FF*. The hope being that, by using different layers, an improved band alignment can be found by using an alternative to SnO_2 and device V_{OC} and *FF* will be improved as a result. The use of a thin CdS layer is to try and utilise the superior $CdS/CdTe_{(1-X)}Se_X$ interface but limit the formation of the unwanted $CdS_{(1-X)}Se_X$ phase.

5.5.1. Device fabrication

A schematic representation of the CdTe device structure used in this section is shown in Figure 5.39. The device window layers were fabricated via a variety of techniques. SnO_2 and CdS layer were deposited as described in the previous sections. 100 nm ZnO was deposited via RF sputtering using a power density of 2.19 W cm^{-2}. TiO_2 was deposited by

spin coating as described in Section 4.2.2**.** All other device processing steps were identical to those described in Section 5.3 and 5.4.

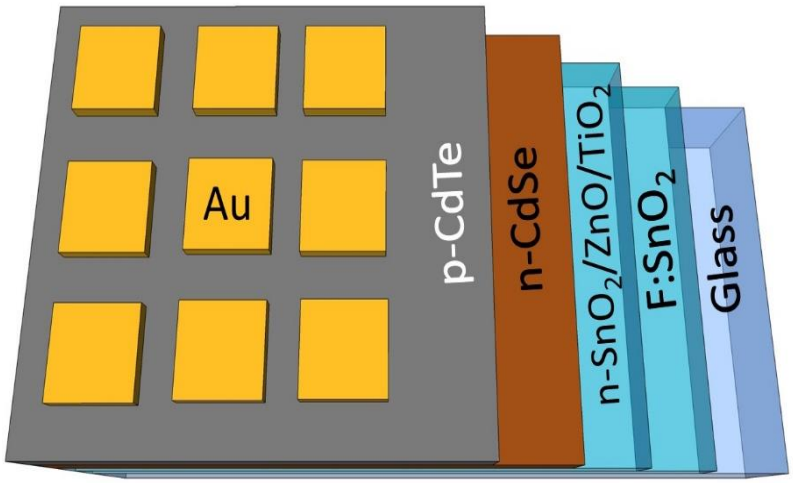

Figure 5.39: *Schematic representation of the as-deposited CdSe/CdTe device structure used in Section 5.5 utilising different window layers.*

5.5.2. Comparison of different window layer's device performance

Figure 5.39a-d shows the influence of the different window layers on the device performance parameters, including SnO_2 based devices for comparison. Figure 5.41a and b show the *JV* and EQE responses produced by the highest efficiency contacts for each cell.

Of the window layers compared in this study, SnO_2 based devices showed both the highest peak and average performance. Devices with a thin CdS layer showed a similar average performance to SnO_2 (11.98±0.47% and 11.17±0.23% respectively), although peak efficiency was slightly lower (13.51% and 11.77% respectively). Other partner layers typically showed a significantly reduced performance. The CdS based devices show an enhanced average *FF* compared to the SnO_2 devices, 63.6% and 54.9% respectively, and improved average V_{OC} from 0.73 V to 0.69 V, however peak V_{OC} values are similar. The improvement in *FF* and V_{OC} would seem to confirm that the CdS/$CdTe_{(1-X)}Se_X$ interface is of a better quality than the SnO_2/$CdTe_{(1-X)}Se_X$ interface. However, the overall performance is still reduced due to a significant reduction in device J_{SC}, via the formation of the $CdS_{(1-X)}Se_X$

layer, visible in EQE losses < 600 nm (Figure 5.41b), even at this significantly reduced CdS thicknesses.

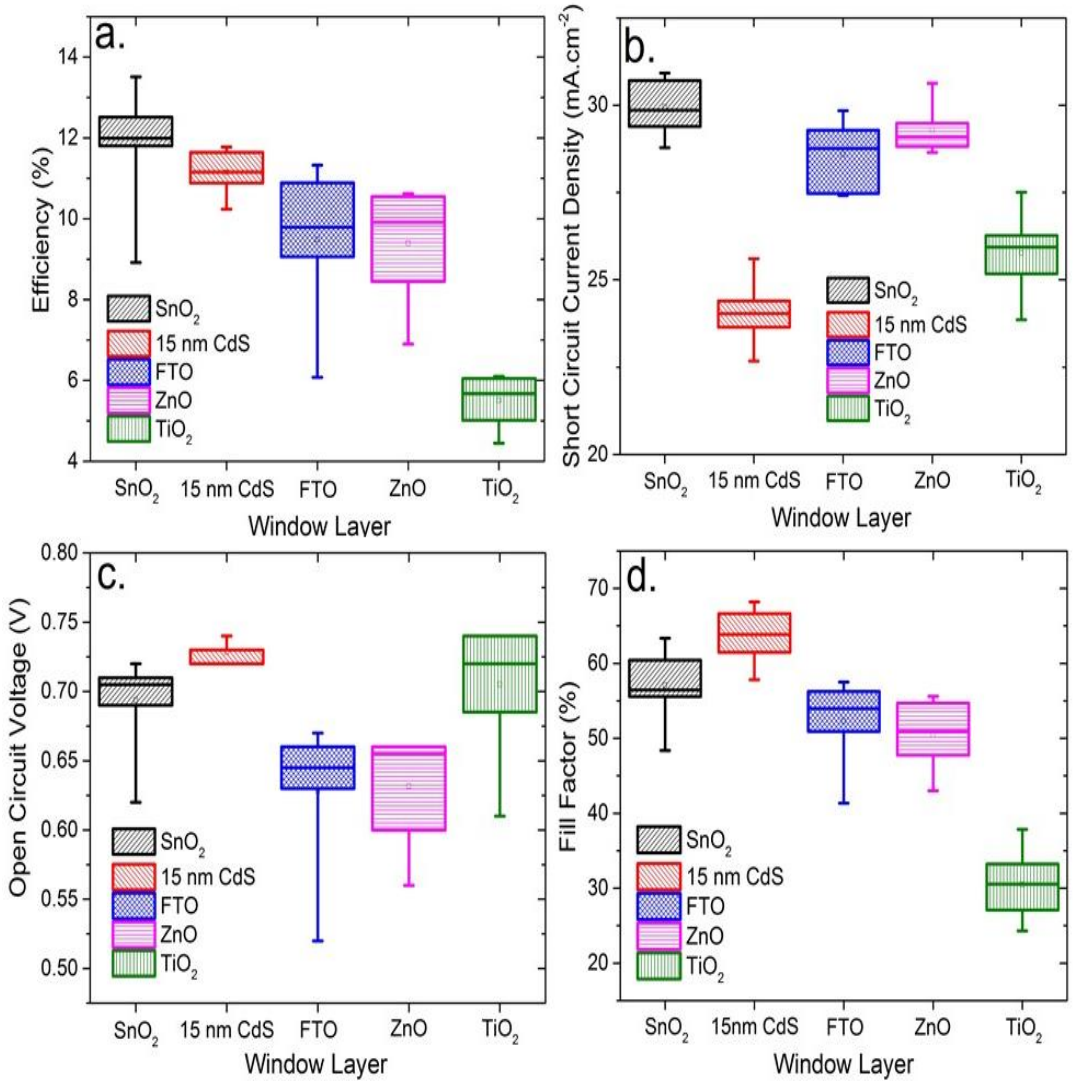

Figure 5.40: *Shows the device performance when using thin CdS (15 nm), FTO, ZnO and TiO_2 as the n-type window layer. The SnO_2 based devices are also shown for comparison. Cells were in-situ post growth annealed at 610°C for 20 mins. N=8.*

The devices which utilise FTO and ZnO as device window layers show a further reduction in performance due to a significant decrease in V_{OC} with the peak dropping from 0.72 V for the SnO_2 cells to 0.66 V for both the FTO and ZnO devices respectively. This indicates that, despite the high current that can be achieved, these layers are unsuited to $CdTe_{(1-X)}Se_X$ devices, either due to a poor quality junction, higher rate of recombination or low built in voltage. The bandgap cut-off for ZnO can also be seen in the EQE response

(Figure 5.40b) where losses occur due to ZnO bandgap in 300 - 350 nm region of the spectrum.

TiO_2 based devices show a particularly pronounced reduction in efficiency (to an average of 5.5%) due to a low *FF* with an average of 30.3%. This results from the formation of an uncharacteristic S – shaped curve in the *JV* data at forward bias. The S – shaped "kink" is not widely observed for CdTe devices but is identified as an interfacial barrier due to a misalignment of the energy bands through either an extraction or injection barrier[13]. S-shape curves are often observed in organic PV devices where a wider variety of partner layers are used compared to CdSe[12–14]. If the interfacial barrier produced is large this results in a significant reduction to device performance, due to significant charge accumulation at the interface. This leads to excessive recombination at the interface, reducing V_{OC} and *FF*. Although the S - shape is not widely observed in CdTe devices, this is due to field almost exclusively using the CdS/CdTe device structure. As the CdTe community moves away from this structure more S – shaped *JV* responses will likely appear in the literature.

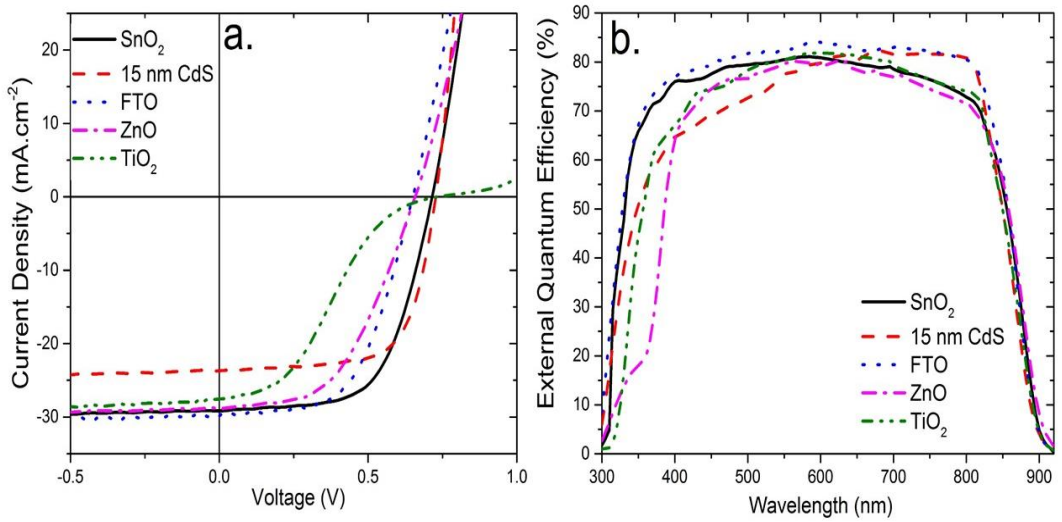

Figure 5.41: *a) JV and b) EQE response comparison for the highest efficiency contacts using ultrathin CdS, FTO, ZnO and TiO_2 as the window layer in CdSe/CdTe photovoltaics. Cell were in-situ post growth annealed at 610 °C for 20 min.*

5.5.3. Discussion

The comparative device results presented in this section demonstrate the importance of the correct choice of partner layer for CdSe based devices. From this development work

the most suitable window structure, identified was SnO_2 coupled to 100 nm of CdSe, with an in-situ post-growth anneal of 20 min at the growth temperature (610 °C).

It has been shown that the device voltage and interface quality depends strongly on the n-type window layer stack. These results would indicate that while J_{SC} improvements are achievable, if a more ideal oxide partner layer to CdSe can be found then the device V_{OC} and thus the performance would be improved for $CdTe_{(1-X)}Se_X$ based devices and go beyond that of the conventional CdS/CdTe based devices. These improvements may be realised through varying the oxide layer deposition conditions, such as deposition temperature and film thickness or else by identifying alternative oxides[41].

5.6. Conclusion

Chapter 5 presents a study of Se incorporation and device optimisation for CdTe based PV.

Through predominately cell led work several key factors related to the incorporation of CdSe into CdTe cell structures have been identified. It has been shown that Se addition to both CdS:O/CdTe and CdS/CdTe device structure may be fundamentally limited due to enhanced optical losses, mainly at short wavelength. TEM and EBIC analysis demonstrated that these optical losses are due to Se diffusion into the CdS layer, forming a $CdS_{(1-X)}Se_X$ phase. Any absorption in this layer has been shown to be parasitic thus resulting in the reduced device J_{SC}. It was also shown via STEM/EDX analysis that intermixing of CdS/CdSe layers resulted in large voids forming at the interface which results in a further reduction to device performance.

The losses associated with the $CdS_{(1-X)}Se_X$ phase can be reduced by altering the device processing, specifically by performing a post CdTe growth in-situ anneal at 610°C. This anneal did improve the devices photo response at short wavelength to a point. However, even with this post growth anneal, incorporating any Se into the conventional CdS/CdTe

device structure was detrimental to device performance, owing to the formation of the $CdS_{(1-X)}Se_X$ phase.

Device photo response could be significantly improved by removing the CdS layer from the device structure and replacing it with SnO_2 as the n-type partner layer. This resulted in the enhancement of device photo response at both short and long wavelength, through effective Se incorporation, the formation of the lower bandgap $CdTe_{(1-X)}Se_X$ phase and removal of parasitic absorption in the CdS layer. Cross-sectional EBIC analysis showed SnO_2/CdSe based devices gave a more conventional junction position, the inference being that recombination losses at the near interface had been significantly improved. SIMS was used to map the Se distribution in the CdS/CdSe and CdSe based devices, showing that Se diffusion into the CdTe layer was enhanced when compared to equivalent CdS/CdSe devices. This data reinforced the idea that a dual window layer of CdS/CdSe is not ideal for CdTe based photovoltaics.

The role of the post growth anneal was further investigated for SnO_2/CdSe based devices, with it found to be essential for achieving a high device current. Annealing was shown to aid performance, presumably due to the conversion of residual CdSe to the photoactive $CdTe_{(1-X)}Se_X$ zincblende structure. SIMS data of the Se profile showed no evidence of effective Se grading throughout the CdTe layer despite the high performance. There also seemed a limit to the amount of Se that could be effectively incorporated into the device structure, with a 100 nm CdSe layer resulting in the highest performance. In addition to this, cross sectional SEM images still showed the presence of voids at the interface due to intermixing of the CdSe and CdTe layers. This demonstrates that alternative CdTe device processing could be required such as deposition temperature and further optimisation of this process could result in an enhancement to device efficiency. This demonstrates that intermixing of the sputtered CdSe and sublimated CdTe layers may be an inappropriate way to incorporate Se in the CdTe layer effectively and therefore

alternatives will need to be investigated, such as a co-sputtered or co-sublimated $CdTe_{(1-x)}Se_x$ layer.

Following optimisation, a SnO_2/CdSe/CdTe cell efficiency of up 13.5% was achieved, compared to 14.0% for an equivalent SnO_2/CdS/CdTe device. J_{SC} values were significantly higher for the CdSe based cell but losses occurred due to a lower V_{OC}. This is suggestive that whilst functional, the $SnO_2/CdTe_{(1-x)}Se_x$ interface is of an inferior quality to the CdS/CdTe interface. This could be due to a number of reasons such as misalignment of the energy bands or lattice mismatch between SnO_2 and $CdTe_{(1-x)}Se_x$ layers. Therefore there remains significant scope for improving the CdSe based devices which may allow for the V_{OC} to be increased while retaining the high J_{SC} values achieved. Initial investigations demonstrated that replacing the SnO_2 with other alternatives, such as TiO_2 ZnO, and FTO were unsuccessful and led to further reductions in device V_{OC}. This highlighted that the choice of an appropriate window layer partner is essential and improving this partner layer is potentially the route to overcoming the V_{OC} deficit.

Overall, this work demonstrates the feasibility of oxide/CdSe structures as a window for CdTe photovoltaics, but that significant work is required to improve the performance further. In addition to this, further work is required to establish how the Se distribution can be better controlled, whether bandgap grading can efficiently be achieved and if an optimal device partner layer can be found.

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6. Use of MZO as the window layer in $CdTe_{(1-X)}Se_X$ PV devices

Parts of this work have been published as:

T.Baines, K.Durose and J.D. Major, Co-sputtered $Mg_XZn_{(1-X)}O$ window layers for $CdTe_{(1-X)}Se_X$ solar cells, in the 45th IEEE Specialists' Photovoltaics Conference Hawaii, 2018.

6.1. Introduction

It was demonstrated in Chapter 5 that through Se incorporation and the removal of the CdS layer that the J_{SC} of CdTe based devices can be enhanced primarily due to an improved device photo response in both short and long wavelength regions. Omission of the CdS layer as the n-type window layer resulted in a reduced V_{OC} and *FF*, possibly due to the formation of an inferior $CdTe_{(1-X)}Se_X/SnO_2$ interface compared to the CdS/CdTe interface. It was also shown that replacing the SnO_2 window layer with alternatives such as ZnO and TiO_2 degraded the device performance parameters, in particular device V_{OC}, indicating that if the correct partner layer can be found device V_{OC} and performance may be enhanced[1].

As mentioned in Section 3.4.2, MZO is a promising alternative to CdS as the partner layer in CdTe PV devices[2,3]. Swanson *et al*.[3] have reported an $MZO/CdTe_{(1-X)}Se_X$ based devices with over 14% efficiency. However, the focus of this study was optimisation of the $CdTe_{(1-X)}Se_X$ phase rather than the MZO layer.

This chapter will report on optimisation of the MZO layer in $MZO/CdTe_{(1-X)}Se_X$ based devices with the aim of an improved V_{OC} compared to 0.72 V for SnO_2 based devices of the preceding chapter. In Section 6.2 MZO layers will be deposited via a co-sputtered fabrication process from MgO and ZnO targets with varied factions of Mg in the MZO films. The impact of incorporating these films into device structure will also be discussed. Section 6.3 will investigate the use of MZO layers deposited from a single sputtering target and will

demonstrate that post growth annealing of the MZO is essential to achieving optimal film properties and improved device efficiency. The performance of MZO based devices will also be compared with ZnO/$CdTe_{(1-x)}Se_x$ based devices.

6.2. Co-sputtered MZO/$CdTe_{(1-x)}Se_x$ based devices

In theory the use of MZO is attractive because, depending on the Mg content the CB position can be shifted to higher values compared to ZnO[4]. Shifting the CB allows its position to be tailored so that the optimal band alignment can be found, resulting in a higher V_{OC} and device performance. It has been demonstrated that the ideal band alignment for PV device is a small spike at the interface as this reduces the amount of recombination and enhances device V_{bi} and V_{OC} (see Section 2.2.2.3.1)[5–8].

In other work, is was shown that a ZnO/CdTe interface results in an unfavourable cliff like interface and through the addition of Mg, the resultant bandgap shift leads to a spike like MZO/CdTe interface and an improved performance[4,5]. The majority of the work carried out on MZO as a window layer for CdTe and $CdTe_{(1-x)}Se_x$ has used MZO layers produced from a single target and performances of over 19% have been achieved, with V_{OC} values greater than 860 mV[2,3]. However, in order for an optimal efficiency to be achieved, a specific Mg content needs to be utilised, a 23 atomic % weight (MgO wt/(MgO wt+ZnO wt)). The wrong composition results in losses to V_{OC} and *FF* due to poorer band alignment[2,5,9].

To date, very little work has been undertaken on how varying the Mg content in the MZO films influences $CdTe_{(1-x)}Se_x$ based device performance. In theory, as the CB is shifted to higher values, the V_{OC} and *FF* should improve to a point until an ideal spike is formed (< 0.3 eV[8]). While the V_{OC} and *FF* are expected to fall when too much Mg is used and a large barrier to transport is formed. Using co-sputtered MZO layers from ZnO and MgO targets allows for fine control of the Mg content in the films compared to the single target

approach, assuming a single-phase material can be produced and no change in doping density occurs.

In this Section co-sputtered MZO layers will be fabricated with a varied Mg content and their optical and structural analysis will be presented in Section 6.2.2. Section 6.2.3 will report on the influence these films had on the MZO/$CdTe_{(1-X)}Se_X$ device performance. It was hoped that the high J_{SC} discussed in Chapter 5 could be maintained but, by using co-sputtered MZO layers, the band alignment could be improved, resulting in an enhanced V_{OC} and device efficiency.

6.2.1. Device Fabrication

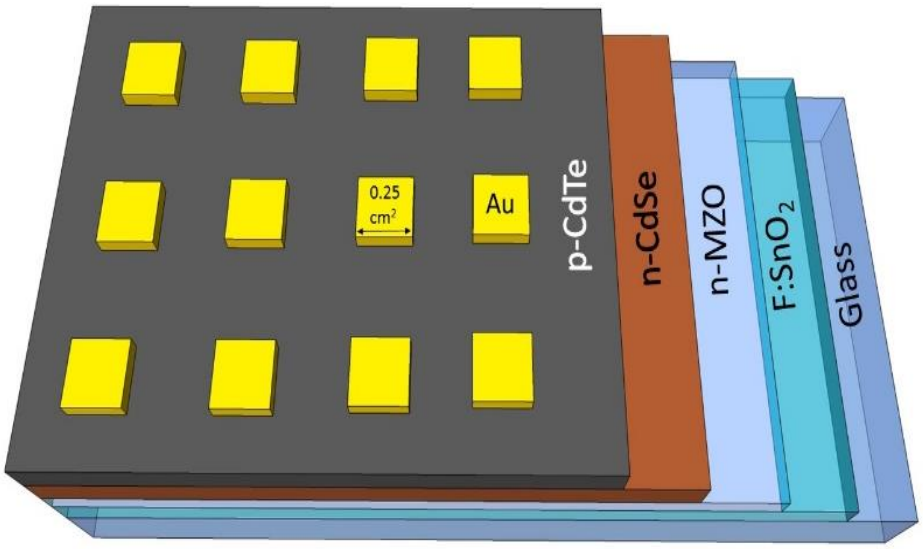

Figure 6.1: *Schematic representation of the 'as-deposited' MZO/CdSe/CdTe device structure used in Section 6.2.*

Figure 6.1 shows a schematic representation of the CdTe device structure used in this section. General device fabrication procedures can be found in the relevant experimental sections (see Chapter 4). Any unique device deposition conditions used in this section are reported here.

100 nm of MZO was deposited via co-sputtering from ZnO and MgO targets at room temperature. Films were fabricated with a varying Mg content as specified in the text. CdSe layers were deposited at RT using a power density of 1.32 W cm^{-2}.

6. Use of MZO as the window layer in $CdTe_{(1-X)}Se_X$ devices

Devices were in-situ post CdTe growth annealed at 610°C in the CSS chamber at an 'elevated' pressure of 200 Torr for 20 mins, in order to aid Se and Te diffusion as demonstrated in Chapter 5 (see Section 5.4.2.4). All samples were then $MgCl_2$ treated at 410°C for 20 mins in an air ambient[10]. A 5 nm Cu layer was also deposited via thermal evaporation at the back surface to facilitate the formation of an Ohmic contact[11].

6.2.2. Co-sputtered MZO film characterisation

Initially the influence of adding increasing amounts of Mg into MZO layers was investigated. A series of MZO layers was fabricated on SLG from ZnO and MgO targets by adjusting the ZnO and MgO targets power densities. The Mg content is calculated by Mg weight (wt) percentage (MgO wt/(MgO wt+ZnO wt)). Figure 6.2a shows the optical transmission curves for MZO films as a function of Mg content in the MZO films. The extrapolated bandgaps calculated also using the measured reflection and the Tauc method are also shown in the insert[12].

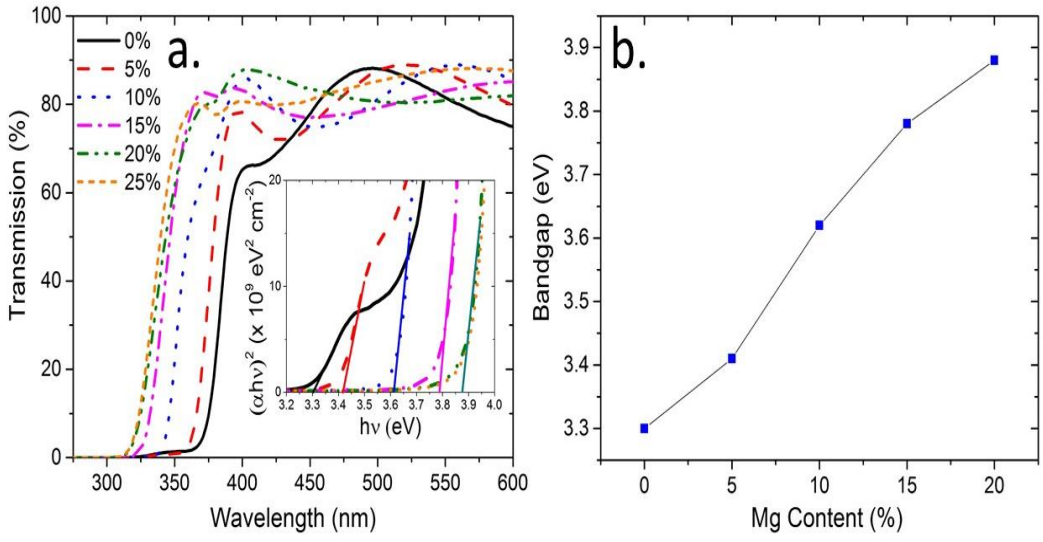

Figure 6.2: *a) Optical transmission curves and Tauc plot (insert) as a function of Mg content in the MZO films grown on SLG, b) extrapolated bandgaps as a function of Mg content.*

Increasing the Mg content in the MZO films significantly widens the bandgap compared to ZnO. The bandgap increases from 3.30 eV to over 4 eV (beyond the transmission of glass) when a 25% by wt Mg content is incorporated into the film. The bandgap also shifts

relatively linearly (Figure 6.2b) as a function of Mg content from 0% (3.30 eV), 5% (3.41 eV), 10% (3.62 eV), 15% (3.78 eV) and 20% (3.88 eV). This demonstrates that the bandgap of ZnO can be increased through the addition of Mg into the MZO films using this co-sputtered approach and that the size of the bandgap can be tailored by adding a specific quantity of Mg.

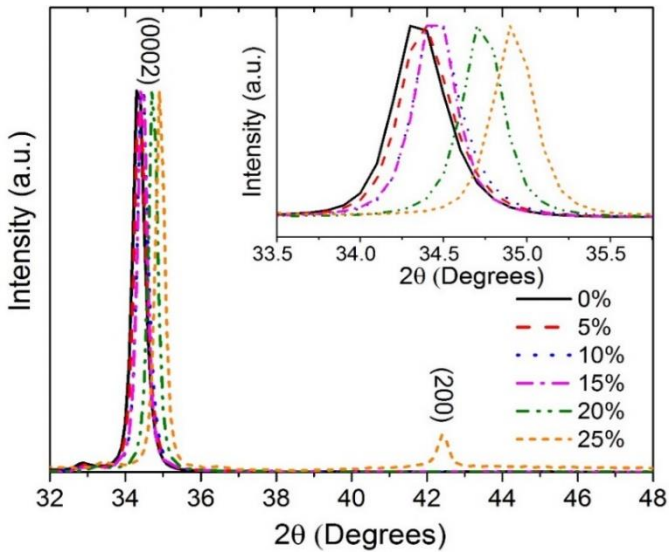

Figure 6.3: *X-Ray Diffraction (XRD) spectra for MZO films as a function of Mg content with (Inset) smaller angle range scan of the (0002) peak showing the shift in position.*

Figure 6.3 shows how the XRD spectra change with increasing Mg content in the MZO films. The ZnO film is preferentially oriented along there c-axis with only the (0002) diffraction peak being present at 34.3°[13,14], the MZO films are similarly highly orientated indicating that the hexagonal wurzite phase is maintained. The (0002) peak is however shifted to larger diffraction angles with increased Mg content up to 34.9° when 25% Mg is incorporated (see inset in Figure 6.3)[15,16]. The larger diffraction angle indicates the Mg incorporation has led to a decrease of the lattice spacing along the c-axis[16,17]. Table 6.1 shows the lattice parameters and grain size (see Section 4.3.3) of the MZO films estimated from the XRD patterns shown in Figure 6.3. It is clear that a reduction to the lattice spacing is occurring when Mg is incorporated into the films, with the lattice parameter c decreasing from 5.218 Å to 5.134 Å. The reduction indicates that MZO has a reduced unit cell size compared to ZnO. This is to be expected given that Mg has a smaller atomic radius

compared to Zn. Hence substituting a Mg atom onto a Zn site will result in a reduction in the wurtzite unit cell[18]. An increased Mg content also reduces the FWHM of the (0002) peak indicating an increased grain size[19]. The estimated grain size increased from 24.97 nm for ZnO to 33.05 nm when a 25% Mg content is incorporated in the films. Although Mg incorporation is resulting in enhanced grain growth, as the grains are still on the nano scale this is unlikely to significantly influence device performance.

Table 6.1: *2θ*, full width half maximum, lattice parameter and grain size estimated from the (0002) peak of the XRD data from Figure 6.3.

Mg content (%)	2θ (°)	FWHM (°)	c (Å)	Grain size (nm)
0	34.34	0.37	5.218	24.97
5	34.38	0.36	5.212	25.67
10	34.44	0.33	5.204	28.00
15	34.45	0.30	5.202	30.80
20	34.72	0.29	5.164	31.89
25	34.91	0.28	5.134	33.05

In addition to this, the film with a 25% Mg content display an additional peak in the spectra at 42.4°. This peak matches the (200) diffraction peak for the rock salt MgO structure[20] and would indicate that due to excessive Mg being incorporated either phase segregation is occurring and regions of ZnO and MgO are forming.

6.2.3. Effect of Mg content in MZO films on MZO/$CdTe_{(1-X)}Se_X$ devices

Following initial optimisation of the MZO layers, a series of MZO/$CdTe_{(1-X)}Se_X$ based devices was fabricated with between 0% and 25% by wt Mg content (defined by the sputtering rate) in the MZO films. Figure 6.4a-d shows the MZO/$CdTe_{(1-X)}Se_X$ device performance parameters, with the accompanying *JV* and EQE for the highest efficiency contacts shown in Figure 6.5a and b. Device EQE spectra for the 20% MZO devices are not shown as they exhibited a low response being dominated by noise, particularly when the measurement switched between the halogen and xenon lamps (700 nm).

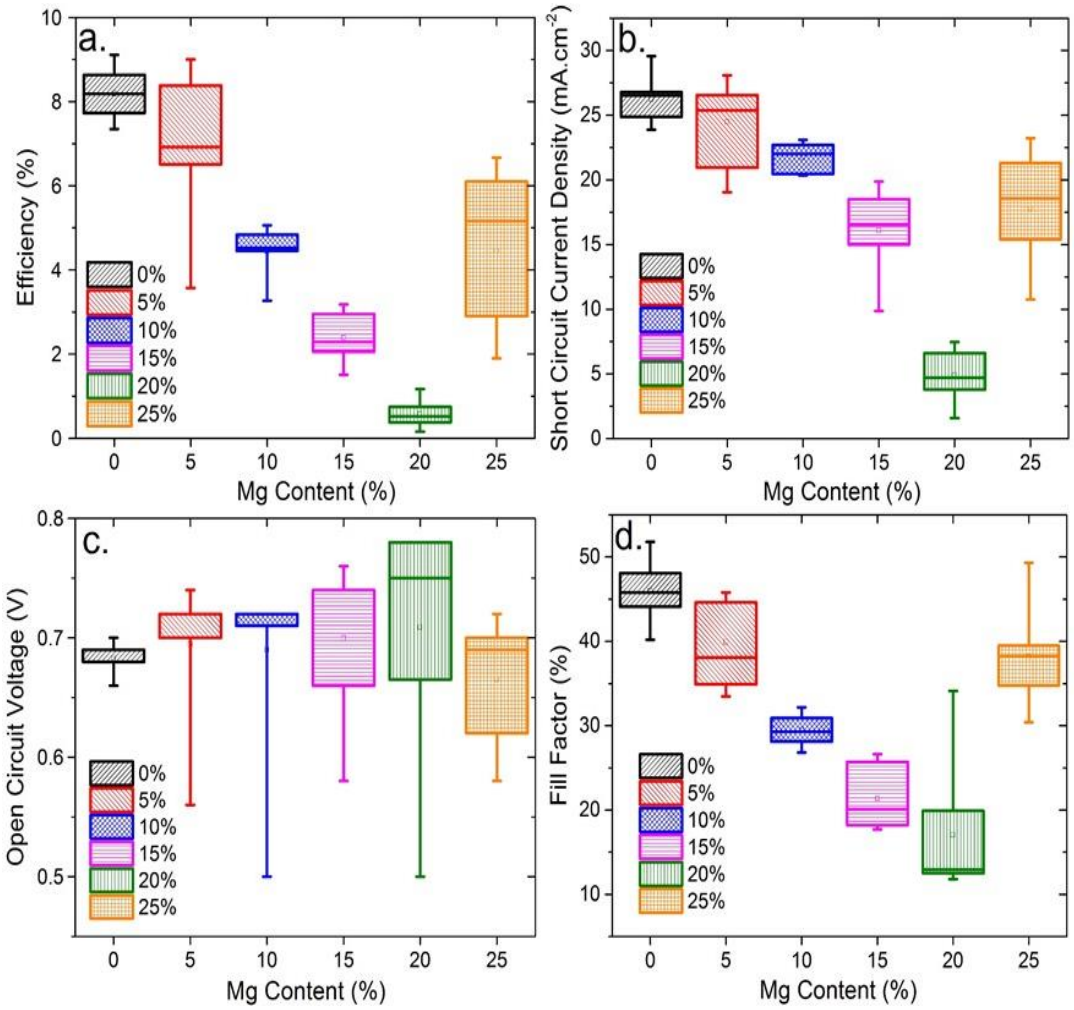

Figure 6.4: *MZO/$CdTe_{(1-X)}Se_X$ device performance parameters as a function of Mg content in the MZO films, a) η, b) J_{SC}, c) V_{OC} and d) FF. N = 9.*

From the data presented, increasing the Mg content has had a detrimental effect on device performance, with peak performance dropping from 9.11% for ZnO (i.e. Mg free) to

0.72% when a 20% Mg content was incorporated. The parameters most affected were J_{SC} and *FF* which dropped from 26.82 mA cm^{-2} to 7.48 mA cm^{-2} and 48.90% to 12.40% respectively.

The reduction to J_{SC} and *FF* is largely driven by the increased R_S and the formation of an S-shaped *JV* curve for a Mg content of greater than 5%. Figure 6.6 shows the effect of increasing the Mg content in the MZO film is having on device R_S. The average R_s increases from 10.8 Ω cm^{-2} to 2489.8 Ω cm^{-2} when 0% and 25% Mg content is utilised. This increase is accompanied by the formation of the S-shaped curves. This could be due to a poor band alignment at the interface or it could be an indication that the introduction of Mg into the MZO films increased the resistivity, reduced the mobility and therefore results in an increased device resistance. It should be noted that Hall effect and four-point probe measurements were attempted in order measure the films' resistivity and carrier concentration directly. However, all the films were too resistive to allow for accurate measurement.

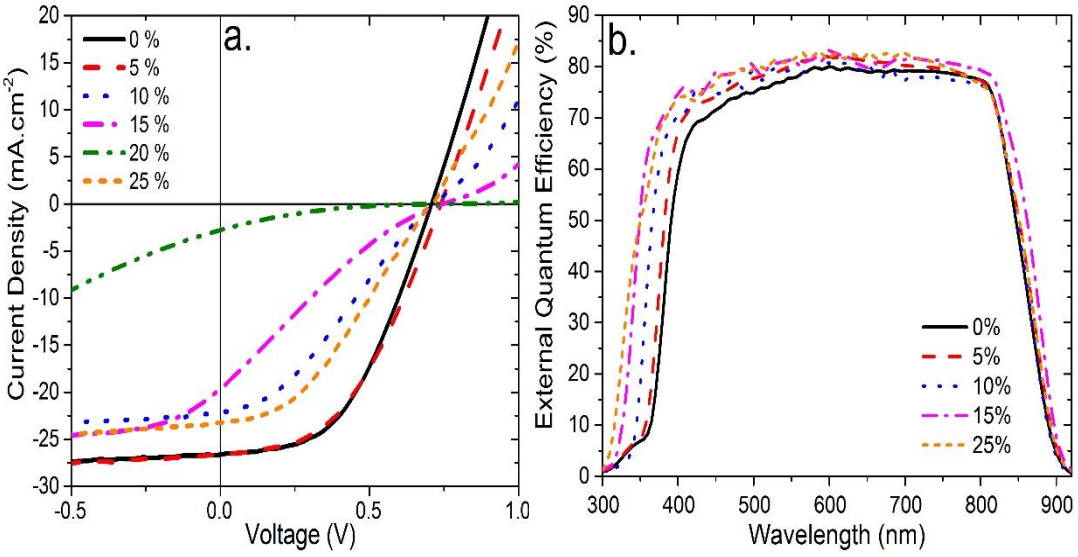

Figure 6.5: *a) JV and b) EQE responses for the highest efficiency MZO/$CdTe_{(1-X)}Se_X$ devices where the Mg content has been varied from 0% to 25%.*

The formation of an S-shaped *JV* curve with Mg incorporation is an indication that a barrier to the extraction of photo generated carriers has occurred at the MZO interface,

resulting in the reduced J_{SC} and *FF*[21]. The creation of this extraction barrier could be due to a number of reasons, such as 1) the increased bandgap for higher Mg content and potential CB shift resulting in a misalignment of the MZO and $CdTe_{(1-X)}Se_X$ bands has formed a large spike and conduction band offset limiting carrier extraction[22] or that 2) the Mg content in the films has increased the resistivity and decreased the mobility[23]. Both of these effects would result in charge accumulation at the interface, increasing the amount of recombination and limiting carrier extraction.

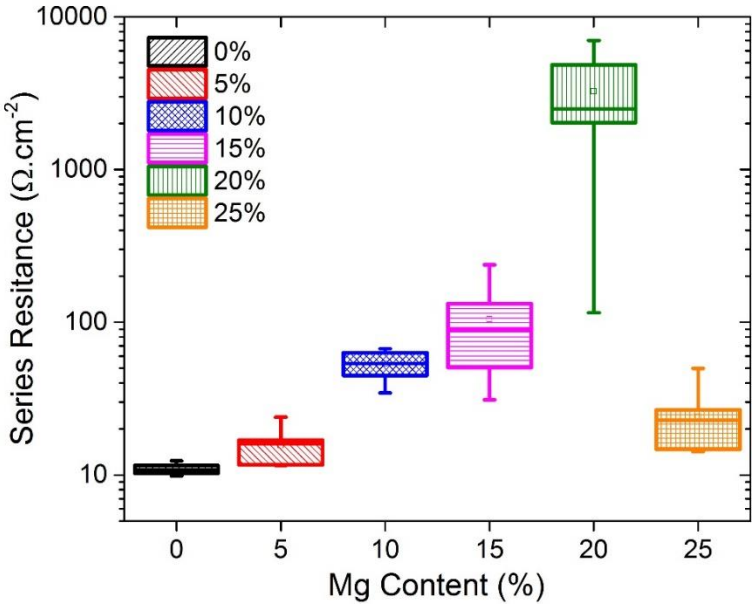

Figure 6.6: *Effect of increasing Mg content in the MZO films has on MZO/* $CdTe_{(1-X)}Se_X$ *device* R_s*. N=9.*

Although the device performance does drop, peak V_{OC} significantly increases from 0.70 V to 0.78 V when a 20% Mg content is incorporated. The increase in V_{OC} would seem to indicate that widening the bandgap of the ZnO by incorporating Mg into the films results in a more favourable conduction band offset and improved V_{bi}. If the MZO CB position is shifted to higher values with increased Mg content, this may result in a slight spike being formed rather than a cliff which would increase the V_{OC}[5]. However, as the size of the spike increases with increasing Mg content the carriers can no longer overcome the barrier leading to accumulation at the interface, consistent with the reduced current and S-shaped curve in the devices with a higher Mg content.

Additionally, while the EQE curves (Figure 6.5b) show an enhanced response at short wavelength with increasing Mg content demonstrating the increased bandgap of the window layer, they do not match well with extracted J_{SC} values. From integration of the EQE curves, we would in fact anticipate a larger current for the higher Mg content. This demonstrates there was an issue with carrier extraction under higher illumination such as in *JV* measurements, supportive of charge accumulation issues. As the EQE measurement is carried out under lower intensity illumination, compared to *JV* measurements, charge accumulation at the interface is less of an issue and therefore, a higher response is observed. When the EQE measurements were carried out under higher illumination, a much lower response was observed, possibly due to accumulation at the interface. However, data was noisy so not included.

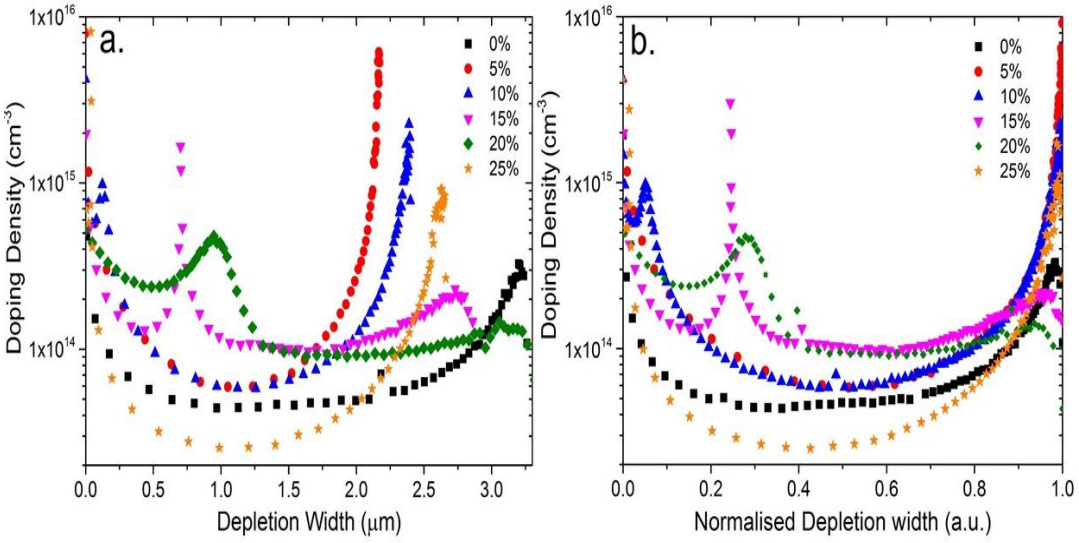

Figure 6.7: *a) Doping density versus depletion width and b) normalised depletion width profiles determined from CV measurements for MZO/* $CdTe_{(1-X)}Se_X$ *based devices with varying amounts of Mg in the MZO films. Where 0 represents the MZO/*$CdTe_{(1-X)}Se_X$ *interface and 1 represents end of the depletion width.*

The device performance does show an improvement when 25% Mg is incorporated into the films, the S-shaped curve is no longer apparent, and R_S is significantly reduced. This may be linked to XRD observation that, due to the high Mg content, phase segregation has

occurred, forming regions of ZnO and MgO compared to other Mg content levels. The device improvement may be due to regions on ZnO/$CdTe_{(1-X)}Se_X$ forming.

In order to evaluate the electrical properties of the MZO/$CdTe_{(1-X)}Se_X$ based devices *CV* measurements were performed, where the $CdTe_{(1-X)}Se_X$ layers doping density and depletion width could be calculated from the CV measurements and the p-n junction capacitance using the equations shown in Section 2.3[24,25]. Figure 6.7a and b shows the doping density versus depletion width profiles and the normalised doping density – depth profiles where 0 represents the MZO/$CdTe_{(1-X)}Se_X$ interface and 1 represents the end of the depletion region, for the same MZO device series.

The doping densities estimated from the Mott-Schottky plots varied from 2.54×10^{13} cm^{-3} to 1.07×10^{14} cm^{-3}, with no discernible trend related to the Mg content. The depth- density profiles show that the 0%, 5% and 25% Mg content MZO/$CdTe_{(1-X)}Se_X$ based devices show a typical U–shape expected for CdTe based solar cells, see Section 2.3[25]. However, the 10%, 15% and 20% MZO based devices show a spike and an apparent N_A increase at various points in the depth density profiles demonstrating a "W-shape". These same cells displayed S-shaped *JV* curves and as with the S-shaped curve, the apparent increase in N_A is attributable to a capacitance effect due to either an energy barrier or an increased MZO resistivity. Charge accumulation occurs at the MZO/$CdTe_{(1-X)}Se_X$ interface similar to that which occurs for a non-Ohmic back contact. The increase in the observed doping level is considered to be capacitance effect rather than a physical increase in the doping level, introducing an additional carrier transport barrier and a W-shaped *CV* response[25,26].

This again emphasises that a significant barrier to carrier collection was formed at the interface, leading to the reduced performance, possibly due to the increased resistivity of the MZO films. One potential route to increase the performance of MZO/$CdTe_{(1-X)}Se_X$ based devices and retain the enhanced V_{OC} reported in the literature was to increase the conductivity or reduce the thickness of the MZO films[23].

6.2.4. Influence of deposition temperature on MZO layers and device performance

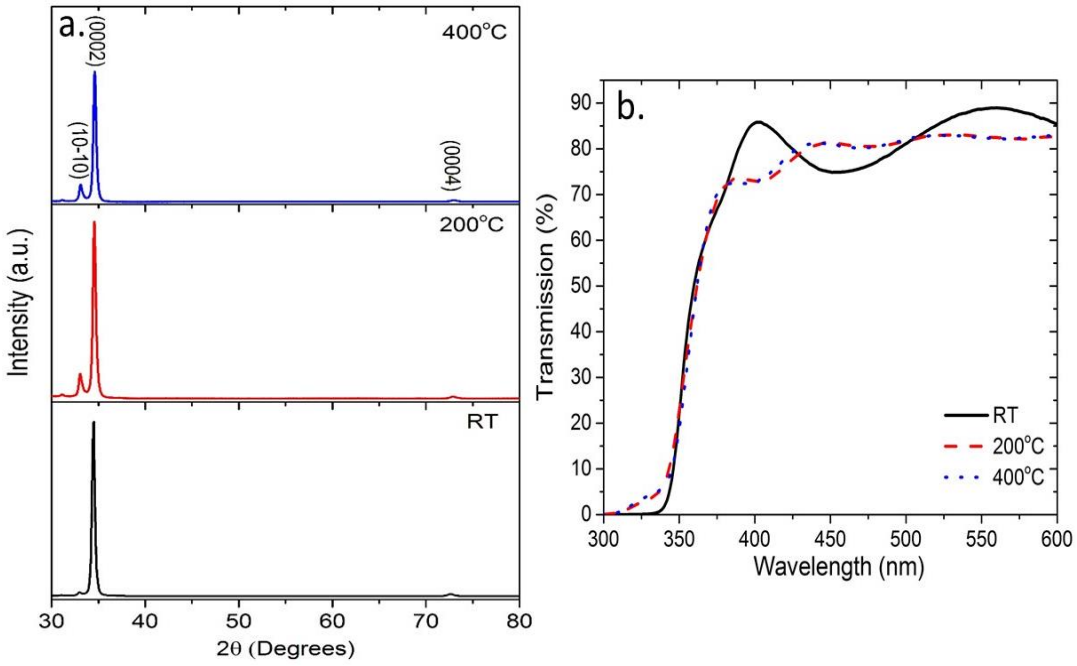

Figure 6.8: *a) XRD pattern and b) optical transmission spectra for 10% MZO films grown at RT, 200°C and 400°C.*

In Section 6.2.3 it was postulated that the S-shaped curves observed, and loss in performance, was due to the resistivity of the MZO films. It has been shown in previous work that increasing deposition temperature can improve the conductivity of thin film materials when compared to those deposited at RT, such as ZnO and MZO[27,28].

In Section 6.2.3 the MZO films produced were all deposited at RT. Therefore, the deposition temperature for the MZO layers was increased with the aim of improving device performance. For optimisation of the temperature, a 100 nm 10% by wt Mg content co-sputtered MZO films was used, as in literature this has been suggested as the optimal Mg composition as it produces the best band alignment to CdTe[2,5]. Figure 6.8a and b show XRD patterns and UV/Vis spectra demonstrating the influence of deposition temperature is having on the structural and optical properties of the MZO films.

From the XRD pattern (Figure 6.8a), increasing the deposition temperature had very little influence on the crystal structure, with preferential growth along the c-axis and still being observed. The only major difference between the patterns is the degree to which preferential orientation occurs with the 200°C and 400°C films showing reduced (0002) preferred orientation and the rise of the (10-10) peak with increasing deposition temperature.

From UV/Vis spectra (Figure 6.8b) it is also clear that increasing MZO deposition temperature similarly had little influence on the bandgap with no shift being (3.62 eV), the films deposited at a higher temperature have less interference fringes indicating the optical properties may have changed, such as the refractive index. It has been previously reported that increasing deposition temperature during MZO fabrication increased the Mg content in the films. However, for the co-sputtered approach this does not appear to be the case[29].

A series of devices were fabricated with MZO deposition temperatures of RT, 200°C and 400°C. All other device parameters were kept identical. The influence of MZO deposition temperature on MZO/$CdTe_{(1-X)}Se_X$ device performance was then evaluated with Figure 6.9a-d showing the device performance variation, with the *JV* and EQE responses for the highest efficiency contacts being shown in Figure 6.10a and b respectively.

Peak performance improved with increasing deposition temperature from 5.06% at RT to 6.57% and 8.61% at 200°C and 400°C respectively. From the device performance parameters, the increase is due to large increases in device *FF*, whist the peak J_{SC} and V_{OC} are relatively unaffected for the RT and 400°C devices. The increase to the *FF* is largely driven by the removal of the S-shape from the *JV* curve (Figure 6.10a) and the resulting reduction to the R_S which falls from 53.7 Ω cm^{-2} to 12.2 Ω cm^{-2} when RT and 400°C deposition conditions were utilised (Figure 6.11). The EQE response (Figure 6.10b) was

largely unchanged by the increased MZO deposition temperature, but this was to be expected given the minimal changes observed with Mg content.

***Figure 6.9**: MZO/$CdTe_{(1-X)}Se_X$ device performance parameters as a function of MZO deposition temperature, a) η, b) J_{SC}, c) V_{OC} and d) FF. N = 9.*

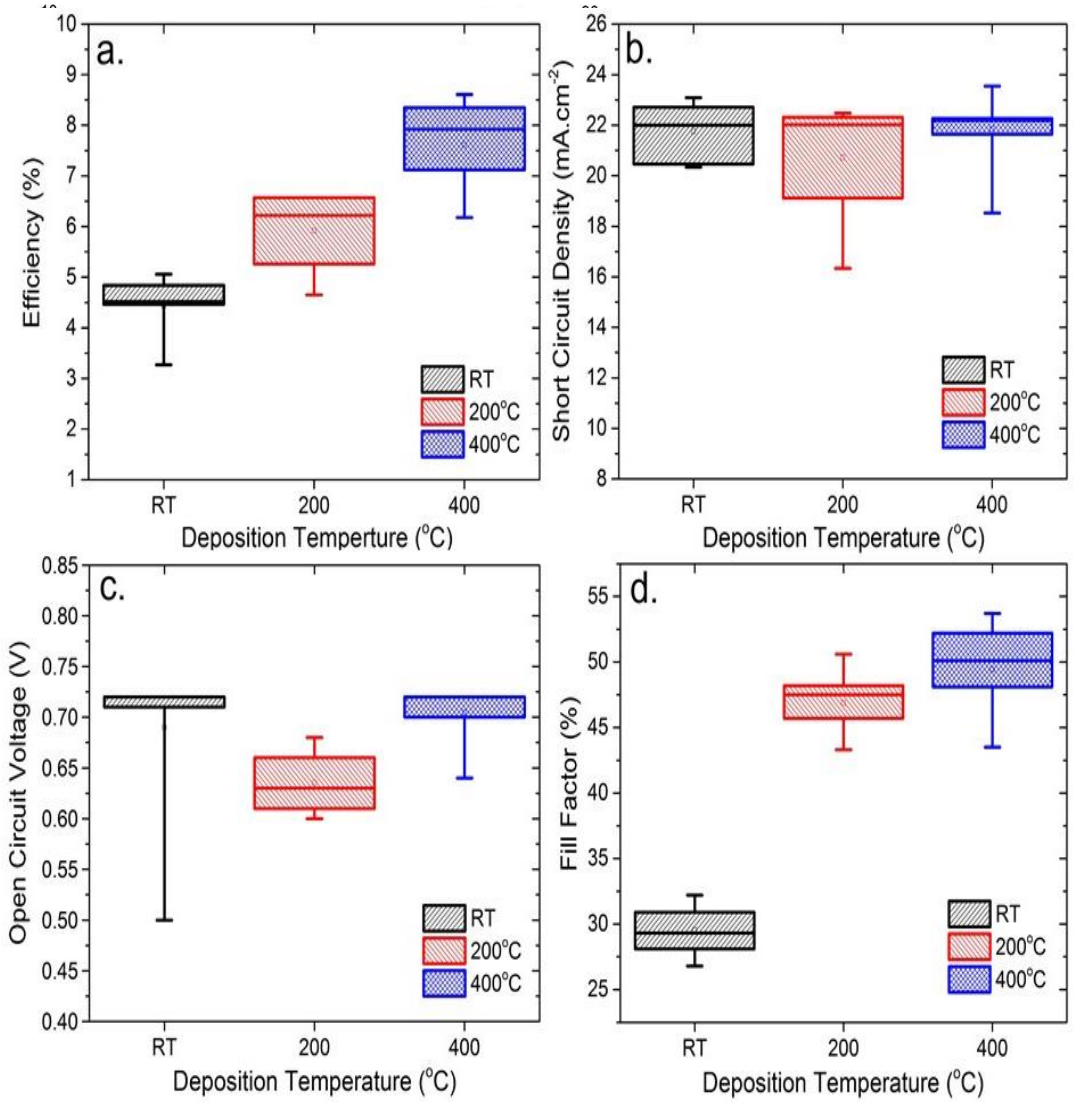

***Figure 6.10:** a) JV and b) EQE response for the highest efficiency MZO/$CdTe_{(1-X)}Se_X$ based devices as a function of MZO deposition temperature.*

The influence MZO deposition temperature is having on the CV behaviour was also evaluated. The normalised depletion width – doping density profiles for the RT and 400°C MZO/$CdTe_{(1-X)}Se_X$ devices are shown in Figure 6.12, where 0 represents the MZO/$CdTe_{(1-X)}Se_X$ interface and 1 represents the end of the depletion region. The depletion widths were normalised so that a direct comparison could be made. It can be seen that the increased

MZO deposition temperature has removed the spike in the profile and the apparent doping density increase, as the doping density – depletion width profile for the 400°C device demonstrates the characteristic CdTe U-shape[25]. The removal of this spike and the S-shaped *JV* curve is an indication that the energy barrier at the MZO/$CdTe_{(1-X)}Se_X$ interface has been reduced or that the generated photo carriers have found a way to overcome the energy barrier possibly due to the increased conductivity and increased mobility of the MZO films following annealing.

As the bandgap of the MZO layer had not changed, it seems unlikely that the band alignment between the MZO and $CdTe_{(1-X)}Se_X$ layers had changed significantly with temperature. Instead the increased deposition temperature and increase in conductivity of the MZO layer is likely to have resulted in the increased device performance. It should be mentioned that MZO films were still too resistive for Hall effect measurements to be undertaken for a direct assessment of the conductivity.

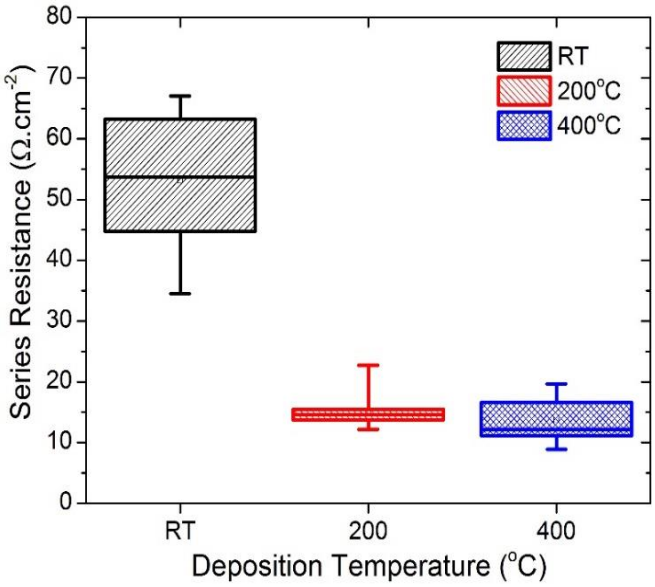

Figure 6.11: *R_S for the MZO/$CdTe_{(1-X)}Se_X$ devices as a function of MZO deposition temperature. N=9.*

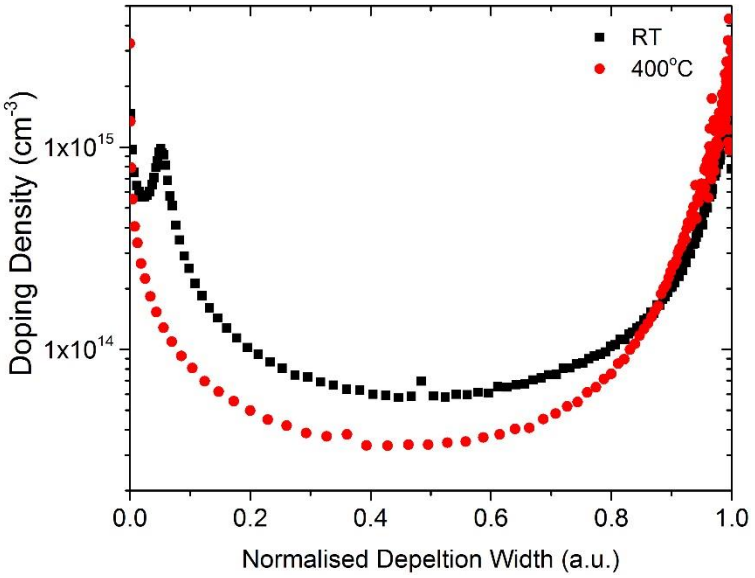

Figure 6.12: *Normalised depletion width – doping density profiles determined from CV measurements for MZO/$CdTe_{(1-X)}Se_X$ based devices with MZO films grown at RT and 400°C. Where 0 represents the MZO/$CdTe_{(1-X)}Se_X$ interface and 1 represents the end of the depletion region.*

Increasing the MZO deposition temperature resulted in an increase to device performance of the 10% Mg content MZO devices, but efficiency was still below that for ZnO based devices. Overall the results presented in this section would seem to indicate there is a limit to the level of performance that can be achieved in co-sputtered MZO based devices despite the enhanced V_{OC}, likely due to the resistivity of the MZO films. A high device performance has been previously demonstrated when using MZO layers produced from a single MZO target however to date a high device performance has never been achieved via co-sputtered method[3,30]. Therefore, the most likely route to improving device performance was thought to be switching to MZO films grown from a single target, as this could potentially result in MZO films with a more uniform Mg content.

6.3. Single target MZO/$CdTe_{(1-X)}Se_X$ based devices

This section will report on the use of MZO films produced from a single target and their influence on $CdTe_{(1-X)}Se_X$ device performance. An MZO target with a Mg content of 11% by wt was chosen for this study as it has been demonstrated by Kephart *et al.*[8] and Albekim *et*

al.[38] to be the optimal Mg content for device performance. It was hoped that by using the MZO films produced from a single target that the high J_{SC} and enhanced V_{OC} (compared to the SnO_2 and ZnO based devices) could be retained, but the low *FF* which resulted from the higher resistivity of the MZO films could be improved.

In this section MZO films fabricated from the single target are characterised and the layers influence on MZO/$CdTe_{(1-X)}Se_X$ device performance analysed. Section 6.3.2 will demonstrate how MZO deposition temperature effected film properties and device performance. It will be shown that an increased deposition temperature was detrimental to performance. Section 6.3.3 will show alternative routes to film optimisation and demonstrate how post MZO growth annealing in an air ambient effected film crystallinity and device performance. Finally Section 6.3.5 will compare MZO and ZnO film properties and their influence on $CdTe_{(1-X)}Se_X$ device performance.

6.3.1. Device Fabrication

100 nm MZO films were fabricated via RF sputtering using a power density of 2.19 W cm^{-2} from a single MZO target (11% MgO and 89% ZnO wt%). Specific MZO layers were post growth annealed in an air ambient for 30 mins. All other device parameters were kept identical to those reported in Section 6.2. A schematic representation of the device structure used in Section 6.3 is shown in Figure 6.1.

6.3.2. Influence of deposition temperature on MZO film properties and device performance

Initially the quality of the MZO layers produced from the single target were characterised, Figure 6.13a shows the XRD patterns for an MZO film grown at RT and 400°C. The films grown at RT demonstrate very little crystallinity being mostly amorphous with a large board peak being observed at around 33°-35°. In Section 6.2.4 it was shown that a deposition temperature of 400°C gave improved device performance therefore, the same conditions were utilised in this section. The MZO films deposited at 400°C displayed a peak

in the XRD pattern at 34.5° which corresponds to the (0002) hexagonal ZnO wurzite phase[32]. This indicates that the increased deposition temperature improved the crystallinity and that the film growth occurs preferentially along the c-axis. The lattice parameters and grain size were estimated from the XRD pattern, the calculated lattice parameter c being 5.192 Å and with an average grain size of 11.52 nm. The grain size from the single target is smaller than that reported previously for the 10-15% MZO films, 28 nm, however the lattice parameter were similar for both a 15% film and the single target MZO film (5.2Å and 5.19Å respectively) indicating a similar Mg content.

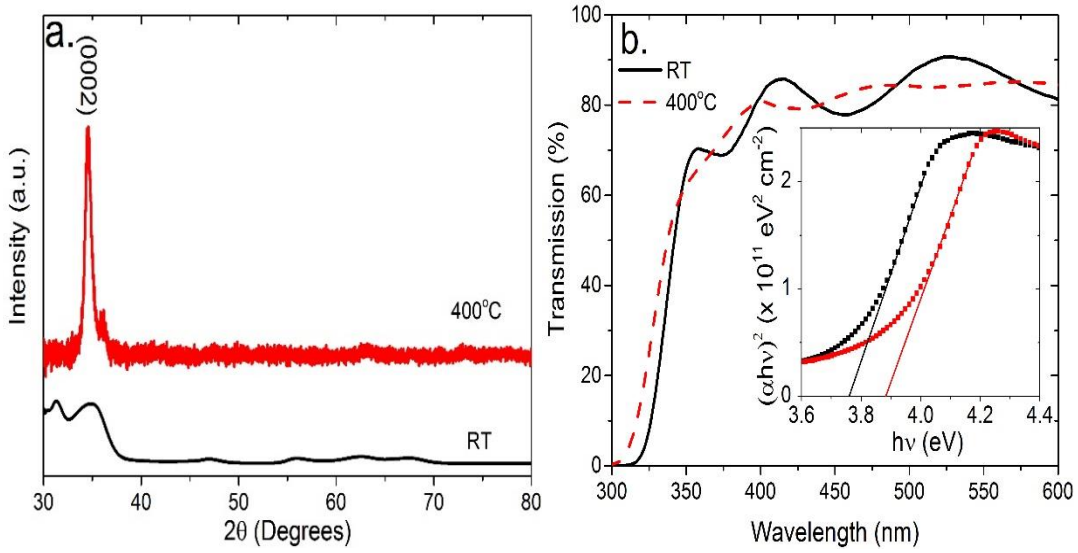

Figure 6.13: *a) XRD patterns and b) transmission spectra (Tauc plot insert) show how deposition temperature effects the crystal structure and optical properties of the MZO films.*

Figure 6.13b shows the optical transmission spectra and Tauc plots produced for the RT and 400°C deposited MZO films. It can be seen that increasing the deposition temperature has increased the bandgap from 3.76 eV to 3.88 eV, this being in contrast to the data presented for the co-sputtered MZO layers where no bandgap shift was observed. Bittau *et al*[29]. demonstrated that an increased deposition temperature can result in an increased Mg content in the MZO film. Therefore, it is proposed that a similar mechanism is occurring here, with higher deposition temperatures resulting in increased Mg incorporation.

6. Use of MZO as the window layer in $CdTe_{(1-X)}Se_X$ devices

Comparative devices were produced using MZO layers deposited at either RT or 400°C. Figure 6.14a-d shows the determined MZO/$CdTe_{(1-X)}Se_X$ device performance parameters for the RT and 400°C devices, with accompanying *JV* and EQE for the highest efficiency contacts shown in Figure 6.15a and b respectively.

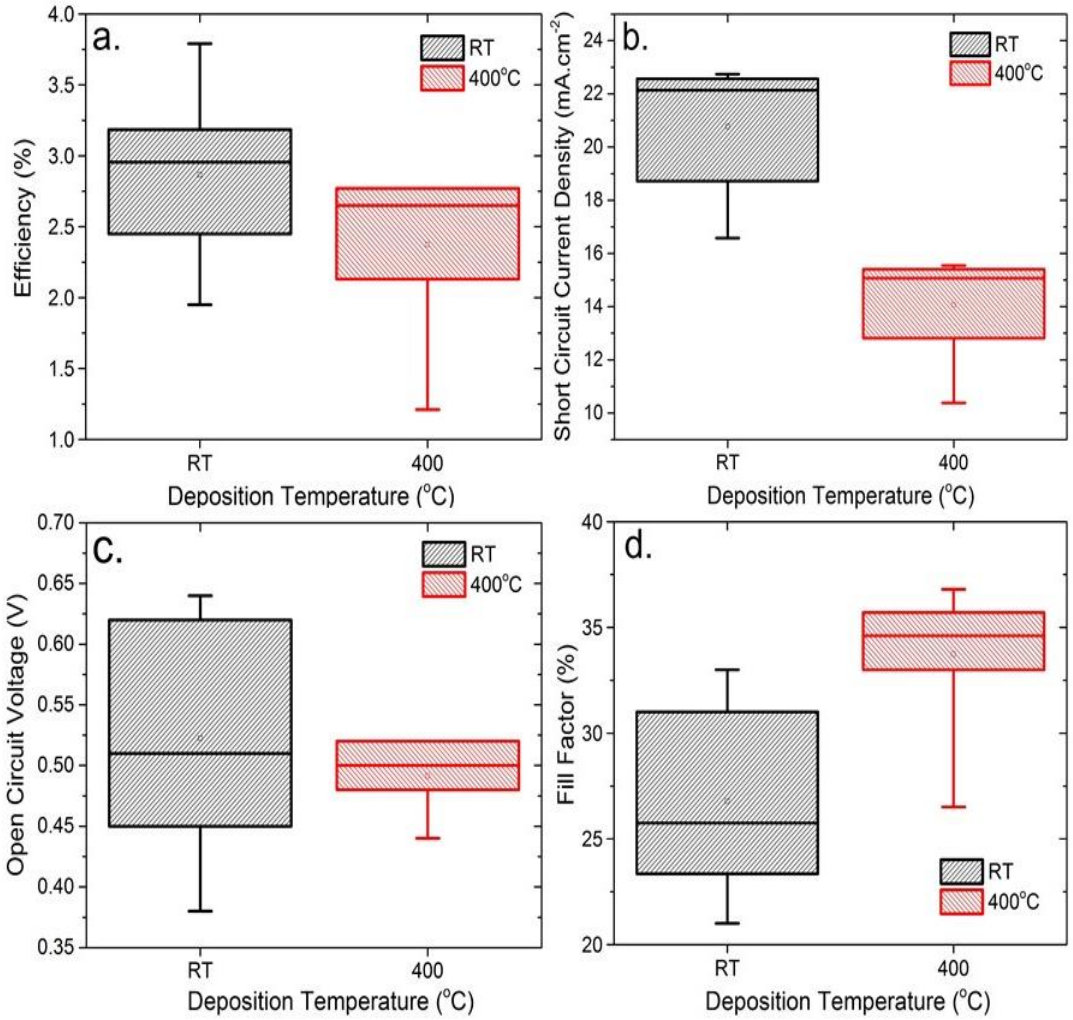

Figure 6.14: *MZO/$CdTe_{(1-X)}Se_X$ device performance parameters a) η, b) J_{SC}, c) V_{OC} and d) FF for devices produced using MZO films grown at RT and 400°C. N = 7.*

The results show that the device performance is universally poor with efficiency < 4% and that the increased deposition temperature is resulting in a reduced efficiency with the average dropping from 2.95% to 2.65% for the RT and 400°C MZO films, respectively. The drop in performance is largely driven by a reduction in J_{SC} and V_{OC} which fell from peak values of 22.75 mA cm^{-2} and 0.64 V to 15.54 mA cm^{-2} to 0.52 V for the RT and 400°C films. The increased deposition temperature did however result in an enhanced *FF* with the

average improving from 25.82% to 34.63%. The improvement to *FF* is largely driven by the removal of the S-shaped *JV* curve.

The removal of the S-shape is an indication the energy barrier produced for the as deposited MZO can be overcome by increasing the deposition temperature, possibly due to the improved conductivity of the MZO films. However, the reduced performance is possibly due to the increased Mg content, which has increased the bandgap and has resulted in a poorer band alignment causing a reduced J_{SC} and V_{OC}. The EQE curves shown in Figure 6.15b show a reduced response across the whole spectrum, this is to be expected as device J_{SC} in the 400°C devices is lower. This results suggested that another route to improving the MZO/$CdTe_{(1-X)}Se_X$ device performance needs to be investigated.

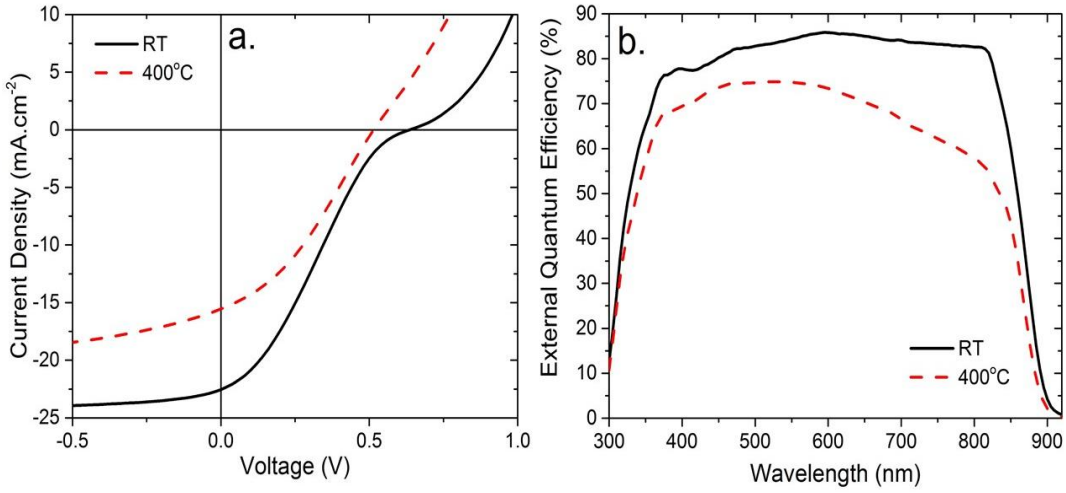

Figure 6.15: *a) JV and b) EQE responses for the highest efficiency MZO/$CdTe_{(1-X)}Se_X$ devices with MZO films grown at RT and 400°C.*

6.3.3. Influence of post MZO growth annealing on film properties and device performance

It has been previously shown that the crystal structure of oxide thin films can be enhanced or modified by post growth annealing the films in a variety of different ambient conditions such as in TiO_2 and ZnO[14,33]. This section will report on efforts to improve the film properties of the MZO layer, and thus MZO/$CdTe_{(1-X)}Se_X$ device performance by performing a post growth anneal.

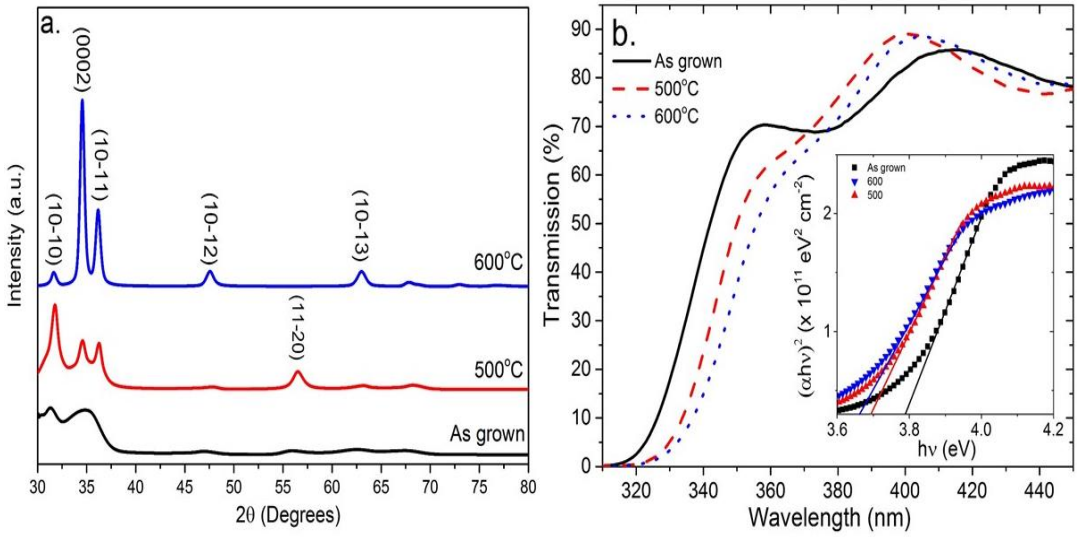

Figure 6.16: *a) XRD patterns and b) transmission spectra (Tauc plot insert) showing how annealing the MZO films at a range of temperatures in an air ambient effects its crystal structure and optical properties.*

Figure 6.16a shows the XRD patterns for MZO films grown at RT and films subsequently post growth annealed in an air ambient at 500°C or 600°C for 30 mins. Temperatures of greater than 500°C were chosen as this was demonstrated to be effective annealing conditions for TiO_2[33]. The unannealed MZO films show very little crystallinity being mostly amorphous as was observed in Section 6.3.2. Annealing the films induces crystallisation, with 600°C exhibiting a more strongly crystalline hexagonal wurtzite structure than the 500°C annealed sample, which retains some amorphous character. Films annealed at 600°C showed preferential recrystallisation along the c-axis, demonstrated by the intensity of the (0002) diffraction peak at 34.56°[17].

The effect of annealing the MZO films on the optical transmission and associated Tauc plot are shown in Figure 6.16b and 6.16b (insert), respectively. Annealing the films resulted in a reduction in the bandgap from 3.76 eV to 3.61 eV for the as-deposited and 600°C annealed films respectively. As previously noted the bandgap change can occur due to a shift in the Mg content in the MZO films due to deposition temperature[29,34]. However, the XRD pattern shown in Figure 6.16a shows no shift in the (0002) peak at 34.56° between the 500°C implying no shift in the Mg content has occurred. To confirm this XPS measurements

were performed on the as-deposited and 600°C annealed films, Figure 6.17a and b show XPS core-level spectra of the Mg 1s and Zn 2p signals before and after annealing. There was no noticeable change in the Mg and Zn peaks, or in the relative intensities which demonstrates that the Mg content remained constant following annealing (see Table 6.2)[17,28].

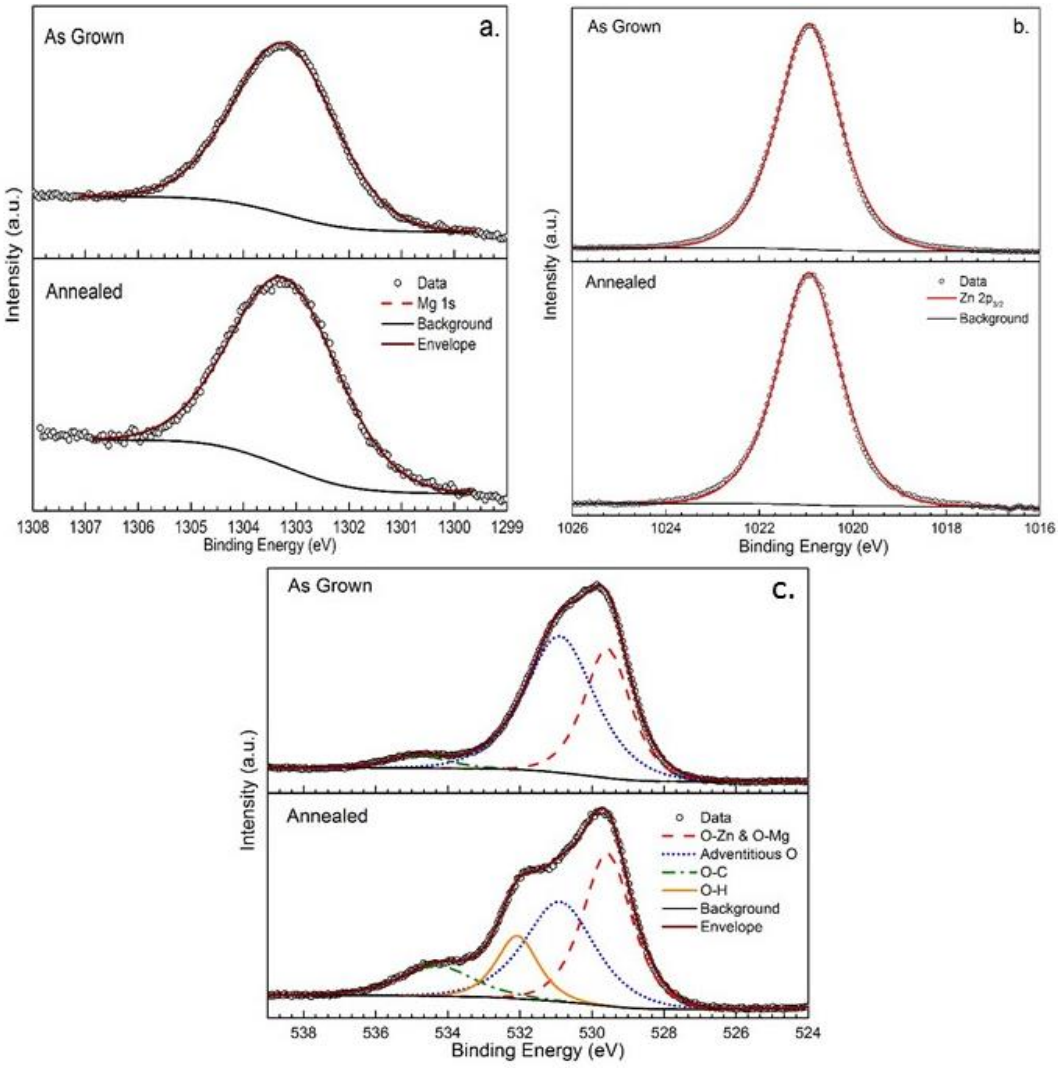

Figure 6.17: *XPS core level spectra of the Mg 1s (a), Zn $2p_{3/2}$ (b) and O 1s (c) region for the as-grown (top panel) and annealed 600°C (bottom panel) MZO films.*

Figure 6.17c also shows the XPS core–level spectra of the oxygen 1s peak for MZO films as-deposited and following annealing at 600°C. The unannealed sample shows three components – assigned to the metal oxides, MgO and ZnO, (included as one peak due to the negligible binding energy difference of Mg-O and Zn-O), un-bonded contaminant, or

adventitious, oxygen and oxygen contaminant bonded to carbon. Upon annealing the relative quantity of adventitious oxygen is reduced along with the formation of another species, assigned to a hydroxyl. The metal oxide peak is unaffected, supporting the conclusion that the annealing does not affect the chemical composition of the metal oxide species. Instead it appears to reduce the amount of surface oxide contamination, whilst also forming a hydroxyl species on the surface[28].

Table 6.2: *Relative peak intensities taken from the XPS measurements shown in Figure 6.17.*

Relative peak areas	As deposited	Annealed at 600°C
Mg:Zn	0.371	0.365
O: Mg+Zn	0.190	0.399

As the Mg content did not appear to be changing, the bandgap shift observed in Figure 6.16b clearly had a different cause. A shift in the bandgap has previously been observed to occur due to changes in crystallinity following an annealing step, similar bandgap reductions have been reported by others in both ZnO[13] and Al_2O_3[35] films, following the change from an amorphous to a crystalline material. The amorphous structure has a larger and more distorted interatomic spacing than in a crystalline structure due to absence of long-range translational periodicity. Therefore, the extended localisation between the CB and VB is increased, thus increasing the optical bandgap. As a result, the bandgap shift observed in this work likely results from the change from an amorphous to a hexagonal wurzite crystalline structure.

SEM images were taken of the as deposited and annealed films (Figure 6.18a and b) but showed little of note other than an increase in the film uniformity for the 600°C annealed sample. Raman analysis (Figure 6.18c) confirmed the presence of the MZO wurtzite phase (RRUFFID: R060027). This confirms that the addition of Mg into the ZnO films is not significantly altering its crystal structure as a wurzite crystal structure is still observed.

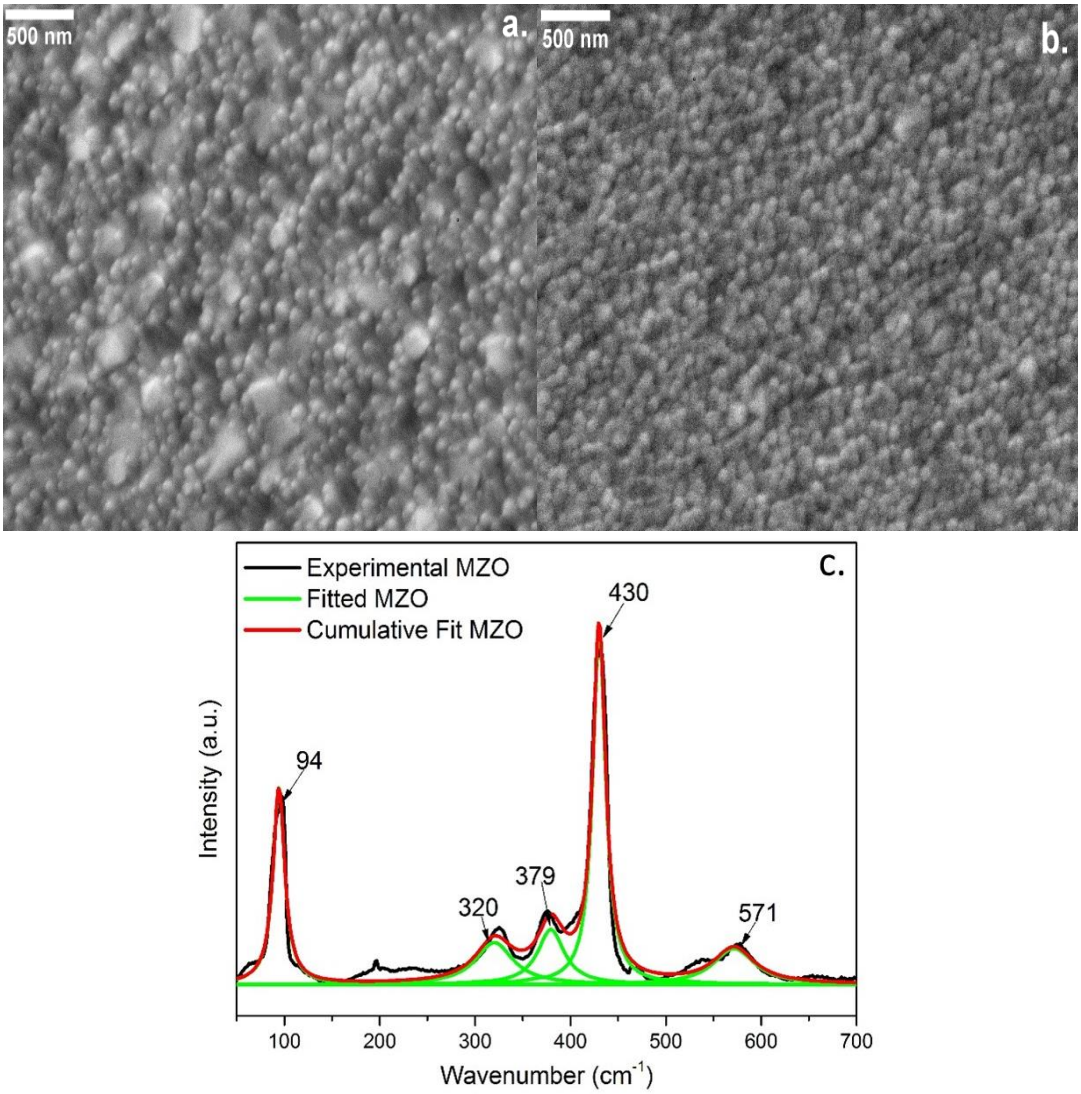

Figure 6.18: *Secondary electron micrographs (SEM) of the as-grown (a) and annealed at 600°C MZO films. Raman spectra (c) of MZO confirming the hexagonal wurzite structure.*

A series of devices were produced where the MZO layer was post growth annealed at either 500°C or 600°C for 30 mins prior to cell fabrication and compared with an as-grown MZO equivalent. The effect of the post MZO growth annealing temperature on MZO/$CdTe_{(1-X)}Se_X$ device performance parameters is shown in Figure 6.19a-d. The as-grown devices, as shown in Section 6.3.2, display a low average performance (< 3%), primarily due to a low V_{OC} and *FF*. The low V_{OC} could be an indication the MZO/$CdTe_{(1-X)}Se_X$ interface is of a poor quality resulting in high levels of recombination, as amorphous films have higher

number of surface states and dangling bonds[36]. The low *FF* in the as deposited MZO devices is primarily due to the very high series resistance (R_S) > 100 Ω.cm^{-2} (Figure 6.20).

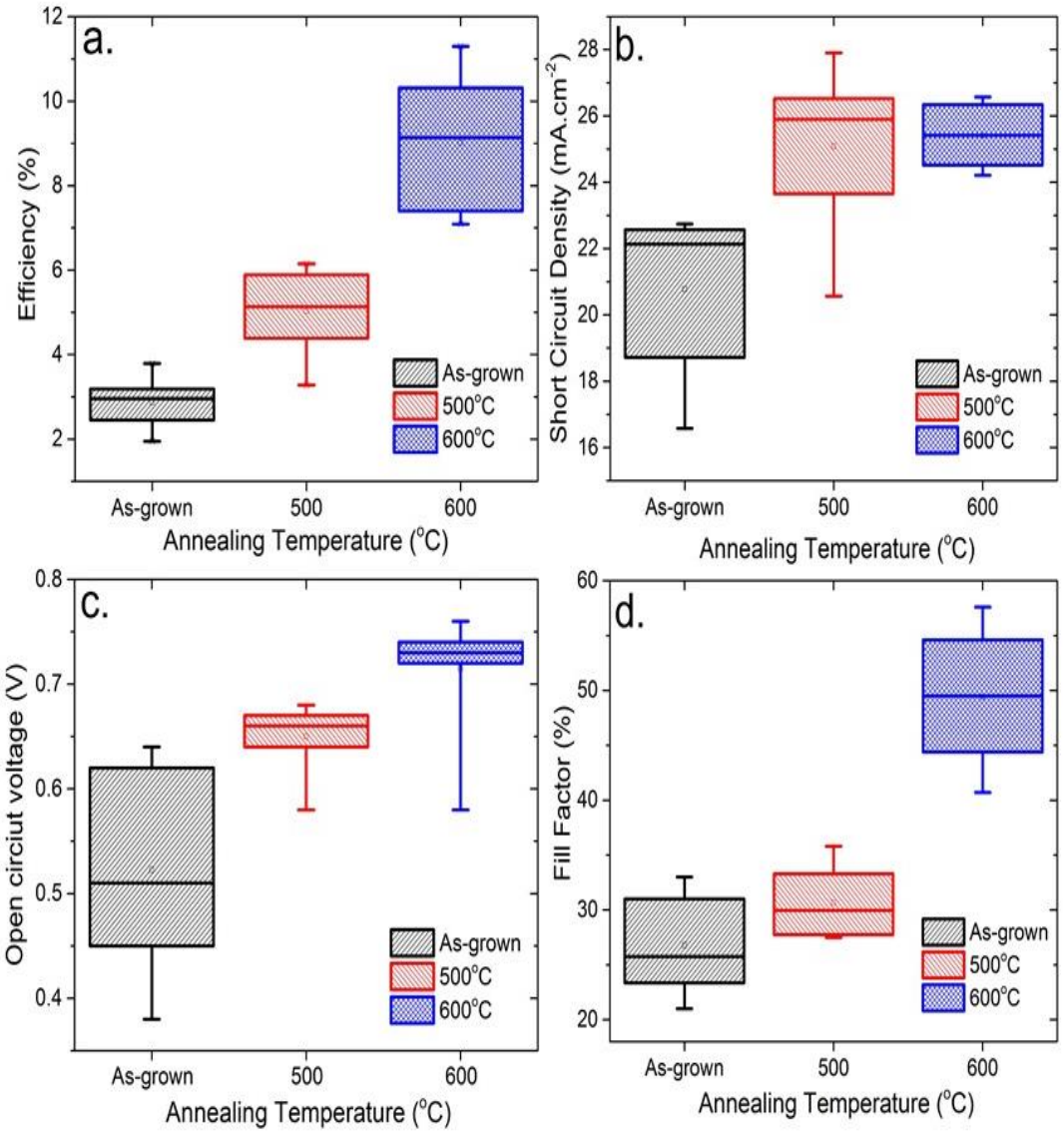

Figure 6.19: *MZO/$CdTe_{(1-X)}Se_X$ device performance parameters a) η, b) J_{SC}, c) V_{OC} and d) FF for cells produced using a variety of post MZO growth annealing temperatures in an air ambient for 30 mins. N = 8.*

Post growth annealing the MZO films at 500°C and 600°C had a significant effect on device performance, increasing from a champion performance of 3.79% in the unannealed devices, to 6.15% and 11.30% for the 500°C and 600°C annealed films respectively. This improvement is predominantly due to improvements in device V_{OC} and a particularly large *FF* improvement between 500°C and 600°C. The improvement in *FF* is due to a substantial reduction to device R_S, reducing from 121.3 Ω cm^{-2} for the unannealed films to 25.4 Ω cm^{-2}

and 10.8 Ω cm^{-2} for the 500°C and 600°C annealed films respectively (see Figure 6.20). The average V_{OC} improved from 0.52 V to 0.73 V in the unannealed and 600°C films respectively, indicating the improved crystal structure of the MZO layers had a significant impact on the quality of the MZO/$CdTe_{(1-X)}Se_X$ interface, reduced the level of recombination and resulting in the enhanced V_{OC}. Additionally when compared to the SnO_2 alternative (Section 5.4) the peak V_{OC} was improved from 0.72 V to 0.76 V, again indicating that MZO/$CdTe_{(1-X)}Se_X$ interface is of a superior quality to the SnO_2/$CdTe_{(1-X)}Se_X$ and possibly has a reduced level of recombination. However, the overall performance is reduced, 11.3% compared to 13.5%, mainly due to losses in *FF* from the higher resistivity of the MZO layer.

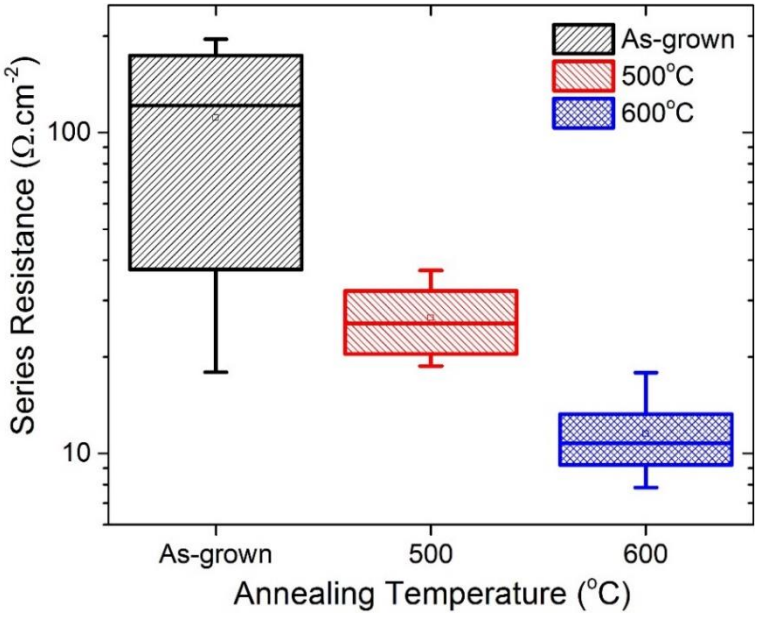

Figure 6.20: *MZO/$CdTe_{(1-X)}Se_X$ device series resistance (R_s) as a function of MZO post growth annealing temperature. N=8.*

This result would indicate that the V_{OC} and *FF* could be improved if a better window layer/$CdTe_{(1-X)}Se_X$ combination could be achieved either by finding a more ideal partner layer or through further optimisation of the MZO layer and interface. The results also demonstrate that whilst the choice of window layer is important, the optimisation of the window layer is also essential in order for a peak performance to be achieved.

Figure 6.21 shows the *JV* (a), EQE (b), doping density – depletion width calculated from *CV* data (c) and normalised carrier density – depletion width (d) responses as a function of post MZO growth annealing for the highest performing contact from each device. The post growth annealing of MZO films has a significant effect on the *JV* (Figure 6.21a) response, with the as-grown films displaying the now familiar S-shaped *JV* curve.

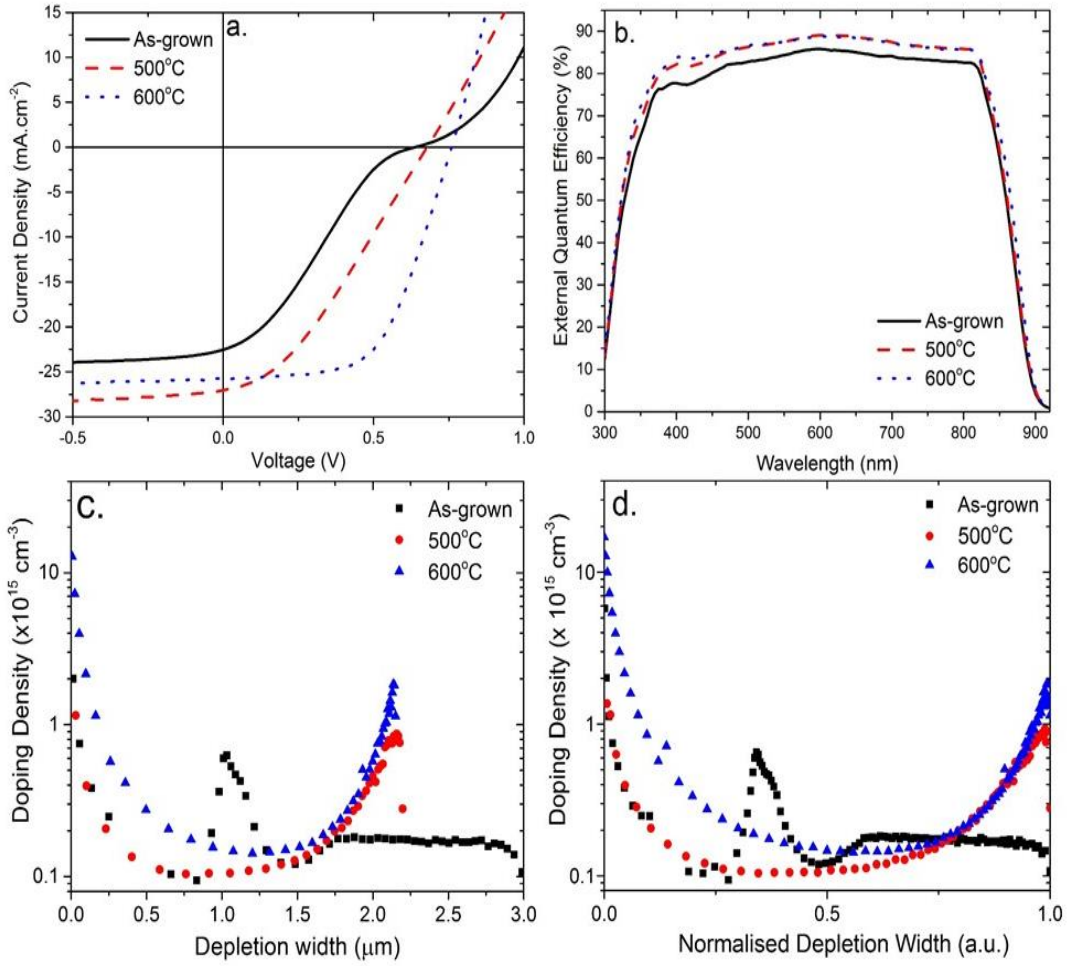

Figure 6.21: *JV (a), EQE (b), carrier density – depletion width (c), carrier density – normalised depletion width profiles (d) response for the highest efficiency contacts as a function of post MZO growth annealing at various temperatures in an air atmosphere for 30 mins. In the normalised plot 1 represents the end of the depletion region and 0 represents the MZO/$CdTe_{(1-X)}Se_X$ interface.*

The doping density - normalised depletion width plots are shown in Figure 6.21d, extracted from *CV* analysis. The depletion width values have been normalised from 0 to 1, where 1 represents the end of the depletion region and 0 represents the front MZO/$CdTe_{(1-X)}Se_X$ device interface, the unnormalized plots are given in Figure 6.21c. Similar to the profiles presented for co-sputtered MZO devices in Section 6.2.3, the as-grown MZO

devices demonstrate a spike in the capacitance, suggesting an apparent doping density increase. This spike, however, results from charge accumulation at the interface due to an energy barrier being formed and the high resistivity of the as-grown MZO films[26,37].

Annealing the MZO film removes the S-shape in the *JV* curves, although the 500°C annealed device still shows high levels of series resistance compared to the 600°C devices (Figure 6.21). The removal of the S-shape in the *JV* curve seems to be the primary driving force behind the improvement to device performance, this coincides with the characteristic U-shape observed in the doping density – depletion width profiles for 500°C and 600°C annealed devices. This would indicate that following annealing photo generated carriers can flow across the interface without being strongly affected by an energy barrier[23]. Post MZO growth annealing of the MZO had very little influence on the device EQE curves (Figure 6.21b), with only a small increase to device response which is broadly in agreement with the minimal change in J_{SC} (Figure 6.19b).

Ren *et al* [9]*.* similarly demonstrated that thermally annealing the MZO films at 600°C was essential in order to achieve optimal performance, however they employed MZO as a highly resistive transparent (HRT) buffer layer in MZO/CdS/CdSe/CdTe based devices, i.e. the device featured a $CdS/CdTe_{(1-X)}Se_X$ interface rather than a $MZO/CdTe_{(1-X)}Se_X$ interface. The improved performance was ascribed to an increase in the conductivity of the MZO films due to an increased grain size and carrier concentration owing to an increase in oxygen vacancies and a reduction in adsorbed oxygen[9]. It is postulated that a similar mechanism is occurring in this instance, where increased conductivity following annealing is leading to the observed reduction in series resistance and resulting in the enhanced performance. The XPS analysis in Figure 6.17 showed that the amount of surface oxygen was reduced in the MZO layer therefore, it is possible that the surface oxygen could be enhancing the resistivity at the interface and the removal of this layer is contributing to the enhanced conductivity.

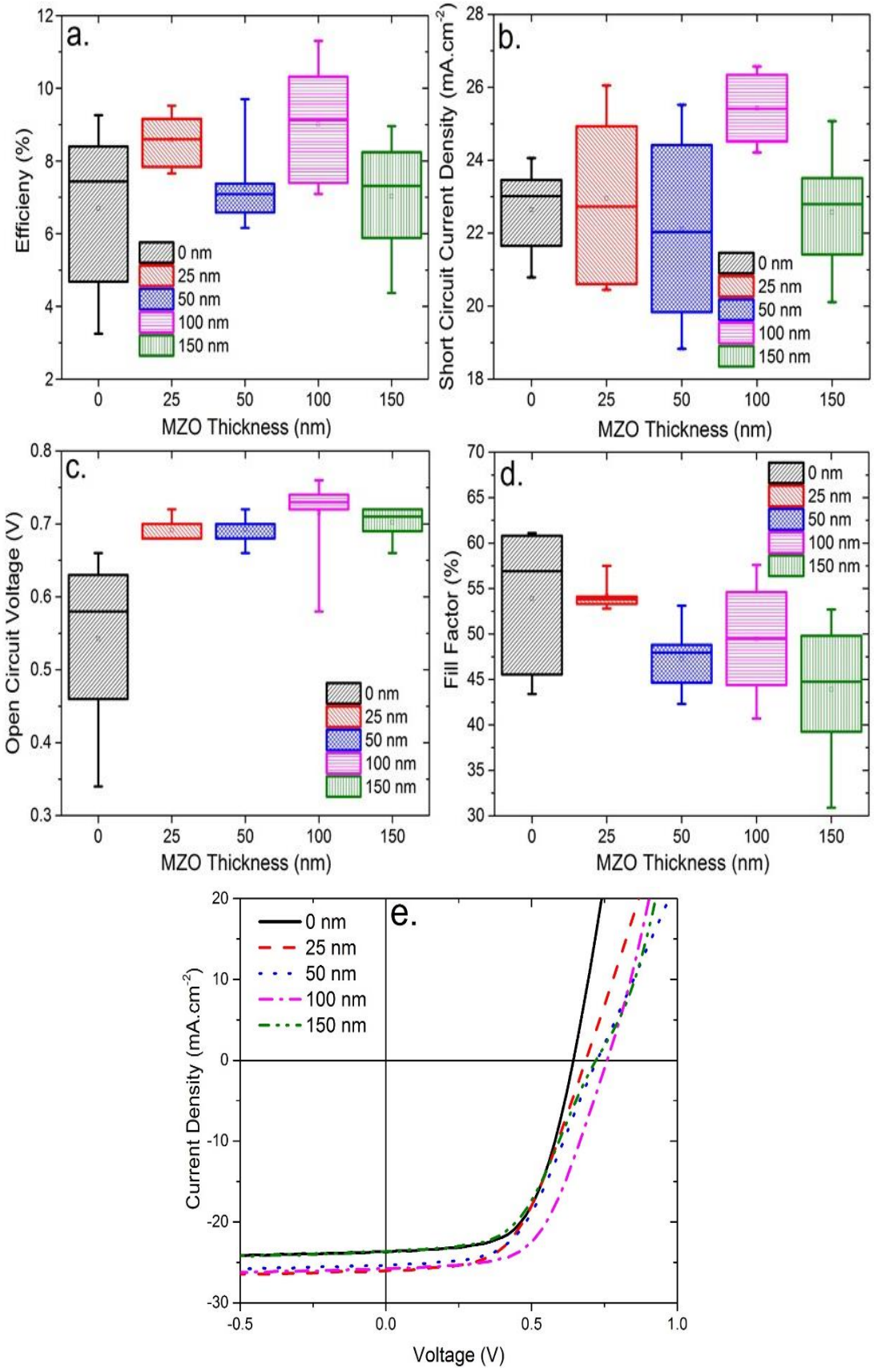

Figure 6.22: *MZO/$CdTe_{(1-X)}Se_X$ device performance parameters a) η, b) J_{SC}, c) V_{OC} and d) FF as a function of MZO layer thickness. N = 8 e) Shows the JV curves for the highest efficiency contacts. MZO layers were post growth annealed at 600°C in an air ambient for 30 mins.*

6. Use of MZO as the window layer in $CdTe_{(1-X)}Se_X$ devices

Following optimisation of the post growth anneal step, the thickness of the MZO layer was investigated as the R_S produced for 100 nm was still quite high, 10.77 Ω cm^{-2}, which could be limiting performance. Figure 6.22a-d shows the device performance parameters as a function of MZO layer thickness ranging from 0 nm (i.e. no MZO layer) to 150 nm. Layers were post growth annealed in an air ambient at 600°C for 30 mins, the *JV* curves for the highest efficiency contacts are shown in Figure 6.22e. The peak efficiency improved from 9.25% to 11.30% when 0 nm and 100 nm layers were incorporated. The peak efficiency improved sequentially with increasing MZO thickness up to 100 nm, with values of 9.52% and 9.70% when 25 nm and 50 nm MZO layers were utilised. The improvement of over 2% was largely driven by improvements to device V_{OC} which improved from 0.66 V to 0.76 V for 0 nm and 100 nm layers respectively, this was again suggestive of a superior interface being formed. The *FF* does however decrease with increasing MZO layer thickness possibly due to enhanced resistive losses. The performance of the devices decreases when 150 nm MZO layers are utilised, due to losses to all device parameters but particularly *FF*. From the *JV* curves (Figure 6.22e) it can be seen that using a 150 nm layer results in the return of the S-shape to the device *JV* response, possibly due to the MZO films being too resistive at this thickness, this strongly indicates that the origin of the S-Shaped curve is due to resistive effects. These results demonstrate that the thickness of the MZO layer is critical in order for an optimal performance to be achieved.

Table 6.3: *Peak and average ± standard deviation (SD) device parameters showing hysteresis in the MZO/$CdTe_{(1-X)}Se_X$ devices when they are scanned forward -ve to +ve and in reverse +ve to - ve. The MZO layer was annealed at 600°C in air for 30 mins.*

Measured	η (%)	J_{SC} (mA.cm^{-2})	V_{OC} (V)	*FF* (%)
Forward	11.3 (9.01±0.54)	25.80 (25.42±0.32)	0.76 (0.72±0.02)	57.6 (49.41±2.08)
Reverse	12.4 (9.28±0.71)	26.02 (23.81±0.83)	0.76 (0.74±0.01)	62.80 (54.64±2.14)

6. Use of MZO as the window layer in $CdTe_{(1-X)}Se_X$ devices

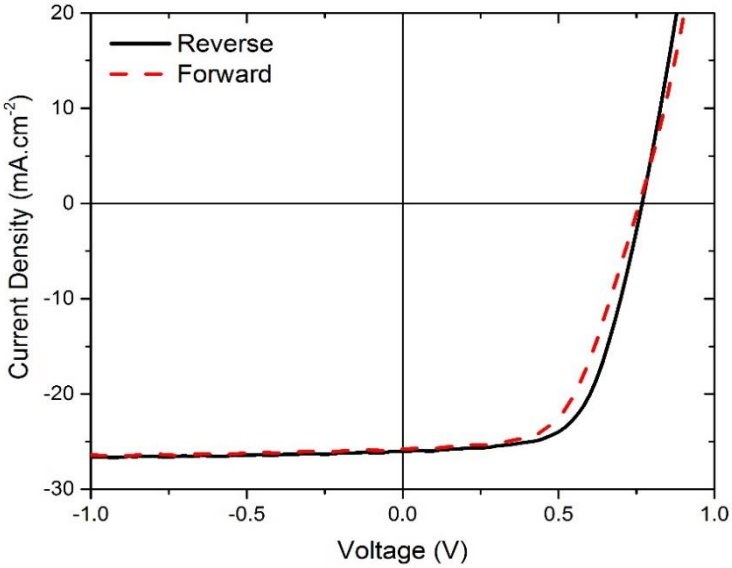

Figure 6.23: *JV response for the highest efficiency contact MZO/$CdTe_{(1-X)}Se_X$ device scanned in the forward (-ve to +ve) and reverse (+ve to –ve) directions showing hysteresis present in these devices. The MZO was annealed at 600°C in air for 30 mins.*

It was observed during *JV* analysis that the addition of MZO into the device structure introduced a small amount of hysteresis into the devices. The performance improved from 11.3% to 12.4% when the devices were scanned in the forward (i.e. –ve to + ve) and reverse (i.e. +ve to – ve) bias directions respectively (see Figure 6.23 and Table 6.3). The device parameter predominately affected by this was the *FF* which improved by over 5%. Hysteresis is a well-known phenomenon in perovskite based solar cells,[38] but is not routinely observed in CdTe. One of the primary reasons for this in perovskites is charge accumulation at the TiO_2 interface, this accumulation being dependant on the bias sweep direction[39]. It is postulated that the same mechanism is happening here despite the removal of the S-shaped curve some charge accumulation is still occurring at the MZO interface resulting in small amounts of hysteresis. No such hysteresis effects are observed for CdS based devices.

It is clear from the device based results presented in this section that the post MZO growth annealing had a key impact on device performance, the improvement being due to a change from an amorphous film to a well-ordered crystalline wurtzite structure. This change in crystallinity results in an increase to the conductivity of the MZO films, reduction

to device R_S and thus increased *FF*. The removal of the spike in the doping density – depletion width profile (see Figure 6.21d) would also indicate that annealing results in less charge accumulation at the MZO/$CdTe_{(1-X)}Se_X$ interface due to the increased conductivity.

The improved V_{OC} following annealing is an indication that the MZO/$CdTe_{(1-X)}Se_X$ interface is of a higher quality, yielding a reduced level of recombination. Again, the increased crystallinity and conductivity of the MZO is the likely cause, yielding a more ordered structure at the interface and fewer dangling bonds, decreasing the level of recombination and limit V_{OC}. An alternative mechanism for the V_{OC} improvement could be the reduced bandgap upon annealing, lowering the conduction band position and spike at the interface providing a more favourable interface and thus an improved V_{OC}. Further optimisation of the MZO layer will be likely to yield additional improvements to device performance particularly by improving device *FF*.

6.3.4. Structural Analysis of MZO/$CdTe_{(1-X)}Se_X$ devices

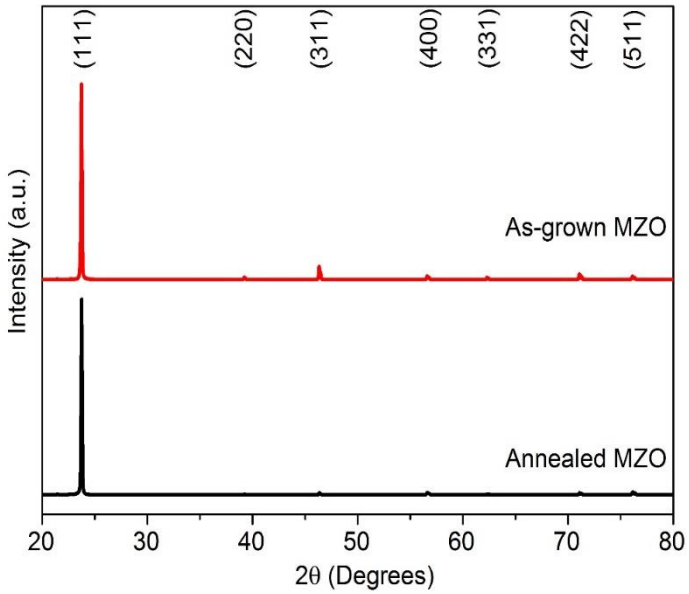

Figure 6.24: *XRD pattern produced for the $CdTe_{(1-X)}Se_X$ layer deposited on as-grown (top) and annealed at 600°C annealed (bottom) MZO layers.*

Following device optimisation and improvement in depth structural analysis was performed to determine the influence of the MZO film on the $CdTe_{(1-X)}Se_X$ layer and device

stack. Figure 6.24 shows the XRD patterns produced for $CdTe_{(1-X)}Se_X$ layers deposited on as-grown and 600°C annealed MZO layers. It is clear from this data that the $CdTe_{(1-X)}Se_X$ layer is highly (111) oriented regardless of MZO layer annealing, with the only difference being the $CdTe_{(1-X)}Se_X$ films grown on annealed MZO do show a slightly more oriented (111) film. This indicates that the change from an amorphous MZO structure to a crystalline structure is having little influence on the $CdTe_{(1-X)}Se_X$ in terms of crystallinity and preferred orientation. As no significant change was observed in the XRD patterns for the as-grown and annealed MZO more in-depth structural analysis focussed on MZO/$CdTe_{(1-X)}Se_X$ devices where the MZO layer was annealed at 600°C, as this gave the best device performance.

Figure 6.25 shows a STEM image of a FIB milled cross section from an MZO/$CdTe_{(1-X)}Se_X$ device stack. It can be seen for this image that depositing the CdTe layer on top of MZO/CdSe seed layers results in a uniform coverage of the MZO layer. This is in contrast to data presented in the prior results chapter (Section 5.4.2.2), where large voids were seen at the interface when SnO_2 was used as the device window layer. The removal of these voids at the interface and improved surface coverage could be contributing to the enhanced V_{OC} observed in the MZO/$CdTe_{(1-X)}Se_X$ devices[40,41]. This suggests that the choice of window layer is important for early stage CdTe growth.

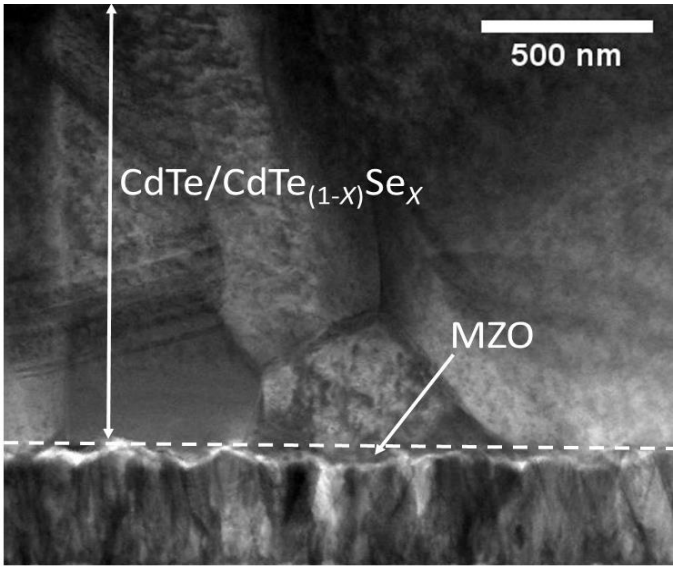

Figure 6.25: *FIB cross sectional STEM image of the MZO/$CdTe_{(1-X)}Se_X$ device stack.*

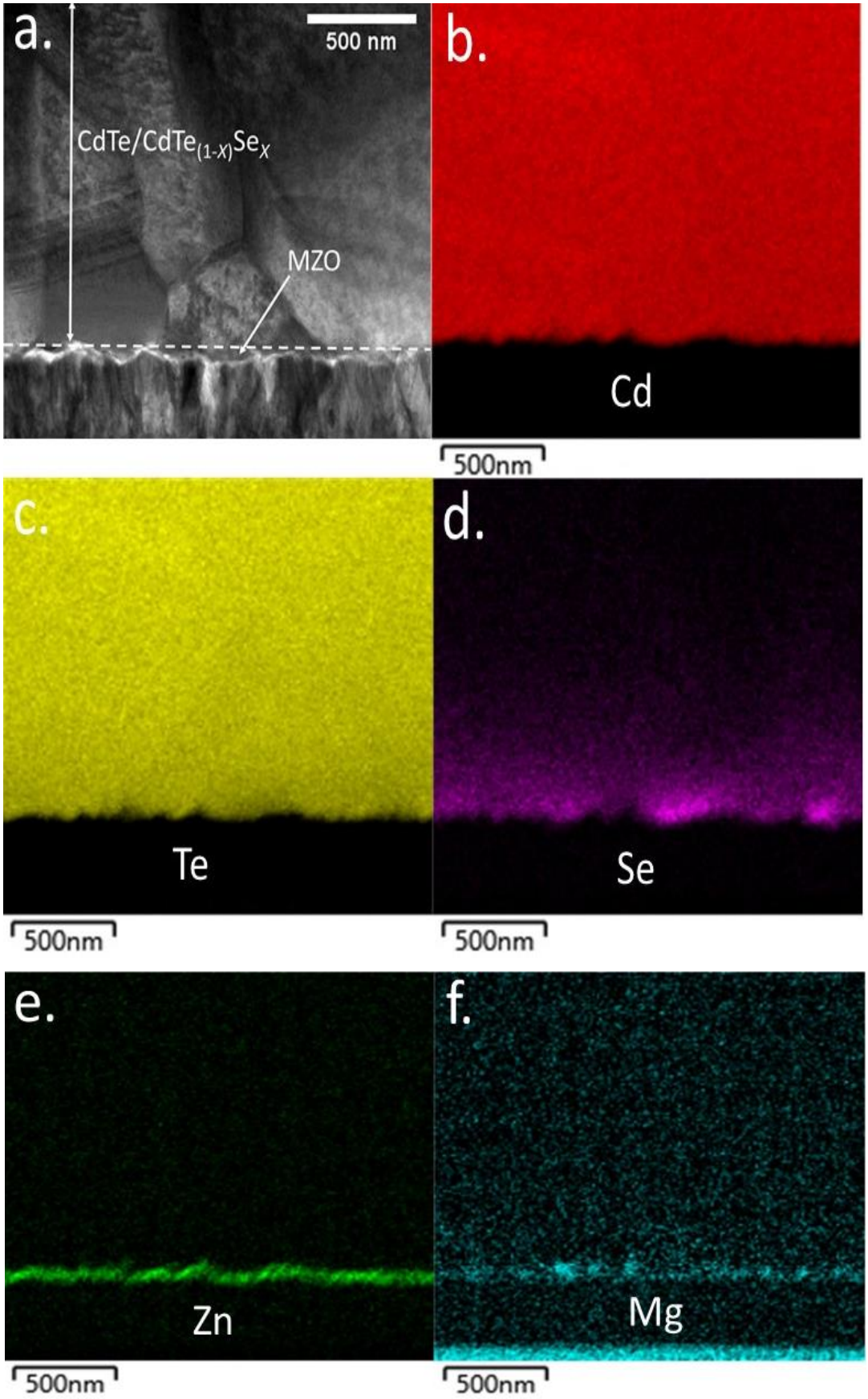

Figure 6.26: *a) STEM cross sectional image of a MZO/$CdTe_{(1-X)}Se_X$ device. Associated EDX maps for the (b) Cd, (c) Te, (d) Se, (e) Zn and (f) Mg.*

Figure 6.26b-f shows the Cd, Te, Se, Zn and Mg EDX maps for the MZO/$CdTe_{(1-X)}Se_X$ STEM image shown in Figure 6.26a, with the accompanying line scan for the all the profiles shown in Figure 6.27a and b. Line scans have been normalised with front surface representing the MZO/ $CdTe_{(1-X)}Se_X$ interface. No voids are visible in the Cd or Te elemental maps (Figure 6.26b, c and Figure 6.27a) again showing that a uniform film is forming at the interface. Apart from the lack of void formation, the Cd, Te and Se maps show very similar results to those seen for the SnO_2/$CdTe_{(1-X)}Se_X$ based devices in Section 5.4.2.2. Te appears to diffuse in the CdSe layer forming the $CdTe_{(1-X)}Se_X$ phase, rather than Se diffusing through the CdTe layer forming a graded $CdTe_{(1-X)}Se_X$ phase. The Se profiles (Figure 6.26d and Figure 6.27a) again shows little evidence of a graded Se content, with a very high Se concentration still present toward the MZO/$CdTe_{(1-X)}Se_X$ front interface and little Se beyond the first 500 nm. The deposited MZO layer can also clearly be seen on top of the FTO layer in the Zn and Mg elemental maps (Figure 6.26e, f and Figure 6.27b). This would suggest that whilst the window layer can influence the surface coverage of the $CdTe_{(1-X)}Se_X$ phase it does little to help enhance the Se out-diffusion and that further developments are needed in order for efficient Se grading to be achieved.

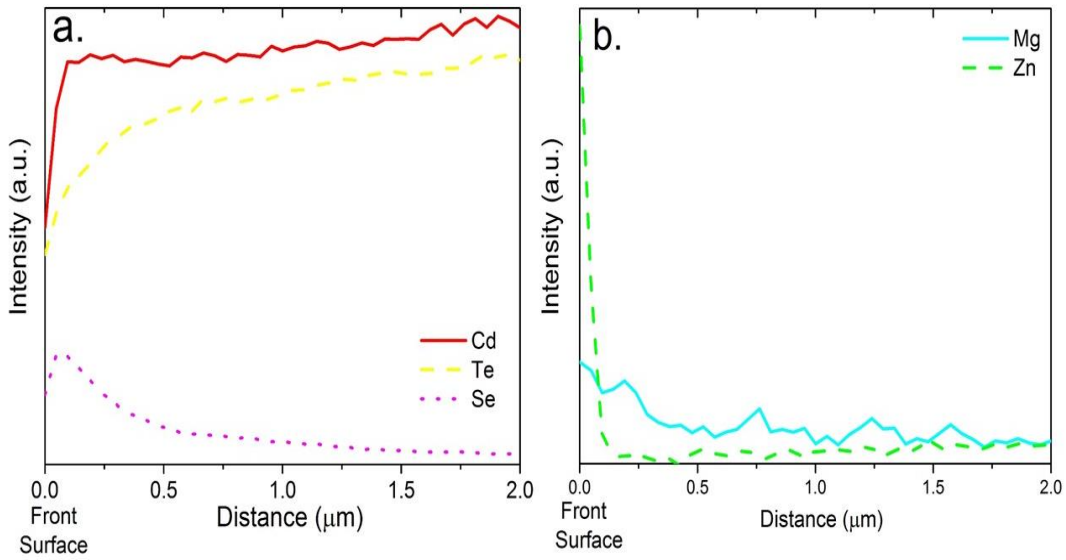

Figure 6.27: *Elemental line scan profiles extracted from EDX maps shown in Figure 6.26. a) Cd, Te and Se profiles and b) Mg and Zn profiles.*

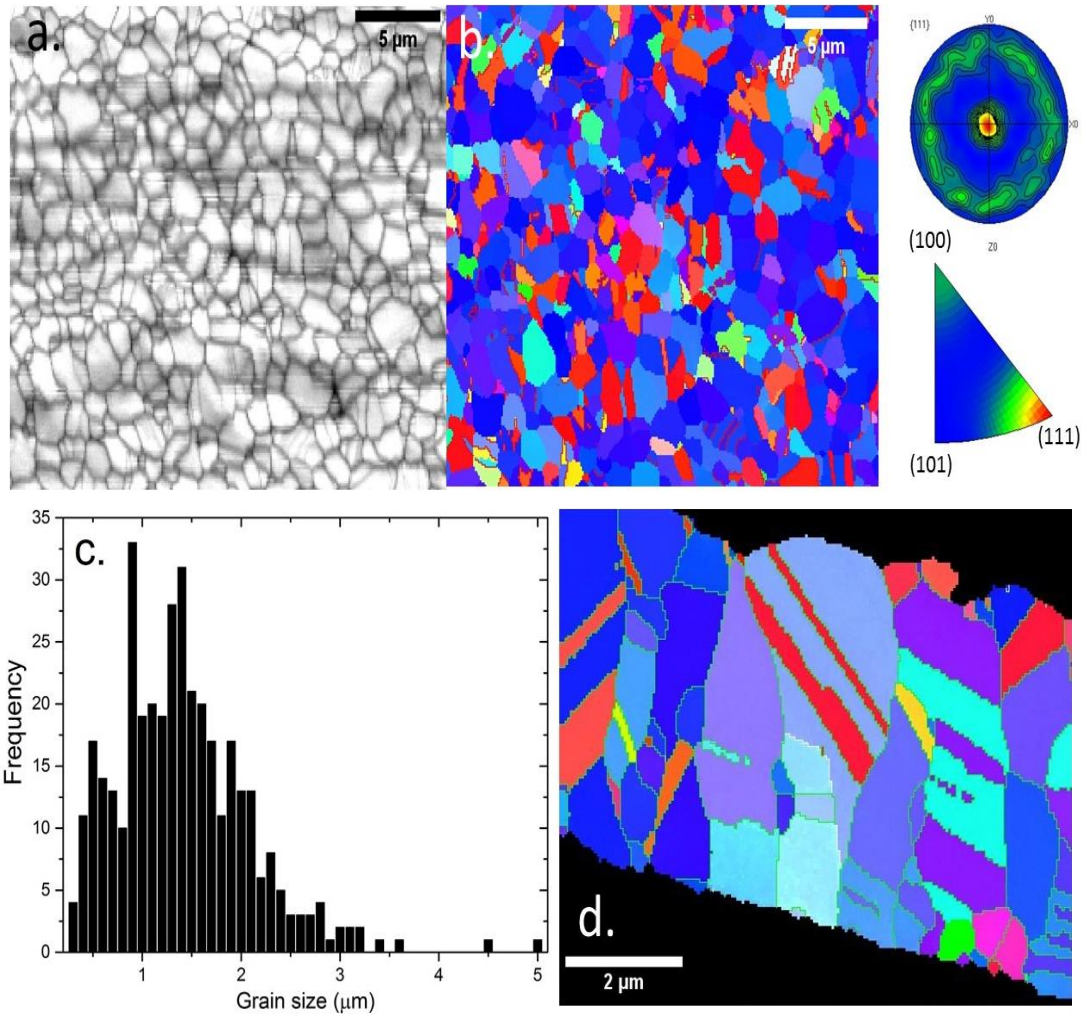

Figure 6.28: *a) Planar electron back scatter image of CSS grown MZO/$CdTe_{(1-X)}Se_X$ layers. b) Planar EBSD inverse pole figure map, the (111) pole and inverse pole figures are also shown, c) grain size distribution from the EBSD image and d) cross sectional EBSD image.*

The influence of using MZO as the window layer on the $CdTe_{(1-X)}Se_X$ growth at a grain to grain level was assessed using EBSD. Figure 6.28a shows the planar electron back scattered image of a MZO/$CdTe_{(1-X)}Se_X$ device back surface and Figure 6.28b shows the planar EBSD inverse pole figure maps of this area. The (111) pole and inverse pole figures are also shown. The grain size distribution extracted from EBSD analysis is shown in Figure 6.28c and a cross sectional EBSD image of the MZO/$CdTe_{(1-X)}Se_X$ device stack is shown in Figure 6.28d.

The $CdTe_{(1-X)}Se_X$ layers are highly orientated in the (111) direction, in agreement with the more bulk sensitive XRD analysis shown in Figure 6.24[42,43]. $CdTe_{(1-X)}Se_X$ layers grown on

MZO show a grain structure that is more orientated in the (111) direction when compared to the CdTe layers grown on SnO_2 (Section 5.4.2.2) indicating the MZO layer is having an impact on the early stage $CdTe_{(1-X)}Se_X$ growth. Also, while the peak of the grain size distribution for growth of $CdTe_{(1-X)}Se_X$ is < 1 μm on SnO_2, it is increased to ≈ 1.5 μm for growth on MZO this may contribute to the higher V_{OC} values for MZO based devices, as films with larger grains have a reduced grain boundary ratio and as mentioned in Chapter 3 this can result in a reduced level of recombination and improved V_{OC}. It is also clear from the cross-sectional image that CdTe film exhibits a preferred (111) growth orientation throughout the entire CdTe layer. This in contrast to the data presented for the SnO_2 based devices where cross sectional EBSD images indicated more random growth at the near interface region, again suggesting that the MZO is influencing the early stage growth of the $CdTe_{(1-X)}Se_X$ layer.

6.3.5. MZO and ZnO window layer film and device comparison

Following optimisation of the MZO layer, it was decided to make a direct comparison of the material and device performance with ZnO to evaluate the overall influence of Mg incorporation. In order for a like for like comparison with MZO, the ZnO films were also post growth annealed at 600°C in an air ambient. Figure 6.29a shows the XRD pattern for ZnO films as deposited and annealed at 600°C, showing peaks at (0002) and (0004), indicating the films grew preferentially along the c-axis regardless of annealing temperature and that the post growth annealing did not have a significant impact on the ZnO wurzite crystal structure. Figure 6.29b shows a high resolution measurement of the (0002) diffraction peak for the annealed MZO and ZnO films. Table 6.4 shows the lattice parameters and grain size estimated from the XRD measurements.

6. Use of MZO as the window layer in $CdTe_{(1-X)}Se_X$ devices

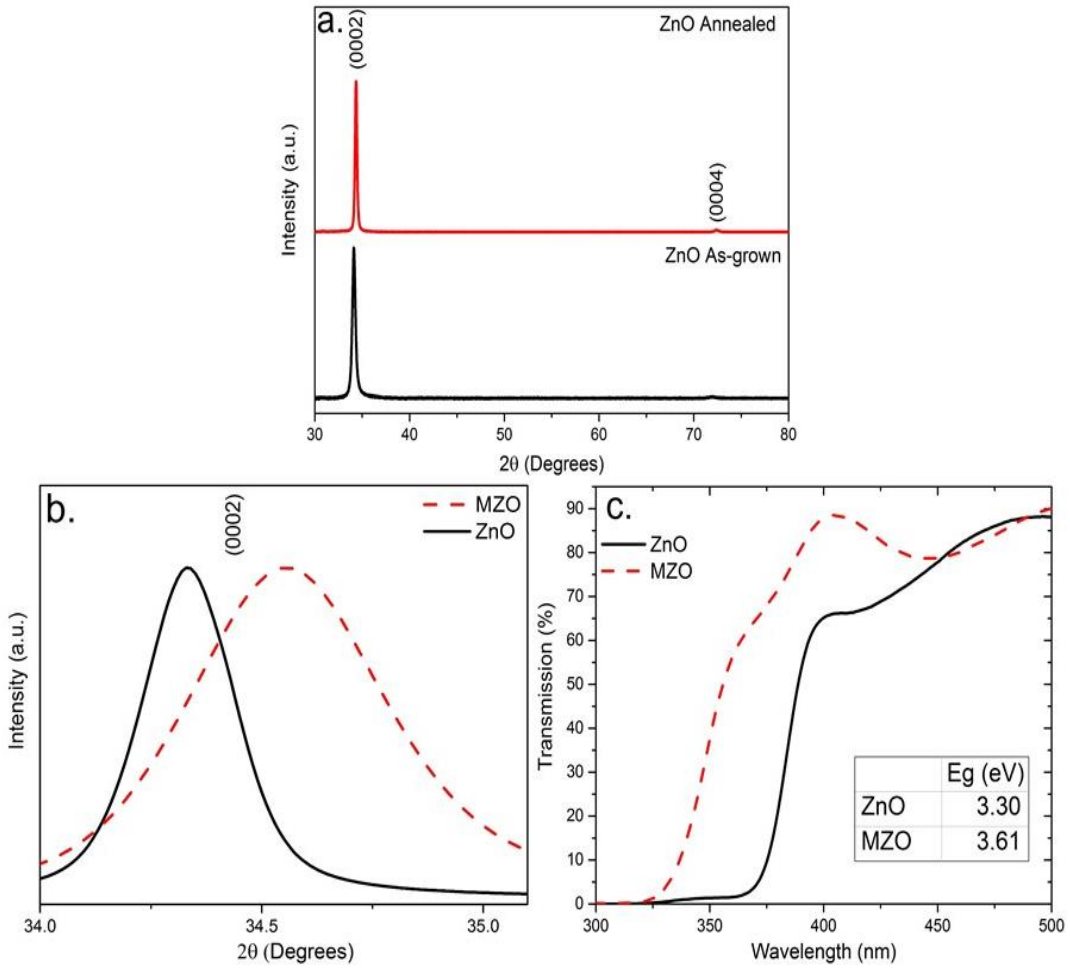

Figure 6.29: *a) XRD pattern of as-grown and 600°C annealed ZnO films. b) Zoomed in XRD pattern of the (0002) peak in the 600°C annealed MZO and ZnO layers and c) transmission spectra for MZO and ZnO films.*

Again, the incorporation of Mg into the MZO resulted in a displacement of the MZO (0002) peak relative to that of the ZnO (34.33° to 35.56°), confirming the expected reduction in the lattice parameter[16].The FWHM was also significantly higher for the (0002) peak in the MZO XRD pattern, 0.53°, compared to the FWHM for ZnO 0.25°. The FWHM values the grain size for the MZO and ZnO layers were evaluated using the Scherrer method (see Section 4.3.3) [19]. The MZO films were estimated to have a much smaller grain size than the ZnO films, 17.52 nm and 37.04 nm respectively. Figure 6.29c shows the optical transmission spectra produced for the MZO and ZnO layers and the calculated bandgaps

using the Tauc method are also shown in the inserted table. Incorporating Mg into the ZnO increases the bandgap from 3.30 eV to 3.61 eV for ZnO and MZO respectively.

Table 6.4: *ZnO and MZO films properties estimated from the XRD patterns in Figure 6.29a.*

	2θ (°)	**FWHM (°)**	**c (Å)**	**Grain Size (nm)**
ZnO	34.33	0.25	5.224	37.04
MZO	34.56	0.53	5.191	17.52

A series of $CdTe_{(1-X)}Se_X$ devices were produced using MZO and ZnO as the device window layer so a direct comparison could be made. Figure 6.30a-d shows the performance parameters for MZO/$CdTe_{(1-X)}Se_X$ and ZnO/$CdTe_{(1-X)}Se_X$ based devices. The *JV* and EQE responses for the highest efficiency contacts are shown in Figure 6.31a and b respectively.

MZO offers superior peak performance, when compared to ZnO the efficiencies being 11.30% and 9.11% respectively. The average J_{SC} value improved from 22.90 $mA.cm^{-2}$ to 25.43 $mA.cm^{-2}$, due to the wider bandgap of MZO (3.61 eV) compared to ZnO (3.30 eV) with improved collection at short wavelength clearly visible in the EQE response (Figure 6.30b). The V_{OC} significantly improved for the MZO based devices, with peak V_{OC} increasing from 0.66 V to 0.76 V. This improvement suggests that the MZO/$CdTe_{(1-X)}Se_X$ interface is of a superior quality when compared to the ZnO/$CdTe_{(1-X)}Se_X$ junction leading to a reduced level of recombination and thus an improved photo voltage [5,6,44]. It has been previously shown that ZnO forms a 'cliff' like band offset with CdTe. Such an interface can enhance recombination, limit the built in voltage and ultimately limit cell efficiency. Therefore, it is postulated that the observed V_{OC} increase of > 100 mV is due to the increased MZO bandgap resulting in the formation of a more favourable 'spike' like conduction band offset.

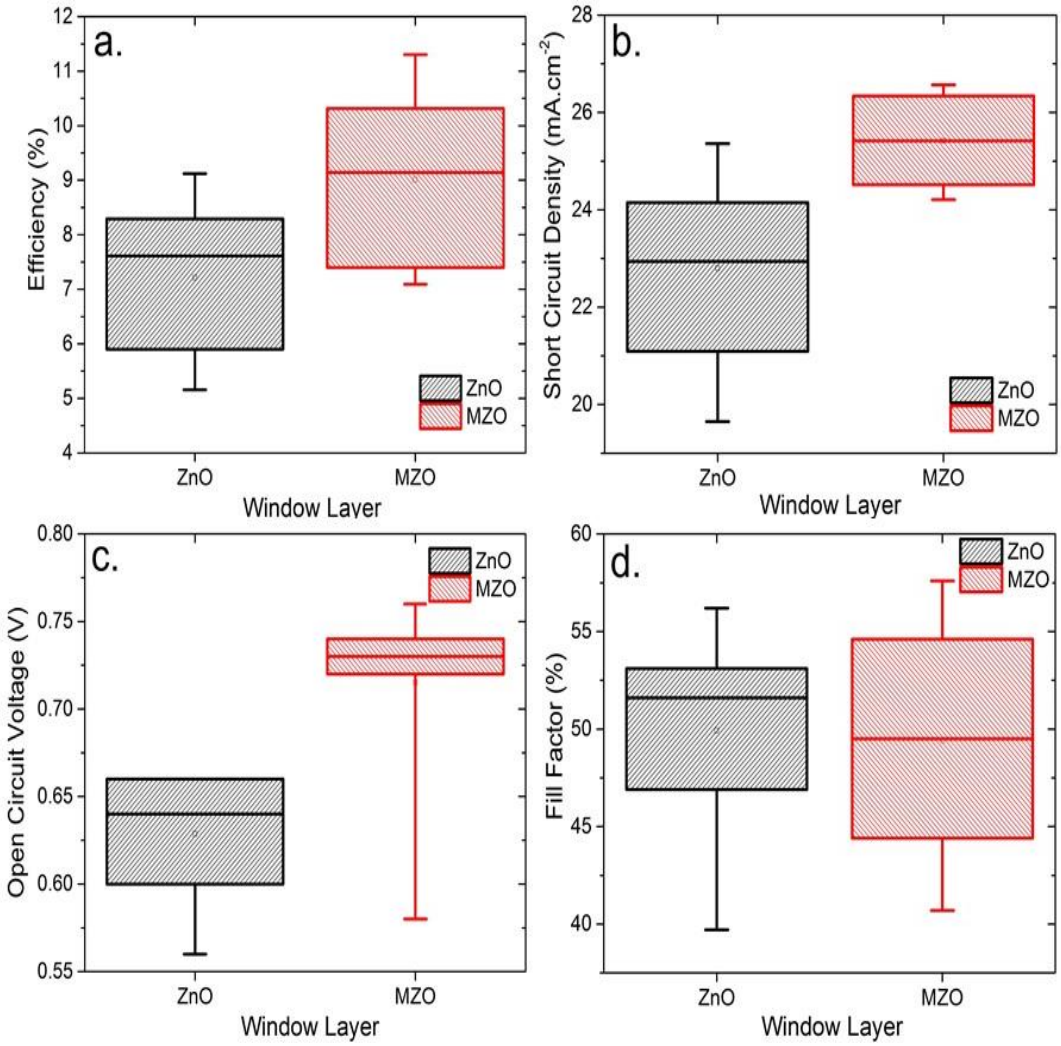

Figure 6.30: *Comparison of ZnO/$CdTe_{(1-X)}Se_X$ and MZO/$CdTe_{(1-X)}Se_X$ device performance parameters a) η, b) J_{SC}, c) V_{OC} and d) FF. N = 8.*

The results show the choice of partner layer is essential to achieving an optimal performance, with the MZO device showing improved efficiencies due to enhanced J_{SC} and V_{OC}. It is also worth noting that the MZO device shows an enhanced V_{OC} when compared to the SnO_2 alternatives (Section 5.4.2.4), increasing to 0.76 V from 0.72 V. However, the overall performance is reduced in comparison the SnO_2 based devices (11.3% compared to 13.5%) respectively due to reduced J_{SC} and *FF*. Further improvements could be achieved either by improving the properties of the MZO layer, such as conductivity or finding alternatives to this layer with an improved band alignment thus an improved photo voltage.

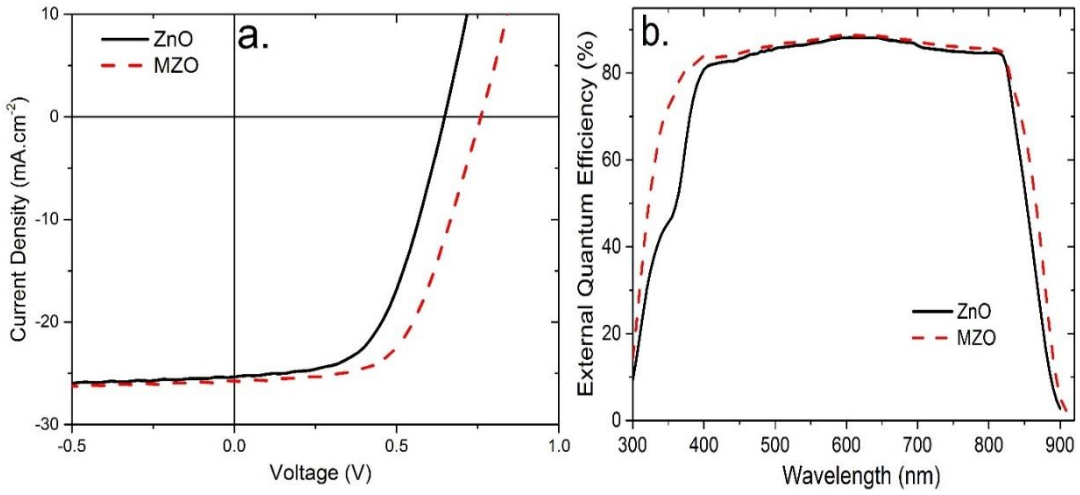

Figure 6.31: *JV (a) and EQE (b) response for the highest efficiency ZnO/$CdTe_{(1-X)}Se_X$ and MZO/$CdTe_{(1-X)}Se_X$ based devices.*

6.4. Discussion and conclusion

In this chapter, MZO was investigated for use as the n-type window layer for $CdTe_{(1-X)}Se_X$ based PV devices. MZO layers were fabricated using two different approaches, the film properties and device performance were then evaluated.

In Section 6.2 co-sputtered MZO layers for use in $CdTe_{(1-X)}Se_X$ based devices were fabricated and their influence on device performance evaluated. MZO layers with compositions varying from 0% (ZnO) to 25% were fabricated from ZnO and MgO targets.

Incorporation of Mg into the MZO films led to the expected increase in bandgap from 3.30 eV to > 3.80 eV and depending on the Mg content the bandgap could be somewhat tailored. It was also shown that Mg incorporation did not result in a significant change to the (0002) hexagonal ZnO wurzite phase with only a shift in the peaks position being observed, due to a reduction of the lattice parameters.

It was found that using co-sputtered MZO in $CdTe_{(1-X)}Se_X$ based devices was detrimental to performance with peak efficiency dropping from 9.11% for ZnO to 0.72% when a 20% Mg content was incorporated into the MZO films. In addition to this, the use of MZO resulted in the formation of an S-shape in the *JV* curves and a spike in *CV* doping density – depletion width profiles. This was indicative of a barrier to transport at the device interface

as a result of the increased bandgap and CB shift [5] and/or the increased resistivity of the MZO layers, resulting in reduced mobility and enhanced recombination [23]. Although the performance of MZO/$CdTe_{(1-X)}Se_X$ devices was reduced the V_{OC} did improve with increasing Mg content from 0.70 V to 0.78 V, when a 20% Mg content was incorporated into the MZO film. This improvement is likely due to better band alignment and enhanced built in voltage however, the enhanced resistivity of the MZO films leads to the formation of an S-shaped *JV* curve and a reduced performance.

In order to test whether the reduced performance was due to the high resistivity of the MZO layers, the deposition temperature was increased from RT to 400°C. It was shown that this led to the removal of the S-shape in the *JV* curve and an improved performance from 5% to > 8%. This suggested the conductivity of the MZO layer had been increased reducing the recombination and improving the device performance.

Results presented in Section 6.2 indicate there is a limit to the level of performance that can be achieved in co-sputtered MZO based devices despite the enhanced V_{OC}, possibly due to the increased resistivity of the MZO layers and the lack of the a single phase material.

In order to try and improve the performance further, MZO layers were fabricated from a single MZO target (11% MgO and 89% ZnO by wt composition) and their properties investigated. Following optimisation of the MZO layers a series of MZO/$CdTe_{(1-X)}Se_X$ based devices were produced.

MZO layers deposited at RT exhibited very little crystallinity and were mainly amorphous in nature. Increasing the deposition temperature improved the crystallinity of the films with the emergence of the (0002) diffraction peak. However, this didn't result in an improved device performance with similar efficiencies being achieved for $CdTe_{(1-X)}Se_X$ devices produced with MZO layers grown at RT and 400°C.

As deposition temperature had no influence on device performance, the influence of post growth annealing the MZO films in an air ambient was investigated. Annealing the

MZO layers at 600°C converted the amorphous MZO films into the crystalline hexagonal wurzite structure and resulted in a dramatic improvement to cell performance, from 3.79% to 11.30% for the 600°C annealed MZO films. This improvement was driven by an increase to all device performance parameters but primarily V_{OC} and *FF*, with the annealing step found to be essential in removing the S-shape from the MZO device *JV* response.

These results suggested of the annealed MZO layer formed a better interface with the $CdTe_{(1-X)}Se_X$ film than the amorphous as-deposited films, due to either, i) the reduction of dangling bonds at the interface resulting in a reduced level of recombination, ii) the conversion to a crystalline layer improved film conductivity, reducing the level of recombination and allowing carriers to tunnel through the energy barrier or, iii) the reduced bandgap of the annealed MZO layer lowered the energy barrier at the interface and produced a better band alignment with the $CdTe_{(1-X)}Se_X$ layer. It is likely that some combination of these factors that has produced superior performance in the annealed MZO/$CdTe_{(1-X)}Se_X$ devices.

Cross sectional STEM and EDS was used to assess the $CdTe_{(1-X)}Se_X$ film quality throughout the device structure. CdTe deposition onto the CdSe/MZO layers resulted in uniform coverage with no voids found at the interface. This was in contrast with the SnO_2/$CdTe_{(1-X)}Se_X$ (Section 5.4.2.2) devices where large voids were present at the interface. The absence of voids could also be the possible cause for the enhanced V_{OC} in the MZO based devices. There was again little evidence of a significantly graded Se content present in $CdTe_{(1-X)}Se_X$ film, with a high Se content at the front device interface and minimal Se towards the device back surface.

MZO and ZnO layers were directly compared and their performance as the device window layer was evaluated. The use of MZO rather than ZnO lead to an almost 2% increase in cell efficiency. As Mg incorporation into the MZO layer led to an increase to the observed bandgap, J_{SC} was enhanced, with the device photo response improving in the short

wavelength region. The V_{OC} is also significantly improved for the MZO devices compared to the ZnO devices, 0.76 V and 0.66 V respectively, indicating less recombination and a superior quality interface.

Despite a performance of over 10% being achieved, there still remains significant scope for further improvements to be made as the V_{OC} is still well below the theoretical limit for CdTe devices and the *FF* is also low compared to state-of-the-art devices. Improvements to these parameters will likely come from further optimisation of the window layer/$CdTe_{(1-X)}Se_X$ interface either through further optimisation of the MZO layer, such as annealing in different atmospheres and doping, or replacing it with a feasible alternatives[45,46].

6.5. References

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7. Conclusion and future Work

7.1. Research overview and outcomes

The main aim of this thesis was to investigate ways to optimise the photo current produced by CdTe PV devices whilst retaining device photo voltage and *FF* by incorporating Se into the CdTe layers and the subsequent use of MZO as the window layer to enhance the device V_{OC} in $CdTe_{(1-X)}Se_X$ devices. The focus was on replacing the conventional CdS/CdTe architecture and investigating feasible alternatives with the two main subjects being investigated in this thesis were; 1) Se incorporation into the CdTe layer leading to the formation of the lower band gap $CdTe_{(1-X)}Se_X$ phase (Chapter 5) and 2) the use of MZO as the n-type window layer in CdSe/CdTe based devices (Chapter 6). During the course of this work a number of different device structures were investigated including CdS:O/CdTe, CdS:O/CdSe/CdTe, CdS/CdSe/CdTe, SnO_2/CdSe/CdTe, ZnO/CdSe/CdTe, TiO_2/CdSe/CdTe, FTO/CdSe/CdTe and MZO/CdSe/CdTe, Table 7.1 summaries the peak device efficiency achieved for each device structures fabricated in this work.

In Chapter 5 Section 5.2.2 it was shown that the band gap of CdS could be increased via the incorporation of oxygen into the films. By adding CdS:O layers into the CdTe devices the performance could be enhanced with improvements to the J_{SC} and V_{OC} being observed. However, it was also found that the performance and J_{SC} remained limited as losses at short wavelengths were still observed due to recrystallisation at the interface. There was also the formation of an energy barrier resulting in S-shaped *JV* responses for a higher oxygen content, therefore an alternative approach required investigation.

Table 7.1: *Peak performance parameters achieved for all the PV device structures utilised in this work.*

Device Structure	η (%)	J_{SC} (mA.cm^{-2})	V_{OC} (V)	FF (%)
FTO/CdSe/CdTe	11.32	29.80	0.66	57.50
SnO_2/CdSe/CdTe	13.50	29.60	0.72	63.30
ZnO/CdSe/CdTe	9.50	28.80	0.66	50.20
TiO_2/CdSe/CdTe	6.10	27.50	0.74	30.00
MZO/CdSe/CdTe	11.30	25.80	0.76	57.60
CdS/CdTe (annealed)	14.00	25.60	0.82	66.40
CdS (15nm)/CdSe/CdTe	11.80	23.60	0.73	68.20
CdS:O/CdTe	12.01	22.77	0.81	65.11
CdS/CdTe (unannealed)	9.96	18.73	0.78	68.16
CdS (100nm)/CdSe/CdTe	7.09	15.63	0.76	59.68
CdS:O/CdSe (100 nm)/CdTe	6.99	15.26	0.74	61.91

It had been previously shown that the incorporation of CdSe layers into the CdTe device structure could enhance device photo response at both short and long wavelengths. Therefore, the incorporation of CdSe into CdS:O/CdTe and CdS/CdTe devices was investigated (Section 5.2.3 and Section 5.3). It was found that adding any amount of CdSe into this device architecture was detrimental to performance, with extensive losses being observed at short wavelengths, although there was some evidence of a the lower band gap $CdTe_{(1-X)}Se_X$ phase being formed due to an enhancement to the devices photo response at long wavelength. STEM and EDX was used to show that the short wavelength losses were due to CdS and CdSe interdiffusion resulting in the formation of a $CdS_{(1-X)}Se_X$ phase which is of a lower band gap compared to CdS and thereby increased parasitic absorption. Cross sectional STEM also revealed that large voids formed at the CdS/CdSe/CdTe interface due to excessive intermixing between these layers. EBIC was used to show that the formation of the $CdS_{(1-X)}Se_X$ phase was effectively resulting in a buried p-n junction thus reducing the devices photo response and ultimately performance.

7. Conclusion and future work

Alterations to device processing was attempted in order to try and rectify the problems associated with the formation of the $CdS_{(1-X)}Se_X$ phase and aid Se diffusion into the CdTe layer. Increasing the chlorine treatment time resulted in no improvement to the devices photo response, the inference here being that the chlorine activation step wasn't having a significant influence on the S, Se and Te interdiffusion. Therefore, an in-situ CSS post CdTe growth anneal was developed which improved the devices photo response at short wavelength and led to an improvement to device efficiency, suggesting that the post growth anneal did aid the Se and Te interdiffusion. However, despite the post growth anneal having some impact on device J_{SC} and performance, the efficiency remained fundamentally limited due to the formation of the $CdS_{(1-X)}Se_X$ phase. This could be somewhat rectified by using a very thin CdS layer (≈ 15 nm) reducing the $CdS_{(1-X)}Se_X$ layer thickness and increasing device J_{SC}.

As it was found that the formation a $CdS_{(1-X)}Se_X$ phase was an unavoidable limit to performance when using a CdS/CdSe structure, ways to remove the CdS layer from the device structure were investigated. Initially the CdS layer was replaced with a SnO_2 partner layer for CdSe/CdTe devices (Section 5.4). This led to significant enhancements to the devices photo response particularly at short wavelength, with close to optimal J_{SC} values being achieved (29.62 mA cm^{-2}), the only losses being reflections from the glass. Again an in-situ post CdTe growth anneal was essential in achieving an optimal device performance, with the annealing aiding the conversion from the photo inactive CdSe wurzite phase to the photoactive zincblende $CdTe_{(1-X)}Se_X$ structure resulting in the high device photo response. STEM and EDS was used to analyse Se and Te distributions throughout the CdTe layer, demonstrating that the conversion of the CdSe layer to the $CdTe_{(1-X)}Se_X$ was as a result of Te diffusion into the CdSe layer rather, than Se diffusion into the CdTe layer. Large voids at the $SnO_2/CdTe_{(1-X)}Se_X$ were still observed due to the extensive intermixing observed between the CdSe and CdTe layers. Whilst the formed $CdTe_{(1-X)}Se_X$ phase was now

photoactive the Se content was very high at the near interface and low in the CdTe layer. This indicated that an efficiently graded band gap has not been achieved and it was therefore unlikely the minority carrier lifetimes would've been improved. The use of a sputtered CdSe layer combined with CdTe CSS deposition to control the Se diffusion throughout the CdTe layer proved challenging due to the competing demands of diffusion control whilst preserving an optimal CdTe grain structure. Alternative approaches will likely need to be investigated such as, co-sputtered or co-sublimated $CdTe_{(1-X)}Se_X$ layers. This would enable the formation of a controlled $CdTe_{(1-X)}Se_X$ layers but would still require interdiffusion with a CdTe layer to achieve a graded structure.

Despite the limitations of the SnO_2/CdSe/CdTe device structure a, performance of over 13% was achieved with high J_{SC} and FF values. The V_{OC} of the SnO_2/CdSe/CdTe based devices was reduced compared to CdS/CdTe devices, 0.72V and 0.82V respectively. This was deemed to be an indication that the SnO_2/$CdTe_{(1-X)}Se_X$ interface was of an inferior quality compared CdS/CdTe interface due to some combination of a poorer band alignment, higher lattice mismatch and the excessive void formation at the interface. Despite the high performance achieved for SnO_2/CdSe/CdTe devices there remains significant scope to improve the V_{OC}. The route to achieving this will be by improving the Se grading in the CdTe, achieving greater control over the CdTe growth so as to avoid the formation of voids at the interface and replacing SnO_2 as the device window layer with viable alternatives.

Section 5.5 focused on replacing SnO_2 with a number of alternatives, TiO_2, ZnO and FTO. It was demonstrated that the n-type window layer had a significant influence on device performance, particularly affecting V_{OC}, with 0.74 V, 0.66 V and 0.66 V being achieved for the TiO_2, ZnO and FTO layers respectively. Despite the improved V_{OC} the device structures utilising TiO_2 also demonstrated an S-shape in their *JV* response, indicating a barrier to extraction at the interface and limited device performance. This work demonstrated the importance of the choice of partner layer for $CdTe_{(1-X)}Se_X$ device

performance and implied a number of overlapping requirements i) high bandgap, ii) suitable band alignment and iii) appropriate conductivity. Any of these being sub-optimal will seriously compromise device performance, making identifying suitable layers a challenge.

It had been reported in the literature that MZO is the ideal n-type partner layer for $CdTe_{(1-X)}Se_X$ PV devices in part due to the ability to tailor the materials properties. Chapter 6 reported on the optimisation of MZO produced via two different approaches and the subsequent influence on device performance.

In Section 6.2 MZO layers were fabricated via a co-sputtered approach from ZnO and MgO targets. It was demonstrated that incorporating Mg into ZnO extended the band gap to well beyond that of SLG and the material remained in the crystalline wurzite phase, with Mg substitution onto the Zn sites. It was found that incorporating Mg into the ZnO layers had a detrimental effect on device performance regardless of the Mg content utilised. The drop in performance was primarily due to the production of S-shaped curves in the devices *JV* response, indicating that the increased band gap and/or the higher resistivity of the MZO layers resulted in a barrier to carrier extraction higher.

The problem could be rectified to a point by increasing the temperature of the MZO deposition, which led to the removal of the S-shape and some increase in performance. However, the performance was still lower than equivalent ZnO based devices. As no band gap shift was observed with increased deposition temperature, it was postulated that the increased performance was due to increased conductivity of the MZO layers meaning photo generated carriers could overcome the extraction barrier following annealing.

As layers deposited via a co-sputtered process can have an uneven distribution of dopants throughout the layer, it was hypothesised that switching from fabricating MZO layers via co-sputtered approach to a single target approach would yield an enhanced performance. Section 6.3 reported on the optimisation of MZO layers fabricated from a

MZO single target (11% MgO and 89% ZnO by wt) and their incorporation into $CdTe_{(1-x)}Se_x$ devices.

It was shown that annealing the MZO layers post growth at 600°C in an air ambient was essential to improve device performance. As grown MZO layers exhibited a mainly amorphous nature, following annealing the films recrystallized into a wurtzite structure. Devices produced using as-deposited MZO layers again resulted in the formation of S-shaped *JV* curves and very low performance. Devices produced using MZO which had been post growth annealed exhibited a much higher performance (11.3%) and removal of the S-shape. It was again proposed that this improvement was due to improved conductivity of the MZO layers, allowing carriers to overcome the extraction barrier. STEM and EDX were used to show that growth on MZO, rather than SnO_2, led to a reduction in the number voids being formed at the interface. Whilst relatively uniform coverage of the MZO layer was observed, the lack of Se grading in the $CdTe_{(1-x)}Se_x$ was still observed in the MZO samples. The MZO/$CdTe_{(1-x)}Se_x$ device structure demonstrated a significantly higher V_{OC} when compared to SnO_2 and ZnO 0.76 V, 0.72 V and 0.66 V respectively. This was suggestive that the MZO/$CdTe_{(1-x)}Se_x$ interface was of a superior quality, has a reduced level of recombination and higher V_{bi}.

Overall the results presented in this thesis demonstrate the feasibility of $CdTe_{(1-x)}Se_x$ based PV devices with over a 10% efficiency being achieved for a variety of different device architectures. The data presented also demonstrates that additional improvements to device performance will likely be achieved through further optimisation of the device junction properties either by improving the MZO/$CdTe_{(1-x)}Se_x$ interface or by finding an alternative window layer structure with a better band alignment and reduced level of recombination. Improving the device V_{OC} beyond that obtainable for the CdS/CdTe devices remains the primary challenge.

7.2. Possible future work

7.2.1. Further optimisation of the Se distribution

A recurring theme most of the data presented in this thesis was that a graded Se content hadn't been achieved, with a very high Se content at the front device interface and very little in the bulk. The main area for future work would be in trying to achieve an efficient Se grading throughout the $CdTe_{(1-X)}Se_X$ material and therefore a graded band gap. This could potentially be done via number of different of routes either by altering the CdSe and CdTe growth in order to try and promote Se diffusion rather than Te diffusion into the CdSe layer or by producing the $CdTe_{(1-X)}Se_X$ layer via a different route. Forming the $CdTe_{(1-X)}Se_X$ layer via co-sputtered or co-sublimated route will likely result in more Se distribution and a finer control of the Se diffusion throughout the CdTe layer during the CSS deposition. This would allow the Se content to be varied during $CdTe_{(1-X)}Se_X$ growth and allow for a graded Se content to be achieved.

7.2.2. Investigating early stage $CdTe_{(1-X)}Se_X$ formation

Large voids were found to be present at the $SnO_2/CdTe_{(1-X)}Se_X$ interface however, little void formation was observed at the $MZO/CdTe_{(1-X)}Se_X$ interface. Therefore it is clear the window layer is having an influence on early stage nucleation and growth of the $CdTe_{(1-X)}Se_X$ phase. One route to further improving the performance of the $CdTe_{(1-X)}Se_X$ based devices would be to have a greater understanding of the initial nucleation of the $CdTe_{(1-X)}Se_X$ layer and monitor how different window layers and device processing effects the films coverage and void formation. This could be done using a variety of techniques such as, TEM, SEM and atomic force microscopy (AFM) to try an assess how initial $CdTe_{(1-X)}Se_X$ growth occurs however, this would be challenging as the device interface is buried, i.e away from the surface, and therefore trying the analyse something that is representative of real device is difficult.

7.2.3. Optimisation of the MZO film properties

Post MZO growth annealing had the biggest influence on device performance, additional improvements will likely come from improving the properties of the MZO layer and thus the MZO/$CdTe_{(1-X)}Se_X$ junction. Altering the MZO processing conditions such as, varying the O_2 content during sputtering growth and post growth annealing the MZO layers in a variety of different atmospheres such as in nitrogen and hydrogen are as yet unexplored. The MZO/$CdTe_{(1-X)}Se_X$ device also exhibited a high R_S and low *FF* indicating the MZO films are still highly resistive. Exploration of routes to increase the conductivity of the MZO films possibly through the addition of dopants such as, Al, Ga and In would seem a logical next step.

7.2.4. Alternative device architectures

This thesis has demonstrated changing the device architecture significantly alters the device performance. If a more ideal device structure can be found then a high device performance will also be established. This could be achieved by improving the band alignments between the $CdTe_{(1-X)}Se_X$ layer and the device n-type window layer meaning a better V_{OC} and V_{bi} would be realised. Possibly future work from this project would be the a more materials focussed investigation of alternative window layers to MZO, i.e. identifying candidate materials and assessing their band alignment with $CdTe_{(1-X)}Se_X$ using XPS or HAXPES.