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Detecting Missing Capacitors by Load Sensing

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Detecting Missing Capacitors by Load Sensing

ABSTRACT

Factory testing on a production line can uncover several types of device failures. However, certain subtle failures can be masked from test procedures only to be discovered too late, e.g., by the customer. An example of such a failure is a missing bulk capacitor in circuits such as amplifiers, regulators, etc. Such a failure can go undetected at a factory due to the presence of smaller capacitors that have a marginally compensating effect. This disclosure describes techniques to detect missing bulk capacitors on circuit boards by inserting a simulated load resistance and measuring the decay time of an injected test voltage. A missing bulk capacitor is detected by decay times that are much faster than normal or expected.

KEYWORDS

- Factory testing
- Bulk capacitor
- Functional test
- Circuit board test
- Time constant
- Decay time
- Discharge time
- RC circuit
- Device under test (DUT)

BACKGROUND

Factory testing on a production line can uncover several types of device failures. However, certain subtle failures can be masked from test procedures only to be discovered too late, e.g., by the customer. Such failures are seen when the device is stressed in a certain fashion, which typical factory test procedures may not exercise. An example of such a failure is a missing bulk (electrolytic) capacitor that serves as electrostatic energy storage in circuits subject to load transients, e.g., amplifiers, regulators, etc. Such a failure can go undetected at a factory due to the presence of smaller capacitors that have a marginally compensating effect.

DESCRIPTION

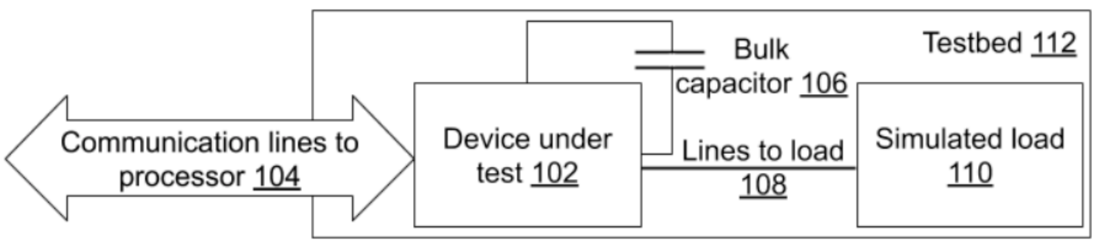

Fig. 1: Factory test configuration

Fig. 1 illustrates a typical factory test configuration for a device under test (DUT, 102). The DUT can be, for example, a printed circuit board that serves as an amplifier, a regulator, etc. The DUT includes a bulk capacitor (106), the presence of which is tested per the techniques of this disclosure. The bulk capacitor can be used to provide transient power, e.g., to a class-D amplifier, to prevent collapse and rebooting of the device during transient periods of high power demand, etc. The DUT typically has communication lines to a processor (104) and lines (108) to load. The load can be, for example, a speaker, which is typically not connected to the DUT during the factory test. The DUT and associated test components rest on a production-line testbed (112), which provides access to internal and external signals of the DUT, and can test multiple DUTs either simultaneously or on a rolling basis.

Per the techniques of this disclosure, a simulated load (110) is connected to the DUT. For example, a load for a speaker can be provided as a resistor with similar impedance as the speaker. A short-duration test signal or electrical stimulus, e.g., a sine wave or a square impulse, is injected into the DUT. The time for the test signal to decay (or the capacitor to discharge) is measured at the load.

The time variation of the load-voltage V is given by $V=V_0\exp(-t/RC)$, where V_0 is the initial voltage, t is time, R is the load resistance, and C is the capacitance to be tested for. Therefore, a quick decay, e.g., a low time constant for the RC circuit formed by the simulated load and the bulk capacitor, is indicative of a missing bulk capacitor. A slow decay, e.g., a high time constant for the RC circuit formed by the simulated load and the bulk capacitor, is indicative of a present and functioning bulk capacitor. The difference in decay times between the missing-capacitor and normal-capacitor cases can be large enough, e.g., in a 10:1 ratio, to be easily discernible. To get a pass/fail threshold test on the decay time, multiple tests are run on DUTs with and without bulk capacitors to get a decay-time distribution, and a threshold is established to detect defective parts, e.g., to a three-sigma confidence.

An advantageous location for screening for missing capacitors can be the board-level functional test station of the production line. Such test stations can power the DUT using power management units (PMU) that have varying output capacitances depending on the design of the PMU.

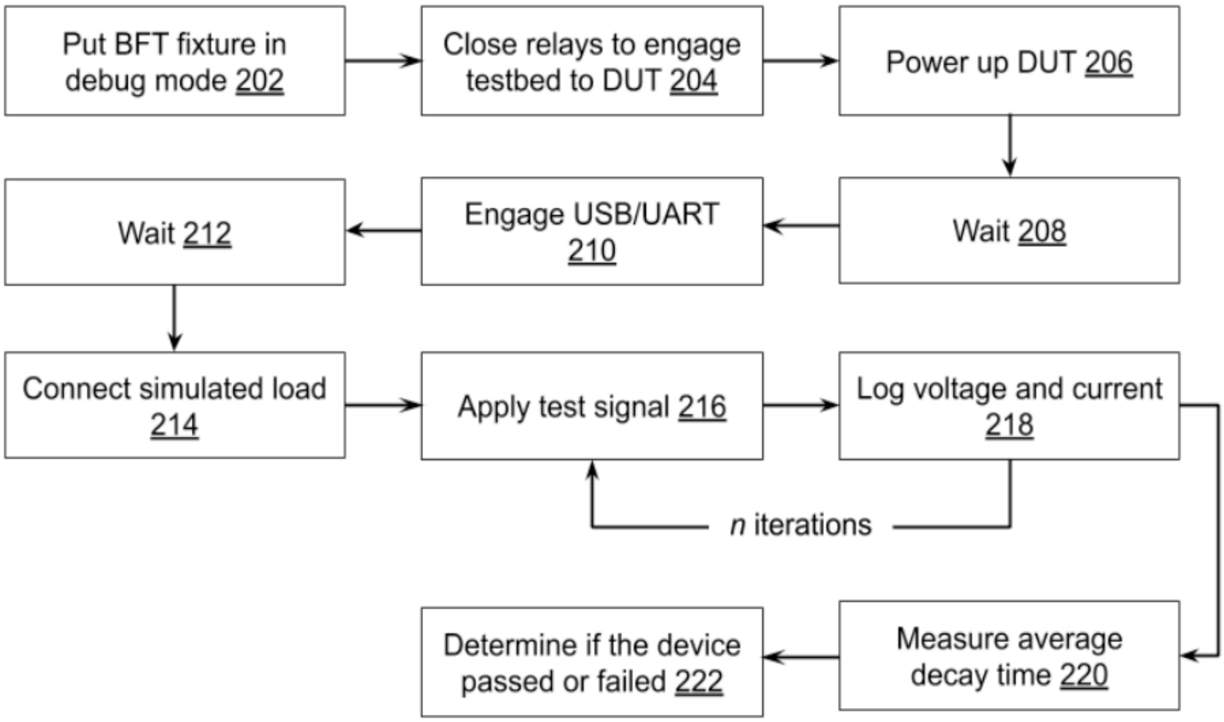

Fig. 2: Factory test workflow

Fig. 2 illustrates a factory test workflow to detect missing bulk capacitors, per the techniques of this disclosure. The board-level functional test (BFT) station fixture is put in debug mode (202). Relays are closed to engage the testbed to the DUT (204). The DUT is powered up (206). After a suitable wait time (208), e.g., five seconds, the USB or UART is engaged (210). After another wait time (212), a simulated load, e.g., a 4 Ohm resistor that mimics a speaker, is connected at the output of the DUT (214).

A test signal, e.g., a short-duration sine wave, is applied (216), e.g., by playing from a file. The voltage and current are logged (218). The test signal application and voltage/current logging procedures are repeated over *n*, e.g., five, iterations. The average decay time is measured (220). A determination is made whether the device passed or failed the test (222) based respectively on whether the measured decay time is above or below the pass/fail threshold.

CONCLUSION

This disclosure describes techniques to detect missing bulk capacitors on circuit boards by inserting a simulated load resistance and measuring the decay time of an injected test voltage. A missing bulk capacitor is detected by decay times that are much faster than normal or expected.