

**A LINEAR HIGH-EFFICIENCY MILLIMETER-WAVE  
CMOS DOHERTY RADIATOR LEVERAGING ON-  
ANTENNA ACTIVE LOAD-MODULATION**

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The Academic Faculty

by

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School of Electrical and Computer Engineering

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**A LINEAR HIGH-EFFICIENCY MILLIMETER-WAVE  
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ANTENNA ACTIVE LOAD-MODULATION**

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## LIST OF SYMBOLS AND ABBREVIATIONS

CW	Continuous Wave
DPD	Digital Pre-Distortion
FoV	Field-of-View
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratios
PAE	Power Added Efficiency
PBO	Power Back Off
$P_{SAT}$	Saturation Output Power
$P_{1dB}$	Output Power at 1dB Gain Compression



## SUMMARY

This thesis presents a Doherty Radiator architecture that explores multi-feed antennas to achieve an on-antenna Doherty load modulation network and demonstrate high-speed high-efficiency transmission of wideband modulated signals. On the passive circuits, we exploit the multi-feed antenna concept to realize compact and high-efficiency on-antenna active load modulation for close-to-ideal Doherty operation, on-antenna power combining, and mm-Wave signal radiation. Moreover, we analyze the far-field transmission of the proposed Doherty Radiator and demonstrate its wide Field-of-View (FoV). On the active circuits, we employ a GHz-bandwidth adaptive biasing at the Doherty Auxiliary power amplifier (PA) path to enhance the Main/Auxiliary Doherty cooperation and appropriate turning-on/-off of the Auxiliary path. A proof-of-concept Doherty Radiator implemented in a 45nm CMOS SOI process over 62-68GHz exhibits a consistent  $1.45\text{-}1.53\times$  PAE enhancement at 6dB PBO over an idealistic class-B PA with the same PAE at  $P_{1\text{dB}}$ . The measured Continuous-Wave (CW) performance at 65GHz demonstrates 19.4/19.2dBm  $P_{\text{SAT}}/P_{1\text{dB}}$  and achieves 27.5%/20.1% PAE at peak/6dB PBO, respectively. For single-carrier 1Gsymb/s 64-QAM modulation, the Doherty Radiator shows average output power of 14.2dBm with an average 20.2% PAE and -26.7dB EVM without digital predistortion. Consistent EVMs are observed over the entire antenna FoV, demonstrating spatially undistorted transmission and constant Doherty PBO efficiency enhancement.

## CHAPTER 1: INTRODUCTION

Radiators in modern mm-Wave communication transmit high-speed modulated signals with large peak-to-average power ratios (PAPR) for high spectrum efficiency and data rate [1]-[9]. This poses increasingly stringent requirements on power amplifiers (PAs)/transmitters (TXs) for power back-off (PBO) efficiency, linearity, and modulation bandwidth.

Popular PA/TX architectures for high PBO efficiency include Envelope Tracking (ET), Outphasing, Doherty, and their variants. Using an envelope detector and supply modulators, the ET PA modulates the supply voltage to track the input power level [10]-[13]. However, the ET PA's PBO efficiency is practically limited by the power efficiency and dynamic range of the supply modulator. Designing high-efficiency supply modulators with GHz modulation is challenging in practice, and most ET PAs can only handle <200MHz modulation bandwidth [10]-[13]. The outphasing PA, on the other hand, vectorially combines constant-envelope phase-modulated PAs for varying envelopes [14]-[20]. It demands extensive digital signal-processing (DSP) and digital pre-distortion (DPD) to generate phase-modulated outphasing signals with a typical  $\times 5\sim 7$  bandwidth expansion [21][22], resulting in significant computation power and low system efficiency for GHz modulations.

In contrast, the Doherty PA employs Main/Auxiliary PAs to achieve active load modulation and an "RF-in-RF-out" solution that supports wideband modulations with low DPD overhead [23]-[41]. Several mm-Wave Doherty PAs have been reported at 60-80GHz [39][40]. However, these mm-Wave Doherty PAs only have marginal PAE enhancement

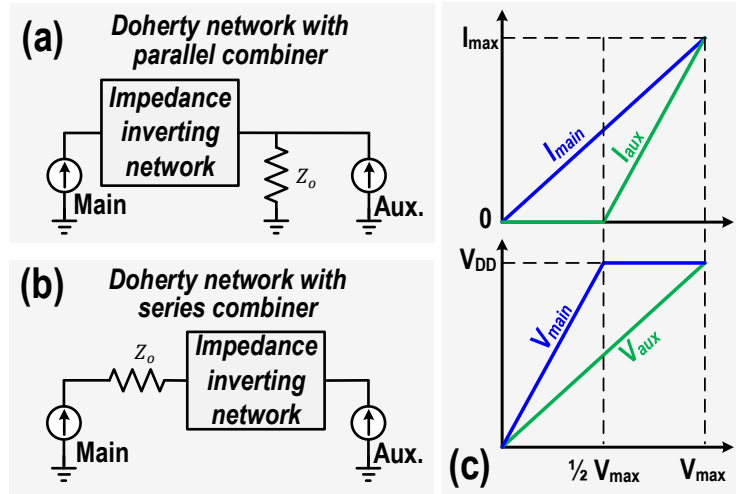
over an idealistic class-B PA, mainly due to non-ideal and lossy Doherty output networks and imperfect Main/Auxiliary PA cooperation.

We propose a Doherty Radiator architecture that explores an on-chip multi-feed antenna as part of the Doherty output network to achieve antenna-based close-to-ideal load modulation and high-speed high-efficiency transmission of large PAPR mm-Wave signals without any DPD. Additionally, we employ a GHz-bandwidth adaptive biasing circuit in the Auxiliary path to radically enhance Main/Auxiliary cooperation and thus improves the PBO PAE over the entire operation frequency. Moreover, contrary to the reported spatial Outphasing TX [42] or spatial IQ combining TXs [43] which are highly directional and support undistorted modulations over limited transmission angles, the proposed Doherty Radiator achieves high-speed and undistorted modulation over the entire antenna Field-of-View (FoV), easing TX/RX alignment in practical mm-Wave communication systems.

The thesis is organized as follows. Chapter 2 reviews the parallel and series Doherty topologies. Chapter 3/4 present the proposed Doherty Radiator with its design approach, theoretical derivation, and simulations. Chapter 5 demonstrates a proof-of-concept 62-68GHz Doherty Radiator in a 45nm CMOS SOI process. Chapter 6 shows the measurement results, and chapter 7 presents the conclusion of the thesis.

## CHAPTER 2: DOHERTY PA ARCHITECTURES

To achieve PAs with high PBO efficiency, William H. Doherty in 1936 proposed two generic architectures that use either parallel or series power combiners to construct active load modulation networks [23] (Fig. 1). We summarize the differences of series and parallel Doherty architectures on their circuit realization, matrix representation, and active load modulation characteristics in Fig. 2.

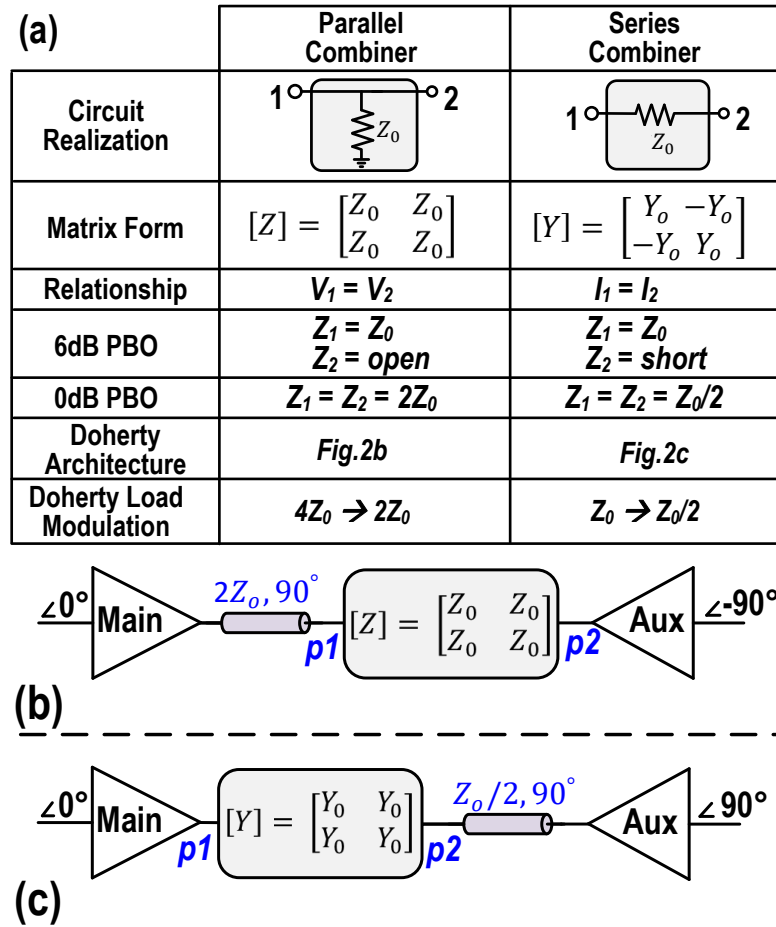


**Figure 1. Generic active load modulation PA architectures proposed by William H. Doherty [23] with (a) parallel Doherty architecture, (b) series Doherty architecture, and (c) desired Doherty current-voltage trajectory.**

### 2.1 Parallel and Series Doherty PA Architecture

A two-port parallel combiner exhibits a non-singular  $[Z]$  matrix with its voltage relationship  $V_1 = V_2$ . For Doherty PA operation below 6dB PBO, port 2 is open-circuited and port 1 sees an impedance  $Z_o$ . At 0dB PBO, i.e., maximum output power, both ports are on and contribute equally to the combiner, and thus each sees a load impedance of  $2Z_o$ . To complete the parallel Doherty structure, an additional  $\lambda/4$  impedance inverter with  $2Z_o$

characteristic impedance is added to port 1 so that the Main PA sees a reduced load impedance versus output power ( $4Z_o$  at or below 6dB PBO and  $2Z_o$  at 0dB PBO), which extends the Main PA linearity and maximizes its efficiency, achieving the desired parallel Doherty operation [Fig. 2(b)].

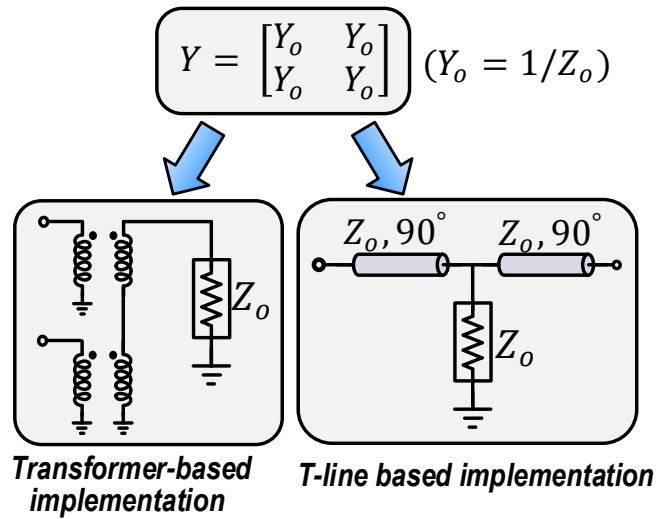


**Figure 2. (a) Comparison between parallel and series combiner (b) Doherty architecture for parallel combiner (c) Doherty architecture for series combiner.**

On the contrary, a two-port series combiner demonstrates a non-singular  $[Y]$  matrix with its current relationship  $I_1=I_2$ . Below 6dB PBO, port 2 is short-circuited such that port 1 sees the total load impedance of  $Z_o$ . At 0dB PBO, both ports are on and each should see a load of  $Z_o/2$  for symmetrical power driving. By duality, forming a series Doherty architecture

requires adding a  $\lambda/4$  impedance inverter with characteristic impedance of  $Z_o/2$  at port 2 [Fig. 2(c)]. At deep PBO (or below 6dB PBO), the  $\lambda/4$  line converts the open-circuited termination of the turned-off current-mode Auxiliary PA to a short termination at port 2 of the series combiner so that the Main PA sees a load impedance  $Z_o$ . At 0dB PBO, both Main and Auxiliary PAs see a  $Z_o/2$  load for symmetrical power driving. Overall, from deep PBO to 0dB PBO, the Main PA load impedance decreases from  $Z_o$  to  $Z_o/2$ , while the Auxiliary PA load reduces from  $\infty$  to  $Z_o/2$ , demonstrating the desired series Doherty operation [Fig. 2(c)].

## 2.2 Challenges of Doherty PA Implementation at Mm-Wave Frequencies



**Figure 3. Implementation of the series power combiner by employing either transformers or transmission lines.**

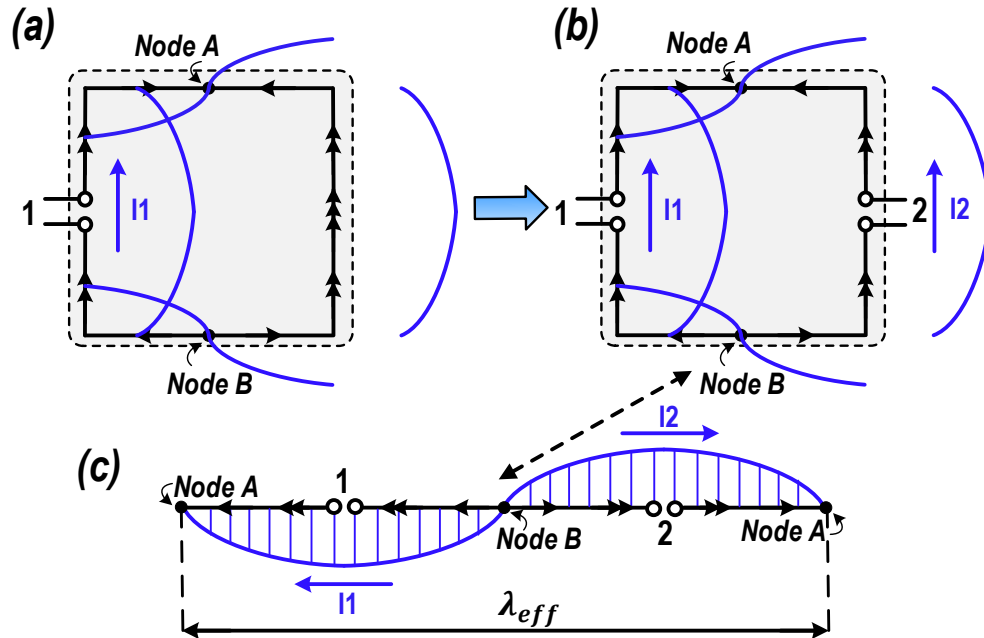
Compared to the parallel combiner that intrinsically scales up the load impedance, the series combiner naturally scales down the load, which is more appealing for voltage-limited silicon process. However, at mm-Wave frequencies, implementation of a series combiner entails practical challenges. To realize the  $[Y]$  matrix of the series combiner, commonly-

used techniques include transformer-based and transmission line-based (T-line-based) implementations (Fig. 3). The transformer-based approach utilizes two or more coils to share the magnetic flux in series for power combining [44] [45]. At mm-Wave frequencies, the transformer series combiners generally exhibit strong coil-to-coil capacitive coupling, resulting in imperfect balancing and severely compromised series combiner [Y] matrix behavior. On the other hand, the T-line-based structures involve two  $\lambda/4$  lines that inherently demand an extensive area and do not naturally support differential PA implementations. Overall, the above challenges limit implementations of efficient series Doherty output network at high mm-Wave frequencies.

## CHAPTER 3: ON-ANTENNA DOHERTY ARCHITECTURE

At high mm-Wave frequencies, antenna sizes are often comparable to active circuits. Conventional off-chip antennas would need packaging technologies with fine feature sizes and low parasitic effects and signal loss. Thus, directly integrating antennas on-chip with front-end circuits becomes a viable option at high mm-Wave regime. Moreover, this close antenna-electronics co-design opens the door to various circuit topologies to achieve unprecedented performance[46]-[60].

### 3.1 Proposed On-Antenna Series Combiner Structure

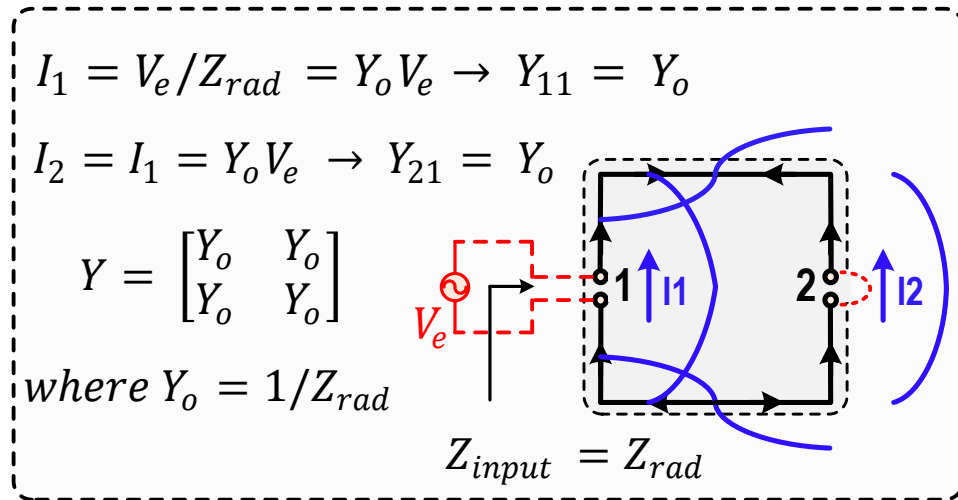


**Figure 4. (a) Single-feed wire loop antenna (b) Proposed multi-feed antenna structure (c) Standing wave current distribution. The blue lines represent the standing-wave current distribution inside the antenna.**

In this work, we leverage this concept of antenna-electronics co-design and exploit a multi-feed antenna [55][56] to realize a mm-Wave Doherty Radiator. On fully integrated silicon,



the proposed network performs signal-processing of the mm-Wave Si PA outputs to simultaneously achieve on-antenna power combining, radiation, and Doherty active load modulation with high-efficiency and high-linearity. As a specific example, a resonant multi-feed one- $\lambda$  wire loop antenna is explored to construct a series Doherty output network (Fig. 4). Starting from a conventional single-feed loop antenna [Fig. 4(a)], we open a new symmetrical feed at the opposite side of the loop to form the multi-feed antenna structure [Fig. 4(b)]. At resonance, the standing wave current distribution is formed inside the loop such that the currents peak at two input locations with the same magnitude and phase ( $I_1 = I_2$ ), while the current nulls happen at the middle nodes A and B ( $I_A=I_B=0$ ) [Fig. 4(c)].



**Figure 5. [Y] matrix derivation of the proposed multi-feed structure.**

The multi-feed structure is inherently a passive, linear, and reciprocal two-port electrical network, so it can be analyzed through its [Y] matrix (Fig. 5). The Y-parameters  $Y_{11}$  and  $Y_{21}$  can be derived by exciting a voltage  $V_e$  at port 1 and assuming a short-circuited termination at port 2. With this short termination condition, the multi-feed structure now resembles a single-feed loop antenna. Under the excitation voltage  $V_e$ , the current  $I_1$  equals  $V_e/Z_{rad}$ , where  $Z_{rad}$  is the radiation impedance of the single-feed antenna. Since the standing

wave current distribution is formed inside the loop, the magnitude and phase of current  $I_2$  equals to that of current  $I_1$ , and thus  $I_2 = V_o/Z_{rad}$ . Therefore, we will have

$$Y_{11} = Y_{21} = 1/Z_{rad}. \quad (1)$$

Similarly, the Y-parameters  $Y_{22}$  and  $Y_{12}$  can be derived based on symmetry:

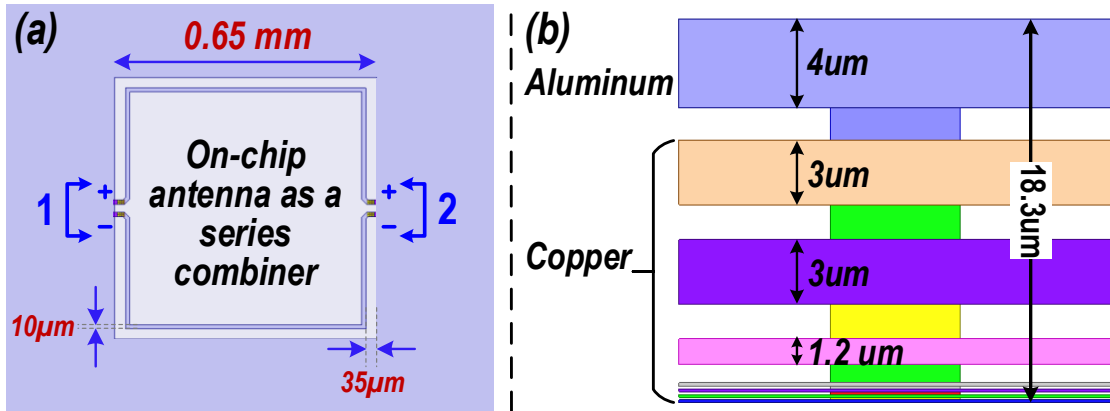
$$Y_{22} = Y_{12} = 1/Z_{rad} \quad (2)$$

The antenna's complete [Y] matrix is thus mathematically identical to an ideal series power combiner:

$$[Y] = \begin{bmatrix} Y_o & Y_o \\ Y_o & Y_o \end{bmatrix} \text{ (where } Y_o = 1/Z_{rad}\text{),} \quad (3)$$

indicating their electrical equivalency and therefore a multi-feed one- $\lambda$  wire loop antenna can be employed as an ideal series power combiner at its resonance frequency.

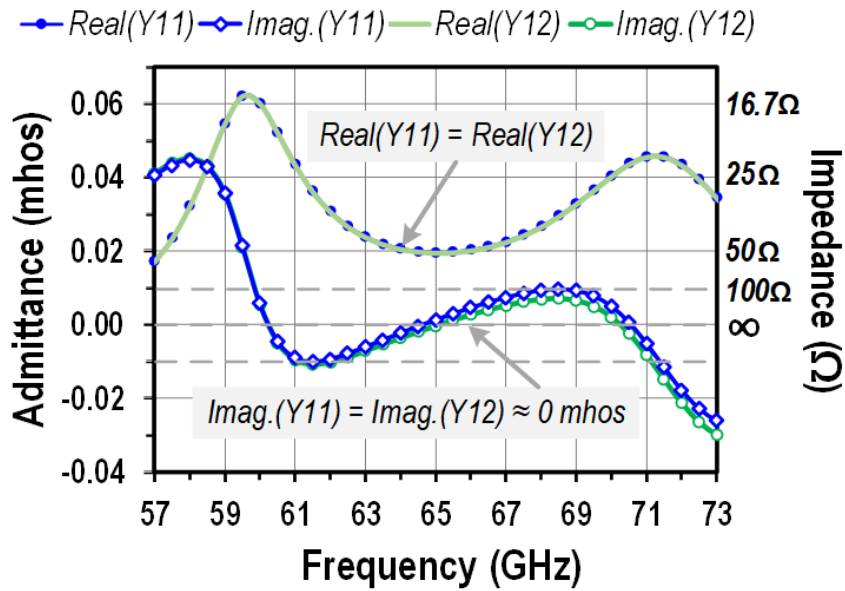
### 3.2 EM Implementation of the Proposed On-Antenna Doherty PA Architecture



**Figure 6.(a) EM model of the on-chip multi-feed one- $\lambda$  wire loop antenna. (b) Detailed metal stack-up for the antenna design.**

Figure 6(a) illustrates the 3D EM model of the on-chip multi-feed antenna, while Figure 6(b) depicts the metal stack used in this design. The antenna is designed on the 4  $\mu\text{m}$

Aluminum layer. In this work, we further shape the loop antenna ground such that it exhibits double resonance for bandwidth extension [60]. The antenna occupies  $650 \times 650 \mu\text{m}^2$  with  $10 \mu\text{m}$  trace width and  $35 \mu\text{m}$  ground separation. The simulated radiation efficiency is 83% on a standard high resistivity silicon provided by GlobalFoundries advanced SOI processes. Figure 7 depicts the simulated [Y] matrix of the multi-feed network. Dual resonance frequencies occur at 60GHz and 70GHz, resulting in relatively constant *Real* and *Imag.* [Y] parameters over 62-68GHz. Across the entire antenna bandwidth,  $Real(Y_{11}) = Real(Y_{21})$  and  $Imag.(Y_{11}) = Imag.(Y_{21}) \approx 0$ , verifying the desired [Y] matrix response. The simulation matches well with the theoretical prediction and validates the expected series combiner response of the on-chip multi-feed antenna structure.



**Figure 7. Simulated [Y] matrix of the proposed on-chip multi-feed antenna. The corresponding parallel impedance values are shown on the right y-axis.**

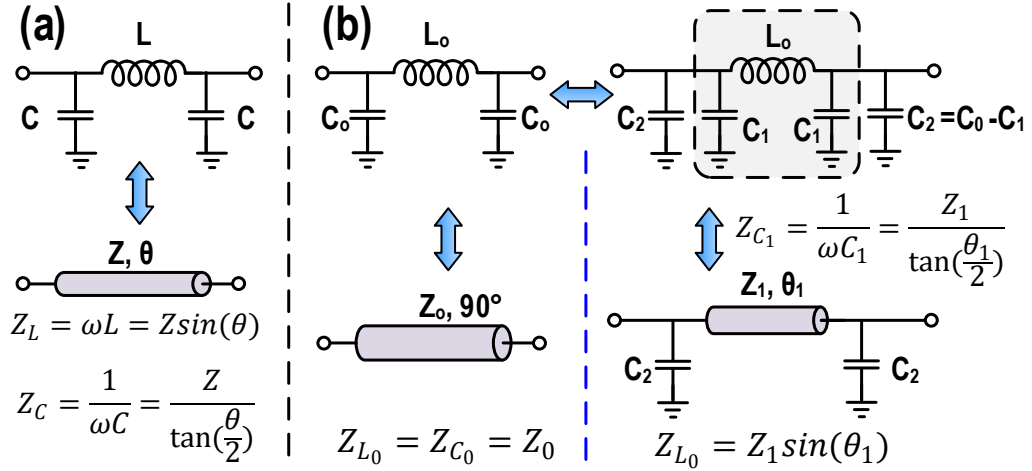


Figure 8.(a) T-line and CLC equivalent structures. (b) Impedance inverting networks as capacitively-loaded T-Line.

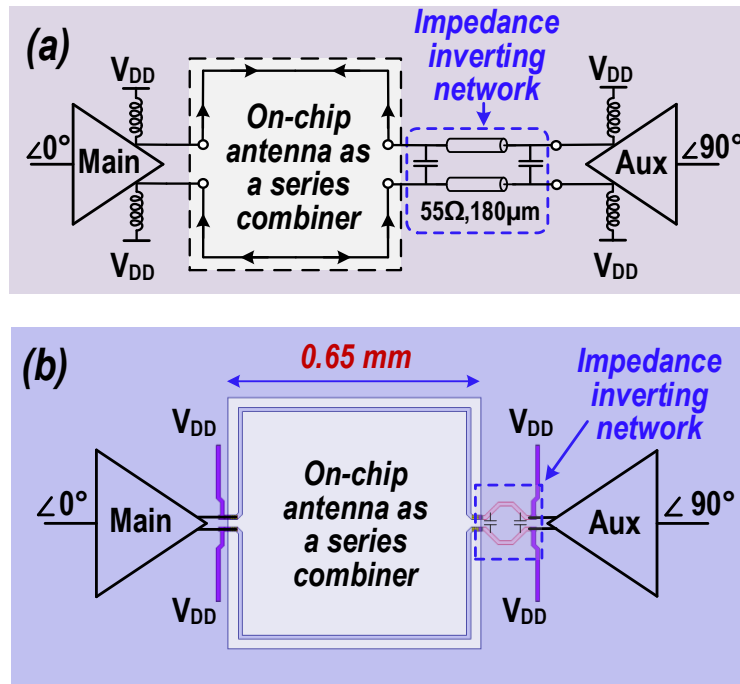
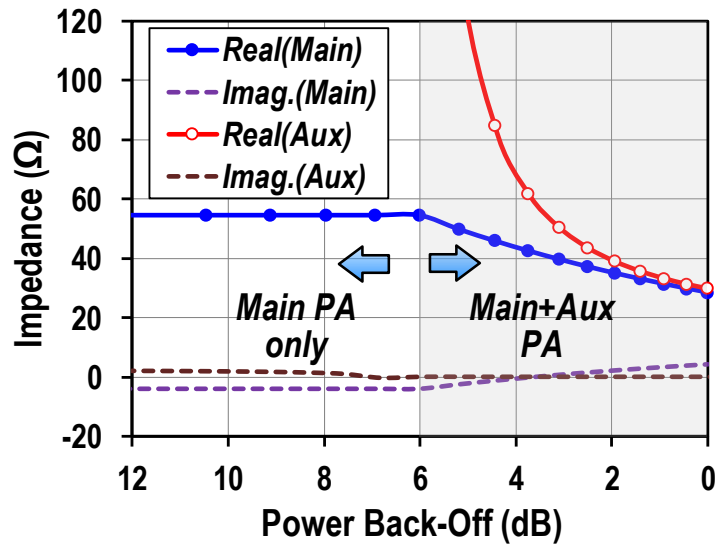


Figure 9. (a) Schematic of the proposed Doherty Radiator (b) 3D EM model of the proposed Doherty structure.

The series Doherty architecture entails an additional impedance inverting network in the Auxiliary path [Fig. 2(c)]. Conventionally, the quarter wavelength T-line is often employed to invert the impedance. By transforming between equivalent T-line and CLC structures

[Fig. 8(a)], the impedance inverting network can be designed as a capacitively-loaded T-line to ensure its short electrical length for size reduction [Fig. 8(b)]. Figure 9 depicts the overall schematic and 3D EM model of the proposed Doherty Radiator. The differential Main PA directly connects the on-chip antenna while the differential Auxiliary PA directly connects to the impedance inverting network with no additional impedance transformation network. Shunt inductors provide supply feeding and resonate out the Main/Auxiliary PA output capacitors.

### 3.3 Advantages of the Proposed Structure



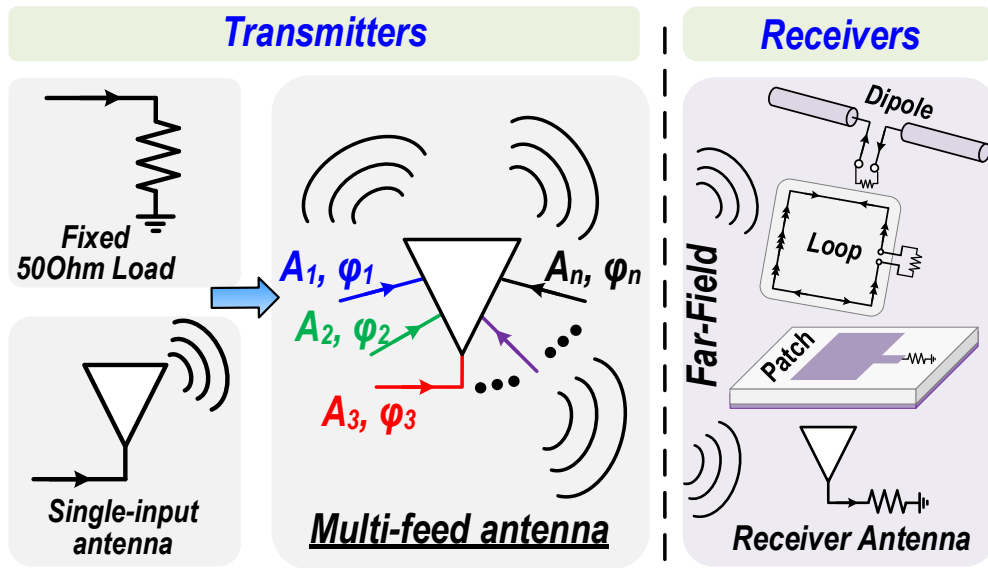
**Figure 10. Simulated active load modulation response of the proposed Doherty structure at 65GHz.**

The proposed architecture offers several advantages. First, the antenna-based Doherty is inherently a low-loss power combining structure, as on-antenna power combining is typically less lossy than conventional power combining methods [53]-[58]. Second, the antenna-electronics co-design substantially simplifies on-chip passive networks. Typical series Doherty architectures demand transformer-based or T-line-based series combiners.

Meanwhile, the Doherty Radiator merges such area-consuming circuits into the antenna, eliminating additional passives and more importantly their loss. Third, the Doherty Radiator demonstrates excellent signal-processing accuracy. The derived [Y] matrix indicates that the multi-feed antenna is electrically equivalent to a differential series-combiner, while using top thick metal layers to construct on-chip antennas minimizes process variations in practice. Overall, we achieve a close-to-ideal Doherty active load modulation by antenna-electronics co-designs (Fig. 10).

# CHAPTER 4: FAR-FIELD TRANSMISSION AND DESIGN CONSIDERATIONS

## 4.1 Design Considerations of Multi-Feed Antenna



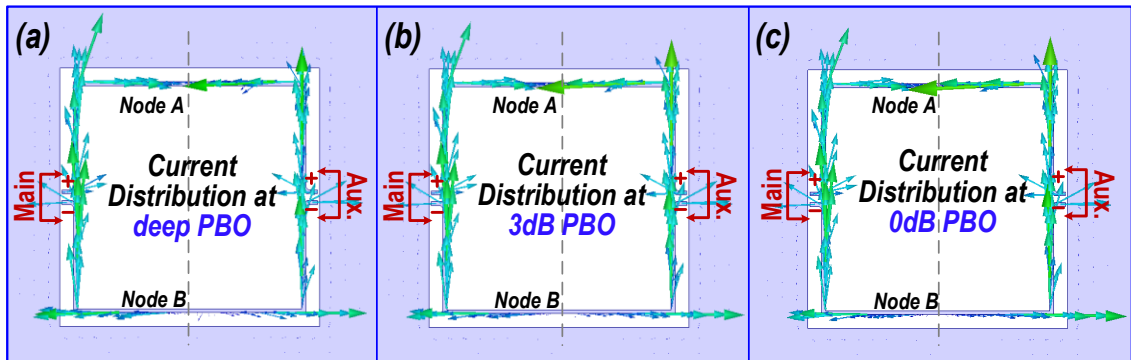
**Figure 11. Transmitter with multi-feed antenna architecture and far-field loads**

Multi-feed radiators do not follow the conventional approach of delivering power to either a fixed  $50\Omega$  impedance or a single-input antenna. Instead, transmitted power is distributed to the multiple antenna feeds to perform on-antenna signal processing and is finally received by far-field receiver antennas. A generalized figure is shown in Fig. 11. Conventional terminal circuit parameters such as output power or large-signal linearities (AM-AM, AM-PM) are less meaningful at the antenna multi-feeds, since the transmitted signals often exhibit dissimilar magnitudes/phases and have not performed on-antenna signal processing at those feed terminals. To resolve this ambiguity, we expand the definition of the final load of the multi-feed radiator to the target RX antenna load in far-field. Subsequently, this load captures the complete on-antenna operations and all non-

idealities in free-space propagation and communication channel, quantifying the large-signal AM-AM and AM-PM linearities of the entire radiator/transmitter chain. Additionally, a far-field receiver and the Friis transmission equation can be used to derive the radiator output power given the path loss, polarization, and TX/RX antenna gains.

## 4.2 Doherty Radiator Analysis

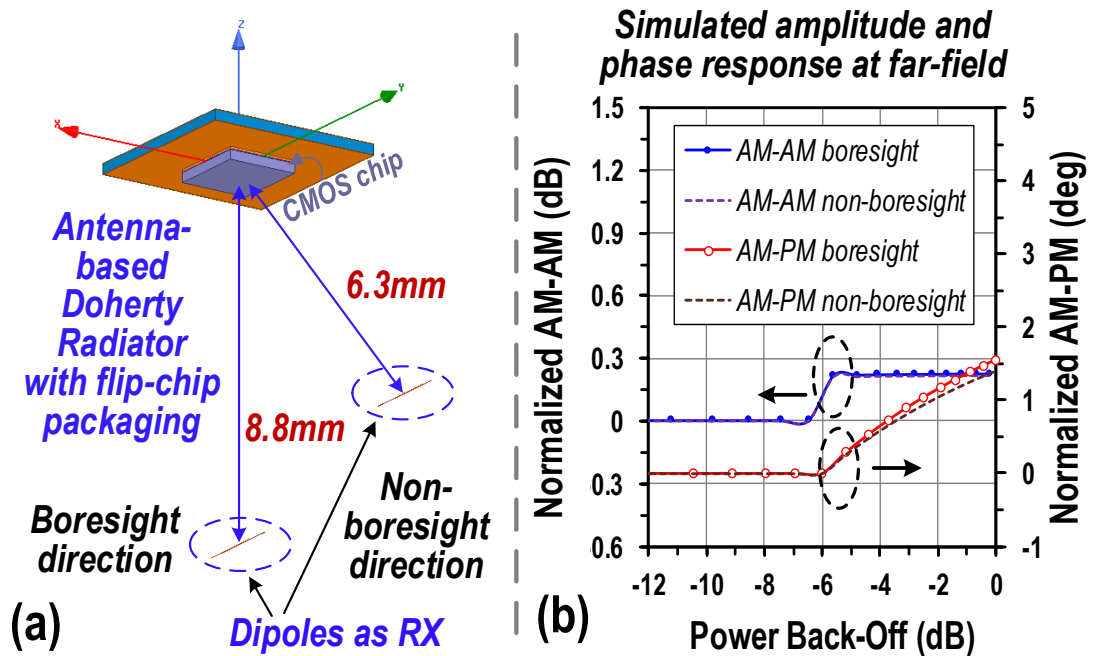
We apply these considerations to characterize our proposed Doherty Radiator. It is worth noting that the driving conditions in the Doherty Radiator varies versus the PBO level. At deep PBO, the Auxiliary PA turns off, thus only the Main PA delivers power to the antenna. During the Doherty operation at medium/low PBO, the Auxiliary/Main PA power ratio gradually increases. Eventually, at 0dB PBO, both Main/Auxiliary PAs contribute the same amount of power to the Doherty Radiator. This varying driving condition causes redistribution and superposition of on-antenna radiation currents, which is different from previously reported multi-feed radiators with fixed antenna's driving condition (in-phase equal-magnitude signals at all feeds) across PBO levels [53]-[57].



**Figure 12. Simulated current distribution of the multi-feed antenna at (a) deep PBO (b) 3dB PBO (c) 0dB PBO.**



To maintain large-signal linearity at far-field receivers, the radiation pattern/gain of the Doherty Radiator must remain the same across the Doherty operation over the entire antenna FoV. Otherwise, spatially dependent AM-AM/AM-PM nonlinearity will appear and corrupt the demodulated signals. Figure 12 depicts the simulated current distribution of the multi-feed antenna at deep PBO, 3dB PBO, and 0dB PBO, where the Auxiliary path is completely turned off, intermediately turned on, and completely turned on, respectively. We observe a standing-wave current distribution inside the loop, where current peaks are at the feeding locations and current nulls are at the middle-nodes A & B. The simulated current distributions are mostly identical, suggesting a stable radiation pattern of the proposed structure during the Doherty active load modulation.



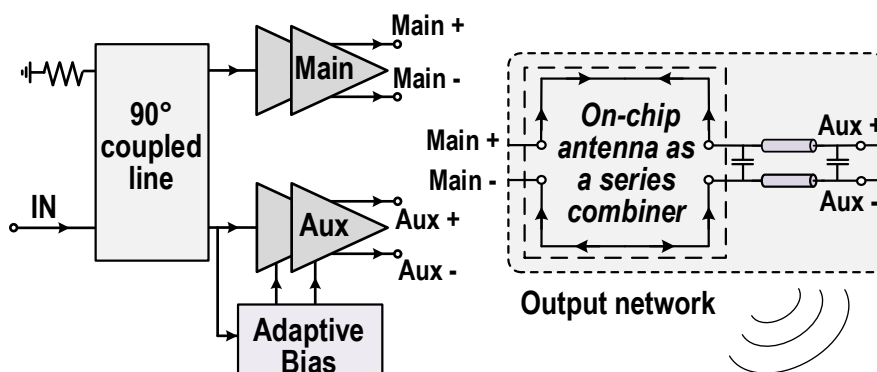
**Figure 13. (a) 3D EM simulation of the Doherty Radiator’s far-field transmission (b) Simulated amplitude and phase responses at far-field.**

Through 3D EM simulation, the full communication link is demonstrated with the Doherty Radiator as the TX and two dipoles at the far-field as the target RXs (Fig. 13). One dipole

is at the boresight main lobe ( $\varphi = 0^\circ$ ,  $\theta = 180^\circ$ ) and the other is at the non-boresight direction ( $\varphi = 0^\circ$ ,  $\theta = 225^\circ$ ). Both dipoles are terminated with their matched loads of  $78\Omega$  and the Doherty Radiator is driven by idealistic class-B linear Main/Auxiliary PAs to quantify the AM-AM/AM-PM nonlinearity only due to the radiator. With the desired Doherty Main/Auxiliary cooperation, we observe excellent large-signal linearity at the two far-field dipoles with very similar  $<0.2\text{dB}$  AM-AM and  $<1.5^\circ$  AM-PM variations. The far-field simulation validates that the multi-feed Doherty Radiator adds minimal large-signal non-linearity to the overall TX/RX wireless link even with varying Main/Auxiliary driving condition across the Doherty operation.

## CHAPTER 5: DOHERTY RADIATOR DESIGN

The top-level schematic of the Doherty Radiator is shown in Fig. 14. It consists of an antenna-based Doherty output network (Chapter 4-5), symmetric Main/Auxiliary PAs, a high-speed adaptive biasing at Auxiliary path, and a  $90^\circ$  coupler input feed.



**Figure 14.** Top-level schematic of the proposed mm-Wave Doherty Radiator.

### 5.1 Power Amplifier Unit Cell Design

The Main/Auxiliary PAs comprise a common source Driver and a cascode PA (Fig. 15). The DC supply is 1.9V for the PA and 1V for the driver. Neutralization capacitors are employed to boost the power gain and enhance the reverse isolation. At input and inter-stage, transformers are utilized as impedance matching networks. The single-ended input impedances of the Main/Auxiliary PAs are matched to  $50\Omega$ . Additional T-lines are added between the common source and common gate of the cascode PA as inter-stack matching to improve the current gain [62][63]. At the output stage, high-Q shunt inductors are used to resonate out the PA output parasitic capacitance and provide supply feeding. Unlike many differential PA designs that use output baluns, the Doherty Radiator employs differential multi-feed antenna to directly combine the differential PA output signals,

eliminating the need for lossy baluns and further improving the balancing of the output stage.

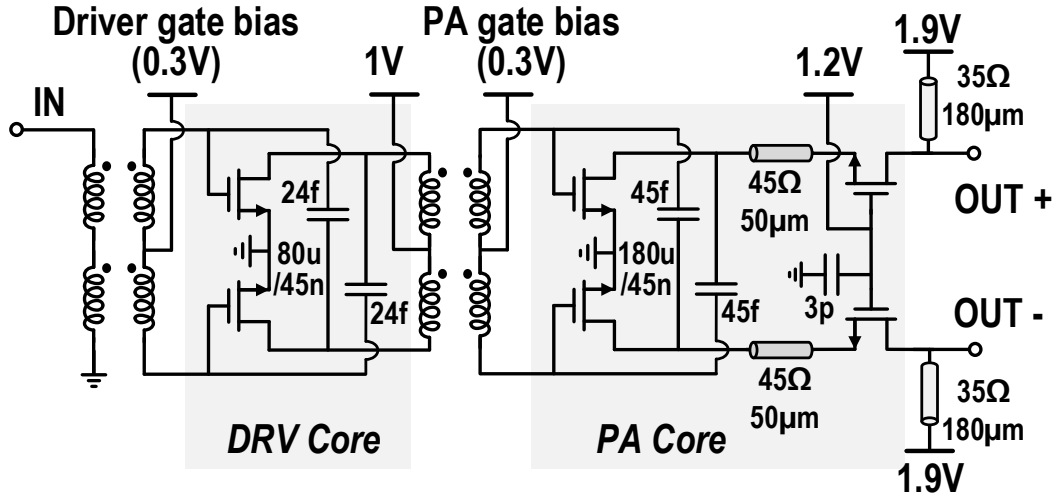


Figure 15. Schematic of the identical Main/Auxiliary PAs.

## 5.2 High-Speed Adaptive Biasing Circuit

Differential Doherty operation demands the Main/Auxiliary PA output currents to follow a desired Doherty current relationship [Fig. 1(c)]. In practice, auxiliary PAs are often biased at class-C region to enable its turning-on at high input power. However, for most Si devices, class-C operation at mm-Wave frequencies exhibit limited sub-threshold transistor gain, early compression, and imperfect Main/Auxiliary cooperation. Adaptive biasing is a popular technique to improve the turn-on characteristics of the Auxiliary PA path (Fig. 16)[40][41]. It is worth mentioning that applying adaptive biasing only at the PA stage is often insufficient for Doherty PAs in advanced Si processes. Even at deep PBO, the driver output voltage swing can be sufficiently high to unwantedly turn-on the Auxiliary PA and result in degraded Main/Auxiliary cooperation and low PBO PAE.

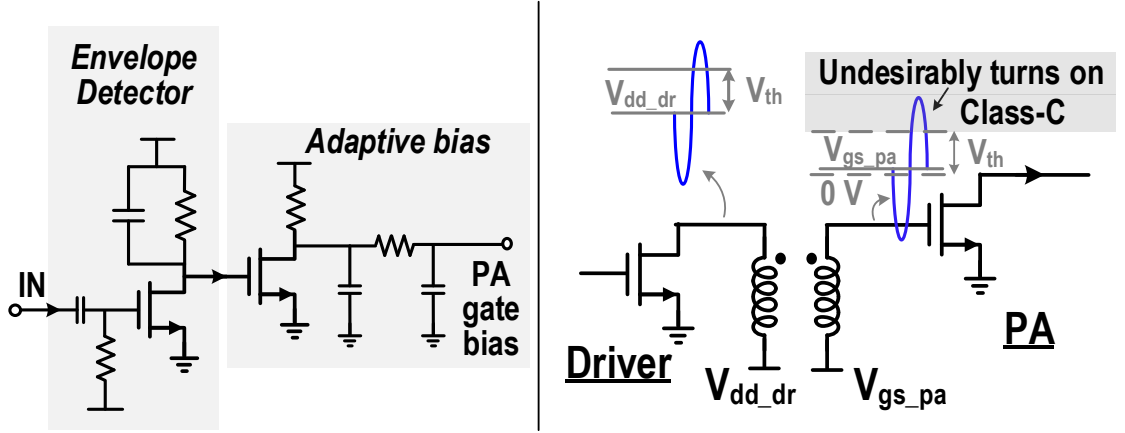


Figure 16. (a) Adaptive biasing for PA stage (b) Undesirable Auxiliary PA turn-on.

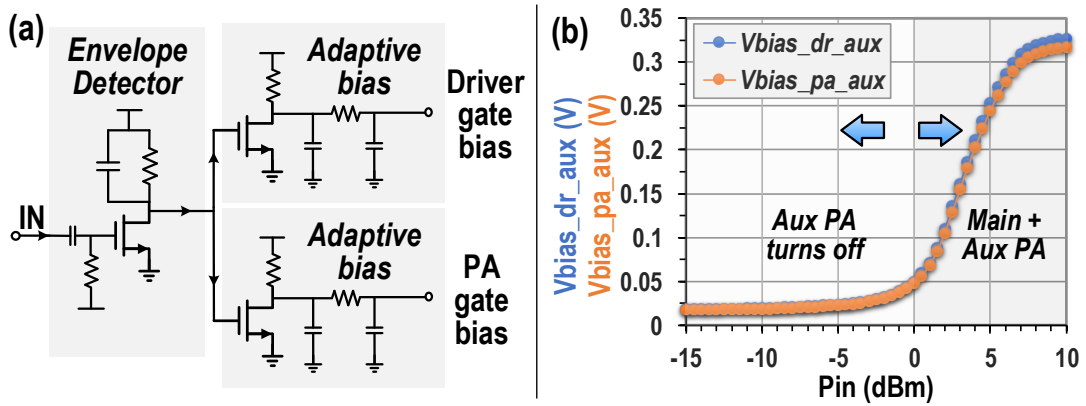
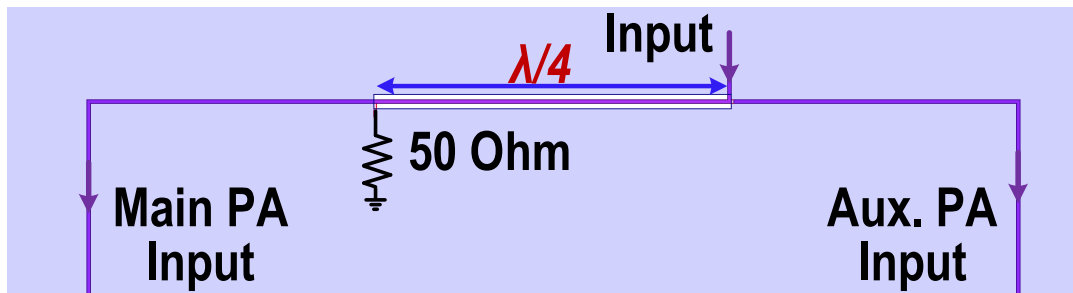


Figure 17. (a) Schematic of the adaptive biasing circuit (b) Adaptive biasing voltage as a function of input power.

In this work, we apply adaptive biasing for both driver and PA stages (Fig. 17), such that at deep PBO the gate voltage of the common source transistors for the driver and PA stages are all biased at  $\sim 0V$ . Subsequently, the Auxiliary path completely turns off at deep PBO. Meanwhile, the gate biasing rapidly increases during the desired Doherty operation [Fig. 15(b)]. At 0dB PBO, the Auxiliary path fully turns on and delivers similar output power and large-signal gain as the Main path. Overall, besides avoiding undesired Auxiliary turning-on, this approach also reduces the power consumption of the Auxiliary path and further enhances the overall radiator PAE at deep PBO.

In addition, the adaptive biasing circuit must be sufficiently fast to support high-speed modulation. As the AM modulation bandwidth is typically  $\times 3\sim 5$  that of the complex modulation, the bandwidth of the adaptive biasing must be at least 3GHz to accommodate 1Gsym/s modulated signal. In this work, the simulated bandwidth of the adaptive biasing circuit is  $\sim 5$ GHz.

### 5.3 Input Feeding Network

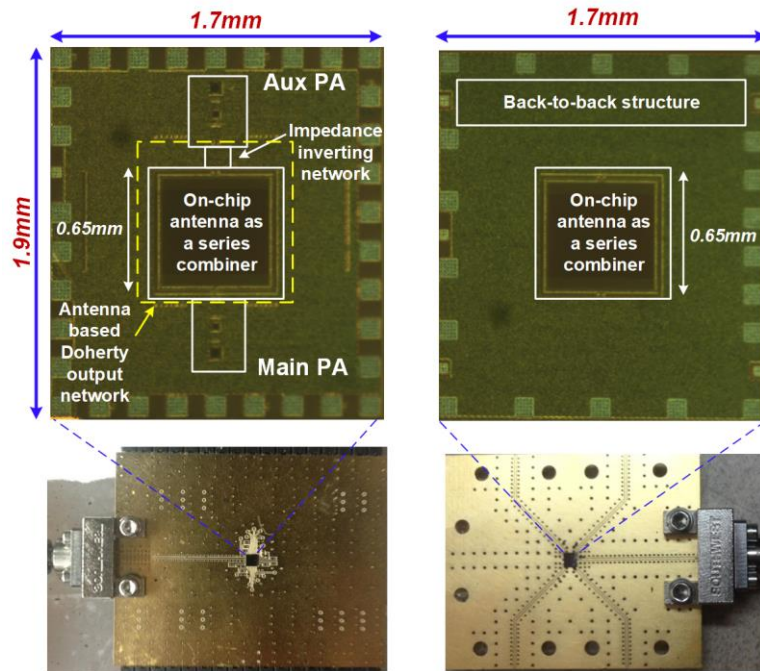


**Figure 18. Input network of the Doherty Radiator to generate two input signals with  $90^\circ$  phase difference.**

An on-chip  $50\Omega$   $90^\circ$  coupled line generates the Main/Auxiliary input signals. The coupled line directly feeds the  $50\Omega$  Main/Auxiliary PA inputs by its through/coupled ports respectively. Both feed lines have the same length to ensure the desired  $90^\circ$  phase difference. The coupler isolation port is terminated with  $50\Omega$  to provide isolation between the Main and Auxiliary PAs (Fig. 18). This isolation further enhances the stability of the Doherty Radiator.

## CHAPTER 6: MEASUREMENT RESULTS

### 6.1 Chip Fabrication



**Figure 19. Die micrographs of the Doherty Radiator, antenna test structure, and photos of the flip-chip packaged PCBs.**

As a proof-of-concept, the 62-68GHz Doherty Radiator is fabricated in GlobalFoundries 45nm CMOS SOI process with trap-rich high resistivity substrate ( $>200 \Omega \cdot \text{cm}$ ) for low-loss on-chip antennas [61]. The chip is  $1.7 \times 1.9 \text{mm}^2$  including the on-chip antenna and pads. A separate antenna test structure in the same process is used for antenna stand-alone characterization. Both the Doherty Radiator and the test structure are flip-chip packaged on a Rogers CLTE-AT<sup>TM</sup> laminate to perform back-side radiation. With considerably higher permittivity ( $\sim 12$ ) than air or PCB ( $\sim 1-3$ ), the silicon substrate traps most of the electric fields and radiated power to the back of the chip, leading to backside radiation with simulated back-to-front ratio of 3.3. The PCB has a ground opening in all the layers

underneath the chip. Southwest end-launch connectors are used to feed the mm-Wave input signals. Figure 19 shows the micrographs of the Doherty Radiator, antenna test structure, and photos of the flip-chip packaged PCBs.

## 6.2 Continuous-Wave (CW) Measurement

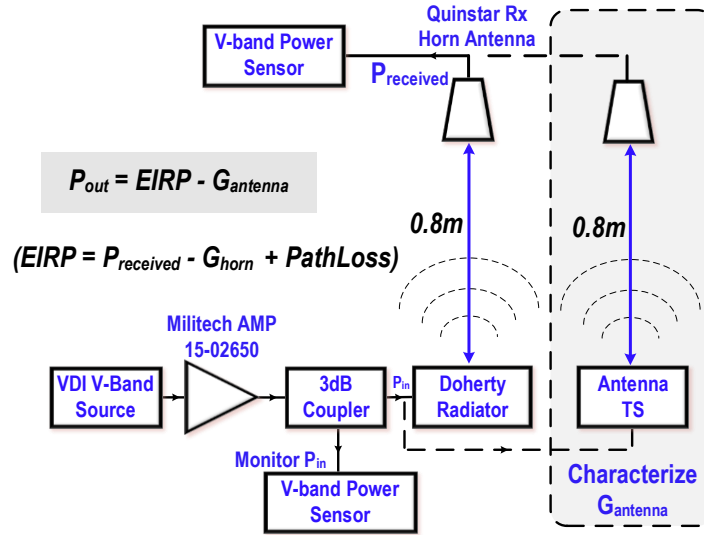


Figure 20. CW measurement setup.

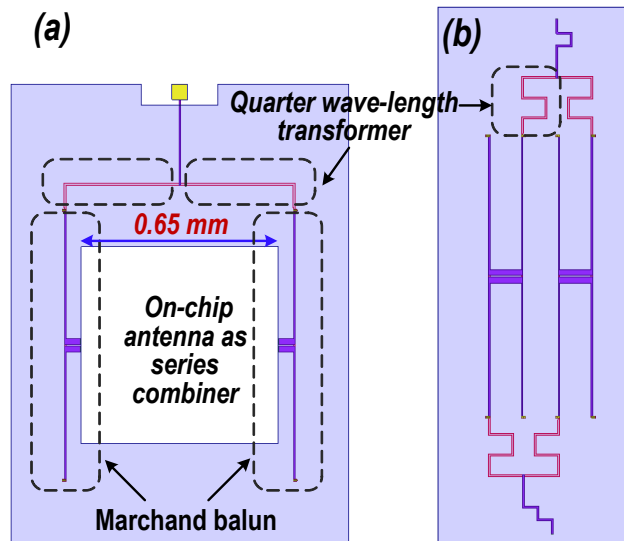


Figure 21. (a) Power distribution network to characterize the antenna gain at peak output power (b) Back-to-back test structure to measure passive loss of the antenna feeding network.



Figure 20 depicts the CW measurement setup. The CW input signal is generated from a VDI V-band source, amplified by an external amplifier, monitored by a 3dB coupler with power sensor, and applied to the Doherty Radiator chip input. Then the signal is amplified and radiated by the Doherty Radiator chip. At far-field ( $d = 0.8\text{m}$ ), the CW signal is received by a horn antenna and the received power is measured by a power sensor. The total output power  $P_{out}$  of the Doherty Radiator is calculated as the power delivered to the antenna:

$$P_{out} = EIRP - G_{antenna}. \quad (4)$$

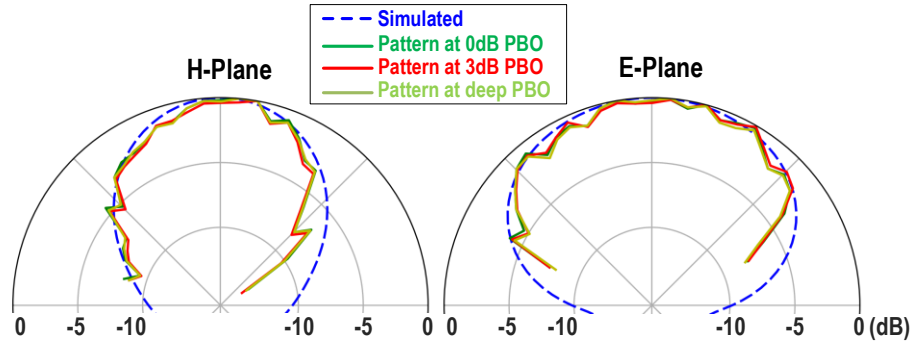
The Equivalent Isotropically Radiated Power ( $EIRP$ ) is then derived based on the Friis transmission equation:

$$EIRP = P_{received} - G_{horn} + Pathloss, \quad (5)$$

$$\text{where } Pathloss = 20\log\left(\frac{4\pi d}{\lambda}\right).$$

The antenna gain  $G_{antenna}$  is characterized from the antenna test structure. While Doherty Radiator gain is constant across the Doherty operation [Fig. 13(b)], we measure the antenna test structure gain at 0dB PBO to specifically characterize the peak total output power. Since the Main/Auxiliary PAs contribute the same power to the antenna at 0dB PBO, a T-junction power divider and Marchand baluns are implemented as the feeding network to deliver equal power to the two differential feeds of the antenna [Fig. 21(a)]. In addition, we measure the loss of the feeding network of this antenna by a back-to-back feed test structure [Fig. 21(b)]. At 65GHz, the measured antenna gain is 4.5dBi and the radiation pattern of the multi-feed Doherty Radiator versus various power level is depicted in Fig.

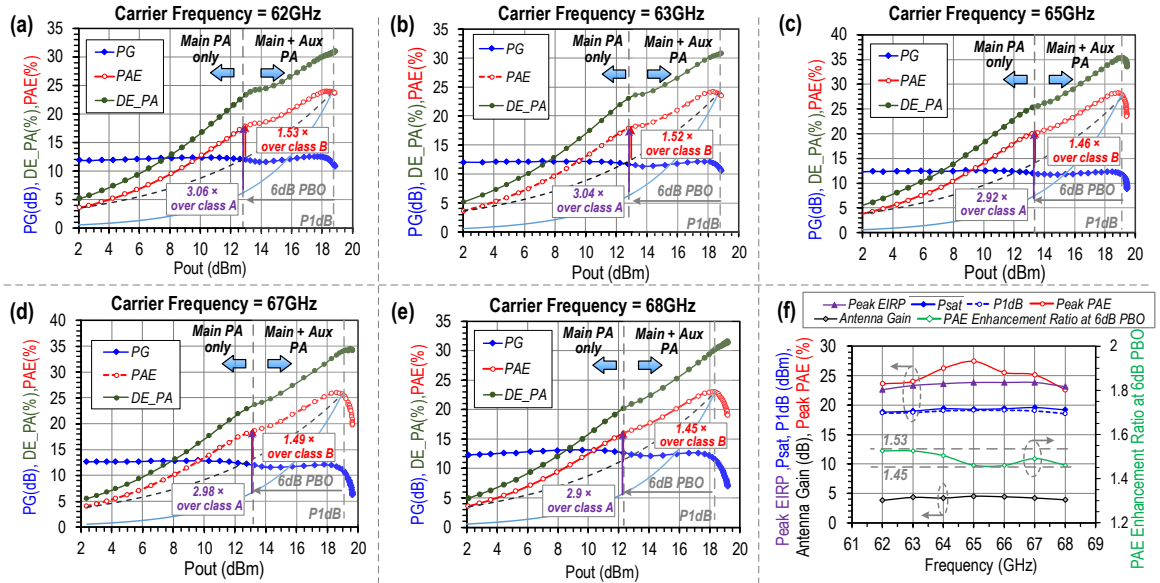
22. The measured radiation pattern remains stable during the Doherty operation and demonstrates a close match between the measurement and simulation results.



**Figure 22. Radiation pattern of the proposed structure in E-/H-plane at 0dB/3dB/deep PBO**

Figure 23 shows the measured CW performance and a performance summary of the Doherty Radiator. Across operation frequencies, the PAE curves demonstrate two distinct regions: the Doherty region with a substantially boosted PAE response for 0-6dB PBO and a class-AB region below 6dB PBO after the Auxiliary path turns off. The measured Doherty Radiator exhibits radical PAE enhancement at 6dB PBO compared to an idealistic class-B PA normalized with the same PAE at  $P_{1dB}$ , demonstrating consistent  $1.45\text{-}1.53\times$  PAE improvement across 62-68GHz. The PAE closely tracks the drain efficiency of PA stage due to the adaptive biasing applied in the Auxiliary PA path. Additionally, the Doherty Radiator features an excellent AM-AM linearity with only  $<0.7\text{dB}$  difference between  $P_{sat}$  and  $P_{1dB}$  over the entire 62-68GHz, which benefits from both on-antenna Doherty output network and adaptive biasing. At 65GHz, the measured saturated EIRP/ $P_{sat}$ / $P_{1dB}$  are 23.9/19.4/19.2dBm, respectively. The total measured PAE including adaptive biasing power consumption at 0dB/6dB PBO are 27.5%/20.1% respectively, exhibiting  $1.46\times$  PAE improvement over an idealistic class-B PA and  $2.92\times$  PAE

enhancement over an idealistic class-A PA with the same PAE at 0dB PBO. Accounting the simulated 83% radiation efficiency, the peak radiated power is 18.6dBm, which is 0.8dB less than the peak power delivered to the antenna of 19.4dBm.



**Figure 23. (a-e) Measured CW performance of the Doherty Radiator at 62/63/65/67/68GHz carrier frequencies (f) CW performance summary.**

### 6.3 Dynamic Modulation Measurement

Next, we characterize the dynamic measurement of the Doherty Radiator. Figure 24(a) depicts the modulation measurement setup. The modulated signal is generated by an arbitrary waveform generator (AWG), up-converted by a mixer with an image-rejection filter, amplified by external amplifiers, and applied to the Doherty Radiator input. After amplification by the Doherty PAs and radiation from the on-chip multi-feed antenna, the modulated output wave at far-field is received by a horn antenna. The signal is then amplified by a low noise amplifier, down-converted by a mixer, amplified again, and analyzed by an oscilloscope. In addition, a wireless loop-back test with two horn TX/RX antennas is employed to perform channel equalization and characterize the EVM floor of the measurement setup. Figure 24(b) depicts the modulation performance of the Doherty

Radiator. The Doherty Radiator supports 3Gbit/s and 6Gbit/s 64-QAM modulation transmission. For 0.5/1Gsym/s 64-QAM without DPD and at average power of 14.5/14.2dBm, the measured EVMs are -28.06/-26.7dB, the measured ACPRs are -26.97/-25.8dBc, and the measured average PAEs are 21.2%/20.2% respectively.

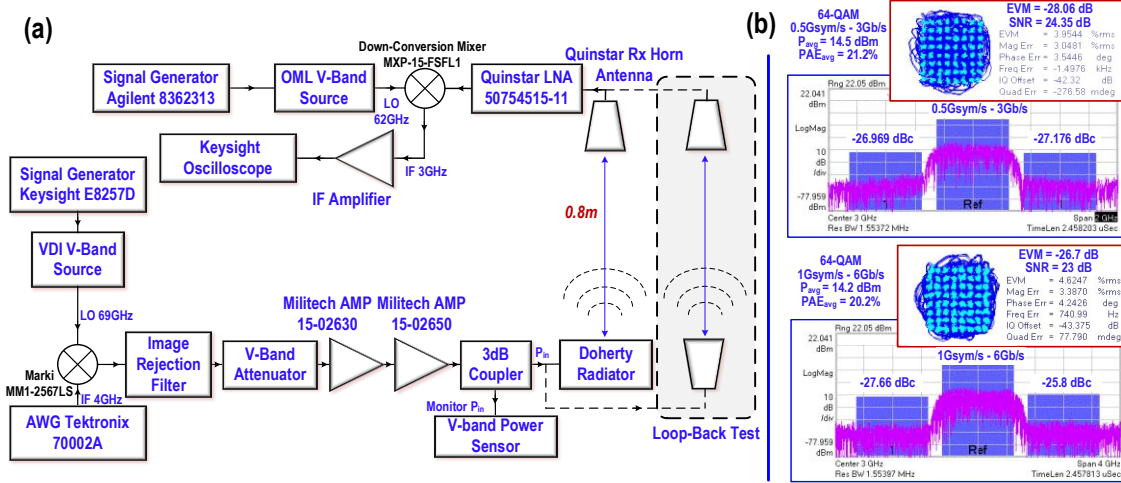


Figure 24. (a) Measurement setup to characterize the dynamic performance of the Doherty Radiator (b) Measured constellations and spectra of the Doherty Radiator with 0.5Gsym/s and 1Gsym/s 64QAM modulation.

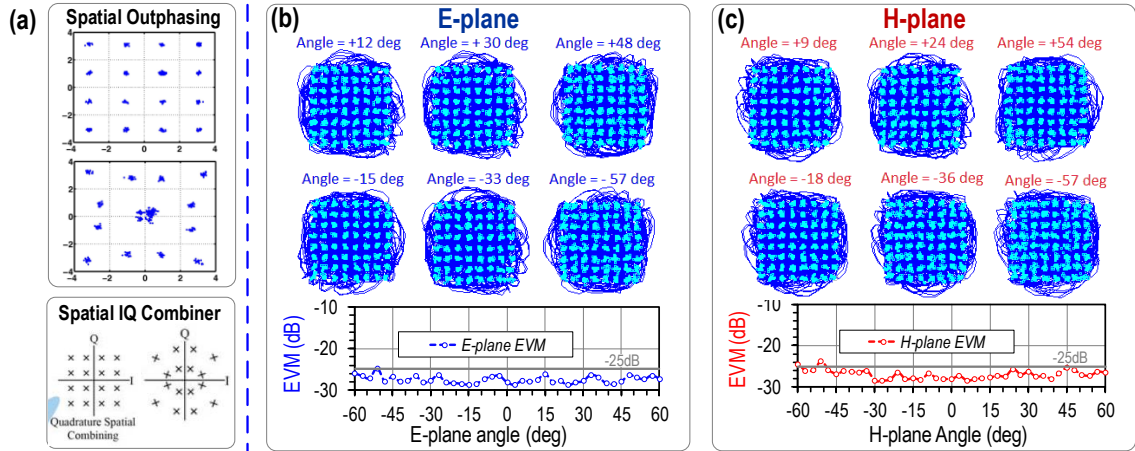


Figure 25. (a) Spatial Outphasing transmitter [42] and Spatial IQ combiner transmitter [43]. (b) Modulation measurement of the Doherty Radiator with 64-QAM 3Gb/s over the (b) E-plane and H-plane, illustrating wide antenna FoV.

Previous literature have shown PA/TX architectures with spatial power combining such as the Spatial Outphasing TX [42] and Spatial IQ Combiner TX [43] [Fig.25(a)]. However, due to the vectoral spatial signal combining, these designs fundamentally exhibit substantially narrower FoV than the intrinsic antenna FoV. Furthermore, undistorted modulations only exist at specific directions and are severely distorted if the TX/RX angles are slightly mis-aligned (e.g., by only  $\sim 5\text{-}10^\circ$  in the design of Spatial Outphasing [42]). On the other hand, the Doherty Radiator combines the TX outputs on the antenna and simultaneously radiates out, avoiding any vectoral spatial combining and ensuring undistorted modulation over the full antenna FoV. Figures 25(b)-(c) depict the modulation results of the Doherty Radiator over various radiation directions. Given the horn antenna rotating with  $3^\circ$  increments over  $\sim -60^\circ$  to  $+60^\circ$  zenith angle in both E-/H-planes, measurement data show that the Doherty Radiator is angle-independent, achieving undistorted modulation and consistent EVMs over the entire FoV. In practical wireless communication scenarios, this helps to establish reliable links and substantially ease the TX/RX alignment. Moreover, multiple Doherty Radiators can form a phased array, where each unit does not compromise the array FoV, thus particularly suitable for massive MIMO applications.

Table I compares the Doherty Radiator with state-of-art [62]-[85]. Compared with 60-80GHz PAs/TXs, the Doherty Radiator features a PA architecture supporting high-efficiency high-speed transmission of modulated signals and demonstrating the record PBO efficiency enhancement ratio at 6dB PBO, absolute PAE value at 6dB PBO, and average PAE for 3Gbit/s and 6Gbit/s 64-QAM wireless transmission. It is worth mentioning that using the same principle, an on-antenna Doherty network or in general active load modulation network can also be implemented on other types of baseline antenna, such as patch, dipole, spiral, bow-tie, etc. The loop-based Doherty Radiator shown in this paper is just a demonstration example.

**Table 1 – Comparison with state-of-art 60-80GHz silicon-based PAs/Transmitters**

	This work	[39] Greene, JSSC' 17	[40] Kaymaksut, TMTT'15	[43] Chen, ISSCC'13	[53] Chi, ISSCC'17	[74] Khalaf, JSSC'16	[68] Zhao, TMTT'15	[79] Lin, TMTT'16	[72] Chappidi, JSSC'17	[81] Datta, JSSC'17	[78] Jayamon, RFIC'16
Architecture	Antenna-based Doherty	Doherty	Doherty	Spatial IQ combiner	On-antenna combiner	Digital Polar Tx	Class AB	Class AB	Asymmetric Combiner	Stacked Class-E	Stacked PMOS
Frequency (GHz)	65	62	72	60	60	60	80	76	55	83	78
V <sub>DD</sub> (V)	1.9	3.6	1.5	1	2	0.9	0.9	1.8	4	6.5	3.6
P <sub>sat</sub> (dBm)	19.4 <sup>‡</sup>	17.5 <sup>*</sup>	21	9.6	27.9 <sup>‡</sup>	10.8	20.9	27.3	23.6	23.3	18.7
P <sub>1dB</sub> (dBm)	19.2	17.1	19.2	9.6	25	7.4	17.8	22.3	19.9	--	15 <sup>*</sup>
Peak PAE	28.3%	23.7% <sup>*</sup>	13.6%	28.5%	23.4%	29.8%	22.3%	12.4%	27.7%	17.1%	24%
PAE @ P <sub>1dB</sub>	27.5%	23.7%	12.4%	28.5%	16.2%	15% <sup>*</sup>	12%	3% <sup>*</sup>	15.7%	--	20% <sup>*</sup>
PAE @ 6dB PBO	20.1%	13%	7%	14.25% <sup>*</sup>	6% <sup>*</sup>	4.5% <sup>*</sup>	4.5% <sup>*</sup>	1% <sup>*</sup>	7% <sup>*</sup>	--	8% <sup>*</sup>
PAE Enhancement Ratio at 6dB PBO <sup>*</sup>	1.46	1.10	1.13	1	0.74 <sup>*</sup>	0.6 <sup>*</sup>	0.75 <sup>*</sup>	0.67 <sup>*</sup>	0.89 <sup>*</sup>	--	0.8 <sup>*</sup>
Mod. Scheme	64-QAM		64-QAM	16-QAM	64-QAM	16-QAM	64-QAM		64-QAM		
Data Rate	3Gb/s		0.6Gb/s	6Gb/s	4.8Gb/s	6.7Gb/s	3Gb/s		3Gb/s		
SNR (MER)	24.3dB		25.6dB	16.2dB	25.4dB	18.1dB	24.7dB		21dB		
P <sub>avg</sub>	14.5dBm		15.9dBm	6dBm <sup>*</sup>	19.3dBm	3.6dBm	11.9dBm		14.8 dBm		
PAE <sub>avg</sub>	21.2%		7.2%	16.5%	5.3%	--	--		--		
Active Area (mm <sup>2</sup> )	0.3 / 3.23 <sup>‡</sup>	0.6	0.19	--	10.5 <sup>‡</sup>	<0.18	0.19	6.48	1.02	1.95	0.12
Technology	45nm CMOS SOI	130nm SiGe	40nm CMOS	65nm CMOS	45nm CMOS SOI	40nm CMOS	40nm CMOS	90nm SiGe	130nm SiGe	90nm SiGe	32nm CMOS SOI

<sup>\*</sup> Estimated from reported figures

<sup>\*\*</sup> Compared to an idealistic class-B PA with the same PAE at P<sub>1dB</sub>

<sup>‡</sup>Wireless-based power measurement

<sup>†</sup>Peak P<sub>Radiated</sub> = 18.6dBm with simulated 83% radiation efficiency

<sup>‡</sup>Including pads and on-chip antenna

## CHAPTER 7: CONCLUSION

The main purpose of this work is to investigate the possibility of employing antennas as a multi-feed network that performs active load modulation. As a proof-of-concept demonstration, we present a mm-Wave Doherty architecture leveraging a loop-based multi-feed network to support high energy-efficiency transmission of wideband modulated signal. Theoretical analysis and simulated results prove that the proposed antenna structure is electrically equivalent to a differential series combiner, which lead to an on-antenna series Doherty network that exhibits desirable Doherty active load modulation behavior. A general viewpoint on a multi-feed antenna wireless link system has been discussed, where the definition of final load is expanded to far-field receivers, and the condition of consistent radiation pattern during Doherty operation and power back-off is investigated and achieved. Additionally, adaptive biasing circuit is designed at the Auxiliary path to linearize the Doherty Radiator, such that wideband modulated signals can be transmitted without DPD. Overall, the Doherty Radiator demonstrates substantial efficiency enhancement at PBO ( $1.46\text{-}1.53\times$  PAE enhancement at 6dB PBO compared to an idealistic class-B PA normalized with the same PAE at P1dB) and illustrates undistorted constellation up-to 6Gbit/s 64QAM over the entire antenna FoV.

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