Goodrich Corporation

Final Report, June 2010

THROUGH-SILICON-VIA PROCESS DEVELOPMENT

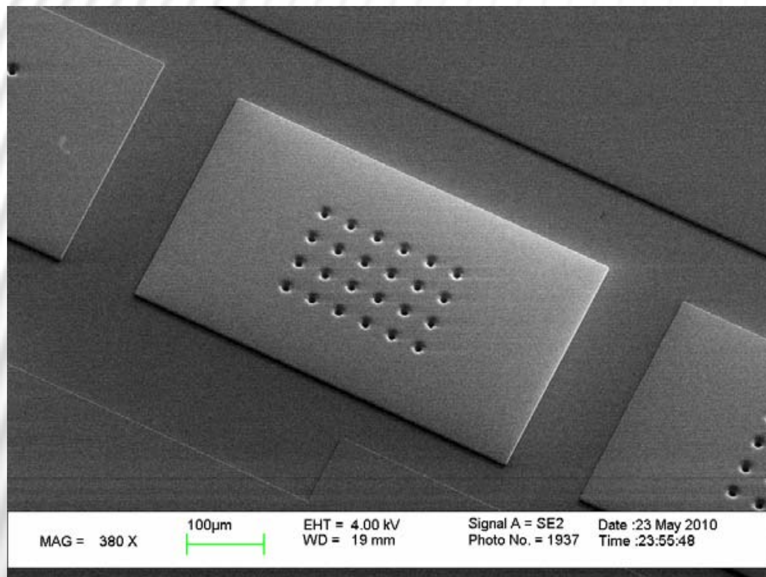
CONTENTS

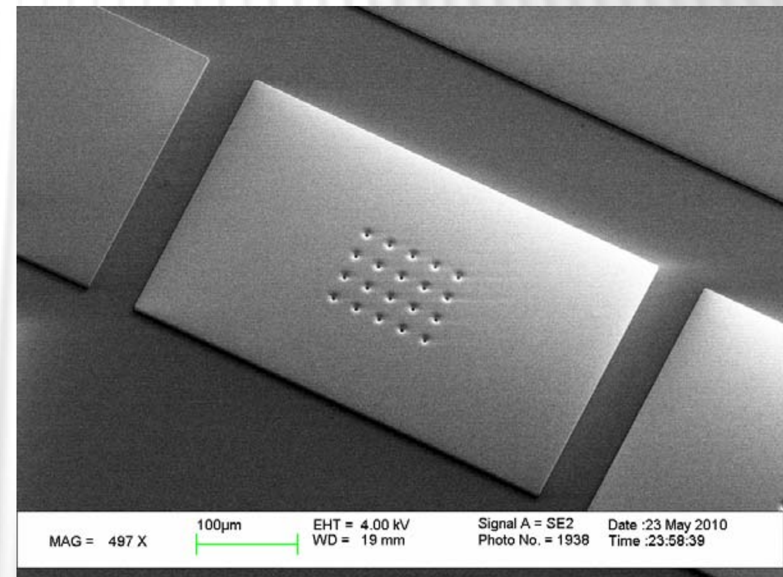
- TSV
  - Poly layer patterned
  - Trench top completely sealed
    - Verified by etching back shown in SEM's
  - A wafer cleaved for profile
    - A small void exit only at the bottom of the trenches shown in SEM's
  - Resistivity measured from 4-point probe
    - 0.008 Ω-cm
    - Parasitic capacitance measured
      - ~16 pF with LCR meter

VIA CLUSTERS SEEN FROM THE SURFACE

23 um wide opening Vias

15 um wide opening Vias

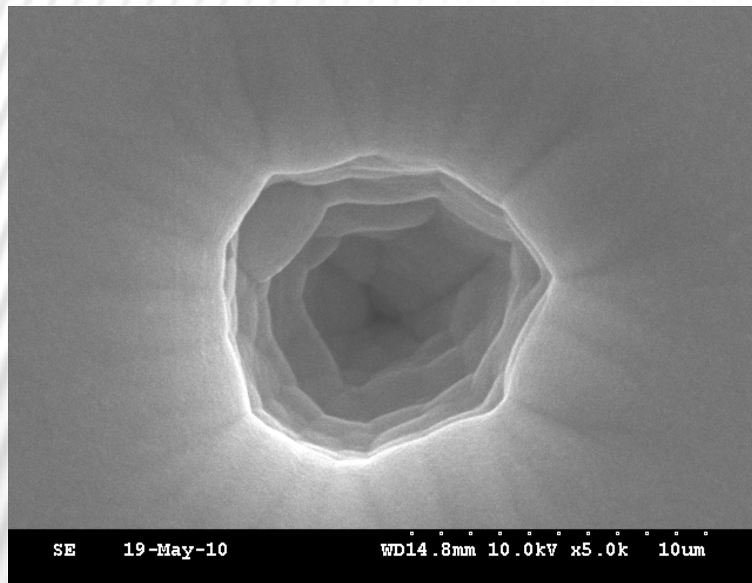




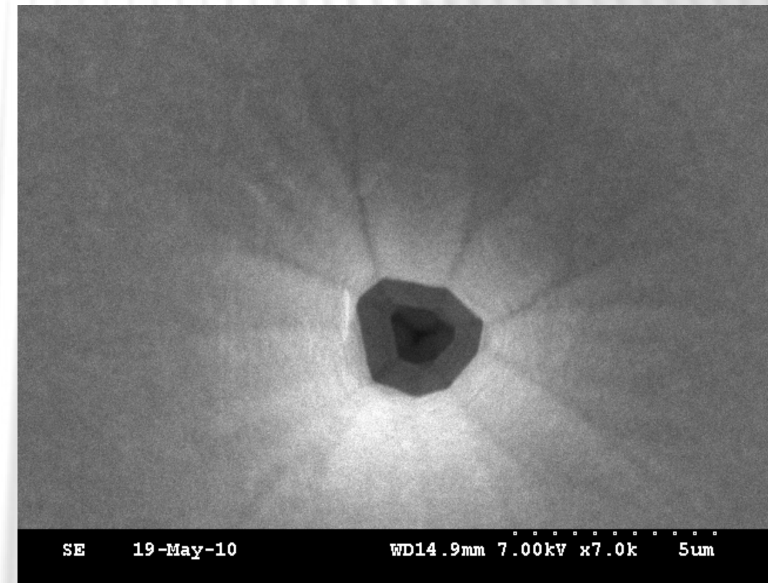
The two SEM's above show the patterned poly layers with clusters of vias isolated by rectangular sections.

TOP VIEW OF THE VIAS AT THE OPENING

23 um wide opening Vias



15 um wide opening Vias



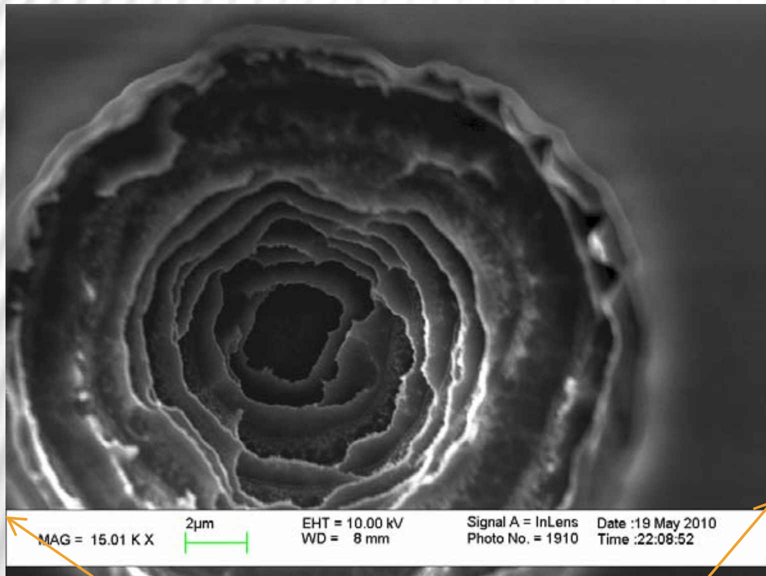
Both vias are completely filled and sealed from the top as shown in the above SEM's. The different concentric pattern at the openings are due to the two-time etching back and three-time poly refill. This was further verified by etching back from the poly from the top for 10 um.

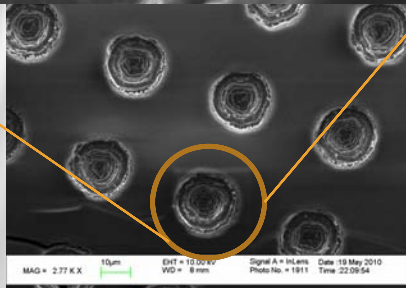
TOP VIEW OF THE VIA OPENING AFTER 10-UM ETCH BACK USING BOSCH PROCESS

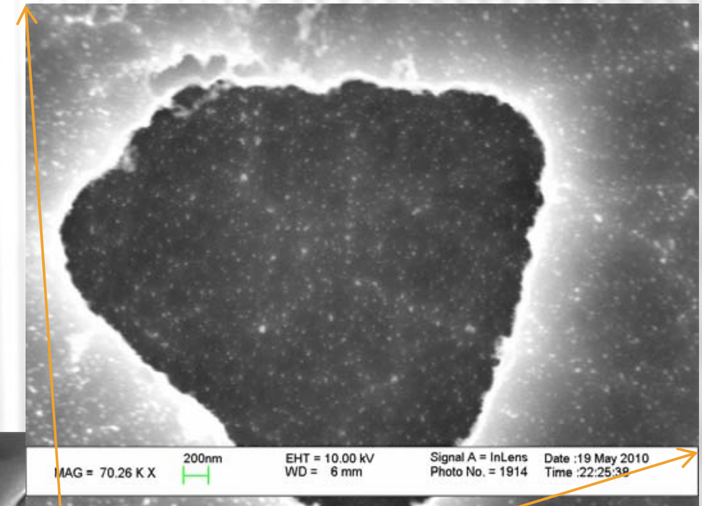
23 um wide opening Vias

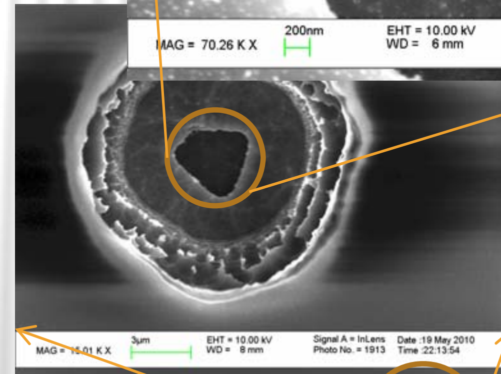
15 um wide opening Vias

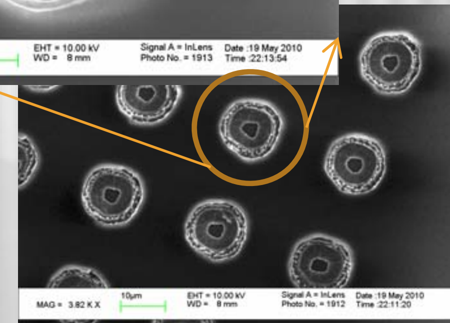
It might appear bottomless but in fact sealed. The layers represent the number of etching cycles.







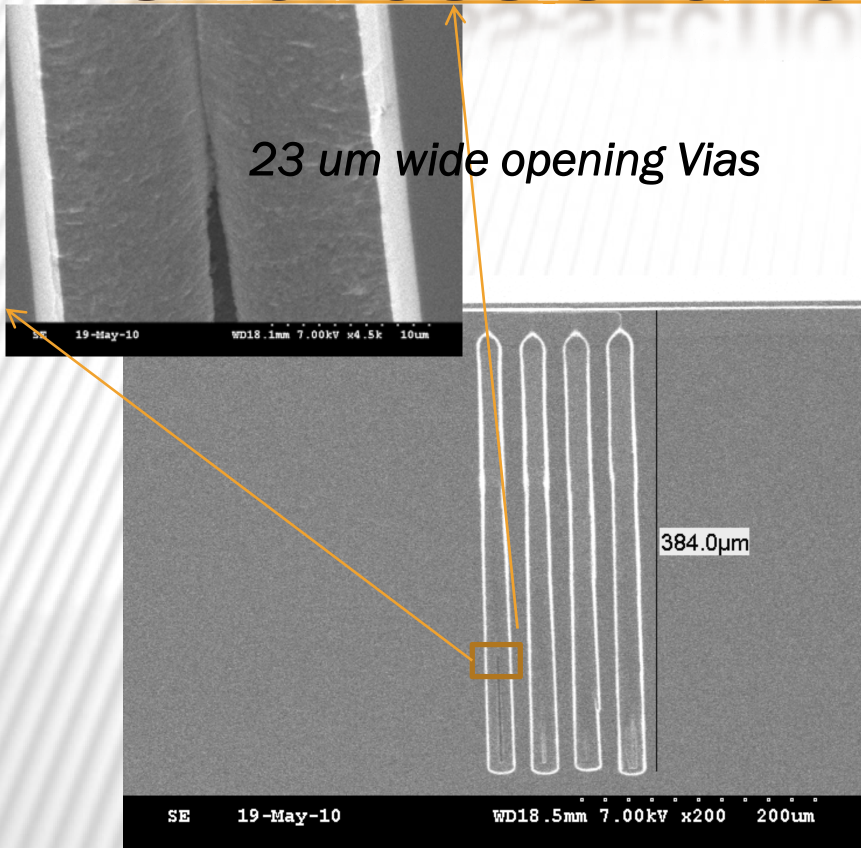


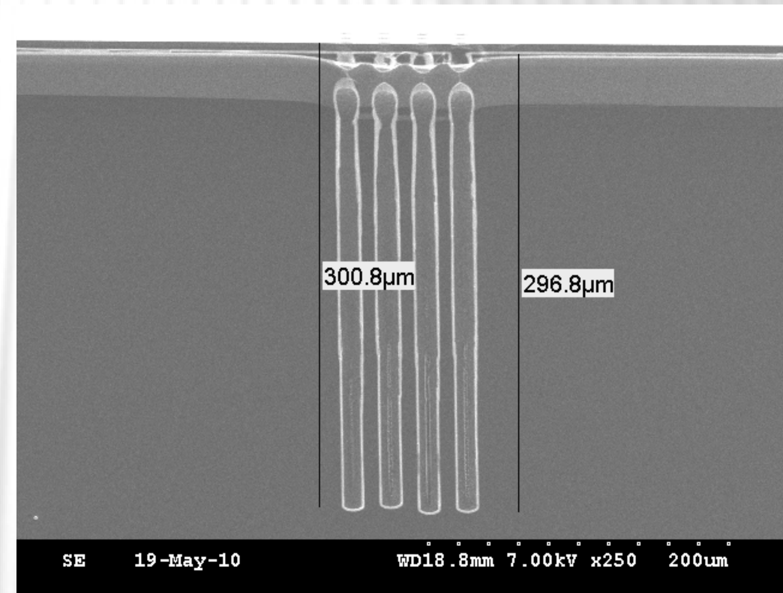


TSV CROSS-SECTION

23 um wide opening Vias

15 um wide opening Vias





As seen in the x-section. There are still a smaller void present in the trenches. The diameter of the voids is about 2.5 um. The length of the large vias is about 80 um more than the small ones. The trenches seem to have a very straight profiles poly voids seem to present at the bottom quarter of the vias.

PARASITIC CAPACITANCE APPROXIMATION

- Calculation based on parallel plate model

$$C = \varepsilon \frac{A}{d}$$

, where A is the area of the plates; d is the thickness of oxidee l; and ε is the dielectric constant of oxide.

$$C \approx 24 \times 3.9 \times 8.854 \times 10^{-18} F / um \times \frac{\pi \times 23um \times 384um}{1.600um} \approx 14.371 pF$$

The measured value using Agilent E4980A Precision LCR meter is approximately 16.0 *pF*, under the conditions of 20 Hz and voltage level of 2V.

NEXT UP

- Wafers are ready to be sent to be thinned and polished from the backside down to 295 +/-5 um if the silicon dioxide layer does not require any patterning.