THERMAL PERFORMANCE ENHANCEMENT OF PACKAGING SUBSTRATES WITH INTEGRATED VAPOR CHAMBER

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THERMAL PERFORMANCE ENHANCEMENT OF PACKAGING SUBSTRATES WITH INTEGRATED VAPOR CHAMBER

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To

My Loving Family

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SUMMARY

As demands on performance for mobile electronics continue to increase, traditional microsystems packaging technology is facing limits in number of input/outputs (I/Os) and thermal challenges. Glass interposers offer many advantages over silicon, as well as previous packaging technology for mobile electronics, including ultra-high electrical resistivity, low loss, and lower cost at processed interposer levels. However, glass has a relatively low thermal conductivity (~1 W/m·K), compared to silicon (~150 W/m·K), which may cause thermal related problems.

The main objective of this thesis is to overcome the limitation associated with low thermal conductivity of glass, by incorporating copper structures and additional cooling technology that can spread heat efficiently. This study focuses on characterizing the effect of copper structures on the thermal performance of glass interposers, and demonstrating ultra-thin (< 1 mm) cooling device, which makes the performance of glass substrate comparable with silicon.

The first part of this research investigates the effects of copper structures, such as copper through-package-vias (TPVs), and copper traces in redistribution layer (RDL), on the thermal performance of glass interposers through numerical and experimental approaches. Numerical parametric study on 2.5D interposers shows that as more copper structures are incorporated in glass interposers, the performance of silicon and glass interposers becomes closer, showing 31% difference in thermal resistance, compared to 53% difference without any copper structures in both interposers. The numerical modeling study on glass interposers with 145 μm-thick glass substrate suggests that if the out-of-plane effective thermal conductivity of glass becomes higher than 50 W/m·K, thermal resistance of other components becomes more dominant, which results in negligible enhancement of thermal performance with further increase in out-of-plane effective thermal conductivity. In the second part of this study, a thermal model of glass interposer mounted on the vapor chamber integrated PCB is developed using multi-scale modeling. The comparison of

thermal performance between silicon and glass interposers through simulation study shows that integration of vapor chamber with PCB makes thermal performance of both interposers almost identical, overcoming the limitation posed by low thermal conductivity of glass. The third part of this thesis focuses on design, fabrication, and performance evaluation of the prototype vapor chamber embedded PCB. Copper micropillar wick structure is fabricated on PCB with electroplating process, and its wettability is enhanced by silica nanoparticle coating. Design of the wick for the vapor chamber is determined based on capillary performance and permeability test results. The thermal performance of the device is found better than copper plated PCB with the same thickness. Finally, a numerical model of vapor chamber is developed, and the results from the model compared with test results.

CHAPTER 1. INTRODUCTION

Mobile electronics are packing more features than ever before, and require higher bandwidth (10-30 GB/s) and larger memory capacity, with the same or lower power consumption. Additionally, the form factors of such devices continue to shrink, especially in thickness. In order to address these demands at a reasonable manufacturing cost, breakthroughs in packaging technologies are needed. Three-dimensional (3D) integrated circuit (IC) structures where multiple chips or dies are stacked have been considered to be an efficient solution to accomplish these goals, achieving the highest possible bandwidth enabled by the shortest interconnection length. However, there remains a number of technical challenges such as electrical interference between disparate functional blocks (RF, digital, analog, and sensors), design complexity, high cost, and thermal issue caused by high power density.

Two and a half dimensional (2.5D) Interposer packaging technology offers a way to achieve the benefits of chip-scale connected configurations without having the issues posed by 3D IC integration, and considered as a good alternative for stacked integration technology. Interposer is a packaging platform with high density of electrical connections, and it is used to fan out the electrical connections to a wider pitch, and also to route the signals between different components placed on the same interposer. Because of the high wiring density, interposers can support large number of inputs/outputs (I/Os) required by the advanced IC technology nodes.

Figure 1.1 shows the schematic of a 2.5D interposer structure, where two dies are interconnected through copper traces in the redistribution layer (RDL) on the interposer

substrate, while both dies are connected to PCB through the copper plated through package vias (TPVs).

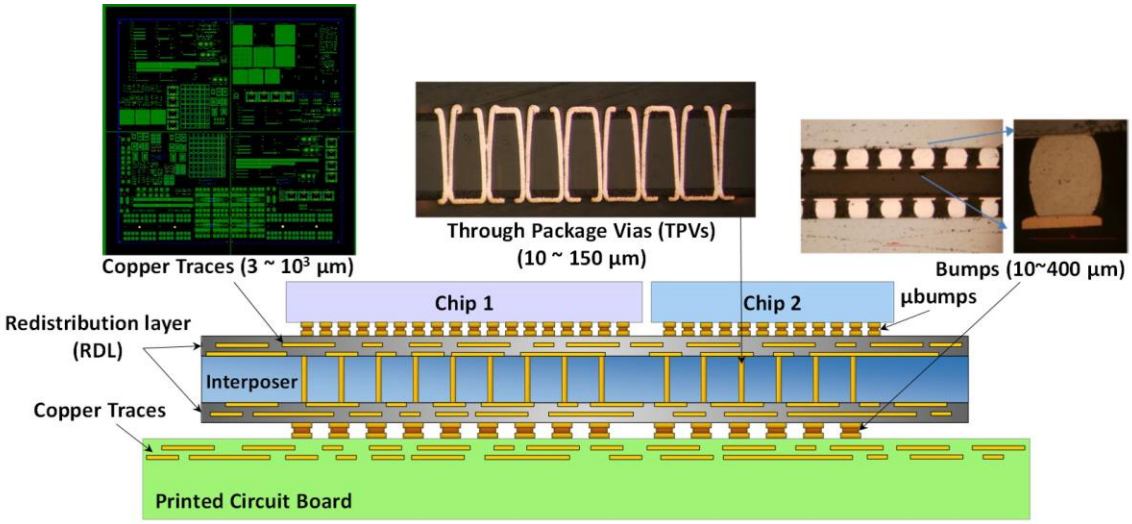


Figure 1.1 The schematic of 2.5D interposer structure. Numbers in brackets are minimum and maximum sizes of the features in each component.

1.1 Glass Interposer Technology

Silicon and glass are two major candidates for an interposer substrate. Silicon interposer has been developed to overcome the limitations of organic substrates due to many advantages, including high I/O density, high manufacturability and reliability, and high thermal conductivity. Recently, 2.5D silicon interposers have been developed by Xilinx for packaging their FPGA modules, which enables them to pack twice more logic capacity compared to any other announced 28-nm FPGAs [1]. However, the size of silicon is limited to 300 mm wafer sizes, leading to high fabrication cost per interposer. Also, its high electrical losses due to its higher electrical conductivity limit its performance. To address these issues, glass interposers are being developed [2]. Glass has the advantage of panel-based processing, which results in lower cost per interposer. Moreover, glass has

high electrical resistivity, resulting in lower insertion loss and cross-talk compared to silicon. Combined with the advantages of ultra-high electrical resistivity and low electrical losses, glass becomes an excellent interposer candidate due to its benefits in thickness, especially for mobile applications [3]. Table 1 compares electrical properties, process complexity, and cost associated with glass, silicon, and organic interposers.

Table 1.1 Comparison of different material candidates for interposer substrate

Characteristics	Required Properties	Materials		
		Glass	Silicon	Organic
Electrical	High Resistivity	Good	Poor	Good
Mechanical	High Strength High Elastic Modulus	Fair	Fair	Poor
Chemical	High Resistance to Process Chemicals	Good	Fair	Poor
Processability	Low Cost Via Formation and Metallization	Poor	Fair	Fair
Cost	Low Cost	Good	Poor	Poor
Thermal	High Thermal Conductivity CTE Match with Silicon	Fair	Good	Poor

1.2 Fundamental Challenges in Glass interposers

Despite several advantages over other materials, glass has two fundamental limitations: its brittleness and thermal conductivity (1 W/m·K) 100 times lower than that of silicon (150 W/m·K). These limitations can cause various challenges including the following:

1) Formation of defect-free TPV holes at small pitch

2) Assembly of interposer with ICs or organic package substrate

3) Thermo-mechanical reliability of TPVs

4) Thermal management of ICs on glass substrate

Recent studies have focused on addressing some of the challenges related to formation of defect-free TPV holes at small pitch [2], assembly of interposer with ICs or organic package substrate [4], and thermos-mechanical reliability of TPVs [5].

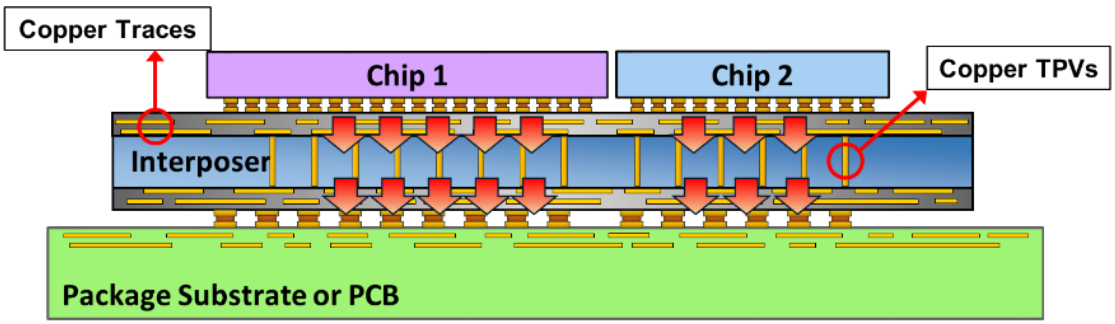


Figure 1.2 Heat flow within interposer through copper structures

This thesis focuses on addressing fundamental challenges associated with low thermal conductivity of glass, namely thermal management of ICs on glass substrate, by incorporating copper structures (TPVs and copper traces) to provide a thermal path within the package as illustrated in Figure 1.2, and integrating package substrate with thin two-phase heat spreaders which can spread the heat more efficiently than copper. The design rules governing the feasibility of such structures can be established by thermal characteristic studies through modeling and test.

The idea of using metal structures for thermal management was first adopted in the design of interconnects between the chip and printed circuit boards (PCBs). Lee et al. developed analytical closed form expressions for the thermal resistance network of metal vias between multichip modules (MCMs), which showed good agreement with experimental data [6]. Li et al. studied relationship between the thermal resistance and the via design parameters. The study shows that adding metal vias can improve the thermal

performance across the PCB by over 10 times [7]. Recent studies with thermal vias were focused on the development of algorithms for an efficient placement of thermal vias in 3D ICs, minimizing the perturbations on routing. Golpen et al. developed an algorithm to determine the optimized number of thermal vias in 3D ICs for various thermal objectives, including minimizing maximum temperature and thermal gradients [8]. Lee et al. presented a co-optimization study for interconnects in 3D ICs, considering signal, power, and thermal aspects [9].

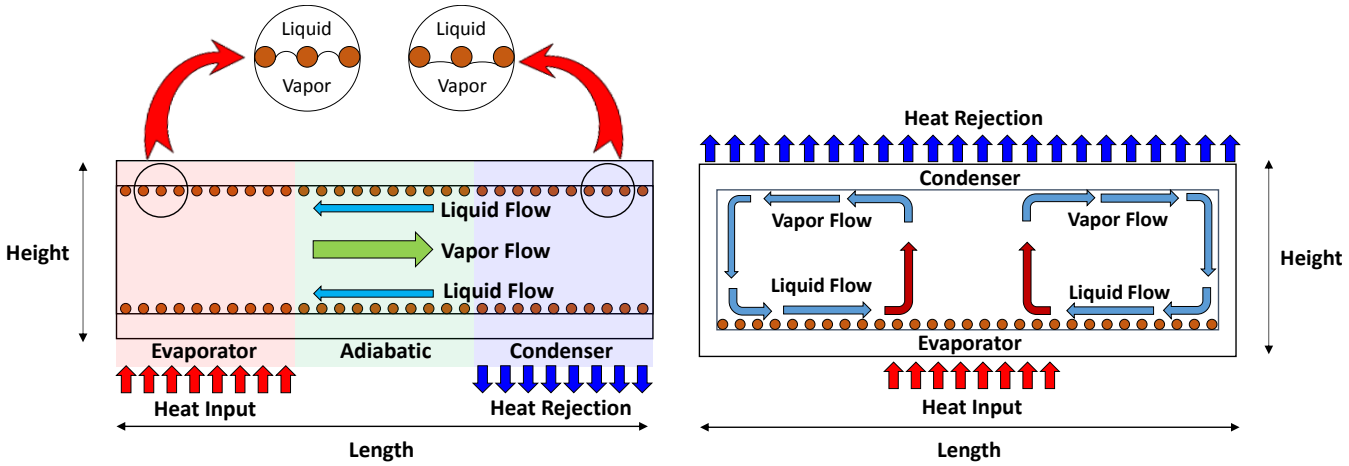
A number of studies have investigated the thermal characteristics of interposers through simulation [10],[11] Also, a few experimental thermal characterizations of interposer structures have been reported [12],[13]. Heinig et al. [14] presented thermal analysis and optimization results for various 2.5D and 3D integrated processor configurations. These results indicated that maximum total power of the processor on 25 mm$\times$16 mm interposer can be increased up to 10 W when there is convective heat removal on bottom side with an effective heat transfer coefficient of 50 W/m^2·K.

1.3 Two-phase Cooling Technologies for Electronics

Heat generation from semiconductor devices in the past was easily managed using air cooling. However, as chip heat flux increase above 100 W/cm^2, air cooled solutions become large, and acoustic noise becomes a challenge. Two phase heat transport systems have been demonstrated as an attractive advanced cooling technology for an increasing number of high power applications. Two phase heat transport systems utilize latent heat of working fluid, which usually is one or two orders larger than the sensible heat. This results in higher heat removal per unit mass of fluid than conventional air cooling technology, and gives an advantage of lower system mass and size. Another advantage of two phase cooling

systems is their temperature stability. Phase change of the liquid occurs at nearly fixed temperature, allowing such systems to operate over narrower operating temperature ranges.

The most well-known two-phase cooling device used in current consumer electronic products is the heat pipe. It is a closed pipe filled with vapor and liquid of a working fluid. The heat pipe is divided into three parts: the evaporator, adiabatic section, and condenser. Heat is externally applied at the evaporator section and is conducted through walls and the capillary wick structure to the working fluid. The working fluid vaporizes within the wick structure in the evaporator, and the resulting vapor pressure drives the vapor through the adiabatic section to the condenser, where vapor condenses, releasing the latent heat of vaporization. The meniscus of liquid-vapor interface at evaporator section is highly curved, while in the condenser section it is almost flat. The difference of menisci radius of curvature between evaporator and condenser sections causes a capillary pressure gradient along the heat pipe wick, which drives the condensate to the evaporator. This capillary driven liquid pumping continues as long as there is a sufficient capillary pressure to drive condensate back to the evaporator. Typical heat pipe has circular cylindrical shape container, but rectangular, conical, corrugated flexible heat pipe geometries have been developed and studied [15].



(a) Heat pipe (b) Vapor chamber

Figure 1.3 The schematics of (a) heat pipe and (b) vapor chamber

As indicated in Figure 1.2, the vapor chamber is a capillary-driven flat heat pipe with a very small length to height ratio compared to conventional heat pipe (CHP) geometry [16]. Vapor chambers are sometimes preferred over CHP for electronics cooling, since heat flow within vapor chamber is two or three-dimensional, which can spread and dissipate the concentrated heat over much larger area than CHP. Vapor chamber usually has wick structure only on evaporator side when the condenser is above the evaporator, as the condensed liquid on upper wall will drip back to the evaporator section. Wick structure on the evaporator side supplies liquid to localized hot spot or heat source to prevent dryout.

The thermal resistance of the vapor chamber is often dominated by the wick structure. Thin evaporator wicks with high effective thermal conductivity are desired to reduce the thermal resistance at evaporator. However, such thin wick structures suffer from low critical heat fluxes due to their large liquid hydraulic resistance. To overcome this difficulty, material with high thermal conductivity, such as carbon nanotubes (CNTs) have been tested as wick structures [17].

The ultra-thin (< 1 mm) and light vapor chambers are an appealing solution for use in cooling glass interposer package to fit in a limited space, especially for its mobile application. Moreover, passive heat spreading technologies are also preferred over active cooling systems to minimize power consumption. However, their performance needs to be high enough to dissipate high heat fluxes from small hot spots, which in turn requires careful design of their wick structures and condensers.

1.4 Research Tasks

The primary objectives of this thesis are 1) characterize the effect of copper structures on thermal performance of glass interposer and 2) develop and characterize ultra-thin (< 1 mm) packaging substrates integrated with vapor chamber for cooling glass interposer package. These objectives are accomplished through the completion of following tasks:

Task 1. Develop an experimentally validated compact thermal model of glass interposer for thermal characterization study

In order to estimate the thermal performance of glass interposer, it is important to develop an experimentally validated thermal model. Research task 1 focuses on investigating out-of-plane and in-plane effective thermal conductivity of glass substrate enhanced by copper structures such as TPVs and copper traces. To develop a numerical model of interposer package with complicated copper structures, compact thermal modeling scheme is used. The results from the model is validated against test results, and the effect of different copper structures on thermal performance of glass interposer is studied through subsequent numerical modeling.

Task 2. Predict the effect of vapor chamber integrated package substrate on thermal performance of glass interposer

A numerical model of glass interposer mounted on the package substrate, combined with vapor chamber is developed to predict its performance, and the result is compared with the result with silicon interposer. The thermal performance of vapor chamber is estimated by using an effective thermal conductivity calculated from the published thermal resistance data, in conjunction with the analytical expression of thermal resistance for a given geometry of the vapor chamber.

Task 3. Develop a vapor chamber integrated package substrate and characterize its performance

A prototype of vapor chamber integrated package substrate is designed, fabricated and tested to demonstrate its performance. The prototype is made of printed circuit board (PCB) with the thickness of 220/330 μm, and oxygen-free copper sheet with 570/950 μm thickness. Cylindrical micropillar structures with different pillar arrangements (square, hexagonal, and rectangular) and porosities (0.45/0.5, 0.6, 0.7, and 0.8) are fabricated on PCB using electrochemical process, and their hydraulic performance is characterized using capillary rate-of-rise test and forced liquid flow test. Pillar arrangement that shows the best performance is chosen as a wick structure for the prototype vapor chamber.

Hermetic sealing is an important requirement for two-phase cooling devices as both the leakage of working fluid and inflow of gases deteriorate their performances. In this thesis, the hermetic sealing is achieved by soldering copper sheet which has its periphery area plated with eutectic SnAg alloy (Sn-3.5Ag) and PCB with its copper surface finished

with electroless nickel immersion gold (ENIG) process. Due to its small volume, the amount of the working fluid charged in the ultra-thin vapor chamber is much smaller (tens of microliters) than that of working fluid in conventional heat pipes/vapor chambers. In this thesis, a peristaltic pump is used to control the volume of charging fluid with microliter-scale accuracy.

1.5 Overview of Chapters

This dissertation is organized into seven chapters. Each chapter begins with the review of relevant literature and theoretical background, followed by fabrication processes/characterization/data analysis, or details of the numerical models/result analysis.

Chapter 1 introduces 2.5D interposer packaging technology, glass interposers, the need for this research, and the research tasks to complete the objectives. Chapter 2 introduces challenges in modeling 2.5D interposers associated with multi-scale size of the components, and explains how each component is modeled using compact modeling scheme. This chapter also compares the modeling approach with test result using glass TPV samples having different via pitches, and diameters. Chapter 3 performs parametric studies with numerical model developed by using compact modeling scheme introduced in Chapter 2 to investigate the effect of different copper structures (TPVs and copper traces) on the thermal performance of glass interposers. The effect of PCB integrated with vapor chamber is also studied, and compared with thermal performance of interposers on the ordinary PCB. Chapter 4 explains the fabrication process of the package substrate integrated with vapor chamber. Details on fabrication steps and any test performed in each step are provided in this chapter, including wick structure fabrication and hydraulic performance testing, and device charging and sealing. Chapter 5 explains the test setups

for measuring thermal performance of vapor chamber. The test results of vapor chambers with different total thickness are presented and discussed. Chapter 6 explains the modeling process of vapor chamber. The code developed for vapor chamber is validated against the literature. 3D numerical model of vapor chamber integrated PCB is then developed and the results are compared with the test. Finally, Chapter 7 summarizes the key findings, research contributions, and potential extension of the research presented in the dissertation.

CHAPTER 2. THERMAL MODELING OF GLASS INTERPOSER

2.1 Compact Thermal Modeling of Electronics

The goal of compact thermal modeling is to predict sufficiently accurate thermal responses of electronic components without constructing highly geometrically detailed models. Two approaches are often used for compact modeling of electronic systems. The first represents the packaging of electronic systems as single or two thermal resistors by using analogy between heat flow and electrical current flow. For commonly used packaging configurations as shown in Figure 2.1, the junction-to-ambient thermal resistance (R_{JA}) can be used as a thermal characterization parameter. R_{JA} consisting of an internal resistance (R_{JC}), and an external resistance (R_{CA}). R_{JC} characterizes the thermal path between die and case, and R_{CA} is associated with the heat transfer between case and the coolant around the case [18]. Although the resistor model is simple and the most intuitive compact model approach, the choice of a reference temperature value becomes ambiguous when describing 3D stacked packages, and non-uniform temperature profile around chip area also poses difficulty in applying resistor concept to the model. The second approach also utilizes thermal resistor model, but reduces it to an effective thermal conductivity. Calculated effective thermal conductivity replaces the thermal properties of the materials. The advantage of this approach is that complicated geometries such as solder ball arrays can be simplified into a single block with effective thermal conductivity, which gives advantages of computational efficiency over detailed model by reducing requirements for mesh size and quality. It also captures temperature profile from non-uniform heat generation better than first approach. However, the second approach averages

out the peak temperature on the localized hot spot, which might lead to an inaccurate prediction of junction temperature. Despite this disadvantage, this approach is often used for a system level analysis to compare thermal performances of different thermal management technologies.

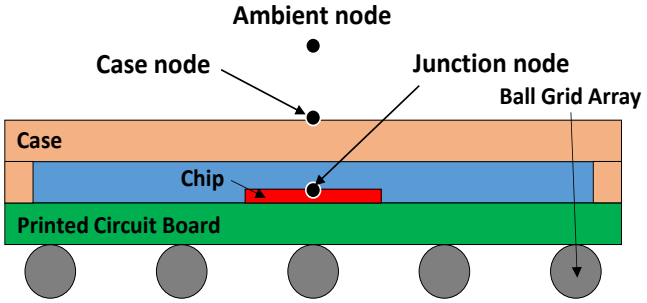


Figure 2.1 Schematic view of ball grid array (BGA) package with junction, case, and ambient nodes [14]

2.2 Compact Thermal Modeling of Glass Interposer

As shown in Figure 1.1, interposers consist of microbumps, interposer substrate, TPVs, and bumps. Bumps are used for forming electrical connections with small bump pitches (~500 µm), and microbumps are miniaturized bumps with pitches less than 50 µm, designed to provide high wiring density in chips. Top and bottom surfaces of the interposer substrate are laminated with dielectric layers, which work as buildup layers for wiring, referred to as redistribution layers (RDLs). Complicated copper traces are buried in the RDLs and connected to enable communication between different chips mounted on the interposer. There are through package vias (TPVs) in the interposer substrate, which pass completely through the substrate for vertical electrical connection between chips and package substrate. The TPVs are either partially or fully filled with copper. Figure 1.1 and Table 2.1 compare the various length scales of different components in interposer. When including all the fine details of interposers in the model results in need of extensive

computational time and resources to solve the simulation. As such, a compact or reduced order modeling methodology is needed. Over-simplification of the geometric features, however, can produce large errors in predicting temperature profile of the system.

Table 2.1 Geometric dimensions of chip, interposer and printed circuit board (PCB)

	Size (Width(mm) x Length(mm) x Height (mm))
Chip	10 x 10 x 0.5
Interposer	25 x 25 x 0.2
Printed Circuit Board (PCB)	50 x 50 x 1.2

Several numerical simulations have been carried out to study the temperature distribution within 2.5D and 3D ICs with through silicon vias (TSVs) by using the second approach. Ma et al. proposed a simplified thermal model for TSVs in interposer by using effective thermal properties [19]. The accuracy and the application limits of the developed compact model were presented, along with the volume ratio of copper and the silicon. Lau et al. studied the thermal performance of 3D IC integration system-in-package (SiP) with TSVs through modeling [20]. The study presented the effect of various parameters, including TSV filler material, diameter, pitch, and aspect ratios, on the thermal resistance of the interposers. While a number of works have been reported on the thermal characterization of silicon-based 2.5D and 3D integration technologies, thermal studies on glass based integration technologies are currently lacking.

2.2.1 Compact thermal modeling of microbump/TPV/bump

Microbump/TPV/bump arrays are modeled by simplifying the geometry into an equivalent block with effective thermal conductivity. Figure 2.2 summarizes the compact modeling procedure used for TPV array. To begin with, a unit cell of TPV is chosen, and

thermal boundary conditions to calculate effective thermal conductivity are applied to this cell.

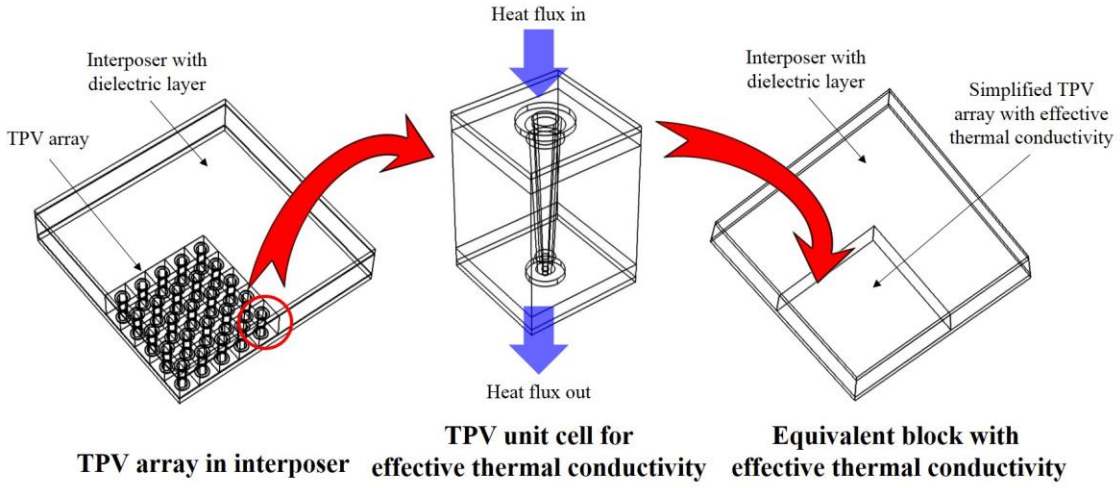


Figure 2.2 Compact modeling scheme used for TPV modeling. Upper part of TPV array is connected to microbumps, and lower part is connected to bumps.

Out-of-plane (z direction) effective thermal conductivity is calculated by imposing uniform heat flux condition at top and negative heat flux at bottom surface, while surrounding surfaces are set as adiabatic. The average temperatures of the top and bottom surfaces are obtained and consequently the equivalent thermal conductivity is calculated using

$$k_{eff} = Q'' \frac{\Delta x}{\Delta T} \tag{1}$$

Where Q'' is the heat flux, Δx the thickness of the sample, and ΔT the temperature difference across it. In-plane (x-y direction) effective thermal conductivity is calculated by applying the same boundary conditions to two side walls, while the other boundaries are kept as adiabatic. This approach averages local hot spot temperature, which may underestimate the peak temperature. However, using average die temperature is still a valid approach to evaluate and compare thermal characteristics of electronics packaging while a

uniform heat generation is assumed. The approach was validated under uniform heat generation boundary condition by comparing the simplified model with detailed model, which showed only ~1% difference between maximum temperatures predicted by the two models. More detailed validation of the approach under various geometric conditions is provided in the literature [19].

2.2.2 Compact modelling of copper traces

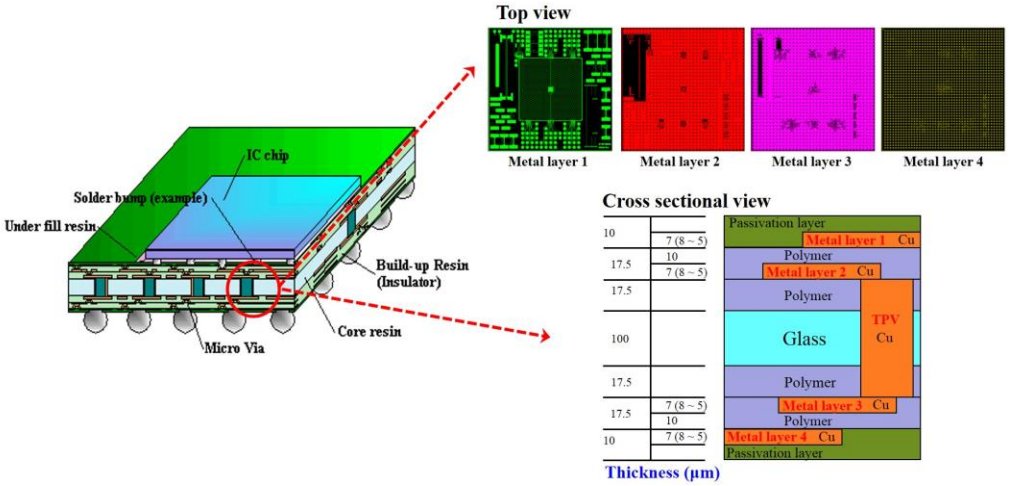


Figure 2.3 Glass interposer substrate with single chip (left image from http://www.shinko.co.jp/english/product/buildup/dll.html), top view of example metal layers' layout, and cross-sectional view of TPV and metal layers (right).

In a redistribution layer (RDL), copper traces are patterned in a sophisticated way to enable I/O layout, and they fan out from the chips to a looser pitch footprint. Such redistribution requires thin film polymers such as dielectric layers, and metallization to enlarge the pitch of the chip I/Os to match that of another array configuration with larger pitch. Figure 2.3 shows a top view of the four example metal layers with different patterns,

and a cross-sectional view of TPV and copper traces patterned in a glass interposer substrate with single IC chip.

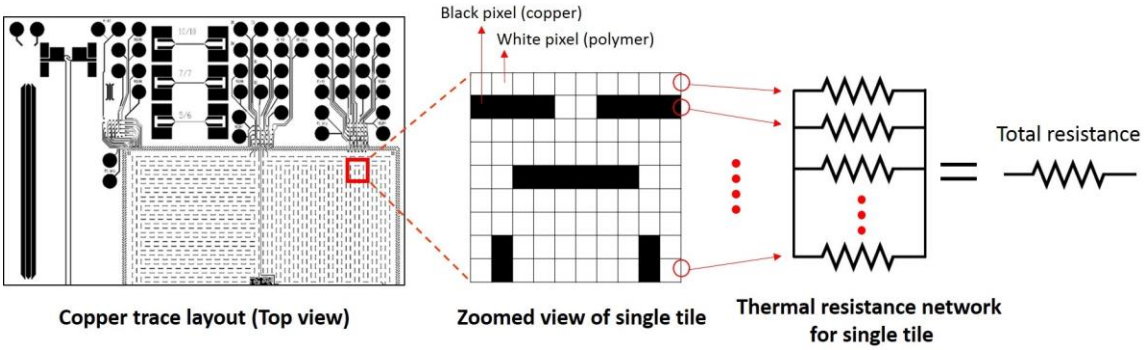


Figure 2.4 Determination of total thermal resistance to obtain in-plane effective thermal conductivity for compact modeling of metal layer.

Figure 2.4 explains how in-plane effective thermal conductivity is calculated for metal layer with copper traces when the layers are assumed to be orthotropic. First, the CAD drawing of a metal layer is converted to a binary image, which contains the size and location information of the copper traces and the polymer. A black pixel in the Figure 2.4 represents copper, and the white pixel represents polymer. Then, the layout is divided into small tiles and each tile's total thermal resistance is obtained by using thermal resistance network analysis. Out-of-plane thermal conductivity of metal layer is calculated with the assumption that black and white pixels are thermally parallel. Pixel resolution of the image is considered acceptable when the difference between calculated effective thermal conductivity from current image and the highest resolution image that CAD program could export is less than 5 %. Generally, 25 times reduction of pixels from maximum resolution results in ~4% difference between the results.

Equation (2) and (3) are used to calculate in-plane (row: x-direction, column: y-direction) and out-of-plane (z-direction) effective thermal conductivity, respectively.

$$R_{row/column} = \frac{(Number\ of\ white\ pixels) \times (Pixel\ size)}{k_{polymer} A_{row/column}} + \frac{(Number\ of\ black\ pixels) \times (Pixel\ size)}{k_{copper} A_{row/column}}$$

$$R_{total} = \frac{1}{\sum (1/R_{row/column})} \qquad (2)$$

$$k_{in-plane} = \frac{L_{total}}{A_{total}} \sum (1/R_{row/column})$$

$$R_{total} = \frac{1}{1/R_{copper} + 1/R_{polymer}}$$

$$k_{out-of-plane} = \frac{A_{copper}}{A_{total}} \times k_{copper} + \frac{A_{polymer}}{A_{total}} \times k_{polymer} \qquad (3)$$

The tile with complicated copper traces is then converted into a simple block with calculated effective thermal conductivities along x, y, and z direction. More details and the validation of this approach are presented in [21].

2.2.3 Thermal conductivity measurement of glass interposer components

Prior to develop a numerical model of glass interposer package, out-of-plane thermal conductivity of polymer is experimentally determined by using IR microscopy. The Quantum Focus Instruments (QFI) Infrascope II infrared (IR) microscope is used for the measurements. The IR imaging is performed using the IR microscope's 15X objective lens, which has a spatial resolution of 2.8 μm and a pixel size of 1.6 μm. The temperature resolution is approximately 0.1 °C.

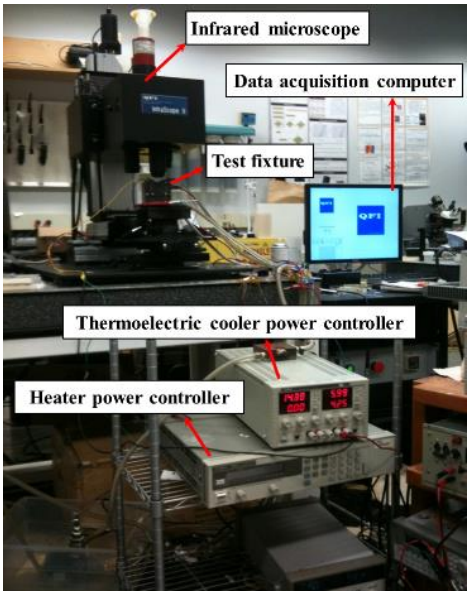


Figure 2.5 Setup for out-of-plane thermal conductivity measurement

Figure 2.5 shows the experimental setup for thermal conductivity measurement. For the measurement, separate test fixture (Figure 2.6) is machined to observe the temperature gradient along the edges of the samples with 1 cm by 1 cm size. Sample is first placed in the test fixture which is equipped with ceramic heater (Barry Industries) and thermoelectric cooler. Then the test fixture is mounted on the IR microscope stage. A water-cooled heat sink is used to remove the heat from the thermoelectric cooler. An Agilent 34970A Data Acquisition/Switching unit reads the thermocouples which are strategically placed to confirm the temperature reading from IR microscope. The cooling water, which flows through the water heat exchanger to cool down the test fixture temperature, is pumped through the system using RM6 Lauda constant temperature bath. The heater power is supplied through an Agilent System 6644A DC Power Supply. A Hewlett Packard E3632A DC Power Supply controlled the thermoelectric cooler.

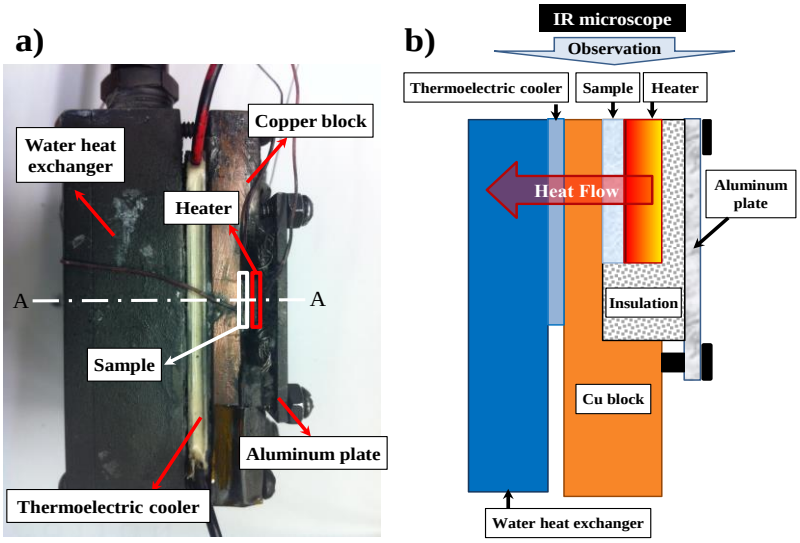


Figure 2.6 a) Top view of test fixture and b) cross-sectional view of section A-A.

Figure 2.6 a) shows a top view of the sample fixture and b) shows a cross sectional view taken along the line A-A in a). A ceramic heater which corresponds to the sample size is used to heat up one side of the sample. The other side of the sample is cooled down by the thermoelectric cooler, attached to a copper block.

Two 1 cm by 1 cm polymer and glass samples are prepared, and placed between a copper block and a heater so that one edge of the sample is exposed for measurements. Unexposed edges are insulated to ensure unidirectional heat conduction. Thermal grease is applied at the heater/sample and sample/copper block interfaces to reduce temperature drops at the interfaces. An aluminum plate is used to firmly fix the sample within the fixture. Once the sample is mounted, its exposed part is coated with carbon spray to keep its emissivity high enough to reduce the experimental uncertainty.

The sample and copper block are heated by a thermoelectric unit until they reach a steady state temperature. Radiance is measured to generate reference emissivity map of the sample and is used to determine temperature distribution along the thickness of the sample. Following the reference emissivity mapping, the heater is turned on to heat one side of the

sample, and the thermoelectric cooler to cool the other side and copper block. The power supplied to the heater is used for heat flux calculation and the thermocouple measurements are used to ensure that the system has reached the steady state. The IR microscope measures temperature distribution of the sample based on the radiance and emissivity map previously recorded.

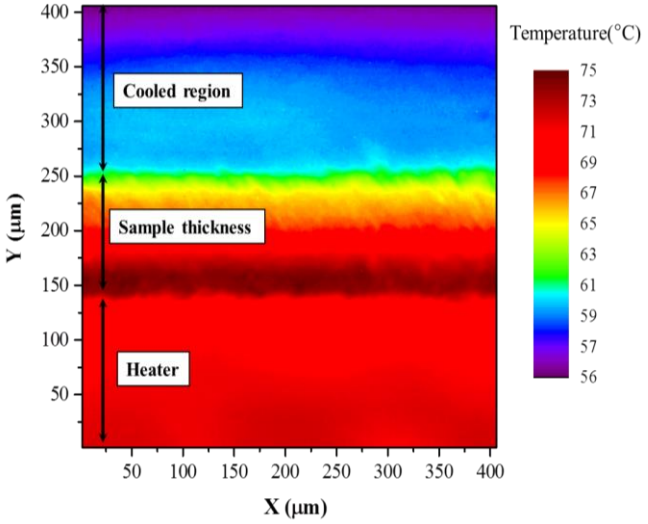


Figure 2.7 Temperature map from IR microscope measurement.

Figure 2.7 shows the temperature distribution measured at the edge of the polymer sample and its surroundings. The temperature change shows almost linear behavior across the sample thickness, between 150 μm and 250 μm region, which corresponds to the sample thickness of 100 μm. The temperature readings of the pixels locating at the same Y axis are averaged for thermal conductivity calculations. The heat flux Q'' generated by heater is calculated by

$$Q'' = \frac{VI}{A} = \frac{I^2 R}{A} \tag{4}$$

where I is the current supplied to the heater, R its resistance, V the voltage readout from the power supply, and A the cross-sectional area of the sample. Thermal conductivity, k, can be determined by Equation (1).

Thermal conductivity of each sample is measured for four different heat fluxes. The uncertainty of the thermal conductivity is determined by Equation (5).

$$U_k = \left\{ \left(\frac{\partial k}{\partial (Q/A)} U_{Q/A} \right)^2 + \left(\frac{\partial k}{\partial (\Delta x)} U_{\Delta x} \right)^2 + \left(\frac{\partial k}{\partial (\Delta T)} U_{\Delta T} \right)^2 \right\}^{1/2} \quad (5)$$

where U is uncertainty. Table 2.2 shows the measured thermal conductivity values of samples and their comparison with manufacturer's value. Comparison results show that the measured thermal conductivities are in reasonable agreement with suppliers' data, showing 4% and 15% difference for each different sample. More details about thermal conductivity measurement technique using IR microscope can be found from [22].

Table 2.2 Measured thermal conductivity of samples

	Measured Value (W/m·K)	Reported Value (W/m·K)
Polymer 1	1.05±0.02	N/A
Polymer 2	0.52±0.01	0.50
Glass	1.15±0.04	1.00

2.2.4 Effective thermal conductivity measurement of copper TPVs

To validate compact thermal modeling scheme used for TPVs, the effective thermal conductivity of glass sample with copper TPVs is measured and compared with the result from numerical model.

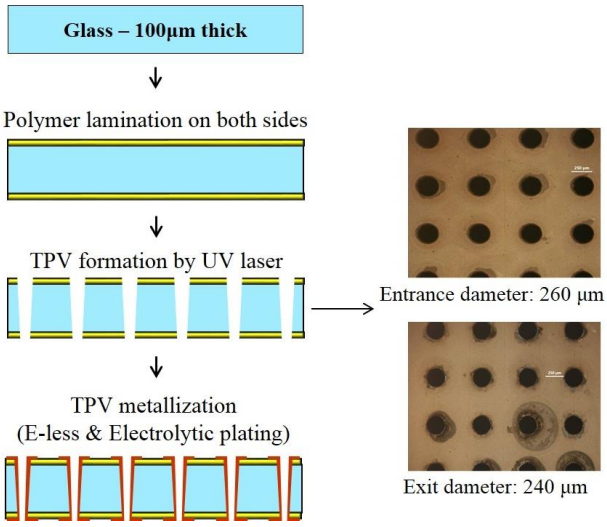


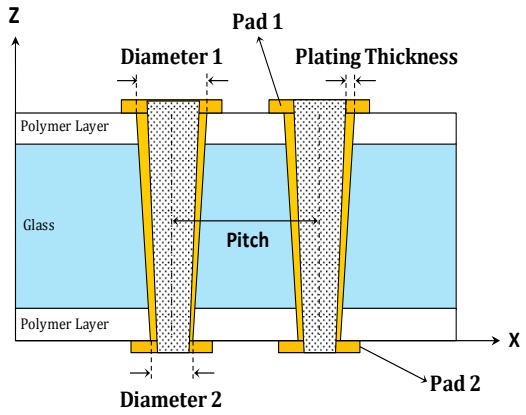
Figure 2.8 Process flow for glass TPV sample fabrication.

TPV via arrays with different diameters and pitches are fabricated on a 114 mm × 114 mm × 100 µm borosilicate glass panel. Prior to via drilling, both surfaces of the panel are cleaned with acetone and isopropyl alcohol (IPA). Then both sides are laminated with 22.5 µm-thick dielectric polymer layers. A hot press machine is used during the lamination process with optimized temperature and time settings. The laminated polymer layer serves as a buildup layer for wiring, and also as a buffer layer which reduces the impact of laser on glass during the ablation process. The laminated glass sample is then subjected to ultraviolet (UV) laser ablation for via formation. The UV laser drilling results in tapered via profiles.

Figure 2.8 summarizes the process flow used for the test sample fabrication. It also shows the optical images of glass samples' via entrance and exit formed by UV laser ablation. To achieve good metal adhesion to the glass panel, the surface of polymer is roughened through micro etch processes. A 1 µm copper seed layer is formed on the roughened surface through electroless copper deposition, followed by electrolytic copper plating processes which results in final copper layer thickness of 10 µm. After having via

side walls plated, via pads are patterned by using photolithography. Via pad diameter is designed to be 40 µm larger than each via diameter. Table 2.3 summarizes the via dimensions of fabricated via arrays including entrance and exit via diameters, pitches, plating thickness, pad size, and the number of vias. After patterning the via pads, the panel is diced into 10 pieces of 2.54 mm × 2.54 mm size glass samples with TPV arrays having different via parameters.

Table 2.3 TPV geometry and dimensions



Diameters (1 & 2)	Pad (1 & 2)	Pitch	# of vias
1:100 µm, 2: 70 µm	1: 140 µm, 2: 110 µm	200 µm	144
1: 180 µm, 2: 160 µm	1: 220 µm, 2: 200 µm	400 µm	36
1: 260 µm, 2: 240 µm	1: 300 µm, 2: 280 µm	600 µm	16

To measure thermal conductivity of via samples, a heater assembly is fabricated, which consists of a heater and a PCB. The size of the heater is 2.54 mm × 2.54 mm, which corresponds to the sample size with 100 µm thickness. The heater is comprised of two resistors, each able to dissipate a maximum power of 6 W and is wire bonded to the PCB for power supply connection. Two diodes placed at the center and the edge of the heater are utilized for surface temperature measurements. The heat generating surface of the

heater is exposed to ambient, and its other sides are surrounded by epoxy with wire bonds. The epoxy protects the heater and wirebonds from mechanical and electrical impact and also minimizes heat loss from the surfaces of heater. After the epoxy is cured, the heater diodes are calibrated by putting the assembly in a large oven. A via patterned glass sample of the size of 2.54 mm × 2.54 mm is attached to the heater by using thermal adhesive pad. After the sample is attached to the heater, the assembly is covered with an insulation material to reduce heat losses through convection and radiation to the ambient.

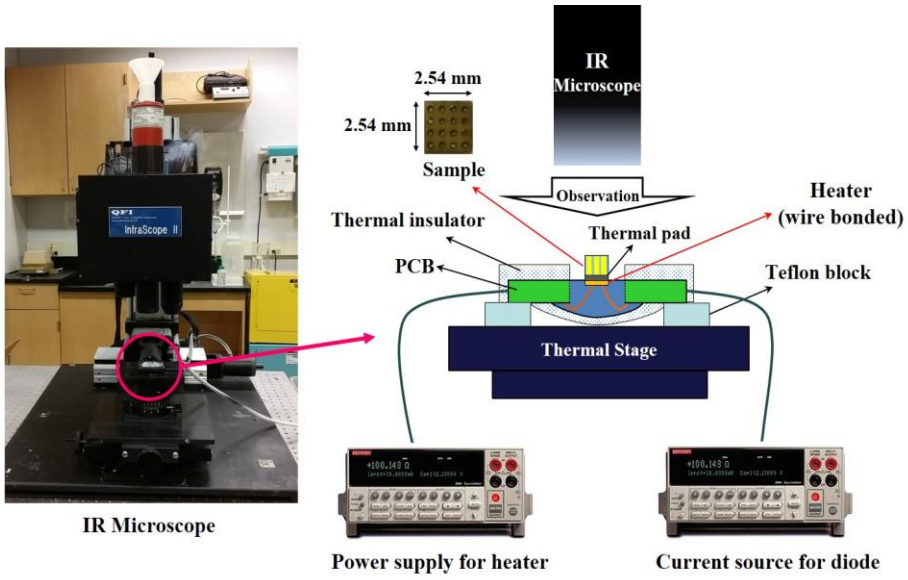


Figure 2.9 Schematic of test setup to measure effective thermal conductivity of glass samples with copper TPVs

Figure 2.9 shows the schematic of test setup used to measure the effective thermal conductivity of glass samples with copper TPVs. A QFI IR microscope is used to measure surface temperature of the sample. The heater assembly is mounted and tightly fixed on the thermal stage of IR microscope by using Teflon blocks. Two source meters are

connected to the heater assembly to supply power to the heater, and to provide constant current source (1 mA) to diodes.

Six additional thermocouples are attached to the PCB and the epoxy area to estimate the amount of heat dissipated through conduction. Prior to the measurements, the surface of the sample is coated with a black carbon spray to reduce the uncertainty in the measurement.

Heat loss through epoxy is estimated by using thermal resistance analysis, including spreading resistance and calculated to be ~ 14% of total power input of the heater. Heat loss through convection Q_c is estimated by using Equation (6) and its heat transfer coefficient h_c is calculated using Equation (7) for small devices in natural convection [23].

$$Q_c = h_c A \Delta T \tag{6}$$

$$h_c = 0.83 f (\Delta T / L_{ch})^n \tag{7}$$

where ΔT is temperature difference between the surface and the ambient, L_{ch} is the characteristic length, f=1 and n=0.33 for horizontal plate facing upward. Heat loss through radiation Q_R is estimated by using the expression for a small surface in large surroundings:

$$Q_R = \varepsilon \sigma A (T_{surf}^4 - T_{sur}^4) \tag{8}$$

where T_{surf} is sample's surface temperature (~ 343 K) at targeted heater power level, T_{sur} is the surroundings temperature, ε (~0.8) is emissivity measured by infrared microscope system, and σ is the Stefan-Boltzman constant (5.67×10^{-8} W/m^2·K^4). Total heat losses through convection and radiation were found to be ~ 5% of total heater power.

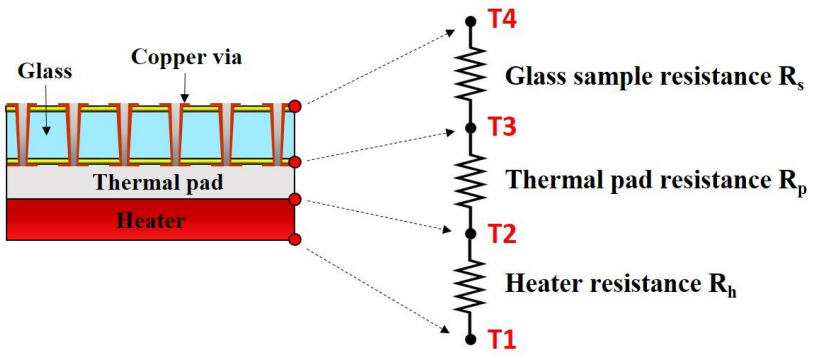


Figure 2.10 Thermal resistance network of sample stack-up on heater.

Figure 2.10 shows the thermal resistance network of the via sample stack-up on heater. Heater resistance R_h and thermal pad resistance R_p were measured separately prior to each stack-up to determine T3. The average surface temperature of the sample, T4 was measured by the IR microscope. Finally, the effective thermal conductivity of the glass sample was calculated using Equation (1) with ΔT calculated from T3-T4.

Figure 2.11 shows steady state infrared images of the glass samples with different via patterns heated from the back side. In each image, copper pads show the highest temperature due to high thermal conductivity compared to polymer-laminated glass around them. However, the temperature profile along the copper pad was not symmetric, a trend observed for all samples.

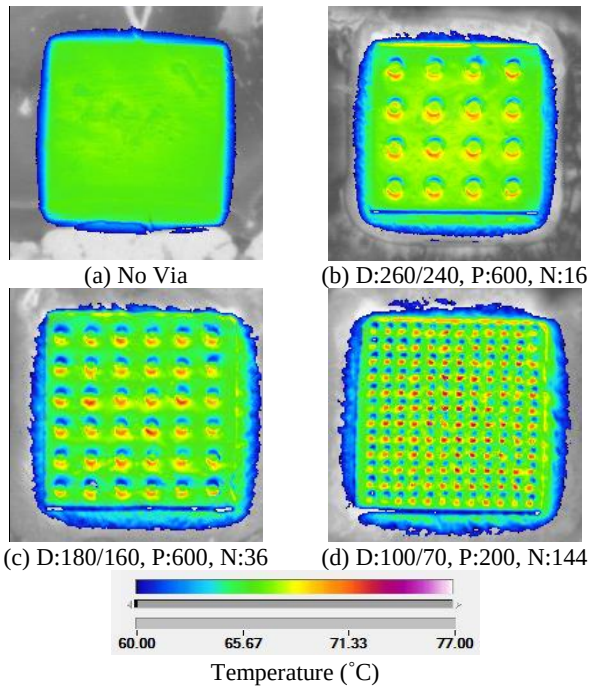


Figure 2.11 Surface temperature profile of (a) Sample 1, (b) Sample 2, (c) Sample 3, and (d) Sample 4 measured with Infrared microscopy. (D: diameters of vias, P: pitches of vias, and N: numbers of vias).

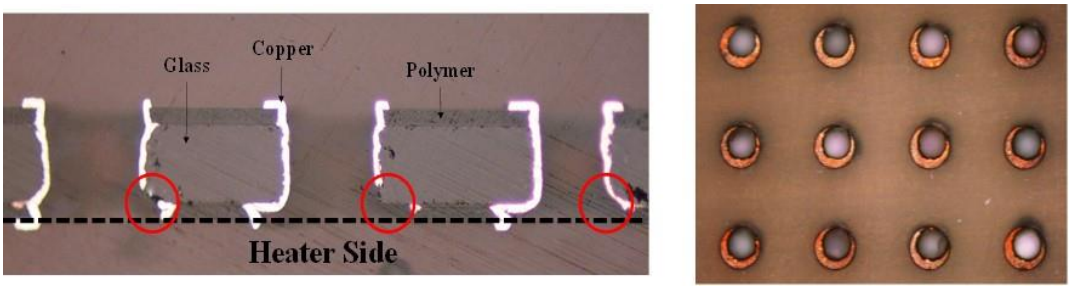


Figure 2.12 Cross-sectional view (left) and top view (right) of Sample 3.

From the cross-sectional and top view images shown in Figure 2.12, it is observed that copper is not evenly plated at the heater side of each TPV, which causes a poor thermal contact between heater and sample. A likely cause is the misalignment of the TPV mask with glass panel during photolithography. This additional interfacial thermal resistance between the sample and heater is thought to be the major reason for the non-uniform temperature profile along the edge of the TPV in IR images.

Table 2.4 compares the effective out-of-plane thermal conductivity of four samples. Volume percentage of copper in each sample is also presented in Table 2.4 to confirm the effect of copper volume on the effective thermal conductivity of glass substrate. Results for samples 2, 3, and 4 are compared with the simulation results from single via analysis using compact thermal modeling, while sample 1 simulation is compared with test result measured using the test section introduced in previous section. Sample 2 and 3 show large differences (~36 and ~39%), while sample 4 shows the least (~5%). Several factors including additional heat loss, quality of thermal contact between each layer in the samples, and copper plating quality, can contribute to the discrepancy.

Table 2.4 The comparison of the measured out-of-plane effective thermal conductivities of the glass samples with simulation.

	Diameter 1&2 (μm)	Pitch (μm)	# of vias	Model Prediction (W/m·K)	Test Data (W/m·K)	Copper Volume (%)
Sample 1	N/A	N/A	0	1.1	1.21 ± 0.35	0
Sample 2	260/240	600	16	7.52	4.76 ± 0.50	3
Sample 3	180/160	400	36	10.9	6.62 ± 1.02	4.5
Sample 4	100/70	200	144	19.5	18.3 ± 3.07	8.5

From the test and simulation results, shown in Table 2.4, the implementation of 144 copper vias with a diameter of 100 μm at a pitch of 200 μm in 2.54 mm by 2.54 mm area increases the out-of-plane thermal conductivity of glass substrate by ~ 20 times compared to its original property (1 W/m·K).

One of the sources of the discrepancy between the test and simulation for Sample 2 and 3 is copper plating quality. Based on the copper plating quality condition acquired from the cross sectional, top and bottom images of the samples, new via models are developed. Figure 2.13 shows two different via models with different copper plating

conditions of vias in original model and corrected model. Another source of error can be the contact resistance between the thermal adhesive and the sample, which is neglected in the model. To evaluate the effect of the contact resistance on the discrepancy between modeling and test results, the contact resistance of the same adhesive material (RTV silicone) from the literature [24] is used, assuming that the contact conditions between the sample and the adhesive are similar.

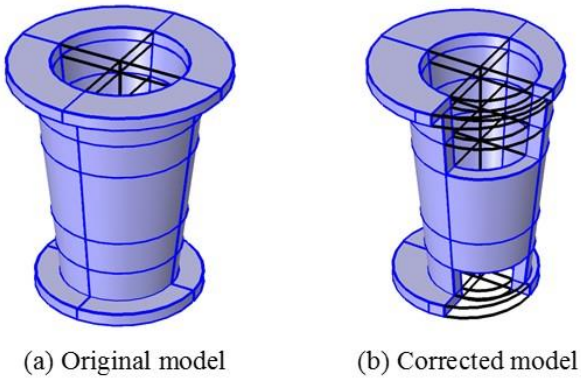


Figure 2.13 Copper plating condition of vias in (a) original model, and (b) corrected model.

Table 2.5 The percentage error between calculated effective out-of-plane thermal conductivity from models and measurements for sample 2 and 3.

	Error (%)		
	Original Model	Copper Plating Condition Corrected Model	Contact Resistance Applied Model
Sample 2	36 %	22 %	8 %
Sample 3	39 %	24 %	5 %

Table 2.5 shows the error (%) calculated after comparing the effective out-of-plane thermal conductivity from original, copper plating condition corrected, and contact resistance applied model with test results. The errors (%) for sample 2 and sample 3

decrease as the models get corrected, which shows that these two factors can be the major causes of the discrepancy. To get more accurate test results, the contact resistance of each sample needs to be measured.

CHAPTER 3. THERMAL PERFORMANCE OF GLASS INTERPOSER

In this chapter, the effect of different copper structures (TPVs and copper traces) on the thermal performance of glass interposers is studied using numerical model developed with compact modeling scheme. To enhance the thermal performance of glass interposers, the concept of PCB integrated with vapor chamber is proposed, and the effect of vapor chamber is also studied.

3.1 The Effect of Copper Structures on Glass and Silicon Interposers

3.1.1 The effect of copper TPVs with ground plane

Prior studies have shown that the thermal conductivity of substrate does not affect the thermal performance of interposer significantly as most of the heat generated from chips is dissipated through the back of the chip to the lid or heat sink [25]. In this study, interposer structures without heat sink are considered for low power application (3 W) to show the effect of interposer components on thermal performance. By using an equivalent interposer model with effective thermal conductivities for copper TPVs, 2.5D glass interposer is developed. The interposer model consists of 5 major components; chips, microbumps, interposer, bumps and PCB. Several assumptions are made in the modeling of each component as geometric details and arrangements of TPVs are dependent on the floor planning of the dies and signal assignment. General assumptions made for current simulation studies are as follows:

1) Both chips on the interposer have identical size (10 mm by 10 mm) and heat generation.

2) Chips are modeled as two blocks which have uniform volumetric heat generations and the distance between the two chips is fixed at 100 μm.

3) Microbumps under the periphery area of the chips have smaller pitch than those in the center area and are assigned for signal delivery between dies.

4) Microbumps under the center area of the chips (9mm by 9 mm area) are directly connected to copper TPVs. TPVs are also connected to bumps directly for ground connection to PCB.

5) 20% of TPVs are assigned as ground TPVs. The ground TPVs are connected to copper vias in PCB, which are directly connected to a ground plane.

6) One ground plane is embedded in PCB. It has the same size as PCB (50 mm by 50 mm) and the thickness of 0.5 oz. (~ 18 μm). A power layer in PCB is not considered in the model.

7) As the number of interconnects increases or decreases, the number of TPVs also increases or decreases for increased-decreased signal delivery. To control interconnects and TPVs together, 4 microbumps are assumed to be connected with 1 TPV, and 2 TPVs are connected with 1 bump. For ground via connection, each bump is mapped one-to-one to copper vias in PCB. Ground TPVs are assumed to be placed under the center of the chip area.

8) All heat generated from chip (3 W) is assumed to be conducted through components and dissipated at the bottom of PCB, which has its bottom plane temperature fixed at 300 K.

Based on above assumptions, parametric design study on silicon and glass interposers is performed to characterize the effect of copper TPVs and copper ground plane.

The purpose of the first simulation is to compare the effect of copper TPVs on the thermal performance of silicon and glass interposers. The model does not include the effect of copper traces within RDL in the interposer or PCB and focuses only on the effect of copper vias and single copper ground plane on the thermal performance of interposer.

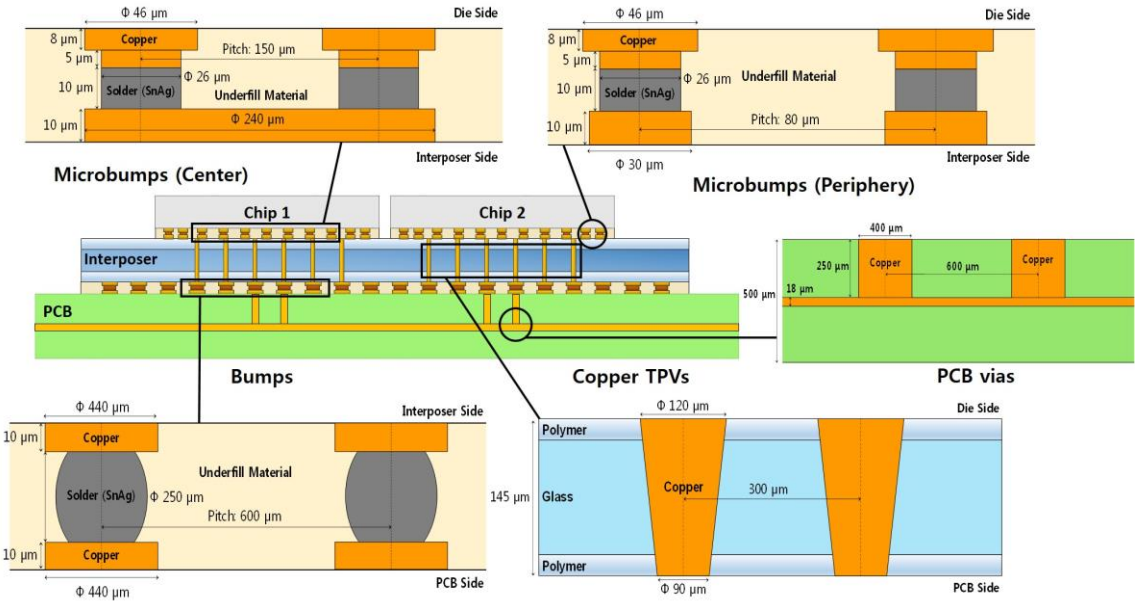


Figure 3.1 Schematic drawing of 2.5D interposer and geometric dimensions of microbumps, TPVs, and bumps used for modeling.

The geometric details of the model are summarized in Figure 3.1. Dimensions of chips, interposer and PCB, and the number of interconnects/vias are tabulated in Table 3.1. Table 3.2 summarizes material thermal conductivities. As a baseline, silicon and glass interposer structures without copper TPVs and ground plane are considered and the maximum temperature of each structure is compared with each interposer structure having

vias and ground plane implemented. TPV shape, diameter and total substrate thickness are kept the same for silicon and glass interposers as shown in Figure 3.1 and 3.2. The thickness of polymer layers in glass interposer is 22.5 μm, which corresponds to the thickness of the polymer laminated on the sample. As shown in Figure 3.2, the SiO_2 layer thickness in Si interposer is modeled as 1 μm, which corresponds to the typical dielectric layer thickness on a silicon interposer.

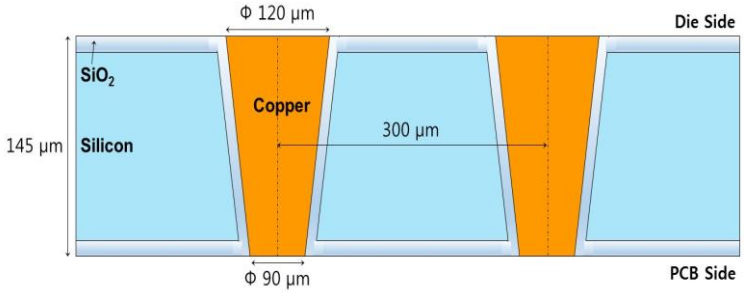


Figure 3.2 Geometric dimension of TPV in silicon interposer

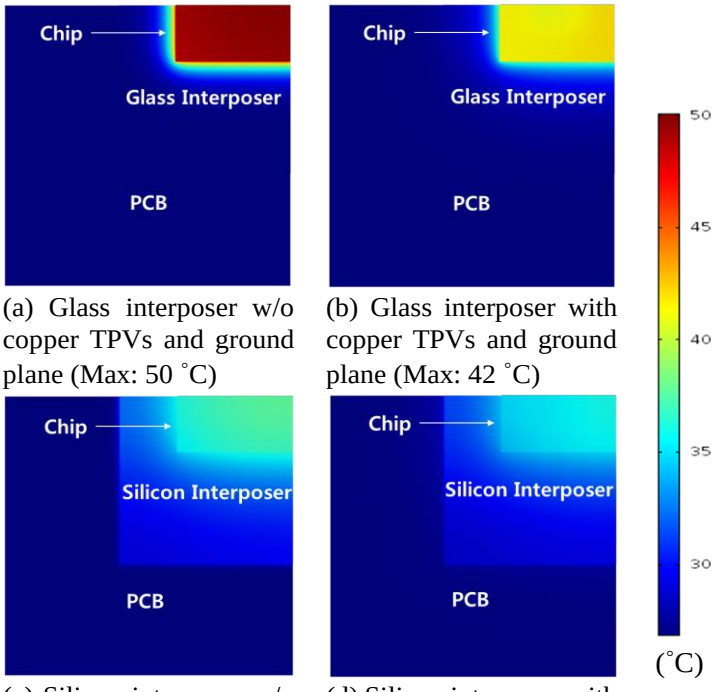
Table 3.1 Geometric dimensions of interposer components

	Length (mm)	*Width (mm)*	*Thickness(μm)*	*Count*
Chips	10	10	500	2
Interposer	25	25	220/182	1
PCB	50	50	500	1
	Dimensions			*Count*
Microbumps	Figure 3.1			Center:3600 Periphery:1900
Vias	Figure 3.1			900
Bumps	Figure 3.1			2500

Table 3.2 Material properties and calculated effective thermal conductivities of interconnects and TPVs

	k_{xy} *(W/m·K)*	k_{zz} *(W/m·K)*
Silicon	130	130
Glass/Polymer/ Underfill material	1	1

SiO_2	1.4	1.4
Copper	400	400
PCB	0.3	0.3
Microbumps	2.8	4.4
Bumps	1.8	4
TPV(Glass)	1.2	33.7
TPV(Silicon)	119.8	87.3



(a) Glass interposer w/o copper TPVs and ground plane (Max: 50 ˚C)

(b) Glass interposer with copper TPVs and ground plane (Max: 42 ˚C)

(c) Silicon interposer w/o copper TPVs and ground plane (Max: 38 ˚C)

(d) Silicon interposer with copper TPVs and ground plane (Max: 36 ˚C)

Figure 3.3 Surface temperature profile of glass interposer ((a) and (b)), and silicon interposer ((c) and (d)) with different via and layer condition

Figure 3.3 compares the surface temperature profile and the maximum temperature of the two interposers for two different cases, when each chip generates 1.5 W. Due to symmetry, only a quarter of the geometry is considered and is shown in the figure. Without copper TPVs and ground layers, glass interposer shows 32% higher maximum temperature than silicon interposer. Glass substrate shows similar temperature with PCB, as glass impedes the heat being conducted through the substrate. Silicon interposer, however,

decreases chip temperature, resulting in substrate temperature higher than glass interposer. The difference in maximum temperature between glass and silicon interposers decreases after TPVs and ground layer are implemented in both interposers as shown in Figure 3.3 (b) and (d). The glass interposer shows 17% higher maximum temperature than silicon interposer. The results indicate that the copper TPVs in glass interposer perform more effectively than those in silicon interposer.

Table 3.3 Pitch/count and normalized Θ_{jb} of microbumps, TPVs, and bumps for 3 cases. Each thermal resistance is normalized by the resistance value from case 1.

	µbumps (Center)	TPVs	Bumps	Normalized Θ_{jb}
	Pitch(µm) /Count	Pitch(µm) /Count	Pitch(µm) /Count	
Case 1	150/3600	300/900	600/2500	1
Case 2	100/8100	200/2025	400/5625	0.94
Case 3	80/12544	160/3136	320/8649	0.91

To characterize the effect of interconnects and TPVs on glass interposer, further analyses of the effect of pitch are performed based on assumption 7. Three cases with different numbers of interconnects and TPVs are considered for glass interposer structure. Table 3.3 lists the numbers and the pitches used for 3 different cases. Other geometric features and dimensions remained the same as shown in Figure 3.1. During the simulation, only the pitch of microbumps in the center area is varied, and outside of it is kept constant as 80 µm. Total number of microbumps in the periphery area is 1,900. To compare thermal performance of different packages, junction-to-board thermal resistance, Θ_{jb} is used, which is defined as:

$$\Theta_{jb} = \frac{T_j - T_b}{Q} \tag{9}$$

where T_j is junction temperature, T_b is board bottom temperature, and Q is total heat generated from the chips. Table 3.3 also compares junction-to-board thermal resistance in 3 cases by normalizing them with maximum value from case 1. As the number of interconnects and TPVs increased, the thermal performance of glass interposer also increased, but its effect was not significant. Case 3 showed 9 % better thermal performance than case 1 by having ~3.5 times higher number of interconnects and TPVs.

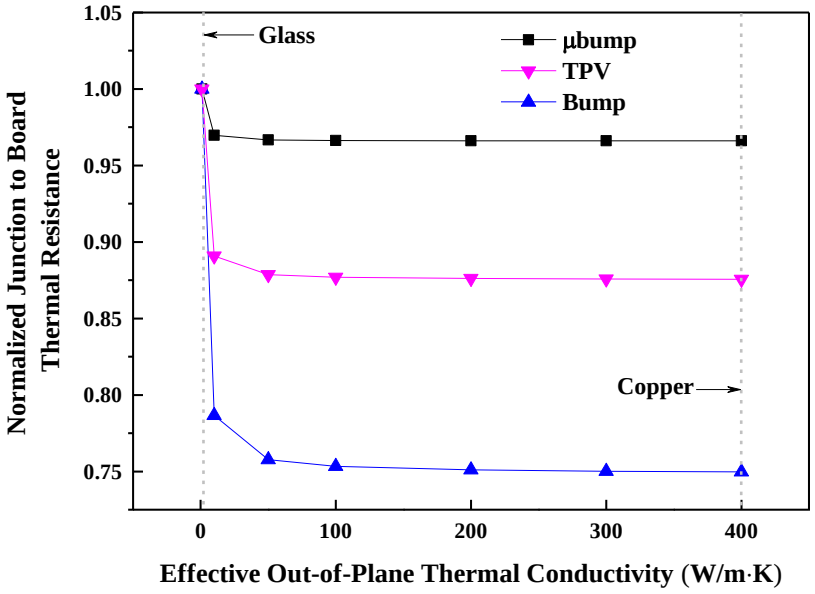


Figure 3.4 Normalized junction to board thermal resistance with different effective out-of-plane thermal conductivities of 3 components (microbumps, TPVs, and bumps). Each component's resistance is normalized by its maximum value.

Figure 3.4 shows the thermal performance improvement of glass interposer by changing the effective out-of-plane thermal conductivity of microbumps, TPVs, and bumps. Interconnect and TPV counts in Case 1 of Table 3.3 are considered for the fixed components. The variation of thermal conductivity ranged from that of glass (1 W/m·K) to

copper (400 W/m·K). The effect of interconnect/TPV on in-plane thermal conductivities is not considered because negligible variation in it is observed compared to out-of-plane thermal conductivity. A consistent dependence trend for all 3 components is demonstrated with a relatively large drop between 1 W/m·K and ~50 W/m·K. Increasing the thermal conductivity of interconnect/TPV layers beyond 100 W/m·K does not enhance the performance much. The thermal conductivity change in bump layer affects the thermal performance of the interposer the most, while microbump affects the least.

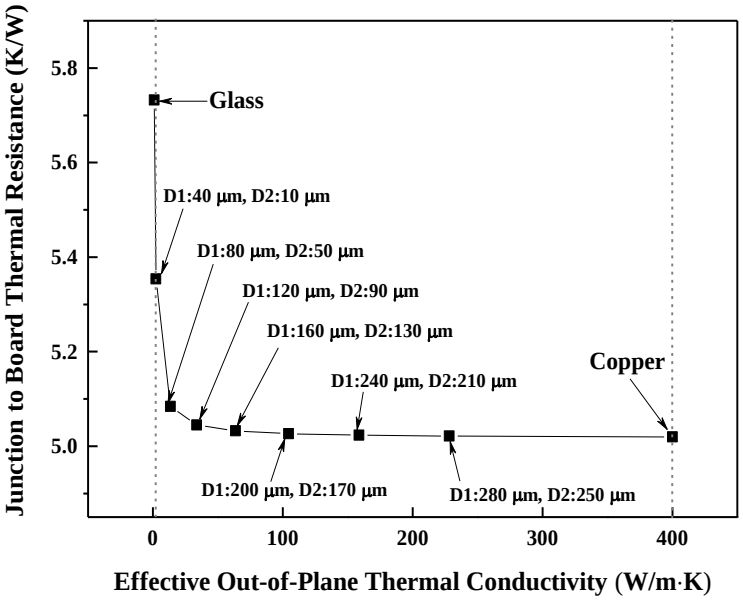


Figure 3.5 Junction to board thermal resistances of glass interposer with different D1 (laser entrance diameter) and D2 (laser exit diameter).

For interconnects, effective thermal conductivity in the range 50~100 W/m·K is hard to achieve, as solder has lower thermal conductivity (~50 W/m·K) than copper. However, TPV only consists of copper and thus can have wider range of effective thermal conductivity values, depending on the amount of copper used for filling vias. Figure 3.5 shows the change in Θ_{jb} for different TPV diameters at fixed pitch (300 μm) and height of

interposer (145 μm). As the diameters (D1 and D2) increases, the effective out-of-plane thermal conductivity of TPV layer also increases due to the increased copper volume fraction. This result indicates that increasing out-of-plane thermal conductivity to that of copper gives insignificant enhancement, when compared to the implementation of TPVs with diameters of 160 μm and 130 μm. This implies that the thermal resistance of other components becomes more dominant than that of interposer substrate after TPV implementation. The change in effective in-plane thermal conductivity of TPV is negligible (~1 W/m·K to ~3 W/m·K) when compared to the change in effective out-of-plane thermal conductivity (~1 W/m·K to ~220 W/m·K) during the analysis.

3.1.2 The effect of copper traces

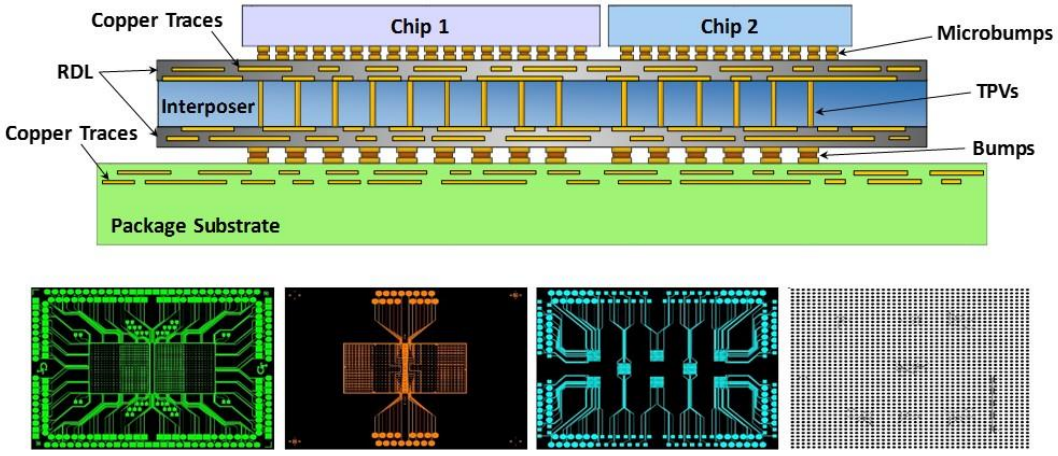


Figure 3.6 The schematic of 2.5D interposer (top) and layouts of four metal layers (bottom) used for simulation.

In addition to microbumps, TPVs, and bumps, copper traces are now incorporated in the interposer thermal model to investigate the effect of them. In this study, interposers are assumed to have four metal layers, two at the top and two at the bottom of the interposer

substrates as shown in Figure 3.6. The design of the metal layers is adopted from daisy chain layout used for electrical connectivity test.

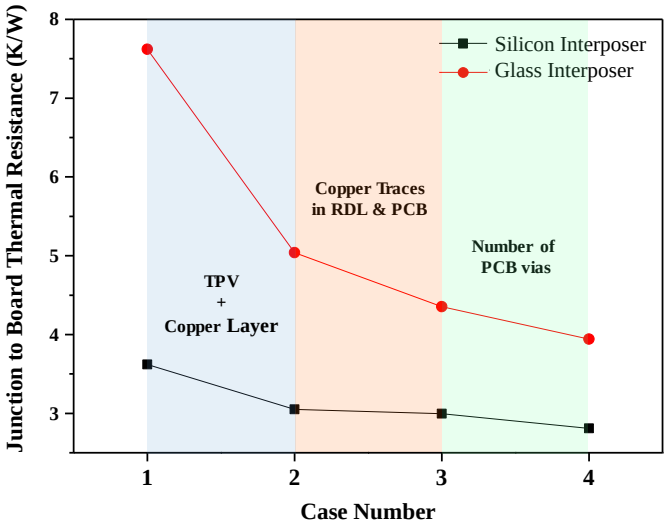


Figure 3.7 Junction to board thermal resistance of 4 different cases. The factors that affect the thermal resistance are indicated on the plot.

Figure 3.7 compares junction-to-board thermal resistance of glass and silicon interposers with different copper structure conditions at given boundary condition. Table 3.4 presents four different copper structure conditions applied when modeling TPV, RDL, and PCB. The thermal conductivities of RDL presented in case 3 and 4 are the averaged values of thermal conductivities from four different metal layers in RDL. Incorporation of copper TPVs and copper ground layer improves thermal performance of glass significantly, making its out-of-plane effective thermal conductivity ~34 times higher than that of bare glass. Due to high thermal conductivity of silicon, the effect of TPVs and copper ground layer is not as significant in silicon as compared to the glass interposer case. Increasing in-plane effective thermal conductivities of RDL and PCB, or out-of-plane effective thermal conductivity of PCB by increasing number of PCB vias does not increase the performance of both interposers much. It is observed that the copper structure implementation has a

significant effect on the thermal performance of glass interposer than that of silicon interposer.

Table 3.4 TPV, RDL, and PCB conditions for 4 different cases

	TPVs	RDL	PCB
Case 1	No TPVs	No copper k_{xy}, k_z =1 W/m·K	k_{xy}= ~14 W/m·K # of PCB vias: 180
Case 2	Table 3.1	No copper k_{xy}, k_z=1 W/m·K	k_{xy}= ~14 W/m·K # of PCB vias: 180
Case 3	Table 3.1	k_x=40 W/m·K k_y=50 W/m·K k_z=12 W/m·K	k_{xy}= 30 W/m·K # of PCB vias: 180
Case 4	Table 3.1	k_x=40 W/m·K k_y=50 W/m·K k_z=12 W/m·K	k_{xy}= 30 W/m·K # of PCB vias: 360

3.2 Effect of Vapor Chamber Integrated Packaging Substrate (PCB)

In this part of study, the application of an ultra-thin (~1 mm) vapor chamber to interposer structure is discussed and its effect on thermal performance is simulated. Figure 3.8 introduces the concept of vapor chamber integrated PCB for the interposer. A cavity formed in PCB is plated with copper and is covered with a copper lid, which is directly connected to PCBs. Heat generated from the chips flows through copper TPVs, and heats up the chamber's evaporator. The working fluid inside the chamber vaporizes at the evaporator, and limits temperature rise of the device. At the condenser, the vapor condenses back to liquid, which is attached to a large copper layer heat sink. A wick structure is used to provide the capillary action needed to drive the liquid against gravity. Thin layer of wick structure over evaporator area will potentially enhance liquid supply to the evaporator. Integration of the vapor chamber directly into the PCB has the following advantages:

1. Total packaging thickness can be reduced.

2. Vapor chamber can be integrated by utilizing standard PCB manufacturing process.

3. Upper space of the chip can be utilized for further thermal management.

4. Integration with PCB can reduce thermal interface resistance between heat source and cooling device more than external attachment at PCB bottom.

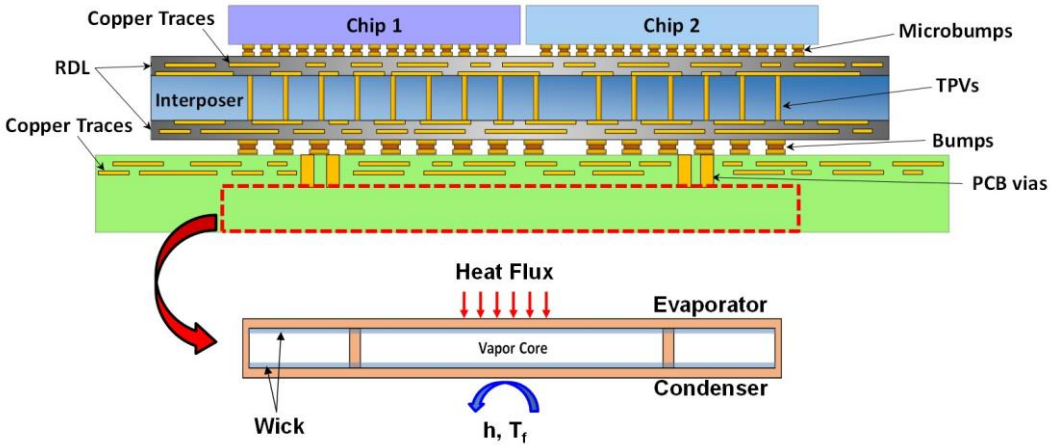


Figure 3.8 Interposer with vapor chamber integrated PCB.

To develop a simplified vapor chamber integrated interposer model, the entire vapor chamber is modeled as a block with an effective thermal conductivity by using the thermal resistance of a vapor chamber with a similar geometry and boundary conditions obtained from literature [26]. An analytical expression for spreading resistance of a 3D rectangular plate (30 mm × 30 mm × 1 mm) with single heat source (5 mm × 5 mm) shown in Figure 3.9 is utilized to extract effective thermal conductivity of a vapor chamber. To further simplify the model, the effective thermal conductivity of the vapor chamber structure is considered isotropic. The governing equation for the system shown in Figure 3.9 and its boundary conditions are:

$$\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}=0 \tag{10}$$

$$\left.\frac{\partial T}{\partial z}\right|_{z=0}=-\frac{Q/A_s}{k_{eff}} \quad \text{(within heat souce area: } A_s=cd\text{)} \tag{11}$$

$$\left.\frac{\partial T}{\partial z}\right|_{z=0}=0 \quad \text{(outside the heat source area)} \tag{12}$$

$$\left.\frac{\partial T}{\partial z}\right|_{z=t_1}=-\frac{h}{k_{eff}}[T(x,y,t_1)-T_f] \tag{13}$$

$$\left.\frac{\partial T}{\partial x}\right|_{x=0,a}=\left.\frac{\partial T}{\partial y}\right|_{y=0,b}=0 \tag{14}$$

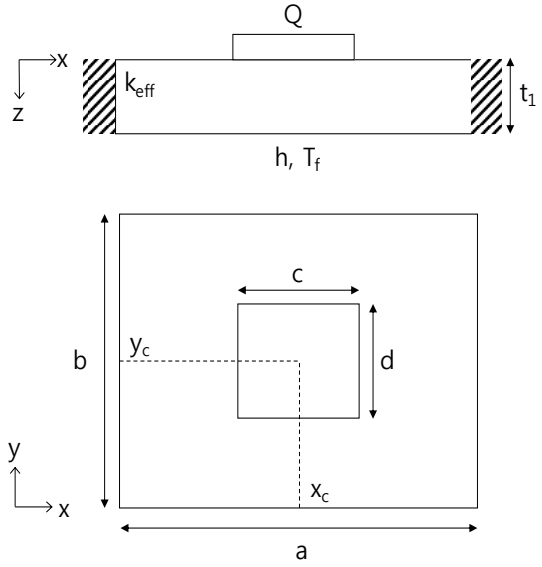


Figure 3.9 Isotropic plate with rectangular heat source on top and boundary conditions for analytical expression of thermal resistance.

The solution for the above differential equations can be obtained by using separation of variables. By integrating the solution, mean source temperature can be found as:

$$\begin{aligned}\bar{\theta} &= \bar{\theta}_{1D} + \bar{\theta}_S \\ &= \bar{\theta}_{1D} + 2\sum_{m=1}^{\infty} A_m \frac{\cos(\lambda_m X_c)\sin(\frac{1}{2}\lambda_m c)}{\lambda_m c} \\ &+2\sum_{m=1}^{\infty} A_n \frac{\cos(\delta_n Y_c)\sin(\frac{1}{2}\delta_n d)}{\delta_n d} \\ &+4\sum_{m=1}^{\infty}\sum_{n=1}^{\infty} A_{mn} \frac{\cos(\delta_n Y_c)\sin(\frac{1}{2}\delta_n d)\cos(\lambda_m X_c)\sin(\frac{1}{2}\lambda_m c)}{\lambda_m c \delta_n d}\end{aligned} \tag{15}$$

where $\lambda = m\pi / a,\ \delta = n\pi / b,\ \beta = \sqrt{\lambda^2 + \delta^2}$,

$$A_m = \frac{2Q[\sin(\frac{(2X_c + c)}{2}\lambda_m) - \sin(\frac{(2X_c - c)}{2}\lambda_m)]}{abck_{eff}\lambda_m^2 \phi(\lambda_m)} \tag{16}$$

$$A_n = \frac{2Q[\sin(\frac{(2Y_c + d)}{2}\delta_n) - \sin(\frac{(2Y_c - d)}{2}\delta_n)]}{abdk_{eff}\delta_n^2 \phi(\delta_n)} \tag{17}$$

$$A_{mn} = \frac{16Q\cos(\lambda_m X_c)\sin(\frac{1}{2}\lambda_m \mathrm{c})\cos(\delta_n \mathrm{Y}_c)\sin(\frac{1}{2}\delta_n \mathrm{d})}{abcdk_{eff}\beta_{m,n}\lambda_m \delta_n \phi(\beta_{m,n})} \tag{18}$$

$$\phi(\zeta) = \frac{\zeta\sinh(\zeta t_1) + {h}/{k_{eff}}\cosh(\zeta t_1)}{\zeta\cosh(\zeta t_1) + {h}/{k_{eff}}\sinh(\zeta t_1)} \tag{19}$$

where $\zeta = \lambda, \delta, or\ \beta$, and

$$\bar{\theta}_{1D} = \frac{Q}{ab}(\frac{t_1}{k_{eff}} + \frac{1}{h}) \tag{20}$$

Finally, total thermal resistance of vapor chamber can be expressed as

$$R_{VC} = \frac{\bar{\theta}}{Q} = \frac{\bar{\theta}_{1D} + \bar{\theta}_S}{Q} = R_{1D} + R_S \tag{21}$$

which can be expressed as a function of k_{eff}. By equating Equation (21) with the vapor chamber thermal resistance listed in the literature [26], equivalent thermal conductivity k_{eff} was calculated. To find a solution, the Levenberg-Marquardt (LM) method, a damped least square minimization technique was used. After calculating the effective thermal conductivity, it was then used for developing finite element (FE) model of a simplified vapor chamber. After FE simulation, thermal resistance was calculated and the result was compared with the original thermal resistance value from the literature for validation, and two thermal resistance values showed ~2% difference. Upon validation, this effective thermal conductivity was then applied to the simplified block in PCB and used for performance estimation. Figure 3.10 summarizes the steps taken for simulation of interposer with vapor chamber embedded PCB.

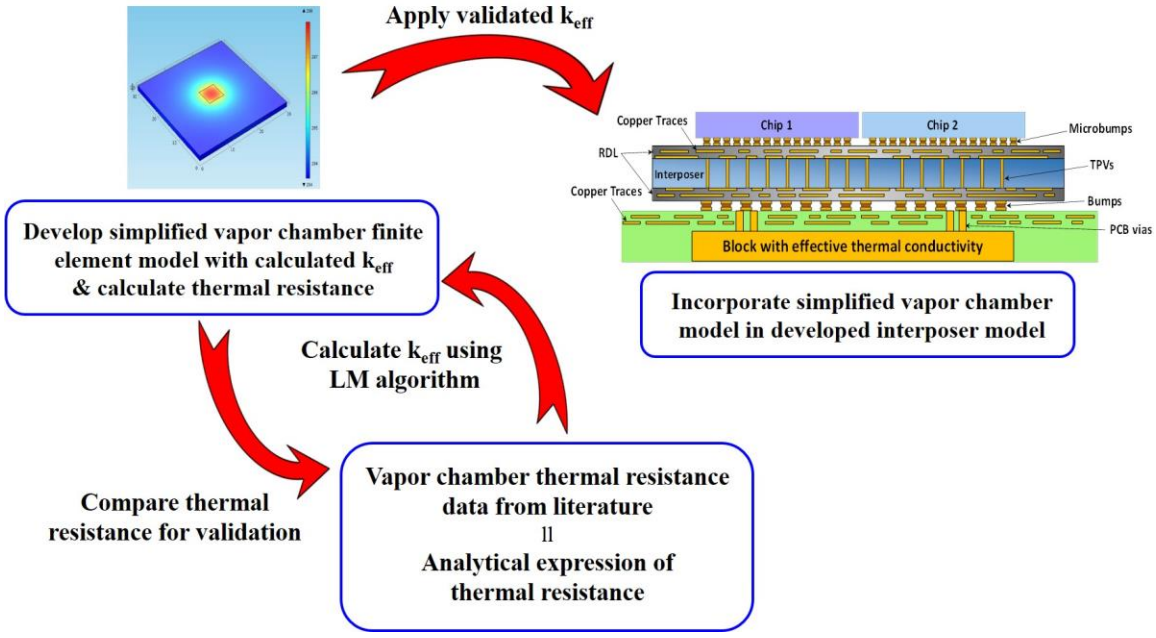


Figure 3.10 Thermal performance simulation steps for interposer with vapor chamber integrated PCB.

Table 3.5 Calculated effective thermal conductivity based on thermal resistance.

	Thermal resistance (K/W)	Effective thermal conductivity (W/m·K)
1D resistance analysis	0.27	1526
Numerical model	0.51	491

Two thermal resistance values in the literature [26], calculated from one-dimensional (1D) resistance network analysis and numerical model, were used to calculate effective thermal conductivity of vapor chamber. The result is shown in Table 3.5. Thermal resistance value obtained from the numerical model was used for effective thermal conductivity calculation, as the result from 1D resistance network analysis does not capture the vapor core resistance and underestimates the total resistance value.

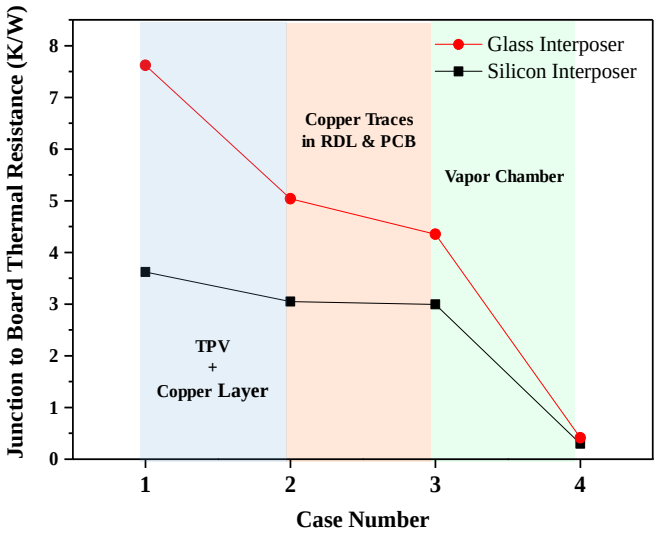


Figure 3.11 Junction to board thermal resistance of 4 different cases. The factors that affect the change of thermal resistance are indicated on the plot

Figure 3.11 shows the effect of vapor chamber and copper structures studied in this paper by including the thermal structures sequentially and comparing the thermal performance of glass interposer to that of silicon interposer for each of these cases.

Different TPV, RDL, and PCB conditions used for case 1, 2, and 3 can be found in Table 3.4. The previous result for case 4 in Figure 3.7 is now replaced with the result from vapor chamber integrated interposer and shown in Figure 3.11. After the implementation of vapor chamber in both interposers, thermal resistance of glass interposer for case 4 is almost identical to silicon interposer, while the difference between the two interposers is significant for case 1. The vapor chamber in PCB, which provides better heat spreading effect than thin copper ground layer in PCB, offers significant thermal performance enhancement to glass interposer with thermal paths made by copper structures.

CHAPTER 4. VAPOR CHAMBER EMBEDDED PACKAGING SUBSTRATE

This chapter presents detailed fabrication process of the package substrate integrated with vapor chamber. Each section describes the challenges faced during the process and explains how they are resolved.

4.1 Prior Art

There have been a few research efforts to integrate two-phase cooling technology with packaging substrate, as shown in Table 4.1. Benson et al. [27] integrated micro-heat pipes with silicon multichip module (MCM) substrate (4.8 cm × 4.8 cm × 1.3 mm). The wick structure is patterned using deep anisotropic plasma etch, and the substrate is hermetically sealed using wafer bonding. The developed substrate was reported to have five times lower thermal resistance compared to unfilled substrate. Jones et al. [28] proposed an embedded micro heat pipe (5.3 cm × 0.6 cm × 5 mm) in PCB (7.5 cm × 2.9 cm × 6 mm). The microgrooves were patterned in PCB by stacking the polymeric layers of the PCB in a staggered lay-up, and used as wick structure. The PCB showed a thermal resistance decrease by 40%, compared to uncharged device. However, the device failed at around 10 W due to the delamination of the PCB layer. Wits et al. [29] proposed another way of integrating micro heat pipe (17 cm × 2 cm × 2 mm) into PCB (~19 cm × ~4 cm × 4 mm). Instead of having microgroove wick by stacking up PCB layers, the groves were placed on the top and bottom layer of internal PCB cavity patterned by using lithography and plating technique. The device was able to transport a maximum of 12 W of heat without

failure under vertical orientation. More recently, Fan et al. [30] integrated a planar thermosyphon into a PCB for cooling LED devices. The device (PCB surface area: 270 mm^2, total thickness: 1.7 mm) uses a dielectric fluid as the working fluid, and their model predicted that it can reduce the thermal resistance of conventional PCB by more than 50%. The study [30], however, did not report the performance of the device, but only presented the boiling heat transfer performance of different wick samples designed for the device.

Table 4.1 Summary of prior researches on integration of two-phase cooling technology

	Device Size	Substrate	Working Fluid	Wick
Benson et al. (1997)	4.8 cm × 4.8 cm × 1.3 mm	Silicon	Alcohol	Etched silicon channel
Jones et al. (2002)	7.5 cm × 2.9 cm × 6 mm	PCB	DI water	Microgrooves (Polymer layer)
Wits and Vaneker (2010)	~19 cm × ~4 cm × 4 mm	PCB	Water	Microgrooves (Polymer layer)
Fan et al. (2012)	270 mm^2 × 1.7 mm	PCB	Dielectric Fluid	Copper Micropillar

4.2 Integration of Vapor Chamber with PCB

This research focuses on integrating vapor chamber with PCB (4 cm × 4 cm), and targets total thickness of the substrate less than 1 mm. Due to its high Merit number at operating temperature range (293 K~ 373 K), and its compatibility with copper, water is chosen for working fluid. Figure 4.1 shows the schematic cross-sectional view of the prototype and summarizes the fabrication subtasks for its successful demonstration. The challenges associated with integration of two-phase cooling device and PCB are as follows.

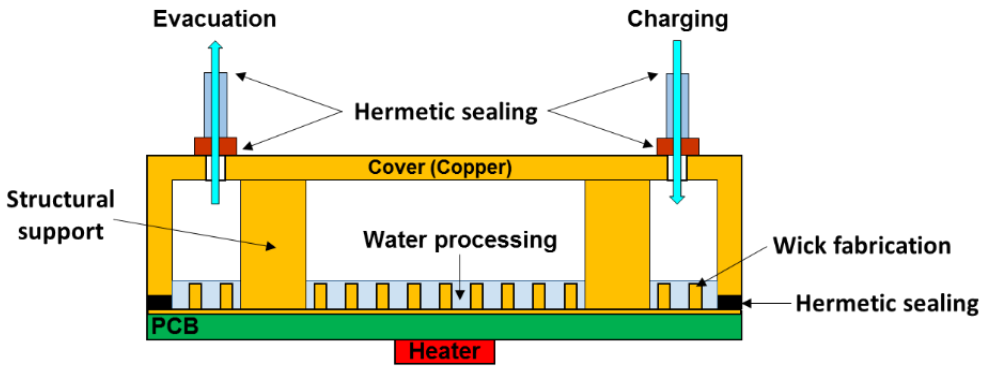


Figure 4.1 Schematic cross-sectional view of vapor chamber integrated PCB and subtasks for fabrication of prototype

1. Wick structure fabrication on PCB: Wick structure needs to be fabricated on PCB to deliver working fluid to heated area. The thermal performance of wick structure targets dissipating heat flux higher than 100 W/cm^2.

2. Hermetic sealing of device: Device should be hermetically sealed to prevent working fluid from leakage. The hermetic sealing is needed at the gaps between edges of PCB (evaporator) and edges of copper cover (condenser), charging/evacuation tubes and copper cover (or PCB). The end of charging/evacuation tubes should be also sealed after charging/evacuation process.

3. Water processing: The working fluid (water) should be highly pure [31], and needs to be processed through distillation prior to charging.

4. Device evacuation and charging: Prior to charging vapor chamber with working fluid, device needs to be vacuumed to remove any non-condensable gases (NCGs) from vapor space. As the volume of charged working fluid affects the performance of vapor chamber, capability to charge the device with accurate amount of working fluid is essential.

The rest of this chapter explains the fabrication process of vapor chamber integrated PCB.

4.3 Micropillar Wick Structure

Heat pipes and vapor chambers are widely used in the thermal management of electronic devices due to their effective and reliable performance. These devices enclose a porous media, also known as wick structure, which transports the working fluid from the condenser to evaporator section by capillary pumping action. Wick structures of conventional heat pipes incorporate simple linear channels, meshes or grooves. However, as the sizes of electronic components become smaller with higher heat fluxes, the design of heat pipes with such wick structure becomes challenging due to its limited capillary transport capability. This limitation occurs when the capillary pressure generated by the wick structure is insufficient to overcome the pressure drop in the wick, which leads to dryout in the evaporator section.

Sintered metal powders are known to provide superior wicking capability, as well as the highest rate of thin-film evaporation compared to other wick microstructures [32]. A number of researchers have characterized the performance of sintered metal wicks [33],[34],[35],[36] and achieved maximum heat flux higher than 500 W/cm^2. While sintered metal particle wick structures have shown excellent capillary performance, metal sintering process requires high temperature (> 900 °C) and pressure condition, which is not compatible with organic substrate such as PCB. Moreover, they have lower effective thermal conductivity compared to conventional wicks and micropillar type wicks due to the small contact areas between spherical powders and heating surfaces, and low permeability caused by small pore size [37]. One of the alternative low-temperature fabrication approaches is growing pillar type wick structures through electrochemical deposition process.

Micropillar array wicks have been proposed to improve the performance limits of conventional wicks. The major advantages of these over other types of wicks are their higher permeability compared to other monoporous wicks, and higher effective thermal conductivity. Recently, several studies have focused on the development and characterization of micropillar wicks for their application in electronics cooling. Ranjan et al. [37] developed numerical models of different micropillar geometries to compare their capillary pressure, permeability, and thin-film evaporation rates. The study found that pyramidal pillars showed better performance than other pillar shapes, and concluded that micropillar wicks can be a viable solution for thin vapor chambers, where large liquid pressure drop at high heat fluxes is of significant concern. Nam et al. [38] fabricated superhydrophilic copper micropillar arrays and measured the capillary performance of arrays with different diameter and pitch conditions. The authors measured the heat transfer performance of nanostructured copper post wicks [39] and reported that the critical heat flux was enhanced by over 70% after nanostructure integration. Ćoso et al. [40] investigated heat transfer characteristics of biporous wicks, which consisted of micro pin fin arrays separated by microchannels. The test result with small heaters showed that the wick structure was capable of dissipating heat flux up to ~733 W/cm^2. Hale et al. [41],[42] performed modeling to optimize the capillary flow through micropillars with square and rectangular arrangements. Ravi et al. [43],[44] measured the capillary pressure and permeability of silicon micro pillars by using dryout threshold data of wick samples with different lengths.

Significant insights have been achieved through the prior studies on micropillars for wick structures. However, only few experimental reports on two important

characteristics of copper micropillars, capillary pressure and permeability, are currently available [38]. Moreover, most literature has considered one type of pillar arrangement, and the effect of the pillar arrangements on the hydraulic performance has been scarcely investigated [42],[45].

In this part of dissertation, capillary pressure and permeability of copper micropillar arrays in hexagonal, square, and rectangular arrangements are investigated for vapor chamber application. To enhance their wettability, the wick structures are coated with SiO_2 nanoparticles using layer-by-layer deposition technique [46]. The diameter and height of pillars are fixed at 50 μm, while the distance between pillars is varied to achieve porosities ranging from 0.45 to 0.8. The wick samples are fabricated on printed circuit boards (PCB) using electrolytic plating process. The capillary rate-of-rise test and forced liquid flow test are carried out to characterize the wick performance. The test results are compared with finite volume modeling, which adopts the shape of the liquid meniscus within the arrays. The capillary performance parameter of the micropillar arrays in different arrangements are also measured and compared with the model predictions.

4.3.1 Hydraulic Performance Test of Micropillar Wick Structure

4.3.1.1 Sample preparation

Prior to the tests, copper pillar arrays are fabricated on copper clad PCB substrate. The pillar arrays cover a 1 cm x 5 cm area of the PCB, and the pillars are arranged in hexagonal, square, and rectangular patterns. For each arrangement, 4 samples with different porosities (0.45, 0.6, 0.7, and 0.8) are fabricated. Micropillars have 50 μm diameter and height. A ruler mark is patterned right next to the pillar patterned area to

measure the height of water rise during the rate-of-rise test. Figure 4.2 summarizes the process flow of sample fabrication.

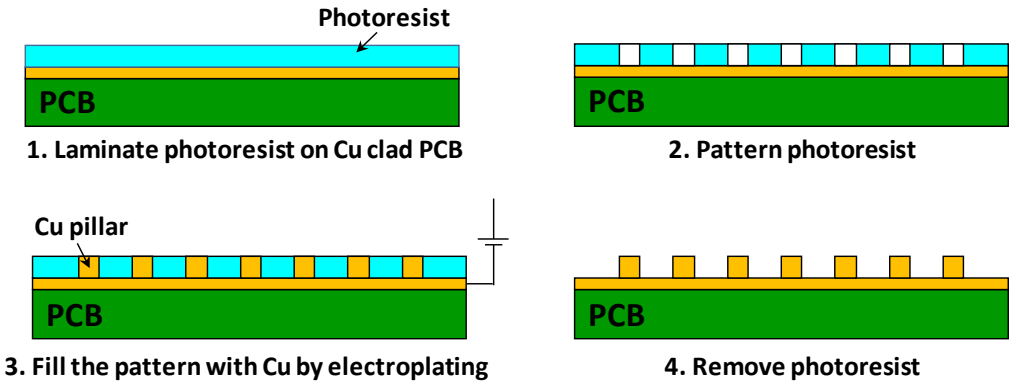
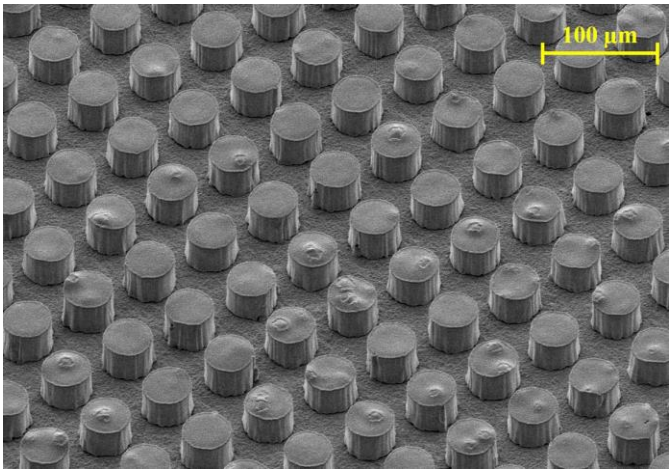


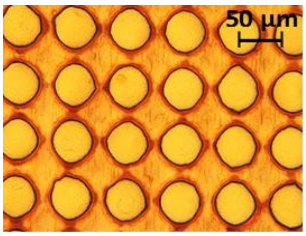
Figure 4.2 Process flow for fabricating micropillars on copper clad PCB.

First, copper clad PCB is laminated twice with 25 µm-thick dry film negative photoresist (Hitachi RY-5125) using roller laminator at 100 °C. The photoresist layer is then exposed to UV illumination (TAMARACK 152R) for 10.3 seconds with circular pillar shape patterned mask. The photoresist layer is developed to expose the copper surface, where the copper pillars pattern will be plated. O_2/CF_4 plasma is used (10 minutes) to remove any photoresist residues left in the pillar pattern holes. After the photoresist residue removal, the sample is put in dilute sulfuric acid bath to remove the oxide layer (1 minute) and enhance the wettability of the exposed copper surface. The sample is then placed in a copper plating bath (~4 hours) equipped with plating solution and copper source. The current density for the plating is fixed throughout the process, and the plating thickness is checked with a 3D optical profiler (Zeta Instruments) every two hours. After the pattern holes are filled with pillars, the photoresist is stripped (Dupont™ EKC162™) at ~ 55 °C in a sonicator (Quantrex®). To enhance wettability and protect copper from oxidation, the sample is plated with 50 nm-thick gold using electroless nickel immersion gold (ENIG)

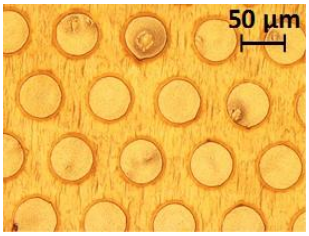
process. More details on the ENIG process is discussed later. Figure 4.3 (a) shows the scanning electron microscope (SEM) image of fabricated micropillar arrays after ENIG process is finished, and Figure 4.3 (b), (c), and (d) show the images of micropillar arrays in different arrangements taken from the optical profiler.



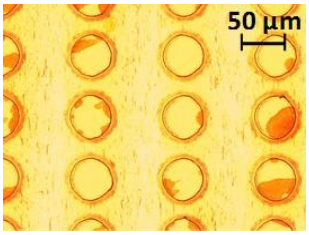
(a)



(b)



(c)



(d)

Figure 4.3 (a) SEM image of fabricated micropillar arrays in square arrangement. 3D optical profiler image of fabricated micropillar arrays in (b) square arrangement, (c) hexagonal arrangement, and (d) rectangular arrangement.

To enhance the wettability of wicks, thin layers of silica nanoparticles are deposited on the micropillar sample substrates via layer-by-layer deposition of oppositely charged SiO_2 nanoparticles. The advantage of the approach is in the simple deposition process, and its good control over the growth of the nanoparticle layer. Two solution baths with 3-

Aminopropyl-functionalized silica nanoparticles (AP-SiO_2, 3% (w/v)) for positively charged silica solution, and Ludox TM-40 (40 wt% SiO_2 suspension in water, Sigma-Aldrich) for negatively charged silica solution are prepared for the silica multilayer assembly process. The pH of each nanoparticle suspension bath is controlled with deionized (DI) water and HCl or NaOH, and maintained at 4.5 throughout the deposition process to achieve maximum growth of the nanoparticles. A multi-layer of thin films of silica nanoparticles is created by dipping the sample in each of the nanoparticle solution for 10 minutes, followed by DI water rinsing for 5 minutes. The total thickness of the coated bilayer on the sample is estimated to be ~ 90 nm based on the characterization study shown in [46].

4.3.1.2 Setup for capillary rate of rise experiment

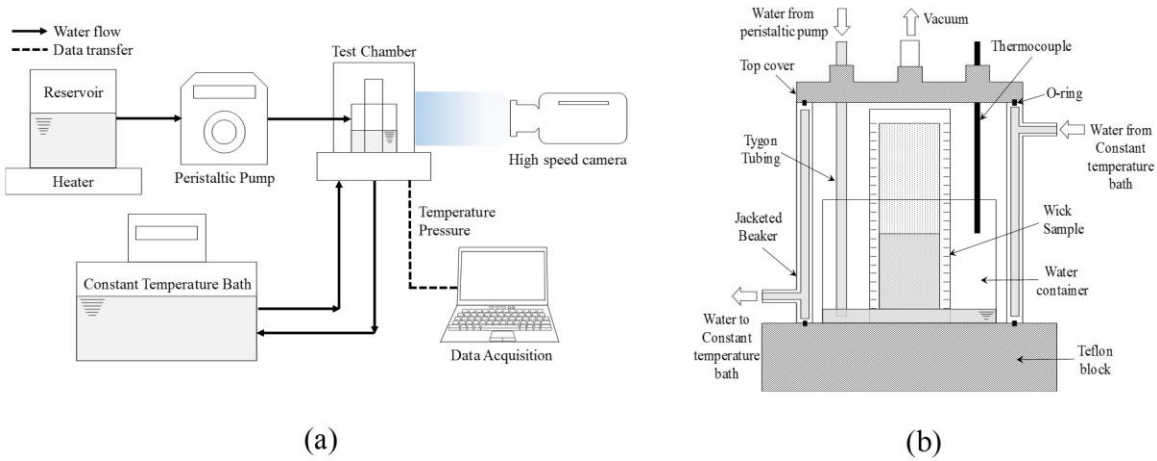


Figure 4.4 Schematic of capillary rate-of-rise test setup (a) test system and (b) detail view of test chamber.

As shown in Figure 4.4, the capillary rate-of-rise test is performed to characterize the capillary performance of the fabricated wicks. The rate-of-rise wick test with sintered powder wicks can lead to unreliable results due to its difficulty in locating the liquid front

in the wick [47]. However, the liquid front within pillar type wick structures can be easily detected, and the spontaneous rise of the liquid can be captured by high speed camera.

Prior to running the test, the wick sample is attached to a fixture and placed in the empty water container in the test chamber, as shown in Figure 4.4 (b). The test chamber has two water supply connections. The first water line is connected to a peristaltic pump, which supplies DI water from the reservoir to the water container in the test chamber. The DI water in the reservoir is heated during the test to maintain constant temperature. The second water line is connected to a constant temperature bath, which supplies water to the water jacket around the chamber to maintain constant temperature condition (±0.5 °C) during the test. After the wick is placed in the container with a fixture, the test chamber is covered with a top cover, and sealed with o-ring by mechanically fastening the cover and chamber with a clamp. After sealing, the chamber is vacuumed to simulate a heat pipe environment, and water is supplied from the constant temperature bath. Temperature and pressure inside the chamber are monitored by using a pressure transducer with ±0.25% uncertainty and T-type thermocouple with ±0.5 °C uncertainty. Water is supplied to the inner container through Tygon® tubing by turning on the peristaltic pump when the pressure and temperature reach steady state. The chamber pressure is maintained at 0.3 bar, and the temperature of water is maintained at 60 °C throughout the tests. Water delivery to the container is stopped when the water meniscus reaches the bottom of the wick, and capillary rise starts. Liquid front height during the capillary rate-of-rise process is captured by a high-speed camera (Phantom V211, Vision Research) at a frame rate of 100 frames/s.

4.3.1.3 Setup for permeability experiment

The permeability of the samples is determined using the forced liquid flow method. Figure 4.5 (a) shows the schematic of the permeability test setup. The reservoir is filled with DI water, and the flow rate of water is controlled by a gear pump (Micropump (GJ-N21), Max flow rate: 1740 mL/min). Pumped water passes through a 7 µm filter to prevent small particles from going into the wick sample under test.

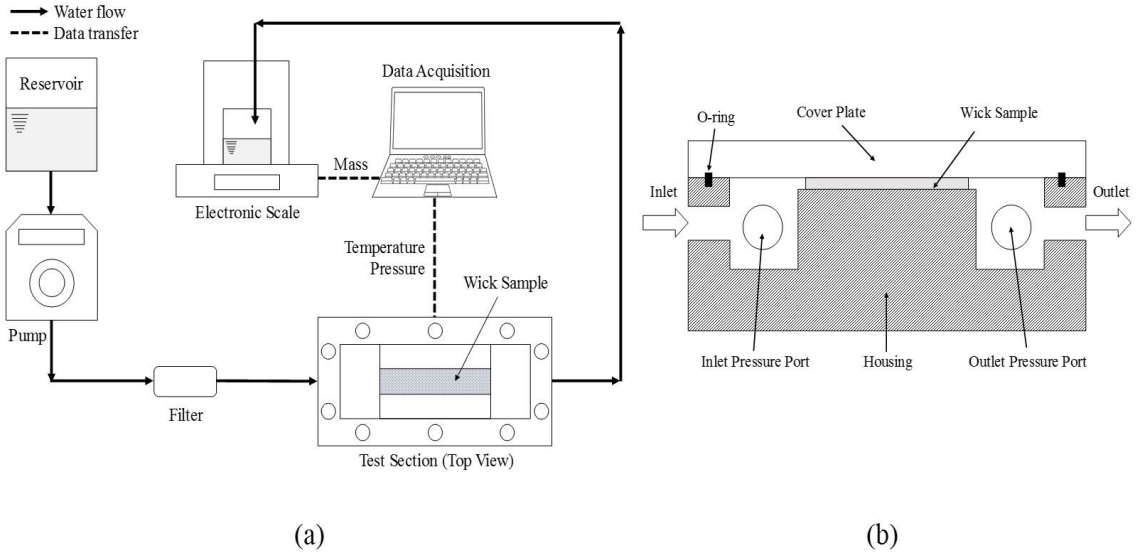


Figure 4.5 Schematic of permeability measurement (a) test setup and (b) cross-sectional view of test section.

As shown in Figure 4.5 (b), the test section consists of a transparent polycarbonate cover plate, wick sample, and a flow housing with two pressure ports. A rectangular channel of 1 cm x 5 cm is cut in the flow housing to place the wick sample. Room-Temperature-Vulcanization (RTV) silicone rubber is placed between wick sample and the housing to prevent any bypass flow. The cover plate and housing are fastened with bolts, and o-ring placed between the two provides a tight sealing. Two pressure transducers (Omega, 0-6.9 bar) are connected to the two pressure ports at housing to measure pressure difference between the inlet and outlet. All tests are performed at three different inlet

pressure conditions, 4, 5, and 6 bar by controlling the flow rate. After the test section, water is collected in a container, and placed on an electronic scale with a resolution of 0.001 g. The scale transfers real-time mass change of the container to a computer through RS232 interface. Measured mass change data is collected for at least 60 seconds, and it is used to calculate mass flow rate for each test case. Water temperature at inlet and outlet of the test section is measured using T-type thermocouples probes with 813 μm diameter to determine the viscosity and density of water. Prior to each test, the sample is blown with pure nitrogen to remove any particulates.

4.3.1.4 Capillary pressure modeling

The capillary pressure difference generated by the micropillar wick structures is dependent on the mean curvature of the liquid meniscus (H) formed between pillars, and can be expressed by the Young-Laplace equation:

$$\Delta P_{cap} = \sigma(\frac{1}{r_1} + \frac{1}{r_2}) = 2H\sigma \tag{22}$$

where ΔP_{cap} is capillary pressure rise across fluid interface, r_1, r_2 are principal radii of curvature at a point on the meniscus, and σ is the surface tension of the liquid. The mean curvature of liquid meniscus in pores with different porosity can be predicted by Surface Evolver (SE) [48], using surface energy minimization, with liquid volume and contact angle as prescribed constraints. Capillary pressure can be calculated using Equation (22) with predicted liquid meniscus curvature from SE. During the analysis, height and diameter of the pillars are fixed at 50 μm, and the liquid level in the pores is assumed to be equal to the height of the pillars.

4.3.1.5 Permeability modeling

The permeability of porous structures with periodic arrays of cylinders has been extensively studied. Sangani and Acrivos [49] performed analytical and numerical studies on the permeability of square and staggered arrays of cylinders. Drummond and Tahir [50] developed analytical solutions for the Stokes flow past parallel and transverse cylinder arrays, which are applicable at low solid volume fraction. Gerbart [51] developed an expression of the permeability of cylindrical fiber arrays for flow along, and perpendicular to the fibers. Tamayol and Bahrami [52] developed an analytical expression for pressure drop and permeability of cylinder wicks assuming a parabolic velocity profile within the unit cells of the wick structure. Yazdchi et al. [53] proposed an expression for the permeability of periodic porous media, valid for the whole range of porosity by combining expressions from Drummond and Tahir, and Gerbart. Xiao et al. [54] solved Brinkman's equation for a square micropillar array, and the solution can be utilized to get an analytical expression for dimensionless permeability. While most of the previous numerical and analytical studies on permeability of microstructures have been with the assumption of flat liquid/air interface, Nam et al. [38] pointed out that this assumption may overestimate the permeability significantly. Byon and Kim [55] investigated the effect of meniscus curvature on the permeability of micro-post arrays and showed that the effect of meniscus shape is more pronounced as the contact angle, or micropost height decreases. Table 4.2 summarizes various existing permeability models.

Table 4.2 Summary of correlation between dimensionless permeability (K*) and porosity (ε).

Model	Dimensionless permeability K* (K/d^2, d: pillar diameter)
Gebart [51] (K^*_G, 1992)	$C\left(\sqrt{\frac{1-\varepsilon_c}{1-\varepsilon}}-1\right)^{5/2}$ $\left\{\begin{array}{l} C=\frac{4}{9\pi\sqrt{2}} \quad \varepsilon_c=1-\pi/4 \quad \text{for square arrang: } K^s_G/d^2 \\ C=\frac{4}{9\pi\sqrt{6}} \quad \varepsilon_c=1-\pi/\left(2\sqrt{3}\right) \quad \text{for hexagonal arrang: } K^h_G/d^2 \end{array}\right\}$ (23)
Drummond and Tahir [50] (K^*_D,1984)	$\frac{1}{32(1-\varepsilon)}\left(\ln\left(\frac{1}{1-\varepsilon}\right)-1.476+\frac{2(1-\varepsilon)-0.796(1-\varepsilon)^2}{1+0.489(1-\varepsilon)-1.605(1-\varepsilon)^2}\right)$ for square arrang: K^s_D/d^2 $\frac{1}{32(1-\varepsilon)}\left(\ln\left(\frac{1}{1-\varepsilon}\right)-1.497+2(1-\varepsilon)-\frac{(1-\varepsilon)^2}{2}-0.739(1-\varepsilon)^4+\frac{2.534(1-\varepsilon)^5}{1+1.2758(1-\varepsilon)}\right)$ for hexagonal arrang: K^h_D/d^2 (24)
Tamayol and Bahrami [52] (K^*_T, 2009)	$\left\{\frac{12(\sqrt{\phi}-1}{\phi\sqrt{\phi}}\left[\frac{2-g(\varepsilon)}{2}\right]+\frac{18+12(\phi-1)}{\sqrt{\phi}(1-\phi)^2}+\frac{18\sqrt{\phi}\left[\tan^{-1}\left(\frac{1}{\sqrt{\phi-1}}\right)+\frac{\pi}{2}\right]}{(\phi-1)^{5/2}}\right\}^{-1}$ where $\phi=\frac{\pi}{4(1-\varepsilon)}$, $g(\varepsilon)=1.274\varepsilon-0.274$ (25)
Yazdchi et al. [53] (K^*_Y, 2011)	From Drummund and Tahir (1984) $\frac{K^s_{G2}+(K^s_D-K^s_{G2})m(\varepsilon)}{d^2}$ where $K^s_{G2}=\frac{K^s_G}{1+0.336(\varepsilon-\varepsilon_c)}$, $m(\varepsilon)=\frac{1+\tanh(\frac{\varepsilon-0.75}{0.037})}{2}$ for square arrang $\frac{K^h_G+(K^h_{D2}-K^h_G)m(\varepsilon)}{d^2}$ where $K^h_{D2}=0.942K^h_D(1+0.153\varepsilon)$, $m(\varepsilon)=\frac{1+\tanh(\frac{\varepsilon-0.55}{0.037})}{2}$ for hexagonal arrang (26)
Xiao et al. [54] (K^*_X, 2010)	$K^*=K^*_{cyl}-K^{*\,1.5}_{cyl}\frac{d}{h\sqrt{\varepsilon}}\tanh\left(\frac{h\sqrt{\varepsilon}}{d\sqrt{K^*_{cyl}}}\right)$ where *h*: pillar height, d: diameter, and ε: porosity (27)

In this study, a numerical simulation is performed to predict the permeability of micropost array in square, rectangular and hexagonal arrangements, and the results are compared with experiments. With an optical profiler, it is observed that fabricated wick samples have uneven pillar heights caused by non-uniform current distribution over the sample during electrochemical deposition process. Due to the irregular height of the pillars, gaps may exist between top surface of the relatively shorter pillars and the polycarbonate cover when the sample is placed in the test section, as shown in Figure 4.6 (a). Utilizing the maximum and minimum measured pillar heights, numerical models of two limiting cases (Figure 4.6 (b) and (c)) for each sample are developed using a commercial

computational fluid dynamics (CFD) software FLUENT®. Figure 4.7 (a) shows the computational domain of post array for the numerical model, and (b) summarizes the boundary conditions of the domain: No-slip boundary condition is applied on the fluid-solid interfaces. Periodic boundary conditions of flow rate acquired from the test are applied on inlet and outlet of the domain, and symmetry condition is applied on remaining surfaces.

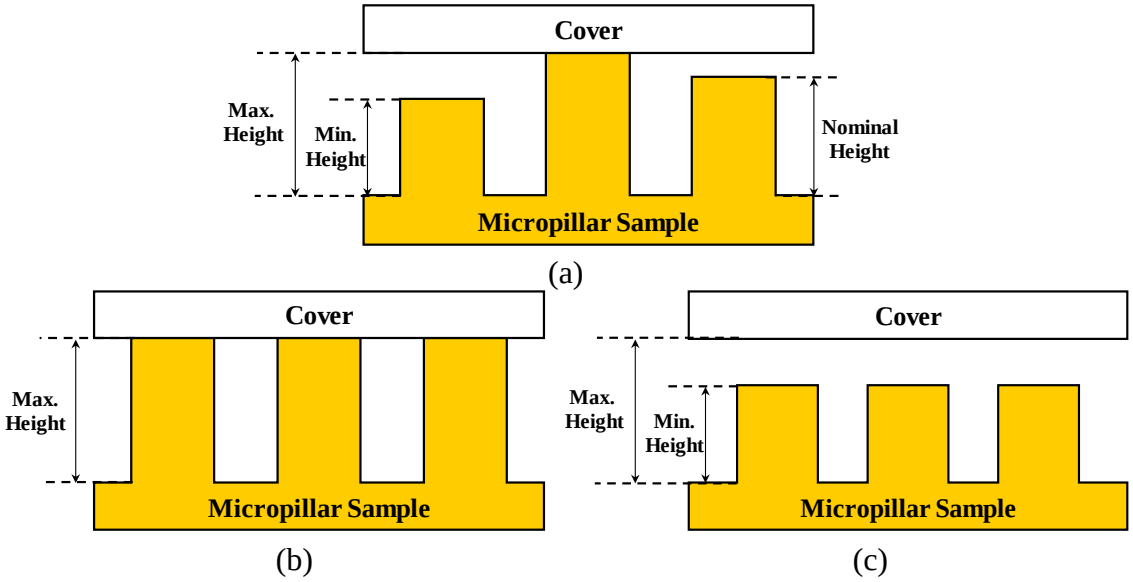


Figure 4.6 The schematic of wick samples with (a) non-uniform pillar height, (b) maximum measured height, and (c) minimum measured height under polycarbonate cover during permeability test.

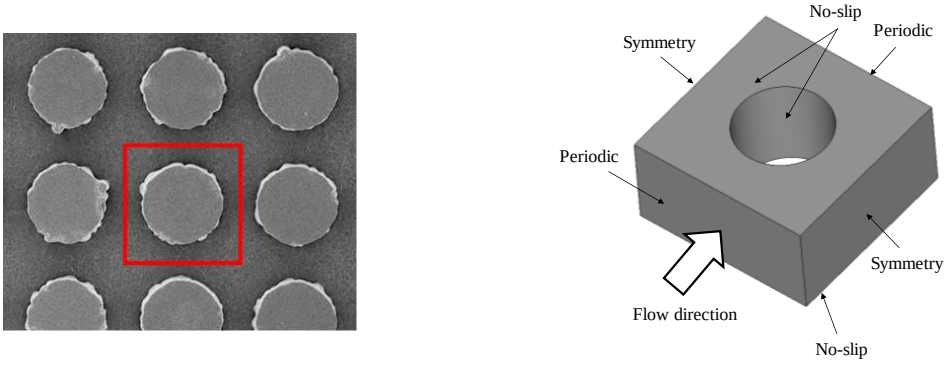
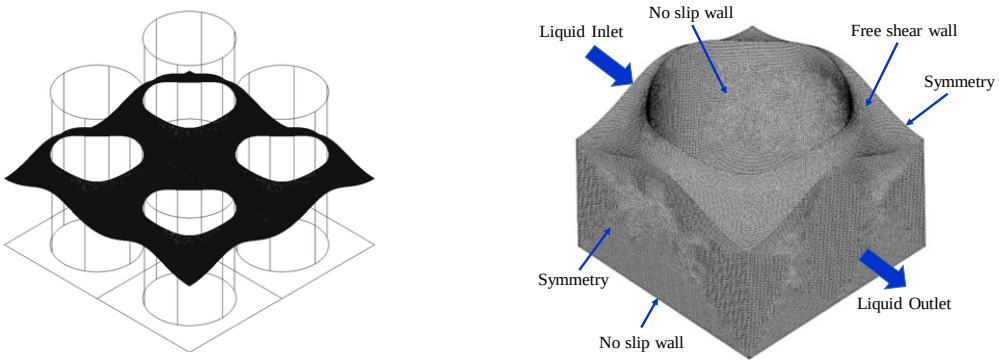


Figure 4.7 (a) SEM image of pillar array (top view) and computation domain (red box) used for numerical model. (b) Boundary conditions for computation domain.

To estimate permeability of wick samples more accurately when the top surface of the sample is exposed to air, SE is used to predict water meniscus shape within micropillar array in each arrangement [38],[55]. To generate the computational domain with water meniscus curvature, the unit cell of meniscus shape from SE is imported to a FLUENT® to solve the fluid flow within the cell. For permeability computation, fluid flow with Re=0.1 (Re = $\rho uL/\mu$ where ρ is density (1000 kg/m^3), u is velocity (10^{-4} m/s), L is characteristic length (1 mm as wick length scale), and μ is dynamic viscosity (10^{-3} Ns/m^2)) is modeled considering typical fluid velocity profile in the micro wick structure [37].



(a) (b)

Figure 4.8 (a) Liquid meniscus shape within micropillar array and (b) unit cell and boundary conditions used to estimate permeability of micropillar structure in square arrangement.

Figure 4.8 (a) shows liquid meniscus shape of micropillar in square arrangement obtained from SE, and (b) displays the exported meniscus geometry and boundary conditions used for the permeability prediction. A periodic condition is applied to inlet and outlet boundary of the unit cell. No-slip condition is applied at the interfaces between

pillar/bottom wall and liquid, while a free shear condition is used at the top boundary as the flow interference caused by air is assumed negligible. Symmetry conditions are used at transverse boundaries. The width and length of the unit cell are varied, along with the change of porosity, while the height of the domain is kept as the same for each pillar arrangement case. Finally, the permeability (K) was determined by the Darcy's law,

$$K = \frac{\dot{m}\mu L}{\rho A \Delta P} \tag{28}$$

where $\dot{m}$ is the liquid mass flow rate, μ is the viscosity of water, L is the length of the unit cell, ρ is the density of water, A is the cross-sectional area of the wick, and ΔP is the pressure drop.

4.3.1.6 Data analysis

The capillary pressure is taken from an axis-symmetric form of the Laplace-Young equation:

$$\Delta P_{cap} = \frac{2\sigma \cos\theta}{r_p} \tag{29}$$

where σ is the surface tension of liquid, r_p is the pore radius and θ is contact angle between liquid and solid. Equation (29) can be expressed in more simplified form by adopting effective capillary radius (r_{eff}), which yields:

$$\Delta P_{cap} = \frac{2\sigma}{r_{eff}} \tag{30}$$

During the capillary rise, the capillary pressure should be balanced with the pressure loss due to friction and hydrostatic pressure [47]:

$$\frac{2\sigma}{r_{eff}} = \frac{\mu\varepsilon}{K} x \frac{dx}{dt} + \rho g x \tag{31}$$

where ε is the porosity of wick structure, x is the liquid rise height, $\frac{dx}{dt}$ is the velocity of liquid rise, and g is the gravitational acceleration. Equation (31) can be integrated from the initial height and time when the capillary rise starts to the observed liquid rise height and time. Then Equation (31) can be expressed as:

$$x^2 - x_0{}^2 = \frac{2K}{\varepsilon\mu}\left[\frac{2\sigma}{r_{eff}}(t - t_0) - \rho g \int_{t_0}^{t} x d\tau\right] \tag{32}$$

where x_0 is initial liquid front height, t is the time when the liquid rise x is observed, and t_0 is the initial time, or time when liquid front is at x_0. Equation (32) can be expressed in a closed form, with the assumption that only displacement changes with time. If x_0 and t_0 are 0,:

$$t = \frac{-\varepsilon\mu}{K\rho^2 g^2}\left[\frac{2\sigma}{r_{eff}} \ln(1 - \frac{\rho g r_{eff}}{2\sigma} x) + \rho g x\right] \tag{33}$$

Using liquid front height data at different time acquired from capillary rate-of-rise test, and permeability data from numerical modeling, best fit for Equation (33) is found using nonlinear least square method to calculate r_{eff} of the wick structure.

Assuming that the hydrostatic pressure can be neglected at early stage of capillary rise process, Equation (31) reduces to Washburn's equation [56]:

$$x^2 = \frac{4\sigma K}{r_{eff}\mu\varepsilon} t \tag{34}$$

Equation (13) can be rearranged to have capillary performance parameter K/r_{eff} [38]:

$$\frac{K}{r_{eff}} = \frac{\mu \varepsilon x^2}{4\sigma t} \tag{35}$$

Equation (35) can be expressed in another form of capillary performance parameter $\Delta P_{cap} K$ as used in [57]:

$$\Delta P_{cap} K = \frac{\mu \varepsilon x^2}{2t} \tag{36}$$

4.3.1.7 Uncertainty analysis

Wick porosity is calculated using diameter, pitch of micropost structures measured by optical profiler, and the uncertainty is estimated to be ~2%. Since the precise control of copper plating thickness over 1 cm × 5 cm area is difficult to achieve, pillar height at different locations are measured to report its uncertainty. 3 different locations (left edge, center and right edge of the wick area) in 4 different wick heights (1 cm, 2 cm, 3 cm, and 4 cm) are chosen for measurement, and the average of measured pillar height are used for uncertainty calculation. The representative uncertainty of pillar height is estimated to be ~15%. The uncertainty of viscosity and density of water is calculated based on the variation of temperature during the tests and found to be ~1%. Pressure transducers are calibrated using pressure transducer calibrator (OMEGA DPI 610 Pressure Calibrator) and the uncertainty is estimated to be ~2.5%. The total uncertainty of permeability is calculated to be ~10%. For capillary rate-of-rise test, the liquid rise height and time are measured by performing frame by frame image analysis acquired from the video recorded with high speed camera at 100 frames per second (fps) rate. The liquid rise height measurement uncertainty is calculated by using 5 sets of time data measured when liquid front reaches

at wick heights ranging from 0.5 cm to 4.5 cm with 0.5 cm increments. The representative uncertainty of measurement is ~12%, estimated for wick structure with porosity of 0.45.

4.3.1.8 Permeability results

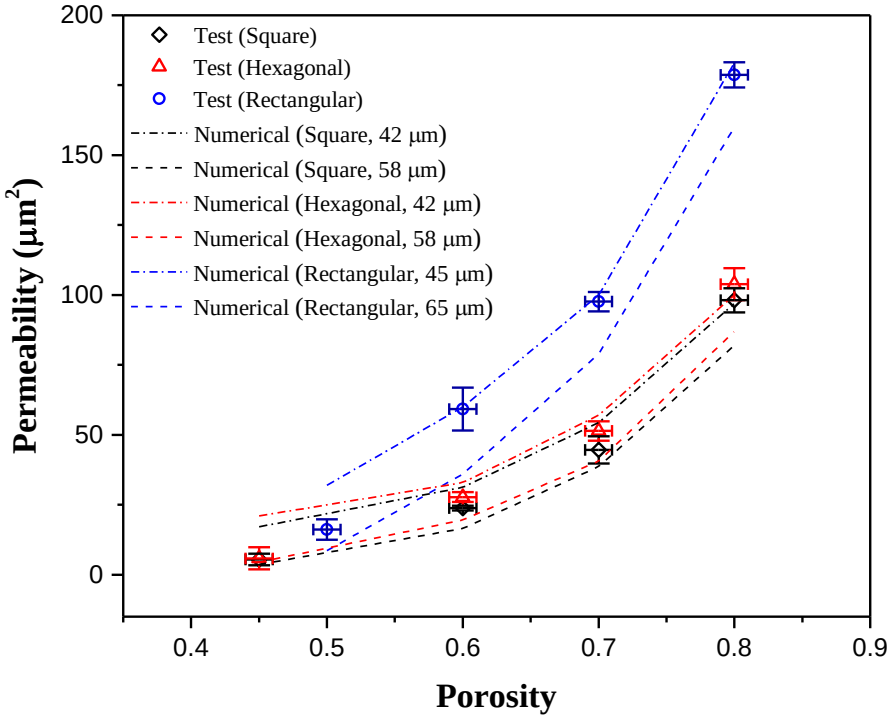


Figure 4.9 Comparison of permeability test results with numerical modeling results for micro post arrays in different arrangement and porosity.

Figure 4.9 shows permeability test results, along with the representative upper and lower limits calculated from two extreme sample height conditions shown in Figure 4.6 (b) and (c). The test data from samples with square and hexagonal pillar arrangements falls within the permeability values calculated from pillar height of 42 and 58 μm. However, test data from rectangular arrangement samples lies within 45 μm and 65 μm range, showing higher average pillar height than other samples. The effect of such height difference between rectangular arrangement sample and other samples on the test result of

rectangular arrangement is estimated to be ~3%, and considered negligible. Among the three different micropost arrangements, rectangular arrangement shows the highest permeability at each porosity condition due to its larger flow path than other arrangements. Difference of permeability between rectangular and other arrangements becomes larger, as the difference in pillar pitches between different arrangements becomes larger at higher porosities. Hexagonal arrangement shows ~5% higher permeability than square arrangement, which agrees with the trend predicted from modeling.

Permeability test results from forced liquid test method, however, cannot be directly applied to capillary rise equation (Equation (31)) for capillary radius measurement, as the result is affected by the cover plate of test section. Since permeability measurement is difficult when the top side of the array is exposed to the ambient, another numerical model is developed to predict permeability of pillar arrays under such condition. For this new model, average pillar height calculated from upper and lower limit case study is used to develop a representative unit cell of each pillar arrangement model. Free shear boundary condition is applied to water-air interface, and the shape of the water-air interface is assumed to be flat. Boundary conditions for all remaining surfaces are kept the same as shown in Figure 4.7 (b).

Figure 4.10 compares the permeability of samples acquired from the numerical model with flat meniscus assumption, and the model that accounts for the meniscus curvature. The meniscus shape is calculated from SE simulations by using contact angle of 55° as reported in [43], which used silicon oxide coated silicon micropillars for capillary radius test. Permeability under different contact angles is also calculated for sensitive analysis. As the contact angle decreases, permeability also decreases due to the sharp edges

formed between pillar surface and fluid. The permeability of pillar array with 0.8 porosity is affected the most by the meniscus shape: Changing 55° contact angle by ±20° results in the change of permeability value by ~ ±20%, and contact angle of 0° makes permeability value decrease by~ 35%.

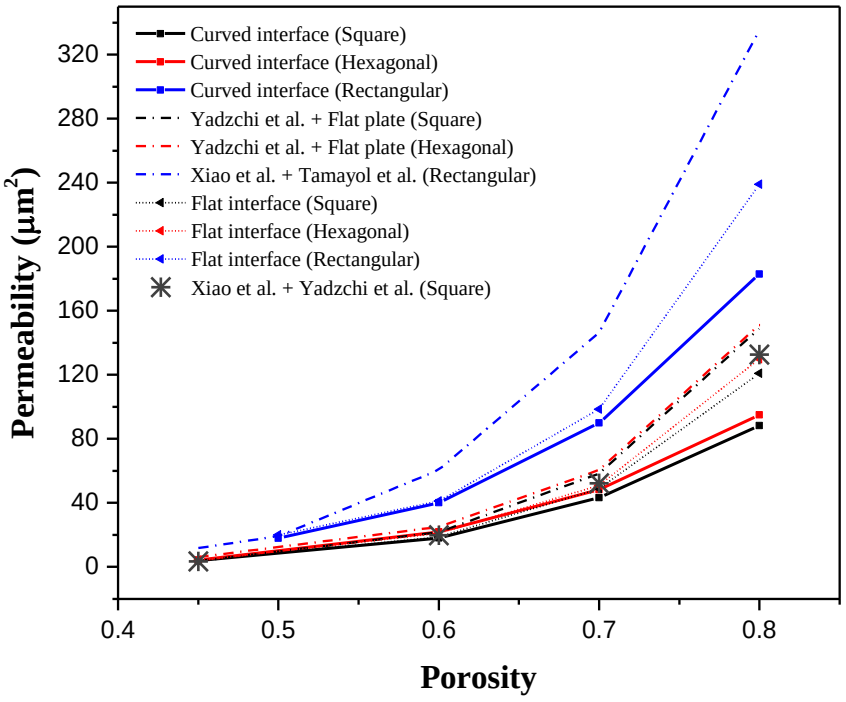


Figure 4.10 Comparison of permeability results from different numerical and analytical models.

Results from existing permeability models listed in Table 4.2 are also presented together in Figure 4.10. As the model from Yazdchi et al. (Equation (26)) was developed for unbounded cylinder array, an additional term is needed to account for the pressure drop caused by bottom surface of the sample. Utilizing the fact that total pressure drop is equal to the sum of the individual component pressure drops, and assuming a constant superficial velocity through the pillar array, total non-dimensionalized permeability K^*_{total} can be expressed as [41]:

$$K^*_{total} = \left(\frac{1}{K^*_{cyl}} + \frac{1}{K^*_{plate}} \right)^{-1} \tag{37}$$

where K^*_{cyl} is two-dimensional (2D) permeability of a cylinder array, and K^*_{plate} is permeability of a flat plate. K^*_{plate} can be derived from steady, laminar flow with no-slip and free surface boundary conditions at bottom and top surface of control volume and can be expressed as [41]:

$$K^*_{plate} = \frac{1}{3}\left(\frac{h}{d}\right)^2 \varepsilon \tag{38}$$

where h is the height of control volume, d is pillar diameter and ε is porosity.

The model by Xiao et al. (Equation (27)) is also used to calculate total permeability of pillar array in square pattern, and Equation. (26) is utilized to calculate 2D permeability of a cylinder array (K^*_{cyl}) in Equation (26). Hale et al. [42] rewrote the expression by Tamayol and Bahrami (Equation (25)) in terms of separate x- and y-direction pillar spacings, and this expression is used to calculate K^*_{cyl} in Equation (27) to get total permeability of micropillar array in a rectangular pattern.

Table 4.3 summarizes the results shown in Figure 4.10, and compares the results from flat meniscus model with other models using % error. The comparison shows that the results from the model by Yadzchi et al. for square and hexagonal arrangements, combined with flat plate model match reasonably well with flat meniscus numerical model results, showing 3.1 ~ 23% error. A potential reason for the error is that the analytical models neglect the effect of velocity profile variation between flat plate and the pillar wall. The model proposed by Xiao et al. shows a good agreement with flat meniscus numerical model for pillars in square arrangement when K^*_{cyl} from the model by Yadzchi et al. is adopted,

with less than 10% of error over entire porosity range considered in this study. Brinkman's equation, however, shows higher error (up to ~48%) for rectangular arrangement when K_{cyl}^{*} is adopted from the model by Tamayol and Bahrami. Such deviation may come from the model's simplification of velocity profile within the pillars, by accounting for velocity variations in y direction only.

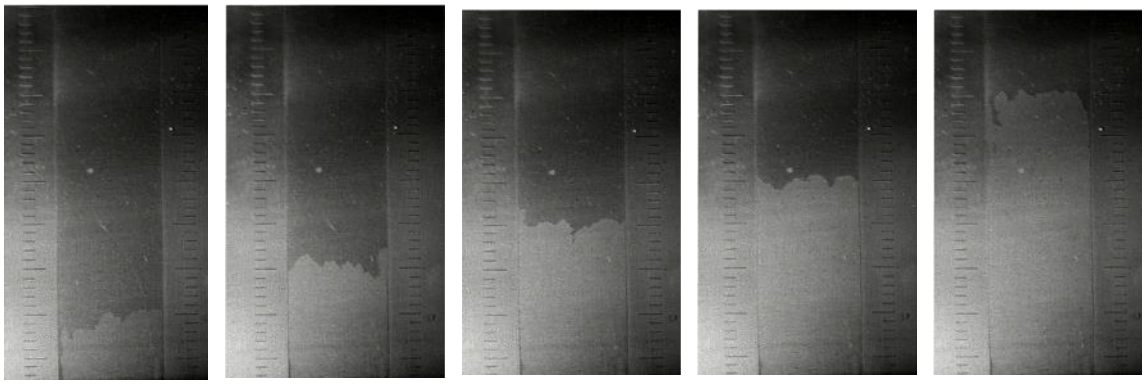
Table 4.3 Wick sample porosity, pitch size, and permeability calculated from a numerical model developed with flat meniscus shape. Results from other models are presented in % error with respect to flat meniscus modeling results.

Pillar arrangement	Porosity	Pitch (μm)	Flat interface (μm^2)	Error (%, Curved)	Error (%, Xiao)	Error (%, Yadzchi)	Error (%, Tamayol)
Square	0.45	60	3.8	1.2	7.7	3.1	—
	0.6	70	19	3.5	5.3	15	
	0.7	81	49	11	7.1	19	
	0.8	99	121	27	9.6	23	
Hexagonal	0.45	64	4.3	2.6	—	15	—
	0.6	75	21	4.1		19	
	0.7	87	51	10		19	
	0.8	107	130	27		16	
Rectangular	0.5	65/60	20	1.1	—	—	4
	0.6	82/60	41	2.1			48
	0.7	100/66	99	8.7			48
	0.8	140/70	239	23			40

While existing models over-estimate the permeability of tested wick structures, results from a numerical model that accounts for the meniscus shape formed between pillars show lower permeability compared to the results from the model with flat meniscus. The difference between flat and curved meniscus models becomes more pronounced (~27%) at higher porosities, showing meniscus shape affects permeability more for micropost arrays at larger pitches. Previous studies [38],[55] also show that the permeability of pillar type wicks is affected by meniscus shape significantly. To predict

the capillary radius from capillary rate of rise test more accurately, this study utilizes the permeability calculated from the numerical model with meniscus curvature.

4.3.1.9 Capillary rate of rise results



t = 500 ms t = 1240 ms t = 2180 ms t = 3340 ms t = 6880 ms

Figure 4.11 Recorded video frames of capillary rise at different time steps (Hexagonal arrangement, Porosity=0.8).

Figure 4.11 shows selected video frames of capillary rise of water in micropost array in hexagonal arrangement with porosity of 0.8. The time is recorded at each video frame when the highest liquid front reaches a certain height of the wick. Time versus height data points determined 8 times, and permeability values from numerical model with meniscus shape are used to find the best fit with Equation (33), as seen in Figure 4.12. Table 4.4 summarizes the effective capillary radius (r_{eff}) acquired from the fit, and compares the results with capillary radius predicted from SE simulation. The capillary performance (K/r_{eff}) of the samples are also presented in the Table 4.4.

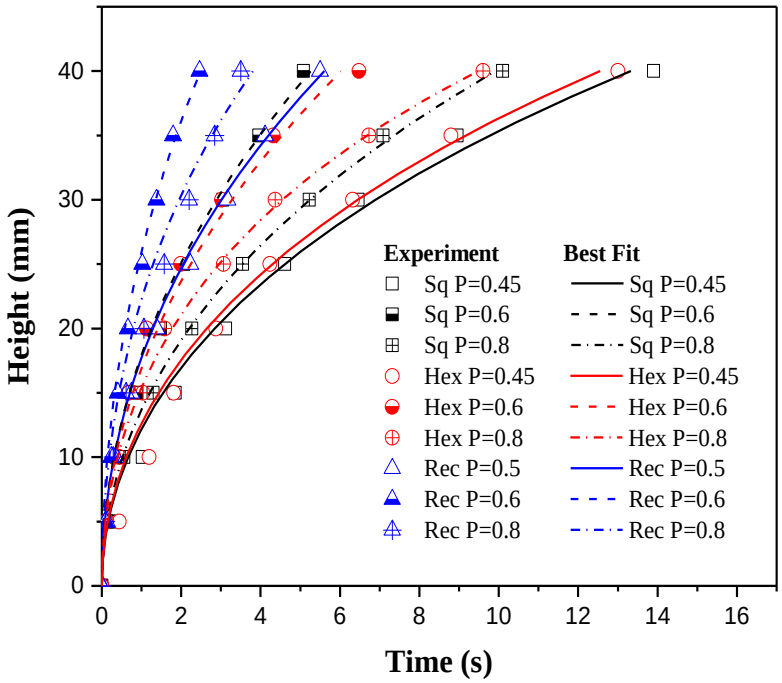


Figure 4.12 The height of the capillary rise versus time data of samples with different pillar arrangements and different porosity acquired from rate-of-rise test.

Table 4.4 Effective capillary radius and capillary performance parameters of samples (Results in parentheses are calculated using correlation from [42] with 55° contact angle).

Pillar arrangement	Porosity	r_{eff} (μm) from Test	r_{eff} (μm) from SE	Error (%)	$\frac{K}{r_{eff}}$ (μm)
Square	0.45	38	34	12	0.10
	0.6	60	59	1.7	0.30
	0.7	110	93	18	0.39
	0.8	222	157	41	0.40
Hexagonal	0.45	25	32	22	0.17
	0.6	52	59	12	0.42
	0.7	110	92	20	0.44
	0.8	187	158	18	0.51
Rectangular	0.5	48	39 (40)	23 (20)	0.38
	0.6	61	59 (60)	3.4 (1.7)	0.66
	0.7	83	92 (94)	9.8 (12)	1.08
	0.8	159	157 (162)	1.1 (1.8)	1.15

Samples with smaller porosity show smaller effective capillary radius than larger porosity, due to smaller spacing between the pillars. Predicted capillary radius agrees reasonably well with the test results, showing average error of 9~24%. Predicted capillary radius of rectangular arrangement from the current study is compared with [42], which expresses the capillary pressure equation with contact angle and porosity of the sample. At each porosity, micropost arrays in different arrangements show similar capillary radius, but the difference in permeability leads to different capillary performance parameter. Among the 3 types of pillar arrangement, micropillar sample with rectangular arrangement shows the highest capillary performance parameter due to its highest permeability, while generating similar capillary pressure compared to other pillar arrangements.

Washburn's equation (Equation (34)) has been widely used to characterize porous media with the capillary rate-of-rise test. The application of the equation, however, is limited to early stage of capillary rise when the hydrostatic pressure generated by water drawn by wick is negligible. In order to check the effect of hydrostatic pressure or gravity on the measured capillary performance parameter, Washburn's equation is used to calculate capillary performance parameter, and the results are compared with the results in Table 4.4.

Figure 4.13 shows the liquid rise at the initial stage of capillary rise of the sample in hexagonal arrangement with 0.8 porosity. After the capillary rise starts, the squared height of water rise shows parabolic increase up to 0.1 seconds. Then the squared height changes linearly with time, which follows Washburn's equation. A similar pattern is reported in [58], and the parabolic regime in Figure 4.13 is where the liquid inertia force is dominant, while the linear regime (Washburn regime) is governed by capillary and viscous

effects. The deviation from Washburn's equation occurs again ~10 seconds after the initial capillary rise, as the effect of hydrostatic pressure becomes more significant. To extract the capillary performance parameter with Washburn's equation, the linear fitting with data points in Washburn regime up to 10 seconds is performed. Table 4.5 summarizes the effect of hydrostatic pressure by comparing the capillary performance parameter acquired from two different equations, Equation (31), with the result from Equation (34).

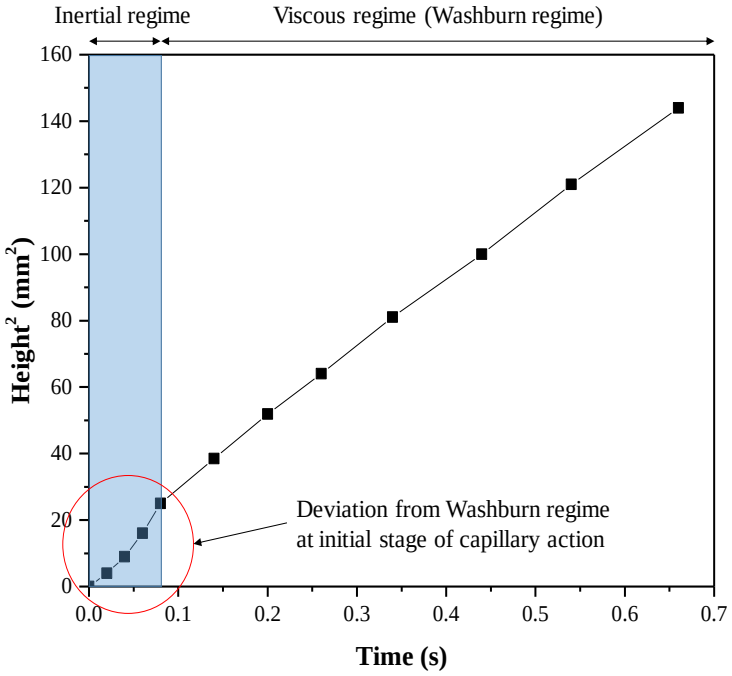


Figure 4.13 Square of liquid front height versus time data of micropost arrays in hexagonal arrangement with 0.8 porosity.

Capillary performance parameters from both equations show good agreement at low porosities (0.45, 0.5, and 0.6), with errors ranging from 2.4% to 18%. However, the error becomes more significant for wicks with higher porosities (0.7 and 0.8) due to relatively smaller capillary pressure of the samples, which in turn increases the effect of gravity or hydrostatic pressure. The ratio of capillary pressure to hydrostatic pressure for

each sample is calculated and presented in Table 4.5. The hydrostatic pressure is calculated for water height at 4 cm, where the capillary rise measurement is stopped. From the comparison, it was found that application of Washburn's equation is valid for samples with the ratio larger than 4, where the gravity effect can be neglected. For samples with the ratio smaller than 4, the capillary performance parameters are underestimated by Washburn's equation up to 46%, which indicates that the hydrostatic pressure effect should not be neglected to characterize the capillary performance of wicks with high porosities (0.7~0.8).

Table 4.5 Comparison of the capillary performance parameter of the wicks acquired with and without considering hydrostatic pressure effect.

Pillar arrangement	Porosity	K/r_{eff} (μm) with hydrostatic pressure effect (Eq. 10)	K/r_{eff} (μm) without hydrostatic pressure effect (Eq. 13)	Error (%)	$\Delta P_{cap}/\Delta\rho gh$
Square	0.45	0.10	0.12	18	11
	0.6	0.30	0.31	3.3	6.2
	0.7	0.39	0.21	46	3.9
	0.8	0.40	0.26	35	2.3
Hexagonal	0.45	0.17	0.16	5.9	15
	0.6	0.42	0.41	2.4	6.2
	0.7	0.44	0.37	16	3.9
	0.8	0.51	0.33	35	2.3
Rectangular	0.5	0.38	0.36	5.3	9.4
	0.6	0.66	0.78	18	6.2
	0.7	1.08	0.84	22	3.9
	0.8	1.15	0.75	35	2.3

4.3.2 Micropillar Wick Design for Vapor Chamber

Figure 4.14 shows the photomask layout of wick structures for the prototype vapor chamber and the pictures (top view) of micropillar array plated on the copper clad PCB fabricated following the process flow in Figure 4.1. The evaporator of the prototype consists of three different areas; wick, structural support, and soldering areas. Wick area is

where the micropillar structures are constructed. Based on the characterization study results, micropillar array with rectangular arrangement is adopted for the wick design to enhance the performance of the vapor chamber. Since the heat generated from the chips on the interposer will be conducted through copper TPVs and solder bumps connected to them, heat source with a small area (2 mm × 2 mm) is used in this study, and the wicks are designed accordingly: To facilitate water supply to the heat source area (center of the PCB, 2 mm × 2 mm), wick structures are aligned so that pillars with wider pitch can face the evaporator area. The diameter of the micropillar is 50 μm, pitches are 82/60 μm. Structural support contact area in Figure 4.14 is where the large copper posts (diameter: 2 mm) which extrudes from the condenser land on.

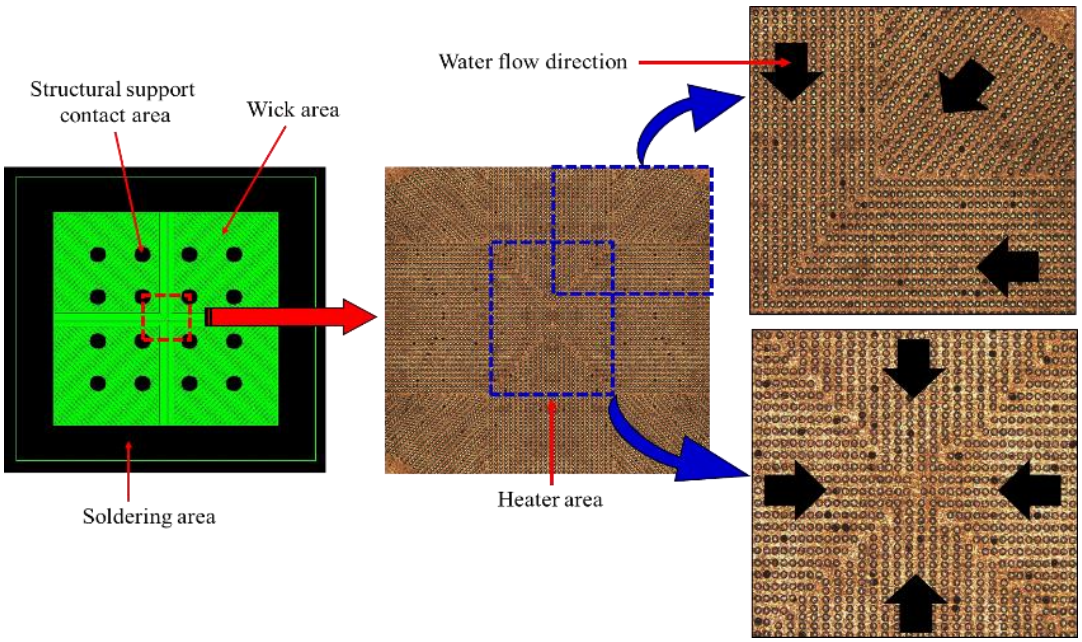


Figure 4.14 Evaporator side wick structure (micropillar array in rectangular arrangement, porosity=0.6) mask layout (left), microscopic image of fabricated sample's center area (center), and zoomed view of the center and upper right area (right).

4.4 Mechanical Design and Machining of Condenser

The condenser of vapor chamber is machined by cutting large oxygen-free copper plate (152 mm × 152 mm) into small pieces with the size of 40 mm × 40 mm and different thicknesses (560 μm ~ 970 μm), and milling them to form cavity and structural support pillars. The location of the pillars is determined through FE simulation with COMSOL®. Figures 4.15 shows the displacement analysis results performed on a quarter of vapor chamber structure (thickness: 950 μm). For boundary condition, uniform pressure of 10^5 Pa is applied on the top surface to simulate atmospheric pressure effect on the deformation of the device when the device cavity is under high level of vacuum. Fixed condition is applied to the bottom surface, and symmetry conditions are used at the surfaces on the symmetry planes. Initial model without structural support shows the maximum deformation (> 6358 μm) occurs at the center of the device. After placing 8 supporting post structures in the cavity, the maximum deformation is decreased to 72 μm. Further adjustment on the location of the pillars results in the maximum deformation value of 23 μm.

Figure 4.16 displays final CAD drawing of condenser based on FE analysis and the photo of computer-controlled mechanical milling process used to machine the condenser. To avoid any in-plane movement and maintain the coplanarity of the sample during the milling process, a strong double-sided tape is applied at the bottom of the sample to fix it to the worktable.

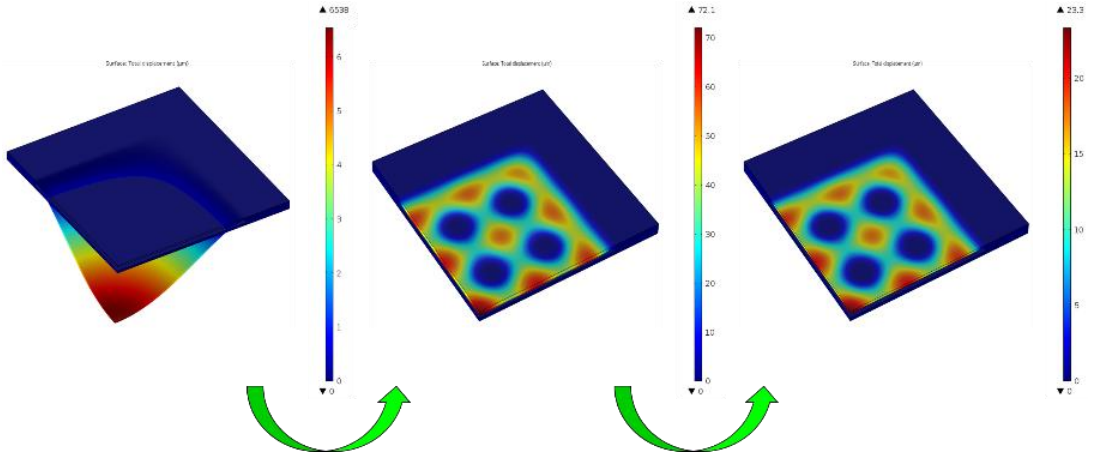


Figure 4.15 Condenser side design of vapor chamber. Displacement (μm) contour plot of the vapor chamber before (left, Max: 6538 μm) and after (middle, Max: 72 μm) the placement of structural support, and after the adjustment of the pillar position (right, Max: 23 μm).

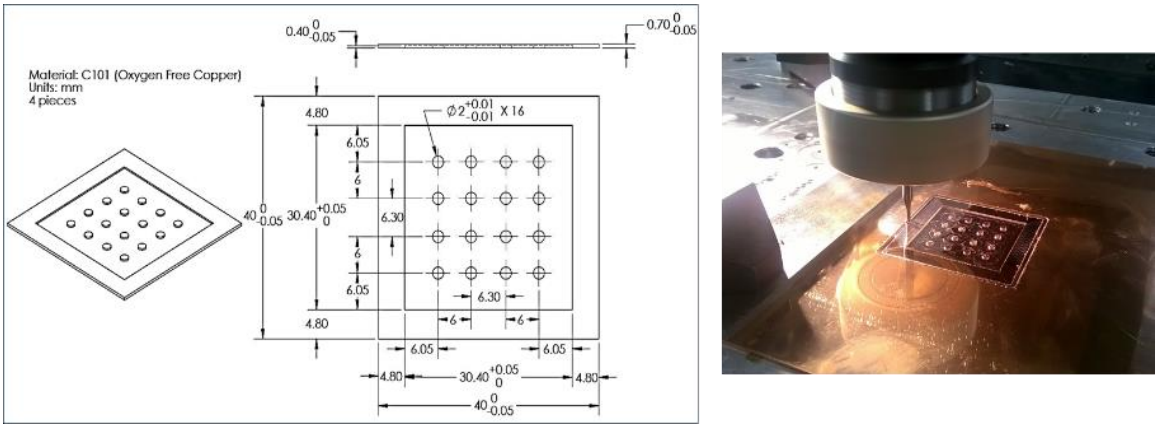


Figure 4.16 CAD drawing of the condenser (left) and mechanical milling process used for machining condenser.

4.5 Device Sealing

4.5.1 Device sealing with soldering

Welding and brazing are the most common methods used to join the different layers of the vapor chamber [59]. However, these technologies produce or require high

temperature conditions well above the critical temperature of PCB. Moreover, it is difficult to use those methods if the size of joining area is small. Laser welding may offer an alternative way to bond the layers due to its ability to deliver the power in precise locations, but the large difference in the thicknesses of two sections (copper layer on PCB (evaporator) and copper cover (condenser)) poses a difficulty as thin copper layer (~ 20 μm) on PCB is likely to get vaporized by the time when the edges of copper cover (thickness: 5 mm) get enough energy to be melted. Other challenges with laser welding are associated with material properties of copper; low absorptivity of infrared laser radiation on the copper surface at room temperature, low viscosity of the copper melt, and high thermal conductivity of copper [60].

Researchers have used different technologies for sealing their heat pipes/vapor chambers. Peterson et al. [61] used UV bonding process to bond the silicon wafer substrate patterned with rectangular/ triangular grooves and Pyrex cover. Le Berre et al. [62] utilized silicon direct bonding process followed by annealing at 1100 °C to seal their silicon heat pipe with silicon wafer. Cai et al. [63] applied glass-frit bonding at 410 °C to bond three silicon wafer layers to develop 3 mm-thick silicon vapor chamber. To assemble polymer-based flexible heat pipe, Oshman et al. [64] thermally welded two polyethylene terephthalate (PET) films using heat sealing machine, and sealed charging tube with vacuum epoxy. Ding et al. [65] used a pulsed neodymium-doped yttrium aluminum garnet (ND:YAG) laser with a wavelength of 1064 nm to weld titanium substrate with titanium square lid. The author explained that the advantage of laser welding over conventional high temperature thermocompression bonding is the elimination of device failure caused by thermo-mechanical stresses. Most of the approaches used in previous works to seal the

silicon based or metal based heat pipes/vapor chambers are high temperature processes, which are not applicable for sealing PCB based devices.

Soldering is a low temperature joining process ranging from near room temperature to several hundred degrees Celsius, and commonly used for heat pipe products since it is low-cost, reworkable, and simple. However, soldering on copper often becomes challenging as copper surface gets easily oxidized and deteriorated when left unprotected. Since the contaminated surface results in poor solderability, PCB with exposed copper circuitry undergoes a surface finish process to prevent its contamination, which forms additional metal interfaces on top of the copper surface. ENIG is one of the surface finishes used for copper structures on PCB, which adds a two-layer metallic coating of thin (50 nm ~ 100 nm) gold over nickel (2 ~ 6 μm). Nickel plated on copper works as a diffusion barrier that prevents copper from migrating to the other metal (gold) layer. The gold layer protects the nickel from oxidation or contamination which offers a long shelf life of the PCB before being soldered.

In this study, soldering is chosen for joining the PCB (evaporator) and copper plate (condenser) due to the temperature limit of PCB. Soldering is also applied to the interface between charging/evacuation tubes and holes on the substrate. To enhance soldering quality and achieve hermetic sealing, different chemical processes are applied to two different components (PCB and copper plate).

4.5.2 Preparation of evaporator side for soldering

ENIG process is used to protect copper structures on PCB from contamination and provide better solderability. Another advantage of having ENIG surface finish on copper

structures is that gold surface exhibit good water wettability compared to copper [66], which enhances capillary performance of wick structures on PCB.

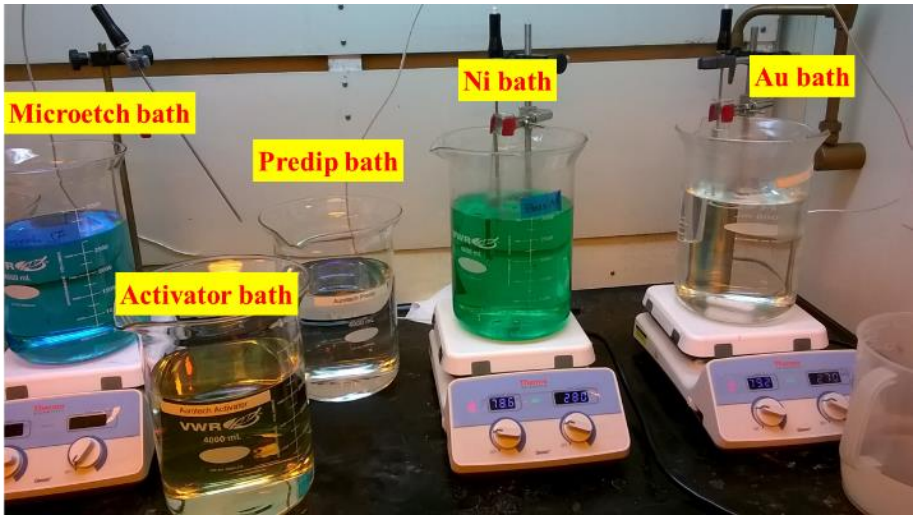


Figure 4.17 Setup for surface finish (ENIG) process.

Figure 4.17 shows the setup of ENIG process for PCB. The ENIG starts with an oxide-clean process by dipping copper clad PCB samples into an acidic-wetting solution (Aurotech) to clean the copper structures. The second step is micro-etching process, which cleans and roughens the surface of copper structures with slow etching rate. The resulting copper surface have a uniform and fine-grain etch, which results in an optimal bonding surface for copper and subsequent layer. The third step is predip process, which is an acid (sulfuric acid) dip process to protect activator solution, used in the next step, from non-compatible drag-in. The fourth process is activating the copper surface for electroless nickel deposition by dipping the sample into Aurotech Activator, which consists of palladium (Pd) ions and sulfuric acid with DI water. Activated sample is then rinsed with DI water and dipped into electroless nickel bath (Aurotech) to deposit uniform nickel-phosphorous alloy (~ 2 µm) for about 12 minutes. To finish ENIG surface finish process,

a thin layer of gold is deposited on nickel surface (~ 75 nm) by placing the sample in gold bath for 10 minutes. Figure 4.18 presents copper wick samples on PCB before and after ENIG.

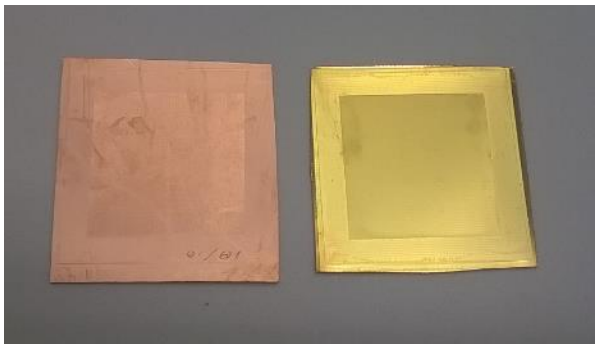


Figure 4.18 PCB wick samples before ENIG (left) and after ENIG (right).

4.5.3 Preparation of condenser side for soldering

Figure 4.19 Setup for SnAg solder electroplating.

Instead of using wire or preform type solder, SnAg alloy (Sn-3.5Ag) solder is electroplated on the periphery area of copper plate (condenser) using solderfill Ag800 solution from Atotech. Figure 4.19 shows the setup used for SnAG solder plating. Prior to

the plating, copper plate is first cleaned with acetone followed by IPA, and DI water rinse. Then all surfaces of the sample except the soldering area is masked with adhesive tape to prevent the surfaces from being plated. After submerging the sample and anode in solder plating solution, current density of 1.5 mA/cm^2 is applied. The calculated plating rate is 0.75 µm, which results in the solder layer with ~45 µm thickness after 1 hour of plating. Figure 4.20 compares the copper plate before and after the plating.

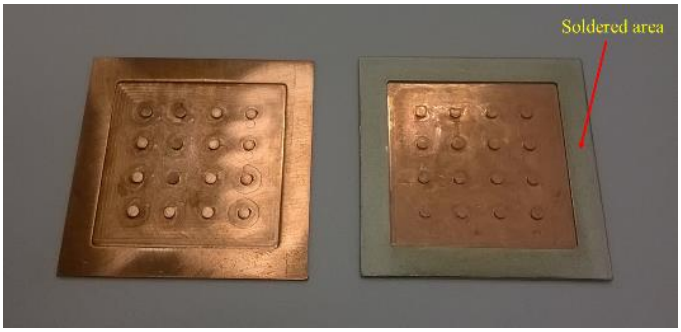


Figure 4.20 Copper plate before (left) and after solder plating.

4.5.4 Soldering PCB and Copper Plate

Figure 4.21 Reflow oven used for PCB/Copper plate soldering.

PCB with ENIG surface finish and copper plate with electroplated solder are put together and placed on the reflow oven shown in Figure 4.21 (OmniFlo 5, Electrovert). The oven is equipped with an edge rail conveyor system, which slowly moves sample through 5 different temperature zones controlled by top and bottom convection heaters. Nitrogen gas is injected into the oven during the reflow to minimize the oxidation of the sample. To apply an adequate amount of pressure for soldering, the edges of PCB and copper plate are bound with binder clips as shown in Figure 4.22. The sample is then fixed on the large PCB (152 mm × 152 mm) using Kapton tape to keep it from blowing away during the reflow process. After turning on the oven, desired temperature setpoints of each zone are entered. Once the temperature readings reach the setpoints, the PCB is placed on the conveyor belt to start the reflow process.

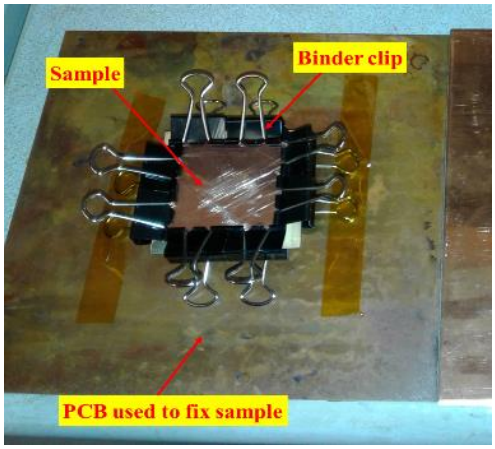


Figure 4.22 PCB/copper plate prepared for soldering.

To find the proper heating profile for the soldering, five dummy samples are tested under different temperature conditions. The soldering was successful when the first heating zone is at 100 °C, the second zone is at 175 °C, the third zone is at 190 °C, the fourth zone is at 240 °C, and the fifth zone is at 265 °C.

4.5.5 X-ray inspection

To visually inspect soldering quality, X-ray images of the soldered sample are taken (Dage X-Ray XD7600NT). Figure 4.23 displays the X-ray image of the soldered sample, and the picture of PCB side after detaching copper cover plate from the sample. The comparison of two images shows that X-ray image can be used to detect the area with poor solder wetting. The soldering quality in Figure 4.23 was not good as the pressure on the sample was not high enough to make PCB and copper plate in contact with each other during the reflow process.

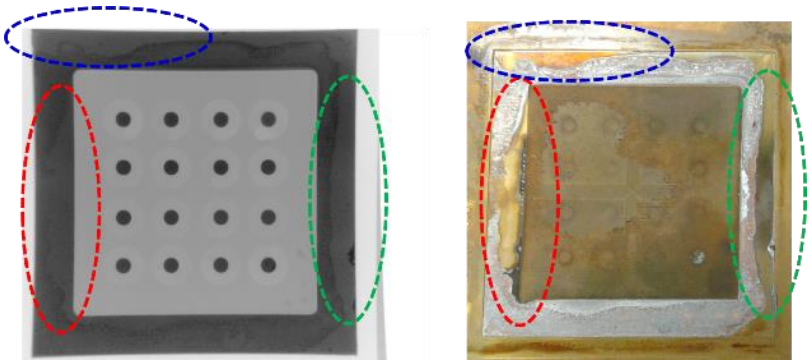


Figure 4.23 X-ray image (left) of soldered sample and photo image (right) of PCB side of the sample.

To apply higher and even pressure on the soldering area, smaller binder clips are used to hold PCB and copper cover together. Figure 4.24 shows the X-ray image of the sample soldered with higher pressure. Although some voids are still detected from the image inspection, the soldering quality on periphery area becomes better with higher pressure. However, some of the solders flowed into the wick structure area due to high pressure or excessive amount of solder. Since it is not easy to precisely control the pressure applied on the sample, the amount of solder is controlled instead by soldering only half of

the periphery area where the other half of the area is covered with adhesive tape during solder plating process. Figure 4.25 compares solder plated areas before and after the change of the soldering area.

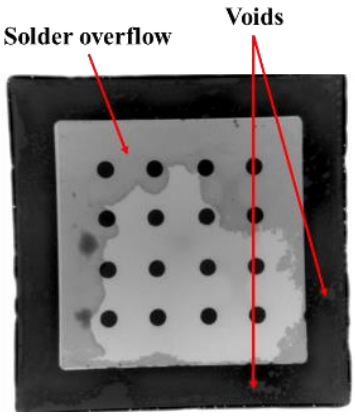


Figure 4.24 X-ray image of soldered sample with high pressure.

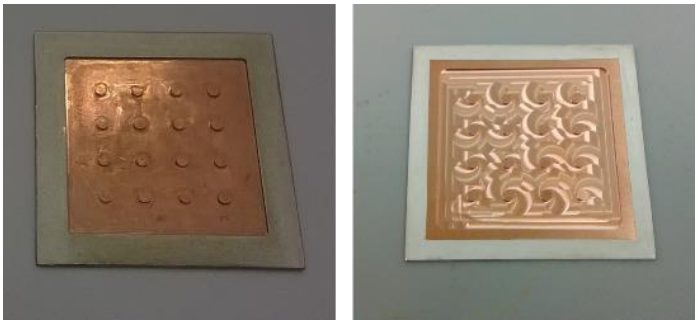


Figure 4.25 Copper cover with plated solder before (left) and after (right) masking half of the periphery area.

Figure 4.26 shows the X-ray image of soldered sample that uses copper plate with solder plated on the half of the periphery area as shown in the right image of Figure 4.25, and confirms better soldering quality without having any noticeable solder overflow in the wick area. Small voids are found in the soldered area from the image, but considered to be negligible as they do not seem to form air paths that continuously cross from inside to outside of cavity and vice versa. Further testing to check the hermetic sealing quality is

done by measuring the mass change of the sample after complete sealing of the device is done. More details about the sealing test result are presented in the device charging station section.

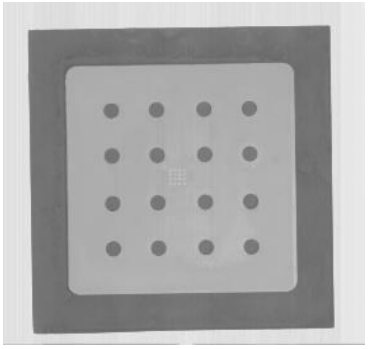


Figure 4.26 X-ray image of soldered sample with reduced solder.

4.5.6 Charging and evacuation tube sealing

Copper tubes (outer diameter: 1.59 mm, inner diameter: 0.88 mm) used to connect vapor chamber to vacuum pump and charging station are soldered to copper plate or PCB. After charging process is finished, the tubes are pinched off to produce a cold weld joint that provides a hermetic sealing. Cold welding is a solid-state bonding process between two surfaces that utilizes pressure and plastic deformation of the base metals [67]. To achieve perfect cold-welded joint at the tubes, a special pinch-off tool is often used [31]. However, this study utilized two types of ordinary pliers (diagonal cutting and long nose cutting pliers) to crimp and cut the tubes to get hermetically sealed copper tubes [68]. Prior to the crimping, the surface of the copper tubes is abraded with low-grit (P600) sandpaper, and cleaned with IPA and DI water. After evacuation or charging process is completed, the copper tubes are first crimped slowly using diagonal cutting plier. Then using the long nose cutting plier, one more crimping/cutting is done at the spot slightly above the firstly

crimped location. This approach results in the most reliable and repeatable sealing quality, which can hold vacuum level higher than 10^{-5} Torr. After the cutting, the tubes are sealed with low vapor pressure epoxy (Torr Seal®, Kurt J. Lesker) to provide mechanical strength and extra sealing to the tubes. Figure 4.27 shows the crimped and cut copper tubes after the charging.

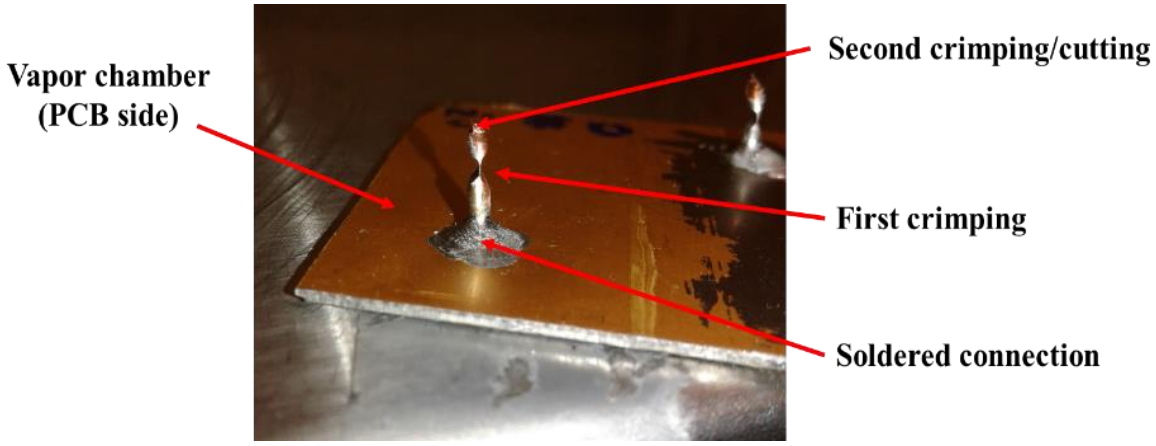


Figure 4.27 Sealing of charging/evacuation tubes.

4.6 Device charging/evacuation station

One of the main factors that affects the performance of two-phase cooling device is evacuation of the system prior to charging to remove non-condensable gases (NCGs) [69]. NCGs degrades the performance of two-phase cooling devices by blocking the part of condenser area. The effect of NCGs varies depending on their concentrations, but can't be ignored as the thermal conductivities of gases are usually 10^4 times smaller than that of copper. In addition to the removal of NCGs, charging the proper amount of degassed working fluid into the system is also an important process to achieve a successful fabrication of heat pipe/vapor chamber. However, the charging of such devices is becoming

more challenging as the size of the devices is getting smaller, which requires a high-precision control on the amount of fluid to be charged.

There have been several research efforts to develop a methodology for filling small heat pipes with small volumes. Peterson et al. [61] reported that reliable charging of micro heat pipe was accomplished by using pressure and temperature controlled chamber. After placing heat pipe in the chamber, the chamber was evacuated. Then a predetermined amount of working fluid is added and the chamber is heated to a point above the critical temperature of the working fluid. The heat pipe is then sealed while inside the chamber using ionic or UV bonding process. Le Berre et al. [62] filled their micro heat pipe array with vaporized working fluid and cooled the device to condense the vapor. The amount of working fluid in the heat pipe was deduced from temperature and pressure measurement in an additional chamber where the fluid is transferred after the filling. Gao et al. [70] introduced three different charging methods for miniature heat pipe (micro-syringe method, capillary tubing method, and thermodynamic equilibrium method) and demonstrated charging capability of thermodynamic equilibrium and micro-syringe methods by charging two types of mini-sized ceramic heat pipe (12.2 mm × 89.5 mm × 2.95 mm and 9.6 mm × 89.5 mm × 3.4 mm). Ababneh et al. [71] developed a new charging station that can charge a very small volume of working fluid by using a burette with fine resolution (0.01 ml). The filling uncertainty of the station was ± 1.64 µl.

The geometric dimensions of the wick structure for the prototype of device is 30 mm × 30 mm × 50 µm. If the porosity of the wick is 0.6, and wick pores are to be fully saturated, the amount of water needs to be charged in the device is ~ 27 µl. Since the effect of wick saturation ratio is significant [68], it is important to control the amount of working

fluid to be charged precisely. The work presented by Ababneh et al. is capable of precisely charging the required working fluid into the prototype. However, the system is complicated and requires several valves, fittings, and tubes. This study uses peristaltic pump (Masterflex® L/S Digital Drive Model: 07522-30 with Easy-Load® II Model: 77200-50), which can dispense fluid by volume in 0.001 mL to 99,999 mL, to precisely control the amount of charging fluid. Turbo-molecular pump (HiCube 80 Eco DN 40, Pfeiffer Vacuum) is used to vacuum the vapor chamber prior to filling. Figure 4.28 describes the schematic of filling station used in this study.

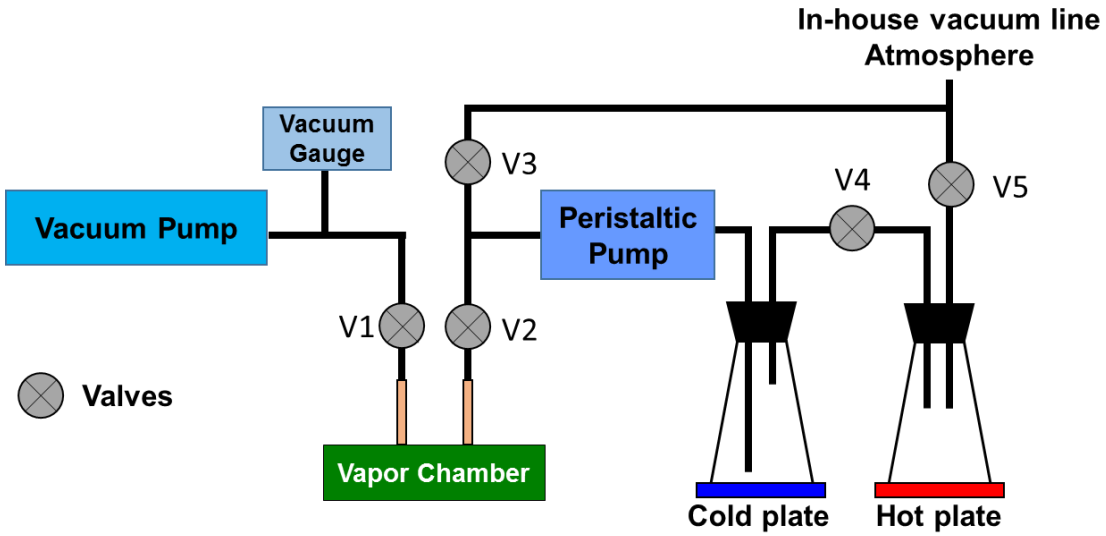


Figure 4.28 Schematic of filling station with peristaltic pump.

Filling station consists of three major parts. The first part is a water processing part, which boils and condenses DI water (total organic carbon level: 1 ppb) to reduce the oxygen dissolved in it. The second part is water pumping part, which is operated by peristaltic pump connected to the container where water vapor is condensed. The third part vacuuming part, performed by turbomolecular pump. The vacuum gauge (digital cold

cathode sensor) installed between valve 1 (V1) and vacuum pump can read pressure level ranging from 10^{-8} to 10^{-2} hPa.

As the performance of charging station is largely dependent on the performance of peristaltic pump, the pump's capability of delivering µl-scale water is tested and calibrated. The test is done by loading DI water at the pump and discharging it to a container with three different volume setpoints at volume discharge mode setting. The mass of the container is measured before and after the discharging by using a high-precision analytical balance (HR-100AZ, A&D) with a tenth of a milligram (0.1 µl for water) resolution. Four measurements at each volume discharging setpoint is performed, and Table 4.6 summarizes the results. The measurement shows consistent results at each pump setting, showing a minimum difference of 0.4 µl at 30 µl setting and a maximum difference of 2.2 µl at 20 µl setting, and confirms the pump's performance. The averages of the mass differences are used to find a relationship with the pump settings, which is used to find a proper pump setting for charging vapor chamber with the target volume of water.

Table 4.6 Mass of the water container measured before and after the discharging with different discharge volume settings. The difference of mass measured before and after the discharging is also presented.

	1st Measurement (mg)		2nd Measurement (mg)		3rd Measurement (mg)		4th Measurement (mg)	
	Before	After	Before	After	Before	After	Before	After
10 µl setting	5419.6	5449.2	5422.6	5450.7	5421.4	5451.5	5422.1	5451.2
	29.6		28.1		30.1		29.1	
20 µl setting	5421.5	5478.6	5304.1	5363.1	5304.8	5363.4	5329.5	5385.7
	57.1		58.3		59.3		57.2	
30 µl setting	5420.9	5508.7	5420.9	5508.3	5624.3	5712.1	5624.6	5712.3
	87.4		87.8		87.5		87.7	

To start the charging process, valve 1 (V1) is opened and valve 2 (V2) is closed. Then the turbomolecular pump is turned on and waited for the vacuum reading to reach $10^{-4} \sim 10^{-5}$ Torr. The vacuum pumping is performed for 24 hours to degas the cavity of vapor chamber. After pumping is completed, the flask is filled with DI water and boiled with hot plate. When the boiling starts, valve 5 (V5) is slightly closed and valve 4 (V4) is opened to allow water vapor flow into the flask on cold plate. When having enough amount of distilled water, valves 3, 4, 5 (V3, V4, V5) are opened to vacuum the system. After few hours of vacuuming, load the Tygon® tube on the peristaltic pump and introduce atmospheric pressure to the system by closing V3 and disconnecting the system from in-house vacuum line so that water can be pumped and loaded in Tygon® tube. Then copper tube connected to V1 is pinched off, and V2 is slowly opened. The peristaltic pump is turned on and starts the water pumping toward the vapor chamber at slow flow rate (10~30 µl/min) with continuous pumping mode setting. When water reaches the end of the charging tube, pumping is stopped and the pump setting is changed to volume dispense mode, which pauses its operation of the pump when the vapor chamber is charged with the desired amount of water. After charging is finished, the charging tube is crimped and cut to complete the charging process.

CHAPTER 5. THERMAL PERFORMANCE OF VAPOR CHAMBER EMBEDED PCB

In the previous chapter, fabrication process of vapor chamber embedded in PCB was described. This chapter presents test setup and procedure for thermal performance measurement of prototype vapor chamber. The test results are also presented and discussed.

5.1 Heat Transport Limitations of Prototype Vapor Chamber

Prior to the performance measurement, various performance limits of the prototype vapor chamber are investigated to predict the power envelope of the prototype vapor chamber limited by capillary, viscous, sonic, entrainment, and boiling limitations.

5.1.1.1 Capillary limitation

During the heat pipe operation, the working fluid is driven by capillary pressure differences across the fluid-vapor interfaces in the evaporator and condenser. Since the capillary difference drives the circulation of the fluid in the heat pipes, dryout occurs at the evaporator wick when the maximum capillary pressure is less than sum of all pressure losses in the heat pipe. For most heat pipes, the maximum heat transfer rate posed by capillary limitation can be expressed as [72]:

$$\dot{Q}_c = \left(\frac{2}{r_c} - \rho_l g l_t \sin\theta \right) \left[\frac{\rho_l \sigma_l h_{fg}}{\mu_l} \right] \left[\frac{A_w K}{l_{eff}} \right] \tag{39}$$

where r_c is the capillary radius of wick in evaporator (m), ρ_l is the liquid density (kg/m^3), g is the gravity acceleration (m/s^2), and l_t is the total length of heat pipe (m), θ is the inclination angle of heat pipe, σ_l is the fluid surface tension (N/m), h_{fg} is the latent heat

of vaporization (J/kg), μ_l is the liquid viscosity (Pa·s), A_w is the cross-sectional area of the wick (m^2), K is wick permeability (m^2), and l_{eff} is the length of the heat pipe.

5.1.1.2 Viscous limitation

At low temperature, vapor pressure at evaporator region may not be large enough to drive the vapor from the evaporator to condenser. In this case, the total vapor pressure will be balanced by viscous forces, which makes total vapor pressure in the vapor space insufficient to sustain an increased flow and limits the performance of heat pipes. Assuming isothermal ideal gas for the vapor and zero vapor pressure at the condenser, viscous limitation can be expressed as [73]

$$\dot{Q}_v = \frac{\pi r_v^4 h_{fg} \rho_v P_v}{12 \mu_v l_{eff}} \tag{40}$$

where r_v is the cross-sectional radius of the vapor core (m), h_{fg} is the latent heat of vaporization (J/kg), ρ_v is the vapor density (kg/m^3), P_v is the vapor pressure (Pa), μ_v is the vapor viscosity (Pa·s), and l_{eff} is the effective length of the heat pipe (m).

5.1.1.3 Sonic limitation

The sonic limit is typically experienced in liquid metal heat pipe and occurs when the compressibility effect is considerable (M>0.2). Sonic limitation serves as an upper bound of the heat transport capacity and does not necessarily result in dryout of the evaporator. The sonic limit is given by:

$$\dot{Q}_s = 0.474 A_v h_{fg} (\rho_v P_v)^{0.5} \tag{41}$$

where A_v is the vapor core cross-sectional area (m^2), h_{fg} is the latent heat of vaporization (J/kg), ρ_v (kg/m^3) and P_v (Pa) are the vapor density and pressure at evaporator.

5.1.1.4 Entrainment limitation

As vapor and liquid move opposite direction in heat pipes, shear force is exerted on the liquid at liquid-vapor interface. When the shear force exceeds the surface tension of the liquid, liquid droplets are entrained into the vapor flow and carried toward the condenser. If the magnitude of the shear force is large enough, the entrainment can lead to dryout of the evaporator. The maximum transport capacity based on the entrainment can be written as:

$$\dot{Q}_e = A_v h_{fg} \left(\frac{\rho_v \sigma_l}{2 r_{c,ave}} \right)^{0.5} \tag{42}$$

where σ_l is the surface tension of liquid (N/m), $r_{c,ave}$ is the average capillary radius of the wick (m^2), h_{fg} is the latent heat of vaporization (J/kg), ρ_v is the vapor density (kg/m^3), A_v is the cross-sectional area of vapor core (m^2).

5.1.1.5 Boiling limitation

At high heat fluxes, nucleate boiling may occur in wick structures, which may block the liquid return and causes dryout at evaporator. Boiling limitation is determined by:

$$\dot{Q}_b = \frac{4\pi l_{eff} k_{eff} T_v \sigma_l}{h_{fg} \rho_v \ln\left(r_i / r_v \right)} \left(\frac{1}{r_n} - \frac{1}{r_{c,e}} \right) \tag{43}$$

where l_{eff} is the effective length of the heat pipe (m), k_{eff} is effective thermal conductivity of wick, T_v is the vapor saturation temperature (K), σ_l is the surface tension of liquid (N/m)

r_v is the cross-sectional radius of the vapor core (m), h_{fg} is the latent heat of vaporization (J/kg), ρ_v is the vapor density (kg/m^3), r_i is the inner container radius (m), r_n is the nucleation radius (m), $r_{c,e}$ is the capillary radius of wick (m).

Utilizing Equation (43) – (47), fluid properties at different temperature conditions, and geometric dimensions of the prototype (wick area: 30 mm × 30 mm, wick height: 50 μm, capillary radius: 61 μm, and wick permeability: 41 μm^2**),** various heat transfer limits are plotted together in Figure 5.1. Note that hydraulic diameter of rectangular shape is used to calculate cross-sectional radius of vapor core and inner container radius in Equation (47).

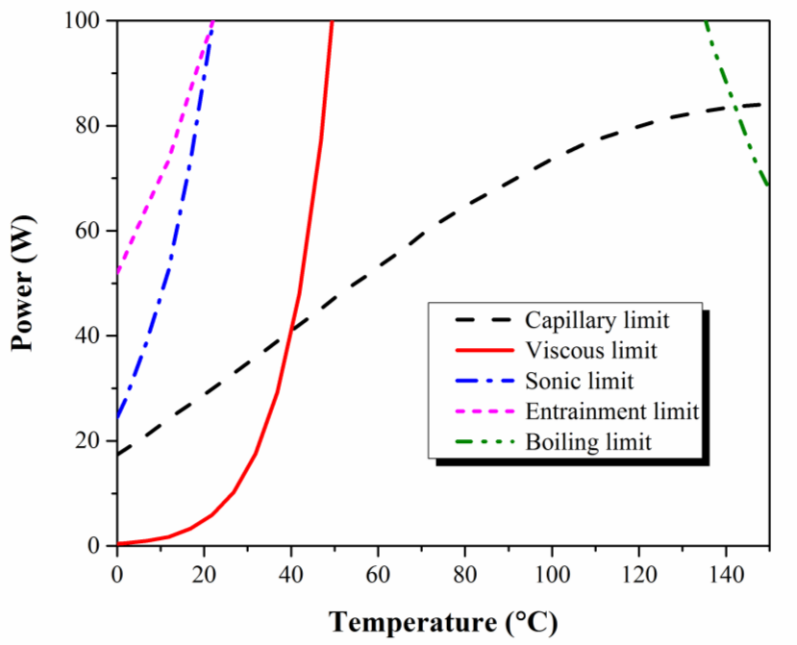


Figure 5.1 Various heat transfer limitations of prototype vapor chamber.

Heat transport capacity of prototype is limited to 6~48 W by viscous limit at the operation temperature ranging 20~40°C. Within temperature range of 45~140°C, capillary performance of the wick limits the device performance, while boiling limit restricts the heat transport at system temperature higher than 140 °C. Based on the heat transport limit

study, the prototype is able to transport target power (100 W/cm^2), without reaching the limits. I t must be emphasized that these predictions use a one-dimensional assumption for liquid and vapor flows. For a vapor chamber, the transport will be two-dimensional, and as such the predictions are meant to provide order of magnitude estimates.

5.2 Test Setup for Thermal Performance Test

A test setup is developed to evaluate the performance of the prototype vapor chambers. A schematic diagram of the test section configuration is shown in Figure 5.2.

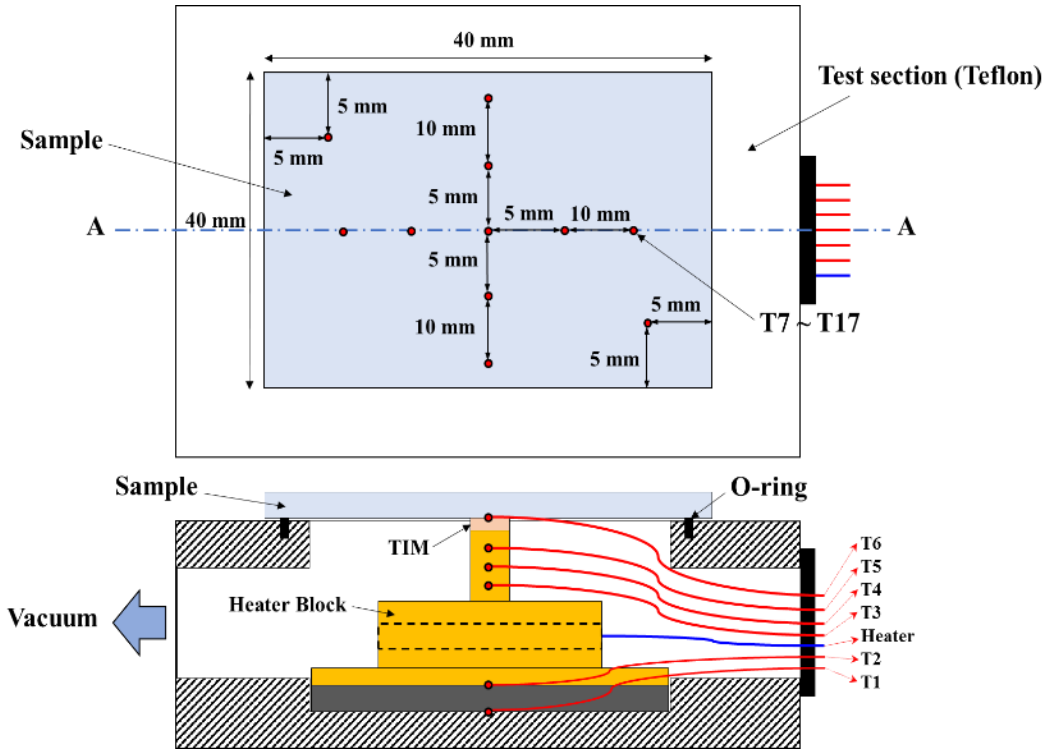


Figure 5.2 Schematic of the test section (Top and cross-sectional view)

The test section is comprised of the fabricated vapor chamber prototype sample, teflon block (k = 0.25 W/m·K) with a square cavity that has inlet and outlet ports, and a heater block assembled with a cartridge heater (Hotwatt, 10W @ 120V). The heater block

has a square pillar (2 mm × 2 mm) on top of the heater housing, and the pillar is attached to the sample with thermally conductive pad (Gap Pad®, Bergquist) to reduce the contact resistance. Three equidistant (~ 2 mm) holes with 0.5 mm diameter and 1 mm depth are drilled on the pillar. Three T-type wire thermocouples (0.25 mm diameter) are inserted into each hole and fixed by using thermally conductive epoxy (OB-200, OMEGA®). Thin foil type thermocouple with the thickness of 10 μm is used to measure the temperature of evaporator, and is placed between thermal interface material (TIM) and the heater block. The inlet port of the teflon block is used to connect heater wires to power supply (Sourcemeter 2400, Keithley) and thermocouples to data logger (Agilent 34970A Data Acquisition/Switching Unit). The inlet port is blocked by using a plug with a small hole where the wires go through. The extra space in a hole is sealed with adhesive silicone sealant. The outlet port is connected to a vacuum line to minimize the heat loss through convection. Two thermocouples are installed underneath the heater block to measure the heat loss through the bottom of heater block. O-ring is placed in a groove patterned around the cavity to seal the gap between the sample and the test section. Vacuum gauge is installed at the outlet port to confirm the vacuum level of the cavity.

Figure 5.3 shows the schematic diagram of test section with heat exchanger mounted on the top surface of vapor chamber sample. A thermal interface material (Thermal Pad, ARCTIC) is used to reduce thermal contact resistance between the heat exchanger and the sample. As shown in Figure 5.2, 11 thermocouples are attached on the top surface of the sample, and 6 thermocouples are installed at the heater block and its bottom for temperature measurement. Two T-type thermocouple probes with stainless sheath (0.5 mm diameter) are used to measure the inlet and outlet temperature of the water.

The temperature of water is controlled by constant temperature bath (AC150 Immersion Circulators, Thermo Sicentific), which is capable of control the water temperatures from -10°C to 200°C. To supply temperature controlled water to the heat exchanger, a gear pump (Micropump (GJ-N21), Max flow rate: 1740 mL/min) is used.

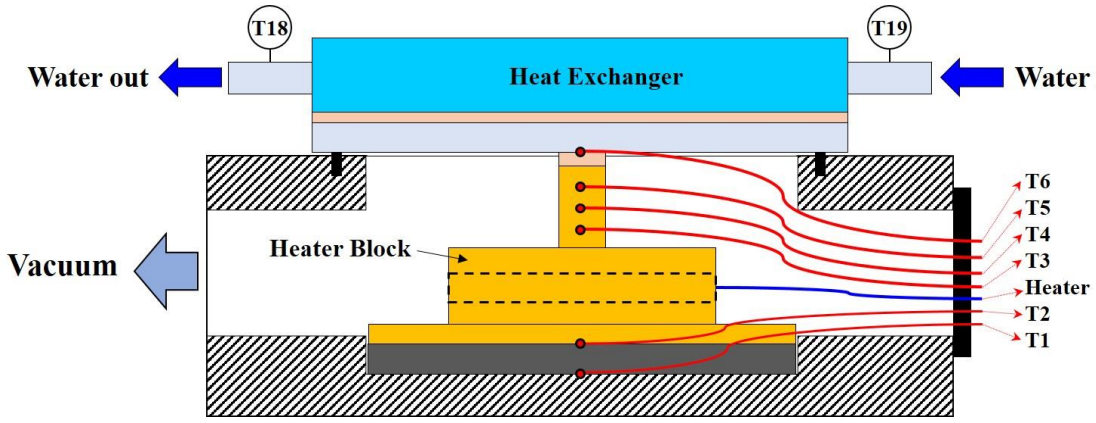


Figure 5.3 Test setup for vapor chamber thermal performance with water heat exchanger

Prior to the test, the mass flow rate from the gear pump at different settings is calibrated. Figure 5.4 displays the setup used for the calibration. The calibration process uses an electronic scale (Explorer® Pro, OHAUS®) connected to the computer via RS-232 interface to determine the mass change of the container at a selected pump setting for one minute. Six different settings (400, 600, 800, 1,000, 1,500, and 2,000 mL/min) are used for calibration. Table 5.1 shows the gear pump settings versus measured flow rate during the calibration. Based on the simple energy balance calculation, the flow rate setting of 800 mL/min is found to be enough for dissipating 10 W of heat by changing the water temperature less than 1°C. However, to provide excessive cooling condition on the condenser, flow rate setting of 1,800 mL/min (actual mass flow rate: 0.01 kg/s) is used during the performance test.

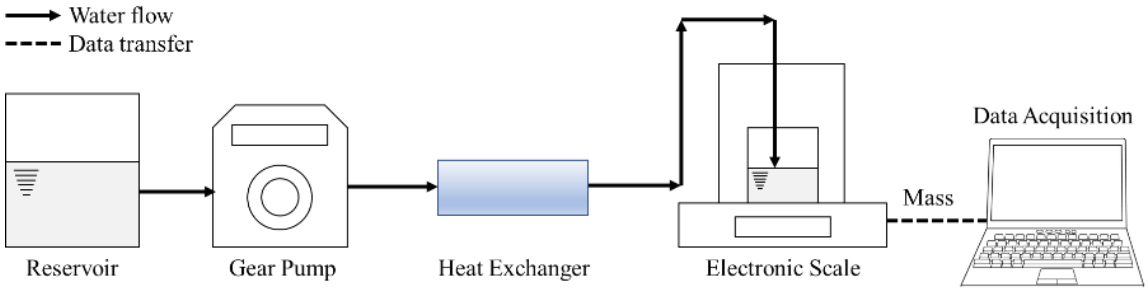


Figure 5.4 Setup for gear pump calibration

Table 5.1 Pump setting versus measured mass flow rate

Pump setting (mL/min)	400	600	800	1000	1500	2000
Actual measurement (g/min)	122.45	203.42	276.77	350.17	532.88	710.94

5.3 Performance Test

Copper block with the size of 40 mm × 40 mm × 950 µm and PCB sample plated with thick copper layer (40 mm × 40 mm, PCB thickness: 310 µm, Total thickness: ~930 µm) are tested prior to vapor chamber performance test. Thick copper layer on PCB is prepared by applying electrodeposition process at the top surface of copper clad PCB. However, due to non-uniform current distribution over the sample during the plating process, the sample shows different measured heights at different locations; hence, the thickness measured at 15 different locations is averaged and reported (Average: ~930 µm, Standard Deviation: 50 µm).

During the test, vacuum switch is always turned on to provide a tight contact between heater block and the sample. The vacuum also offers an insulated environment

around the heater block. Different heater power is used to test the sample's thermal resistance at different power input. Temperatures measured by 20 thermocouples are recorded and monitored to check if the system reaches steady-state, defined here as the condition when the temperature of the heater changes less than 0.1 ^{o}C within 10 minutes of measurement. After reaching steady-state, the temperature is recorded for 5 additional minutes to collect 60 temperature data points for each thermocouple. The final 60 data points are then averaged for thermal performance calculation. The thermal performance of the samples is compared by using the thermal resistance defined as:

$$R_{Sample} = \frac{T_{heater} - T_{cond,avg}}{Q} \tag{44}$$

where T_{heater} is the temperature of the heater labeled as T6 in Figure 5.2, $T_{cond,avg}$ is the average of condenser temperatures, T7~T17 in Figure 5.2, and Q is the heat input to the sample under test calculated from:

$$Q = -k_{Cu} A \frac{\Delta T}{\Delta x} \tag{45}$$

where k_{Cu} is the thermal conductivity of copper (387 W/m·K), A is the area of heater (4 mm^2), ΔT is the temperature difference, and Δx is the distance between thermocouples. Note that slope of a linear fit to the measured temperatures T3, T4, and T5 in Figure 5.3 is used to calculate the temperature gradient. The calculated Q represents the heat directly transported to the samples and accounts for the losses through the test section bottom and vacuum environment. After recording steady-state temperature, the heater power is increased to test the device at higher heating power conditions. The test continues until the heater temperature reaches the temperature limit of the test section. Two sets of tests are performed for each vapor chamber sample, and each set of tests takes about ~18 hours.

The uncertainty analysis is performed for heat flow rate (Q) and thermal resistance of samples (R_{Sample}). The uncertainty of heat flow rate (Q) is estimated by evaluating the expression in Equation (41):

$$U_Q = \left\{ \left(\frac{\partial Q}{\partial A} U_A \right)^2 + \left(\frac{\partial Q}{\partial \Delta x} U_{\Delta x} \right)^2 + \left(\frac{\partial Q}{\partial \Delta T} U_{\Delta T} \right)^2 \right\}^{1/2} \tag{46}$$

where U_A is an estimated heater area measurement uncertainty, $U_{\Delta x}$ is the uncertainty in the thermocouple location measurement, and $U_{\Delta T}$ is the uncertainty associated with temperature measurement. The uncertainty of heat flow rate calculated from Equation (41) is then used to calculate the uncertainty of thermal resistance by using the expression:

$$U_R = \left\{ \left(\frac{\partial R}{\partial \Delta T} U_{\Delta T} \right)^2 + \left(\frac{\partial R}{\partial Q} U_Q \right)^2 \right\}^{1/2} \tag{47}$$

All thermocouples are calibrated using OMEGA CL120 cool and heat source [74], and the uncertainty is estimated to be ±0.3 °C. The thermocouple location measurement uncertainty is ±0.1 mm and is attributed to the tolerance in the dimensions of thermocouple holes. The uncertainty of heater area is determined after measuring the width of heater pillar extension for 10 times, and estimated to be 10% of measured area. Uncertainty of the temperature is found to contribute the most to the uncertainty of the measured heat flow.

Figure 5.5 presents the thermal resistance of two samples, copper block and PCB, and compares the results with numerical modeling results from commercial software COMSOL®. To simulate excessive cooling condition on top surface of the sample, heat transfer coefficient condition of 5,000 W/m^2·K is applied, while other surfaces are considered to be adiabatic. The copper block (950 μm) shows ~23 times lower thermal resistance compared to that of PCB (~930 μm) with thick copper layer due to PCB's low

thermal conductivity (0.3 W/m·K). The comparison between the simulation and the test shows a reasonable agreement. Higher discrepancy between the thermal resistance between the model and the test may attribute to the sample's non-uniform thickness.

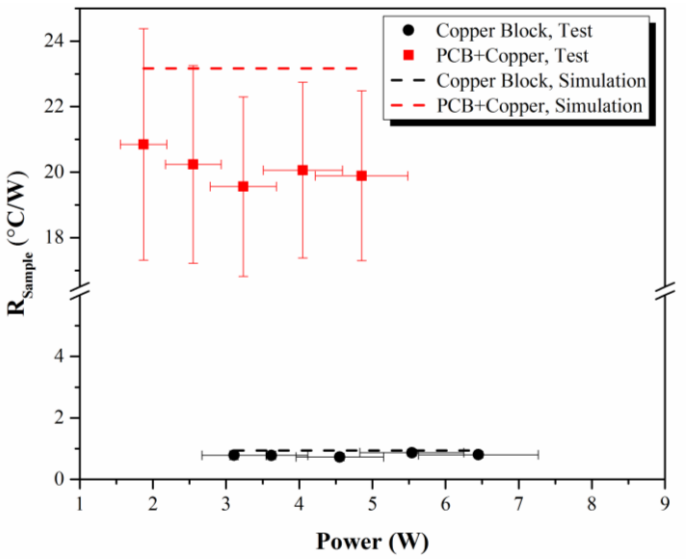


Figure 5.5 Copper block and PCB sample thermal resistance test results vs. simulation results.

Despite the effort to reduce the uncertainties associated with fabrication process, there can be unnoticed, and thus uncontrolled factors that may affect the performance of the device. Controlled factors during current fabrication process include: time that takes from the completion of vapor chamber fabrication to charging to reduce the contamination of the sample (within 24 hours), vacuuming time of vapor chamber (~12 hours), sample storage condition prior to charging (use of vacuum container), and wick sample cleaning process prior to nanoparticle coating (use of acetone, IPA, and DI water), and handling of nanoparticle coated wick sample (avoid any contact to the wick area, and clean the wick area only with DI water after the coating).

To investigate the effect of uncontrolled factors, two vapor chambers (sample 1 and sample 2) with similar geometric conditions are fabricated and tested. Prior to the test, sample 1 is charged with 51±0.1 mg of DI water, and sample 2 is charged with 52±0.1 mg of DI water. The devices are slightly over-charged (135% of wick void volume) to fill the extra volume in the pinched charging/vacuuming tubes and ensure complete saturation of the wick structure. The geometric conditions of the vapor chambers are measured by using micrometer with 0.001 mm resolution (Mitutoyo), and reported with its uncertainties in Table 5.2. The height of the pillar wick is measured with 3D optical profiler (Zeta Instrument).

Table 5.2 Geometric conditions of two vapor chambers with different pillar arrangement conditions.

	Condenser wall thickness (μm)	Vapor space (μm)	PCB thickness (μm)	Wick thickness (μm)
Sample 1	517 ± 30	405 ± 30	330 ± 2	50 ± 10
Sample 2	508 ± 30	412 ± 31	328 ± 2	50 ± 10

As shown in Figure 5.6, two vapor chambers show similar thermal resistance values, showing the maximum difference of ~6% over the heating power conditions. Conduction thermal resistance of the charged vapor chamber calculated from numerical model is also presented in Figure 5.6 to show the thermal resistance enhancement caused by evaporation. At low heating power condition, thermal resistance of both vapor chambers shows higher values than that of PCB with copper layer. However, the resistance decreases as the heating power increases, and starts to become lower than the thermal resistance of copper plated PCB at ~2.5 W. The samples show their minimum thermal resistance at maximum heating power used during each test. Minimum thermal resistance value of

sample 1 and sample 2 is ~25% and ~27% lower than the resistance value of copper plated PCB, which confirms the superior performance of vapor chamber over copper substrate.

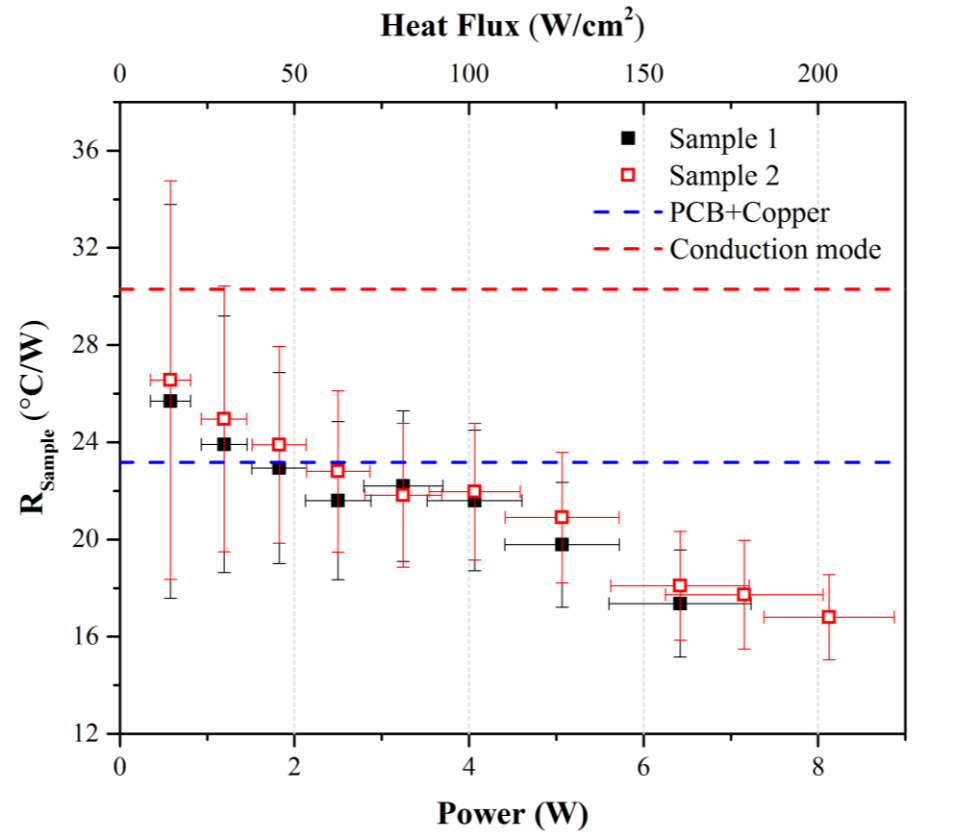


Figure 5.6 Thermal resistance of two vapor chambers (total thickness: ~1250 µm) with similar geometric conditions (Table 5.2) at different heating power/heat flux conditions. Thermal resistance of copper plated PCB (thickness:1250 µm) and conduction thermal resistance of charged vapor chamber obtained from numerical modeling are presented for comparison.

Figure 5.7 compares the thermal resistance of vapor chambers with micropillar wick structures (porosity:0.6) in different arrangements, square and rectangular arrangements, at different heating power conditions. The diameter of the pillars 50±5 µm, and the height is 50±10 µm. The pitch of square-packed pillar array is 70 µm, and the pitch of rectangular-packed pillar array is 82/60 µm. The devices with square-packed and

rectangular-packed vertically aligned pillars are charged with 52±0.1 mg and 51±0.1 mg of DI water, respectively. Table 5.3 summarizes the geometric conditions of two vapor chambers.

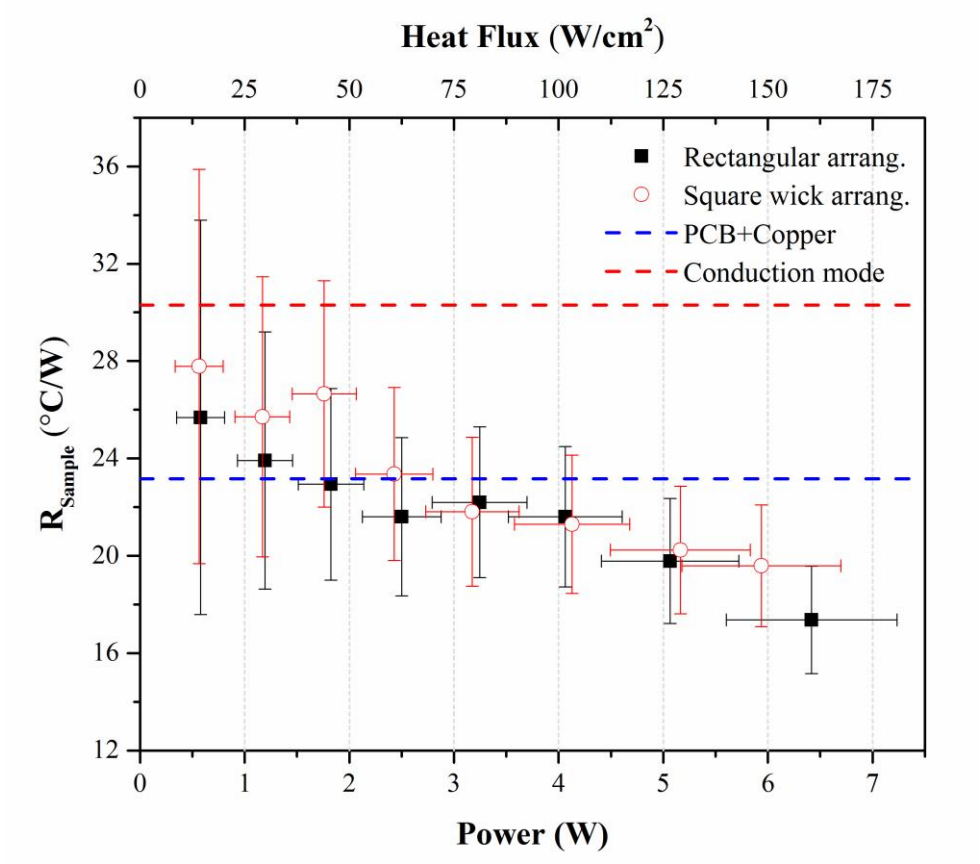


Figure 5.7 Thermal resistance of vapor chambers (total thickness: ~1250 µm) with micropillar wick structure in square and rectangular arrangement measured at different heating power/heat flux conditions. Thermal resistance of copper plated PCB with the same thickness (1250 µm) and conduction thermal resistance of charged vapor chamber obtained from numerical modeling are presented for comparison.

Table 5.3 Geometric conditions of two vapor chambers with different pillar arrangement conditions.

	Condenser wall thickness (μm)	Vapor space (μm)	PCB thickness (μm)	Wick thickness (μm)
Rectangular arrangement	517 ± 30	405 ± 30	330 ± 2	50 ± 10
Square arrangement	529 ± 33	386 ± 33	330 ± 2	50 ± 10

At low power conditions (< 2 W), the vapor chambers show higher thermal resistance values than copper plated PCB sample with the same thickness. The resistances then become lower than that of PCB and keeps decreasing until heating power conditions of ~6.5 W (170 W/cm^2) without showing any sign of dryout. The thermal resistance of each device reaches its minimum at maximum heating power condition used during the test, 6.4 W for the sample with rectangular-packed pillar array, and 5.9 W for the sample with square-packed pillar wicks. When compared to copper plated PCB, both prototypes of vapor chamber integrated PCB show about 15~25% enhanced thermal performance. Heat flux presented in Figure 5.7 is calculated by dividing heating power supplied to the sample by the area of the heater block tip (2 mm × 2 mm). However, it should be noted that due to the thin copper layer (20 μm) at the bottom of the PCB, heat is spread before being delivered to PCB, which may result in the larger heating surface than heater tip and consequently the lower heat flux than presented value.

Both vapor chambers show similar thermal performance over the test power condition, regardless of the pillar arrangement. Since the pillar arrangement affects more on the changes in maximum flow rate within the wick, the device with rectangular-packed pillars will have higher critical heat flux than the one with square-packed pillars. However,

the enhancement in critical heat flux does not necessarily lead to enhanced thermal resistance of the device. As both devices are charged with the same amount of water and have the same effective thermal resistance due to their identical wick porosity, thermal resistance of the devices is largely dependent on the area of the thin-film region. Thin-film region is the area formed along the extended meniscus near the three-phase contact line and has few microns length scale [40]. A previous modeling study has shown that more than 50% of the total heat transfer from the evaporating meniscus occurs in the thin-film region [75]. As intense evaporation occurs at this area, increasing the thin-film region can lead to decreased thermal resistance of device. To compare the area of thin-film region around the pillars in the two different arrangements, meniscus shapes are predicted by utilizing Surface Evolver.

Figure 5.8 presents meniscus shape within pillar array with square and rectangular arrangements. For comparison, both pillar wicks are assumed to be fully saturated with water. Since the width of thin-film region is defined variously in different studies [75],[76] a range of the thin-film thickness is defined in this study (0.05, 0.1, and 0.15 times of the pillar radius) [32] and utilized to calculate the area of thin-film region around the meniscus for pillar unit cell. The comparison shows that the thin-film area of the square-packed pillar is only 1~4% larger than that of rectangular-packed pillar, which can be considered as insignificant and justifies the results shown in Figure 5.6.

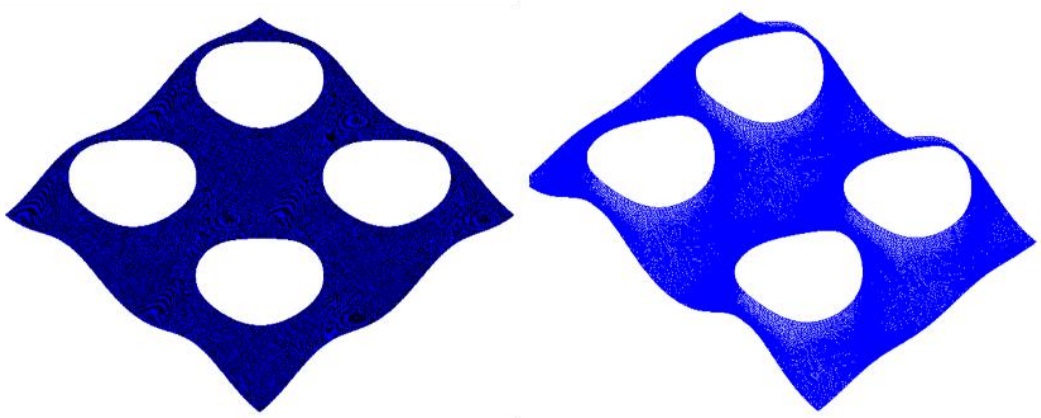


Figure 5.8 Meniscus shape of water within square-packed pillar array (left) and rectangular-packed pillar array (right) obtained from Surface Evolver.

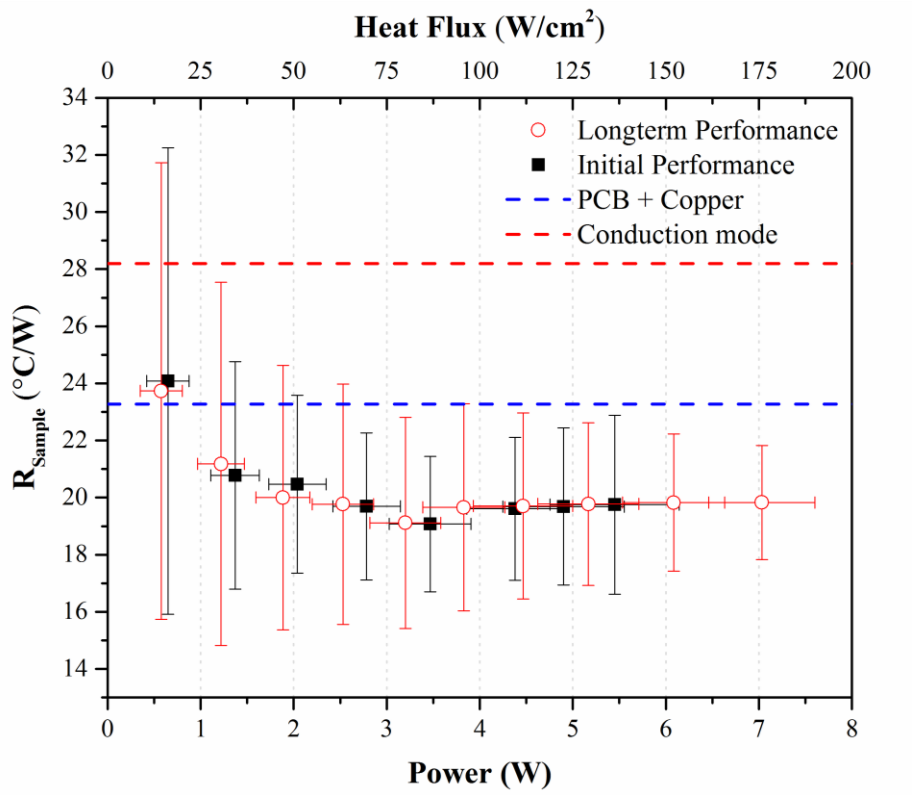


Figure 5.9 Thermal resistance of vapor chamber (total thickness: ~800 μm) measured within ~24 hours, and ~2,160 hours (3 months) after the completion of charging.

Thermal resistance of copper plated PCB (thickness: 800 μm) obtained from numerical modeling is presented for comparison.

Table 5.4 Geometric conditions of vapor chamber used for long-term performance.

	Condenser wall thickness (μm)	Vapor space (μm)	PCB thickness (μm)	Wick thickness (μm)
Vapor chamber	166 ± 12	367 ± 31	218 ± 2	50 ± 10

Ultra-thin vapor chamber with total thickness of 802 μm is fabricated, and tested for its long-term performance. To fabricate ultra-thin vapor chamber, thin condenser (thickness: 584 μm) and PCB (218 μm) is used while keeping the vapor space (367 μm) close to the other tested samples (~400 μm).

Figure 5.9 shows long-term thermal performance of ultra-thin vapor chamber sample by comparing its thermal resistance measured ~12 hours and ~2,160 hours after the completion of charging process. The thermal resistance of vapor chamber measured after ~2,160 hours shows almost identical value with the resistance from the initial measurement. The vapor chamber shows higher thermal resistance values than copper plated PCB sample with the same thickness at low power condition (< 1 W), but the resistances become lower than that of PCB at higher power conditions.

Although a long-term performance (up to ~2,160 hours) degradation is not observed in this study, some researchers have reported long-term performance degradation of their devices. Cai et al. [63] observed a performance degradation of silicon vapor chamber, and reported in their separate literature [77] that the reaction of Sn with water at elevated temperature or thermal cycling can generate NCG (hydrogen gas) which causes the degradation of device performance.

The change in the performance of silica nanoparticles (decrease in the contact angle between water and wick structure surfaces) may affect the long-term performance (> ~2,160 hours) of the device. Hydrophilic nature of silica nanoparticle not only enhances the capillary pressure of the wick but also increases the area of extended meniscus and the thin-film region by varying the surface area-to-volume ratio [78], which maximizes the rate of heat dissipation. However, if the wettability of the wick reduces, it may lead to increased thermal resistance of the device.

Galvanic corrosion can also cause performance degradation. Galvanic corrosion occurs when two or more metals come into contact in an electrolyte which provides a path for ion migration. Since there are joints that connect different metals (gold-SnAg solder-copper), galvanic corrosion may occur due to their different galvanic corrosion potentials and produce impurities in the cavity of vapor chamber.

CHAPTER 6. MODELING OF VAPOR CHAMBER INTEGRATED PCB

This chapter illustrates the development of CFD model for vapor chamber embedded PCB.

6.1 Prior Works on Modeling of Heat Pipes/Vapor Chambers

The primary difficulty in the analysis of the two-phase cooling devices is the strong coupling among the velocity, temperature and pressure fields at the interface of liquid and vapor. Extensive reviews of both heat pipe modeling and their applications have been reported [79],[80],[81]. Xiao and Faghri [82] developed a steady-state three-dimensional heat pipe model which accounted for heat conduction in the wall, fluid flow in the vapor chambers and porous wicks, and the coupled heat and mass transfer at the liquid/vapor interface. Aghvami and Faghri [83] developed an analytical thermal-fluid model to study steady-state performance of flat heat pipe in two dimensions with different heating and cooling configurations. Rice and Faghri [84] performed 2D analysis of heat pipe with no empirical correlations with single and multiple heat sources. Do et al. [85] developed a mathematical model to predict the thermal performance of a micro flat heat pipe with a rectangular-grooved wick structure. They considered the effects of liquid–vapor interfacial shear stress and contact angle on device performance. Li and Peterson [86] used a quasi 3D numerical model to study coupled heat and mass transfer problem in a flat evaporator of a loop heat pipe. Ranjan et al. [87] developed a transient flat heat pipe model which includes wick structure effects such as meniscus curvature, thin-film evaporation, and

Marangoni convection by integrating a microstructure-level evaporation model into device-level model. This study aims to numerically investigate the transient heat transfer, fluid flow and mass transfer in a prototype vapor chamber. The model is developed using CFD software FLUENT® with user-defined functions developed to calculate the evaporation/condensation mass flow rates, temperature and pressure at vapor-wick interface.

6.2 Governing Equations

The numerical model developed in this study is based on the approach from Vadakkan et al. [88]. The continuity equation for wick and vapor core is:

$$\varphi \frac{\partial \rho}{\partial t} + \nabla \cdot \left(\rho \vec{V} \right) = 0 \tag{48}$$

where φ is the porosity of the zone with $\varphi = 1$ in vapor core. The momentum equations in the wick and vapor core are:

$$\frac{\partial \rho u}{\partial t} + \nabla \cdot \left(\rho \vec{V} u \right) = -\frac{\partial \varphi p}{\partial t} + \nabla \cdot (\mu \nabla u) - \frac{\mu \varphi}{K} u - \frac{C_E \varphi}{K^{1/2}} \rho \left| \vec{V} \right| u \tag{49}$$

$$\frac{\partial \rho v}{\partial t} + \nabla \cdot \left(\rho \vec{V} v \right) = -\frac{\partial \varphi p}{\partial t} + \nabla \cdot (\mu \nabla v) - \frac{\mu \varphi}{K} v - \frac{C_E \varphi}{K^{1/2}} \rho \left| \vec{V} \right| v \tag{50}$$

$$\frac{\partial \rho w}{\partial t} + \nabla \cdot \left(\rho \vec{V} w \right) = -\frac{\partial \varphi p}{\partial t} + \nabla \cdot (\mu \nabla w) - \frac{\mu \varphi}{K} w - \frac{C_E \varphi}{K^{1/2}} \rho \left| \vec{V} \right| w \tag{51}$$

where K is the permeability of the zone. The energy equation in the wall, wick and vapor core is

$$\frac{\partial \left(\rho C \right)_m T}{\partial t} + \nabla \cdot \left[\left(\rho C \right)_l \vec{V} T_l \right] = \nabla \cdot (\mathrm{k}_{eff} \nabla T) \tag{52}$$

where $(\rho C)_m$ assumes different values in the wall, wick, and vapor core:

$$\begin{aligned} &\text{Wall: } (\rho C)_m = (\rho C)_s \\ &\text{Wick: } (\rho C)_m = (1-\varphi)(\rho C)_s + \varphi(\rho C)_l \\ &\text{Vapor core: } (\rho C)_m = (\rho C)_v \end{aligned} \tag{53}$$

The following boundary conditions are applied at wick-vapor interface:

1. Temperature:

$$-k_{eff} A_i \frac{\partial T}{\partial y} + m_i C_i T_i = -k_v A_i \frac{\partial T}{\partial y} + m_i C_i T_i + m_i h_{fg} \tag{54}$$

where negative m_i indicates evaporation while a positive value indicates condensation.

2. Pressure:

$$\frac{R}{h_{fg}} \ln(\frac{P_i}{P_0}) = \frac{1}{T_0} - \frac{1}{T_i} \tag{55}$$

3. Mass flux:

$$\left(\frac{2\hat{\sigma}}{2-\hat{\sigma}}\right)\left(\frac{A_i}{2\pi R}\right)^{1/2}\left(\frac{P_v}{(T_v)^{1/2}} - \frac{P_i}{(T_i)^{1/2}}\right) = \dot{m}_i \tag{56}$$

The following boundary conditions are applied at walls:

1. Wick-wall and vapor-wall interface:

$$u = 0,\ v = 0 \tag{57}$$

2. Top wall:

Condenser section:

$$-k_w \frac{\partial T}{\partial y} = h_c (T - T_c) \tag{58}$$

3. Bottom walls:

Evaporator section:

$$k_w \frac{\partial T}{\partial y} = q_e \tag{59}$$

Other sections:

$$u = v = \frac{\partial T}{\partial y} = 0 \tag{60}$$

4. Lateral walls:

$$u = v = \frac{\partial T}{\partial y} = 0 \tag{61}$$

6.3 Code Validation

Prior to model vapor chamber embedded PCB, developed code is validated against the results published in the literatures [88],[89].

6.3.1 2D model

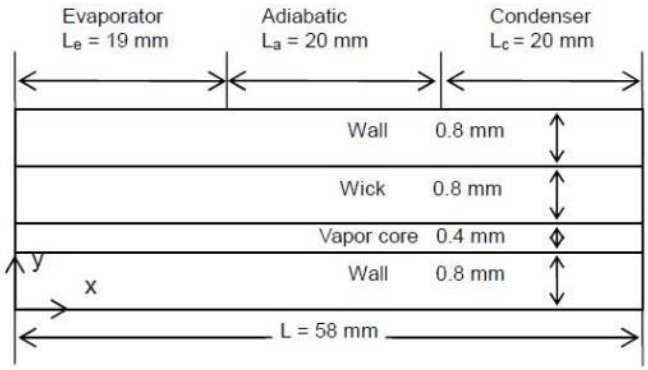


Figure 6.1 Computational domain of 2D model used for code validation. Image adapted from [84].

Figure 6.1 shows the computational domain of heat pipe 2D model used for developed code validation. In the model, the wick is present only on one side of the heat pipe, and the heating and cooling boundary conditions are applied at the outer wall only on the wicked side. Two heat inputs (10 W and 35 W) are used for comparison. Figure 6.2 compares transient variation of the axial wall temperature distribution for two heat input powers obtained from literature and developed code. It can be seen from the Figure 6.2 that the results from developed code agrees reasonably well with the results from the literature, showing the maximum difference of ~ 2 K.

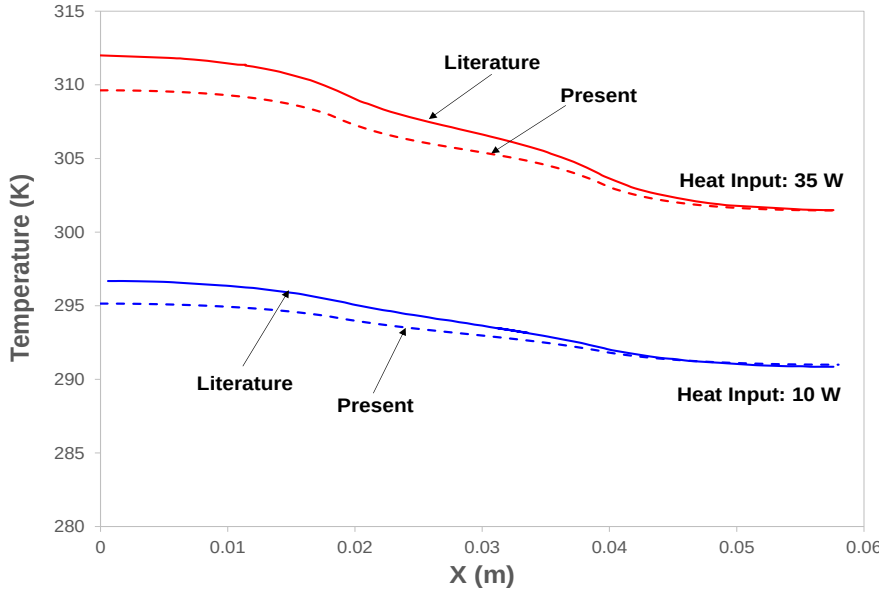


Figure 6.2 Axial wall temperature distribution in the heat pipe at different times (10 seconds and 30 seconds) for two input powers. The results from developed numerical model (FLUENT) is compared with the results from [88].

6.3.2 3D Model

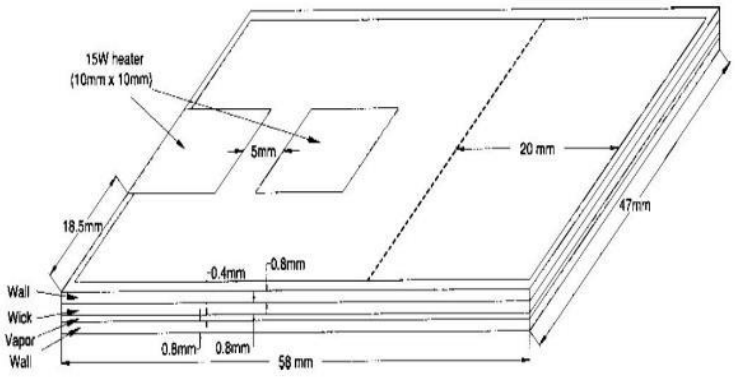


Figure 6.3 Computational domain of the flat heat pipe used for 3D model code validation. Image adapted from [89].

Figure 6.3 shows the computational domain of a flat heat pipe used for the validation. There are two discrete heat sources on the top surface of heat pipe. The heat inputs used for validation is 15 W-15 W. The condenser covers 20 mm of the heat pipe, and the area other than the heater and condenser is assumed adiabatic.

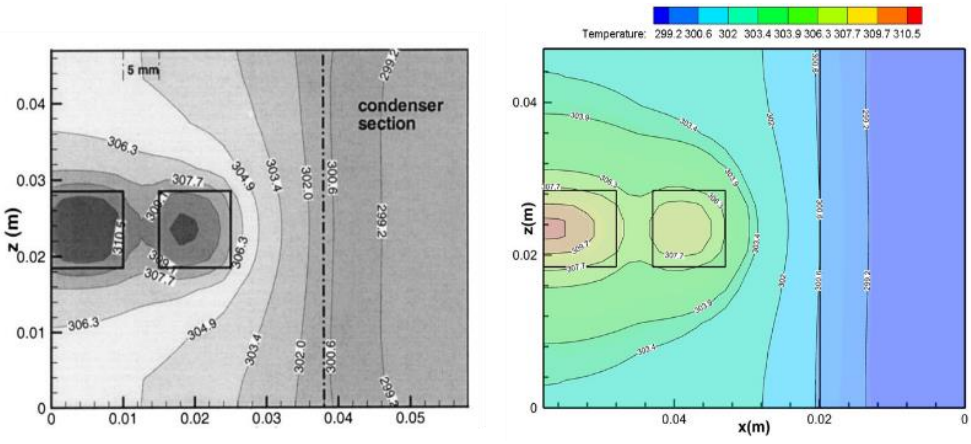


Figure 6.4 Temperature contours of heat pipe (top surface) for heat inputs of 15 W - 15 W. The result on the left is from [89], and the result on the right is from the code numerical model developed for current study.

As shown in Figure 6.4, temperature contour obtained from developed code agrees well with the results from the literature, showing the maximum difference of ~ 2 K.

6.4 3D Numerical Model of Vapor Chamber Embedded PCB

Using the validated code, 3D numerical model of vapor chamber embedded PCB is developed.

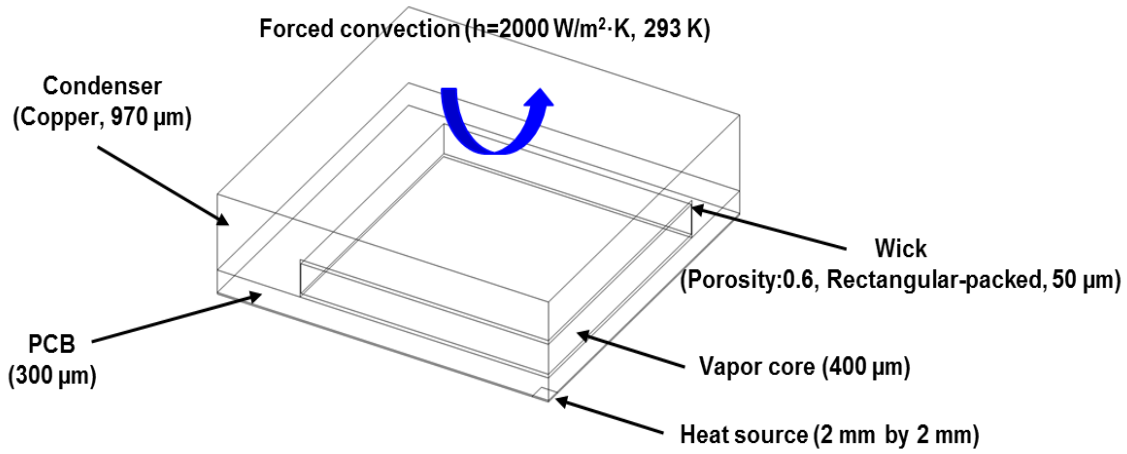


Figure 6.5 3D computation domain of prototype vapor chamber

Table 6.1 Detailed thermal properties of vapor chamber components

	PCB	Copper	Vapor	Water	Copper Wick
Thermal conductivity (W/m·K)	0.3	386	0.02	0.6	150
Density (kg/m^3)	1900	8978	0.01	1000	8978
Specific heat (J/kg·K)	1369	381	2014	4182	381
Viscosity (Pa·s)	–	–	1.34e-5	0.001	–

Permeability (m^2)	–	–	–	–	4.1×10^{-11}
Porosity	–	–	–	–	0.6
Latent heat (J/kg)	–	–	2473×10^3	2473×10^3	–

Figure 6.5 shows the computation domain of 3D vapor chamber model. The external dimensions are 40 mm × 40 mm × 1.3 mm, with a PCB thickness of 0.3 mm and a copper cover thickness of 0.97 mm. The bottom surface of PCB is clad with thin copper sheet (~20 μm). It also incorporates a 2 mm × 2 mm heater area at the center of bottom surface of PCB while the entire top surface of copper cover is the condenser area where convective boundary condition is applied to represent the effect of water cooling. Although the prototype vapor chamber does not have wick structures on condenser side, wick is assumed to cover all the surfaces of vapor space in current model to simulate condensate flowing back to evaporator as it has been reported that the presence of a wick structure on condenser does not affect the performance of vapor chamber significantly [26]. The wick has a thickness of 50 μm with a porosity of 0.6, and permeability of 4.1×10^{-11} m^2, which is a permeability of micropillar array in rectangular arrangement. All surfaces other than condenser and evaporator area are modeled as adiabatic walls. An input heat flux of 5 W (125 W/cm^2) is applied to evaporator region. The coolant water temperature and the heat transfer coefficient on the condenser are 298 K and 2000 $W/m^2\cdot K$, respectively. The initial temperature of vapor chamber is 298 K, and the wick is assumed to be fully saturated. Table 6.1 summarizes the thermal properties of the vapor chamber components and the working fluid.

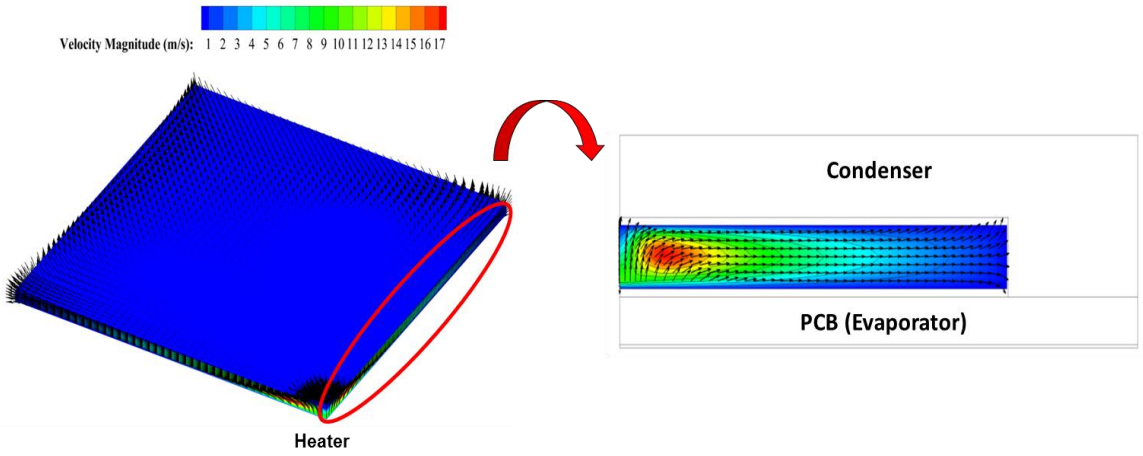


Figure 6.6 Steady-state velocity contour and vector of vapor in vapor core.

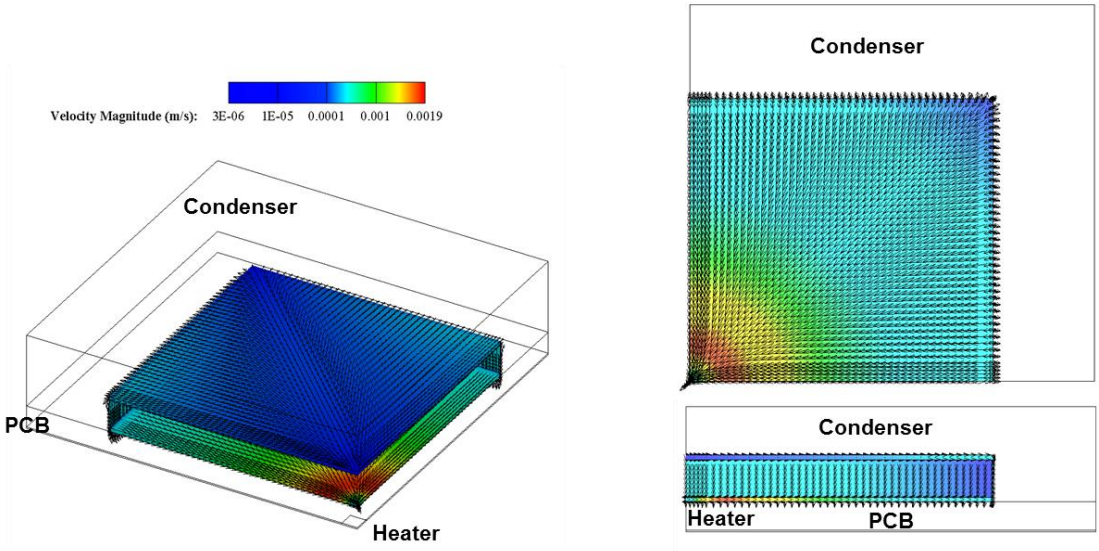


Figure 6.7 Steady-state liquid (Water) flow velocity contour and vector in wick structure.

Figure 6.6 and 6.7 show the steady-state velocity vectors of vapor in the vapor space and water in the wick structure of vapor chamber. Note that the length of the velocity vectors does not represent the magnitude of the vector and drawn to be uniform. The maximum velocity of vapor is ~17 m/s (Mach number: 0.05), and hence satisfies the assumption of incompressibility. Liquid velocity shows maximum value near the heated

region due to mass addition to the vapor caused by the evaporation of liquid in the wick structure. The velocity of vapor decreases near the condenser side due to the mass depletion of vapor caused by condensation. Average liquid velocity is much smaller than the average vapor velocity, showing 10^4 smaller maximum velocity. The difference is mainly caused by the large difference in density between vapor and liquid. Liquid in evaporator flows toward the heated area, and gets accelerated as it reaches closer to the heated area. Liquid in condenser moves away from the heated area and flows back to the evaporator wick through wick structure on the side walls.

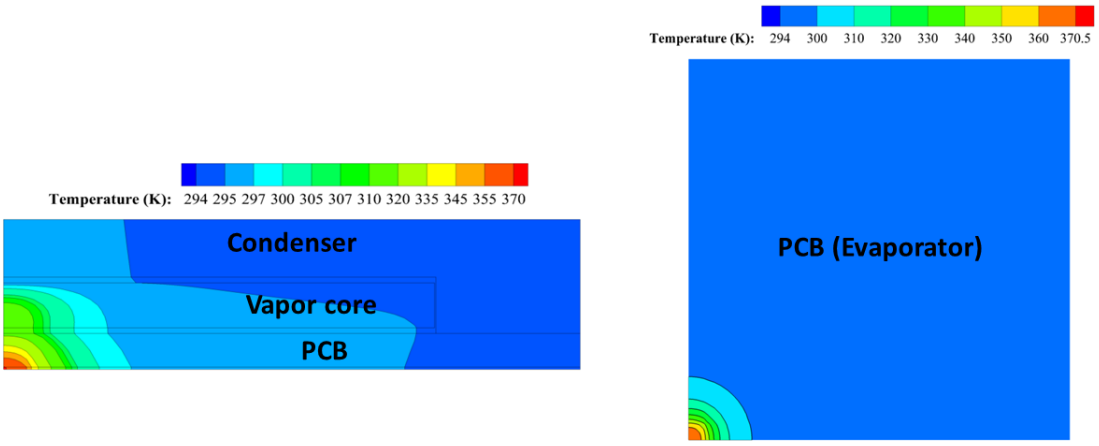


Figure 6.8 Steady-state temperature profile (K) at the mid plane (left) and evaporator (right) of the vapor chamber with 5 W heat input.

Figure 6.8 shows steady-state temperature distribution at the mid plane and the bottom surface (evaporator) of vapor chamber with 5 W of heat input. Wall temperature of the vapor chamber is the highest at the center of evaporator region. A large temperature drop of ~ 50 °C along the vertical direction from the bottom of PCB to vapor core can be observed due to the low thermal conductivity of PCB. Temperature distribution in the evaporator along the horizontal direction also shows a large temperature drop. Condenser

side temperature is more uniform than evaporator, and shows the highest temperature at the center area of the wick. The maximum temperature difference at condenser region is ~3 K.

Using the maximum temperature at evaporator, heat input and the average temperature of condenser, thermal resistance of the device is calculated to be ~29 K/W. This is slightly higher (~20%) that measured value ~24 K/W. The reason for the discrepancy is that current model does not capture microstructure effect on the thermal performance of vapor chamber. Prior study on the effect of microstructure on thermal performance of vapor chamber showed that depending on the accommodation coefficient used for the simulation, neglecting the effect of microstructure can overestimate the temperature drop between evaporator and the condenser up to ~16%. Copper structural support is not modeled in this simulation study, and this can also affect the result. More comparison studies between test and modeling at different heating power conditions are needed to develop more reliable and robust vapor chamber model.

CHAPTER 7. CONCLUSIONS AND RECOMMENDATIONS

This research focuses on addressing fundamental challenges of glass interposers associated with low thermal conductivity of glass by: 1) increasing the effective thermal conductivity of the substrate by incorporating copper structures to provide an enhanced thermal path within the package, and 2) developing thin two-phase heat spreaders integrated in packaging substrate which can spread the heat better than copper plated packaging substrate with identical thickness.

From numerical modeling study on interposers, it was found that the implementation of copper TPVs in glass interposers and copper ground layers in PCBs enhances thermal performance of interposers as interconnects and TPVs perform as thermal, as well as electrical paths. Increasing the number of interconnects and TPVs by decreasing their pitch further improves thermal performance of glass interposers due to the increased effective out-of-plane thermal conductivity of interconnect and TPV layers. However, it is shown that glass interposer's out-of-plane thermal resistance became no longer significant for effective thermal conductivity higher than 100 W/m·K. Further improvement in thermal performance can be achieved through the implementation of vapor chamber in PCB. Glass and silicon interposers showed almost identical performance with vapor chamber, overcoming the low thermal conductivity of glass.

Hydraulic performance test was conducted to determine the design of micropillar wick structure for vapor chamber. From forced liquid flow test, the permeability of micropillar array in rectangular arrangement was found to be larger than the pillars in other arrangements at the same porosity. By changing horizontal and vertical spacing between

the pillars in rectangular arrangement, the permeability can be further enhanced while maintaining the porosity, but manufacturability will limit the configuration. Measured permeability values were compared with existing 2D permeability models, combined with flat plate permeability model. The models estimated permeability of the samples with square and hexagonal arrangements reasonably well. The analytical model considered in this study, however, showed large deviation (~48%) from the numerical model for pillars in rectangular arrangements. The permeability predicted using meniscus shape showed a smaller value compared with the flat meniscus model, and the difference became larger at higher porosity. The capillary pressure of pillar arrays was measured using capillary rate-of-rise test. The test results showed capillary pressure's strong dependency on the porosity regardless of the type of arrangement. For this reason, micropillars in rectangular arrangement showed the highest capillary performance parameter due to their higher permeability, compared to other pillar arrangements with the same porosity. The capillary rate-of-rise test results showed that the gravity effect in capillary rise is more prominent in samples with high porosity (0.7~0.8) than low porosity (0.45~0.6). By comparing the ratio of capillary pressure to gravity force between the samples, this study found that application of Washburn's equation to get capillary performance parameter from fitting can be limited when using the samples with high porosities, where the ratio of capillary pressure to gravity force becomes larger than 4.

Finally, a prototype of packaging substrate integrated with vapor chamber was fabricated. Micropillar array was incorporated in the vapor chamber as a wick structure. From the thermal performance tests, it was found that the use of vapor chamber integrated PCB can be justified at heat input condition > 2 W since the vapor chamber showed high

thermal resistance at lower heating power conditions. Among different pillar arrangement designs, the rectangular-packed pillar array may lead to the highest critical heat flux of the device. However, the effect of wick arrangement on thermal resistance of vapor chamber was not significant. Ultra-thin (~800 μm) vapor chamber sample was fabricated which showed consistent thermal performance, confirmed by the test result measured ~2,160 hours after the initial performance test.

7.1 Key Contributions

In this study, a computationally efficient and experimentally validated thermal model of copper TPVs in glass substrate was developed. Detailed analysis was performed for the effect of different copper structures on the thermal performance of glass and silicon interposers, which provides a guideline for thermal design of the interposers.

Additionally, this work has described the concept of ultra-thin package substrate integrated with vapor chamber. A complete fabrication process flow of the device was successfully established, and its superior performance over the PCB with thick copper layer was demonstrated through fabrication and thermal tests. To enhance the performance of the device, silica nanoparticles were coated on micropillar wick structure, and the effect of different pillar arrangements (square, hexagonal, and rectangular) on the hydraulic performance of the wick structure was studied. The results from the pillar arrangement study provide a practical design guideline for micropillar wick structure, where only square and hexagonal arrangements have been considered for the application. Although the prototype has been tested with single heat source, the PCB can have multiple electronic components or heat sources, which enables the thermal management of multiple heat sources.

Lastly, 3D transient CFD/heat transfer model for vapor chamber integrated package substrate was successfully developed. The model can be utilized to study the effect of various design factors on device performance through parametric study.

7.2 Recommendations for Future Works

Significant research work on the fundamental study to improve the performance and reliability of vapor chamber integrated PCB can be accomplished.

7.2.1 The effect of nanoparticle coating

In the current study, the wettability of wick structure is enhanced by coating 7 bilayers of silica nanoparticles using layer by layer technique. However, the wicking performance may be further improved with additional number of coating. Conducting hydraulic performance tests on the wick samples with different number of coated layers may be useful to find the optimized number of layers. Since nanostructures can affect the area of thin-film region, which directly relates to the thermal resistance of the device, separate thermal performance test may be required. Long-term performance of nanoparticle coating also needs to be tested to ensure device's reliable performance.

7.2.2 Condenser design for vapor chamber performance improvement

While current study only focuses on the design of wick structures on evaporator, condenser side design still has a room to improve. For example, the effect of the existence of wick structures on the performance of the device, or the wettability effect on the performance of the device can be studied. However, modifying surface wetting characteristic usually involves chemical treatment, which is often complicated and

expensive process. One of the easy and cheap way to modify wetting characteristic of the surface is using Teflon coated tape. Since Teflon is well-known for its hydrophobicity, attaching thin Teflon tape can change the wetting characteristics of condenser surface. Furthermore, the contact angle of Teflon surface can be modified by mechanical abrasion (sand paper) which can be used to study the effect of condenser wettability on the device performance.

7.2.3 Liquid chamber

Ultra-thin liquid chamber is another two-phase cooling device that can be integrated with packaging substrate. It can be fabricated by utilizing the fabrication techniques presented in this thesis. Liquid chamber, which utilizes boiling of liquid instead of evaporation of liquid, does not require wick structure for capillary pumping, and has a simpler fabrication steps compared to vapor chamber. Moreover, the performance of liquid chamber will not be limited by capillary performance of the wick. However, surface modification may be needed on evaporator to promote the nucleate boiling.

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