BATTERY-SOURCED SWITCHED-INDUCTOR MULTIPLE-OUTPUT CMOS POWER-SUPPLY SYSTEMS

A Dissertation
Presented to
The Academic Faculty

by

Carlos J. Solis

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
May 2018

BATTERY-SOURCED SWITCHED-INDUCTOR MULTIPLE-OUTPUT CMOS POWER-SUPPLY SYSTEMS

Approved by:

Dr. Gabriel A. Rincón-Mora
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. John D. Cressler
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Maysam Ghovanloo
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Sung Ha Kang
School of Mathematics
Georgia Institute of Technology

Dr. Thomas G. Habetler
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: April 3, 2018

ACKNOWLEDGEMENTS

I would like to first thank my advisor, Dr. Gabriel Alfonso Rincón-Mora, whose drive and passion for excellence, technical guidance, and advise made this research possible.

Also, I want to thank my proposal and committee members, Dr. Maysam Ghovanloo, Dr. Thomas G. Habetler, Dr. John D. Cressler, and Dr. Sung Ha Kang for their invaluable technical feedback and support for my research.

I am tremendously grateful to Bryan Legates, Tony Bonte, JD Morris, and Analog Devices, Inc. for their technical and financial support for this research.

I am also very thankful for my colleagues at the Georgia Institute of Technology, Andres Blanco, Rajiv Damodaran Prahba, Orlando Lazaro, Karl Peterson, Luke Milner, Dongwon Kwon, Suhwan Kim, Joshua Cowan, Jun-Yang Lei, Kowshik Murali, Amy C Wilson, Nan Xing, Siyu Yang, and Devon Janke, for the priceless technical discussions, guidance, and their support through this journey.

A very special thanks to family and friends especially to my parents, Lydia E. Ramírez-Santiago and Carlos D. Solis-Orria, for their unconditional support and encouragement.

Finally, I am extremely grateful for my loving wife, Ivonne M. Matos-Guerra, without whose endless love, support, sacrifice and encouragement none of this journey would had been possible.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Portable electronics such as wireless microsystems incorporate functions such as sensing, data processing, and transreceiver that allows adding intelligence, improve use of resources and even saves lives. These systems are powered by tiny batteries to achieve a small overall solution to reduce costs and allow a large deployment of microsystems. These various functionalities in these systems require different supply levels optimized for their respectively technology used and performance requirements. Moreover, as battery depletes and for transmitting signals with enough power over large distances, regulating a boosted supply from the battery becomes necessary. In addition, the voltage levels can be dynamic to optimize for the instantaneous workload of the function and the system might duty cycle blocks when not in use to conserve energy. These system designs impose stricter requirements on the power-supply system on board since it must quickly react to load dumps and changes in supply levels in a compact and cheap solution. The incorporated tiny battery exacerbates the challenges as power losses must be minimized to prevent a costly battery replacement.

The objective of this research is to investigate, develop, test and evaluate a compact and efficiency power converter capable of regulating buck and boost voltages while quickly responding to load dumps. Among power converter topologies, switched-inductor converters achieve the highest efficiency across operating conditions. However, inductors are bulky and difficult to integrate and therefore limiting the power converter to a single inductor while regulating multiple outputs balances size and efficiency. The fundamental challenge is in the operation and sharing of the single inductor to generate buck and boost voltages, increase regulation bandwidth and reduce cross-regulation between outputs.

Literature commonly uses the well-understood PWM to accurately regulate multiple supplies in a SIMO; however, its takes multiple switching cycles to respond and correct the output after a load dump. Luckily, hysteretic current-mode control achieves good dynamic performance but literature has not analyzed its stability and applied it to SIMO converters. A fully hysteretic control for SIMO achieves a fast response closest to the fast but inefficient linear regulators.

A boosted output from a buck power stage is possible without changing operation. Fundamentally, as long inductor energizes through buck outputs, it can energize through any buck and boost outputs without changing operation. However, a limited quantity power can be boosted, and therefore an auxiliary switch is proposed when a higher boosted power must be delivered. Although hysteretic control has good dynamic response, it is noise sensitive as it regulates instantaneous signal. Therefore, a novel PWM−hysteretic hybrid control is proposed for applications that have stricter noise requirements that balances the good dynamic performance of hysteretic control with accuracy of a PWM control.

This dissertation starts by discussion motivation, and benefits and challenges of switched-inductor converters in Chapter 1. Chapter 2 reviews the literature and discusses the state-of-the-art control and operation of single-inductor multiple-output (SIMO) converters with their benefits and disadvantages for portable electronics. Chapter 3 analyses the stability and discusses the design of hysteretic current-mode control for single-output converter at first; and then expand it for SIMOs. Chapter 4 presents the proposed fully hysteretic control for SIMOs that achieves a fast response time while having a low silicon real state per output. Chapter 5 elaborates on how to generate a boosted output from a buck power stage without altering its operation under certain restrictions. Therefore, this

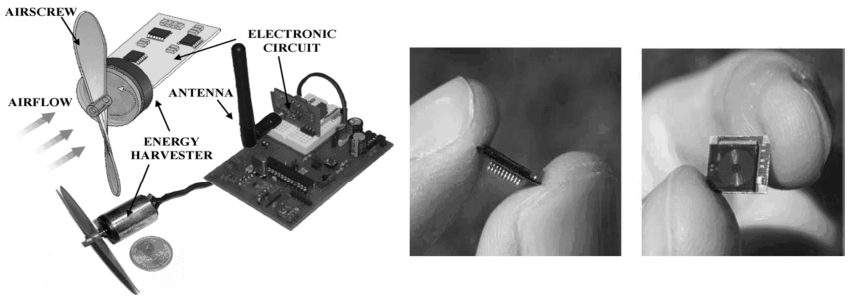
allows to conserve the efficiency by avoiding using a buck-boot power stage operation unless necessary. Chapter 6 discusses the noise sensitivity challenge of the hysteretic control and then proposes a hybrid PWM−hysteretic control that balances response time while having lower noise sensitivity. Finally, Chapter 7 summarizes the resulting contributions of this research along with the technical challenges and future research directions.

CHAPTER 1

POWERING MULTIFUNCTIONAL MICROSYSTEMS

1.1 Emerging Applications

Current trends in portable electronics increases the integrated functionalities and capabilities in products such as laptops, tablets, phones, and networked microsystems. Specifically, networked (or wireless) microsystems can sense, process, store, transmit, and receive information in hospitals, factories, farms, and homes and can save lives, energy, and money [1−9]. As an example, Figure 1.1 (a) shows an air quality monitor for industrial applications by sensing temperature and velocity [3]. Also, Figure 1.1 (b) shows an implantable wireless neural recorder that circumvent limitations of wired versions during brain studies [4]. These wireless microsystems have the advantage on reaching tough places like the inside of walls or the human body for monitoring and reporting. Therefore, it is imperative for microsystems to be as small as possible to be non-intrusive and avoid frequent, if any, battery replacement by extending battery life.



(a) (b)

Figure 1.1. Wireless microsystem examples: (a) air temperature and velocity monitor for industrial applications [3] © 2010 IEEE and (b) implantable neural recorder for biomedical applications [4] © 2009 IEEE.

These microsystems generally have three main functionalities: sensing, data processing, and communication. Sensing has an analog interface to the real world and commonly an analog-to-digital converter (ADC) for a digital-signal processor (DSP) to process the information. These can be implemented in a low-cost CMOS technology and either on the same or separate dies. Finally, wireless communication for these microsystems requires a power amplifier (PA) which can output enough power to communicate over the required distance required.

Unfortunately, higher cost technologies, such as GaAs and InP, implement the PA to transmit high enough power at fast communication speeds [10]. These technologies achieve high performance in a PA because they can tolerate higher voltages in the range of 4–5 V [11]. These high voltages reduces current levels during transmission and therefore losses [12], while maintaining high mobility in transistors for higher bandwidth. In the other hand, DSPs are low voltage and noise tolerant, so noisy 0.5–1-V power supplies can drive them to conserve energy [13–14]. Sensors and ADCs, on the other hand, usually require higher supplies with lower noise content to keep a high signal to noise ratio [15]. Efficient power-supply systems, like Figure 1.2 illustrates, must therefore supply and regulate several outputs for all these functions [16–17].

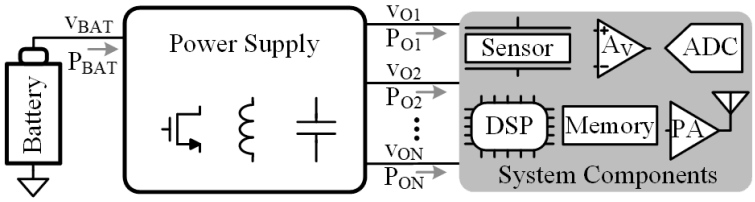


Figure 1.2. Power management for wireless microsystems.

A battery provides energy and portability for these systems but different chemistries provide a wide range of voltages to regulate from. Also, as the battery drains and its state of charge changes, so is their voltage. For example, a high energy-density chemistry as lithium-ion batteries can have a voltage between 2.7−4.2 V depending of its state of charge [18]. This would require the power supply to boost a voltage for the PA to use, while regulating a supply lower than the battery voltage for the other functions. Hence, the power supply must supply a mix of buck (step-down) and boost (step-up) voltages.

The overall size of these networked microsystems need to be compact and non-intrusive, and thus battery is often small with limited energy storage which makes battery lifetime becomes a challenge. In despite work to harvest ambient energy to extend battery lifetime [19−22], ambient energy is limited or often not continuously abundant; therefore, an efficient power converter is imperative to preserve energy regardless if the system harvests ambient energy. Plus, tiny batteries cannot sustain power for long, so even though DSPs, ADCs, and power amplifiers (PAs) can tolerate higher voltages, they (for the sake of saving energy) should not as long as they meet performance requirements [23].

1.2 Power Management Requirements

To conserve the limited energy in wireless microsystems, there exists two main approaches at the system level: block duty-cycling and dynamic voltage scaling (DVS). Block duty-cycling turns off or idle blocks when they are unnecessary for the proper operation of the system [24−26]. For instance, while the system waits for an external trigger, the digital processing and communication blocks can be turned off, until they are necessary to process and transfer data like Figure 1.3 shows. On the other hand, DVS minimizes the power

consumption without sacrificing required throughput by adjusting supply voltage [27−29]. Figure 1.3 displays voltage scaling on the digital signal processor power profile P_{DSP} that during heavy processing it has the highest supply voltage and decreases when the computation demand reduces. Moreover, process variation can affect the optimal supply power efficient throughput such as in multi-core applications [14], [30]. Hence a higher supply granularity provides more flexibility for a more efficient system as long as the performance degradation does not overwhelms energy loss reduction given the added complexity [31].

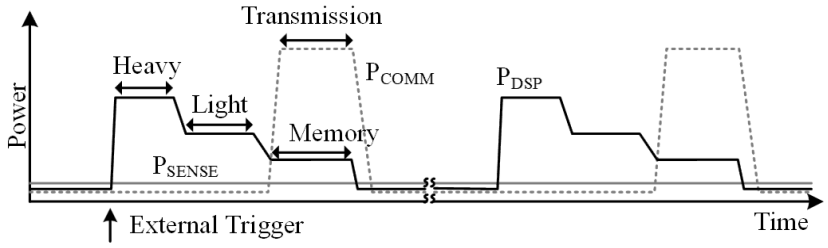


Figure 1.3. Sample power profile of their function in a wireless microsystem.

These system-level energy-savings techniques imposes tougher efficiency and accuracy requirements on the power supply. Since the maximum to idle power consumption ratio can be large, the converter must be efficient across the wide load range. Otherwise, battery can excessively discharge during short operation at maximum capacity or long idling (or standby) periods. Thus, the converter must have high power conversion efficiency across a wide output load range. This means that besides a power converter having a high peak conversion efficiency $\eta_{C(PK)}$, it should also have a high average efficiency $\eta_{C(AVG)}$ across the power range, or a high full-load efficiency $\eta_{C(FL)}$ depending on the most likely power profile for a given application.

Regulation accuracy become more constrained since either block-duty cycle or DVS also requires the converter to quickly provide energy demanded to the corresponding function. When waking up from an idling state, for instance, latency reduces efficient use of energy resources and functions as they wait for the supply to settle [32]. Moreover, the supply regulator should follow the optimum target, under DVS operation, to minimize losses as long as energy savings outweighs losses from increasing tracking speed [33]. Hence, each output of the power converter needs a high bandwidth to handle fast full-load transients while maintaining a high efficiency across a wide range of loads.

1.3 Power Supplies

Potential power converters topologies include non-switching options such as linear regulator that is a simple linear system and produces negligible noise. Another set of option are switching topologies like the switched-capacitor and switched-inductor variations, although noisy they are more efficient. Each has their own advantages and disadvantages that must be weighted in for each microsystems application.

1.3.1 Linear Regulators

A linear regulator consist of a pass transistor M_P which resistance is modulated to regulate the output voltage to the target like Figure 1.4 depicts. Deploying dedicated linear regulators to each block is a compact solution and can accurately regulate at a high bandwidth [34–35]. Also, since linear regulators is a linear system, they tend to have a simpler design and stabilization for high bandwidth contrary to switching converters.

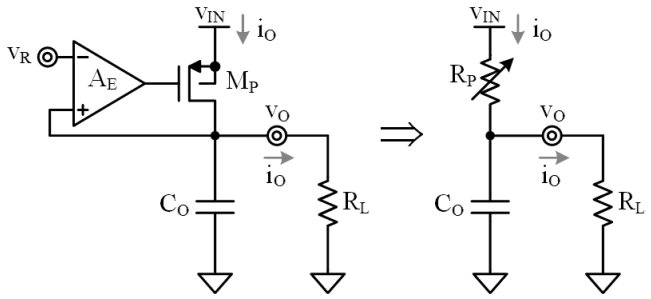


Figure 1.4. Linear regulator for regulating a supply.

Unfortunately, linear regulators tend to be lossy since the modulated resistance R_P absorbs considerable ohmic losses by sitting across input voltage v_{IN} and output voltage v_O. Its conversion efficiency $\eta_{C(LR)}$ depends linearly on the output power P_O or $v_O i_O$ divided by the input power P_{IN}. Since all output current i_O flows through the pass transistor M_P and originates at v_{IN}, P_{IN} depends on output load i_O. In addition, quiescent power P_Q from the control also comes from the input supply v_{IN}. In the ideal case where there is no quiescent power P_Q, $\eta_{C(LR)}$ is theoretically limited by the output voltage v_O to input voltage v_{IN} ratio:

$$\eta_{C(LR)} = \frac{P_O}{P_{IN}} = \frac{v_O i_O}{v_{IN}\left(i_O + i_Q\right)} < \frac{v_O}{v_{IN}}. \tag{1.1}$$

For applications where input to output voltage spread is large, their low efficiency will shorten battery life as operating condition changes. In addition, linear regulators can only regulate voltages below the battery voltage, or in other words, can only buck. These drawbacks limit their use among applications requiring high efficiency and at least one boosted supply such as in wireless microsystems.

1.3.2 Switched-Capacitor Converters

Switching converters incorporate switches with low voltage across when closed to reduce conduction losses. Therefore, switched capacitor supplies have higher efficiency than

linear regulators and although they occupy a larger silicon real estate than linear regulators, they can be fully integrated [36–37]. Switched capacitors can either buck or boost supplies depending how its flying capacitor is charge and discharged. For instance, Figure 1.5 depicts a series to parallel sequence that downconverters a supply from the input.

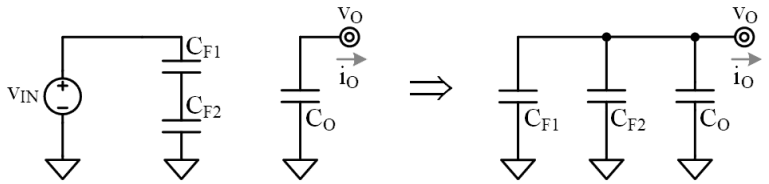


Figure 1.5. Sample switched-capacitor converter with a series to parallel sequence.

For every state in the sequence, the converter will charge each capacitance to a certain voltage as a function of the input and output voltages. This means that every switching sequence has an associated voltage gain, e.g. Figure 1.5 has a voltage input-to-output translation of 0.5 V/V. The converter regulates the output by replenishing the flying capacitor(s), C_{F1} and C_{F2} in Figure 1.5, and the output capacitor more frequently or reconfiguring gain stages in between cycles [38]. As load increases, so is ripple voltage and thus the charge to be replenished on the capacitors. This will slightly increase the voltage across switches during charge redistribution because capacitor's voltages will be farther apart, hence increasing losses.

When the power-stage gain does not match input to output voltage vo, irrespective of load level, the converter regulates by allowing more ripple voltage. This decreases efficiency as the required voltage conversion mismatches the power stage gain [38–39]. Therefore, efficiency will be dependent on the output to input voltage although to a much lesser degree than linear regulators. Topologies with modifiable gain stages moderately increase efficiency at the expense of design complexity and more switches [38]. Also,

integrated switched capacitors have an additional loss due to their bottom plate capacitance, which further degrades the efficiency unless expensive technologies or manufacturing steps are used such as deep trench capacitors [40−42].

1.3.3 Switched-Inductor Converters

Switched-inductor converters adjust the inductor current to satisfy the output demand and replenish the output capacitor. It does so by switching the voltage across the inductor in alternating cycles by engaging and disengaging switches. The voltage across engaged switches can be minimum unlike a switched-capacitor converter, hence switched-inductor converter can achieve a higher efficiency among the power topologies considered for a wider range of operating conditions such as input and output voltages, and load currents. The switched-inductor converter can either buck or boost depending in the switch configuration like in Figure 1.6.

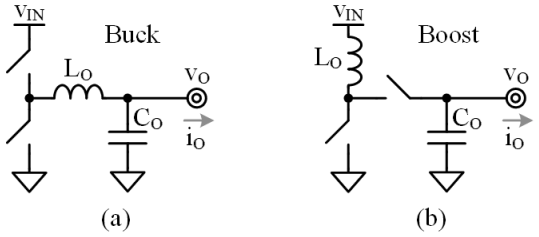


Figure 1.6. Switch-inductor converters in the buck (a) and boost (b) configuration.

The switched-inductor converter is the most suitable power topology for power management in a wireless microsystem. Minimizing losses is imperative when operating from a tiny battery with a wide range of battery voltage and regulation voltages which switched-inductors can provide. However, as Figure 1.6 shows, it requires two passives which present some challenges due to the required compactness on the overall system

specially if multiple regulated supplies are required in microsystem applications or portable electronics in general.

1.4 Challenges

Although switched-inductor converters provide high efficiency, they have integration challenges. Since they require at least two passives, i.e. a capacitor and inductor, it is difficult to integrate both on the same die at a reasonable cost. Also, generating a multiple-output solution based in a switched-inductor converter add more technical challenges to be addressed such as the optimum way to share the inductor.

1.4.1 Miniaturization

Unfortunately, integration of a switched-inductor converter is challenging. Research has been conducted to integrate the passives, i.e. inductor and capacitor, in the same integrated circuit (IC). Figure 1.7 summarizes state of the art switching converter using the literature survey reported in [43]. There are 4 main categories of integration: product modules (PCB), system-in-package (SiP), and system-on-chip (SoC) solutions. Products modules tend to have a lower power density because they require external passives. Increasing the switching frequency decreases the size of the required passives until the point they are possible to co-package in a SiP solution and hence, more power density. There is active research as well as products in a SiP solution (or SiPP), like in Figure 1.7 (b), that shows performance close to product modules. However, increasing switching frequency beyond 10 MHz allows passives to be small enough to be integrated in the same die in a SoC design and ultimately improving power density; however, it is at the expense of higher switching

losses. The efficiency drop can be in the order of 10−30% due to the increased switching-related losses of switches and quiescent power [44−46].

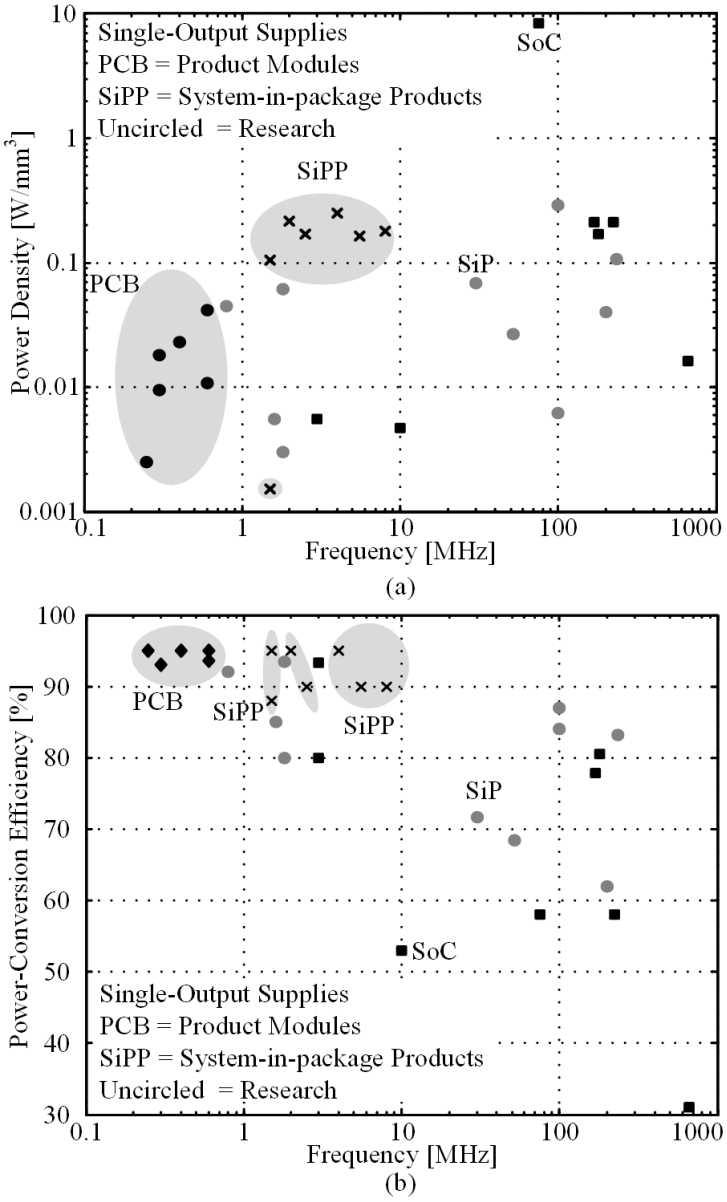


Figure 1.7. Power density of single-output supplies as a function of frequency [43].

On the passive integration, the inductor is the most challenging element to integrate [47−49]. Figure 1.8 shows a summary of state-of-the-art inductors, compiled from data surveyed at [43], which shows quality, or inductance per resistance, versus energy density

for a given volume and saturation current. Inductors with no magnetic materials, such as air-core [44] or spiral-shaped inductors, tend to have low energy density and quality due to the low permeability of air. Inductor with magnetic materials, on the other hand, can store more energy per length, hence better quality due to lower series parasitic resistance. The magnetic material increases the magnetic flux the inductance can store for a given current flowing through because of a higher permeability [50]. However, this magnetics materials are not readily available in all processes and can increase manufacturing fabrication steps and challenges [51]. Because external inductors have better quality and large energy density by more than an order of magnitude compared to the state of the art, this research will concentrate on solving the generation of multiple supplies in a lower cost and size without adding the challenges of an integrated inductor. However, inductor integration should ultimately be part of the solution in the future.

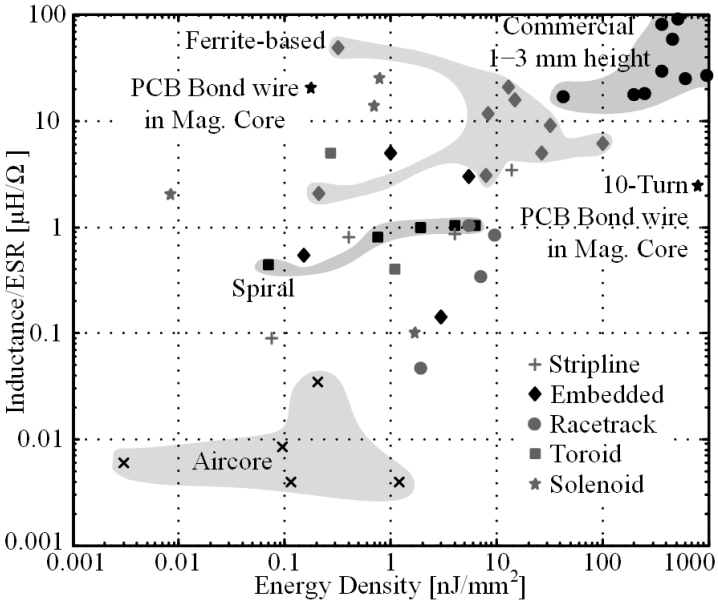


Figure 1.8. Quality vs energy density for integrated and external inductor [43].

1.4.2 Multiple Outputs

A simple alternative to efficiently generate various regulated supplies from a battery or unregulated supply is to dedicate a whole switched-inductor converter for each. In despite of being an efficient option, using multiple inductors increase the size of the solution as well as the cost. Therefore, generating multiple supplies using a single inductor balances efficiency and size (and cost) [52].

A single-inductor multiple-output converter (SIMO) will present its own set of technical and design challenges. Most of them stem from the fact that the inductor is shared among the outputs in alternating cycles and the increased complexity of the design. The principal challenges are:

1. Insightful stability analysis
2. Accuracy of individual outputs
3. Output cross-regulation
4. Efficient buck-boost supplies

1.4.2.1 Insightful Stability Analysis

The switching nature of SIMOs makes them a non-linear system which complicates the analysis and design to ensure a fast and stable converter. Despite work to simplify design and analysis for the single-output switching converters, analysis for the SIMO is seldom. The multiple regulating loops in SIMOs complicates the analysis as they can interact and affect others. This adds complexity in the design because heavy simulations or math-intensive approaches are needed to ensure stability.

1.4.2.2 Accuracy

While in a single output switched-inductor buck converter the output will continuously receive energy, it will be duty-cycle irrespective if it is a buck or boosted output in a SIMO. In other words, a SIMO replenishes each output for less time and less often and it has an inherent increased delay when responding to load transients/dumps. This increases output voltage deviations from the target because the output capacitor must provide all the energy for a fraction of the switching period. Therefore, accuracy will degrade as compared to the single-output counterpart by increasing voltage ripple and voltage deviations from load dumps.

1.4.2.3 Cross Regulation

Another challenge with SIMOs is that a change in one output's energy needs will affect the energy remaining for distribution among the rest of the outputs. This is known as cross-regulation because the outputs are coupled through the energy stored in the inductor. There are two main types of cross-regulation: transient and load disparity. Transient-induced cross-regulation is when a load step or dump on an output suddenly disturb the energy in the inductor to cause an undershoot or overshoot on the other outputs due to excessive or lack of energy received.

Load-disparity cross-regulation occurs when the load between the outputs is considerable large. During steady-state, the inductor must carry enough energy to satisfy all outputs, and since one output is heavily loaded the inductor must carry at least this current. When a lightly-loaded output connects to the inductor and quickly receives a lot of energy, control must react almost immediately to prevent an overshoot. However,

limitations on minimum on-time in the light-loaded output's switch, its driver, and control would make the output receive more energy than consumed every cycle. This can create a run-away condition with the lightly-loaded voltage as it keeps increasing that must be prevented.

1.4.2.4 Efficient Buck-Boost Supplies

Single-output switched-inductor converters can only generate a buck or boost supply unless a four-switch buck-boost topology is used. A single-inductor multiple-output inherently has a higher number of switches to connect the output supplies. Fortunately, this also provides flexibility in the control to adapt the switching sequences to generate a mix of buck and boost supplies. However, this must be done with the minimum number of switching transitions to reduce power losses and design complexity.

1.5 Summary

Portable electronics, such as wireless microsensors, incorporate many features and functions that improve our quality life, save energy and money, and can save lives. These microsystems, powered by a small battery, incorporate blocks that often include sensing and converting sensed signals to a digital domain, a digital signal processor and communications to a central location for reporting. Each of these functions have their own specific supply and power requirements to optimize energy usage and performance which includes step-down and step-up regulation. Also, at the system level, blocks are duty-cycled when not in use and their supplies adaptively adjusted depending on their workload to minimize power consumption. Regulators, besides supplying a mix of buck and boosted

supplies, must be efficient and quick responding to this energy optimizing techniques to leverage their impact.

Linear regulators are fast and compact, but can only buck and are energy inefficient. Meanwhile, switched-capacitor circuits can be integrated and are more efficient, however they can only transfer limited energy per cycle and therefore have limited accuracy and their efficiency is still dependent on voltage conversion. Luckily, switched-inductor converters are the most efficient, but inductor are difficult to integrate. Even though research is being conducted to reduce the size of the passive to allow integration, tradeoffs with efficiency and manufacturing cost prohibits such implementation for wireless microsystems. Fortunately, using a single-inductor to regulate and supply several outputs balances efficiency and size, and hence costs.

Single-inductor multiple-output (SIMO) converters present their own challenges: analysis, accuracy, and cross-regulation. SIMO is multi-loop and non-linear system that increases complexity in the analysis and design. Accuracy degrades in a SIMO because each output is duty cycled and forces the output capacitor to solely provide the output's energy for a longer period compared to the single-output counterpart. Also, during transient events such as load dumps, outputs must wait for their turn to receive the energy necessary to replenish the output capacitor and adjustment of energy delivered. Because the inductor is shared, a sudden energy change in an output affects what other receives, therefore causing transient cross-regulation. During steady-state, load disparity between outputs also causes cross-regulation when an output receives much more energy than it needs. If left uncontrolled, this can continuously charge lightly loaded outputs and loose regulation.

Also, a SIMO will inherently have a higher number of switches and switches events. Regulating a mix of buck and boost outputs can make them advantageous given their flexibility on switching sequences; however, it must be done efficiently. In conclusion, SIMO converters can greatly improve the form factor for microsystems, or more generally portable electronics, with high efficiency to prevent excessive battery drain. Research groups has been focusing on understanding and solving the challenges with SIMO during operation and control. Bridging the performance gap between single-output and multiple-output switched-inductor converters will propel a cost reduction and miniaturization that will help to deploy more microsystems to leverage their benefits.

CHAPTER 2

SINGLE-INDUCTOR MULTIPLE-OUTPUT CONVERTERS

2.1 SIMO Operation

The control scheme in a single-inductor multiple-output (SIMO) allocates time to each output to receive energy from the inductor and adjust their on-time to achieve regulation against variations. There are two basic approaches for time allocation: dedicated energy packets or shared energy packets [52–53]. This section discusses the advantages and shortcomings for both operations used in the state of the art.

2.1.1 Dedicated Energy Packets

A dedicated energy transfer allocates a full inductor energizing and de-energizing sequence to each output [54−58]. This means that the SIMO behaves like independent single-output switching converters that shares the inductor after each switching period. Figure 2.1 (a) shows a buck power stage with the output shared by two outputs while Figure 2.1 (b) shows its operation with dedicated energy packets. From the beginning of a cycle, output v_{O1} receives energy until the inductor current i_L completely de-energizes and stays de-energized until the end of the next period. Similarly, output v_{O2} will receive energy on the following cycle. Equivalently, each output operates at a higher switching period, which for the example in Figure 2.3 will be at twice the switching period for two outputs.

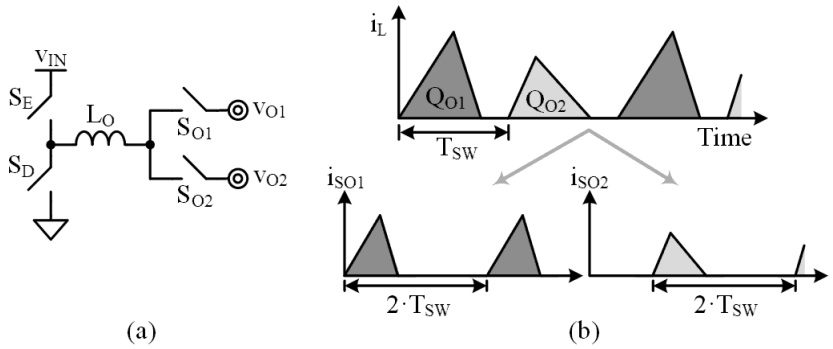


Figure 2.1. A sample two-output SIMO (a) and dedicated energizing operation (b).

Since there is no sharing of the energy packet that inductor transfers, its main advantage is no output interferences in the regulation of other outputs, or in other words, minimum cross-regulation. However, for minimum cross-regulation, the converter requires that inductor completely de-energizes before the end of the period otherwise known as discontinuous conduction mode (DCM) operation. This way, the current will always start from a known value independent of load conditions among the outputs. However, this imposes a maximum deliverable output power with a given time allocation [58]. For instance, in the SIMO from Figure 2.1, the maximum power $P_{O1(MAX)}$ for output v_{O1} is when the energy packet occupies the entire allocation period T_{SW}. By calculating the maximum charge Q_{O1} that can be delivered, $P_{O1(MAX)}$ can be expressed as:

$$P_{O1(MAX)} = \frac{Q_{O1(MAX)}V_{O1}}{T_{SW}} = \frac{(V_{IN} - V_{O1})V_{O1}^2 T_{SW}}{4L_O V_{IN}}. \quad (2.1)$$

To increase the maximum output power, the inductance should be low at the expense of higher conduction losses due to the current ripple increase. Alternatively, switching period can be high to increase output power but regulation suffers because each output receives energy less frequently compromising dynamic and voltage ripple performance [52].

To circumvent the power limitation, the inductor current i_L can stop de-energizing before it reaches zero and operate in a pseudo continuous-conduction mode (PCCM) [56]. As Figure 2.2 shows, instead of the inductor current i_L starting from zero, it starts from a fixed value I_{PCCM}, which allows the outputs to receive more energy from the beginning of the cycle. Unfortunately, an additional switch is necessary to circulate the I_{PCCM} current around the inductor when no output receives energy. This extra switch introduces more power losses that are more noticeable at higher load currents that can limit the full-load efficiency $\eta_{C(FL)}$. The dedicated energy packet scheme, irrespective of DCM or PCCM operation, has either higher current ripples or more switching losses that limits the power conversion efficiency at full load $\eta_{C(FL)}$ to below 80% [55–56], [58].

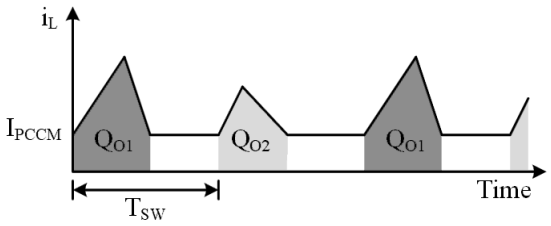


Figure 2.2. Pseudo CCM operating mode to increase power delivery.

2.1.2 Shared Energy Packet

The other energy transferring scheme is to share the energy packet in the inductor among outputs in a single switching cycle [59−78], as Figure 2.3 shows the corresponding inductor current i_L waveform under this scheme. The main advantage is that there is no output power limitation since it can operate in continuous conduction mode (CCM) unlike the dedicated energy packets scheme. Another benefit is that every output receives energy every switching cycle, or in other words, every output refresh rate is the switching frequency. This keeps accuracy high compared to the dedicated energy packet scheme [52].

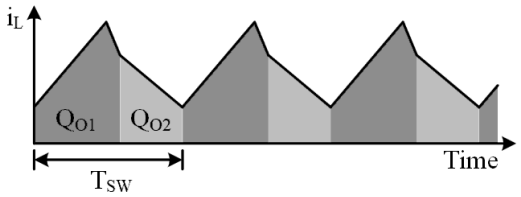


Figure 2.3. Inductor current waveform during shared energy packet operation.

However, the fact that the outputs share the same energy packet results in cross-regulation. If a single output requires more energy, it can deprive subsequent outputs of energy and thus affecting their regulation. For instance, in a two-output buck power stage, when inductor ripple is very small, the duty cycle, or fraction of the period that connects to the inductor, of an output voltage v_{O1} is a function of the ratio between its load i_{O1} to the total load:

$$d_{O1} = \frac{i_{O1}}{i_{O1} + i_{O2}}. \tag{2.2}$$

This means that duty cycle of one output has a load dependence on the other making them susceptible to interaction, and therefore cross-regulation.

2.1.2.1 Cross Regulation

There are two ways to mitigate the cross-regulation with a shared energy packet scheme: matching output and inductor current [69], and having a freewheeling period or auxiliary output as an energy buffer [63], [72], [78]. Matching output current i_O to the closest level of inductor current i_L reduces cross regulation when there is a load disparity among outputs. It achieves so by connecting the output with the lightest load at the beginning and near the end of the switching period when inductor current is low. The disadvantage of this technique is the control complexity for comparing and sorting output loads for more than

two outputs. Also, the benefit reduces as inductor current ripple is very small compared to the DC value because the current discrepancy between i_L and i_O is reduced only slightly after sorting.

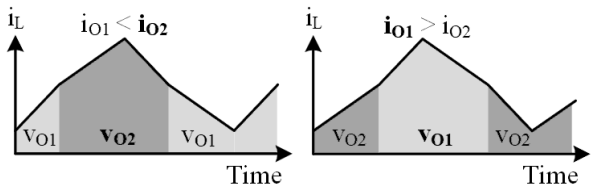


Figure 2.4. Matching load to inductor current level reduces load-disparity cross regulation [69].

A limitation to matching current levels of the load to inductor is that it still does not address transient cross regulation as when one output's energy demand suddenly change. An alternative to mitigate this cross regulation is to add an energy buffer through a freewheeling period [78] or an auxiliary output [63], [73]. Since cross regulation propagates towards the last output in the sequence, an energy buffer at the end of the period provides or absorbs energy require to recover from a sudden load change. Figure 2.5 shows the power stage and operation with an extra switch that circulates a regulated fixed current across the inductor toward the end of the switching period [78]. This forces the inductor to store more and prevent energy starvation if any or multiple outputs suddenly need more energy. Likewise, if outputs need less energy, it prevents the last output in the sequence, e.g. v_{ON} in Figure 2.5, to receive excess energy and allow the excess to flow in the freewheeling period t_{FW}. The control eventually readjusts energy in the inductor to compensate for the excess. Since the regulation target of the current during the freewheeling period can be relatively high during heavy loads, it represents an additional power loss when flowing through the additional free-wheeling switch S_{FW}.

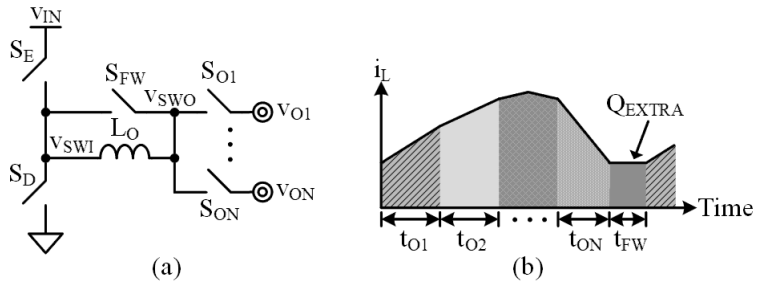


Figure 2.5. Freewheeling period as an energy buffer based on [78].

Alternatively, an auxiliary output can act as the energy buffer. It can either be stored in another temporary output and then transferred back to the supply with an auxiliary switched-inductor converter [63], or connect the input supply as the auxiliary output to reduce component count [73]. Figure 2.6 shows the respective power stage (a) and operating waveforms (b) to use the input supply v_{IN} as an auxiliary output. This is slightly more efficient than recirculating the extra energy through the inductor because the energy is recovered and store back at the input capacitor or battery. Nevertheless, the extra switch and switching events can limit the peak efficiency $\eta_{C(PK)}$ to below 85% [63], [73].

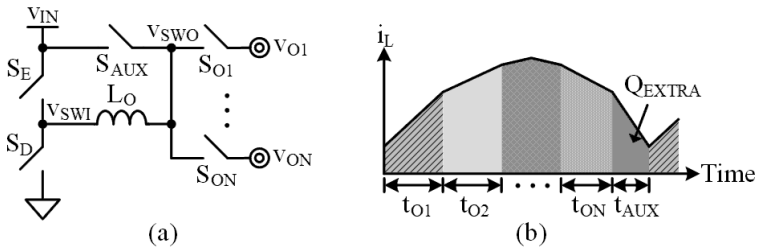


Figure 2.6. Auxiliary output to reduce cross-regulation [73].

2.1.2.2 Mixed Output

Fortunately, a major benefit of the shared energy packet operation is the opportunity to create a mix of buck, boost and inverting supplies. Figure 2.7 shows a generic power stage with possible power flows to generate buck, boost and inverting supplies. Initial inductor energizing can occur from supply to ground (S_E & S_G engages) or from supply to a buck

output v_{BU} (S_E & S_{BU} engages). Afterwards, because the inductor still carries current, a boost output can de-energize the inductor by engaging S_{BO} and the supply S_E or input-side ground S_D switch. Moreover, if inductor still carries current, an inverting output v_{IN} can connect on the input switching node v_{SWI} by closing S_{INV} to generate a negative voltage. Fundamentally, the inductor can only energize through buck outputs or a ground path but can be de-energize with either buck or boost outputs if the input switching node v_{SWI} is connected to ground; otherwise, if the input side is connected to the supply, it can only de-energize through a boosted output.

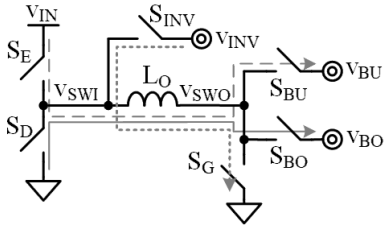


Figure 2.7. Power paths for mixed output generation on a SIMO.

Literature shows various configurations to generate a mix of output voltages including buck & boost outputs [57], [64], [67], [68], [70], [75], and [78]. For the portable microsystem applications, the majority of outputs are buck and few or one needs to be a boosted voltage. When using a boost-derived topology such as in [64] or [67], boost power must dominate the total buck power to prevent overcharging boost outputs. Otherwise, control bypasses inductor and transfer energy directly to the outputs to prevent the runaway condtion, and doing so reduces power conversion efficiency between 5-10%. Therefore, a buck-derived boost is more compatible with the targeted application to avoid unnecesary switching events and minimize losses.

Other work uses single energy packet scheme which as previously discussed limit efficiency [78]. Work at [70] avoids such extra losses with adaptively adjusting the switch sequence to generate buck and boost outputs; however, its extended-PWM, which compares the ramps for each output, to generate such control adds higher complexity for more than two outputs. Therefore, a scalable, simple implementation and efficient mixed output converter able to generate buck and boost supplies is neccesary for microsystems applications.

2.2 SIMO Control

The shared energy packet scheme increases control complexity because it needs to regulate both the stored energy in the inductor as well as the distribution among the outputs. Although voltage-mode control is possible [59], [61]; it often limits the control bandwidth due to the complex conjugate pole of the power stage that must be compensated for. A current loop that regulates inductor current effectively transforms the inductor in a current source up to the loop's bandwidth. This eliminates the pole that the inductor contributes in the system or main loop leading to a simpler compensation, design and higher bandwidth [79]. Most of the state of the art uses a pulse width modulation (PWM) approach with few variations on the control that distributes the energy among outputs.

2.2.1 Current-Mode PWM Variations

When implementing the current loop, state-of-the-art SIMOs commonly uses peak current control [60], [63], [64], [67], [69], [72], [73], [76], and [77]. Figure 2.8 (a) shows the control structure that includes a sampling point for the inductor current i_L, a conversion to

voltage v_{IL} through equivalent resistor R_S and a comparator. When a cycle begins, a clock engages the inductor L_O into energizing until its peak equates a reference point v_{ERR}. The reference v_{ERR} set by an amplified total error among outputs, or alternatively only the last output in the sequence, dictates how long energizing time t_E, or duty cycle d_E, lasts as Figure 2.8 (b) shows. This control provides a simple and robust control; however, it needs a saw tooth voltage v_{SAW} added to the sensed current to compensate for sub-harmonics oscillations when energizing duty cycle d_E is higher than 50% as the single-output counterpart requires [80].

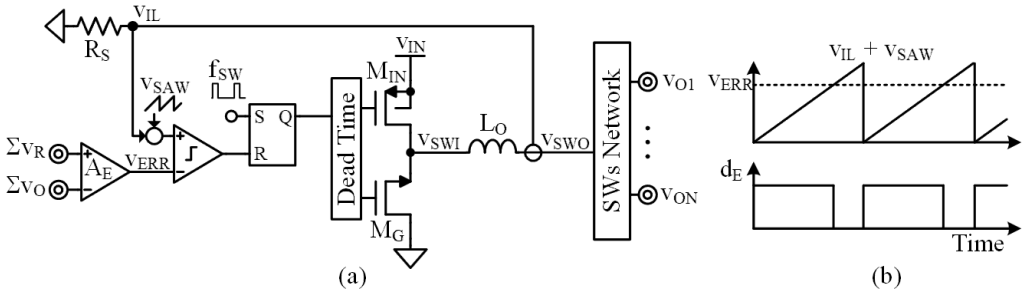


Figure 2.8. Peak current control for SIMO converters (a) and operating waveforms (b).

The current loop will store enough energy in the inductor to satisfy all outputs; but additional loops are required to distribute this energy. Because one output can be connected for the reminder of the switching period until a new cycle begins, an additional N – 1 loops are required for an N-output SIMO converter. These loops are local to each output, which makes them independent of the of the current loop, or in other words independent voltage loops. There are two main approaches for the independent voltage loops in literature: PWM and peak-voltage control.

2.2.1.1 Fully PWM

The independent voltage $v_{OI(K)}$ loops, i.e. all outputs except the last in the sequence, can be controlled using a simple PWM loop [69], [77]. Under this scheme, an output starts to receive energy, and when ramp voltage v_{RAMP} reaches the amplified error of the controlled output, it disconnects from the inductor like implementation in Figure 2.9. This control provides good accuracy for a simple implementation.

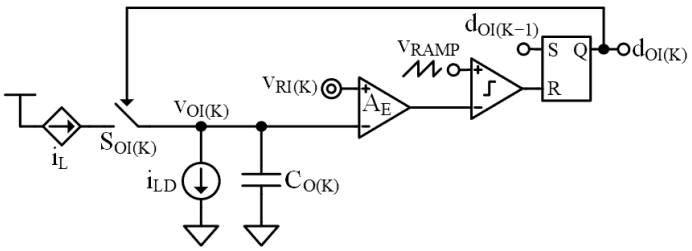


Figure 2.9. PWM control for the independent voltage loops.

The incorporation of the inductor current in the modulation while the output receives energy improves accuracy and cross-regulation specially when there is load disparity among outputs [64], [67], [73]. Figure 2.10 shows such implementation by replacing the modulation from a constant-slope ramp to a ramp with slope proportional to the sensed current through the switch. As an example, if an output receives a large current through its switch, the modulation ramp increases faster. This effectively increases the loop gain and the comparator can resolve finer duty cycles that helps reduce load-disparity cross regulation.

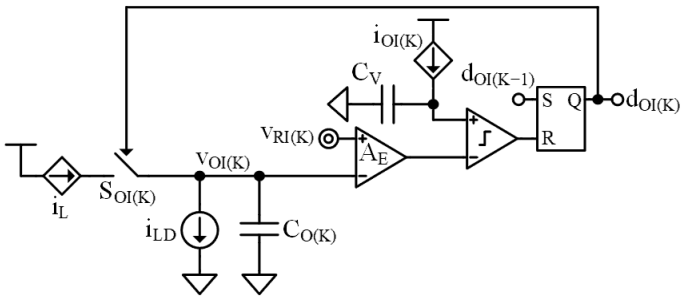


Figure 2.10. PWM control with current feed forward on independent loops.

Although any of the discussed PWM methods can regulate independent outputs accurately, they are slow responding to load dumps. They require multiple cycles to recover from a load dump because they control an average quantity of the output voltage [81]. Because portable microsystems must react and regulate supplies to a moving target or after a waking up a block, bandwidth is an important requirement for the control.

2.2.1.2 Peak Voltage

Direct regulation of an instantaneous signal is faster because it bypasses any filtering or intermediate block. A simple implementation, as shown in Figure 2.11, is to regulate the voltage of the independent outputs to a reference directly with a comparator to determine the on-time. This control effectively regulates the output's peak voltage [60], [63], [66], [72], [76]. The direct regulation of the outputs creates a challenging aspect of this simple control since it is noise sensitive due to the lack of filtering. Also, because this control is often combined with a current-mode PWM approach, the total response of the converter is limited by the PWM bandwidth of the current regulation.

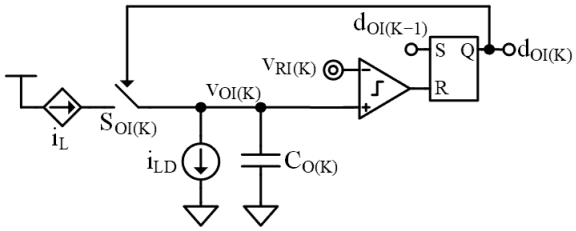


Figure 2.11. Peak voltage control for independent outputs.

2.2.2 Linear Regulator Hybrids

An alternative power stage topology and control combines the high efficiency of a switched-inductor converter with the high bandwidth of a linear regulator. Figure 2.12 (a) shows a power stage that adds a linear regulator to each output while Figure 2.12 (b) shows

the switched-inductor control's block diagram [55]. Each linear regulator directly corrects any error in the output while the SIMO drives the current in each linear regulator to zero. This allows the converter to react to a rising load dump in less than 50 ns, while achieving a peak efficiency of 83% at steady-state. However, since the linear regulators can only supply currents, the benefits are less for a falling load step, increasing to a 2 μs response time. Also, since the linear regulator has high bandwidth, it will try to regulate against the output voltage ripple at steady-state. This means that its current will be non-zero and will reduce efficiency specially at high current levels as noted by the 72% reported in [55].

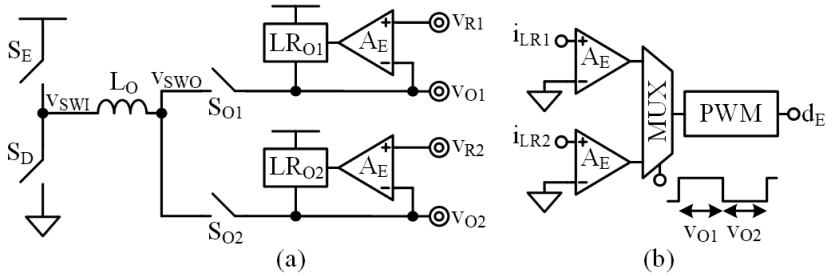


Figure 2.12. (a) Switching-linear hybrid converter with dedicated linear regulator on each output (a) and (b) PWM control scheme that multiplex between outputs [55].

Despite the integrability of a linear regulator, dedicating one per out increases silicon real estate and hence cost. An alternative is to allocate one linear regulator available for all outputs from the switching node [54]. Figure 2.13 shows the concept where the linear regulator sources or sink current from the output switching node v_{SWO} according to the total error among outputs. This implementation results in a higher power conversion efficiency because the steady-state current the linear regulator provides is closer to zero due to ripple cancelation because of the error summation. In addition, because it is a shared linear regulator, its quiscent power is less. This results in a peak efficiency $\eta_{C(PK)}$ of 88.7% but can drop to 82% at full load conditions [82]. Leveraging a single linear regulator for

many outputs can be very challenging because no independent loop regulate the output voltages directly. Using an error-based approach, in which only the output with the largest error receives energy in a given cycle, is possible but it can result in cross-regulation and unregular switching at steady-state [82].

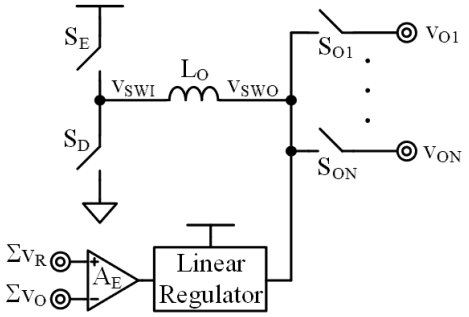


Figure 2.13. Switching-linear hybrid converter with single linear shunt regulator for all outputs [82].

2.3 Context and Comparison

A quantitative comparison among proposed supplies is necessary to evaluate the merits of control and operation techniques given a certain context and application. For a fairer comparison, the approach would be divided between control approaches and mixed-output (buck and boost) operation to account for the inherent design tradeoffs of the later. Nevertheless, the same figure of merit (FoM) will compare both as it is focused on the SIMO performance for wireless microsystem applications.

2.3.1 Figure of Merit

Comparing the state of the art (SoA) is difficult because too many metrics describe the performance of a switched-inductor power supply. Plus, the significance and relative weight of each parameter can vary widely from one application to the next. Still, comparing

under equivalent conditions and uniform weights can be useful. So, for the purposes of the following discussion, all independent parameters carry equal weight.

A multiple-output inductor is more appealing when it supplies higher total current $i_{O(MAX)}$ and more outputs N_O with higher power-conversion efficiency η_C. Although η_C can be more important at one level, peak and full-load efficiencies $\eta_{C(PK)}$ and $\eta_{C(FL)}$ reflect what is possible when optimized and stretched to output as much power as possible. And although maximum output-voltage variation $\Delta v_{O(MAX)}$ is important, $\Delta v_{O(MAX)}$ ultimately depends on output capacitance C_O, maximum load dump $\Delta i_{O(MAX)}$, and response time t_R. t_R, however, is largely independent of the others. Plus, given t_R and any of the other two, the third is simply their consequence. Hence, t_R is arguably the one that represents the rest.

A power supply is also more attractive when it costs less and occupies less space. In this respect, fewer off-chip components N_{OC} and smaller silicon die size A_{SI} cost and occupy less, and longer channel-length technologies L_{MIN} cost less. Plus, longer L_{MIN} technologies can sustain higher voltages. Assuming all these parameters are equally significant, an all-encompassing figure of merit (FoM) should rise with higher $i_{O(MAX)}$, N_O, $\eta_{C(PK)}$, $\eta_{C(FL)}$, and L_{MIN} and lower t_R, N_{OC}, and A_{SI}. Normalizing the FoM to one point of reference PoR reveals a relative FoM or RFoM that is useful when comparing devices:

$$\text{RFoM} \equiv \frac{\text{FoM}}{\text{PoR}} = \frac{i_{O(MAX)} N_O \eta_{C(PK)} \eta_{C(FL)} L_{MIN}}{t_R N_{OC} A_{SI} \text{PoR}}, \tag{2.3}$$

where PoR is the FoM of the best SoA in each comparison.

2.3.2 Mixed-Output SIMO Comparison

The mixed-output SoA, summarized in Table 2.1, commonly uses a PWM control approach. This control consistently has a peak efficiency $\eta_{C(PK)}$ close or higher than 90%. However, [63] and [78] uses an energy buffer as an auxiliary output that increases losses as [78]'s full-load efficiency $\eta_{C(FL)}$ of 74% shows. Also, Table 2.1 shows that the design has been focused on operation and steady-state performance given the lack of report for response time t_R.

Table 2.1. SoA Comparison of Mixed-Output (Buck & Boost) SIMO Converters.

	Units	**[63]**	**[78]**	**[67]**	**[64]**
Notes	–	I-PWM, V-PK Energy Buffer	Fully PWM Energy Buffer	Fully PWM	Fully PWM
L_{MIN}	µs	0.5	0.25	0.25	0.25
A_{SI}	mm^2	3.6	10	2.1	3.8
v_{IN}	V	2.5–4.5	2.7	0.9–1.6	1.8–2.2
v_O	V	2–12	1.8–3.3	0.6, 1.8	1.25–2.25
$i_{O(MAX)}$	mA	145	650	240	400
N_O	#	5	4	2	4
N_{OC}	#	10	5	3	5
$\eta_{C(PK)}$	%	83	91	92	93
$\eta_{C(FL)}$	%	–[1]	74	92	92
t_R	µs	–[1]	10[2]	–[1]	–[1]
RFoM	%	39[3]	49	90[3]	100[3]

[1]Not reported. [2]Estimate. [3]assumes t_R = 10 µs for comparison.

2.3.3 Control Comparison

Table 2.2 compiles the state of the art (SoA) which reported almost all considered parameters and with the best control performance for wireless microsystem applications. The best performing technique using the discussed FoM in equation (2.3) is the hybrid with

dedicated linear regulators [55], thanks from its 2 μs response time in despite its low 72% full-load efficiency $\eta_{C(FL)}$. Using a dedicated energy transfer scheme resulted in a low 72% full-load efficiency $\eta_{C(FL)}$ and slow response time of 20 μs [58]. A full PWM approach helps balance the response time to around 5 to 40 μs while maintaining a full-load efficiency $\eta_{C(FL)}$ above 80%. Using a peak voltage control can provide bandwidth benefits but the complexity of the particular implementation of [76] of a shared comparator and a time limit for any outputs increases response time to 200 μs.

Table 2.2. SoA Comparison of Control schemes for SIMO Converters.

	Unit	[58]	[55]	[65]	[77]	[69]	[72]	[73]	[76]
Notes		Dedicated E-Packet	Hybrid	Fully PWM	Fully PWM	Fully PWM	Fully PWM	Fully PWM	I-PWM V-PK
L_{MIN}	μm	0.5	0.35	0.25	0.04	0.055	0.5	0.065	0.35
A_{SI}	mm^2	2.4	3.84	5.29	4.00	0.98	4.40	1.86	5.04
v_{IN}	V	1.3–2.85	2.7–3.3	2.7–5	2.7–3.6	2.7–3.6	1.2–2.2	3.4–4.3	2.0–3.0
v_O	V	3, 3.6	1.2, 1.8	1.2, 1.8	1.1–2.25	1.8, 1.2	3.0, 2.5	1.2–2.8	2.5–5
$i_{O(MAX)}$	mA	170[2]	200	600	900	600	100	1150	400
N_O	#	2	2	2	4	2	2	5	8
N_{OC}	#	3	3	4	5	3	3	6	9
t_R	μs	20[2]	2[1]	15[2]	40[2]	8[2]	5[2]	12[2]	200[2]
$\eta_{C(PK)}$	%	88	83	87	89	91	81	83	92
$\eta_{C(FL)}$	%	72[2]	72[2]	80[2]	86[2]	83[2]	80[2]	83[2]	74[2]
RFoM	%	21	100	18	4	58	27	53	2

[1]uses linear regulator, [2]estimated from reported measurements.

2.4 Summary

A SIMO can operate by delivering a dedicated energy packet or a shared energy packet to the outputs. By dedicating a full energizing/de-energizing event to a single output per switching cycle, the converter can isolate the outputs from each other if the inductor current consistently reaches a known value at the end of the cycle. This minimizes interaction, or cross regulation, among outputs. However, the maximum output power is limited when inductor current reaches zero at the end of the cycle. An alternative is to de-energize the inductor current to a fixed value greater than zero at the cost of higher conduction losses. Also, this operation also decreases accuracy since each output is refreshed less frequently and must wait several switching cycles to receives energy again.

Operation under a shared energy packet scheme, on the contrary, refreshes every output more frequently and does not have a maximum output power restriction. However, because the energy packet is shared, interaction between outputs, or cross regulation, is possible. This means that one output can disturb the remnant energy for the other outputs. Ordering the output sequence such that the load is close to the inductor current level can alleviate the load disparity cross regulation but is limited when inductor current ripple is small and increases complexity due to the sorting every cycle. Having an energy buffer to absorb most of the cross-regulation at the end of the cycle is possible but this increases losses and silicon real estate due to the added switches and sequence.

An additional benefit of a shared energy packet is the flexibility to generate mixed outputs voltages, this means buck and boost. An inductor always energizes through a buck and de-energizes through a boost output; hence, having the correct sequence allows for the SIMO to generate a mix of buck and boost voltages without increasing complexity.

However, most work in literature use a boost-derived buck where boost are the dominant output. If not, it can create a runaway problem in the inductor current that currently is solved by transferring energy bypassing the inductor and therefore increasing losses.

Besides the power stage and its operation, a SIMO requires two control knobs: one to sufficiently energize the inductor and another to distribute energy among outputs. Literature mostly uses a current-mode PWM approach to adjust the inductor current. Specifically, it uses peak current control which is simple and provides and inherent current protection, but requires slope compensation to prevent subharmonic oscillations. For energy distribution control, there exist two main approaches: fully PWM solution and peak-voltage. Incorporating a local PWM loop among independently controlled outputs provides accurate regulation and uncomplicated design. Even though feedforwarding the inductor current as the modulation ramp improves the control, the total solution is PWM which takes several cycles to respond to load dumps. Peak voltage can improve response time by using a simpler circuit but the bandwidth is still limited by the current-mode PWM loop.

Combining a linear regulator which handle fast transients can improve response time, while keeping the high efficiency of a switched inductor at steady-state. However, linear regulators increase losses because even at steady-state, they provide a small current to regulate against the ripple voltage. Dedicating a single linear regulator for each output, which can be integrated, occupies a large silicon real state. Using a single linear regulator that provides all the current at a shared node such as the switching node decreases die area but increases complexity in the distribution of the energy.

Comparison of the state of the art (SoA) reveals that operation validation has been the objective among the mixed-outputs converters with buck and boost outputs. Hence, there is lack of discussions in the literature on techniques to improve response time, and the pro and cons of generating a mix of voltages at varying power ratios between buck and boost outputs. Also, the SoA has been focused on mostly fully PWM schemes that balances a high efficiency with a modest response time. Adding a parallel linear regulation to each output provides the fastest response time for the SoA at the expense of higher losses at high current levels. Hence, a control technique that can respond close as a linear regulator but without the sacrifices of efficiency and silicon real estate will improve the state of SIMO converters for wireless microsystems.

CHAPTER 3

STABILITY ANALYSIS OF HYSTERETIC CURRENT-MODE CONTROL FOR SWITCHED-INDUCTORS CONVERTERS

3.1 Hysteretic Control

PWM control loops are well understood, robust and easy to stabilize but require multiple cycles to respond to a sudden load change [81]. Fortunately, hysteretic loops respond when their controlled variables surpass the hysteretic window limits, so they react within one switching cycle [83]. Despite its transient benefits, understanding the nonlinear feedback dynamics of hysteretic converters is arduous. Phase-plot portraits [84], sliding-mode theory [85-87], state-space averaging [88–89], and circuit averaging [90−94] help in the design process of single output hysteretic converters, but the equations they generate are often abstract and difficult to relate to circuit operation, to inductor-current and output-voltage ripples, response time, and others. Thus, an intuitive and insightful analysis that asses the stability of a hysteretic converter is necessary for easier design and understanding.

Moreover, analysis and design of single-inductor multiple-output (SIMO) supplies are largely absent in literature. To simplify the analysis, the hysteretic current mode must be analyzed for a single-output converter before extending it to the multiple output counterpart that has additional feedback loops. The following sections break down the analysis by starting for a single-output switched-inductor converter and then extending the analysis to a multiple output converter and the interactions among its feedback loops.

3.2 Single-Output Hysteretic Current-Mode Design

Current-mode control turns the inductor L_O into a current source and thus removing its pole in the main loop [79]. In the hysteretic case, which Figure 3.1 illustrates, like a relaxation oscillator, the control keeps L_O's i_L rippling about i_L's average $i_{L(AVG)}$ between the hysteretic limits that comparator CP_{OSC} and feedback resistor R_S set. This way, L_O's ripple Δi_L is constant and the oscillator is a transconductor block G_{OSC} inside the voltage loop that outputs $i_{L(AVG)}$ set by amplified error voltage v_{ERR}.

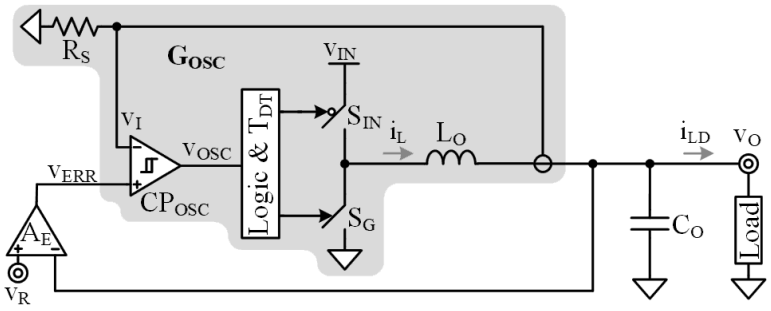


Figure 3.1. Hysteretic current-mode switched-inductor buck dc-dc converter.

3.2.1 Operation

Since the system regulates output voltage v_O and v_O's ripple Δv_O is miniscule with respect to v_O, v_O for the oscillator is practically constant at V_O. As such, i_L in Figure 3.1 and the voltage $i_L R_S$ that i_L generates across R_S rise linearly when input switch S_{IN} energizes L_O from v_{IN} to v_O with voltage v_E at $v_{IN} - v_O$ at di_L^+/dt or v_E/L_O, as Figure 3.2 shows. When $i_L R_S$ surpasses comparator CP_{OSC}'s upper threshold, CP_{OSC} trips and opens S_{IN} and closes ground switch S_G, which drains L_O to v_O. With a negative de-energizing voltage $-v_D$ at $-v_O$ across L_O, i_L and $i_L R_S$ reverse direction at di_L^-/dt or $-v_D/L_O$ until $i_L R_S$ reaches CP_{OSC}'s lower threshold. This way, $i_L R_S$ rises and falls to traverse CP_{OSC}'s hysteresis V_{HYS} across energizing and de-energizing times t_E and t_D, and together, across t_{OSC}, so

$$\Delta i_L = \frac{V_{HYS}}{R_S}, \tag{3.1}$$

$$t_E = \left(\frac{L_O}{v_E}\right)\Delta i_L \approx \left(\frac{L_O}{v_{IN} - v_O}\right)\left(\frac{V_{HYS}}{R_S}\right), \tag{3.2}$$

$$t_D = \left(\frac{L_O}{v_D}\right)\Delta i_L \approx \left(\frac{L_O}{v_O - 0}\right)\left(\frac{V_{HYS}}{R_S}\right), \tag{3.3}$$

$$\text{and } f_{OSC} = \frac{1}{t_{OSC}} = \frac{1}{t_E + t_D}. \tag{3.4}$$

In short, Δi_L is constant and traverses across V_{HYS}/R_S every t_{OSC} period.

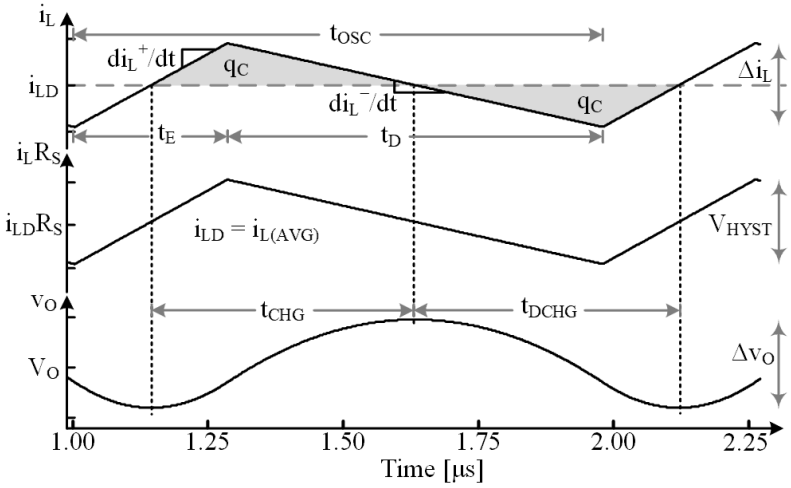


Figure 3.2. Single-output steady-state waveforms of the hysteretic buck converter.

Since the load sinks $i_{L(AVG)}$, i_L's ripple Δi_L flows entirely into C_O to establish how much the output v_O ripples in steady state. The charge q_C that Δi_L sources and sinks across every half period $0.5t_{OSC}$, is basically the area under Δi_L about $i_{L(AVG)}$ during C_O's charging time t_{CHG}. So, since Δi_L is a triangular waveform, C_O's ripple Δv_O reduces to

$$\Delta v_O = \frac{q_C}{C_O} = \frac{(0.5)(0.5\Delta i_L)(0.5t_{OSC})}{C_O} = \frac{\Delta i_L t_{OSC}}{8C_O}. \tag{3.5}$$

3.2.2 Loop Analysis

To the overall system, the oscillator is simply a block that outputs and adjusts $i_{L(AVG)}$ in response to a voltage v_{ERR}. To see this, recall that comparator CP_{OSC}'s hysteresis voltage V_{HYS} is about its input v_{ERR}. This means v_{ERR} is the center voltage $i_{L(AVG)}R_S$ about which i_LR_S oscillates. In other words, the block's low-frequency transconductance gain G_{OSC0} or $i_{L(AVG)}/v_{ERR}$ is:

$$G_{OSC0} = \left.\frac{i_{l(avg)}}{v_{err}}\right|_{\text{Low frequency}} = \frac{1}{R_S}. \tag{3.6}$$

Since bandwidth essentially describes response time, the time t_R the oscillator requires to adjust $i_{L(AVG)}$ to a new value is a measure of its bandwidth f_{IBW}. A straightforward way to characterize the current loop as a close loop system is to step its input v_{ERR} and observe and model its response with an equivalent linear system that similarly responds. In this light, a voltage step in v_{ERR}, as Figure 3.3 shows at 5 and 20 μs, shift CP_{OSC}'s thresholds. Hence, i_L's rising and falling rates di_L^+/dt at v_E/L_O and di_L^-/dt at $-v_D/L_O$ determine response time t_R. Since the RC-equivalent bandwidth that corresponds to reaching 98% of i_L's target is $1/2\pi R_{EQ}C_{EQ}$ from i_L^* in Figure 3.3 and

$$t_R \equiv R_{EQ}C_{EQ}\ln\left(\frac{1}{1-0.98}\right) = 4R_{EQ}C_{EQ} \equiv \frac{4}{2\pi f_{IBW}}, \tag{3.7}$$

$1/2\pi R_{EQ}C_{EQ}$ is a linear equivalent that can model f_{IBW}.

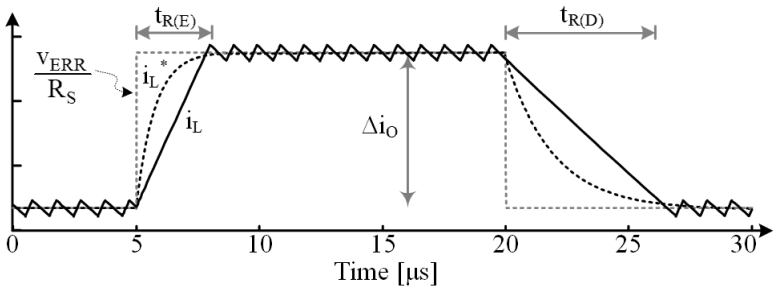


Figure 3.3. Step response of inductor current i_L and its $R_{EQ}C_{EQ}$ equivalent i_L*.

Although i_L slews to 98% of its target and its linear counterpart i_L^* rises exponentially, both reach 98% at the same time. Since i_L^* slows as it nears its ultimate target and the actual does not, modeling i_L to 80% with i_L^* means i_L^* requires more time to reach its final value than i_L. This is a pessimistic expectation that results in an over-sized C_O. As simulations will later prove, modeling the response to 98% predicts the oscillator's bandwidth and response fairly well.

For $i_{L(AVG)}$ to traverse across $\Delta i_{L(AVG)}$, i_L must rise or fall by an equivalent amount. Since quasi-constant voltages v_E and v_D energize and de-energize L_O, i_L ramps at a constant rate di_L/dt according to L_O's impressed voltage v_L. Since v_L is v_E when i_L rises and v_D otherwise, the response time t_R for rising and falling load dumps is different:

$$t_R = \frac{\Delta i_{L(AVG)}}{di_L / dt} = \Delta i_{L(AVG)} \left(\frac{L_O}{v_L} \right) = \Delta i_O \left(\frac{L_O}{v_L} \right), \tag{3.8}$$

where $i_{L(AVG)}$ flows to the load as i_O as in the buck converter. Unfortunately, modeling f_{IBW} with the longest t_R is overly pessimistic and with the shortest delay overly optimistic. Plus, a real response incorporates ringing that invokes both rising and falling slopes. Therefore, emulating the average of these delays with the previously defined 98% $R_{EQ}C_{EQ}$ model

balances the approximation and reduces v_L to two times the parallel equivalent of v_E and v_D, f_{IBW} to

$$f_{IBW} = \left(\frac{4}{2\pi}\right)\left(\frac{1}{\Delta i_O}\right)\left[\frac{2}{L_O}\left(\frac{v_E v_D}{v_E + v_D}\right)\right], \tag{3.9}$$

and the oscillator's close loop gain G_{OSC} to

$$G_{OSC} = \frac{i_{l(avg)}}{v_{err}} = \frac{G_{OSC0}}{1 + \frac{s}{2\pi f_{IBW}}}. \tag{3.10}$$

Since i_L requires more time to reach its target with higher load dumps Δi_O, f_{IBW} is inversely proportional to Δi_O. This means the worst-case delay across the oscillator corresponds to the highest load dump. In other words, hysteretic current-mode converters are least stable when subjected to wider load dumps, when f_{IBW} is lowest and closest to the systems unity-gain bandwidth f_{0dB}. Incidentally, f_{IBW}'s dependence on Δi_O is an indication of the nonlinear nature of the hysteretic transconductor block.

Amplifier A_E in Figure 3.1 compares v_O to reference v_R to generate an error voltage v_{ERR} as in Figure 3.4. When multiplied by A_E and the oscillator's G_{OSC}, v_{ERR} produces and feeds $i_{L(AVG)}$ to the load's C_O and R_O. So, with negative feedback, offsetting v_O from v_R raises and amplifies v_{ERR} to oppose and reduce the offset between v_O and v_{REF} to zero.

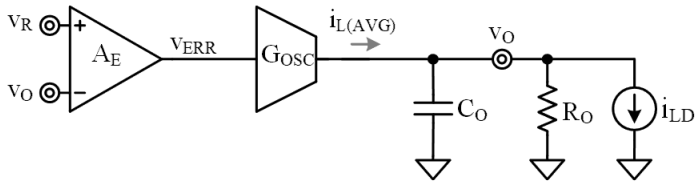


Figure 3.4. Equivalent block diagram of the hysteretic buck dc-dc converter.

The loop is stable with more than 45° of phase margin when the loop gain A_{LG} reaches zero dB and the unity-gain frequency f_{0dB} at 20 dB per decade, which can only

happen after one pole. For this, the output pole p_O that R_O and C_O establish must be low enough to ensure A_{LG} reaches f_{0dB} before G_{OSC}'s bandwidth f_{IBW}:

$$A_{LG} \equiv \frac{v_O}{v_R - v_O} = A_E G_{OSC}\left(R_O \parallel \frac{1}{sC_O}\right). \tag{3.11}$$

Because A_{LG} falls linearly with frequency past p_O, the gain–bandwidth product that A_{LG0} and p_O establish is constant between p_O and f_{0dB} and equivalent to f_{0dB} at 0 dB:

$$f_{0dB} = A_{LG0} p_O = \frac{A_E G_{OSC}}{2\pi C_O}. \tag{3.12}$$

C_O must therefore be sufficiently high to ensure f_{0dB} is near or below the oscillator's f_{IBW}. In feedback terms, A_{LG} must reach f_{0dB} with enough phase margin PM to maintain stable conditions. Since p_O is well below f_{0dB} and f_{IBW} near or above f_{0dB}, p_O lowers 90° of phase from the loop's 180° and f_{IBW} another fraction of 90° to reduce PM to

$$PM = 90 - \tan^{-1}\left(\frac{f_{0dB}}{f_{IBW}}\right). \tag{3.13}$$

Since the oscillator's bandwidth f_{IBW} changes with load dumps Δi_O, so does phase margin PM. With 10 µF of output capacitance C_O, the design of Figure 3.1 when v_{IN} is 3.6 V, v_O is 1 V, L_O is 20 µH, R_S is 0.277 Ω, and A_E is 10 V/V gives a PM of roughly 64° when subjected to 50-mA load dumps and 45° under 100-mA dumps, as Figure 3.5 shows. With 20 µF, PM is 76° with 50 mA and 45° with 200 mA. In other words, the lowest allowable PM and the largest Δi_O ultimately dictate the lowest possible C_O.

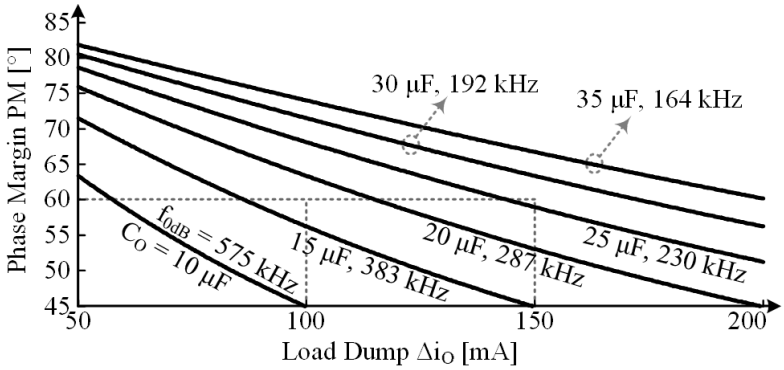


Figure 3.5. Stability curves for a given capacitance and load dump size.

Figure 3.6b shows the simulated response of the designed system. The resulting current and voltage ripples Δi_L and Δv_O are, as expected, roughly 36 mA and 0.4 mV. Inductor current i_L undergoes two oscillating rings before it settles after 100-mA rising and falling load dumps. The second ring is basically an oversized current ripple Δi_L of 45 mA. This means the system has, as expected, about 45° of phase margin [95].

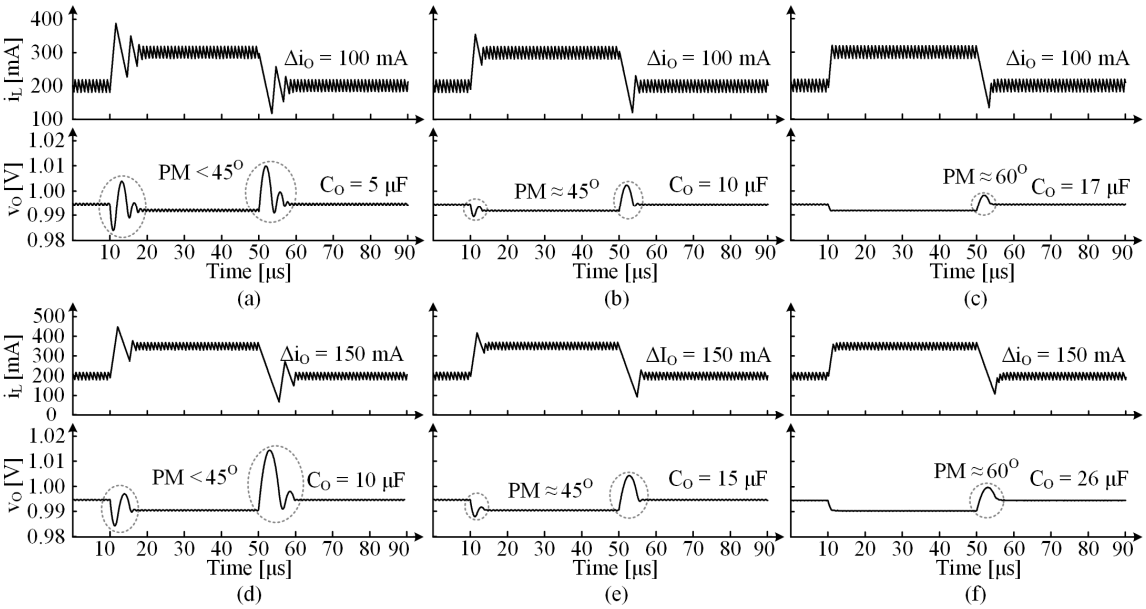


Figure 3.6. Simulation of load dump response across various capacitance and load dump sizes

With less output capacitance C_O, as Figure 3.6a demonstrates for 5 µF, i_L settles after four to five rings, which corresponds to less than 45° of phase margin. In contrast, 17

μF produces no more than one ring, as Figure 3.6c shows, so phase margin is higher at roughly 60° [95]. Note phase margin is worse for falling load dumps in Figure 3.6a and Figure 3.6c, when C_O is 5 and 17 μF, than for rising load dumps. This is because L_O's energizing voltage v_E at 2.6 V is higher than its de-energizing counterpart v_D at 1.0 V, so i_L rises more quickly than it falls. In other words, the oscillator is faster when i_L climbs than when i_L drops.

With a higher load dump at 150 mA, the system recovers after three rings, as Fig. Figure 3.6d illustrates. In other words, phase margin falls below 45° when Δi_O rises above its specified target. To maintain 45°, C_O must therefore rise to 15 μF, and for 60°, to 26 μF, as Figure 3.6e–f further show. Irrespective of the conditions, however, phase margin for rising load dumps is, as before, equal or better than for their falling counterparts.

3.2.3 Measurement Results

To verify the analysis and corroborate simulations, the hysteretic current-mode buck converter was designed in a 0.18-μm CMOS and was implemented as in Figure 3.7. Current sensing was implemented by using RC sensing [96] for ease of implementation and testing flexibility. When L_O's and C_{IL}'s corner frequencies with R_{IL} and R_{LESR} are well below the oscillating frequency f_{OSC}, sL_O and R_{IL} overwhelm R_{LESR} and $1/sC_{IL}$ near f_{OSC}. So L_O's voltage v_L is $i_L sL_O$, v_C is $v_L/sR_{IL}C_{IL}$ or $i_L L_O/R_{IL}C_{IL}$, and v_I is $i_L(10L_O/R_{IL}C_{IL})$ or $i_L A_R$.

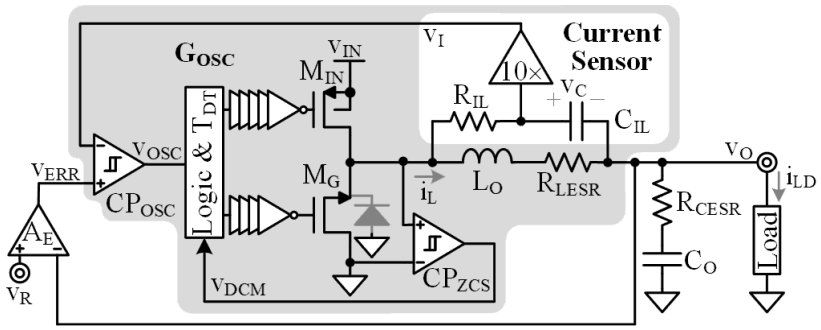


Figure 3.7. Implemented hysteretic current-mode switched-inductor converter.

For a v_{IN}, v_O , Δi_{LD}, and L_O of 1.5 V, 1 V, 180 mA, and 3.3 uH set current bandwidth f_{IBW} to 714 kHz. However, when accounting for parasitics resistances from the PCB, switches, inductor and traces, energizing effective voltage can drop to as low as 0.1 V which pushes f_{IBW} to 195 kHz. For 45° of phase margin, f_{0dB} should not exceed f_{IBW}'s 195 kHz. C_O should therefore be no less than 10 µF when A_E is 12, R_{IL} is 33 kΩ, and C_{IL} is 1 nF, so A_R is 1 Ω, but, for margin, the design on Figure 3.7 uses a C_O of 15 µF.

The measured output v_O in Figure 3.8 ripples 5 to 10 mV and responds within 5.6 µs to rising 40-, 80-, and 180-mA load dumps. The delay t_R is basically how long L_O requires to slew i_L across these load steps. The system responds faster (within 3.4 µs) to similar falling load dumps because L_O's drain voltage v_D is higher at v_O's 1.0 V than L_O's energizing counterpart v_E, which is $v_{IN} - v_O$ or 1.5 – 1.0 V less any voltage drops from parasitic resistances.

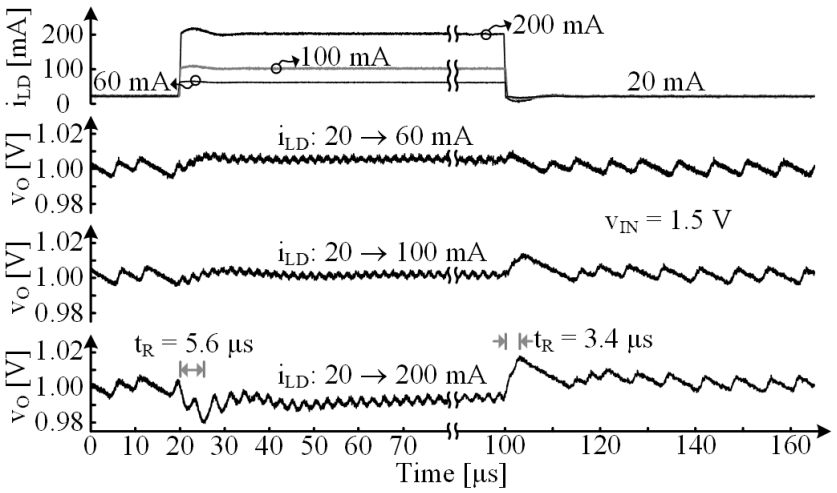


Figure 3.8. Measured response to 40-, 80-, and 180-mA load dumps when input voltage v_{IN} is 1.5 V.

In Figure 3.8, the feedback loop is more prone to ringing when responding to rising than to falling load dumps. This is because L_O requires more time to respond to rising loads. In other words, the bandwidth pole of the current loop is lower, and as a result, closer to the unity-gain frequency f_{0dB} of the loop. Similarly, the ringing worsens as the load step increases from 40 to 180 mA because L_O requires more time to slew across wider load steps. Ringing also worsens as input voltage falls in Figure 3.9 from 1.8 to 1.4 V for the same reason, because with a lower voltage across L_O, i_L slews more slowly.

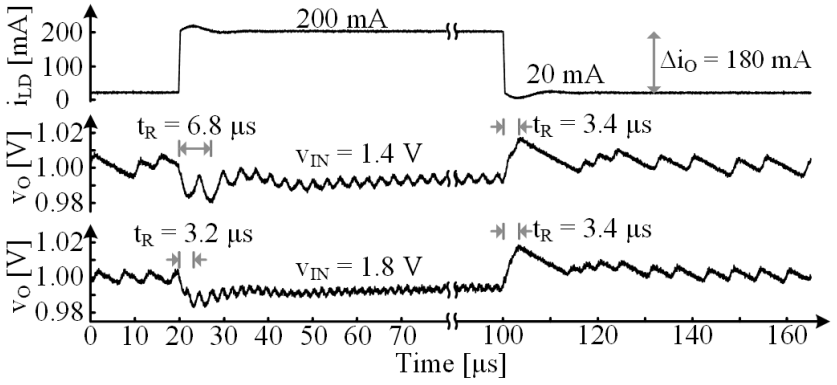


Figure 3.9. Measured response to 180-mA load dump when input voltage v_{IN} is 1.4 and 1.8 V.

3.3 Multiple-Output Hysteretic Current-Mode Design

As in the single output case, the current loop in a multiple-output converter is a hysteretic oscillator that outputs a rippling current i_L about an average current level that the error amplifier A_E sets as Figure 3.10 shows. Each independent output, i.e. v_{O1} through $v_{ON,}$ incorporates a regulating loop that feeds sufficient energy from the inductor to satisfy each load. With A_E, the master loop then adjusts i_L so that the last output v_{OM} receives enough leftover i_L to satisfy v_{OM}'s load. L_O therefore feeds one output at a time, from v_{O1} to v_{OM}.

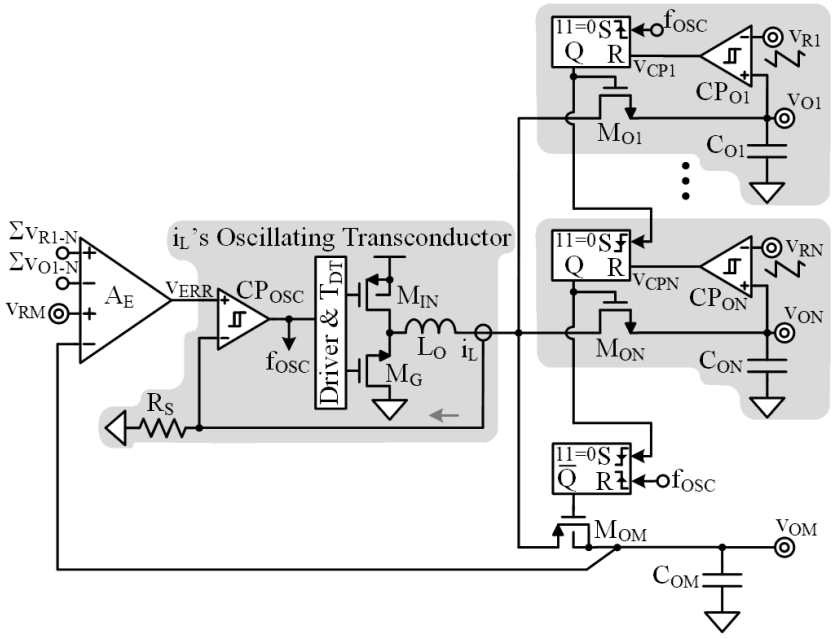


Figure 3.10. Hysteretic current-mode SIMO buck converter.

3.3.1 Operation

The hysteretic control around inductor current i_L in a SIMO converter operates like the single output counterpart. So irrespective of which output L_O feeds, i_L in Figure 3.11 climbs until $i_L R_S$ rises above $v_{ERR,}$ by engaging $M_{IN,}$ by half of comparator CP_{OSC}'s hysteresis v_{HYS}. After that, M_{IN} opens and M_G closes and then drains L_O until $i_L R_S$ reaches CP_{OSC}'s lower

threshold $v_{ERR} - 0.5v_{HYS}$. i_L therefore swings across v_{HYS}/R_S and about v_{ERR}/R_S. And the time that lapses across these events is the oscillating period t_{OSC}.

In the hysteretic SIMO, inductor L_O dictates response time when it slews when responding to a step at the loop's reference v_{ERR}. Contrary to the single output, the voltage across the inductor during slewing depends on the combination of output voltages given a set of load and operating conditions. So, the worst-case inductor voltage $v_{L(MIN)}$ can guarantee stability, with the risk of over compensation and simplify the analysis unless simulations are readily available to interactively determine an effective inductor voltage v_L during response time. At the worst case, lowest bandwidth $f_{IBW(MIN)}$ occurs when delay is longest, or response time $t_{R(MAX)}$, at $\Delta i_{O(MAX)}$ and $v_{L(MIN)}$, which is L_O's lowest possible energizing or drain voltage v_E or v_D:

$$f_{IBW(MIN)} \approx \frac{4}{2\pi}\left(\frac{1}{\Delta i_{O(MAX)}}\right)\left(\frac{v_{L(MIN)}}{L_O}\right). \tag{3.14}$$

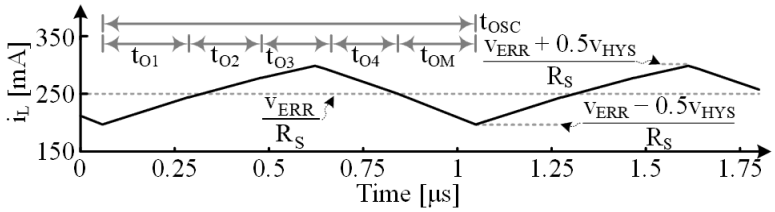


Figure 3.11. Simulated inductor current waveform for an evenly loaded 5-output SIMO.

3.3.2 Independent Loop Analysis

The oscillator starts every cycle by energizing L_O (with f_{OSC} in Figure 3.10) to the first independent output v_{O1} (by way of M_{IN} and M_{O1}). L_O's i_L then charges C_{O1} like Figure 3.12 shows until v_{O1} reaches comparator CP_{O1}'s threshold v_{R1}. At that point, CP_{O1} opens M_{O1} and closes M_{O2} to redirect i_L to the next output. This lets v_{O1}'s load discharge C_{O1} until f_{OSC} reconnects L_O back to v_{O1}. Since identical feedback loops close each independent output

v_{OI}, i_L feeds all outputs like a current source and each independent output voltage v_{OI} ripples and peaks to its respective target v_{RI}.

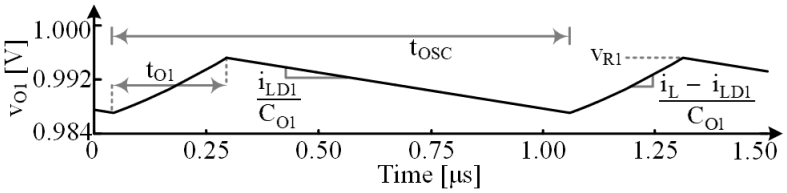


Figure 3.12. Simulated waveform of the first independent output in a 5-output SIMO.

Each independent loop regulates peak voltage like peak-current converters regulate inductor current. Similarly, it can suffer from sub-harmonics if not properly compensated. Figure 3.13 shows how a perturbation $\Delta v_{OI(k)}$ at the beginning of a cycle to a steady state output voltage waveform propagates to the next cycle as $\Delta v_{OI(k+1)}$. An initial perturbation $\Delta v_{OI(k)}$ changes the on time t_{oi} and, with a fixed period t_{OSC}, so will the off time t_{offi} with the amount dictated by the rising and falling slopes of v_{OI}:

$$\begin{aligned}\Delta v_{OI(k+1)} &= \Delta v_{OI(k)}\left(\frac{t_{oi}}{v_{oi(pk)}}\right)\left(\frac{t_{offi}}{t_{oi}}\right)\left(\frac{v_{oi(pk)}}{t_{offi}}\right) = \\ &= \Delta v_{OI(k)}\left(\frac{C_{OI}}{i_L - i_{LDI}}\right)(-1)\left(\frac{i_{LDI}}{C_{OI}}\right) = \Delta v_{OI(k)}\left(\frac{-d_{OI}}{1-d_{OI}}\right)\end{aligned}, \tag{3.15}$$

Where d_{OI} is approximately the ratio of load current to inductor current or i_{LDI}/i_L.

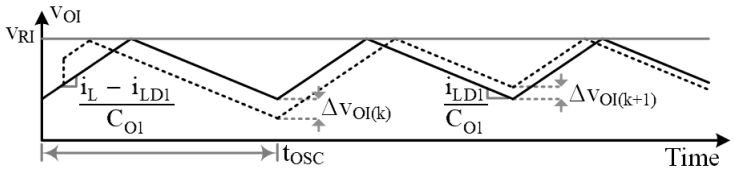


Figure 3.13. Sub-harmonic propagation in peak-voltage regulation of independent outputs.

So, when L_O connects to an output longer than 50% of the period t_{OSC}, small variations grow to produce the subharmonic oscillations in Figure 3.14. But like in peak-current control, adding a ramp [79] to each threshold v_{RI} that shortens L_O's connection to

v_{OI} when responding to loop variations reduces the growth rate of these oscillations. And if the ramp drops at half the falling rate of v_{OI}, which its load i_{LDI} dictates and the maximum load $i_{LDI(MAX)}$ sets to $0.5i_{LDI(MAX)}/C_{OI}$, oscillations disappear for all duty cycles d_{OI}.

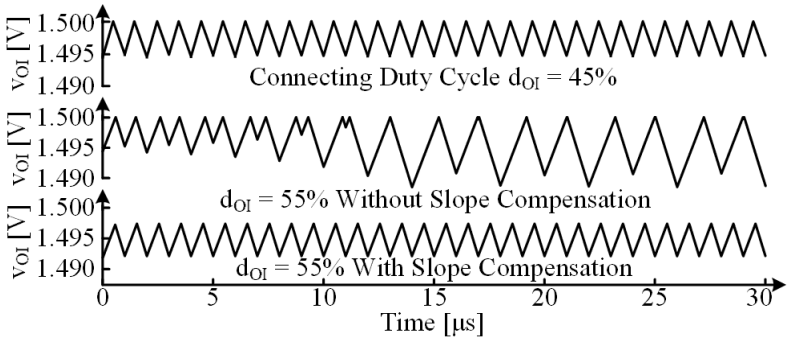


Figure 3.14. Simulated peak-voltage control showing sub-harmonics oscillations and compensated waveform.

Each CP_{OI}, flip-flop, and M_{OI} combination closes a feedback loop that regulates $v_{OI(PK)}$ to v_{RI} like shown in Figure 3.15. So, variations in v_{OI} prompt CP_{OI} to adjust v_{OI}'s connection time t_{OI} and connecting duty cycle d_{OI}. This, in turn, modifies the current i_{LI} that v_{OI} receives. The small-signal loop gain A_{VLG} is therefore the gain from CP_{OI}'s error $v_{oi(pk)} - v_{ri}$ to $v_{oi(pk)}$ via t_{oi}, d_{oi}, and i_{li}:

$$A_{VLG} = \left(\frac{t_{oi}}{v_{oi(pk)}}\right)\left(\frac{d_{oi}}{t_{oi}}\right)\left(\frac{i_{li}}{d_{oi}}\right)\left(\frac{v_{oi(pk)}}{i_{li}}\right) = \\ = \left(\frac{C_{OI}}{i_L - i_{LDI} + 0.5i_{LDI(MAX)}}\right)\left(\frac{1}{t_{OSC}}\right)(i_L)\left(R_{OI} \parallel \frac{1}{sC_{OI}}\right). \quad (3.16)$$

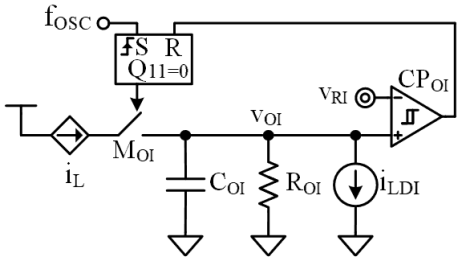


Figure 3.15. Equivalent small-signal model of peak-voltage control of independent outputs.

v_{OI}'s rising and v_{RI}'s falling ramps dictate how soon CP_{OI} ends t_{OI}. Since v_{RI}'s fall into CP_{OI} reinforces v_{OI}'s rise, t_{oi} is the combined slew-rate translation $C_{OI}/(i_L - i_{LDI} + 0.5i_{LDI(MAX)})$ of the error $v_{oi(pk)} - v_{ri}$. L_O connects a t_{oi}/t_{OSC} fraction of the time d_{oi} to deliver with i_{li} a d_{oi} fraction of L_O's current i_L. This current i_{li} into the combined impedance that v_{OI}'s resistance R_{OI} and C_{OI} establish determines $v_{OI(PK)}$'s variation $v_{oi(pk)}$.

C_{OI} sets the only shunting pole p_{OI} at $1/2\pi R_{OI}C_{OI}$ that attenuates A_{VLG} to unity-gain frequency f_{V0dB}. Thus, the product of A_{VLG}'s low-frequency gain A_{VLG0} and its bandwidth p_{OI} is constant and equivalent to f_{V0dB}:

$$f_{V0dB} = A_{VLG0}p_{OI} = \left(\frac{f_{OSC}}{2\pi}\right)\left[\frac{1}{1+\left(0.5i_{LDI(MAX)} - i_{LDI}\right)/i_L}\right]. \tag{3.17}$$

This means A_{VLG} reaches f_{V0dB} with 90° of phase margin. Using the replica circuit time-domain simulation technique in [97] when i_{LDI} is $i_{LDI(MAX)}$, $i_{LDI(MAX)}$ is 20% of i_L, R_{OI} is 10 kΩ, C_{OI} is 4.7 µF, and t_{OSC} is 1 µs, Figure 3.16 shows that A_{VLG0} is 94 dB, f_{V0dB} is 177 kHz, and phase margin is 90°, which matches theory.

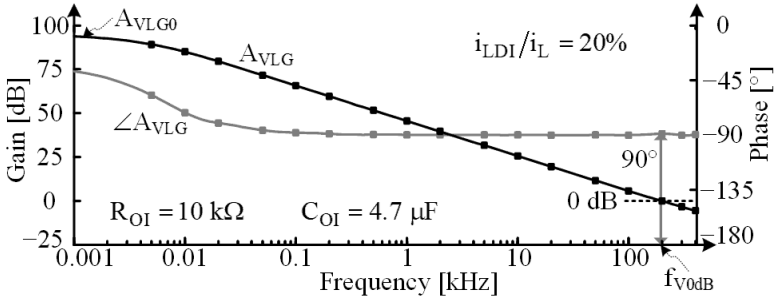


Figure 3.16. Simulated Bode response of peak-voltage control.

Although the analysis uses the hysteretic control scheme for the independent loops regulation to achieve fast dynamic performance, the analysis procedure is applicable to any other control scheme. For instance, if the voltage peak is not effectively being regulated, it

does not require compensation for sub-harmonic oscillations. Also, if required, modulation from voltage error to time can occur with a fixed-slope ramp like PWM control schemes with added frequency shaped amplification for the desired control response.

3.3.3 Master Loop Analysis

For G_{OSC}'s output i_L to behave like a current source within the master loop's bandwidth f_{M0dB}, G_{OSC}'s minimum bandwidth $f_{IBW(MIN)}$ should surpass f_{M0dB}. Irrespective of i_L, however, each independent output sinks a d_{OI} fraction of i_L before connecting L_O to the next output. To v_{OM}, these fractional losses $d_{OI}i_L$ are equivalent to current loads i_{O1}–i_{ON} in Figure 3.17. Stated differently, the bandwidths of the independent loops f_{V0dB} are closer to f_{OSC} and therefore higher than f_{M0dB}, so their closed-loop effects on v_{OM} up to f_{M0dB} are like independent load currents.

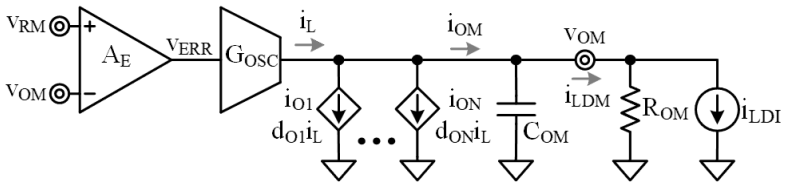


Figure 3.17. Equivalent small-signal model of the master feedback loop.

Although C_{OM} keeps v_{OM}'s ripple Δv_{OM} low, A_E can amplify Δv_{OM} to an extent that i_L's average can also ripple. But since outputs receive i_L at separate times, summing output ripples into A_E, like Figure 3.10 illustrates, tends to produce a ripple-free sum. Since independent loops regulate their outputs near their targets, their small-signal errors in A_E are largely absent. A_E therefore senses v_{OM}'s median error to v_{RM}, as Figure 3.17shows.

A_E and G_{OSC} in Figure 3.10 close a loop that regulates v_{OM} to v_{RM}. For this, A_E senses and amplifies v_{OM}'s error $v_{OM} - v_{RM}$ to adjust the current i_L that G_{OSC} feeds to all

independent outputs and v_{OM}'s load R_{OM} and C_{OM}. The loop gain A_{MLG} is therefore the gain translations across A_E and G_{OSC} to v_{om}:

$$A_{MLG} = A_E \left[\frac{G_{OSC0}}{1 + \frac{s}{2\pi f_{IBW}}} \right] \left(R_{OM} \parallel \frac{1}{sC_{OM}} \right). \tag{3.18}$$

Since this loop's bandwidth f_{M0dB} should precede $f_{IBW(MIN)}$, C_{OM} should shunt well below f_{IBW} to set a pole p_{OM} at $1/2\pi R_{OM}C_{OM}$ that attenuates A_{MLG} to unity at f_{M0dB}. So the product of A_{MLG}'s low-frequency gain A_{MLG0} and its bandwidth p_{OM} is constant and equal to f_{M0dB}:

$$f_{M0dB} = A_{MLG0} p_{OM} = \frac{A_E}{2\pi R_S C_{OM}}. \tag{3.19}$$

p_{OM}'s and f_{IBW}'s phase shifts therefore determine the phase margin left PM_M at f_{M0dB} to the 180° inversion point:

$$PM_M = 180 - \mathrm{Tan}^{-1}\left(\frac{f_{M0dB}}{p_{OM}} \right) - \mathrm{Tan}^{-1}\left(\frac{f_{M0dB}}{f_{IBW}} \right). \tag{3.20}$$

The simulation in Figure 3.18 shows that f_{M0dB} is 191 kHz and PM_M is 83° when A_E is 28 V/V; R_S is 5 Ω; R_{OM} is 10 kΩ; C_{O1}, C_{O2}, C_{O3}, C_{O4}, and C_{OM} are 4.7 µF; i_{O1}, i_{O2}, i_{O3}, i_{O4}, and i_{OM} are 50 mA; and t_{OSC} is 1 µs. PM_M nears 90° because the small-signal simulation cannot account for the large-signal delay that wide load dumps produce. f_{IBW} is therefore close to f_{OSC}, near which switching feedback dynamics reduce PM_M to 83°.

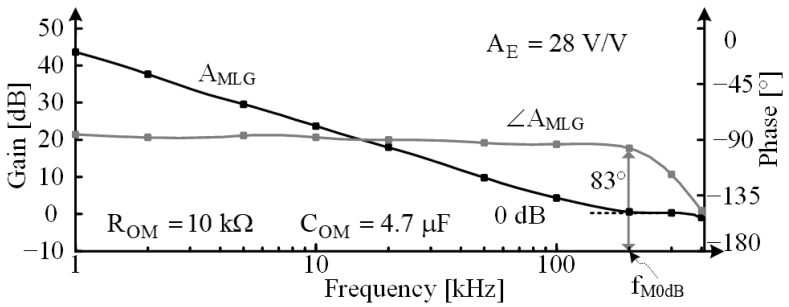


Figure 3.18. Simulated small-signal master feedback's loop gain for a 5-output SIMO.

3.3.4 Five-Output SIMO Validation

For validation, consider a 5-output supply with a 2.7–4.2-V input v_{IN}; 1.00-, 1.25-, 1.50-, 1.75-, and 2.00-V outputs; 100-mA loads; and combined 400-mA load dumps. L_O's drain voltages are therefore v_{O1}'s, v_{O2}'s, v_{O3}'s, v_{O4}'s, and v_{OM}'s 1–2 V. L_O energizes from v_{IN} into these outputs, so L_O's lowest energizing voltages are 0.7–1.7 V. This means, L_O's lowest weighted average voltage $v_{L(MIN)}$ happens when L_O energizes, which from simulations is 0.98 V when evenly loaded.

To keep i_L's ripple at 20% of the highest combined load: at 100 mA, R_S and comparator CP_{OSC}'s hysteresis in Figure 3.10 can be 5 Ω and 500 mV. For i_L to oscillate at 1 MHz when evenly, but half-way loaded and supplied from v_{IN}'s 2.7 V, L_O should be 8.2 µH. This way, 4.7 µF per channel can keep 100-mA loads from rippling outputs more than 20 mV.

The bandwidths of the independent loops f_{V0dB} when evenly loaded are therefore 177 kHz. The oscillating transconductor's minimum bandwidth $f_{IBW(MIN)}$ can be 191 kHz. So, to keep the phase margin of the master loop PM_M above 45°, its bandwidth f_{M0dB} should be no greater than 191 kHz, for which A_E can be 28 V/V. This way, i_L can slew up to $1/f_{IBW(MIN)}$ or 5 µs and independent outputs can recover $1/f_{V0dB}$ or 6 µs after that and v_{OM} $1/f_{M0dB}$ or 5 µs after that.

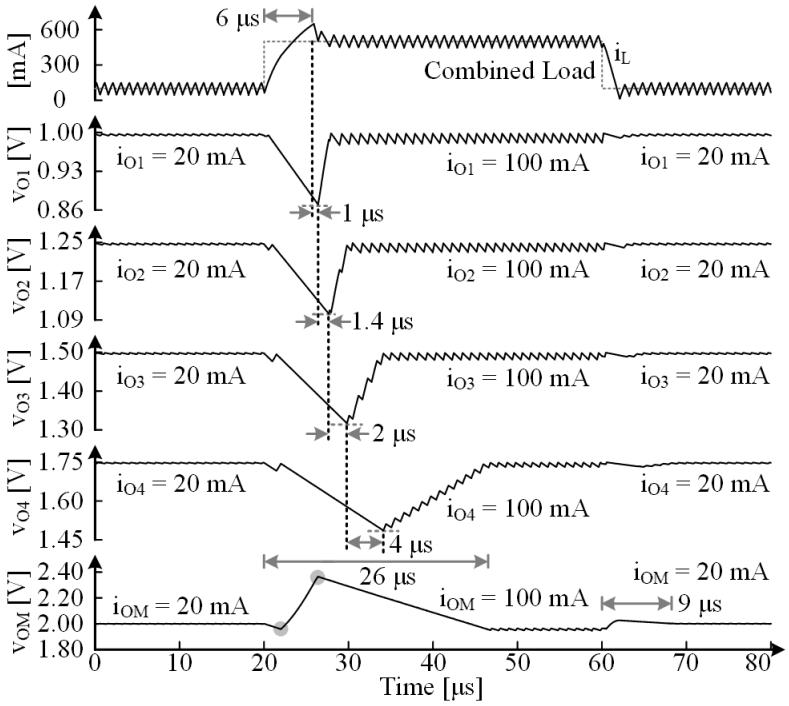


Figure 3.19. Simulated 100-500 mA load-dump response of the 5-output SIMO.

To test this, all loads in Figure 3.19 rise 80 mA in 10 ns at 20 µs. When reaching v_{OM}, the master loop energizes L_O until i_L slews to a level that can supply and replenish all outputs, so v_{OM} overshoots to 2.40 V. v_{O1}–v_{O4} stop drooping within 4 µs of one another and recover within another 12 µs. v_{OM} under- and overshoots like 45° of phase margin would predict [95].

All transitions are faster for the falling load dump at 60 µs because L_O drains with higher voltages than with which L_O energizes. So i_L requires less time to slew and outputs drift less. All outputs therefore recover within 9 µs without under- or overshooting, as 90° of phase margin would predict [95]. So, like theory predicts, i_L slews across $1/f_{IBW}$, independent outputs stop drooping within $1/f_{V0dB}$ of one another, and the last output settles $1/f_{M0dB}$ after the previous outputs recover.

3.3.5 Limitations

Due to the sequential nature of the control, each subsequent output that receives energy will have a slightly higher response time while the previous output recovers like depicted in Figure 3.19. The analysis does not consider this large signal effect during large load steps. Fortunately, as each output responds, it does so stably and with enough phase margin.

Also, to simplify the analysis, it assumed that the master's loop bandwidth is well below the oscillating, or switching, frequency so that its effect in negligible. However, a very high bandwidth can approach the oscillating frequency such that it affects the phase margin by adding phase delay and therefore decreasing phase margin [98]. Thus, to minimize this effect, the design can assume to push the bandwidth about five time lower than the oscillating frequency.

3.4 Summary

Hysteretic converters can react within a switching cycle allowing them to have a good dynamic performance. However, its non-linear control increases the difficulty of designing the control loop, especially when applied on time-variant systems such switched-inductor

converters. In literature, there has been design approaches and equations derived that help but lack to insightfully relate them to circuit operation for an intuitive design. Thus, an intuitive and simple analysis help understand hysteretic control to an easier stable and robust design of hysteretic current mode control for both single- and multiple-output converters.

On the single output converter, the hysteretic current-mode behaves as a relaxation oscillator by constraining the inductor current ripple within a hysteretic window around an average current. The voltage loop adjusts the average current to correct for any voltage regulation error. The current loop can be modeled as a close-loop gain from voltage error to inductor current with a gain and a bandwidth. The feedback gain dictates the low frequency gain while the response time to a step can be used to model its bandwidth with an equivalent linear system that takes the same amount of time to respond. So, because hysteretic control forces the inductor current to slew up or down during a step, the rate in which inductor current increases (or decreases) and the amount it must change determines the response time. Incidentally, the fact that the inductor current slews during the whole response is the reason why hysteretic control enjoys excellent dynamic performance. The model of the current loop can be used to easily find the output capacitance in the voltage loop to stabilize the system with enough phase margin.

The hysteretic control can be applied on the SIMO with additional feedback loops around all output voltages except the last one, or master loop. This locally regulated, or independent, output voltages, bypasses the inductor current, and therefore, are inherently stable with the dominant pole at their output. Hysteretic comparator on the independent

voltages effectively regulate their peak voltages. Like peak current control, this control would suffer from sub-harmonic oscillations which would require compensation. Otherwise, it is a single pole loop with its bandwidth scaling with the oscillating frequency.

The master loop receives the left-over energy from the inductor after all independently regulated outputs. So, it measures the energy need of all outputs to adjust the inductor current to the level that satisfy all outputs. For this reason, the independent loops' bandwidth should be higher than the master's bandwidth to propagate the information quickly to the current loop. Under this condition, the independent loops behave as current loads in the master loop so that all small signal changes in the inductor reaches the master output. In this way, the master loop will be a single-pole and stable system if the current loop or oscillator's bandwidth is at or higher than the cross-over frequency.

The hysteretic current-mode converter design and analysis presented helps to insightfully understand bandwidth limitations and design for a robust and stable system. Moreover, it is scalable and can be applied to any number of outputs in a hysteretic current-mode SIMO converter. Therefore, it helps to design stable hysteretic controlled SIMO for high bandwidth converters ideal for microsystems.

CHAPTER 4

PROPOSED FULLY HYSTERETIC SINGLE-INDUCTOR DUAL-OUTPUT BUCK CONVERTER

The proposed single-inductor dual-output (SIDO) buck converter in this chapter reduces cycling time by supplying all outputs within one energize/drain sequence of the inductor. It shortens response time by using a hysteretic current-mode control to quickly establish the inductor's current to the appropriate level. It also regulates the independently controlled output with a hysteretic comparator to speed its recovery during load dumps. Shortening response time of the control loops reduces the burden on the filtering output capacitors and cross-regulation interactions because outputs are corrected quicker.

4.1 Dual-Output Power Supply

The circuit in Figure 4.1 essentially transforms inductor L_O into an adjustable current source i_L that supplies and responds to the demands of two outputs. So when first energizing L_O, G_{OSC}'s v_{OSC} connects L_O to v_{O1} until comparator CP_{O1} senses that L_O satisfies v_{O1}. L_O then connects to v_{O2}, and if L_O's leftover energy is insufficient or excessive, v_{O2}'s error adjust and tune G_{OSC}'s i_L to meet total load demand. Functionally, G_{OSC} is an oscillating current source that implements the function of the current loop in this current-mode system as analyzed in Chapter 3. CP_{O1} closes the independent voltage loop that ensures v_{O1} peaks near target voltage v_{R1}. Comparator CP_{OSC} mixes and closes the master loop that adjusts G_{OSC}'s current i_L to ensure v_{O2} nears target v_{R2}.

Drivers insert dead times between the conduction periods of adjacent switches M_{IN} and M_G and M_{O1} and M_{O2} to keep them from shorting the input voltage v_{IN}, ground, and v_{O1} and v_{O2}. M_G's and M_{O2}'s body terminals connect to their drains to ensure their body diodes conduct L_O's i_L during M_{IN}–M_G's and M_{O1}–M_{O2}'s dead-time periods. M_G's driver, in conjunction with comparator CP_{ZCS}, also opens M_G when L_O's current reaches zero to keep L_O from conducting negative current. This way, in discontinuous-conduction mode (DCM), M_G does not consume unnecessary ohmic power and output discharge is avoided. M_{O1} is an NFET because v_{IN}'s 2.6–4.2 V is high enough above v_{O1}'s 1.5 V to drive M_{O1}'s gate. Also, the use of an NFET blocks current in both direction when the bulk is grounded; and even though there is a threshold shift, the resistance is the same or lower than a PFET given the same area. M_{O2} is a PFET because ground is similarly low enough below v_{O2}'s 2.5 V to drive M_{O2}'s gate across operating conditions.

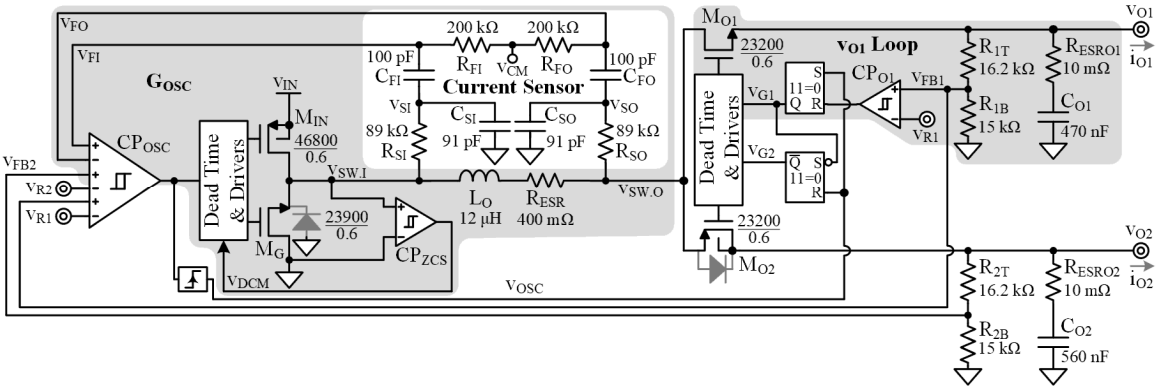


Figure 4.1. Prototyped 0.6-µm CMOS SIDO hysteretic current-mode converter.

The IC includes switches and their drivers, comparators, control and test logic in a 1.4 × 2.0-mm^2 0.6-µm CMOS die as in Figure 4.2. A finer-pitched CMOS process is possible, but also costlier, with lower breakdown voltages, and for proof of concept,

unnecessary. Nonetheless, the concept and limitations presented here also applies for any technology operating within its limits such as breakdown voltage.

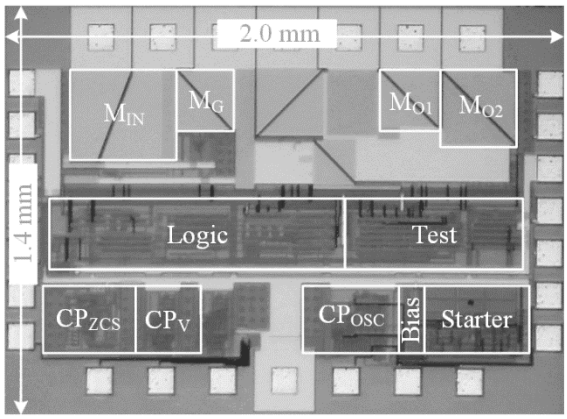


Figure 4.2. Die of prototyped 0.6-µm CMOS SIDO converter.

4.1.1 Operation

Comparator CP_{OSC}, M_{IN}, M_G, L_O, and current sensor implement a relaxation oscillator that ramps L_O's current i_L between the hysteretic limits that CP_{OSC} and equivalent feedback gain R_S from the current sensor establish and about the total output load demand set. For this, CP_{OSC} closes M_{IN} and M_{O1} to energize L_O from v_{IN} to v_{O1} with energize voltage v_{E1} or $v_{IN} - v_{O1}$ until i_L into R_S reaches CP_{OSC}'s upper threshold. Therefore, i_L in Figure 4.3 climbs across energize period t_E. After that, CP_{OSC} opens M_{IN} and closes M_G to drain L_O from ground into v_{O1} with drain voltage v_{D1} or $0 - v_{O1}$, and after i_L satisfies v_{O1}'s load, into v_{O2} with v_{D2} or $0 - v_{O2}$. i_L therefore falls across drain period t_D, first at v_{D1}/L_O and then at v_{D2}/L_O. Current sensor network, with equivalent gain of R_S, senses i_L and translates CP_{OSC}'s hysteresis V_{HYS} into a current. i_L therefore oscillates across V_{HYS}/R_S which sets the ripple Δi_L. Since L_O's voltage determines how fast i_L crosses Δi_L, energize voltage v_E sets t_E, drain voltage v_D sets t_D, and together, they set oscillating period t_{OSC} to:

$$t_{OSC}' = t_E + t_D = \Delta i_L \left(\frac{L_O}{v_E} + \frac{L_O}{v_D} \right) = \left(\frac{V_{HYS}}{R_S} \right) \left(\frac{L_O}{v_E} + \frac{L_O}{v_D} \right). \quad (4.1)$$

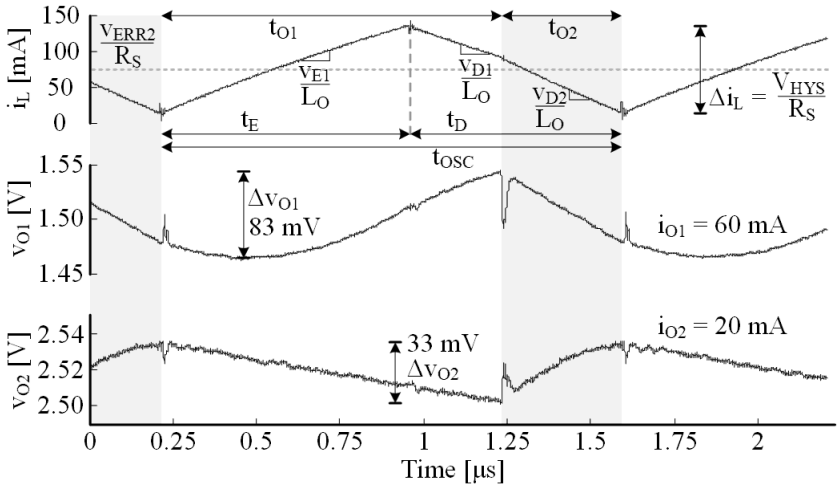


Figure 4.3. Measured steady-state waveform in continuous-conduction mode.

Relative load levels dictate the fraction of time L_O connects to each output. In Figure 4.3, for example, i_{O1}'s 60 mA is 75% of the combined 80-mA load, so v_{O1}'s connection time t_{O1} is roughly 75%, or $i_{O1}/i_{O(TOT)}$, of t_{OSC}, well past L_O's energizing period t_E. As a result, energize voltage v_E is v_{E1} or $v_{IN} - v_{O1}$ and drain voltage v_D is first v_{D1} or $-v_{O1}$ and then v_{D2} or $-v_{O2}$.

Voltage across inductor L_O must be balance and equal to zero in steady-state, otherwise, the current will continuously increase or decrease. For this, the average voltage on the input switching node $v_{SW.I}$ or $d_E v_{IN}$ must equal the average on the output switching node $v_{SW.O}$:

$$d_E v_{IN} = v_{SW.I} \equiv v_{SW.O} = d_{O1} v_{O1} + d_{O2} v_{O2}. \quad (4.2)$$

When i_{O2} is approximately higher than 46% of the combined load when v_{IN}, v_{O1} and v_{O2} are 3.6 V, 1.5V and 2.5 V, v_{O2}'s connection time t_{O2} extends into t_E, so v_E is first v_{E1} or v_{IN}

– v_{O1} and then v_{E2} or v_{IN} – v_{O2}, and v_D is v_{D2} or $-v_{O2}$. This shift in relative connectivity translates to a variation in the oscillating period t_{OSC} and resulting frequency f_{OSC} or $1/t_{OSC}$.

When the combined load is light, the loop lowers the error voltage to the current loop to the point i_L reaches zero before $i_L R_S$ reaches CP_{OSC}'s lower threshold. Once at zero, M_G's driver opens M_G to keep i_L from reversing, so v_{O2}'s load discharges C_{O2} past 1.5 µs in Figure 4.4 until total v_{O2}'s error finally trips CP_{OSC}. In other words, i_L's lower ripple produces an offset $V_{HYS} - \Delta i_L R_S$ that v_{O2}'s fall must overcome to trip CP_{OSC}. This means, i_{O2} reduces v_{O2}'s lower peak when L_O is in discontinuous conduction, from 2.5 V in Figure 4.3 to 2.44 V in Figure 4.4, and i_{O2} extends $t_{OSC,}$ from equation to t_{OSC}':

$$t_{OSC}' = t_{OSC} + t_{DCM} = t_{OSC} + \left(V_{HYS} - \Delta i_L R_S\right)\left(\frac{C_{O2}}{i_{O2}}\right). \tag{4.3}$$

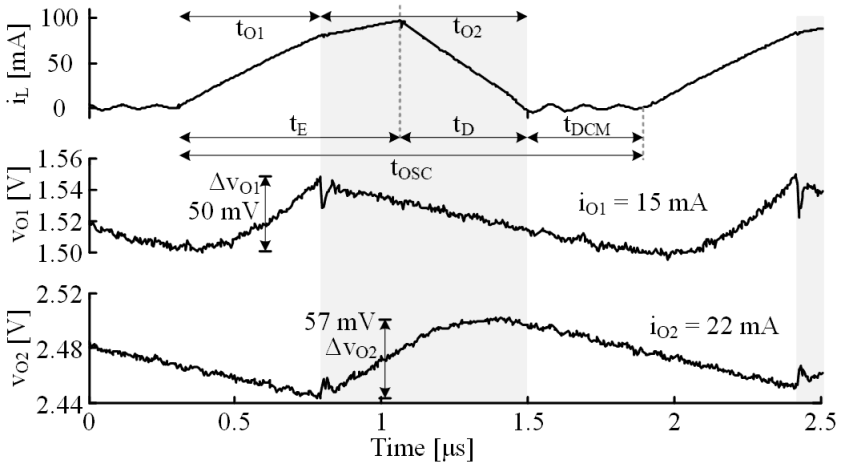


Figure 4.4. Measured steady-state waveform discontinuous-conduction mode.

f_{OSC}, or $1/t_{OSC}$', in Figure 4.5 climbs with i_{O1} (and i_{O2}) until discontinuous time t_{DCM} in Figure 4.4 vanishes, after which t_{OSC}' levels to t_{OSC} and f_{OSC} to $1/t_{OSC}$. Also, when similarly loaded, the frequency is relatively constant in continuous-conduction mode at about 800 kHz. Although the oscillating, or switching, frequency of a hysteretic switching

converter can move or drift, it is deterministic when components values and operating conditions are known [99–100]. For applications that requires an accurate value of switching frequency, techniques exist to stabilize it with feedback and by direct compensation [101–102]. In either case, frequency stabilizers can have a low bandwidth so that hysteretic control maintains its transient performance and the analysis in Chapter 3 still applicable.

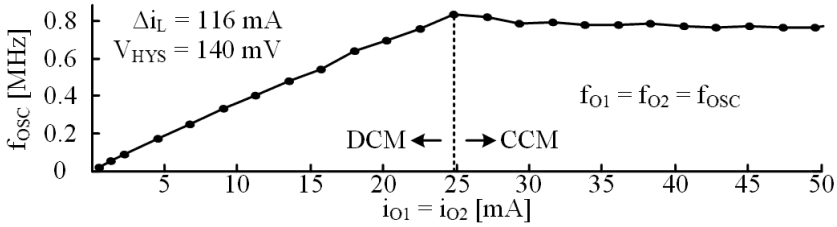


Figure 4.5. Measured oscillating frequency with balanced loads

4.2 Design Implementation

Feedback resistors R_{1T}, R_{1B}, R_{2T}, and R_{2B} in Figure 4.1 translate reference voltages v_{R1} and v_{R2} to v_{O1}'s and v_{O2}'s actual targets of 1.5 and 2.5 V. Comparator CP_{ZCS} opens M_G when i_L into M_G's resistance reaches zero to keep i_L from reversing and push L_O into discontinuous conduction. v_{O1}'s CP_{O1} incorporates hysteresis V_{H1} to keep noise in v_{O1} from inadvertently tripping CP_{O1}. To complete the system, it requires a current sensor and a feedback mixer at the hysteretic comparator CP_{OSC}.

4.2.1 Dead Time Generator and Drivers

The dead time generator and drivers shown in Figure 4.1 drives the power switches M_{IN} and M_G depending if comparator CP_{OSC} commands an energizing or de-energizing event. For this, a chain of inverters with a gain factor from stage to stage implements the drivers

as in Figure 4.6. The gain is such that switches turns fully turns on (or off) in less than 15 ns. This way the turn-on (and turn-off) time is low enough compared to the switching period t_{OSC} to avoid effects from this delays and large enough to minimize power consumption, silicon area, and shoot-through currents of the drivers [79].

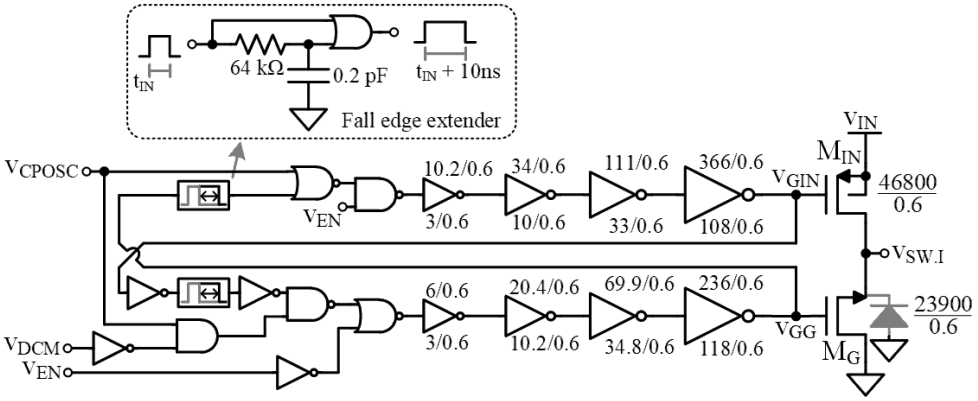


Figure 4.6. Implementation of dead time generator and drivers for the input side switches.

To prevent both M_{IN} and M_G engaging simultaneously and short the supply to ground, a dead time generator is inserted before turning on of any switch. Figure 4.6 implements this by adding a 10-ns delay to the sensed gate voltage and using the resulting signal to disable the other switch. For instance, when output of CP_{OSC} or v_{CPOSC} goes low, it will quickly turn off M_G and want to turn on M_{IN}. However, because M_G was previously engaged, its gate v_{GG} is high and prevents M_{IN} to turn on until M_G completely turns off. After v_{GG} falls, the fall edge extender adds an additional 10 ns for extra margin, after which M_{IN} can safely engaged.

In addition, the logic for the drives, has an enable signal v_{EN} that is held low as the system starts to ensure none of the switches accidentally turns off while control signals settle. It also has a discontinuous conduction mode (DCM) signal v_{DCM} that immediately

turns off M_G when its current reaches zero. This prevents unnecessary losses and allows discontinuous-conduction mode operation.

4.2.2 Current Sensor

For testing purposes, the current sensor is the off-chip filter network in Figure 4.1. Here, R_{SI} and C_{SI} and R_{SO} and C_{SO}, from Figure 4.7, filter L_O and R_{ESR}'s voltage v_L or $v_{SWI} - v_{SWO}$ into voltages v_{SI} and v_{SO} like L_O and R_{ESR} filter v_L into current i_L. It requires a differential current sensing because it must distinguish also when the output switching node changes to accurately mimic the inductor current i_L. Otherwise, the sensed signal would not distinguish when another output connects to the output switching node $v_{SW.O}$ if it only filter $v_{SW.I}$. If both sides of the RC filter have equal values, when $R_{SI}C_{SO}$ and L_O/R_{ESR} time constants match, $v_{SI} - v_{SO}$ is a linear translation of i_L with a gain of R_{ESR} [96]:

$$v_{SI} - v_{SO} = i_L\left(sL_O + R_{ESR}\right)\left(\frac{Z_{CSI}}{Z_{CSI} + R_{SI}}\right) = i_L R_{ESR}\left(\frac{sL_O / R_{ESR} + 1}{sC_{SI}R_{SI} + 1}\right). \qquad (4.4)$$

However, for high efficiency, R_{ESR} must be low which makes the sensed signal small and difficult to discern when accounting for noise. Therefore, $R_{SI}C_{SI}$ is different than L_O/R_{ESR}, such that at least a decade below f_{OSC}, current sense gain R_S reduces to $L_O/R_{SI}C_{SI}$.

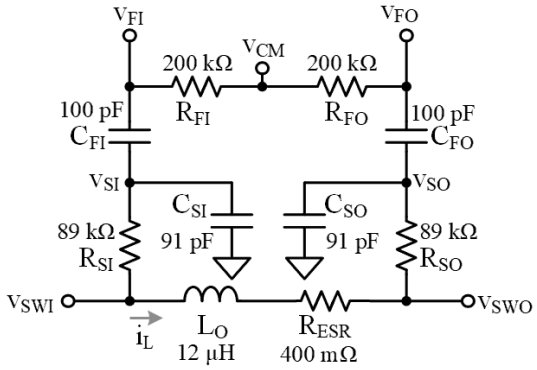


Figure 4.7. Current sensing and filter circuit.

With variations of v_{IN}, v_{O1}, and v_{O2}; averages voltages on either side of L_O can shift which difficult CP_{OSC} to accommodate such wide input common-mode range. C_{FI}–R_{FI} and C_{FO}–R_{FO} high-pass filter v_{SI} and v_{SO} block dc components from propagating to the input terminals of CP_{OSC} but still allowing the sensed i_L without attenuation. v_{CM} is a bias dc voltage that establishes v_{FI} and v_{FO}'s common-mode level. Hence, with an adjustable v_{CM}, v_{FI} and v_{FO} can be within the input common-mode range of CP_{OSC}.

For a simpler implantation, the high-pass filter can be in series with the low-pass filter if it does not load the low-pass filter. For this, the equivalent load of the high-pass filter Z_{HI} must be greater than the equivalent impedance of the low-pass filter Z_{LO} at node v_{SI} or low-pass filter's output:

$$Z_{HI} = R_{FI} + \frac{1}{sC_{FI}} >> Z_{LO} = R_{SI} \| \frac{1}{C_{SI}}. \tag{4.5}$$

Because in this design, Z_{HI} is a minimum of 200kΩ while Z_{LO} is a maximum of 89 kΩ, the inequality is always true and the difference increases past the pole located at $1/(2\pi R_{SI}C_{SI})$. When considering the impedance of the capacitors, Z_{HI} is at least five time larger than Z_{LO}. Hence, the high-pass filter does not significantly load the low-pass filter and a buffer is unnecessary between them.

Summing comparator CP_{OSC} in Figure 4.1 adds $v_{O2} - v_{R2}$ to $v_{FO} - v_{FI}$, where $v_{FO} - v_{FI}$ is the voltage representation of inductor current v_I. But for the system to regulate v_{O2} about v_{R2} accurately, $v_{FO} - v_{FI}$'s dc component should be negligibly low. This is another reason why the differential current sensing helps, to ensure $v_{FO} - v_{FI}$ is near zero at dc and low frequencies. This way, CP_{OSC} and the master loop can keep v_{O2} near v_{R2}.

4.2.3 Summing Comparator

When L_O is in discontinuous conduction, i_L reaches zero before i_L's translation v_I in Figure 4.1 reaches CP_{OSC}'s lower threshold. Assuming only v_{O2}'s error feed CP_{OSC}, v_{O2}'s load therefore discharges C_{O2} until v_{O2}'s droop finally trips CP_{OSC} to start another cycle. When v_{O2}'s load is very light, discontinuous-conduction time t_{DCM} between cycles (from Figure 4.4) is long. Therefore, if v_{O1}'s load suddenly rises, response time t_R is that much longer. Feeding v_{O1}'s error $v_{O1} - v_{R1}$ into CP_{OSC} in Figure 4.1 allows v_{O1}'s error to trip CP_{OSC} sooner for a faster response. In steady state, v_{O1}'s loop keeps v_{O1} near v_{R1}, so $v_{O1} - v_{R1}$ is low at dc. Since $v_{FO} - v_{FI}$ is also low at dc, CP_{OSC} keeps v_{O2} near v_{R2}.

The IC implementation of the summing comparator, shown in Figure 4.8, is based on current summation in a folded cascode multi-stage comparator. It achieves so by summing current from multiple differential input stages including one that sets the hysteresis voltage v_{HYS}. Since all pairs contributes a small signal change proportional to the input voltage differential $v_P - v_N$ or v_D, matching their transconductances with same transistor sizing and tail currents ensures the summation is at the same scale:

$$\begin{aligned} v_{GB} - v_{GA} &= \left[g_{MP1} v_{D1} + \ldots + g_{MP5} v_{D3} + g_{MP7} \left(0.5 v_{HYS} + v_{RH} - v_{RH} \right) \right] \left(\frac{1}{g_{MP9}} \right) \\ &= \frac{g_{MP1}}{g_{MP9}} \left(v_{D1} + \ldots + v_{D3} + 0.5 v_{HYS} \right) \end{aligned} . \quad (4.6)$$

Hence, CP_{OSC} sums and mixes output voltages errors along with the inductor current.

An extra differential pair creates an offset which sets the hysteretic window. Due to the offset across pair M_{P7-8} in Figure 4.8 (a), the total error sum of voltages and inductor current must overcome this offset. When the comparator trips, switches interchange the

drain connections of $M_{P7\text{-}8}$ to create the same offset in the opposite direction effectively implementing a hysteresis. Hence, CP_{OSC}'s hysteresis implementation is symmetric and the reason the differential voltage across $M_{P7\text{-}8}$'s inputs requires half of the target hysteretic window or $0.5v_{HYS}$. Finally, after the low-gain pre-amplifier, the comparator has three more gain stages, two low gain and one high gain as in Figure 4.8 (b), that amplifies the summed voltages into a rail-to-rail signal. The uses of multiple stages with small gain and large gain at the last helps minimize propagation delay with a given current budget [103], [95].

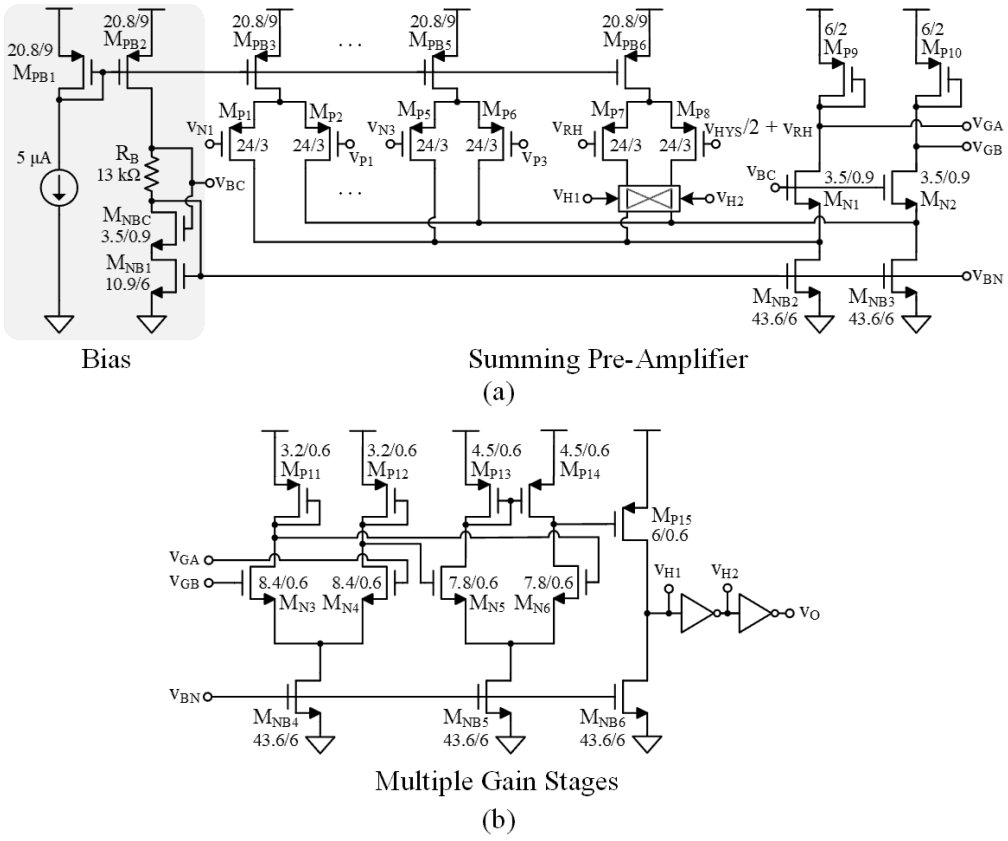


Figure 4.8. (a) Summing pre-amplifier stage and its bias, and (b) multiple stages afterwards of summing comparator CP_{OSC}.

Considering stability, adding v_{O1}'s error at CP_{OSC} creates a feedforward path in parallel to the local loop that may inadvertently increase the total loop gain and extend the bandwidth of independent voltage v_{O1}. It does so by modifying the inductor current through its close-loop gain G_{OSC}, and by v_{O1}'s steady-state duty cycle D_{O1}:

$$A_{VLG(FF)} = \left(\frac{i_l}{v_{o1}}\right)\left(\frac{i_{o1}}{i_l}\right)\left(\frac{v_{o1}}{i_{o1}}\right) = \left(\frac{1}{R_S}\right)\left(D_{O1}\right)\left(R_{O1} \parallel \frac{1}{sC_{O1}}\right). \tag{4.7}$$

For the implemented design, this feedforward gain is low compared to the local independent loop to have a major effect on stability. Thus, error summation helps to accurately regulate v_{O1} under unbalanced loads without compromising stability.

4.2.4 Independent Loop Comparator and Zero Current Detector

Comparator CP_{O1} accurately regulates the peak voltage of independent output v_{O1}. However, to keep regulation with unbalanced loads, allow skipping output voltage during a cycle, and be immune to switching noise it requires a hysteretic window. For this reason, the comparator CP_{O1} implementation in Figure 4.9 engages an asymmetrical hysteretic after the comparator detects v_{O1}'s peak reaches its target. After this transition, CP_{O1} adds a bias current I_{HYS} at the folding node of its pre-amplifier stage (first stage) which sets a hysteresis voltage v_{HYSO1} translated by the input pair transconductance g_{MP1}:

$$v_{HYSO1} = \frac{I_{HYS}}{g_{MP1}}. \tag{4.8}$$

Output voltage v_{O1} must fall below the target voltage by v_{HYSO1} to enable it to receive energy at the next available opportunity, which for v_{O1} is at the beginning of a cycle.

Unfortunately, to discern a large enough signal the hysteresis window must be in the few millivolts range. With the gain of the feedback resistive network, this sets a lower limit to the ripple Δv_{O1} on the independent voltage v_{O1}. Hence the minimum ripple voltage $\Delta v_{O1(MIN)}$ is the amplified hysteretic window v_{HYSO1}, where the gain is set by the inverse of the feedback gain of the resistor network R_{1T} and R_{1B}:

$$\Delta v_{O1(MIN)} = v_{HYSO1}\left(1+\frac{R_{1T}}{R_{1B}}\right) = \frac{I_{HYS}}{g_{MP1}}\left(1+\frac{R_{1T}}{R_{1B}}\right). \tag{4.9}$$

In this design, v_{HYSO1} is set to 5 mV which results in a minimum ripple $\Delta v_{O1(MIN)}$ of 10 mV.

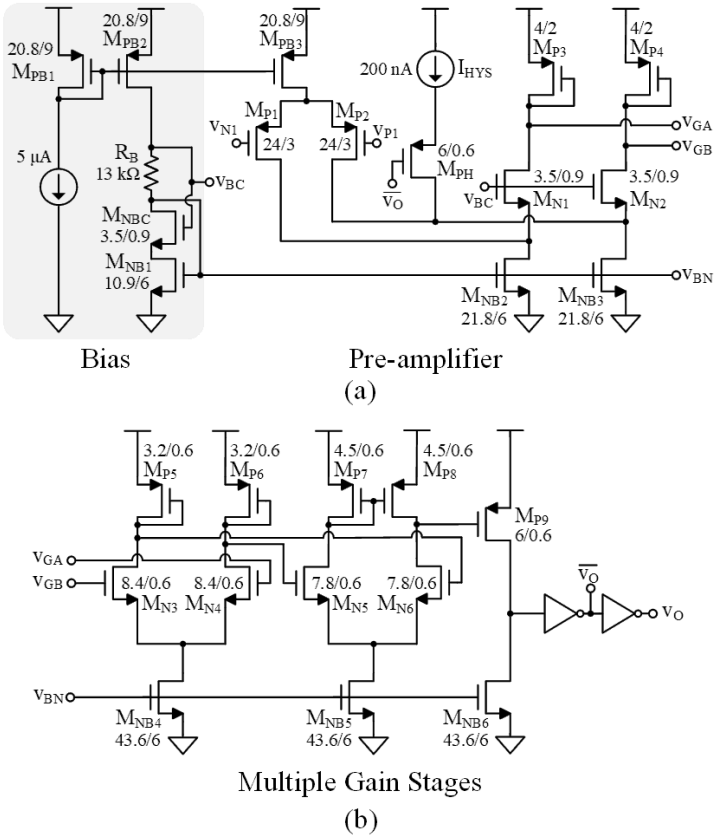


Figure 4.9. (a) Pre-amplifier stage and its bias, and (b) multiple stages afterwards of comparator CP_{O1}.

Like comparator CP_{OSC}, CP_{O1} has three pre-amplifier stages and a high gain stage with inverters to achieve a rail-to-rail output signal. The multi stage approach helps to

minimize delay by keeping high bandwidth in the low gain pre-amplifier so the high gain stage has enough overdrive to quickly drive the output. The first pre-amplifier has a diode-connected PMOS as the active loads to minimize variations across process and temperature ensuring the gain is sufficient to amplify the signal for later stages.

Zero current detector comparator CP_{ZCS} uses a similar topology as CP_{O1}. Its main difference is that it injects hysteresis at the high gain stage instead of the initial stage. Because the CP_{ZCS}'s hysteresis requirements is more relaxed compared to CP_{O1}, it can tolerate more variation due to the gain of the pre-amplifiers stages. Thus, injecting hysteresis at the last stage saves area because matching is not as critical in the last high-gain stage.

4.2.5 Power Management

Resistances, switching gates, and the controller consume ohmic, gate-drive, and quiescent power P_R, P_G, and P_Q. To minimize switches' conduction and gate losses $P_{R(SW)}$ and P_G, transistor channel lengths are minimum at 0.6 μm and widths are wide enough to balance their ohmic and gate-drive losses by minimizing the total power for a given switching frequency f_{OSC} and gate voltage v_G [104]:

$$P_{L(SW)} = P_{R(SW)} + P_G = R_{SW} i_{O(RMS)}^2 + C_G f_{OSC} V_G^2 , \tag{4.10}$$

where

$$i_{O(RMS)} \approx \sqrt{d_O \left(\frac{i_O}{d_O} \right)^2} = \frac{i_O}{\sqrt{d_O}} \approx \frac{i_O}{\sqrt{i_O / i_{O(TOT)}}} = \sqrt{i_O i_{O(TOT)}} . \tag{4.11}$$

Interestingly, the output's RMS current $i_{O(RMS)}$ climbs with the other output load current $i_{O(TOT)}$ since it must receive the same energy in less amount of time as duty cycle shortens. Even for a fixed load i_O, the pulsed current through the switch is narrower with a proportionally higher amplitude, and hence higher RMS current.

This way, L_O's series resistance 400 mΩ and other ohmic losses in P_R climb in Figure 4.10 with load power from nearly zero to 22 mW, when the combined load is 200 mW. Logic and other gate-drive losses in P_G rise with f_{OSC} from Figure 4.5 in discontinuous conduction and flatten past 96 mW, when f_{OSC} settles in continuous conduction. CP_{OSC}, CP_{O1}, and CP_{ZCS} dissipate about 2 mW as P_Q across load levels.

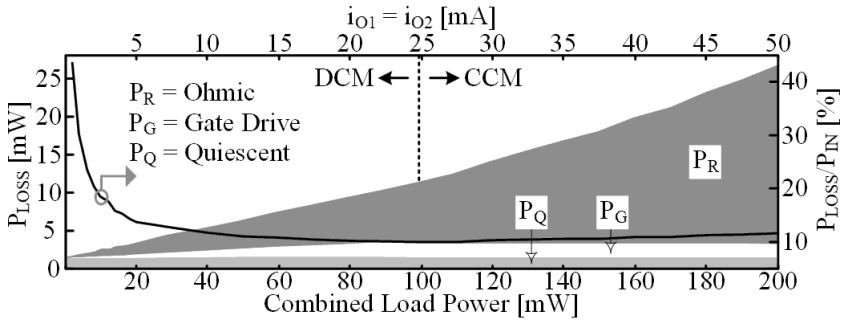


Figure 4.10. Simulated power losses with balanced losses.

4.3 Measured Performance

The hysteretic current-mode converter must be assessed and evaluated with an appropriate test setup. The test sweep should explore output regulation when loads are similar and with unbalanced conditions. Also, the response to load dumps must be carefully measured for fast responding converters because bandwidth and/or delays of the test setup may alter the measured performance.

4.3.1 Test Setup

Load emulation needs special consideration for fast responding converters. If the rising and falling edges of the load steps are not faster than the converter, the voltage response is optimistic as the controller start reacting in the middle of the transition and not at the worst case, when the load has settled [105–106]. For sub 10-µs response times, the edges of the load step should be ideally less than 1µs, and although switching a resistor might achieve so, it models the whole output load as resistive. To have the flexibility of an arbitrary current shape with desired output resistance such as for a mixed load that contains resistive and current source loads, Figure 4.11 shows a high-bandwidth current regulator with a load resistance R_{LD}.

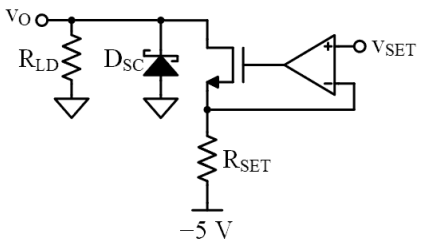


Figure 4.11. Flexible high-bandwidth load emulation circuit.

It consists of a high bandwidth amplifier, such as Texas Instruments' OPA747, regulating the voltage across current-setting resistor R_{SET} through a small-signal transistor, such as On Semiconducot's NTR4003N. To accommodate and regulate to low output voltages v_O, a –5 V is used as the reference instead of ground to circumvent headroom limitations. This is the reason a Schottky diode D_{SC} is necessary to protect the device under test if regulation is lost by limiting v_O just below ground. This circuit can achieve rising or falling edge time of around 100-300 ns for a 1 V amplitude input stepped signal at v_{SET} referenced to –5 V.

Figure 4.12 shows the two-layer PCB board used for evaluation, which including the current sensor and feedback resistors for testing flexibility. L_O occupies 3.5 × 2.7 × 2.4 mm^3 of the board shown and incorporates 400 mΩ of equivalent series resistance R_{ESR}. C_{O1} and C_{O2} each occupy 1.6 × 0.81 × 0.91 mm^3 and incorporate 10 mΩ of series resistance. The test circuits in Figure 4.12 allow to change test modes, move reference voltages, adjust hysteretic voltage for CP_{OSC}, and components for current measurements. The PCB board has dimensions of 15.6 cm × 10 cm or roughly 6.1 in. × 4 in.

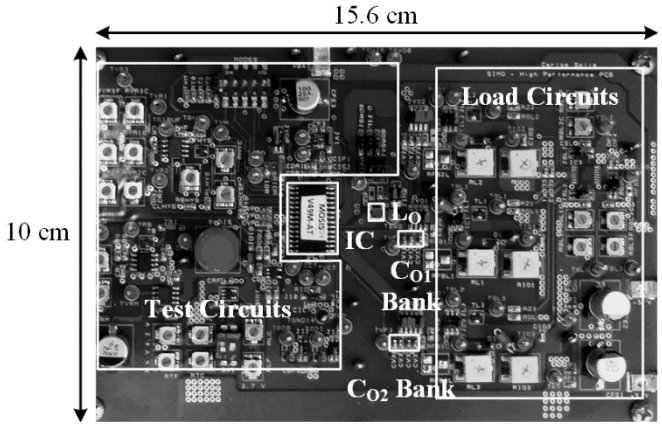


Figure 4.12. Two-layer board for prototype testing.

4.3.2 Regulation with Balanced Loads

A starting point for evaluation of the proposed dual-output converter is to have both outputs equally loaded within their respective load range. This way, the converter is characterized from the lowest loading to the full-load condition. It also decouples possible issues or operation variations to when loads are unbalanced because each output might not receive energy every cycle.

4.3.2.1 Steady State

Since v_{OSC} connects L_O to v_{O1} and comparator CP_{O1} disconnects L_O from v_{O1} when v_{O1} rises to v_{R1}, CP_{O1} keeps v_{O1}'s peak near v_{R1}. After, v_{O1}'s load droops v_{O1} across what remains of t_{OSC} after v_{O1}'s connection time t_{O1} lapses. So as i_{O1} and i_{O2} together climb above 25 mA in Figure 4.13, v_{O1}'s bottom and average levels droop to lower levels:

$$v_{O1(AVG)} = v_{R1} - v_{LR} = v_{R1} - \left(\frac{i_{O1}}{2}\right)\left(\frac{t_{OSC} - t_{O1}}{C_{O1}}\right). \tag{4.12}$$

Also, noticeable in Figure 4.13, the regulated peak of v_{O1} varies slightly with load. Because CP_{O1} has finite delay, and v_{O1}'s rising rate increases with either higher i_L or low load i_{O1}, v_{O1}'s peak shift higher above or below when both loads are 25 mA.

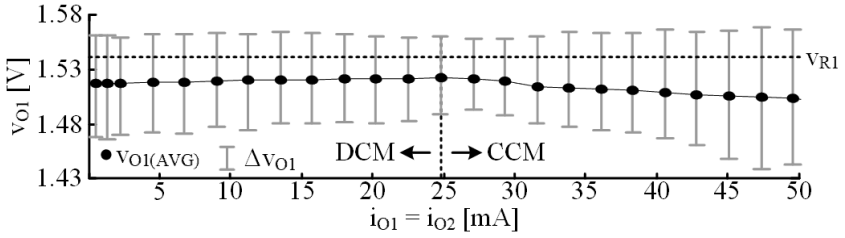


Figure 4.13. v_{O1}'s measured load regulation with balanced loads.

In discontinuous conduction, when i_{O1} and i_{O2} are both below 25 mA in Figure 4.13, raising v_{O2}'s load reduces discontinuous time t_{DCM} in Figure 4.4, which shortens t_{OSC} and the time v_{O1}'s load discharges C_{O1}. As a result, t_{OSC}'s reduction counters the effect of i_{O1}'s rise on v_{O1} to produce less variation in v_{O1}'s low and average values. This means, load regulation is worse in continuous conduction as load increases.

Since the master loop adjust G_{OSC}'s i_L, v_{O2}'s average $v_{O2(AVG)}$ in Figure 4.14 is near v_{R2}'s 2.5 V when L_O is in continuous conduction and both load currents are above 25 mA. Below 25 mA, when L_O is in discontinuous conduction, i_L reaches zero before $i_L R_S$ reaches CP_{OSC}'s lower threshold. v_{O2}'s load therefore continues to discharge C_{O2} until v_{O2}'s error

overcomes the difference. Thus, v_{O2} drops, and as the loads continue to lighten, i_L's ripple diminishes and v_{O2} falls further.

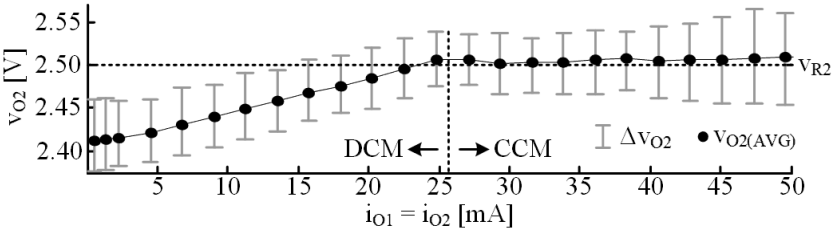


Figure 4.14. v_{O2}'s measured load regulation with balanced loads.

4.3.2.2 Load Dumps

Response time t_R in power supplies sets how long load dumps slew their outputs. So after a rising load dump $+\Delta i_{O1}$, the difference between the load and i_{O1} (which is equivalent to Δi_{O1}) discharges C_{O1} across t_R to produce a falling variation $-\Delta v_{LD}$ in v_{O1}. After a falling load dump $-\Delta i_{O1}$, the difference between i_{O1} and the load (which is equivalent to Δi_{O1}) charges C_{O1} to produce a similar rising variation $+\Delta v_{LD}$. Unfortunately, these load dumps are often fast and wide, so $\pm\Delta v_{LD}$ can be ±7% to ±10%, high enough to overwhelm other effects and to, alone, limit a supply's accuracy [79]. This worsens when several outputs share one inductor because cycling between outputs extends t_R.

In this case, v_{O1}'s load regulation $-\Delta v_{LR}$ from Figure 4.13 is significant by design. Δv_{LR}, however, does not affect $v_{O1(MIN)}$ because a fast-rising load dump normally pulls v_{O1} well below $v_{R1} - \Delta v_{LR}$ to $v_{R1} - \Delta v_{LD}$. But since a falling load dump raises v_{O1} from its loaded level $v_{R1} - \Delta v_{LR}$, $-\Delta v_{LR}$ counters $+\Delta v_{LD}$ to reduce $v_{O1(MAX)}$ to $(v_{R1} - \Delta v_{LR}) + \Delta v_{LD}$. In other words, load regulation mitigates the effect of the falling load dump [107]. So adding a positive offset v_{OS} to v_{R1} that is similar, but opposite in magnitude to $-\Delta v_{LR}$ can

reduce $v_{O1(MIN)}$ to $v_{OS} - \Delta v_{LD}$, and when v_{OS} matches Δv_{LR}, reduce v_{O1}'s total variation $\Delta v_{O1(MAX)}$ to

$$\Delta v_{O1(MAX)} = v_{O1(MAX)} - v_{O1(MIN)} = \pm\left|\Delta v_{LD} - \Delta v_{LR}\right|. \tag{4.13}$$

Therefore, v_{R1} is slightly above 1.5 V and v_{O1} in Figure 4.15 and Figure 4.16 ripples about 1.5 V when loaded with 50 mA.

During a simultaneous rising load dump of 45 mA for both channels, the converter recovers within 3 µs at which point v_{O2} stops falling as capacitor C_{O2} starts being replenished as in Figure 4.15. v_{O1} regulates with an accuracy of ±78 mV or ±5% about 1.5 V. v_{O2} undershoots up to 140 mV for an accuracy within ±6% of 2.5 V.

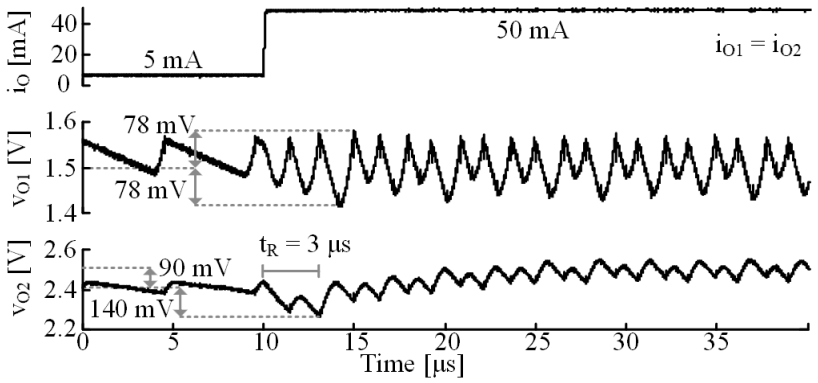


Figure 4.15. Measured response to simultaneous rising 45-mA load steps.

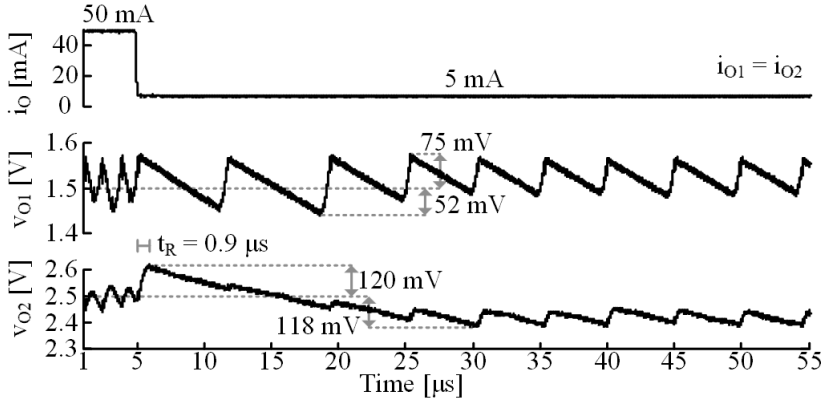


Figure 4.16. Measured response to simultaneous falling 45-mA load step.

The controller responds faster to a falling load dump because the de-energizing voltage of L_O is higher and i_L slew faster to the new target. As in Figure 4.16, the control reacts within 1 μs as v_{O2} overshoots about 120 mV. v_{O1}'s ripple decreases without any overshoot during the load dump because the local loop can accurately regulate the peak voltage. Also, v_{O2} slews down as it recovers as load discharges C_{O2}; hence, both sets the settling time after a falling load dump.

4.3.3 Regulation under Unbalanced Loads

In certain applications, such as microsystem some blocks or functions might turn off to save energy in the system as explained in Chapter 1. This means, that the converter must supply each output different power levels even when one load is fully engaged and the other are in idle or turned off. This can create unbalanced load conditions where the converter must regulate both outputs while dedicating more time on the heavily loaded output.

For good regulation performance, the system should be able to skip outputs that do require less energy as when lightly loaded. In this way, an output does not receive excessive energy until the load has discharge the output capacitance enough. Therefore, v_{O1}'s flip-flop in Figure 4.1 does not set when both set and reset signals are high. This way, if CP_{O1} senses v_{O1} is already near or above v_{R1}, v_{OSC} cannot set M_{O1}'s flip-flop to connect L_O to v_{O1}. CP_{O1} inherently senses if v_{O1} need energy through its hysteretic window. The flip-flop's low output therefore sets v_{O2}'s flip-flop to close M_{O2} and connect L_O to v_{O2}.

Skipping v_{O2} is more natural because, when v_{O1}'s load is much greater than v_{O2}'s load, L_O's energy per cycle is not enough to satisfy v_{O1}'s load. Thus, v_{O1} does not reach v_{R1} until the next or following cycles. Extending v_{O1}'s connection time t_{O1} to t_{OSC} this way keeps L_O from connecting to v_{O2} across that cycle.

4.3.3.1 Steady State

When v_{O2}'s load is constant, at 25 mA for example, and v_{O1}'s load exceeds 7 mA, i_{O1} is high and close enough to i_{O2} for v_{O1} to demand current every oscillating cycle. Therefore v_{O1}'s switching frequency f_{O1} and v_{O2}'s f_{O2} in Figure 4.17 (black traces) match i_L's oscillating frequency f_{OSC} above 7 mA when i_{O2} is 25 mA. L_O starts skipping v_{O1} when i_{O1} falls below 7 mA, when one cycle is enough to satisfy v_{O1} for two cycles. Moreover, when v_{O1}'s load i_{O1} falls below 1 mA, the system skips v_{O1} an additional cycle. Thus, f_{O1} falls below f_{O2} for low levels of i_{O1}.

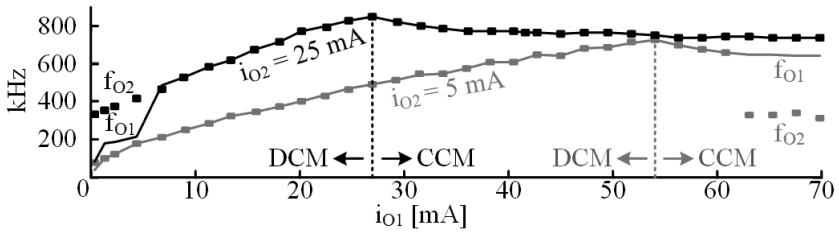


Figure 4.17. Outputs' switching frequencies across unbalanced load levels.

Similarly, when i_{O2} is 5 mA and i_{O1} is less than 60 mA, i_{O2} is close enough to i_{O1} for v_{O2} to demand current every cycle. f_{O1} and f_{O2} in Figure 4.17 (gray traces) therefore match i_L's f_{OSC} below 62 mA when i_{O2} is 5 mA. L_O starts skipping v_{O2} above 62 mA because v_{O1}'s demand is so much greater than v_{O2}'s that v_{O1}'s load sinks L_O's i_L continuously across multiple cycles. In this case, v_{O2} receives i_L every other cycle.

Skipping an output will cause their switching frequencies to differ and therefore their harmonic content. To set a benchmark of the frequency spectrum, Figure 4.18 and Figure 4.19 respectively show the frequency spectrum of outputs v_{O1} and v_{O2} with balanced loads of 80 mA and 48 mA. Both shows the same switching frequency of 793 kHz at its harmonics with their magnitudes decreasing in a comparable way.

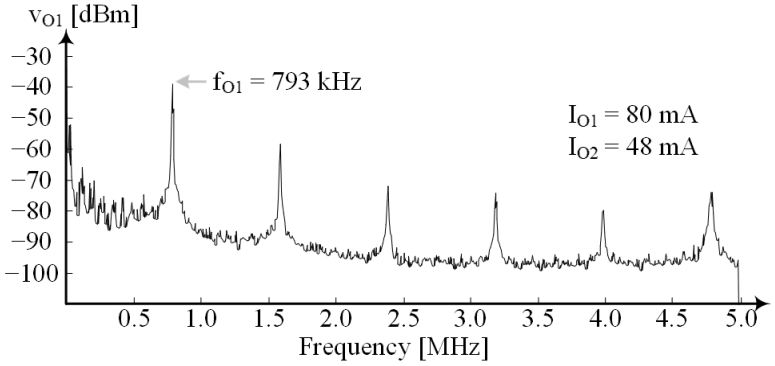


Figure 4.18. Frequency spectrum of output v_{O1} with balanced loads.

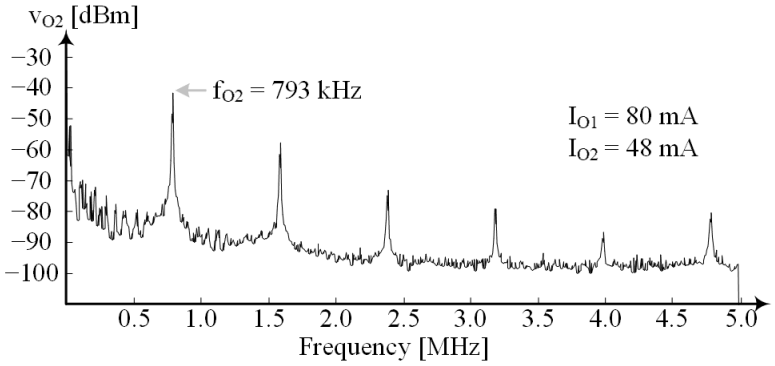


Figure 4.19. Frequency spectrum of output v_{O2} with balanced loads.

With unbalanced load, such as when v_{O1} has a much lower load than v_{O2}, the control skips v_{O1} every other cycle. That is why Figure 4.20 shows its dominant frequency, or switching frequency f_{O1}, of 312 kHz which decreases at a rate of approximately 8 dBm or about a decade in power for every harmonic. On the other hand, output v_{O2} receives energy every switching cycle: one whole cycle and partially when v_{O1} receives energy.

Accordingly, Figure 4.21 shows two frequencies, one at 312 kHz and its second harmonic with only a 0.7 dBm difference on their strength. The first harmonic accounts for the fundamental frequency of receiving energy every other cycle, and the second harmonic to account for the fact that every switching cycle, v_{O2} receives energy. Also, note that the fundamental frequency changes when compared to the balanced load condition because the fraction that each output is connected to the inductor changes.

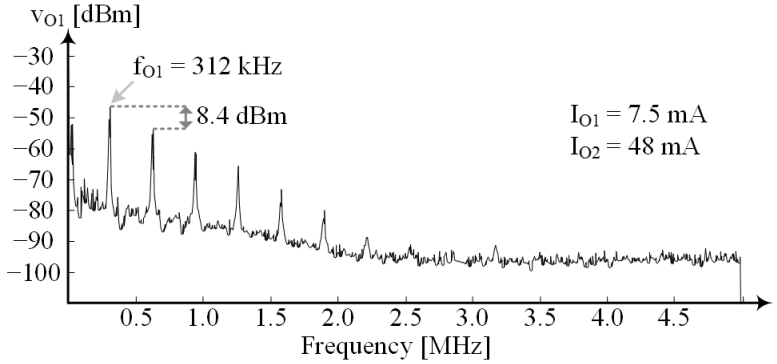


Figure 4.20. Frequency spectrum of output v_{O1} with unbalanced loads.

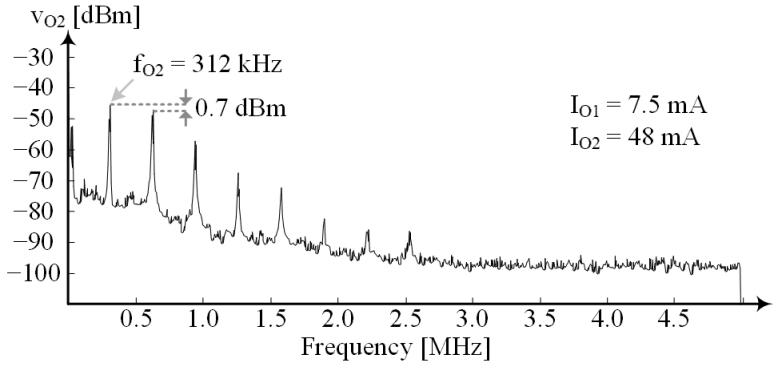


Figure 4.21. Frequency spectrum of output v_{O2} with unbalanced loads.

4.3.3.2 Load Dumps

When v_{O1}'s load i_{LD1} suddenly rises to a vastly higher level, L_O's initial current cannot satisfy the higher load. CP_{O1} and the flip-flops in Figure 4.1 therefore skip v_{O2} until i_L satisfies i_{LD1}. As a result, load dump Δi_{LD1} droops v_{O1}, like Figure 4.22 shows, and v_{O2}

indirectly. And because v_{O2} does not receive energy until L_O satisfies v_{O1}, v_{O2} recovers after v_{O1} does. But since G_{OSC}'s hysteretic loop responds within CP_{OSC}'s and drivers' combined propagation delay, i_L rises quickly to recover v_{O1} within one oscillating cycle and recover v_{O2} 3.8 µs after v_{O1}'s load dump when oscillating frequency is 760 kHz.

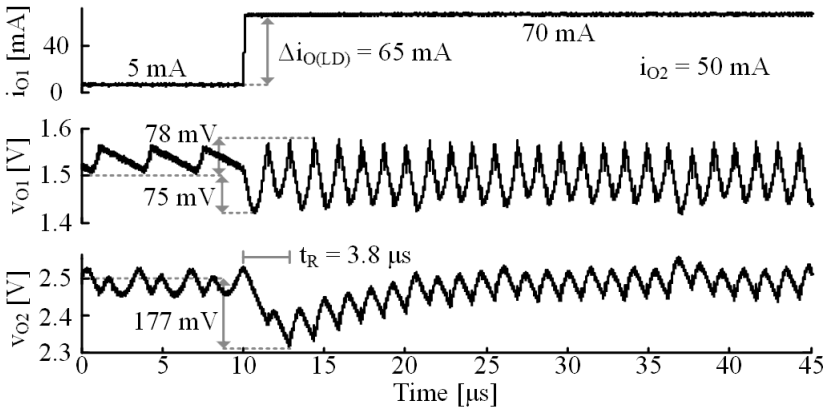


Figure 4.22. Measured response to a rising 65-mA load step at v_{O1}.

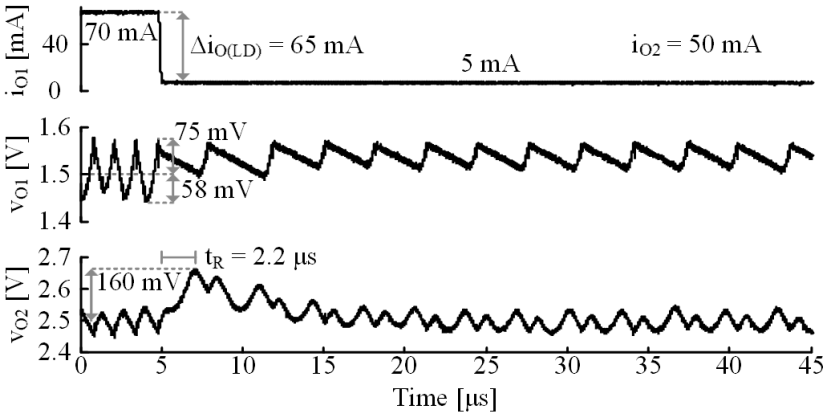


Figure 4.23. Measured response to a falling 65-mA load step at v_{O1}.

When a heavy load suddenly disappears from v_{O1}, CP_{O1} disconnects L_O from v_{O1} quickly enough to keep v_{O1} in regulation. L_O's excess current, however, charges C_{O2} above v_{O2}'s target v_{R2}, like Figure 4.23 demonstrates. Like before, though, CP_{OSC} respond quickly to recover v_{O2} 2.2 µs after v_{O1}'s falling load dump. In other words, v_{O1}'s rising and falling

load dumps, for the most part, only affect v_{O2}, but the hysteretic loop is fast enough to recover v_{O2} within 3.8 µs.

Since the system always satisfies v_{O1} first, fast and wide load dumps at v_{O2} induce little to no effects on v_{O1}. v_{O2}'s rising load dumps in Figure 4.24, for example, lower v_{O2} out of regulation, but not v_{O1}. The control keeps supplying energy to v_{O1} first before delivering energy to v_{O2} as it recovers in 3 µs. This results in v_{O1} having the same ripple voltage before and after the load dump.

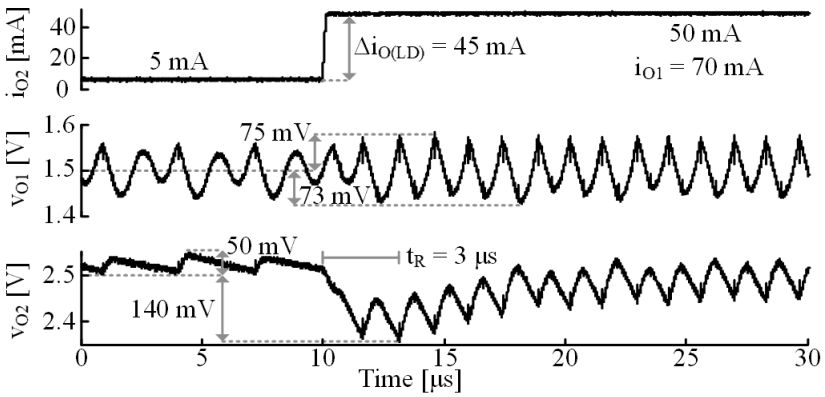


Figure 4.24. Measured response to a rising 45-mA load step at v_{O2}.

Similarly, v_{O2}'s falling load dumps in Figure 4.25 raises v_{O2} during the response of 2 µs. As v_{O2} decays, the control continuously provides energy to v_{O1} and skips v_{O2} until v_{O2} requires energy again. That is why v_{O1}'s ripple is lower as v_{O2} droops than when it reaches steady-state since it received a continuous current as opposed to pulsed.

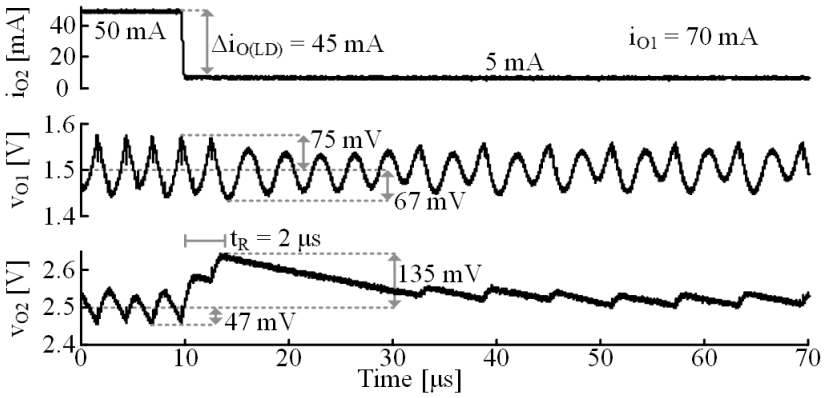


Figure 4.25. Measured response to a falling 45-mA load step at v_{O1}.

4.3.4 Efficiency

Like Figure 4.26 shows, power-conversion efficiency η_C peaks at 88% when i_{O1} is 25 mA and i_{O2} is 43 mA, when the combined load is 145 mW. η_C remains above 85% when i_{O2} pulls at least 25 mA or 62 mW and above 80% when i_{O2} pulls more than 5 mA or 13 mW. η_C is generally higher when i_{O2} is greater than i_{O1} because M_{O2}'s current–voltage overlap loss is lower. This is because M_{O2}'s initial voltage when it shorts is about 0.65 V (across its body diode) and M_{O1}'s is about 1.65 V (between v_{O1} and v_{O2} and M_{O2}'s body-diode voltage).

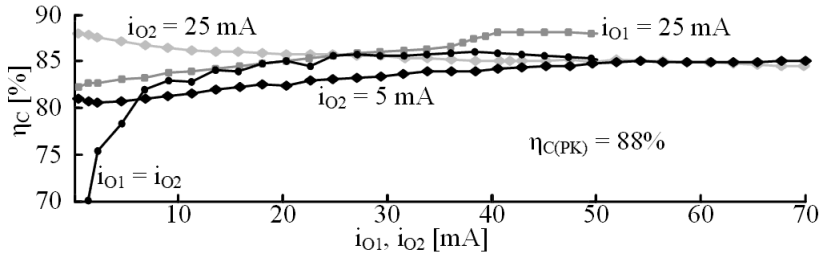


Figure 4.26. Measured power-conversion efficiency across load levels.

4.4 State-of-the-Art Comparison

As explained in section 2.3 from Chapter 2, a figure of merit (FoM) helps to compare unique designs across technologies by weighting tradeoffs and performance metrics. Using equation 2.3, the design presented has a 93% relative FoM (RFoM) compared to the best

available SoA in control for SIMOs. Table 4.1 summarizes performance metrics of the SoA and the system discussed in this chapter.

Table 4.1. SoA Comparison of Control schemes for SIMO Converters.

	Unit	[58]	[55]	[65]	[77]	[69]	[72]	[73]	This Work
Notes		Dedicated E-Packet	Hybrid	Fully PWM	Fully PWM	Fully PWM	Fully PWM	Fully PWM	Fully Hysteretic
L_{MIN}	μm	0.5	0.35	0.25	0.04	0.055	0.5	0.065	0.6
A_{SI}	mm^2	2.4	3.84	5.29	4.00	0.98	4.40	1.86	2.80
v_{IN}	V	1.3− 2.85	2.7− 3.3	2.7− 5	2.7− 3.6	2.7− 3.6	1.2− 2.2	3.4− 4.3	2.6− 4.2
v_O	V	3, 3.6	1.2, 1.8	1.2, 1.8	1.1− 2.25	1.8, 1.2	3.0, 2.5	1.2− 2.8	1.5, 2.5
$i_{O(MAX)}$	mA	170[2]	200	600	900	600	100	1150	120
N_O	#	2	2	2	4	2	2	5	2
N_{OC}	#	3	3	4	5	3	3	6	3
t_R	μs	20[2]	2[1]	15[2]	40[2]	8[2]	5[2]	12[2]	3.8
$\eta_{C(PK)}$	%	88	83	87	89	91	81	83	88
$\eta_{C(FL)}$	%	72[2]	72[2]	80[2]	86[2]	83[2]	80[2]	83[2]	85
RFoM	%	21	100	18	4	58	27	53	93

[1]Uses linear regulator, [2]Estimated from reported measurements.

The work presented has a higher RFoM than [58], [65], [77], and [73] because their response times are higher than 10 μs versus a 3.8 μs of the proposed converter. Also, although [73] only has 12 μs of response time, it only has peak conversion efficiency $\eta_{C(PK)}$ to a 83% while [58]'s and [65]'s full load efficiency $\eta_{C(FL)}$ drops to 72% and 80% respectively compared to the proposed converter at 85%. Work from [69] achieve 8 μs and has a third of the area but uses a 10x smaller technology node which increases cost. [72]'s

response time of 5 µs is close to the proposed design's 3.8 µs. However, even though it uses a similar technology node, it occupies 57% more area and has 7% less peak efficiency $\eta_{C(FL)}$.

Work from [55] has a 7% higher RFoM to the propose design thanks to its fast response time because it combines a linear regulator, that handles transient events, with a SIMO. This is why it occupies 37% higher area A_{SI} even though that uses an almost half-size technology node as compared to the proposed SIMO. [55]'s efficiency drops at full load to 72% because it uses a dedicated energy packet transfer scheme and the lossy linear regulators can supply a small fraction of the output load at steady-state as it tries to counteract the ripple. Because all performance metrics are equally weighted the advantages of the proposed control balances with the disadvantages of [55]. The proposed would serve best for compact microsystems where efficiency across a wide load range is of utmost importance with the fastest response time without the aid of linear regulators to minimize silicon real estate.

4.5 Limitations

A limitation of the control is caused by the mixing at the summing comparator CP_{OSC}. Because summing comparator sums all output voltages errors, load regulation at the independent output will be reflected as an offset in the opposite direction at the master loop. If the master loop's error is not amplified as in this design, master loop can have the same load regulation, but opposite direction, as the other output.

Also, as discussed above, CP_{O1}'s hysteresis window sets a minimum ripple at the output voltage. Unfortunately, this limits how much the output can be filter with

capacitance to be able to allow the output to receive energy at every switching cycle under nominal conditions and balanced loads. This is the main reason the proposed design has more ripple voltage that the state of the art despite responding quickly to load dumps.

4.6 Summary

To improve bandwidth and response time to load dumps, the proposed design uses a fully hysteretic current-mode control. It was fabricated in a 0.6 μm CMOS technology and can regulate two outputs. The control first delivers energy, if needed, to the independent output voltage that has its own local loop and after it receives enough energy, the last output, or master output, receives energy for the reminder of the period. It requires two hysteretic comparators, a current sensor, a zero-current sensing comparator for discontinuous mode operation, and switches and their drivers.

The external current sensor, for testing purposes, uses a differential RC filter that generates a scaled version of the inductor current. A series high pass filter blocks the wide range dc voltage from the switching nodes and therefore, alleviates the input common-mode range requirements of the summing comparator. Incidentally, the summing comparator, besides mixing the error from the master loop with the inductor current information, also mixes error information from the independent voltage. This provides a low-gain feedforward path in the control loop of the independent voltage and improves regulation under unbalanced conditions specifically when the master is lightly loaded.

A hysteretic comparator regulates the peak voltage of the independent output voltage and hence has load regulation as its load increases. This means that the average voltage will decrease with load. However, if an offset is induced in the reference voltage,

the control can compensate load dump voltage error with the load regulation. The same hysteretic control naturally skips the output if the output voltage has not droop enough. This permits regulation for unbalanced loads and the control can focus on regulation of the master loop.

The master loop receives energy only after the independent voltage has or if it was skipped. The control can regulate the master loop accurately in continuous-conduction mode. However, in discontinuous-conduction mode the average voltage falls with falling load level when the inductor current ripple cannot cover the whole hysteretic window.

During load dumps, the converter can react within 3.8 μs at which point the outputs start recovering. Also, an individual load dump in the independent output results in cross-regulation in the master loop because it does not receive energy (or the excess) after the independent output recovers. For the same reason, the independent output does not suffer from cross-regulation when the master loop suffers from a load dump.

The hysteretic control allows a short response time that minimizes the error voltage at the output. Albeit the proposed design has twice the response time from a hybrid converter that combines linear and switching regulators, it does so with higher efficiency across the full power range and in a smaller silicon area. Extending this control where it can generate buck and boost power stage can provide a high bandwidth, efficient and compact power management for microsystems.

CHAPTER 5

PROPOSED SINGLE-INDUCTOR TRIPLE-OUTPUT BUCK–BOOST POWER SUPPLY

Designing one power supply to meet the power demands of all function is challenging and inefficient. As detailed in Chapter 1, DSPs are low voltage and noise tolerant while sensors and ADCs usually require higher supplies with lower noise content. And to drive the power that antennas require, power amplifiers often need higher voltages to decrease ohmic losses. In these applications, the power management calls for multiple buck and boost supplies. Moreover, as battery discharges and its voltage decreases, the converter might need to boost instead of buck to one or more outputs. The proposed triple-output power supply can generate two bucks and one boost voltages with the least number of switching events to meet the demands of multi-functional microsystems while preserving high efficiency.

5.1 Power-Supply System

Switched-inductors converters deliver power by energizing and draining an inductor L_O from input source v_{IN} into an output v_O in alternating phases of a switching sequence. In a SIMO, the outputs share the inductor, and in the proposed controller, outputs share a single inductor energy packet during a switching cycle. This allows the inductor to keep delivering energy to all outputs regardless if they are buck or a boost. For instance, if a buck output energizes the inductor, any buck or boost output can de-energize it. However, there will be a power limitation for the boosted output as buck outputs can only receive

limited energy. When boosted output's power limit is surpassed, the power stage must be able to supply enough energy by having assisting the energizing period.

5.1.1 Power Stage

The power stage in Figure 5.1 regulates two buck outputs, v_{O1} and v_{O2}, and a boost output v_{O3} from a 2.7−4 V supply v_{IN}. v_{O1} can provide energy to analog loads with a target of 1.8 V because it receives energy first and therefore suffers from the least cross-regulation as measured and explained in Chapter 4. v_{O2} targets a voltage of 1.2 V suitable for digital circuits such a digital signal processor (DSP) and even though can suffer from cross-regulation, digital circuits are noise tolerant. Lastly, v_{O3} is a boost voltage that can provide up to 30 mA to a 4 V load such a power amplifier. As explained in detail later, v_{O3} receives energy last to allow the inductor to energize as much as possible through buck outputs to maintain high efficiency across the most load combinations.

Since switches M_1 and M_2 feed buck outputs at relatively low targets, they can be NFETs. Moreover, to reduce size and conserve high over drive over the v_{IN} range for M_1 and M_2, v_{O3} serves as the supply of their drivers. On the other hand, M_3 is a PFET because v_{O3} is high enough to give a high overdrive. To avoid shorting v_{IN} to ground, M_{IN}'s and M_G's gate signals include a dead period across which M_G's body diode conducts i_L. M_1's, M_2's, and M_3's gates similarly incorporate a dead period to keep M_1, M_2, and M_3 from shorting their outputs. But since i_L must nevertheless flow, M_3's bulk connection to v_{O3} adds a body diode that conducts i_L to v_{O3} through this dead-time period.

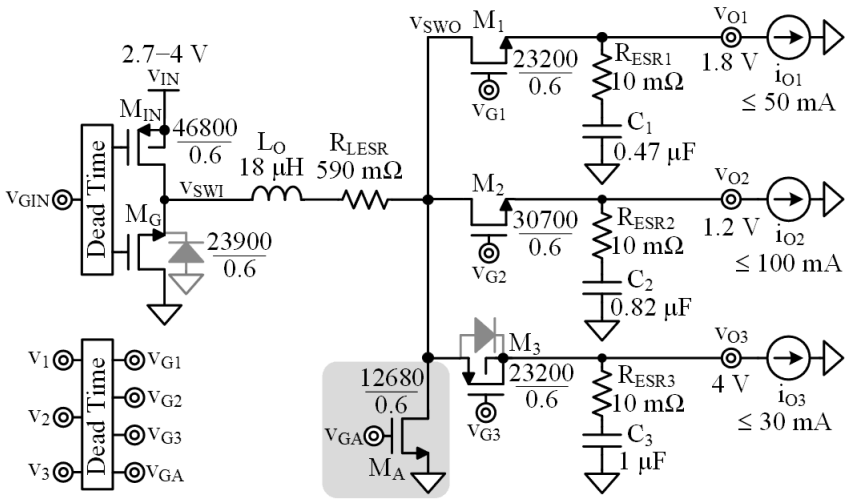


Figure 5.1. One-inductor triple-output buck–boost power supply.

5.1.2 Operation – Five-Switch Mode

The buck–boost supply in Figure 5.1 closes M_{IN} and M_1 first to energize L_O from the input v_{IN} into the first output v_{O1}. L_O's current i_L and v_{O1} in Figure 5.2 therefore rise past 450 ns. When v_{O1} reaches its 1.84-V target v_{T1}, after t_1, M_1 opens and M_2 closes to supply v_{O2}. But since L_O still does not hold enough energy to feed the rest of the loads, M_{IN} continues to energize L_O. As a result, i_L and v_{O2} both rise after 1.25 µs.

When L_O holds enough energy to feed the rest of the loads, M_{IN} opens and M_G closes to begin draining L_O. So i_L starts to fall at 1.75 µs. But since M_2 still supplies v_{O2}, v_{O2} continues to climb. When v_{O2} reaches its 1.24-V target v_{T2} (at 2.05 µs), M_2 opens and M_3 closes to feed v_{O3}. v_{O3} therefore rises until the feedback controller finishes draining L_O at 2.45 µs. This way, L_O feeds all outputs across one energize–drain sequence. Notice that in this scenario with the given load conditions, the converter must energize through both v_{O1} and v_{O2}. However, the converter can stop energizing when delivering energy to v_{O1} if v_{O1}'s load is high relative to v_{O2} and v_{O3}.

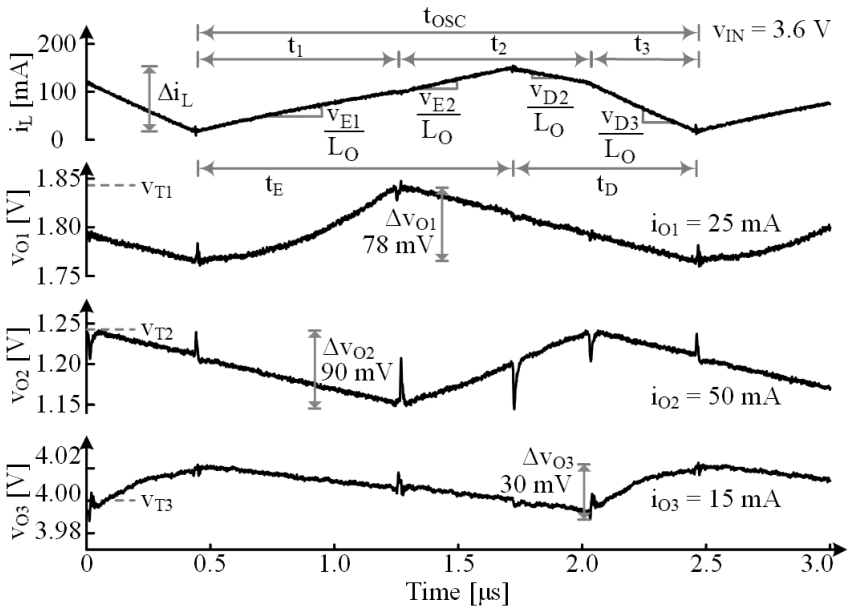


Figure 5.2. Measured waveforms when operating in the five-switch mode.

L_O operates in discontinuous conduction when loads are so light that L_O can satisfy them with small and infrequent energy packets. Still, the operation is generally the same. In Figure 5.3, for example, L_O energizes to v_{O1} across t_1 and v_{O2} for part of t_2. Then, M_{IN} opens and M_G closes to drain L_O to v_{O2} for the remainder of t_2 and to v_{O3} across t_3. In this mode, the energy the outputs receive is sufficient to satisfy them for the rest of the oscillating period t_{OSC}. The sequence repeats after that.

L_O can energize and drain into any buck output v_{BK} because L_O's energizing voltage v_E or $v_{IN} - v_{BK}$ is always positive and L_O's drain voltage v_D or $0 - v_{BK}$ is always negative. Without ground switch M_A in Figure 5.1, however, L_O can drain, but not energize into a boost output v_{BT} because $v_{IN} - v_{BT}$ is negative. But if L_O energizes sufficiently into buck outputs, L_O can drain into boost outputs. Therefore, L_O in Figure 5.2 and Figure 5.3 can drain into v_{O3}'s boosted 4.0 V.

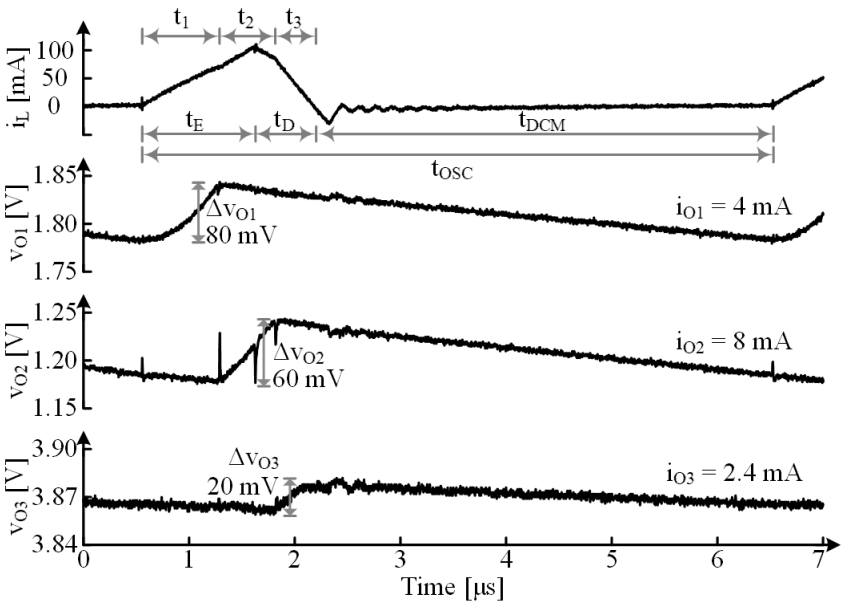


Figure 5.3. Measured waveforms in discontinuous conduction.

5.1.3 Operation – Six-Switch Mode

If v_{IN}'s power when energizing through buck outputs is not sufficient to supply boost power, M_A in Figure 5.1 can help. So, if after energizing to buck outputs L_O's energy is not

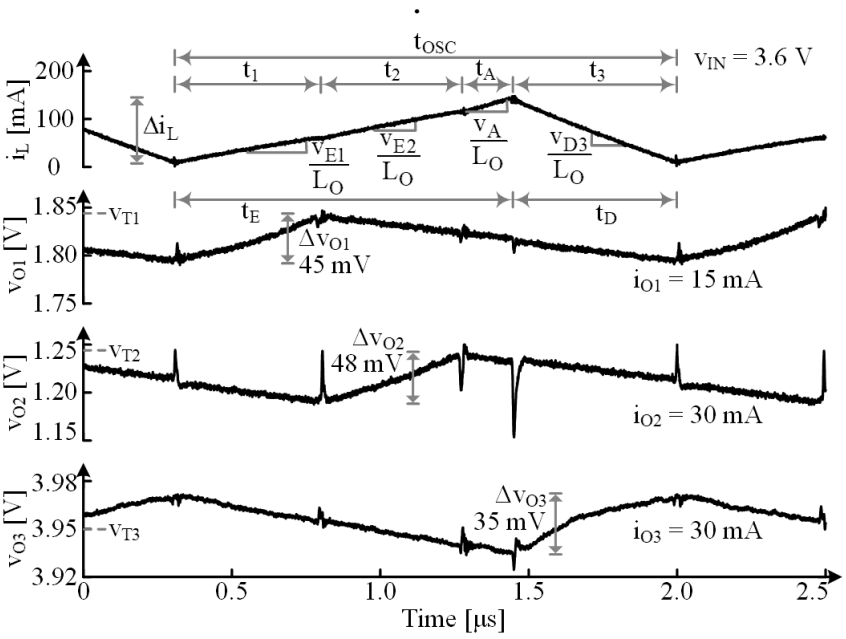


Figure 5.4. Measured waveforms when operating in the six-switch mode.

enough to supply boost outputs, M_A can energize L_O further. In Figure 5.4, for example, M_{IN} and M_1 and M_2 first energize L_O into v_{O1} and v_{O2} across t_1 and t_2. But since energy in L_O is not enough, M_2 opens and M_A closes. In this way, L_O continues to energize (from v_{IN} to ground). Then, with sufficient energy in L_O, M_A opens and M_3 closes to feed v_{O3}.

When v_{O3}'s load i_{O3} just rises above the five-switch limit P_{O3}' in discontinuous conduction, v_{O3} needs M_A's assistance, but at first, only occasionally. In Figure 5.5, for example, v_{O3} requires additional energy every other cycle or about every 50 µs. That is in addition to the energy packet v_{O1}, v_{O2}, and v_{O3} receive every 25-µs cycle. When i_{O3} rises above a threshold level, v_{O3} starts receiving energy every cycle. At that point, L_O operates more like Figure 5.4 shows, but with intervening zero-current time gaps t_{DCM} between energy packets like Figure 5.3 illustrates.

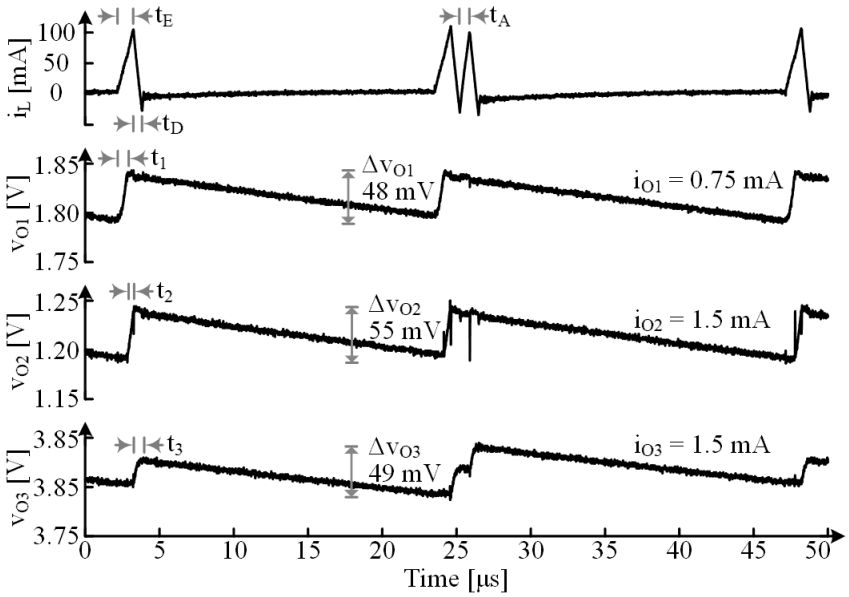


Figure 5.5. Measured six-switch waveforms in discontinuous conduction.

5.2 Design and Implementation

Since microsystems adapts power consumption for each function to conserve power, the converter must react quickly providing energy when required. Ideally, the converter should have a simple control that can incorporate a boosted output to minimize area consumption while having a high bandwidth. Adapting the hysteretic controller from the previously proposed in the dual-output switched-inductor converter from Chapter 4 helps maintain the dynamic performance of hysteretic control while keeping the overall control simple.

5.2.1 Boost Control

The triple-output buck–boost power supply in Figure 5.6 adapts the controller in Figure 4.1 to include M_A. This way, M_1 feeds L_O to v_{O1} until comparator CP_1 senses that v_{O1} reaches target v_{T1}. M_2 then feeds L_O to v_{O2} until CP_2 similarly senses v_{O2} reaches v_{T2}. M_3 ends the sequence by directing L_O to v_{O3}.

If control tries to energize through boosted v_{O3}, it will first engage M_A to extend L_O's energizing. The control, as shown in Figure 5.6, achieves this if hysteretic comparator CP_{OSC} does not stop energizing L_O by the time L_O satisfies v_{O2}; then, AND_A invokes M_A's assistance. For this, $NAND_3$ keeps M_3 from opening, and instead, directs L_O to ground. L_O therefore continues to energize to ground until CP_{OSC} opens M_{IN} to stop energizing L_O. At that point, AND_A opens M_A and $NAND_3$ closes M_3 to supply v_{O3}.

Like the dual-supply system proposed in Chapter 4, a DCM detector disengages M_G to prevent unnecessary conduction and therefore losses. Because v_{O3} is a boosted output, M_3 must be off after i_L reaches zero in DCM. Otherwise, a conduction path exists between v_{O3} and supply v_{IN} through M_3 and M_{IN}'s body diode. This conduction path

discharges v_{O3} to the supply v_{IN} if v_{O3} is higher than v_{IN} by one diode voltage drop or 0.6 V. This would increase losses as the M_3's lost energy gets replenished at the next cycle. However, turning M_3 off (in addition to M_G) when i_L reaches zero eliminates this loss since there will be back-to-back diodes between v_{IN} and v_{O3}.

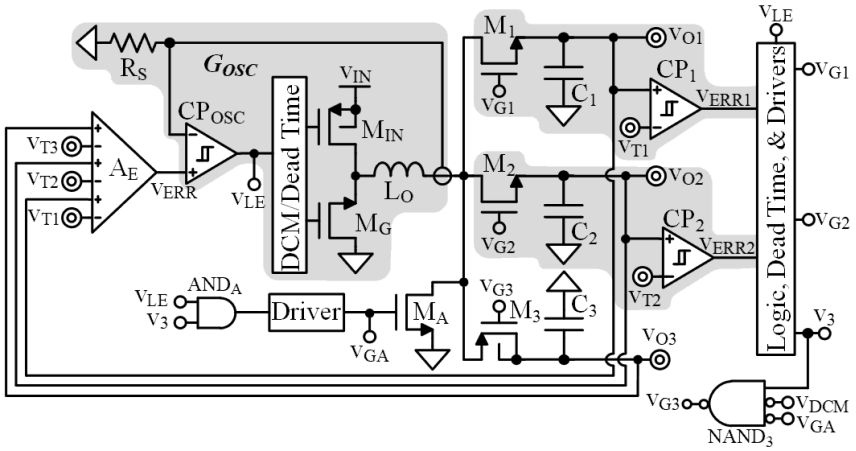


Figure 5.6. Triple-output buck-boost switched-inductor supply system.

5.2.2 Output Sequence Logic

Combinational logic implements the sequence control while giving priority to output v_{O1}, followed by v_{O2}, and lastly v_{O3}. The logic decides which outputs receives energy at the beginning of the cycle using the status of comparator output's v_{ERR1} and v_{ERR2} which senses if their outputs are satisfied. Figure 5.7 shows the logic to engage v_{O1} which simply consists of setting the latch of control signal v_1 if the output requires energy at the beginning of the cycle. A fall edge detector creates a 20-ns pulse signal v_{OSC} used throughout the logic control at the beginning of a new cycle when CP_{OSC} commands a new energizing event. After setting v_1's reset-dominant latch, it commands drivers to engage M_1. As soon as v_{O1} gets satisfied (by v_{ERR1} going logic high), it reset the latch and M_1 turns off.

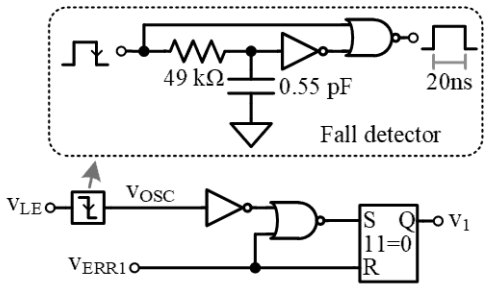


Figure 5.7. Logic to engage and turn off output v_{O1}.

To engage v_{O2}, output v_{O1} must be satisfied (v_{ERR1} logic high), and v_{O2} require energy (v_{ERR2} logic low) as Figure 5.8 shows. If at the beginning of the cycle v_{O1} requires energy, the latch resets and command the M_2's driver to turn off through control signal v_2. To prevent error and lock in the sequence, as soon the last output starts receiving energy v_3 is logic high and resets the latch for v_2. This prevents inadvertently engaging v_{O2} if it requires energy again and v_{O1} is still satisfied while the converter supplies energy to v_{O3}. To minimize glitching events if v_{O1} is engaged, v_1 also keep resetting v_2's latch.

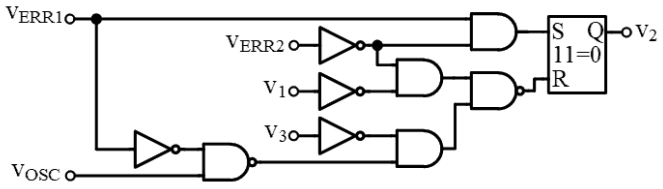


Figure 5.8. Logic to engage and turn off output v_{O2}.

The last output in the sequence engages for the remaining of the cycle after output v_{O2} receives energy. For this, as soon as v_{O2} gets satisfied, i.e. v_{ERR2} is logic high, and v_{O1} is not engaged and not satisfied this will set the last output to receive energy as in Figure 5.9. If at any time both outputs are satisfied, it will allow v_{O3} to receive energy by giving a logic high to control signal v_3. Setting v_3 logic high allow the output to receive energy but additional logic gates, as shown in Figure 5.6, decides to turn on auxiliary switch M_A or M_3 depending if the converter is energizing or de-energizing the inductor. Also shown in

Figure 5.9, logic resets signal v_3 and disallow v_{O3} to receive energy whenever any previous outputs are engaged or if any of them are not satisfied at the beginning of a cycle.

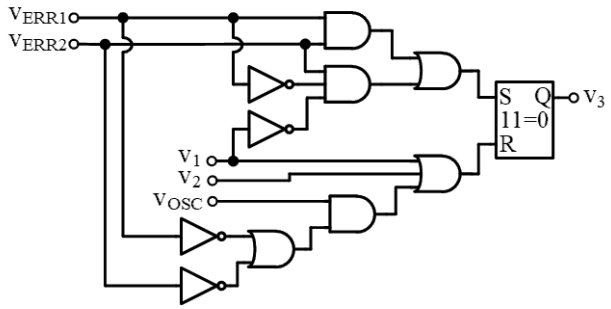


Figure 5.9. Logic to engage and turn off output v_{O3}.

5.2.3 Output Dead-Time Generator and Drivers

The proposed triple-output buck-boost converter has a similar implementation of dead-time generator and drivers for the input switches M_{IN} and M_G as in Figure 4.6. However, switching among outputs switches M_1, M_2, M_3, and M_A requires more consideration to avoid engaging two or more switches in all possible sequence combinations. To avoid two switches turning on simultaneously and introduce a dead time period, the logic in Figure 5.10 creates a signal for each switch that extends beyond the actual on time and then combine them in an OR operation so that if there are two or more switches trying to turn on, none of them will.

For example, if switch M_1 is on, signal $v_{1(ON)}$ is logic high and force switches M_2, M_3, and M_A to be off. If logic want to engage M_2 by making v_1 and v_2 logic low and high, M_1's gate will start falling quickly. However, $v_{1(ON)}$ will be logic high for around 10 ns as the fall edge extender will delay the sensed fall of v_{G1}. During the extension of 10 ns, both $v_{1(ON)}$ and $v_{2(ON)}$ will be logic high and therefore force all the switches to be off, and hence creating the dead-time period. After the 10-ns extension, $v_{1(ON)}$ falls and M_2 turns on.

Although the control logic does not allow any two outputs to be on at any time, the implementation of the dead-time period gives extra protection in case of an unexpected or unforeseen glitch.

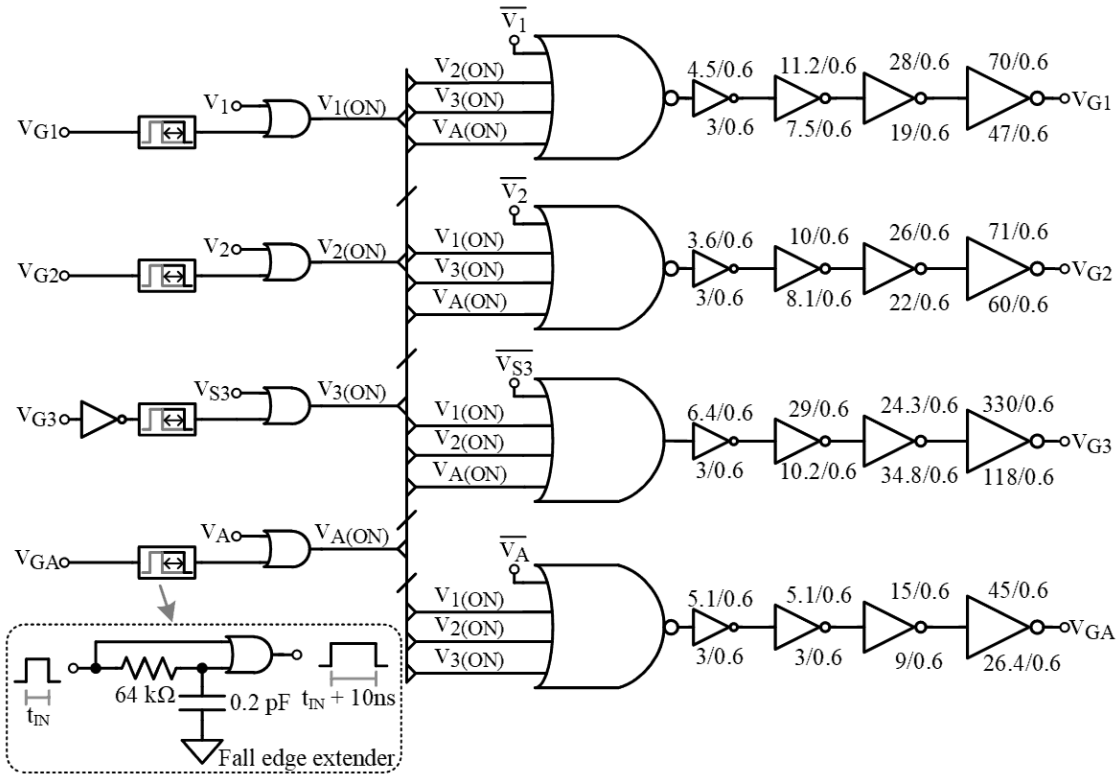


Figure 5.10. Drivers and dead-time generator for outputs' switches.

Figure 5.10 also shows the drivers size for the output switches. They are sized to achieve almost symmetrical turn on and off times of about 5-10 ns. In this way, their sizes and switching noise during the hard-switching event are decreased without the turn-on and turn-off times affecting the performance. Note that M_3's body diode conducts before engaging the switch making the switching on or off smoother and less noise generating. Thus, its driver is sized more aggressively.

5.2.4 Power Management

As explained in Chapter 4, the converter will incur in power losses due to resistances, switching gates, and controller consuming ohmic, gate-drive, and quiescent power P_R, P_G, and P_Q. To minimize switches' conduction and gate losses $P_{R(SW)}$ and P_G, transistor channel lengths L_{MIN} are minimum at 0.6 μm and widths W_{SW} are wide enough to balance their ohmic and gate-drive losses by minimizing the total power for a given switching frequency f_{OSC} and gate voltage v_G [104]:

$$\begin{aligned} P_{L(SW)} &= P_{R(SW)} + P_G = R_{SW} i_{O(RMS)}^2 + C_G f_{OSC} V_G^2 \\ &= \left[\frac{L_{MIN}}{W_{SW} k \left(V_{GS} - V_{TH} \right)} \right] i_{O(RMS)}^2 + \left(L_{MIN} W_{SW} C_{OX} \right) f_{OSC} V_{GS}^2 \end{aligned} . \tag{5.1}$$

To find such width W_{SW} that balance minimizes losses, the loss equation should be derived, equated to zero and then solve for W_{SW}:

$$\begin{aligned} W_{SW} &= \sqrt{\frac{i_{O(RMS)}^2}{k C_{OX} f_{OSC} \left(V_{GS} - V_{TH} \right) V_{GS}^2}} \\ &\approx \sqrt{\frac{i_O i_{O(TOT)}}{k C_{OX} f_{OSC} \left(V_{GS} - V_{TH} \right) V_{GS}^2}} \end{aligned} , \tag{5.2}$$

where k is the transconductance, C_{OX} the oxide capacitance per area and V_{TH} the threshold voltage of the switch. This gives a minimum switch loss $P_{LSW(MIN)}$ of:

$$P_{LSW(MIN)} = 2 \left(\sqrt{\frac{L_{MIN}^2 f_{OSC} C_{OX} i_O i_{O(TOT)} V_{GS}^2}{k \left(V_{GS} - V_{TH} \right)}} \right) . \tag{5.3}$$

Below the optimization point which is half the full load in this design, switching losses from the gate drive P_G increases the fastest, and above conduction losses P_R does.

Hence, the fractional loss of losses to input power P_{LOSS}/P_{IN} bottoms at around half the full power of the converter as simulations shown in Figure 5.11. A benefit of hysteretic control is that it scales the frequency as load decreases and converter operates in discontinuous-conduction mode. This improves efficiency for light load conditions and the main reason P_G decreases when combined power load is below 100 mW. This efficiency enhancement is limited by the quiescent power of the controller P_Q that slightly scales with frequency but has a minimum loss of 1.4 mW. Hence, fractional loss increases sharply when combined load power is below 20 mW.

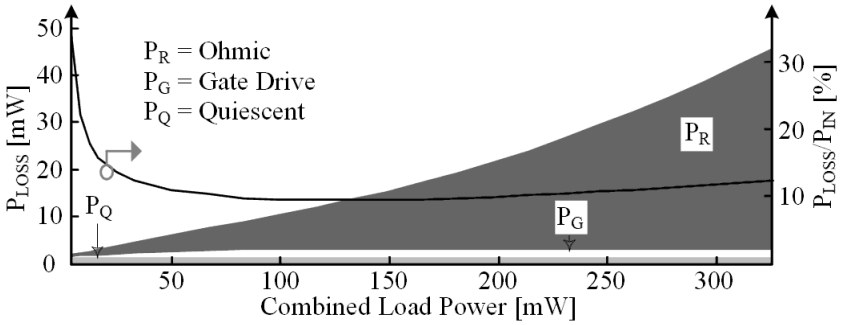


Figure 5.11. Simulated losses of the triple-output buck-boost converter.

5.2.5 Stability

The stability design follows the same methodology presented in Chapter 3 for a SIMO with all buck outputs. The hysteretic current mode control will form an oscillator with inductor current i_L, where the hysteretic window fixes the ripple Δi_L around its average $i_{L(AVG)}$. The output error will adjust $i_{L(AVG)}$ until all outputs receive the required energy. Independent outputs v_{O1} and v_{O2} will have their own local loop which regulates the peak voltage of their outputs. The master loop forms the outer loop through output v_{O3} which commands the current loop to adjust i_L until all outputs are satisfied.

Even though v_{O3} is a boosted output, the same analysis from Chapter 3 still applies because during a five-switch operation it operates just like an all buck SIMO. The current loop's bandwidth is limited by the rising or falling rate of the inductor current. The bandwidth of the independent loop still scales with switching frequency f_{OSC} and depends on load conditions while the master loop depends on the output impedance. The only time the analysis requires modification is when the SIMO resembles a boost converter during six-switch operation where, for a brief time, none of the output receive energy as inductor energizes from supply to ground.

Like in boost converters, disconnecting all outputs to energize L_O introduces an out-of-phase right-half-plane zero z_{RHP}. This is because, while energizing L_O with switch M_A, which without z_{RHP} should raise v_{O3}, load i_{O3} discharges C_3. In other words, what should raise v_{O3} also lowers v_{O3}. z_{RHP} therefore appears at the frequency when the fall exceeds the rise [79].

To find z_{RHP}, first consider that L_O's energizing and drain voltages v_E or v_{IN} and v_D or $-v_{O3}$ across L_Os and across and after M_A's connection time t_A set how much additional current L_O collects i_l [79]. The fraction of the oscillating period t_{OSC} that L_O connects to v_{O3}: d_3 or t_3/t_{OSC} which can be approximated to $i_{O3}/(i_{O1}+i_{O2}+i_{O3})$, determines how much of i_l reaches v_{O3}. So, a rise in t_A ultimately delivers i_{l+} to v_{O3}:

$$i_{l+} = i_l d_{o3} = d_a \left(\frac{v_E - v_D}{sL_O} \right) \left(\frac{t_{O3}}{t_{OSC}} \right) \approx \left(\frac{t_a}{t_{OSC}} \right) \left(\frac{v_{IN} + v_{O3}}{sL_O} \right) \left(\frac{i_{O3}}{\sum i_{OX}} \right) \tag{5.4}$$

The current M_A sinks, however, does not reach v_{O3}. This current: i_{lA}, is the charge i_L supplies at its peak $i_{L(PK)}$ across t_a:

$$i_{l-} = \frac{q_{l-}}{t_{OSC}} \approx \frac{i_{L(PK)} t_a}{t_{osc}} = i_{L(PK)} d_a \tag{5.5}$$

The loop is inverting as long as i_{l+} surpasses i_{l-}. But since i_{l+} drops with frequency, v_{O3} inverts when i_{l+} falls below i_{l-}. This means that z_{RHP} appears when i_{l-} matches and exceeds i_{l+}:

$$z_{RHP} \approx \left(\frac{v_E - v_D}{2\pi L_O i_{L(PK)}} \right) d_{O3} \approx \left(\frac{v_{IN} + v_{O3}}{2\pi L_O i_{L(PK)}} \right) \left(\frac{i_{O3}}{i_{O1} + i_{O2} + i_{O3}} \right) \tag{5.6}$$

5.3 Measured Performance

The 0.6-µm CMOS die in Figure 5.12 shows the prototyped triple-output buck-boost supply system. The die integrates the power switches, drivers, and the controller, except for the current sensor, 18-µH inductor L_O, and 0.47-, 0.82-, and 1-µF capacitors C_1, C_2, and C_3. Also, the die, packaged in a SOIC, has a silicon area of 2.0 × 1.4 mm^2 including 28 bond pads and test circuits.

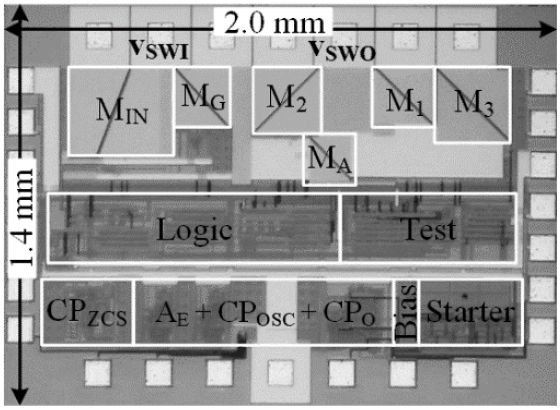


Figure 5.12. Prototyped 0.6-µm CMOS die.

Aside from the integrated circuit (IC), L_O, C_1, C_2, and C_3, the board also includes test and load circuits as Figure 5.13 shows. L_O, and each of the capacitors occupy 3.5 × 2.7 × 2.4 mm^3, and 1.6 × 0.81 × 0.91 mm^3. With these dimensions, L_O's equivalent series

resistance (ESR) is 590 mΩ and those of C_1, C_2, and C_3 are 10 mΩ. All included circuits, proposed and test, occupies an area of 8.6 × 13.2 mm^2 of the two-layer PCB board.

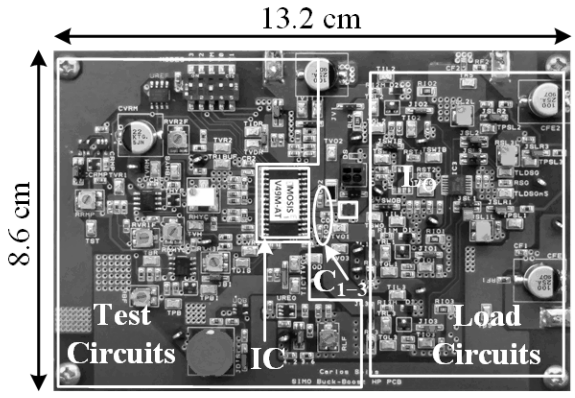


Figure 5.13. Two-layer board for testing buck-boost prototype.

5.3.1 Operation Mode Boundary

L_O can feed v_{O3} during de-energizing, after supplying v_{O1} and v_{O2}, L_O can still satisfy v_{O3}'s load P_{O3} across the time t_{O3} that L_O feeds v_{O3}. To determine this limit, first consider that the feedback controller ensures L_O delivers enough current to satisfy all outputs. With that much current, L_O connects to each output v_{OX} the fraction d_{OX} of the oscillating period t_{OSC} that i_L requires to satisfy each load i_{OX}. When i_L's ripple is much lower than i_L's average, d_{OX} is nearly the fraction of current that i_{OX} demands of all the loads combined Σi_{OX}:

$$d_{OX} = \frac{t_{OX}}{t_{OSC}} = \frac{t_{OX}}{t_{O1} + t_{O2} + t_{O3}} \approx \frac{i_{OX}}{\sum i_{OX}} = \frac{i_{OX}}{i_{O1} + i_{O2} + i_{O3}}. \tag{5.7}$$

L_O can supply the most P_{O3} when L_O energizes the entire time L_O connects to v_{O1} and v_{O2} and drains the entire time L_O connects to v_{O3}. But to balance i_L, i_L must rise as much as i_L falls across t_{OSC}. i_L must therefore climb Δi_L with v_{O1}'s and v_{O2}'s energizing voltages v_{E1} and v_{E2} or $v_{IN} - v_{O1}$ and $v_{IN} - v_{O2}$ and fall Δi_L with v_{O3}'s drain voltage v_{D3} or $-v_{O3}$:

$$\Delta i_L = \left| \left(\frac{v_{E1}}{L_O} \right) t_{O1} + \left(\frac{v_{E2}}{L_O} \right) t_{O2} \right| = \left| \left(\frac{v_{D3}}{L_O} \right) t_{O3} \right| . \tag{5.8}$$

When factoring L_O out and noting t_{O1}, t_{O2}, and t_{O3} relate like i_{O1}, i_{O2}, and i_{O3}, the expression reveals that, of the power v_{IN} supplies with i_{O1} and i_{O2}, v_{O3} receives as P_{O3}' what v_{O1} and v_{O2} do not collect with P_{O1} and P_{O2} or $v_{O1}i_{O1}$ and $v_{O2}i_{O2}$:

$$\begin{aligned} v_{O3}t_{O3} &\approx v_{IN}(t_{O1} + t_{O2}) - v_{O1}t_{O1} - v_{O2}t_{O2} \\ v_{O3}i_{O3} &\approx v_{IN}(i_{O1} + i_{O2}) - v_{O1}i_{O1} - v_{O2}i_{O2} \\ P_{O3}' &\approx v_{IN}(i_{O1} + i_{O2}) - (P_{O1} + P_{O2}) \end{aligned} . \tag{5.9}$$

The system, however, loses power to the controller and switches. To generalize and adjust for losses, of what v_{IN} supplies with buck currents Σi_{BK}, boost outputs can receive as $\Sigma P_{BT}'$ what buck outputs and losses do not consume with ΣP_{BK} and P_{LOSS}:

$$\sum P_{BT}' = v_{IN} \sum i_{BK} - \sum P_{BK} - P_{LOSS} = (v_{IN} \sum i_{BK}) \eta_C - \sum P_{BK} , \tag{5.10}$$

where $(v_{IN}\Sigma i_{BK})\eta_C$ is the fraction of v_{IN}'s power not lost to P_{LOSS}. Incidentally, efficiency depends also on power levels, which means that the boundary must be found in an iterative process during the design and/or evaluation phase.

Since v_{IN} is greater than all buck outputs, v_{IN}'s buck power $v_{IN}\Sigma i_{BK}$ climbs faster with buck currents Σi_{BK} than buck power ΣP_{BK}. Boost power limit $\Sigma P_{BT}'$ therefore rises with buck currents and input voltage v_{IN}. Therefore, the six-switch boundary that v_{O3}'s boost power limit P_{O3}' establishes in Figure 5.14 increases with input voltage v_{IN} and buck currents i_{O1} and i_{O2}. In other words, even with constant current loads, rising buck voltages v_{O1} and v_{O2} reduces available boost power as buck power increases, and hence the limiting available boosted power.

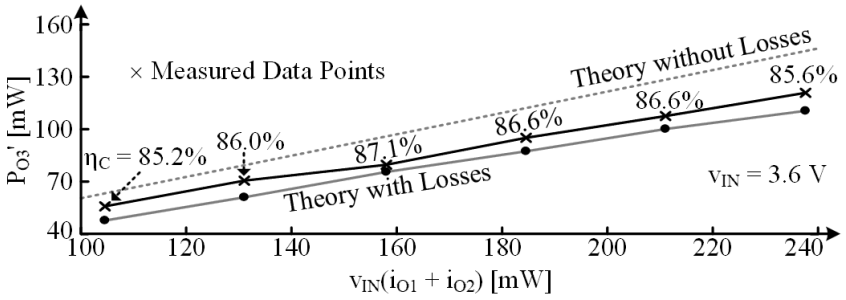


Figure 5.14. Theoretical and measured maximum boost power with five switches when v_{IN} is 3.6 V.

Figure 5.15 corroborates the five-switch boundary dependency to supply v_{IN} while holding output voltages at the same targets. Since energizing time must increase with lower v_{IN} to deliver the same power to buck outputs, the boost power P_{O3}' available reduces. For instance, each data point on Figure 5.14 and Figure 5.15 correspond to the same total buck current (horizontal axis scaled with v_{IN}) and for each corresponding data point, P_{O3}' is significantly lower when comparing the vertical axis scales.

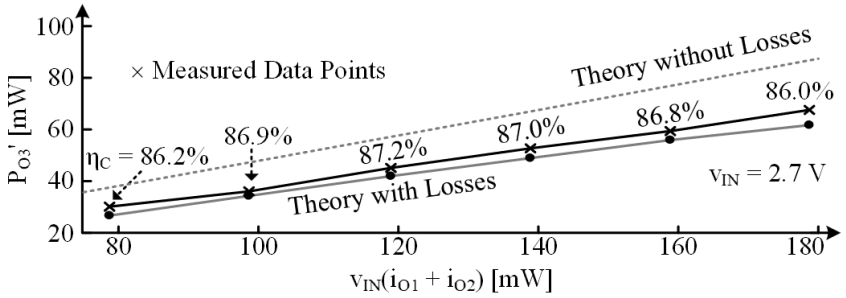


Figure 5.15. Theoretical and measured maximum boost power with five switches when v_{IN} is 2.7 V.

5.3.2 Load Regulation

As load levels and combinations changes, so will the regulated average voltage due to load regulation. Figure 5.16 shows average voltage for v_{O1} across buck and boost load where buck loads has a fixed ratio of $i_{O2} = 2 \cdot i_{O1}$. Because the independent loop regulates the peak voltage, v_{O1}'s load droops v_{O1} across what remains of t_{OSC} after v_{O1}'s connection time t_1 lapses. Therefore, average voltage $v_{O1(AVG)}$ decreases by an effective load regulation

voltage v_{LR} that increases proportionally to v_{O1}'s discharge rate i_{O1}/C_1, disconnect time $t_{OSC} - t_1$:

$$v_{LR1} = \left(\frac{i_{O1}}{2}\right)\left(\frac{t_{OSC} - t_1}{C_1}\right). \tag{5.11}$$

That is why, $v_{O1(AVG)}$ decreases linearly as the buck loads increases. Also, notice that $v_{O1(AVG)}$ slightly increases with boost load i_{O3}. This is due to a smaller period t_{OSC} as boosted output v_{O3} connects for a larger fraction of the total de-energizing time and hence decreasing t_{OSC}.

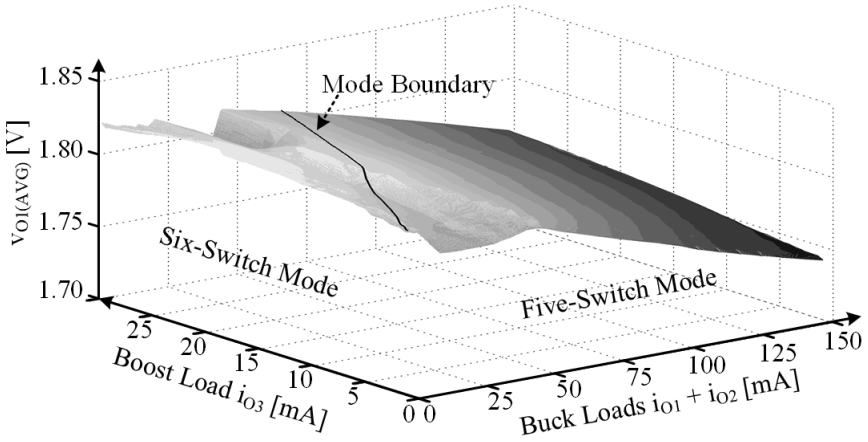


Figure 5.16. Measured load regulation for output v_{O1}.

The average voltage for v_{O2} or $v_{O2(AVG)}$ will behave similarly as $v_{O2(AVG)}$ as Figure 5.17 shows. Both outputs also exhibit a decrease in their average voltages when increasing total buck load at a high boost load. As boost load i_{O3} is disparately large compared to the buck loads, controller will skip v_{O1} and v_{O2} to deliver more energy to v_{O3}. Thus, buck voltages will decrease with increases buck load until the converter no longer skip any output as it approaches the mode boundary as shown in Figure 5.17 when i_{O3} is 30 mA.

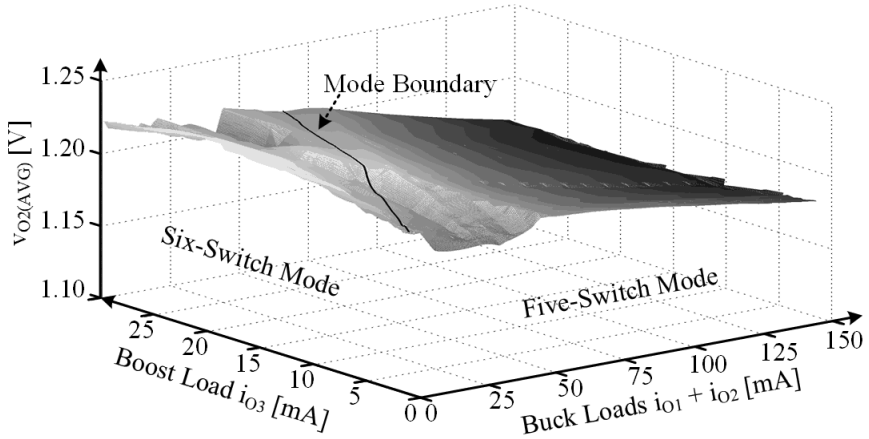


Figure 5.17. Measured load regulation for output v_{O2}.

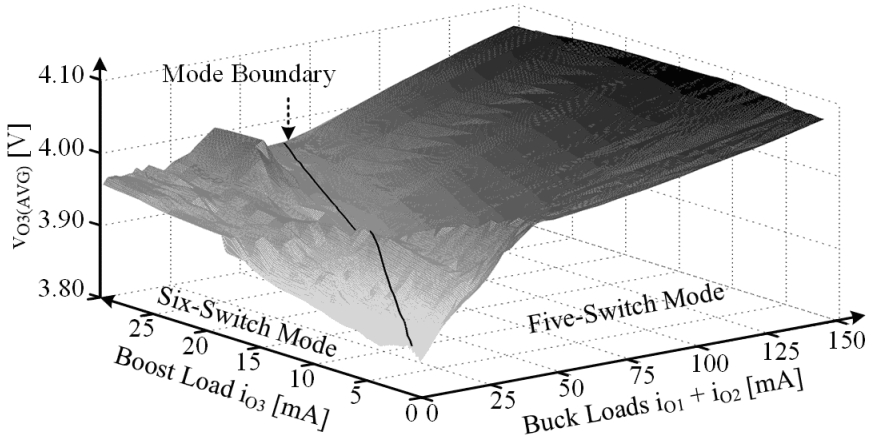


Figure 5.18. Measured load regulation for output v_{O3}.

Since the current loop mixes the outputs of all errors as shown in Figure 5.6, any error on v_{O1} and v_{O2} will transfer as an offset on v_{O3}. Therefore, average voltage $v_{O3(AVG)}$ climbs with buck load in Figure 5.18. Because both buck outputs decrease at a rate of v_{LR1} and v_{LR2}, v_{O3}'s load regulation v_{LR3} climbs with sum of both but opposite in direction:

$$v_{LR3} = -\left(v_{LR1} + v_{LR2}\right). \tag{5.12}$$

Also, because v_{O1} and v_{O2} falls when boost load is high approaching the mode boundary by increasing buck loads, v_{O3} will increase in this region. Also, as explained in

Chapter 4, as current ripple reduces in DCM, v_{O3} will suffer an offset to cover the remaining of the hysteretic window that the inductor current ripple fails to completely cover. Hence $v_{O3(AVG)}$ falls for the plane when i_{O3} is less than 20 mA and buck load ($i_{O1} + i_{O2}$) is less than 50 mA as shown in Figure 5.18.

5.3.3 Efficiency

Figure 5.19 shows the simulated and measured efficiency under balanced loads which always operates in the five-switch mode. However, simulated efficiency considers idealized connections to the PCB board from the die and therefore tends to be 5−6% higher than the measured one. The difference is due to parasitics capacitances and traces such from bondwire, package's leadframe and PCB connections. Also, due to the inherent offset of comparator CP_{ZCS}, control signals DCM has reached before i_L reaches zero and therefore, for a brief time the conduction loss increases as inductor completed de-energizing through two body diodes instead of switches M_G and M_3.

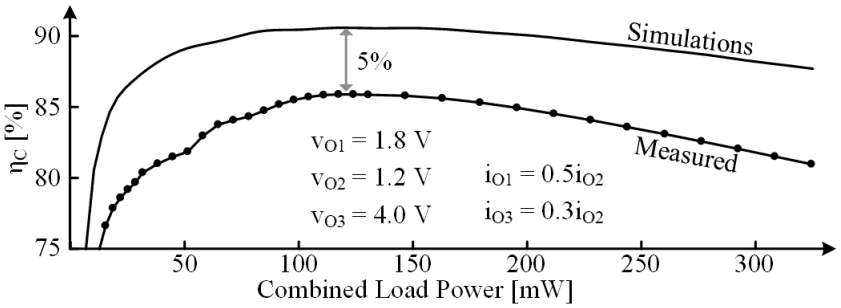


Figure 5.19. Loss comparison of simulated and measured efficiency during five-switch operation.

When M_A energizes L_O, none of the outputs receive power. As a result, all outputs droop across t_A in Figure 5.4, and accuracy suffers. Engaging M_A also requires power that adds to losses in P_{LOSS}. Thus, power-conversion efficiency η_C also drops. Two non-negligible extra loss mechanisms are conduction and switch losses. Like a boost converter,

because M_A engages for a brief time, the inductor must carry more current to provide required total load power is less than a switching period t_{OSC}. This translates to higher conduction losses in switches and parasitics resistances due to the increased dc current level in the inductor. The other loss mechanism, and perhaps more straightforward, is power loss due to engaging M_A: gate, current-voltage overlap (hard-switching) and conduction losses related to the switch itself.

This is why η_C in Figure 5.20 for the proposed supply is generally higher when operating in the five-switch mode, maxing at $\eta_{C(PK)}$ or 87%. When delivering the same total current, η_C is 2% to 3% higher with five switches than with six. Full-load efficiency $\eta_{C(FL)}$ when i_{O1}, i_{O2}, and i_{O3} are 50, 100, and 30 mA is 81%. Also, the proposed converter has a minimum efficiency of 75% when total load current is at least 20 mA.

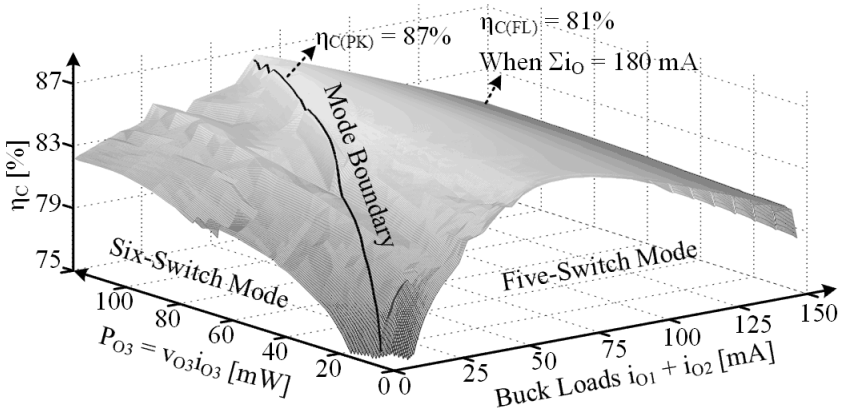


Figure 5.20. Measured power-conversion efficiency across load power.

5.3.4 Dynamic Response

When all loads suddenly rise four times their initial 12.5-, 25-, and 7.5-mA levels while in five-switch operation, the system responds in 5.2 µs and all outputs settle within another 15 µs, as Figure 5.21 shows. During the load step, outputs discharges the capacitors as the

inductor start replenishing them and provides the new required energy to the loads. Since by design, the converter feeds and satisfies v_{O1} and v_{O2} first, they recover and settle faster than v_{O3}.

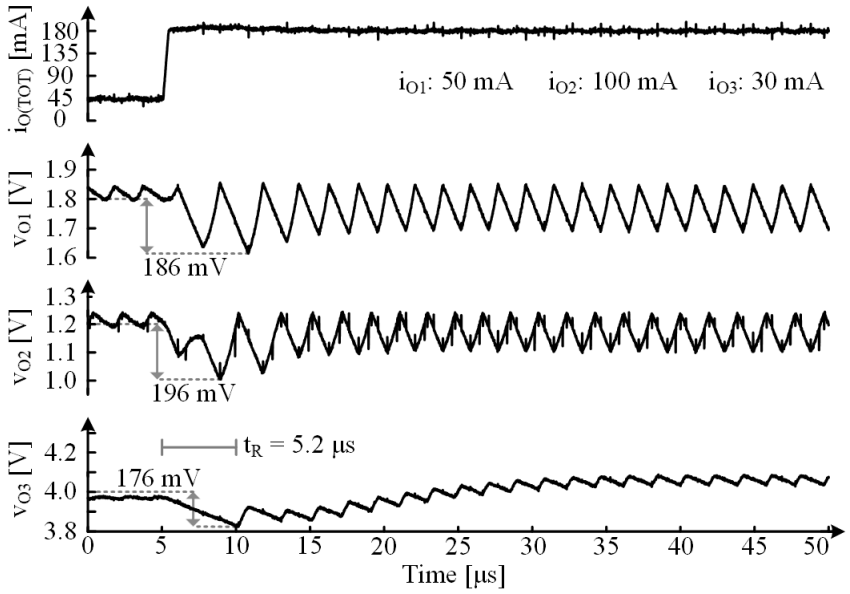


Figure 5.21. Measured rising load-dump response when operating with five switches.

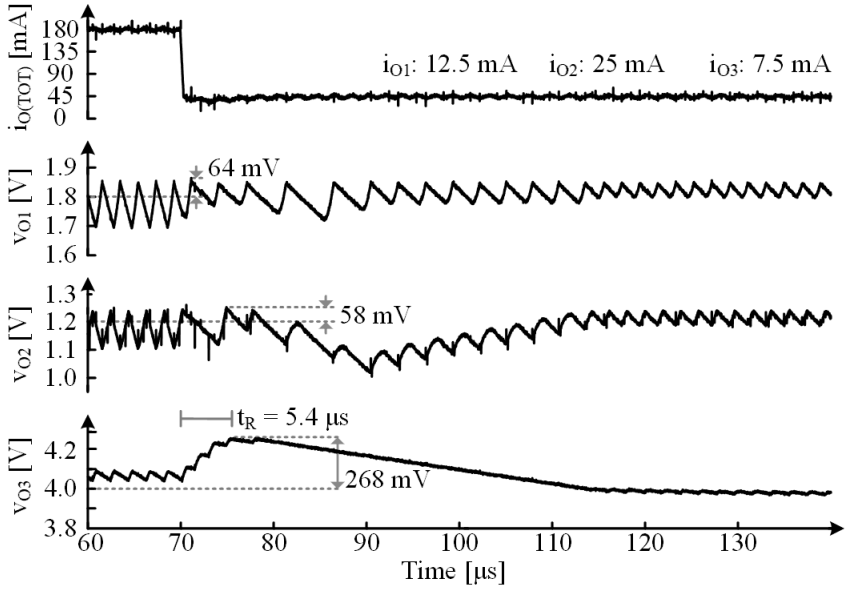


Figure 5.22. Measured falling load-dump response when operating with five switches.

The system similarly responds in 5.4 µs and all outputs recover within another 40 µs when those same loads return to their initial levels. As in Figure 5.22, the system requires more time to settle after the loads disappear because, with such a light load, C_3 slews slowly back to its target. Irrespective of direction, v_{O3} suffers the most variation at −176 and +268 mV while v_{O1} and v_{O2} overshoot are negligible as their peak voltages are accurately regulated.

The system responds a little less quickly when operating in the six-switch mode. This is because connecting L_O to ground requires additional time. So, when subjected to the sudden 1.67× load variations in Figure 5.23, the system responds in 6.2 µs and outputs settle within another 17 µs with a rising load step. During this time, v_{O3} drops 118 mV or 3% while v_{O1} and v_{O2} about 40 mV and 48 mV, respectively.

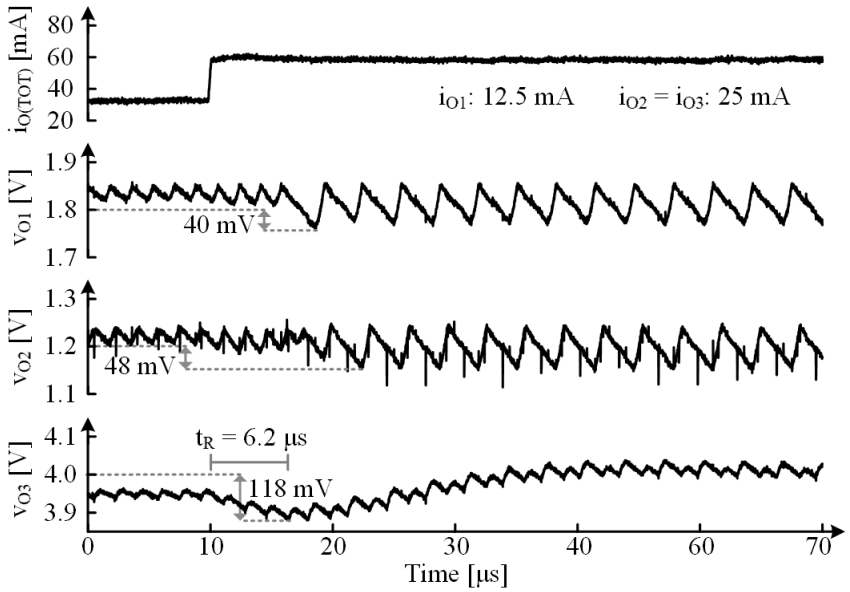


Figure 5.23. Measured rising load-dump response when operating with six switches.

During the falling load step, the system similarly responds in 7 µs and outputs settle within another 20 µs as in Figure 5.24. Independent outputs do not have overshoot as

expected while v_{O3} only overshoots 60 mV or 1.5%. Also, notice that the system overshoots/undershoots once when operating constantly under five-switch or six-switch mode which shows a response with phase margin close to 90°.

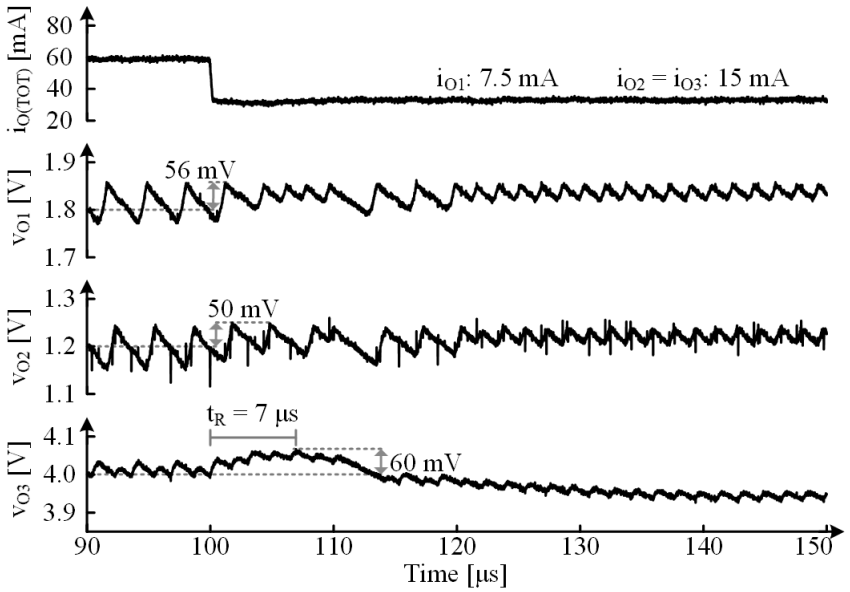


Figure 5.24. Measured falling load-dump response when operating with six switches.

Transitioning between modes adds additional overhead. So, when responding to v_{O3}'s 3–30-mA load dumps in Figure 5.25, the system responds in 8 µs and outputs settle within another 20 µs to rising load step on v_{O3} as its move from the five-switch to the six-switch mode. Notice, v_{O3} over-reacts before finally settling with a slight second ring when i_{O3} increases. This is because z_{RHP} reduces the phase margin of the system as its moves to lower frequencies as the converter transitions to the six-switch operation. Still, the system recovers within one or two rings, which corresponds to 60° to 70° of phase margin [95].

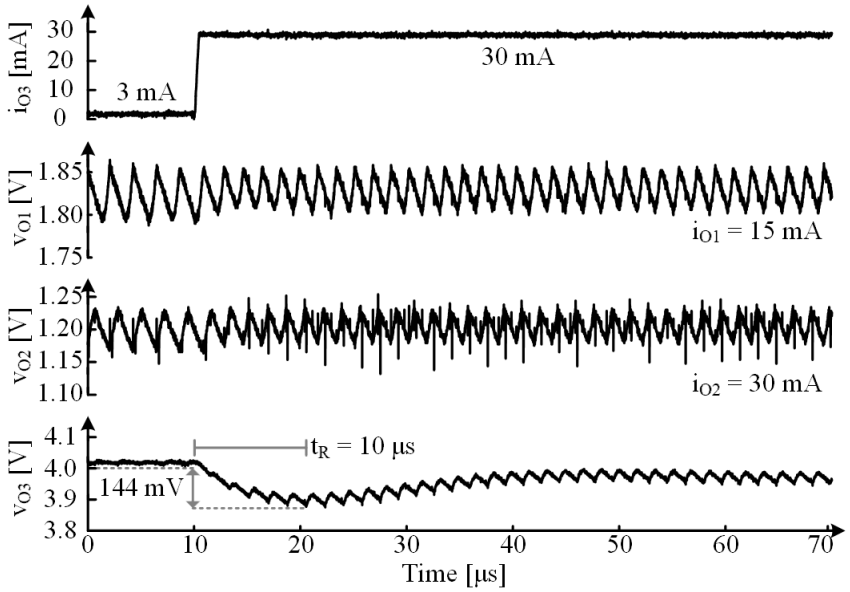


Figure 5.25. Measured rising load-dump response across switching modes.

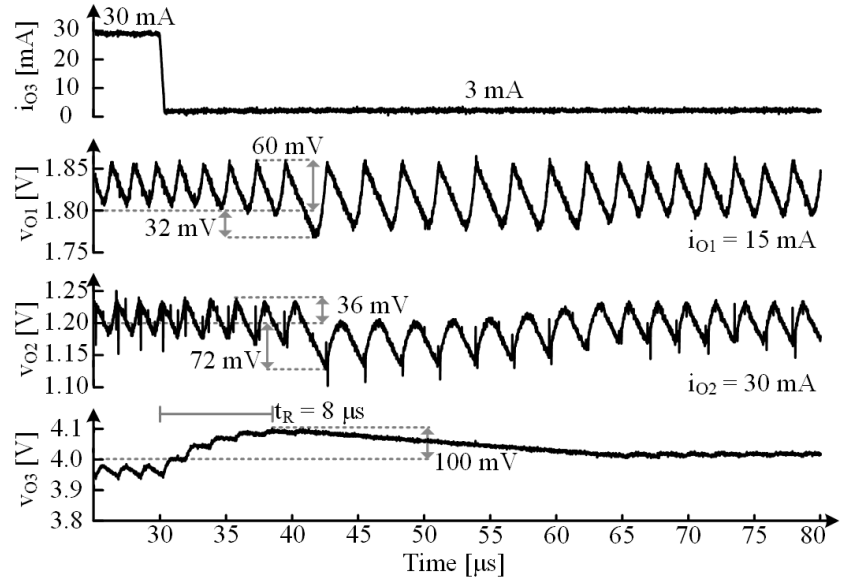


Figure 5.26. Measured falling load-dump response across switching modes.

The controller reacts within 10 µs and outputs settle within another 26 µs for a falling load step in v_{O3} as in Figure 5.26. In this case, no extra ring is noticeable in the response as z_{RHP} moves to higher frequencies and disappears. During the response v_{O3}

overshoots 100 mV or 2.5% while v_{O2} slightly undershoots as converter adjust power delivery. v_{O1}, however, do not overshoot as it has the highest priority.

5.4 State-of-the-Art Comparison

Table 5.1 summarizes he performance of the proposed triple-output buck-boost converter and compared it to the state of the art that (SoA) generates a mix of buck and boost voltages. Due to limited information on response time t_R, the relative figure of merit (RFoM) from Chapter 2 (Equation 2.3), uses the same 10 μs for all designs, effectively cancelling it for the comparison. The proposed converter achieved 13% higher performance than the next best SoA, work presented in [64]. The advantage comes from the simpler implementation which results in the same silicon area per output but with a more than twice bigger technology node which reduces costs. Similarly, although the third best performing SoA, [67] uses less than half the technology size compared to the proposed and dedicated 13% more silicon area for each output.

Other implementations from the SoA, such as [78] don't maintain high efficiency across the load range. Work from [63] requires two external components per output increasing solution cost and size at the board level. Although note reported for most SoA, response time t_R will most likely be higher than 10 μs for those that did not reported. These works used control relaying on PWM control, and as showed in Chapter 4, fully hysteretic control like used in the proposed buck-boost can respond faster to load dumps. This will likely increase the RFoM for the proposed converter relative to the SoA when accounting of performance metrics.

Table 5.1. SoA Comparison of Mixed Output (Buck & Boost) SIMO Converters.

	Units	[63]	[78]	[67]	[64]	Proposed
Notes	–	I-PWM, V-PK Energy Buffer	Fully PWM Energy Buffer	Fully PWM	Fully PWM	Fully Hysteretic
L_{MIN}	µs	0.5	0.25	0.25	0.25	0.6
A_{SI}	mm^2	3.6	10	2.1	3.8	2.8
v_{IN}	V	2.5–4.5	2.7	0.9–1.6	1.8–2.2	2.7–4.0
v_O	V	2–12	1.8–3.3	0.6, 1.8	1.25–2.25	1.2–4.0
$i_{O(MAX)}$	mA	145	650	240	400	180
N_O	#	5	4	2	4	3
N_{OC}	#	10	5	3	5	4
$\eta_{C(PK)}$	%	83	91	92	93	87
$\eta_{C(FL)}$	%	–[1]	74	92	92	81
t_R	µs	–[1]	10[2]	–[1]	–[1]	10
RFoM	%	39[3]	49	90[3]	100[3]	113

[1]Not reported. [2]Estimate. [3]Assumes t_R = 10 µs for comparison.

5.5 Summary

Microsystems that optimizes subsystems, such as sensing, processing and transmission; requires different voltage supplies for optimal performance. In some operating conditions, it requires a mix of regulated buck and boost voltages. Luckily, when the energy packet of the inductor is shared among all outputs in one switching cycle, the distribution sequence can be used to generate both buck and boost voltages with few modifications.

The proposed converter has a triple-output buck power stage that can regulate two bucks and one boost output. It can regulate a boosted output because it receives energy last when inductor de-energizes. This operating mode continues if the buck load is high enough that the inductor can fully energize when only supplying energy to buck outputs. This five-

switch operating mode behaves like a triple buck converter which results in same stability criteria, and similar performance in regulation.

Unfortunately, as for microsystems that have dynamic power consumption for each sub-system, the buck power is not always required or high enough to fully energize the inductor to deliver to the boosted output. In such cases that the inductor already satisfied buck outputs but still requires more energy, the power stage uses an additional switch to ground to extend energizing. This six-switch operation results in higher power losses due to the extra switch but not significant to negate the size and simplicity benefits.

The mode transition between five- and six-switch operation occurs when the five-switch mode reaches the maximum boost power it can provide while energizing entirely on the two buck outputs. This boost power limit increases as input supply increases, and buck power increases because it respectively decreases energizing time or shorten the time the boost output connects to the inductor.

The six-switch mode adds a right-half plane zero that must be considered in the design and analysis. As in boost converter, this result because when inductor energizes to ground, none of the outputs receives energy. This implies that it must energize further to compensate for the additional droop from the time of all the outputs discharged simultaneously.

The proposed triple-output buck-boost supply system can regulate three outputs while minimizing switching transitions only when necessary. This keep losses low when operating in the five-switch mode. Although losses increase when in the six-switch mode, the extra switch engages for a brief period of time which keeps its size relatively low and

hence does not increases silicon real estate and losses considerably. This helps to maintain a compact and efficiency power management system for microsystems capable of regulating buck and boost voltages.

CHAPTER 6

BALANCING SPEED AND ACCURACY WITH PROPOSED HYSTERETIC–PWM CONTROL

A fully hysteretic control implementation can achieve sub 10-µs response time as shown in Chapter 4 and 5. However, using a hysteretic comparator to directly regulate an output voltage is noise sensitive from switching noise generated by parasitic resistances and inductances from external components and PCB traces. Although noise can be reduced through filtering, filters can increase the external component count or silicon real state in the die. Alternatively, output voltage comparator can have a large hysteretic window to reduce noise sensitivity at the expense of imposing a larger minimum output voltage ripple that can reach tens of millivolts. This chapter proposes the combination of PWM and hysteretic control to reduce noise sensitivity while preserving the dynamic performance benefits of hysteretic control.

6.1 PWM–Hysteretic Power Supply System

Current-mode control transforms the inductor L_O into a voltage-dependent current source G_{OSC} and as a result its pole in the main loop disappears. Therefore, using hysteretic control for current regulation, as in Figure 6.1, allows to push system's bandwidth to higher levels compared to PWM control. The dual–supply requires an additional control loop for the independent output. For this, a simple high-bandwidth PWM control can regulate the energy of the independently control output v_{OI} and allow the L_O's remnant energy to flow to the master output v_{OM}. Additionally, the proposed controller adds amplifiers to improve

accuracy of regulation instead of buffering the output errors as in previously discussed control schemes in Chapter 4 and 5.

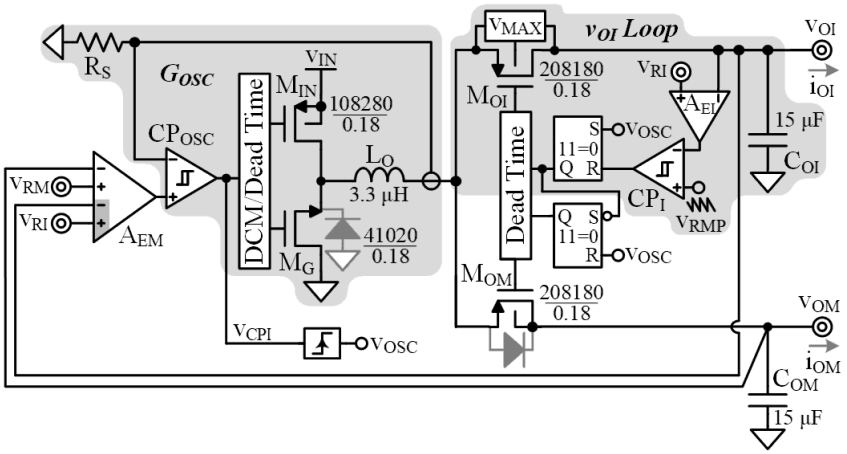


Figure 6.1. Proposed PWM–Hysteretic dual-output power supply system.

The operation of the dual-supply system is like the fully hysteretic converter previously discussed. The current loop will energize the inductor for time t_E until it can supply both outputs as in Figure 6.2. The PWM loop connects the independent output v_{OI} for time t_{OI} until it receives enough energy while master output v_{OM} receives energy for time t_{OM} or the remaining of the switching period.

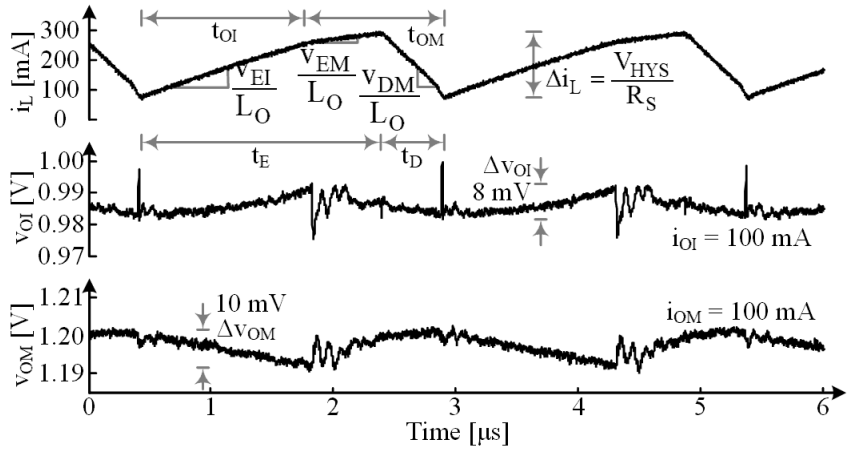


Figure 6.2. Measured waveforms of proposed PWM–hysteretic dual-supply.

The fact that v_{OI}'s PWM control loop is less sensitive to noise, it allows for lower voltage ripple across the outputs. Because the loop regulates the average voltage on v_{OI}, and an amplifier A_{EI} amplifies v_{OI} with limited bandwidth, comparator can have a lower hysteretic window, just enough to ensure a robust comparison. That is why Figure 6.2 shows 10 mV or less across the outputs at maximum load of 100 mA on each output.

6.2 Load Regulation Cross–regulation

Summing all outputs' errors at the current loop improves transient performance and helps to regulate when there is load disparity across outputs. However, at the same time any deviation from the target, such as with load regulation, on the independently controlled output v_{OI} (or outputs if more than two) will appear in the master output v_{OM} as an offset and hence error. The proposed PWM–hysteretic control, adds a filter across v_{OI}'s mixing point in the current loop to reduces cross–regulation to v_{OM}.

6.2.1 Non-Filtered Error Summation

Figure 6.3 shows simulation results when summing amplifier adds all output voltages errors. Due to finite gain across v_{OI}, its average, or dc, voltage decreases as its load level i_{OI} increases. Summing amplifier A_{EM} will drive the total difference across its inputs to zero by adjusting the inductor current i_L target to the appropriate level. Thus, as v_{OI} decreases with increasing i_{OI}, v_{OM} increases by the same amount even though v_{OM} keeps the same load level at half the full–load 50 mV while sweeping v_{OI}'s load.

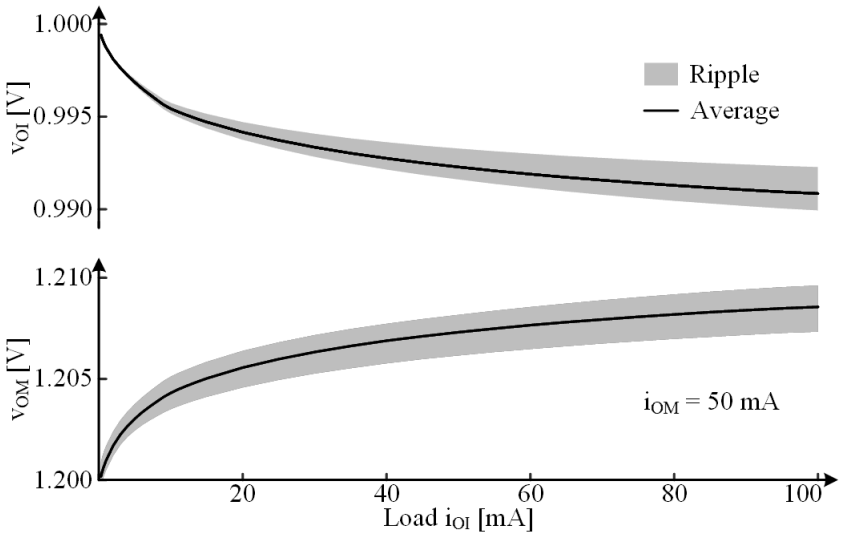


Figure 6.3. Simulated load regulation of v_{OI} and cross–regulation to v_{OM} while summing all frequency components of v_{OI} in the current loop.

6.2.2 High–frequency v_{OI}'s Error Summation

Including a filter that attenuates frequencies lower than 8 kHz from v_{OI} at the summing amplifier reduces the cross–over regulation. In Figure 6.4, simulations show that v_{OI} has the same load regulation as the main control loop, its local PWM control, has the same finite gain as when summing all frequencies. However, v_{OM} has the same finite gain but unlike in Figure 6.3, summing amplifier A_{EM} drivers only v_{OM}'s error to zero at low frequencies since A_{EM} filters v_{OI}'s low-frequency components. Therefore, v_{OM}'s low-frequency cross–regulation is negligible when kept at a fixed load. Interestingly, Figure 6.4 also shows voltage ripple decrease on v_{OM} when v_{OI}'s load decreases even though v_{OM} has a fixed 50 mA load. This happens because inductor current level i_L matches more closely that of v_{OM}'s load i_{OM} and the connection time is longer. This allows the capacitor to receive or deliver only the difference in current between i_L and i_{OM} for longer times, resembling a buck converter, hence reducing ripple.

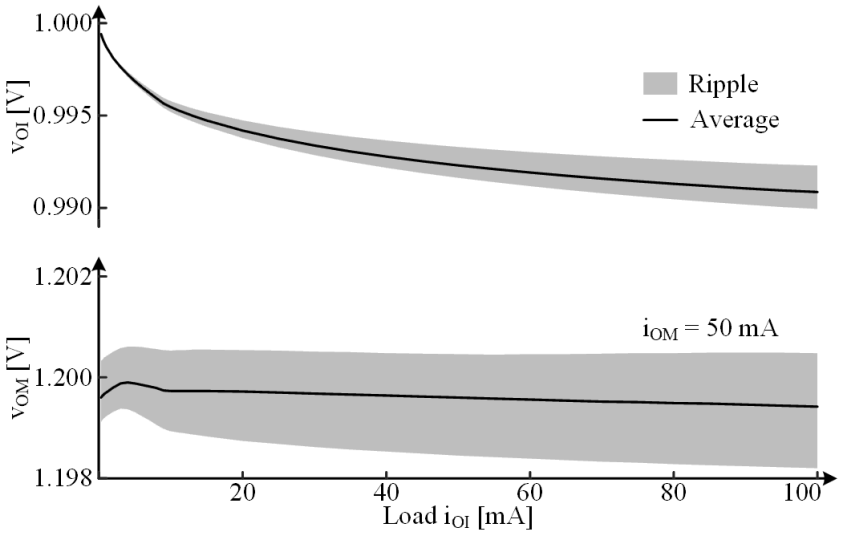


Figure 6.4. Simulated load regulation of v_{OI} and cross–regulation to v_{OM} while summing all frequency components higher than 8kHz of v_{OI} in the current loop.

6.3 PWM Independent Loop Control

The PWM loop across independently controlled output v_{OI} reduces noise sensitive. However, even though a high bandwidth can be achieved, the modulation of its duty cycle differs from the hysteretic. This section explores its differences and how it will affect the stability while also taking in account the filtered mixing point in the current loop.

6.3.1 Operation

The PWM control for independent outputs consists of an error amplifier A_{EI}, a ramp signal v_{RMP}, and a comparator CP_I as Figure 6.5 (a) shows. At the beginning of a new cycle, indicated with pulse signal v_{OSC}, sets the latch for v_{OI} to start receiving energy. At that point switch M_{OI} turns on v_{RMP} starts increasing until it surpasses a reference point v_{EI} defined by the output of A_{EI}. This reference v_{EI} is proportional to v_{OI}'s error and sets v_{OI}'s on time t_{OI} and hence when M_{OI} turns off as in Figure 6.5 (b).

When having a load disparity among the outputs, skipping outputs improves regulation as the converter focus on outputs with heavier loads and avoids overcharging those with light loads. To have the ability to skip the output, CP_I must have a logic high at the output at the beginning of a cycle, when v_{OSC} has a pulse, so that the reset-dominant latch does not engages M_{OI}. For that, the A_{EI}'s output must go lower than the minimum value of v_{RMP} after a reset or $v_{RMP(MIN)}$. That is why Figure 6.5 (b) highlights that the low end of input common-mode range of CP_I $v_{CPI(ICMR)}$ must be lower than v_{RMP}. Also, A_{EI}'s output must be able to swing below $v_{RMP(MIN)}$ as well.

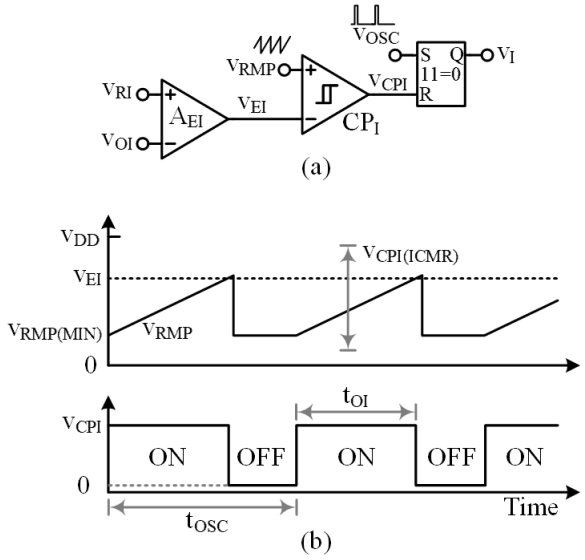


Figure 6.5. PWM control for independent output v_{OI} (a) schematic and (b) operating waveforms.

6.3.2 Stability

Although the proposed PWM differs from hysteretic control on how the modulation occurs, the loop gain analysis and incorporation into the master loop follows the same approach as previously discussed. When a deviation on the output v_{oi} occurs, it changes the amplified error v_{ei} through gain A_{EI}. This in turn updates the duty cycle d_{oi} through v_{RMP} with

modulation gain of A_{PWM}. This change in connection increases (or decreases) the current i_{oi} that output v_{OI} receives proportionally to the average inductor current I_L in steady–state which in turns update v_{oi} through its output impedance and sets the total loop gain $A_{OI.M}$:

$$A_{OI.M} = \left(\frac{v_{ei}}{v_{oi}}\right)\left(\frac{d_{oi}}{v_{ei}}\right)\left(\frac{i_{oi}}{d_{oi}}\right)\left(\frac{v_{oi}}{i_{oi}}\right) = A_{EI}\left(A_{PWM}\right)\left(I_L\right)\left(R_{OI} \parallel \frac{1}{sC_{OI}}\right). \quad (6.1)$$

The modulation gain A_{PWM} defines how much duty d_{oi} changes from voltage v_{ei} through change in connection time t_{oi}. This happens through modulating ramp v_{RMP} as its rate of change determines change in t_{oi} with respect to amplifier error v_{ei}. This change t_{oi} with respect to total period t_{OSC} gives duty change d_{oi} and defines total modulation gain:

$$A_{PWM} = \left(\frac{t_{oi}}{v_{ei}}\right)\left(\frac{d_{oi}}{t_{oi}}\right) = \left(\frac{dv_{RAMP}}{dt}\right)^{-1}\left(\frac{1}{t_{OSC}}\right). \quad (6.2)$$

Since the control implementation sums v_{OI}'s error higher than a certain frequency from to that of v_{OM}'s, the path through the mixing point and current loop provides a feed-forward path with gain $A_{OI.S}$ to v_{OI}. This effectively increases loop gain near the cross-over frequency which can affect stability depending on the design and application. A change in output error v_{oi} higher than the corner frequency f_{SUM} that summing happens, will change error reference to the current loop v_{em} through summing amplifier gain A_{EM}. This change prompts the current loop to update inductor current i_l according to its close-loop gain $1/R_S$, which increases, or decreases, current ioi into v_{OI} proportionally to the steady–state duty cycle D_{OI}. Finally, the extra, or less, current ioi updates v_{OI} through its output impedance:

$$A_{OI.S}\Big|_{f>f_{SUM}} = \left(\frac{v_{em}}{v_{oi}}\right)\left(\frac{i_l}{v_{em}}\right)\left(\frac{i_{oi}}{i_l}\right)\left(\frac{v_{oi}}{i_{oi}}\right) = A_{EM}\left(\frac{1}{R_S}\right)\left(D_{OI}\right)\left(R_{OI} \parallel \frac{1}{sC_{OI}}\right). \quad (6.3)$$

Under the assumption that f_{SUM} is well below the cross-over frequency $f_{OI.0dB}$, both paths contribute to the total gain. Hence adding both gain and equation to one, gives $f_{OI.0dB}$:

$$f_{OI.0dB} = \frac{A_{EI}A_{PWM}I_L + \frac{A_{EM}D_{OI}}{R_S}}{2\pi C_{OI}}. \tag{6.4}$$

Since D_{OI} approximates to i_{OI}/I_L and I_L to $i_{OI} + i_{OM}$, and assuming A_{EI} are at a similar level, $A_{OI.S}$ becomes influential when:

$$\frac{d_{OI}}{\left(i_{OI} + i_{OM}\right)} > R_S A_{PWM}. \tag{6.5}$$

This means, that when i_{OM} is very light–load so that the left terms approximate to $1/i_{OI}$ can be relatively higher than $R_S A_{PWM}$ and become the dominant term in the loop gain. However, when i_{OM} is high so that d_{OI} is below one and closer to zero, the left term most likely is below $R_S A_{PWM}$. This is how the feedforward path helps to keep v_{OI} in regulation when v_{OM} has a very light load but has less influence otherwise.

6.3.3 Dynamic Response

Unlike the hysteretic control, the PWM loop regulate the average output voltage instead of an instantaneous value such as the v_{OI}'s peak voltage in hysteretic control. Therefore, v_{OI} would not completely recover after a load dump in one cycle. Instead, it will require multiple cycles to completely recover. However, because the hysteretic current loop has a high bandwidth and recovers quickly, PWM loop across v_{OI} can have high bandwidth to minimize response and recovering time after a load dump.

On the rising load dump of a simultaneous 10–100 mA load step on both v_{OI} and v_{OM}, the converter responds in 10 µs. In that time v_{OI}'s error reaches −33 mV or −3.3% of

a 1 V target and v_{OM} increases by 14 mV or 1.2% of 1.2V as in Figure 6.6. After the response time, takes about 12 µs to completely recover to the target while v_{OM} does in about 15 µs.

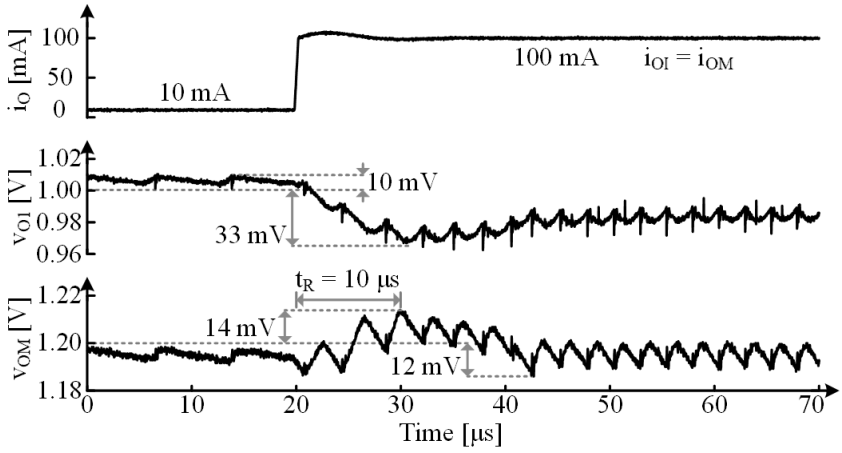


Figure 6.6. Measured response to simultaneous rising 90-mA load dumps.

Figure 6.7 displays the response to simultaneous falling load dumps of 90 mA on each output. The converter responds within 4 µs for the falling load dump in which v_{OI} increases by 15 mV or 1.5 % and v_{OM}'s error is −16 mV or −1.3%. Because of the light load condition on v_{OM}, it completely recover after an additional 60 µs while the light load discharges the output capacitance back to the target voltage.

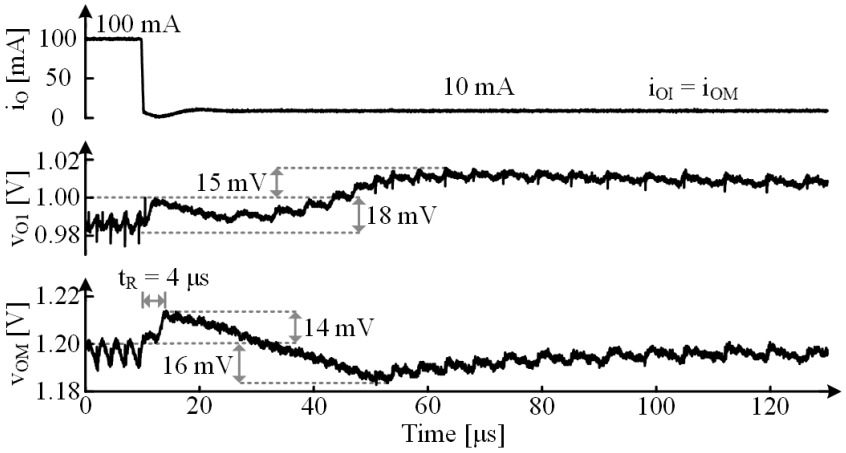


Figure 6.7. Measured response to simultaneous falling 90-mA load dumps.

6.4 Implementation

The prototype of the proposed PWM–hysteretic controller was implemented in a 0.18 µm CMOS technology. The target of the output voltages is 1 V for v_{OI} and 1.2 for v_{OM} when the input voltage is within the range of 1.4−1.8 V. Figure 6.8 shows the die of the prototype which includes power switches, drivers and control. It occupies a total area of 1.6 mm^2 including the bond pads.

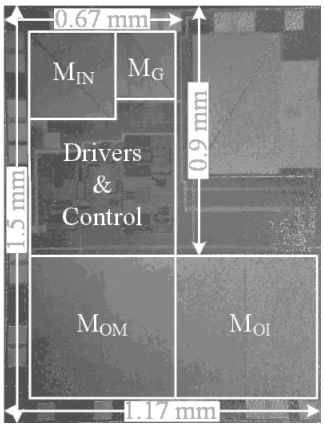


Figure 6.8. Die of proposed PWM–hysteretic controller in 0.18 µm CMOS process.

Figure 6.9 shows the PCB boars to test and evaluate the prototype. Besides the prototyped IC, it includes inductor L_O, output capacitors (C_{OI} and C_{OM}), inductor current sensing, load emulator and test circuits. It occupies a total area of 10.2 × 8.6 cm^2 for a two-layer board.

The implementation of the prototype requires some consideration when designing the IC. Among such are bulk biasing of the power switch, current sensor design, input common–mode considerations for amplifiers and comparators. Albeit a few differences with other technologies such as the type of transistors and passives availability, the concepts can be implemented in all technologies.

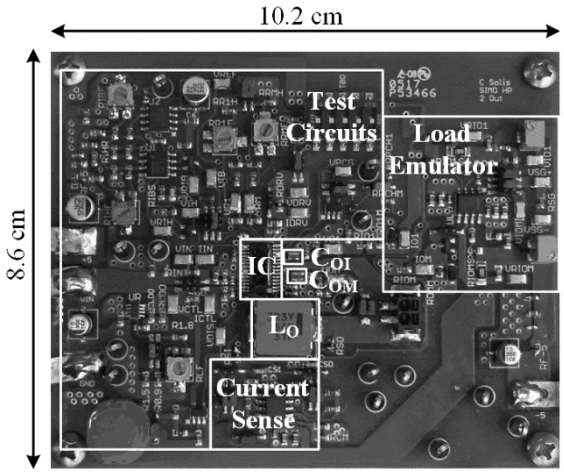


Figure 6.9. Testing PCB to measure performance of the dual-supply system.

6.4.1 Power Switch Bulk Bias Circuit

By design, current in the inductor freewheels to one of the output voltages during the deadtime period. In the proposed design, master output v_{OM} power switch's body diode serves this purpose. However, the other (or others if more than two) output must block any current flow by using a back-to-back diode configuration when the switch is off. This prevents energy sharing among the outputs as the output switching node moves during switching transitions. A simple implementation is using two PMOS switches in series and connect their bulk connections at the intermediate node to achieve back-to-back connection of their body diodes. However, driving two gates and having two series resistances increases total power loss across the switch [79].

Figure 6.10 shows the implementation that consists of a single power switch and two cross-coupled switches to bias the bulk node v_{BULK}. Connections of the bulk connections allow all the body diodes to conduct to the bulk and function as a peak voltage detector. During the dead-time period, as v_{SWO} goes a diode above v_{OM}, transistor M_{BU1}

has enough overdrive to increase the bulk voltage as in this design v_{OI} is lower than v_{OM}. If control engages switch M_{OI}, M_{BU1} will discharge the bulk up to a threshold above output voltage or $v_{O1} + v_{THN}$. This allows to minimize the bulk effect when the switch is on to keep lower switch resistance. Transistor M_{BU2} seldom engages during normal operation as the bulk voltage v_{BULK} does not need to go below v_{OI}. However, its relatively small size keeps the functionality of keeping the bulk biased to the highest potential during transient events and, combined with its higher threshold voltage compared to M_{BU1} minimizes leakage current through the cross-coupled bulk-biasing transistors.

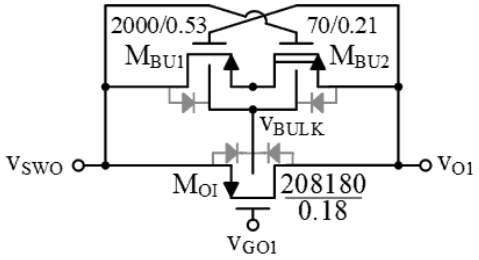


Figure 6.10. Circuit to bias bulk of power switch of independent output v_{OI}.

6.4.2 External Current Sensor

Like the proposed dual-supply system in Chapter 4, the current sensing implementation for the proposed PWM–Hysteretic power supply uses an RC to sense the inductor current. However, because of the small energizing and de-energizing voltage across the inductor, the inductance is lower to meet inductor slewing demands to achieve fast transient response. Due to the lower inductance and because sensing gain is L_O/R_SC_S, the RC filter time constant t_S is lower to achieve similar or higher bandwidth in the master loop as discussed on the current sensor design of Chapter 4.

When energizing and de-energizing times are much lower than τ_S the response of the RC sensor is approximately linear and the reason it can replicate the shape of the inductor current. Unfortunately, during a relatively large response time or switching period, the RC filter will show an exponential voltage across sensing capacitor when ideally it should be linear. This creates a sensing error e_{SEN} from the ideal response which becomes a function of the time t at a single state (i.e. long energizing or de-enegizing) relative to τ_S:

$$e_{SEN} = \frac{v_L\left(1-e^{-\frac{t}{\tau_S}}\right)-v_L\left(\frac{t}{\tau_S}\right)}{v_L\left(\frac{t}{\tau_S}\right)} = \frac{\left(1-e^{-\frac{t}{\tau_S}}\right)-\left(\frac{t}{\tau_S}\right)}{\frac{t}{\tau_S}}. \tag{6.6}$$

To maintain an error lower than 10%, time at any state should be lower than $0.2\tau_S$. With a total sensing gain of one, means that τ_S must be 3.3 μs for a 3.3 μH inductor. This limit any energizing or de-energizing state, during steady–state or a transient, to be below 0.66 μs. However, a transient event can easily take over this limit even for fast responding converters. As a trade–off, Figure 6.11 includes a discrete differential amplifier with a small gain of ten. Amplifying the output of the current sensor, allows to use a higher τ_S while maintaining the same current sensing gain. In this case, the time in any state can be within 6.6 μs to limit the error within 10% which is more suitable for the proposed control. Even though differential amplifier might be integrated, a discrete amplifier was used for testing and debugging purposes such as to adjust its gain.

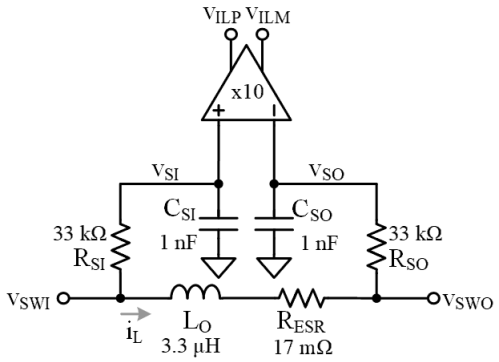


Figure 6.11. Current sensor implementation for low voltage converters.

6.4.3 Summing Amplifier

Figure 6.12 shows the circuit implementation of the summing amplifier A_{EM} that filters out the dc component of independent output voltage v_{OI}. To achieve this summing above a certain frequency f_{SUM}, a RC filter is included across the input terminals for v_{OI} or $v_{1P–1M}$. This way, above f_{SUM}, the differential pairs have matching gain since they sum each differential current at the folding stage before reaching output nodes v_{OP} and v_{OM}. When the frequency of the input signal is below the cutoff frequency f_{SUM}, amplifier only consider master output v_{OM} to adjust inductor current level which reduces cross–regulation from v_{OI} to v_{OM}.

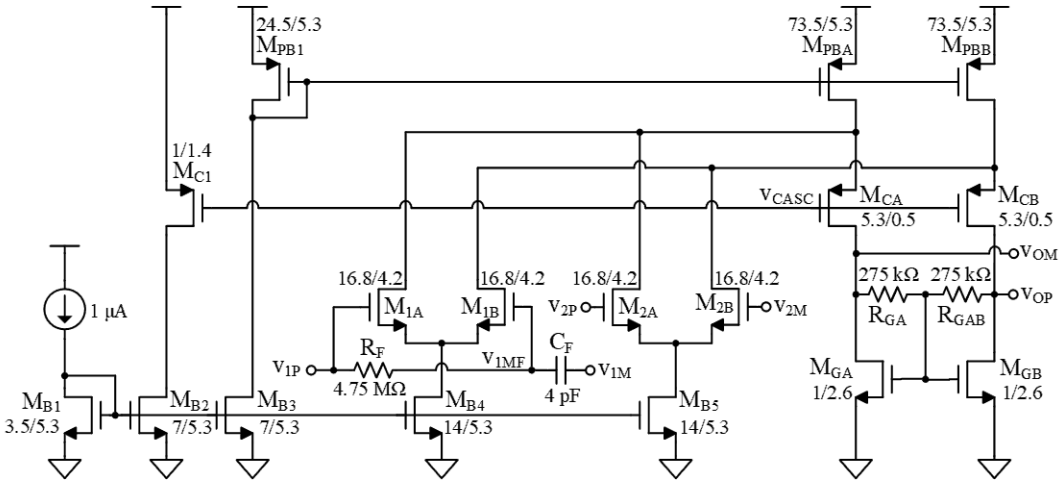


Figure 6.12. Summing amplifier A_{EM} implementation in 0.18 µm CMOS process.

The implementation of the RC filter consists of a resistor R_F in between input terminals of the differential stage, and a capacitor C_F between the v_{OI}'s feedback point and the negative terminal v_{IMF} as in Figure 6.12. To maintain high linearity against voltage, a poly-poly capacitor is used for C_F but the bottom poly or plate must be connected to the feedback point of v_{O1}. Otherwise, a voltage divider results between feedback point to ground due to the bottom poly-substrate capacitance [108], effective reducing the total gain of v_{OI} across A_{EM} relative to that of v_{OM}. The corner frequency of the R_F–C_F filter in this design is 8.4 kHz, low enough to for the filter's gain to settle before any crossover frequency of any loop. This avoids interaction with the other loops and does not affect previous stability analysis discussed.

Another implementation alternative is to degenerate the gain of the differential pair at low frequencies as Figure 6.13 suggests. At low frequencies, the gain is reduced by the degeneration magnitude $1/(1+g_{m1}R_{DEG})$. As frequency increases past $1/(2\pi\times 2C_FR_{DEG})$, the gain of the input pair increases until capacitor's impedance is well below transconductance g_m of the input differential pair. In this design g_m was approximately 40 μs, and achieving the same corner frequency as the circuit in Figure 6.12 would require a C_F of 760 pF which is prohibitively large. To balance size, implementation in this design uses the R_FC_F filter but depending on the application requirements using resistor degeneration might be feasible or even optimal choice.

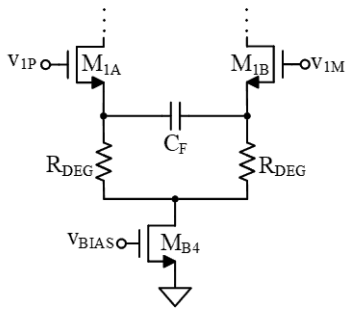


Figure 6.13 Filtered summing implementation alternative.

6.4.4 Hysteretic Comparator CP_{OSC}

Hysteretic comparator CP_{OSC} mixes the output error from amplifier A_{EM} and sensed inductor current. Since A_{EM} provides a differential signal as the current sensing circuit also does, CP_{OSC} consists of input differential pairs that mixes current in a folding cascode pre–amplifier as in Figure 6.14. The differential implementations avoid conversion to a single-ended signal and reduces noise sensitivity to noise injected due to routing in the die and PCB [109]. This implementation follows the same approach as the summing comparator discussed in Chapter 4. It has an initial pre–amplifier stage with a small gain followed by multiple small-gain amplifier stages that ends with a large-gain single-ended class A amplifier. This way, the amplifier can have balanced quiescent current and speed.

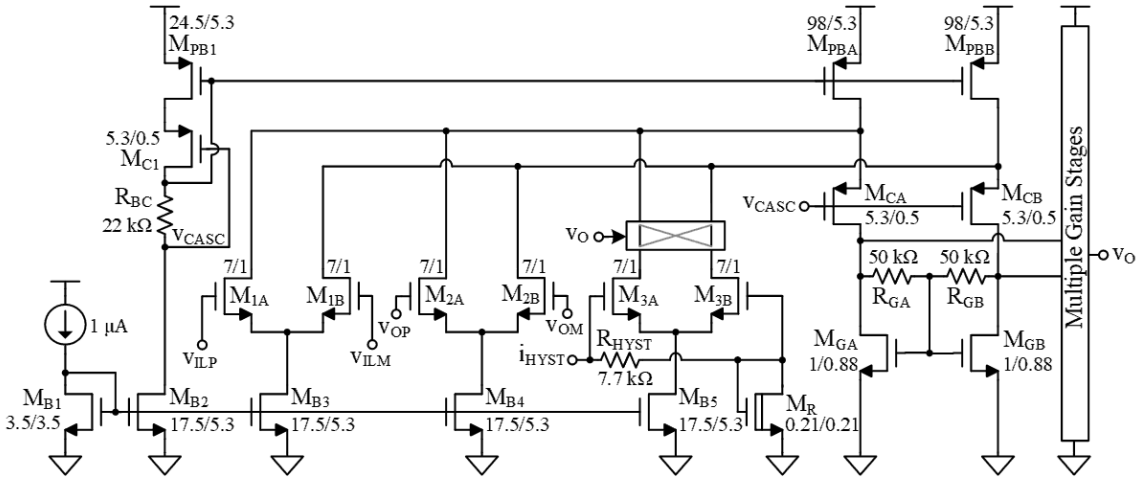


Figure 6.14. Pre–amplification of hysteretic comparator CP_{OSC} of the current loop.

On this implementation, however, a current i_{HYST} flowing through a resistor R_{HYST} sets half of the hysteretic voltage across an additional differential pair, $M_{3A–B}$ in Figure 6.14, while a diode connected transistor M_R sets a reference on one input of the differential pair. This method is easier to integrate and provides a low impedance to shunt noise that the node might encounter while connecting to a test circuit on the PCB board. M_R is a high threshold device to allow common-mode voltage at the input pair to track and be within the comparator's common-mode range.

6.4.5 PWM Control

As explained in section 6.3, the PWM control consist of error amplifier A_{EI}, ramp signal v_{RMP} and comparator CP_I. A_{EI} uses a folded cascode implementation, shown in Figure 6.15 to use a NMOS input differential pair and be compatible with the input-common range (ICMR) of CP_I. The target gain for this amplifier is about 10 V/V set by the input pair's g_m and output resistance $R_{GA–B}$. Using diode-connected NMOS transistors through resistors decouples the bias point at the output node and gain. The bias point is set by the gate-source voltage across transistors $M_{GA–B}$ since there is no current flowing through the resistors. In the other hand, the small-signal gain is set by resistors $R_{GA–B}$. This helps to ensure the output is within CP_I's ICMR which uses an NMOS differential pair.

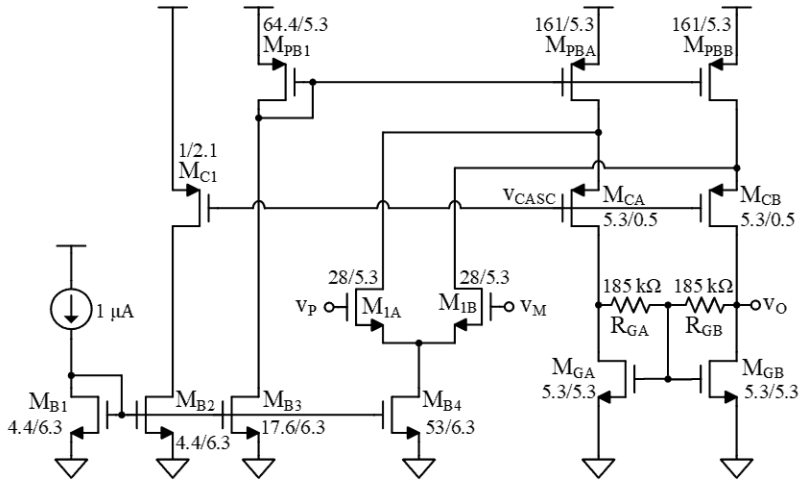


Figure 6.15. PWM loop's A_{EI} implementation.

A current that charge a capacitor implements the modulating ramp v_{RMP} as in Figure 6.16. A diode-connected high-threshold NMOS M_{LS} ensures v_{RMP} has a minimum voltage within CP_I's input common-mode range and higher than A_{EI}'s output voltage range. It is to this value that v_{RMP} resets every cycle before increasing at a nominal rate of 0.12 V/µs. NMOS and PMOS switches M_{RS1} and M_{RS2} resets the ramp every cycle and both are required since v_{RMP} has a typical range a diode above ground and a couple hundred millivolts below the supply.

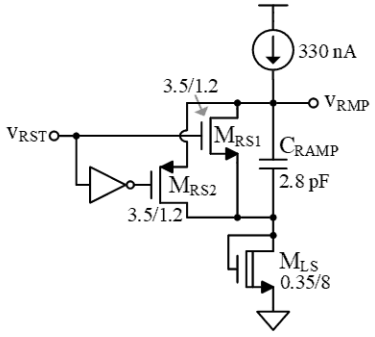


Figure 6.16. Modulating ramp for PWM control of independent voltage v_{OI}.

Figure 6.17 show comparator CP_I's implementation in the prototyped IC. It has a NMOS input differential pair going to a folding cascode output stage as the pre-amplifier

stage. Then a second stage provides high gain while a class–A stage ensures the output signal goes rail to rail. The output signal goes through additional inverters to sharpen the edges of the output signal v_O and provide enough signal strength for parasitic capacitances. The small hysteresis to avoid a false trip during the transitions due to noise is implemented before the class-A stage by engaging a sinking current after the CP_I's output goes logic high. Engaging hysteresis after CP_I goes high helps having an accurate comparison as v_{OI} rises (when it is receiving energy).

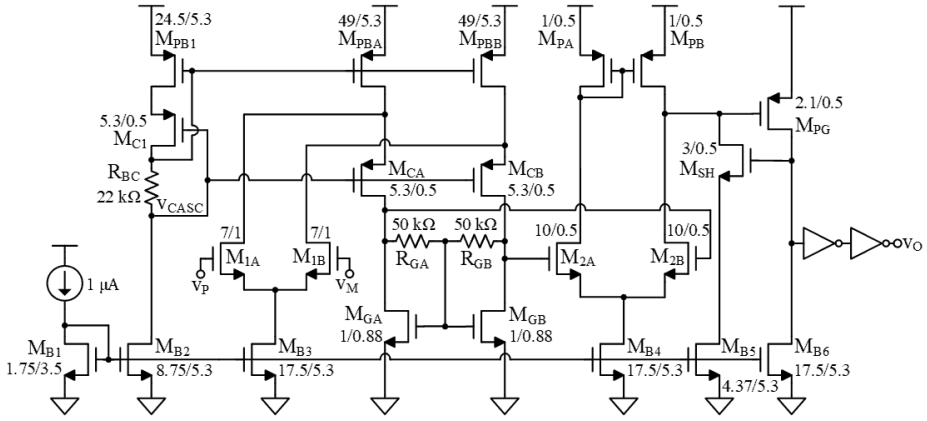


Figure 6.17. PWM loop's CP_I CMOS implementation.

6.4.6 Scalable Output Logic

Despite designing a dual-output supply, the logic for output sequencing was designed to allow easy scaling while increasing the number of regulated output voltages. Unfortunately, combinational logic requires anticipating possible scenarios and figuring which output receives energy first at the beginning of each cycle as shown in Chapter 5. Conceptually, the proposed scalable logic enables every output to receive energy in sequence and it passes control to the next output after receiving enough energy or if it is being skipped. One key is to use reset-dominant latches so even if the logic tries to enable

output to receive energy, its comparator, from the PWM loop or hysteretic control, can force the output to be skipped if it is already satisfied.

Figure 6.18 shows the circuit diagram for such scalable logic control. The first independently controlled output v_{O1} will receive energy at the beginning of a new cycle, when pulse signal v_{OSC} goes high sets v_{O1}'s latch. If v_{O1} is already satisfied, output of comparator or signal v_{CP1} is high and keep the output from engaging. v_{O2} will engage either when v_{O1} receives enough energy and v_{O1}'s latch resets or if v_{O1} was skipped. During the later, v_{O2}'s latch sets if v_{O1}'s comparator is high and v_{OSC} pulse starts to fall. This means that v_{O1} can engage as long as v_{OSC} is high when v_{O1}'s latch has a logic high at the set input, if it does not at the end of v_{OSC}'s pulse, then v_{O1} is skipped and v_{O2} engages. The sequence continues for the other outputs until the last output v_{OM} engages until the remaining of the period where at the next pulse at v_{OSC}, v_{OM}'s latch resets.

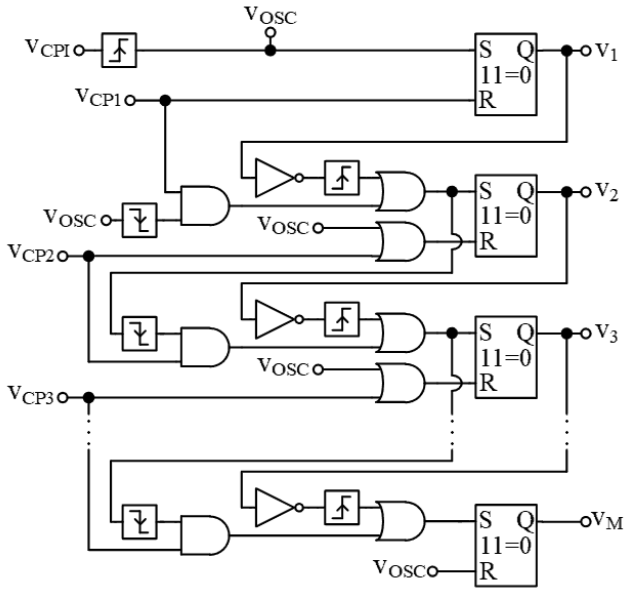


Figure 6.18. Scalable output logic that sequences the output by priority.

Unlike the previous approach of using combinational logic, the sequence tries to set each latch of every output. As a result, the pulses at each set input of the latch represents a delay to engage the following output if the previous output (or outputs) is being skipped. For instance, if at the beginning of a new cycle, v_{O1} and v_{O2} are satisfied already, v_{O3} has to wait past the pulse of v_{OSC} and the pulse at the set input of v_{O2}'s latch (after v_{OSC} goes low) to finally engage. This results in additional dead–time period as these pulses are around tens of nanoseconds to gives enough time to the logic to settle. Also, the pulse from v_{OSC} must be wider than the other pulses generated in the sequence to allow enough time for all latches to reset even as disengaging one output is interpreted as if it has received enough energy.

6.5 SIDO Measured Performance

Figure 6.19 shows v_{OI}'s load regulation of the proposed dual-supply converter. During continuous-conduction mode (CCM) operation, the converter regulates both outputs with a finite output resistance which makes their dc value decrease as both load increases at a rate of 0.24 mV/mA. When v_{OI}'s load is fixed to 20 mA the output voltages settle and changes less versus v_{OM}'s load. Due to its priority to receive energy first at the beginning of each cycle, v_{OI} have low cross–regulation from v_{OM}.

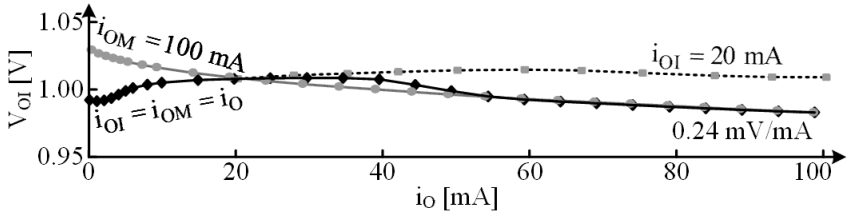


Figure 6.19. Measured load regulation of independent output v_{OI}.

Similarly, master output v_{OM} has a finite close-loop output impedance in regulation and therefore its output decreases as load increases as in Figure 6.20. When v_{OM} has a 100–mA constant load, its value changes slightly at a rate of 0.02 mV/mA even though v_{OI} decreases at a rate of 0.24 mV/mA. This reduced low-frequency cross–regulation is due to the decoupling of the low-frequency components from outputs at A_{EM}. During discontinuous conduction mode (DCM), v_{OM} dc voltage decreases with decreasing load since inductor ripple decreases below V_{HYS} and induces a dc offset at the summer that v_{OM} compensates. However, it is less than in the fully-hysteretic control because this implementation includes an amplifier in the master loop instead of a buffer.

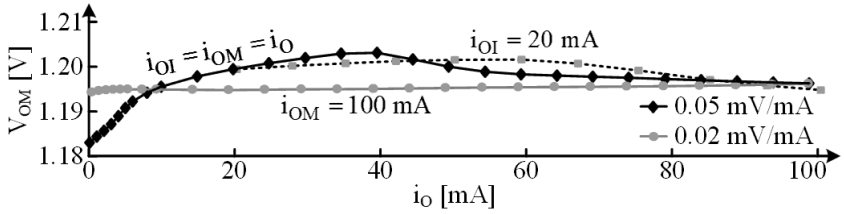


Figure 6.20. Load regulation of master output v_{OI}.

Resistances, switching gates, and the controller consume ohmic, gate-drive and quiescent power. Power transistors balance gate-drive and ohmic losses by optimally sizing their widths with minimum channel length. With the resulting design, the peak efficiency $\eta_{C(PK)}$ for the proposed controller is 94% when delivering full load to v_{OM} and less than 5 mA to v_{OI} Figure 6.21. At full-load conditions, when each output consume 100 mA, the efficiency $\eta_{C(PK)}$ settles to 91.3%. Also, the converter achieves 85% when delivering more than 2 mA when targets for v_{OI} and v_{OM} are 1− and 1.2−V, and supply is 1.5 V.

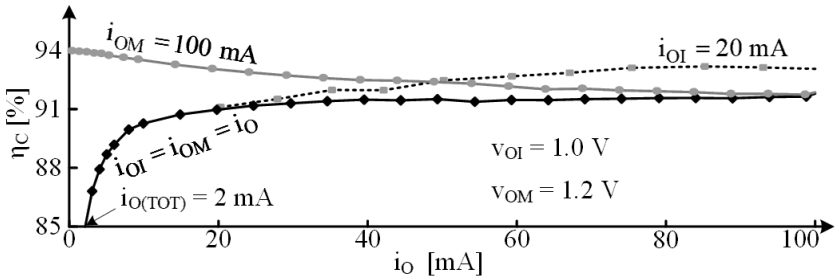


Figure 6.21. Efficiency of PWM–hysterteic SIDO supply system.

6.6 SIDO Comparison to Similar Single-Output

Although saving an inductor and using a single integrated circuit to generate one, or many, additional outputs is an appealing and obvious benefit of a SIMO converter, it is valuable to keep in mind the trade–offs associated with such a topology. The main difference to dedicating a switch-inductor converter to each output is that all outputs are duty–cycled regardless if they are buck or boost voltages. Also, the fact that output shares the inductor current can increase cross–regulation between them as previously discussed.

For the comparison of performance between a single- and dual-supply, the proposed dual-output converter is used for both. To operate the converter as a single output, the independent output voltage is forced high to the supply through a resistor. This forces the converter to sense that v_{OI} is always satisfied and therefore is always skipped in the control logic. Also, to discard performance differences due to the output targets, both outputs are targeted to 1 V in the dual-supply as in the single-supply system.

6.6.1 Power Losses

From an efficiency point of view, the dual-supply incurs in about 4% more losses than the single-supply at higher load levels as Figure 6.22. At light–loads, the difference is higher and dominated by the quiescent power for the output switches control. At mid-load

conditions, gate charge and I–V overlap losses become a dominant while conduction losses dominate as load levels continue to increase. In summary, although using multiple supplies allow energy savings higher than 5% at the system level, the dual supply provides a smaller solution for the application with low percent loss in efficiency.

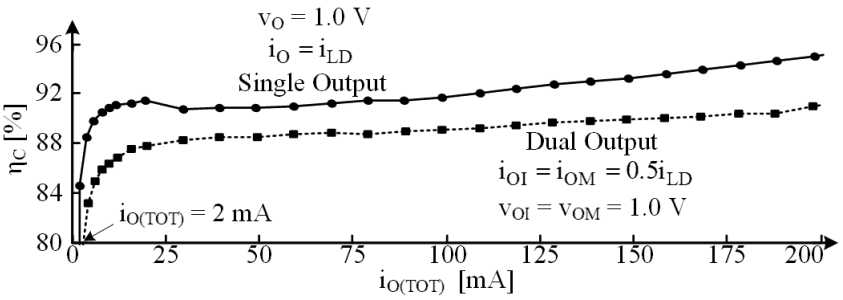


Figure 6.22. Conversion efficiency comparison between single and dual supplies.

To account for topologies inaccuracies, the single-supply efficiency measurements contains two adjustments. First, because there is an unnecessary series power switch, i.e. M_{OM}, in the single-supply topology, its losses were subtracted using the measured output current and M_{OM}'s resistance. Secondly, because v_{OI}'s control is not turned off, its measured quiescent current was subtracted from the total losses measured.

6.6.2 Accuracy

A dual-output converter must duty cycle outputs to share the inductor irrespective if it has buck or boosted outputs. Therefore, the output capacitor C_O must provide the load current i_O when disconnected from L_O. Thus, ripple voltage Δv_O climbs as $i_{O(TOT)}$ increases like in Figure 6.23. For comparison, Figure 6.23 also include the measured ripple for a similar converter delivering same power to a single output. In a single-output buck converter, the output capacitor C_O receives or provides the difference between i_L and load i_O. Hence, in

CCM the ripple is independent of the load level and the lowest since C_O only provides, or receives, a fraction less than the load.

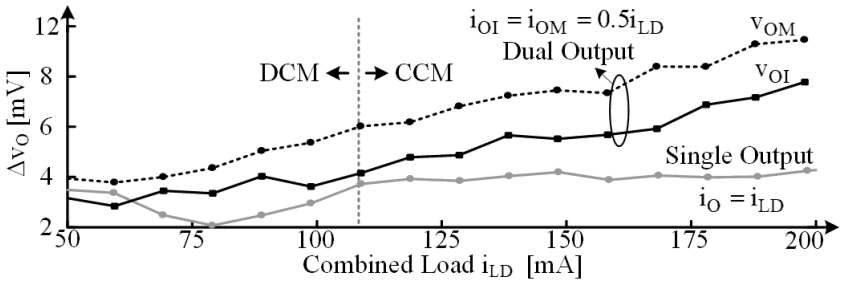


Figure 6.23. Ripple comparison between single and dual supplies.

6.6.3 Dynamic Response

Figure 6.24 shows the response for the dual output, in which it took 10 µs to respond to a rising load step of 180 mA split equally among the outputs when both outputs target 1 V. This is like the response in Figure 6.6 when outputs v_{OI} and v_{OM} target 1 V and 1.2 V respectively. For the falling load dump, Figure 6.25 shows the converter reacting and responding within 4 µs like the response in Figure 6.7. Hence, the response of the dual supply does not change noticeably when the target of v_{OM} is between 1–1.2 V. For comparison with the single-supply converter, the total load change was kept constant so that the inductor moves for the same time to the same levels null its effect.

When responding to rising load step in the single-supply converter, the control takes about 5.6 µs to react and start correcting the output error as in Figure 6.26. Even though the total load is the same as in the dual-supply system, it takes almost have the time to respond. One reason for this is that the output receives energy continuously, and therefore, it does not have to wait for another output to receive energy like in the dual supply. Hence,

sharing the inductor among several outputs adds a delay as each output recovers which would tend to increase as more outputs are being regulated from the same inductor.

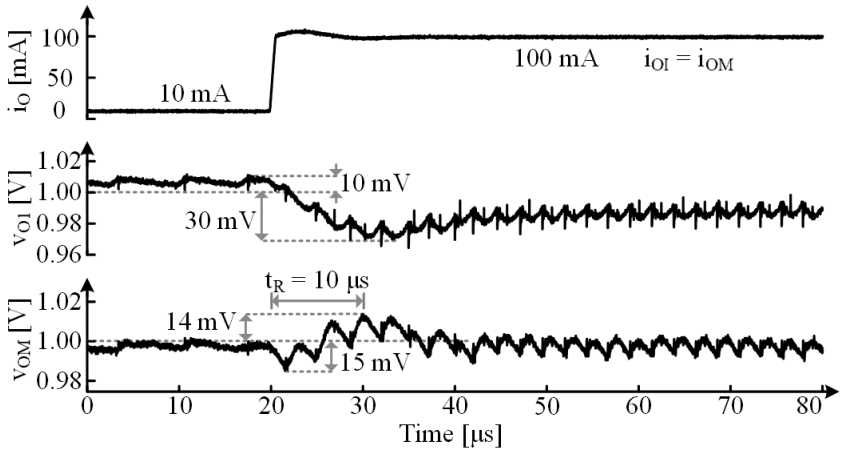


Figure 6.24. Measured dynamic response for a rising load dump in the dual-supply system.

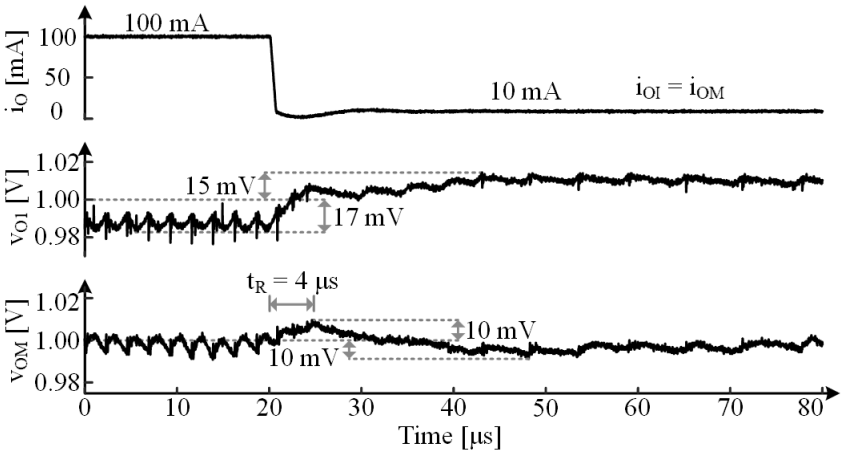


Figure 6.25. Measured dynamic response for a falling load dump in the dual-supply system.

In the case of a falling load dump of 180 mA in the single-supply system, the converter reacts within 3.4 µs as in Figure 6.27. Comparing to the dual-supply system, the converter responds only 0.6 µs faster suggesting that even when supplying multiple outputs, the hysteretic control reacts fast to start decreasing the inductor current to avoid overcharging the outputs.

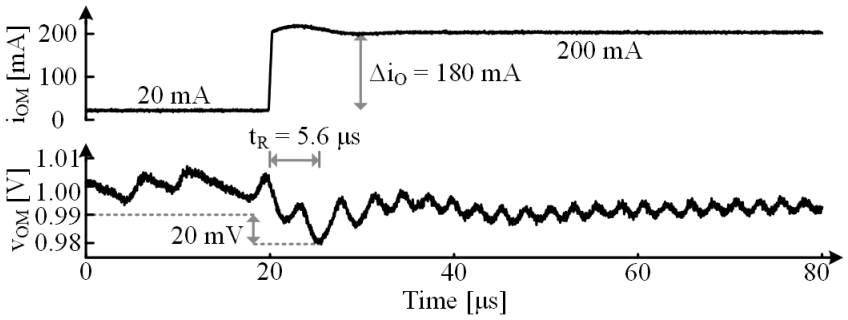


Figure 6.26. Measured dynamic response for a rising load dump in the single-supply system.

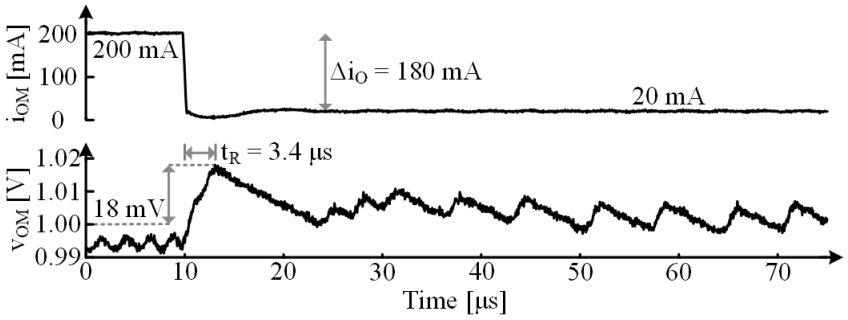


Figure 6.27. Measured dynamic response for a falling load dump in the single-supply system.

6.7 Summary

Hysteretic control for switching converter enjoys fast dynamic performance; however, because it senses instantaneous voltages it is sensitive to noise generated at the IC and board level. That is why, in the previously proposed fully hysteretic converter, the hysteretic comparator that regulates the peak voltage for the independent output requires tens of millivolt of hysteretic window. This results in higher minimum ripple at the output when the target is to share the energy packets in the inductor every cycle among the outputs.

This chapter proposed a balanced tradeoff to keep good dynamic performance but increase accuracy. For this the current loop has hysteretic control to achieve the highest bandwidth. Also, because the independent output does not reside within the master loop, it can have a high bandwidth PWM loop to maintain high speed but decrease noise sensitivity

and therefore output ripple. Although the approach to analyze the stability does not change, this implementation gives more control as the stability is dependent on the amplifier, modulation gain, and the output capacitor.

In addition, this chapter proposed mixing output error in the current loop by summing all frequency components except the low-frequency component of the independent output. This helps to reduce cross regulation to the master loop as the summation would otherwise transfer any error on the independent output as an offset. Simulations and measurements showed that with increasing independent output load, master loop seldom droops if its load is fixed. Also, this summation scheme does not interfere with stability, as the summing starts more than a decade before any other cross-over frequency among the loops.

The implementation on a 0.18 μm CMOS process was also discussed including all components of the PWM loop and current loop. In addition, a new logic control showed that it can be scaled to any number of outputs. Unlike combinational logic which requires anticipating cases, the new sequential logic try to engage all output in a sequence after each one has received enough energy. If an output must be skipped, a reset-dominant latch does not engage but allows the next output to do after its allowed time to engaged has passed. Also, the current sensing was modified to accommodate a lower inductance. In this case, an amplifier with small gain was included to allow the use of a higher time-constant RC filter. This helped reduced error from the exponential response of the filter due to long response times during transients.

Finally, this chapter also compared the single- and dual-supply systems under the same control and operation conditions. The additional switches at the outputs and their respective drivers increase losses by approximately 5% in the dual-supply converter compared to the single supply counterpart. Also, the response time of the converter increased substantially from the single supply to the dual for a rising load dump. This is because in the dual-supply system, master output must wait for independent output to recover, adding a delay in the total response time even though the total load change in both converters. However, for the falling load dump, the converter reacts in a similar amount of time. This is because the hysteretic control in the current loop reacts faster and decreases the inductor current quickly to stop the outputs to keep overcharging.

CHAPTER 7

CONCLUSIONS

7.1 Applications

Portable electronics and microsystems, such as wireless micro sensors, adds intelligence to larger systems leading to energy savings, best use of resources and even saving lives. For this, microsystems incorporate diverse on-board functions such as sensing, data processing and transmission powered by a tiny battery. To optimize energy consumption and battery size, each function has unique voltage requirements while simultaneously adjusting its power consumption proportionally to the workload by means of block-duty cycle and/or voltage scaling. This imposes stricter requirements on supply regulators fur such systems since it must react quickly to load dumps as blocks turn on (or off) while maintaining a high efficiency and compactness.

Also, as battery discharges, it is necessary for the power converter to boost a voltage or voltages such as when transmitting information through power amplifiers. Although inductors are difficult to integrate, switched-inductor converters enjoy a high efficiency across wide operating conditions. Therefore, limiting the converter to a single inductor and generating multiple outputs (i.e. supplies) balances the requirements of high efficiency and compactness for the power-supply system for microsystems and, more generally, portable electronics with several functionalities.

7.2 Single-Inductor Multiple-Output Converters (SIMO)

A single-inductor multiple-output converter shares the inductor among the outputs by partitioning the switching cycle and delivering energy to an output at a time. As an example, a dual-output converter shown in Figure 7.1 stores energy in the inductor L_O while simultaneously delivering energy to output v_{O1}. When inductor has enough stored energy to supply all outputs, the converter begins de-energizing the inductor. Also, when v_{O1} receives sufficient energy, the other output v_{O2} receives energy for the remaining of the cycle. The time allocation for each output during the switching period is proportionally dependent on each output's load level relative to the other. In other words, the heavier the load is the longer the fraction of time connected to the inductor.

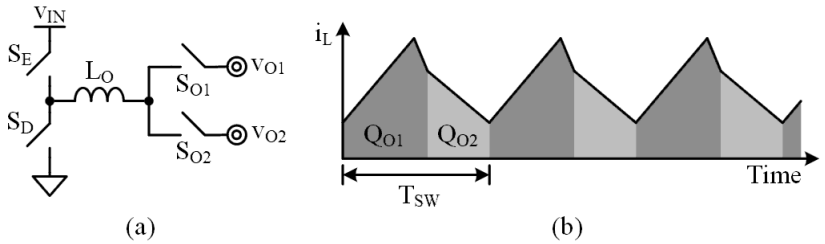


Figure 7.1. (a) A dual-output converter and (b) its operating waveform when sharing the energy packet.

Literature presents full current-mode PWM control as the most common method to regulates a SIMO converter. It consists of a current-mode PWM to regulate energy stored in the inductor as shown in Figure 7.2 (a)-(b) and a PWM loop, as in Figure 7.2 (c), for each independently-controlled output (all outputs except the output that receives energy last). This control approach is easy to implement and well understood since it has been vastly used for single-output converters. Unfortunately, PWM has an inherent delay when responding to sudden load dumps as it goes through multiple cycles to start responding to

load dumps and correcting the outputs. In addition, because the current loop is an inside loop, limiting its bandwidth also limit the bandwidth of other loops that relay on it.

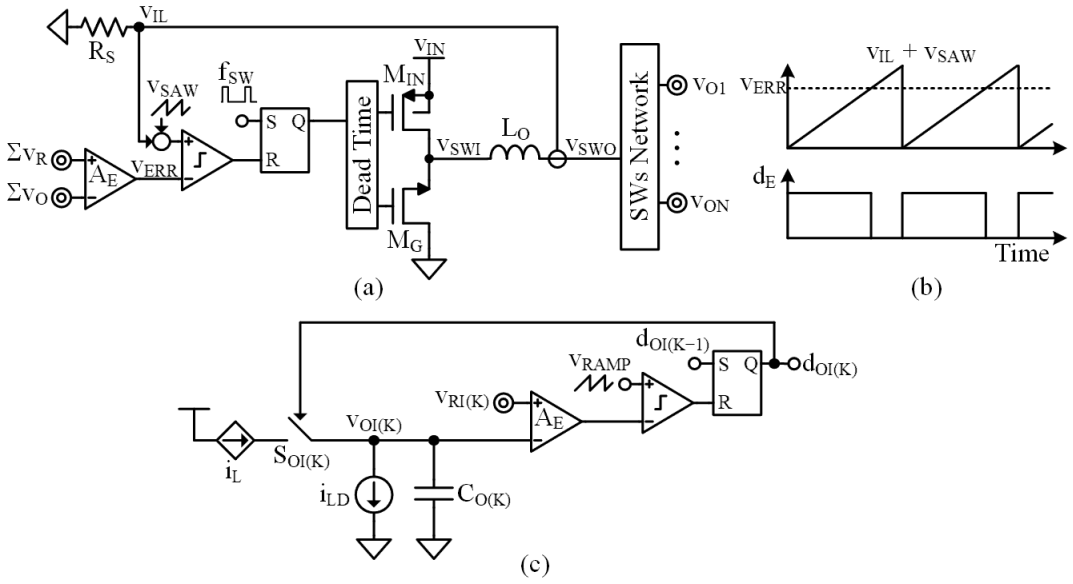


Figure 7.2. (a) Current-mode PWM control to regulate energy in inductor and (b) its operation waveform; and (c) PWM control to regulate voltage on the independent loops.

As detailed in Chapter 2, an alternative method of delivering energy to the outputs is trough dedicating a full energizing/de-energizing cycle for each output. It provides immunity among the outputs but refreshes them less frequently and hence is less accurate. Also, equally important, it cannot efficiently generate buck and boost outputs because a full buck-boost power stage would be required when outputs are a mix of buck and boosted voltages. Using the shared-energy packet operation (as in Figure 7.1), with minimum or no alteration to the operation, a SIMO can generate both buck and boosted voltages. However, for large discrepancies between the delivered buck power and boost power the inductor can be over-energized (or under-energized) each cycle resulting in an unstable operation. Careful consideration and management of these load conditions can reduce unnecessary losses and maintain a high efficiency across load combinations.

7.3 Research Objective

The objective of this research is to explore, develop, analyze, prototype, test, and evaluate how one switched inductor can derive power from a small battery to supply, regulate, and respond to several independent buck and boost outputs reliably and accurately. One fundamental challenge with this work is integration, because miniaturized dc-dc converters cannot afford to accommodate more than one off-chip power inductor. Managing and stabilizing the feedback loops that supply several outputs at different voltages under diverse and dynamic loading conditions with one CMOS chip and one inductor is also challenging. Plus, since a single inductor cannot supply all outputs at once, steady-state ripples and load steps produce cross-regulation effects that are difficult to manage and suppress. Small batteries exacerbate these issues because, with limited energy, the power-supply system cannot consume much power. So with several microwatt to milliwatt loads to manage and supply, the state of the art in this area trades accuracy and response time for footprint and power consumption to such an extent that using one inductor to supply several outputs is often impractical. The underlying aim of this research is this, to diminish these tradeoffs to practical levels.

7.4 Research Contributions

The main contributions of this research are a fully hysteretic control for SIMO converters and its analysis, and an efficiency generation of buck and boost voltages. The stability analysis covers hysteretic control for single-output converter and then expand it to SIMO converters. Then it uses this in the design and evaluation of a fully-hysteretic control and in the generation of boost outputs from a buck power stage. This research also proposes a

balanced PWM−hysteretic control approach that address the limitations of a fully hysteretic approach. In addition, the research also contributes in specifics of the design during the development process.

7.4.1 Hysteretic Current-Mode Analysis

The hysteretic control achieves fast response against load dumps because when error surpasses hysteretic window, the natural oscillation at steady-state stops and the inductor current slews to a new current as in Figure 7.3. This is unlike PWM control that engages in a new cycle during the response interrupting it and therefore delaying the response. Forcing the inductor current to slew and maintain that state until it provides the new appropriate amount of current, is the fastest the current loop can respond and the highest achievable bandwidth. This in turn, allows for the other loops in the system to have a higher bandwidth while conserving stability and hence faster response.

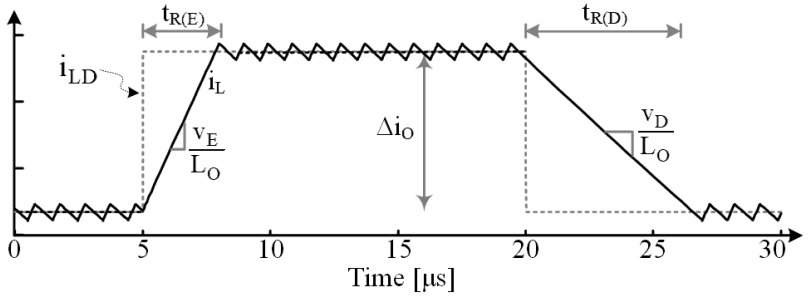


Figure 7.3. Slew response of inductor current with hysteretic control.

Since bandwidth relates to delay, the delay it takes for the current to slew to the new target sets the bandwidth of the current loop. This means that bandwidth has a non-linear dependence to the amount the inductor current must travel between the old and new target. Finding the equivalent RC time constant that gives a similar delay approximates the bandwidth of the hysteretic current loop.

Resulting publications:

- C. J. Solis, and G. A. Rincón-Mora, "Stability Analysis & Design of Hysteretic Current-Mode Switched-Inductor Buck DC-DC Converters," *International Conference on Electronics, Circuits, and Systems*, pp. 811–814, Dec. 2013.
- C. J. Solis, and G. A. Rincon-Mora, "Stability and Design Limits of Hysteretic Current-Mode Switched-Inductor Converters," *IEEJ Transactions on Electrical, and Electronic Engineering,* [Submitted for Review: January 2018].

7.4.2 Analysis and Design of Hysteretic Current-Mode Buck SIMOs

One of the research main contribution is a novel fully-hysteretic control that achieves a high bandwidth with a compact implementation for a SIMO. The simplicity of the control reduces silicon area per output which allows to reduce cost by higher throughput in manufacturing or the possibility of using a low-cost technology. The control, shown in Figure 7.4, is realized by a hysteretic current-loop and an additional hysteretic control across only one of the outputs, hence the independent output.

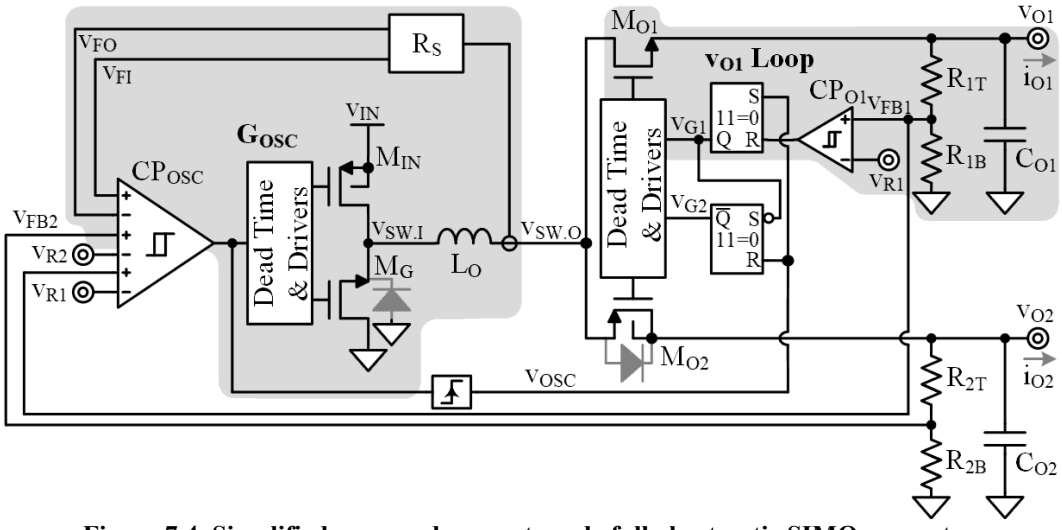


Figure 7.4. Simplified proposed current-mode fully hysteretic SIMO converter.

The current-mode hysteretic control regulates the inductor current ripple as its self oscillates as in a relaxation oscillator. This current loop converts inductor L_O into a current source up to the regulation bandwidth. The hysteretic loop for the independently-controlled outputs v_{O1} equivalently regulate its peak voltage, and due to its highest priority, it will receive energy first until it reaches such target. After v_{O1} receives enough energy, v_{O2} receives energy for the remaining of the period and if v_{O2} does not reaches its target, hysteretic current loop will readjust the current in the inductor proportionally to the summation of error voltages.

The hysteretic control stability analysis was extended to SIMO converter by modeling the additional loop around independently controlled output and how to incorporate them in the total loop. Since the independently-controlled output, e.g. v_{O1} in Figure 7.4, has its own local loop, the inductor and its hysteretic current loop does not influence the independent output loop, unless independent output's error is mixed in the current loop. This would create a small gain feedforward path through the summation at hysteretic comparator CP_{OSC}. Similarly, independently-controlled outputs do not influence the master output stability, e.g. v_{O2} in Figure 7.4, if their bandwidth is lower than the one of the master loop. As a result, master loop is only influenced by the hysteretic current loop even though it is a multiple-output converter. This simplifies the analysis and design of the control scheme for SIMO converters.

The hysteretic response across the independent output naturally skips the outputs if it is disparately lower than the others. This simplifies the skipping capabilities necessary to avoid overcharging outputs during such load differences among outputs load levels. As

a benefit, unnecessary losses are avoided and the converter can dedicate more time regulating the heavily loaded outputs. Also, because the hysteretic current loop naturally oscillates, the switching frequency lowers proportionally with total load current during discontinuous conduction mode which maintains a higher efficiency across a wider range of load levels and combinations. This converter achieved an efficiency of up to 88% while being able to respond within 3.8 μs and regulating the outputs within 7%.

Resulting publications:

- C. J. Solis, and G. A. Rincón-Mora, "Nested hysteretic current-mode single-inductor multiple-output (SIMO) boosting buck converter," *IEEE International New Circuits and Systems*, pp. 1–4, Jun. 2013.
- C. J. Solis, and G. A. Rincon-Mora, "0.6-μm CMOS-Switched-Inductor Dual-Supply Hysteretic Current-Mode Buck Converter," *IEEE Transactions on Power Electronics,* vol. 32, no. 3, pp. 2387–2394, Mar. 2017.
- C. J. Solis, and G. A. Rincón-Mora, "Stability and Design of Hysteretic Current-Mode Single-Inductor Multiple-Output Power Supplies," *IEEE International Midwest Symposium on Circuits and Systems*, pp. 1368–1371, Aug. 2017.

7.4.3 Analysis and Design of Buck-Boost SIMOs

An energized inductor in a buck power stage can be de-energized by any voltage as long it reverses the its voltage polarity. Hence, a boosted output might de-energized the inductor after being energized through the buck outputs. Ordering the outputs such that the boosted one receives energy last, allow to keep a high efficiency as long the boosted output only de-energizes the inductor since the inductor energizes the most through buck outputs. In

the case the inductor does not sufficiently energizes through the buck outputs, an additional power switch, M_A in Figure 7.5, assist the energizing process of the inductor only for the extra energizing time required. This ultimately avoid increasing silicon real estate for the extra switch (as current through it is a fraction of the total inductor current compared to an equivalent buck-boost power stage) and minimize losses by simultaneously delivering energy as inductor energizes as much as possible.

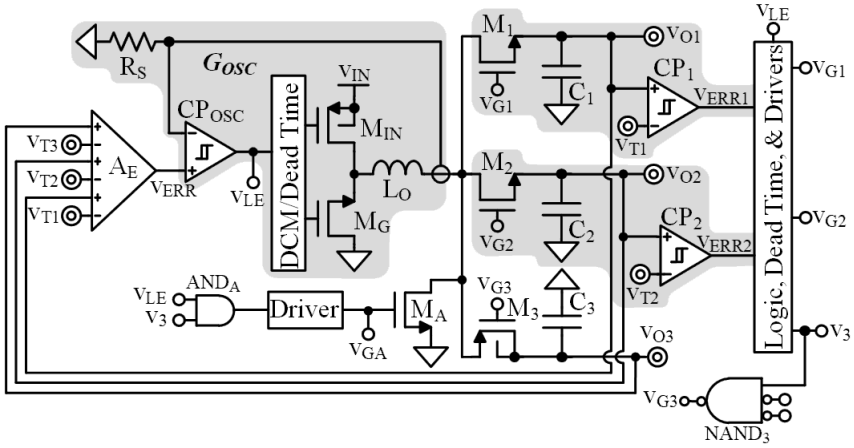


Figure 7.5. Proposed current-mode fully hysteretic buck-boost SIMO converter.

Resulting publications:

- C. J. Solis, and G. A. Rincon-Mora, "87%-Efficient 330-mW 0.6-µm Single-Inductor Triple-Output Buck-Boost Power Supply," *IEEE Transactions on Power Electronics,* [Accepted: September 2017].

7.4.4 Hysteretic Current-Mode SIMO with Independent PWM Loops

Albeit its fast response and dynamic accuracy, hysteretic control is noise sensitive and as a result, has a large voltage ripple to avoid false tripping in the comparators. To alleviate this output ripple in applications sensitive to it, this research proposed a hybrid between

hysteretic and PWM loops that balances dynamic and steady-state performance for the next generation SIMO. As Figure 7.6 shows, a hysteretic current-loop regulates the current in the inductor allowing it to have the highest bandwidth possible. Instead of a hysteretic comparator, a high-bandwidth PWM loop regulates the voltage on the independent loops. With this hybrid, the control can respond quickly to load dumps thanks to the hysteretic current loop and have less steady-state ripple since PWM loops are less noise sensitive. However, future research should investigate the further features and shortcomings.

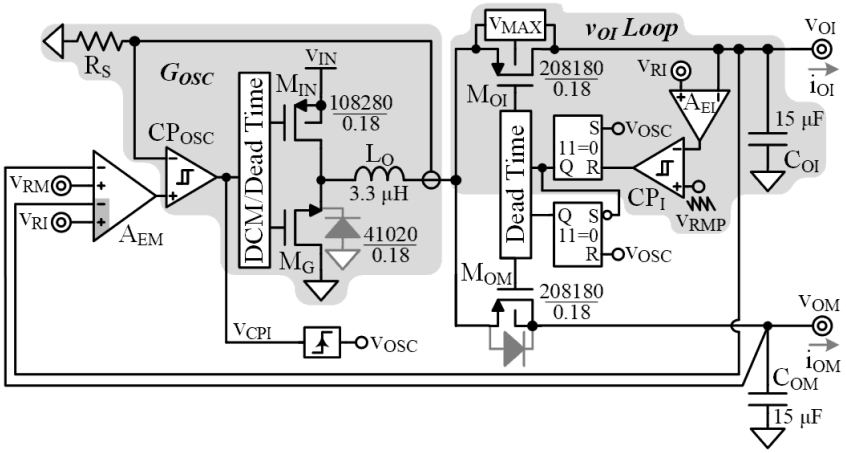


Figure 7.6. Hysteretic current-mode SIMO with independent PWM loops.

7.4.5 Other Contributions

In addition to the main contributions already discussed above, the research had other contributions related to the development and design of the prototypes. A scalable logic was developed to ease the design process for applications which requires a SIMO with a larger number of outputs. A dead-time logic was designed to protect all outputs by preventing any two outputs to simultaneously engaged even if the converter had a bug and tried to engage more than one output at a time. Blocks for all prototypes had a common trade-off between power consumption and bandwidth which required consideration. Comparators

and amplifiers were design to have just enough low delay to become negligible to minimize power dissipation which becomes important at light-load conditions. Also, power switches selection was a challenge when outputs were mid-levels compared to input supply or high output voltages, the design had to be adapted to the best option given by the technology either by levering a boosted output already present or by optimizing the bias point of the bulk terminal for PMOS switches.

7.5 Design Considerations

7.5.1 Process Technology

The process technology used in the design of the SIMO converter has several effects on the performance for the proposed work and in general. For instance, technology with smaller dimensions has faster speed and can therefore achieve lower delays with a smaller power budget [115]. Hence quiescent losses can be lower which results in higher efficiency primordially at light-load conditions. Another example where finer technologies can excel is in applications that requires higher switching frequencies in the power supply system.

In the other hand, finer technologies have a higher manufacturing cost and lower breakdown voltages. In such cases, as when regulating energy from a lithium-ion battery, larger technologies nodes are more appropriate. So the technology choice is driven by the best available and affordable technology capable to sustain the required voltages from the application. Other factors that can influence technology choice such as if integration in the same die of the entire system is required for a compacter solution.

7.5.2 Accuracy versus Power

Component, such as inductor and capacitors, values have an impact across several performance metrics of a SIMO converter. A high inductance value reduces current ripple which helps to increase accuracy and lower conduction losses (through lower rms current). However, as shown in the proposed converters, a higher inductance also reduces the bandwidth of the hysteretic control which results in longer response time and more susceptible to instability.

Similarly, higher capacitance values increase accuracy by decreasing ripple, or, if accuracy is fixed, allows to deliver higher current levels. But also, a higher capacitance limits the bandwidth of the system and hence increases response time. During the design process, the inductance and capacitance should be chosen to meet the more stringent requirement and interactively find the values to meet all specifications while balancing the inherent tradeoffs.

7.5.3 Startup

A controlled startup sequence avoids high inrush current as the initial output voltage errors are large. Forcing all references to zero at startup, the same voltage at the outputs for a discharged power converter, avoids the converter to engage aggressively. Then, the references voltages can rise slowly and then settle to their steady-state value. A topological possibility is to use a ramp signal at a third input terminal of a PMOS based differential amplifier parallel to the reference voltage input PMOS [79]. In addition, to avoid large current levels during start-up, each output can be charged individually so that the inductor only charges one output capacitor at a time. The sequence then should start by charging the

output that freewheels the inductor current and then the other outputs as determined by the application.

For the proposed buck-boost SIMO converter in Chapter 5, several extra considerations for the startup sequence are important. One is that the driver's supply for the boosted output PMOS switch must use the regulated boost voltage itself to be able to turn fully off. And since a higher supply for one driver already is required, the remaining NMOS output switches also use the same boosted supply for their drivers to use less area. When the converter is discharged at startup and all output voltages are (or close to) zero, the supply for the output drivers is not high enough to reliably engage/disengage the switches. Fortunately, because the PMOS switch's body diode is the freewheeling path for the inductor current, it allows the boost output to charge during startup. As it charges beyond several threshold voltages of the transistors, the supply becomes strong enough to allow the drivers to control the gate of the output switches. Therefore, boosted output voltage charges first and then each buck output voltage for a controlled startup sequence.

7.5.4 Boost Ratio

The boost ratio for a buck-boost SIMO is limited by the breakdown voltage of the technology. Even if an external high-voltage diode replaces the switch for the boosted output that freewheels the inductor current, the output switching node is shared among other outputs and therefore their switches must be able to withstand the highest voltage. As a result, the maximum measured boost ratio was 1.67 (from 2.7V to 4.5V) for the proposed circuit in Chapter 5. If a higher boost ratio is desired, a high-breakdown technology is necessary to sustain such voltages.

7.6 Publications

The current work has resulted in two published journal publications, three conference publications and an additional journal paper under consideration. Among the conference publications, conference from ICECS presented the new analysis approach for stability in hysteretic controllers using simulations across various operating conditions as shown in Chapter 3. Also, the paper presented in MWSCAS conference extended the stability analysis to SIMO converters also discussed in Chapter 3. Finally, conference from NEWCAS presented the fully hysteric control for SIMO detailed in Chapter 4 with simulations and a general design approach.

Both published journals on TPE presents the converter and controller discussed in Chapter 4 and 5 with measurement results. Journal paper published on Mar 2017 discusses the performance of hysteretic control on SIMO. The TPE journal paper accepted in September 2017, measures the performance and limits of the buck-boost capability in a triple-output SIMO converter. The third journal publication under review in TEEE journal presents measurements on the stability under various conditions as discussed in Chapter 3 for single-output converters.

7.6.1 Peer-Reviewed Journals

- C. J. Solis, and G. A. Rincon-Mora, "0.6-μm CMOS-Switched-Inductor Dual-Supply Hysteretic Current-Mode Buck Converter," *IEEE Transactions on Power Electronics,* vol. 32, no. 3, pp. 2387–2394, Mar. 2017.

- C. J. Solis, and G. A. Rincon-Mora, “87%-Efficient 330-mW 0.6-µm Single-Inductor Triple-Output Buck-Boost Power Supply,” *IEEE Transactions on Power Electronics,* [Accepted: September 2017].
- C. J. Solis, and G. A. Rincon-Mora, “Stability and Design Limits of Hysteretic Current-Mode Switched-Inductor Converters,” *IEEJ Transactions on Electrical, and Electronic Engineering,* [Submitted for Review: January 2018].

7.6.2 Peer-Reviewed Conferences

- C. J. Solis, and G. A. Rincón-Mora, “Nested hysteretic current-mode single-inductor multiple-output (SIMO) boosting buck converter,” *IEEE International New Circuits and Systems*, pp. 1–4, Jun. 2013.
- C. J. Solis, and G. A. Rincón-Mora, “Stability Analysis & Design of Hysteretic Current-Mode Switched-Inductor Buck DC-DC Converters,” *International Conference on Electronics, Circuits, and Systems*, pp. 811–814, Dec. 2013.
- C. J. Solis, and G. A. Rincón-Mora, “Stability and Design of Hysteretic Current-Mode Single-Inductor Multiple-Output Power Supplies,” *IEEE International Midwest Symposium on Circuits and Systems*, pp. 1368–1371, Aug. 2017.

7.7 Technological Challenges

Technical limitations with the proposed SIMO converter exists in despite of its benefits over the state of the art. A limitation of the proposed SIMO is the lack of integration of various energy sources as energy harvesting circuits useful in microsystems application. Since replacing batteries in microsystems is costly and cumbersome, energy harvesting is

vital to achieve a completely independent microsystem for a longer period. Therefore, the power management system should efficiently incorporate other energy sources to supply energy to the outputs while storing the excess in the battery.

The proposed SIMO uses an auxiliary switch only when required to supply enough boost power, but the sequence can be further optimized to minimize switching transitions and therefore losses. One way is to push the energizing phase as the boosted output receives energy. This would increase the deliverable boosted power without affecting operation. In addition to this benefit, the output sequence might also be optimized to reduce switching losses by using zero-voltage switching in certain applications.

Finally, hysteretic controller has fast response time as it regulates instantaneous signals but, due to the same reason, it will be sensitive to switching noise which results in a voltage ripple including a large enough hysteretic window. Mixing PWM and hysteretic balances the trade-offs but, unfortunately, slightly increases response time. Being able to use a fully hysteretic control while reducing noise sensitivity might improve these tradeoffs. These challenges pave the path for future research and improvements for SIMO converters in microsystems applications.

7.8 Future SIMO Research

7.8.1 Single-Inductor Multiple-Input Multiple-Output Converter

Since microsystems has a tiny battery, harvesting energy from the environment prolongs the time without a costly replacement of the battery [21–22]. To this end, a SIMO converter should also incorporate a mix of input sources to achieve a multiple-input multiple-output

converter. Figure 7.7 shows the concept of a switched-inductor converter that receives energy from two harvesting sources v_{HR1} and v_{HR2} to regulate two output voltages v_{O1} and v_{O2}. Also, it includes a battery v_{BAT} which act as a load when harvesting energy is higher than the power the load requires and as an energy source when harvested energy is below the energy the loads needs.

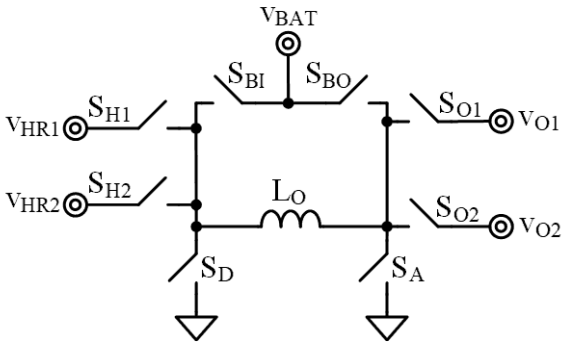


Figure 7.7. Single-inductor multiple-input multiple-output converter for microsystems applications.

Research for multiple-input multiple-output is at its infancy [74], [110−112]; and most approaches aim to prove the concept with discrete implementation. Some works already include the functionality of using the battery as an input and an output [22], [113]. Albeit efficient, these works can only deliver a few miliwatts to the load. Hence, the challenge is to explore an integrated solution that simultaneously maximizes bandwidth, deliverable power, and efficiency.

7.8.2 Switch Sequence Optimization

Wireless microsystems duty-cycle blocks when not needed; so, when transmitting data, sensing and data processing functions might be idling or less frequent. Because the supply for the power amplifier might need boosting, generating an efficient boost is important. The proposed operation in Chapter 5 allowed to generate an efficient boost output without

adding additional switches. However, the deliverable power at the boundary is limited and proportional to the buck power delivered. Figure 7.8 shows a possible scheme that extend energizing time t_E even as the boosted output receives energy. Technically, the inductor is not energizing, but the benefit is that the input supply and the inductor simultaneously deliver energy to boosted output instead of just the inductor as in Chapter 5.

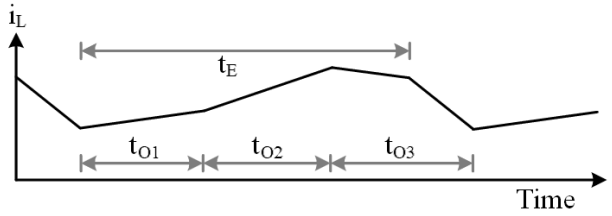


Figure 7.8. Converter operation by extending energizing time to boosted output.

The maximum power deliverable to boosted output power P_{O3} without changing operation occurs when energizing time extends for the whole switching cycle or t_E equals $t_{O1} + t_{O2} + t_{O3}$. During this time, although the inductor is truly de-energizing, input supply v_{IN} is providing more power as it sees the inductor current i_L (or $i_{O1} + i_{O2} + i_{O3}$) all the time instead of the buck loads (outputs v_{O1} and v_{O2}) as equation (5.9):

$$P_{O3}' \approx v_{IN}\left(i_{O1} + i_{O2} + i_{O3}\right) - \left(P_{O1} + P_{O2}\right). \tag{7.1}$$

Substitution of i_{O3} as P_{O3}/v_{O3} and grouping of terms gives the maximum deliverable boost power:

$$P_{O3}' \approx \frac{v_{IN}\left(i_{O1} + i_{O2}\right) - \left(P_{O1} + P_{O2}\right)}{1 - \frac{v_{IN}}{v_{O3}}}. \tag{7.2}$$

Compared to equation (5.9) the boost power limit is increased by the fraction $v_{O3}/(v_{O3} - v_{IN})$. When supply is 2.7 V for the proposed buck-boost converter it can deliver three times more boosted power as Figure 7.9 shows, and up to ten times when supply is 3.6 V.

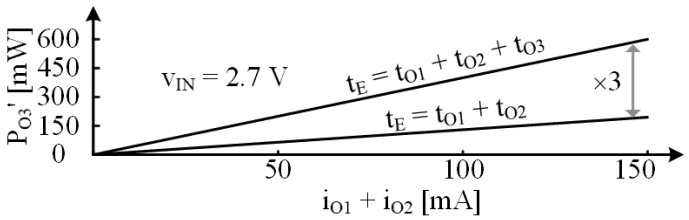


Figure 7.9. Maximum deliverable boosted power when energizing only through buck outputs and extended comparison.

Unfortunately, the challenge is implementing this technique with hysteretic control since, during the energizing period t_E, the controller is expecting the inductor current to hit the upper limit of a hysteretic window. This happens because the hysteretic control regulates the instantaneous value of the inductor current and not reaching the upper hysteretic limit would stall the converter in an indefinite energizing state. A controlled timer or a hybrid control with some fixed period can prevent the converter to get stuck and would increase deliverable boosted power without assistance of an additional power switch for a wider set of operating conditions.

7.8.3 Output Switches Zero Volt Switching

Another opportunity to increase efficiency is trying to implement zero-voltage switching (ZVS) across the output switches. This is relevant as the number of outputs increase since more switching transitions occurs among output switches. Figure 7.10 shows a power stage suitable for zero volt switching on the outputs switches which are PMOS transistors and outputs receives energy starting from the lowest voltage to the highest. The goal is to avoid

each output discharge the switching node $v_{SW.O}$ from a high voltage. This work best when outputs receives energy in an ascending order with respect to their voltage levels, so than when a lower voltage is disconnected, the next one is ready to clamp the switching node voltage to its output level.

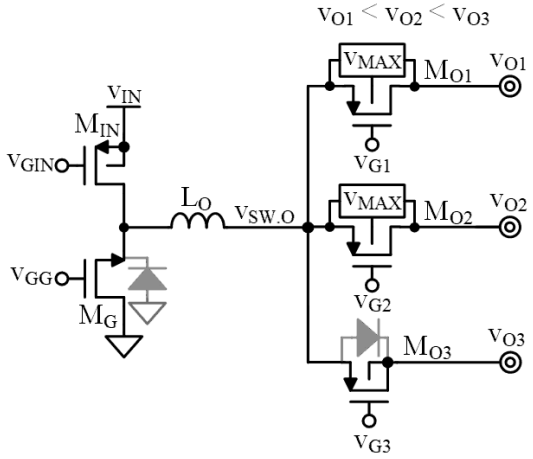


Figure 7.10. Power stage for output switches zero-voltage switching technique.

After output v_{O1} receives energy, switch M_{O2}'s driver can set its gate v_{G2} to v_{O2} before control turns-off switch M_{O1}. As inductor current freewheels and charges switching node $v_{SW.O}$, M_{O2} will clamp $v_{SW.O}$ a source-gate voltage above v_{O2} as in Figure 7.11. In other words, forcing v_{G2} to v_{O2} will make v_{O2} the free-wheeling path for the inductor current instead of the highest voltage (v_{O3} in this example) as previously proposed. After some dead-time t_{DT}, M_{O2} fully engages as v_{G2} is driven to ground. Similarly, because v_{O3} is the supply of the drivers, turning off M_{O2} makes M_{O3} naturally clamp $v_{SW.O}$ a v_{SG} or diode voltage v_{DIO} above v_{O3}, whichever is lower. When v_{O1} turns on for the next cycle, it does without zero volts across the switch because it must discharge $v_{SW.O}$ from the highest potential.

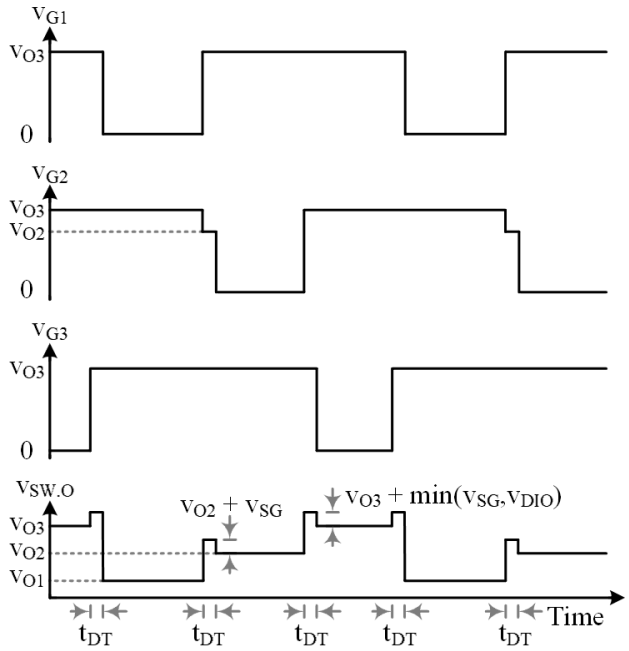


Figure 7.11. Operating waveform for output switches with zero-volt switching.

In summary, this ZVS technique can reduce switching losses for all switches except one. It also reduces switching noise, as switches with ZVS does not have to discharge v_{SWO} as much and therefore reducing current spikes at the transition from one output to another. The challenges for this technique, however, is when the application does not allow the output sequence to be with ascending output voltage. Also, the potential for loss reduction depends on the spread of the output voltages where benefits increases proportional to the voltage spread. Hence, the added complexity might be justified for microsystems with a load that requires a relatively high voltage supply such as a power amplifier and other load requires a much lower supply.

7.8.4 Noise Sensitivity

As previously mentioned, the hysteretic control is sensitive to noise as it regulates instantaneous values, especially for the independent loops where noisy voltages are

regulated. To prevent false triggering or noisy switching, the hysteretic windows include a large enough hysteresis that unfortunately set a minimum output voltage ripple. Even though filtering might help the noise at the input of comparators [114], they slow the response and complicates loop compensation, and in some cases, requires knowledge of the filtered frequencies. Using the fact that the logic control in the proposed SIMOs has an all-or-nothing control in a cycle (no output is re-engaged in the same cycle), increasing the hysteresis only at the transitions might reduce noise sensitivity while imposing a lower steady-state minimum ripple at the outputs.

Figure 7.12 (a) shows a possible comparator implementation and its operating waveform (b). When the signal being regulated, i.e. feedback voltage v_{FB}, crosses the reference v_R comparator trips and the comparator's output v_O is ac coupled to v_{FB} though capacitor C_{HYS}. During the transition, this effectively creates a hysteretic windows $\Delta v_{H(AC)}$ depending on the voltage divider from the sypply by capacitors C_{HYS} and equivalent C_{FB} at v_{FB}:

$$\Delta v_{H(AC)} = V_{DD}\left(\frac{C_{HYS}}{C_{FB}+C_{HYS}}\right). \tag{7.3}$$

After the comparator trips the hysteretic window $\Delta v_{H(AC)}$ will relax to the inherent hysteresis in the comparator as total capacitance at v_{FB} discharges through equivalent resistance R_{FB}. Hence, $\Delta v_{H(AC)}$ will last for approximately five time-constants from node v_{FB}:

$$t_{H(AC)} \approx 5R_{FB}\left(C_{FB}+C_{HYS}\right). \tag{7.4}$$

This relaxation time $t_{H(AC)}$ can be set-up high enough until the point that does not affects the operation of the converter.

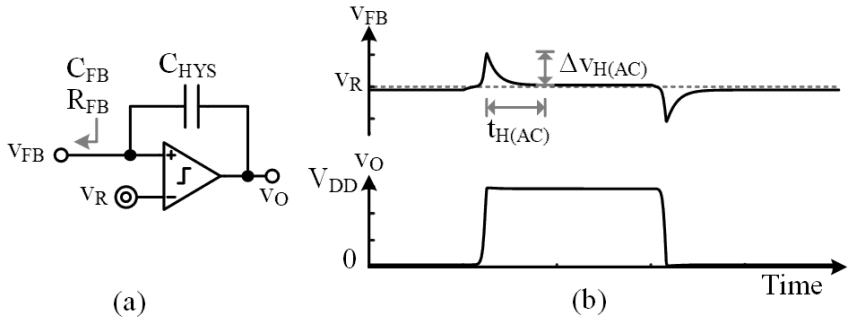


Figure 7.12. AC hysteresis (a) schematic and (b) operating waveforms for hysteretic control on independent outputs.

7.9 Conclusions

The contributions presented here allows SIMO to advance and reduce trade-offs to practical levels and circumvent previous challenges such as response time, size and cost. Such advances help to expand the application space and ease the design of SIMO converters. However, limitations still exist in despite of the contributions presented here. Tackling these limitations will accelerate the use and availability of SIMO converters.

7.9.1 Advances

Contributions presented here decrease response time without increasing silicon real-estate or decreasing efficiency, and regulate supplies suitable for applications with a wide range of output and input voltages. This means that components such as output capacitors can be smaller because the converter reacts faster, and that supplies has improved accuracy during load dumps. Also, a system is not limited to only step down or step up the battery voltage to power its circuits. Without increasing board component count, the proposed converter

can operate to regulate mix of buck and boost voltages from the same energy source. This means that as the energy source depletes, or if higher voltage technology is preferred for certain functions, the power management system can handle a wider combination of conditions.

7.9.2 Limitations

The main limitation that impedes SIMOs to proliferate its presence in multi-functional systems is the cross-regulation among the outputs. Although a SIMO can have minimal cross-regulation under certain operation schemes such as dedicating a full energizing/de-energizing cycle to each output, it comes at the expense of efficiency and limited power delivery. For high efficiency and output power requirements sharing inductor current within the same cycle is appropriate. However, cross-regulation will be present but can be equally balanced or weighted according to the sensitivity of each load. Unfortunately, this limitation is addressed specifically to an application by weighting priority and sensitivity to cross regulation.

Another limitation that should be address is the mixing of more energy sources. This enables a complete solution for portable electronics or wireless microsystems with energy harvesting for portable electronics. It allows to harvest energy while using a storage element such as a battery or capacitor to assist power delivery at peak load and save when in low power state. Power management systems for these applications are proven but with limited deliverable power or a single regulated supply. Increasing the capacity of power delivery, and the number of regulated supplies for these application makes SIMO

converters not only advance in the portable electronics space, but also in bigger power systems such as hybrid vehicles, photovoltaic systems, and lighting.

7.10 SIMOs in the Future

SIMOs offer a compact and low-cost solution by means of using less board components while conserving the benefits of high efficiency of a switching converter. This means that wireless microsystems can be light in weight, compact and cheaper which can improve products in markets such as medical devices, power utilities, surveillance and military to name a few. Specifically, the low-cost advantage can propel a large deployment of microsystems to add intelligence to large systems and/or objects. For instance, homes and buildings can add temperature sensors in all rooms or as a grid to better gauge insulation and precise control of air conditioning. Another example is to add sensor that detect tilt or movement in walls and floors to monitor their integrity to remedy them before an accident or repair cost raises. Also, markets such as consumer electronics, such as phones, can cost less and reduce time to market due to the lower component count in the design and manufacturing process.

For a successful adoption of the SIMO converters, its limitations, such as cross-regulation, must be considered and their impact considered to maintain the same or improved performance in the current products. This is critical in application such as in communication which can result in unwanted crosstalk or interference. As technologies advances and becomes faster, cheaper, and smaller; SIMOs can improve such that its limitations would become negligible or minimized. This will allow market penetration and

adoption starting a new generation of compact and cheaper power management systems in an increasingly complex and function-heavy application space.

7.11 Summary

A microsystem includes several functions with their unique supply voltage level and power profiles. A single-inductor multiple-output (SIMO) converter can compactly and efficiently generate multiple supplies that these functions require. Doing so balances size and efficiency trade-offs as inductors are bulk and difficult to integrate. Literature provides several control schemes but most rely on some variation of PWM. Although accurate, they require multiple cycle before responding to load dump. Since microsystem duty-cycle functions to save energy, a quick responding control improves accuracy for frequent load dumps. Luckily, hysteretic control has a fast-dynamic response but its stability is seldom insightful and has not been analyzed and implemented for SIMO controllers.

The objective of this research is to explore, develop, analyze, prototype, test, and evaluate a SIMO with hysteretic control at the core capable of regulating a mix of buck and boost supplies. The research has produced analysis for a stable design of hysteretic single-output converters and for SIMO converters. Also, it provided with measurements and assessment of SIMO converters that can efficiently generate buck and boost outputs simultaneously. The research resulted in a control with fast response, a compact solution, and an efficient converter compared to the literature. Albeit its benefits, there is still limitations and potential future research such as including additional input supplies from energy-harvesting sources and further optimizing the energy delivery sequence to further reduces losses and increase output power. This will allow SIMO converter to become the

default power management system in portable electronics with a continuous grow of capabilities and features.

REFERENCES

[1] D. Puccinelli, and M. Haenggi, "Wireless Sensor Networks Applications and Challenges of Ubiquitous Sensing," *IEEE Circuits and Systems Magazine,* vol. 5, no. 3, pp. 19–31, 2005.

[2] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, and A. P. Chandrakasan, "A Micro-Power EEG Acquisition SoC With Integrated Feature Extraction Processor for a Chronic Seizure Detection System," *IEEE Journal of Solid-State Circuits,* vol. 45, no. 4, pp. 804–816, Apr. 2010.

[3] E. Sardini, and M. Serpelloni, "Self-Powered Wireless Sensor for Air Temperature and Velocity Measurements With Energy Harvesting Capability," *IEEE Transactions on Instrumentation and Measurement,* vol. 60, no. 5, pp. 1838–1844, May 2011.

[4] R. R. Harrison, R. J. Kier, C. A. Chestek, V. Gilja, P. Nuyujukian, S. Ryu, B. Greger, F. Solzbacher, and K. V. Shenoy, "Wireless Neural Recording with Single Low-Power Integrated Circuit," *IEEE Transactions on Neural Systems and Rehabilitation Engineering,* vol. 17, no. 4, pp. 322–329, Aug. 2009.

[5] Z. Cao, R. Zhu, and R. Y. Que, "A Wireless Portable System with Microsensors for Monitoring Respiratory Diseases," *IEEE Transactions on Biomedical Engineering,* vol. 59, no. 11, pp. 3110–3116, Nov. 2012.

[6] K. Nishihara, W. Iwasaki, M. Nakamura, E. Higurashi, T. Soh, T. Itoh, H. Okada, R. Maeda, and R. Sawada, "Development of a Wireless Sensor for the Measurement of Chicken Blood Flow Using the Laser Doppler Blood Flow Meter Technique," *IEEE Transactions on Biomedical Engineering,* vol. 60, no. 6, pp. 1645–1653, Jun. 2013.

[7] E. G. Kilinc, G. Conus, C. Weber, B. Kawkabani, F. Maloberti, and C. Dehollain, "A System for Wireless Power Transfer of Micro-Systems In-Vivo Implantable in Freely Moving Animals," *IEEE Sensors Journal,* vol. 14, no. 2, pp. 522–531, Feb. 2014.

[8] H. Hafezi, T. L. Robertson, G. D. Moon, K. Y. Au-Yeung, M. J. Zdeblick, and G. M. Savage, "An Ingestible Sensor for Measuring Medication Adherence," *IEEE Transactions on Biomedical Engineering,* vol. 62, no. 1, pp. 99–109, Jan. 2015.

[9] A. Somov, E. F. Karpov, E. Karpova, A. Suchkov, S. Mironov, A. Karelin, A. Baranov, and D. Spirjakin, "Compact Low Power Wireless Gas Sensor Node With Thermo Compensation for Ubiquitous Deployment," *IEEE Transactions on Industrial Informatics,* vol. 11, no. 6, pp. 1660–1670, 2015.

[10] C. Nguyen, and M. Micovic, "The State-of-the-Art of GaAs and InP Power Devices and Amplifiers," *IEEE Transactions on Electron Devices,* vol. 48, no. 3, pp. 472−478, Mar. 2001.

[11] Y. Li, J. Lopez, P.-H. Wu, W. Hu, R. Wu, and D. Y. C. Lie, "A SiGe Envelope-Tracking Power Amplifier With an Integrated CMOS Envelope Modulator for Mobile WiMAX/3GPP LTE Transmitters," *IEEE Transactions on Microwave Theory and Techniques,* vol. 59, no. 10, pp. 2525–2536, Oct. 2011.

[12] B. Razavi, *RF Microelectronics - Second Edition*, Pearson Education, New Jersey, 2012.

[13] T. Niiyama, P. Zhe, K. Ishida, M. Murakata, M. Takamiya, and T. Sakurai, "Dependence of Minimum Operating Voltage on Block Size of 90-nm CMOS Ring Oscillators and Its Implications in Low Power DFM," *International Symposium on Quality Electronic Design*, pp. 133–136, Mar. 2008.

[14] S. Dighe, S. R. Vangal, P. Aseron, S. Kumar, T. Jacob, K. A. Bowman, J. Howard, J. Tschanz, V. Erraguntla, N. Borkar, V. K. De, and S. Borkar, "Within-Die Variation-Aware Dynamic-Voltage-Frequency-Scaling With Optimal Core Allocation and Thread Hopping for the 80-Core TeraFLOPS Processor," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 1, pp. 184–193, Jan. 2011.

[15] B. Bae, Y. Shim, K. Koo, J. Cho, J. S. Pak, and J. Kim, "Modeling and Measurement of Power Supply Noise Effects on an Analog-to-Digital Converter Based on a Chip-PCB Hierarchical Power Distribution Network Analysis," *IEEE Transactions on Electromagnetic Compatibility,* vol. 55, no. 6, pp. 1260–1270, 2013.

[16] M. K. Stojčev, M. R. Kosanović, and L. R. Golubović, "Power Management and Energy Harvesting Techniques for Wireless Sensor Nodes," *International Conference on Telecommunication in Modern Satellite, Cable, and Broadcasting Services*, pp. 65–72, Oct. 2009.

[17] H. Shaoxiong, and Q. Gang, “Voltage Setup Problem for Embedded Systems With Multiple Voltages,” *IEEE Transactions on Very Large Scale Integration Systems,* vol. 13, no. 7, pp. 869–872, Jul. 2005.

[18] T. B. Reddy, *Linden's Handbook of Batteries - Fourth Edition*, McGraw-Hill, 2011.

[19] S. Sudevalayam, and P. Kulkarni, “Energy Harvesting Sensor Nodes: Survey and Implications,” *IEEE Communications Surveys & Tutorials,* vol. 13, no. 3, pp. 443–461, 2011.

[20] R. J. M. Vullers, R. v. Schaijk, H. J. Visser, J. Penders, and C. V. Hoof, “Energy Harvesting for Autonomus Wireless Sensor Networks,” *IEEE Solid-State Circuits Magazine,* vol. 2, no. 2, pp. 29–38, Spring 2010.

[21] D. Kwon, and G. A. Rincon-Mora, “A single-inductor 0.35μm CMOS energy-investing piezoelectric harvester,” *IEEE Journal of Solid-State Circuits,* vol. 49, no. 10, pp. 2277–2291, Oct. 2014.

[22] R. D. Prabha, and G. A. Rincon-Mora, “0.18-μm Light-Harvesting Battery-Assisted Charger–Supply CMOS System,” *IEEE Transactions on Power Electronics,* vol. 31, no. 4, pp. 2950–2958, Apr 2016.

[23] E. Sanchez-Sinencio, and A. G. Andreou, *Low-Voltage/Low-power Integrated Circuits and Systems*, IEEE Press, New York, 1998.

[24] Y. H. Lu, and G. D. Micheli, “Comparing System Level Power Management Policies,” *IEEE Design & Test of Computers,* vol. 18, no. 2, pp. 10–19, 2001.

[25] C. Alippi, G. Anastasi, M. D. Francesco, and M. Roveri, “Energy Management in Wireless Sensor Networks with Energy-Hungry Sensors,” *IEEE Instrumentation & Measurement Magazine,* vol. 12, no. 2, pp. 16–23, Apr. 2009.

[26] A. Sinha, and A. Chandrakasan, “Dynamic Power Management in Wirelesss Sensor Networks,” *IEEE Design & Test of Computers,* vol. 18, no. 2, pp. 62−74, Mar./Apr. 2001.

[27] E. Beigne, F. Clermidy, H. Lhermet, S. Miermont, Y. Thonnart, X.-T. Tran, A. Valentian, D. Varreau, P. Vivet, X. Popon, and H. Lebreton, “An Asynchronous

Power Aware and Adaptive NoC Based Circuit," *IEEE Journal of Solid-State Circuits,* vol. 44, no. 4, pp. 1167−1177, Apr. 2009.

[28] T. D. Burd, T. A. Pering, A. J. Stratakos, and R. W. Brodersen, "A Dynamic Voltage Scaled Microprocessor System," *IEEE Journal of Solid-State Circuits,* vol. 35, no. 11, pp. 1571−1580, Nov. 2000.

[29] K. J. Nowka, G. D. Carpenter, E. W. MacDonald, H. C. Ngo, B. C. Brock, K. I. Ishii, T. Y. Nguyen, and J. L. Burns, "A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling," *IEEE Journal of Solid-State Circuits,* vol. 37, no. 11, pp. 1441–1447, Nov. 2002.

[30] N. Drego, A. Chandrakasan, D. Boning, and D. Shah, "Reduction of Variation-Induced Energy Overhead in Multi-Core Processors," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 30, no. 6, pp. 891−904, 2011.

[31] I. Vaisband, and E. G. Friedman, "Heterogeneous Methodology for Energy Efficient Distribution of On-Chip Power Supplies," *IEEE Transactions on Power Electronics,* vol. 28, no. 9, pp. 4267–4280, Sep. 2013.

[32] J. Park, D. Shin, N. Chang, and M. Pedram, "Accurate Modeling and Calculation of Delay and Energy Overheads of Dynamic Voltage Scaling in Modern High-Performance Microprocessors," *ACM/IEEE International Symposium on Low-Power Electronics and Design*, pp. 419–424, Aug. 2010.

[33] P. Sangyoung, P. Jaehyun, S. Donghwa, W. Yanzhi, X. Qing, M. Pedram, and C. Naehyuck, "Accurate Modeling of the Delay and Energy Overhead of Dynamic Voltage and Frequency Scaling in Modern Microprocessors," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 32, no. 5, pp. 695–708, May 2013.

[34] G. A. Rincon-Mora, *Analog IC Design with Low-Dropout Regulators - Second Edition*, McGraw-Hill, New York, 2014.

[35] R. J. Milliken, J. Silva-Martinez, and E. Sanchez-Sinencio, "Full On-Chip CMOS Low-Dropout Voltage Regulator," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 54, no. 9, pp. 1879–1890, Sep. 2007.

[36] Y. Lu, J. Jiang, W.-H. Ki, C. P. Yue, S.-W. Sin, S.-P. U, and R. P. Martins, "A 123-Phase DC-DC Converter-Ring with Fast-DVS for Microprocessors," *IEEE International Solid-State Circuit Conference*, pp., Feb. 2015.

[37] B. Zimmer, Y. Lee, A. Puggelli, J. Kwak, R. Jevtić, B. Keller, S. Bailey, M. Blagojević, P.-F. Chiu, H.-P. Le, P.-H. Chen, N. Sutardja, R. Avizienis, A. Waterman, B. Richards, P. Flatresse, E. Alon, K. Asanović, and B. Nikolić, "A RISC-V Vector Processor With Simultaneous-Switching Switched-Capacitor DC–DC Converters in 28 nm FDSOI," *IEEE Journal of Solid-State Circuits,* vol. 51, no. 4, pp. 930–942, Apr. 2016.

[38] I. Chowdhury, and D. Ma, "Design of Reconfigurable and Robust Integrated SC Power Converter for Self-Powered Energy-Efficient Devices," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 10, pp. 4018–4028, Oct. 2009.

[39] H.-P. Le, S. R. Sanders, and E. Alon, "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 9, pp. 2120−2131, Sep. 2011.

[40] R. D. Prabha, G. A. Rincon-Mora, and S. Kim, "Harvesting Circuits for Miniaturized Photovoltaic Cells," *IEEE International Symposium on Circuits and Systems*, pp. 309–312, May 2011.

[41] T. M. Andersen, F. Krismer, J. W. Kolar, T. Toifl, C. Menolfi, L. Kull, T. Morf, M. Kossel, M. Brändli, P. Buchmann, and P. A. Francese, "A Deep Trench Capacitor Based 2:1 and 3:2 Reconfigurable on-Chip Switched Capacitor DC-DC Converter in 32 nm SOI CMOS," *IEEE Applied Power Electronics Conference and Expo*, pp. 1448–1455, Mar. 2014.

[42] S. A. Campbell, *Fabrication Engineering: at the Micro- and Nanoscale*, Oxford, New York, 2008.

[43] C. O. Mathúna, W. Ningning, S. Kulkarni, and S. Roy, "Review of Integrated Magnetics for Power Supply on Chip (PwrSoC)," *IEEE Transactions on Power Electronics,* vol. 27, no. 11, pp. 4799–4816, Nov. 2012.

[44] P. Hazucha, G. Schrom, J. Hahn, B. A. Bloechel, P. Hack, G. E. Dermer, S. Narendra, D. Gardner, T. Karnik, V. De, and S. Borkar, "A 233-MHz 80%–87%

efficient four-phase DC-DC converter utilizing air-core inductors on package," *IEEE Journal of Solid-State Circuits,* vol. 40, no. 4, pp. 838–845, Apr. 2005.

[45] M. Lee, Y. Choi, and J. Kim, "A 500-MHz, 0.76-W/mm Power Density and 76.2% Power Efficiency, Fully Integrated Digital Buck Converter in 65-nm CMOS," *IEEE Transactions on Industry Applications,* vol. 52, no. 4, pp. 3315–3323, 2016.

[46] D. Bhatia, L. Xue, P. Li, Q. Wu, and R. Bashirullah, "High-Voltage Tolerant Digitally Aided DCM/PWM Multiphase DC-DC Boost Converter With Integrated Schottky Diodes in 0.13 μm 1.2 V Digital CMOS Process," *IEEE Journal of Solid-State Circuits,* vol. 48, no. 3, pp. 774–789, Mar. 2013.

[47] C. R. Sullivan, "Integrating Magnetics for on-Chip Power: Challenges and Opportunities," *Custom Integrated Circuits Conference*, pp. 291–298, Sep 2009.

[48] P. Artillan, M. Brunet, D. Bourrier, J.-P. Laur, N. Mauran, L. Bary, M. Dilhan, B. Estibals, C. Alonso, and J. L. Sanchez, "Integrated LC Filter on Silicon for DC–DC Converter Applications," *IEEE Transactions on Power Electronics,* vol. 26, no. 8, pp. 2319−2325, Aug. 2011.

[49] F. C. Lee, and Q. Li, "High-Frequency Integrated Point-of-Load Converters: Overview," *IEEE Transactions on Power Electronics,* vol. 28, no. 9, pp. 4127−4136, Sep. 2013.

[50] P. Dhagat, S. Prabhakaran, and C. R. Sullivan, "Comparison of Magnetic Materials for V-Groove Inductors in Optimized High-Frequency DC-DC Converters," *IEEE Transactions on Magnetics,* vol. 40, no. 4, pp. 2008–2010, Jul. 2004.

[51] C. R. Sullivan, D. V. Harburg, J. Qiu, C. G. Levey, and D. Yao, "Integrating Magnetics for On-Chip Power: A Perspective," *IEEE Transactions on Power Electronics,* vol. 28, no. 9, pp. 4342–4353, Sep. 2013.

[52] K. Dongwon, and G. A. Rincon-Mora, "Single-Inductor–Multiple-Output Switching DC–DC Converters," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 56, no. 8, pp. 614–618, Aug. 2009.

[53] D. Ma, and R. Bondade, "Enabling Power-Efficient DVFS Operations on Silicon," *IEEE Circuits and Systems Magazine,* vol. 10, no. 1, pp. 14–30, Mar. 2010.

[54] M. Y. Jung, S. H. Park, J. S. Bang, and G. H. Cho, “An Error-Based Controlled Single-Inductor 10-Output DC-DC Buck Converter With High Efficiency Under Light Load Using Adaptive Pulse Modulation,” *IEEE Journal of Solid-State Circuits,* vol. 50, no. 12, pp. 2825–2838, Dec. 2015.

[55] Y. Zhang, and D. Ma, “A Fast-Response Hybrid SIMO Power Converter with Adaptive Current Compensation and Minimized Cross-Regulation,” *IEEE Journal of Solid-State Circuits,* vol. 49, no. 5, pp. 1242−1255, May 2014.

[56] D. Ma, W. H. Ki, and C. Y. Tsui, “A Pseudo-CCM/DCM SIMO Switching Converter with Freewheel Switching,” *IEEE Journal of Solid-State Circuits,* vol. 38, no. 6, pp. 1007–1014, Jun. 2003.

[57] Y. Zheng, M. Ho, J. Guo, K. L. Mak, and K. N. Leung, “A Single-Inductor Multiple-Output Auto-Buck-Boost DC–DC Converter With Autophase Allocation,” *IEEE Transactions on Power Electronics,* vol. 31, no. 3, pp. 2296–2313, Mar. 2016.

[58] D. Ma, W. H. Ki, C. Y. Tsui, and P. K. T. Mok, “Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode,” *IEEE Journal of Solid-State Circuits,* vol. 38, no. 1, pp. 89–100, Jan. 2003.

[59] E. Bonizzoni, F. Borghetti, P. Malcovati, F. Maloberti, and B. Niessen, “A 200mA 93% Peak Efficiency Single-Inductor Dual-Output DC-DC Buck Converter,” *IEEE International Solid-State Circuits Conference*, pp. 526–619, Feb. 2007.

[60] H. P. Le, C. S. Chae, K. C. Lee, S. W. Wang, G. H. Cho, and G. H. Cho, “A Single-Inductor Switching DC-DC Converter With Five Outputs and Ordered Power-Distributive Control,” *IEEE Journal of Solid-State Circuits,* vol. 42, no. 12, pp. 2706–2714, Dec. 2007.

[61] M. Belloni, E. Bonizzoni, E. Kiseliovas, P. Malcovati, F. Maloberti, T. Peltola, and T. Teppo, “A 4-Output Single-Inductor DC-DC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current,” *IEEE International Solid-State Circuits Conference*, pp. 444–626, Feb. 2008.

[62] C. S. Chae, H. P. Le, K. C. Lee, G. H. Cho, and G. H. Cho, “A Single-Inductor Step-Up DC-DC Switching Converter With Bipolar Outputs for Active Matrix

OLED Mobile Display Panels," *IEEE Journal of Solid-State Circuits,* vol. 44, no. 2, pp. 509–524, Feb. 2009.

[63] K. S. Seol, Y. J. Woo, G. H. Cho, G. H. Gho, and J. W. Lee, "A Synchronous Multioutput Step-Up/Down DC–DC Converter With Return Current Control," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 56, no. 3, pp. 210–214, Mar. 2009.

[64] M. H. Huang, and K. H. Chen, "Single-Inductor Multi-Output (SIMO) DC-DC Converters With High Light-Load Efficiency and Minimized Cross-Regulation for Portable Devices," *IEEE Journal of Solid-State Circuits,* vol. 44, no. 4, pp. 1099–1111, Apr. 2009.

[65] W. Xu, Y. Li, X. Gong, Z. Hong, and D. Killat, "A Dual-Mode Single-Inductor Dual-Output Switching Converter With Small Ripple," *IEEE Transactions on Power Electronics,* vol. 25, no. 3, pp. 614–623, Mar. 2010.

[66] K. C. Lee, C. S. Chae, G. H. Cho, and G. H. Cho, "A PLL-Based High-Stability Single-Inductor 6-Channel Output DC-DC Buck Converter," *IEEE International Solid-State Circuits Conference*, pp. 200–201, Feb. 2010.

[67] M. H. Huang, Y. N. Tsai, and K. H. Chen, "Sub-1 V Input Single-Inductor Dual-Output (SIDO) DC–DC Converter With Adaptive Load-Tracking Control (ALTC) for Single-Cell-Powered Systems," *IEEE Transactions on Power Electronics,* vol. 25, no. 7, pp. 1713–1724, Jul. 2010.

[68] C.-S. Huang, D. Chen, C. J. Chen, and K. H. Liu, "Mix-Voltage Conversion for Single-Inductor Dual-Output Buck Converters," *IEEE Transactions on Power Electronics,* vol. 25, no. 8, pp. 2106–2114, Aug. 2010.

[69] Y. H. Lee, T. C. Huang, Y. Y. Yang, W. S. Chou, K. H. Chen, C. C. Huang, and Y. H. Lin, "Minimized Transient and Steady-State Cross Regulation in 55-nm CMOS Single-Inductor Dual-Output (SIDO) Step-Down DC-DC Converter," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 11, pp. 2488–2499, Nov. 2011.

[70] W. Xu, Y. Li, Z. Hong, and D. Killat, "A 90% Peak Efficiency Single-Inductor Dual-Output Buck-Boost Converter with Extended-PWM Control," *IEEE International Solid-State Circuits Conference*, pp. 394–396, Feb. 2011.

[71] S. W. Wang, G. H. Cho, and G. H. Cho, "A High-Stability Emulated Absolute Current Hysteretic Control Single-Inductor 5-Output Switching DC-DC Converter with Energy Sharing and Balancing," *IEEE International Solid-State Circuits Conference*, pp. 276–278, Feb. 2012.

[72] Y. J. Moon, Y. S. Roh, J. C. Gong, and C. Yoo, "Load-Independent Current Control Technique of a Single-Inductor Multiple-Output Switching DC–DC converter," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 59, no. 1, pp. 50–54, Jan. 2012.

[73] C. W. Kuan, and H. C. Lin, "Near-Independently Regulated 5-Output Single-Inductor DC-DC Buck Converter Delivering 1.2W/mm^2 in 65nm CMOS," *IEEE International Solid-State Circuits Conference*, pp. 274–276, Feb. 2012.

[74] C. N. Onwuchekwa, and A. Kwasinski, "A Modified-Time-Sharing Switching Technique for Multiple-Input DC–DC Converters," *IEEE Transactions on Power Electronics,* vol. 27, no. 11, pp. 4492–4502, Nov. 2012.

[75] P. Patra, A. Patra, and N. Misra, "A Single-Inductor Multiple-Output Switcher With Simultaneous Buck, Boost, and Inverted Outputs," *IEEE Transactions on Power Electronics,* vol. 27, no. 4, pp. 1936–1951, Apr. 2012.

[76] J. Kim, D. S. Kim, and C. Kim, "A Single-Inductor Eight-Channel Output DC–DC Converter With Time-Limited Power Distribution Control and Single Shared Hysteresis Comparator," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 60, no. 12, pp. 3354–3367, Dec. 2013.

[77] W. C. Chen, Y. P. Su, T. C. Huang, T. W. Tsai, R. H. Peng, K. L. Lin, K. H. Chen, Y. H. Lin, C. C. Lee, S. R. Lin, and T. Y. Tsai, "Single-Inductor Quad-Output Switching Converter With Priority-Scheduled Program for Fast Transient Response and Unlimited Load Range in 40 nm CMOS Technology," *IEEE Journal of Solid-State Circuits,* vol. 50, no. 7, pp. 1525–1539, Jul. 2015.

[78] Y. Zheng, M. Ho, J. Guo, and K. N. Leung, "A Single-Inductor Multiple-Output Auto-Buck–Boost DC–DC Converter With Tail-Current Control," *IEEE Transactions on Power Electronics,* vol. 31, no. 11, pp. 7857–7875, Nov. 2016.

[79] G. A. Rincon-Mora, *Power IC Design - Fifth Edition*, Lulu, Raleigh, 2016.

[80] A. I. Pressman, K. Billings, and T. Morey, *Switching Power Supply Design*, McGraw-Hill, 2009.

[81] X. Duan, and A. Q. Huang, "Current-Mode Variable-Frequency Control Architecture for High-Current Low-Voltage DC–DC Converters," *IEEE Transactions on Power Electronics,* vol. 21, no. 4, pp. 1133–1137, Jul. 2006.

[82] M. Y. Jung, S. H. Park, J. S. Bang, D. C. Park, S. U. Shin, and G. H. Cho, "An Error-Based Controlled Single-Inductor 10-Output DC-DC Buck Converter with High Efficiency at Light Load Using Adaptive Pulse Modulation," *IEEE International Solid-State Circuits Conference*, pp. 1–3, Feb. 2015.

[83] N. Keskar, and G. A. Rincon-Mora, "Designing an Accurate and Robust LC-Compliat Asynchronous DS Boost DC-DC Converter," *IEEE International Symposium on Circuits and Systems*, pp. 549–552, May 2007.

[84] K. Lee, F. C. Lee, and M. Xu, "A Hysteretic Control Method for Multiphase Voltage Regulator," *IEEE Transactions on Power Electronics,* vol. 24, no. 12, pp. 2726–2734, Dec. 2009.

[85] P. Mattavelli, L. Rossetto, and G. Spiazzi, "Small-Signal Analysis of DC–DC Converters with Sliding Mode Control," *IEEE Transactions on Power Electronics,* vol. 12, no. 1, pp. 96–102, Jan. 1997.

[86] S. C. Tan, Y. M. Lai, and C. K. Tse, "General Design Issues of Sliding-Mode Controllers in DC–DC Converters," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 3, pp. 1160–1174, Mar. 2008.

[87] P. Garces, J. Calvente, R. Leyva, R. Giral, and L. Martinez-Salamero, "Simulation-Oriented Continuous Model of Hysteretic Controlled DC-to-DC Converters," *IEEE International Symposium on Industrial Electronics*, pp. 633–637, Jun. 2007.

[88] S. K. Mishra, and K. D. T. Ngo, "Dynamic Characterization of the Synthetic Ripple Modulator in a Tightly Regulated Distributed Power Application," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 4, pp. 1164–1173, Apr. 2009.

[89] Y. F. Liu, and P. C. Sen, "Large-Signal Modeling of Hysteretic Current-Programmed Converters," *IEEE Transactions on Power Electronics,* vol. 11, no. 3, pp. 423–430, May 1996.

[90] J. Sun, “Small-Signal Modeling of Variable-Frequency Pulsewidth Modulators,” *IEEE Transactions on Aerospace and Electronic Systems,* vol. 38, no. 3, pp. 1104–1108, Jul. 2002.

[91] C. C. Chuang, H. P. Chou, and M. L. Chiu, “A Buck Converter Using Accurate Synthetic Ripple Hysteresis Control Scheme,” *IEEE International Conference on Power Electronics and Drive Systems*, pp. 682–686, Dec. 2011.

[92] R. Redl, “Small-Signal High-Frequency Analysis of the Free-Running Current-Mode-Controlled Converter,” *IEEE Power Electronics Specialists Conference*, pp. 897–906, Jun. 1991.

[93] J. h. Park, and B. H. Cho, “Small signal modeling of hysteretic current mode control using the PWM switch model,” *IEEE Workshops on Computers in Power Electronics*, pp. 225–230, Jul. 2006.

[94] M. Castilla, L. Garcia de Vicuna, J. M. Guerrero, J. Matas, and J. Miret, “Design of voltage-mode hysteretic controllers for synchronous buck converters supplying microprocessor loads,” *IEE Proceedings - Electric Power Applications,* vol. 152, no. 5, pp. 1171–1178, Sep. 2005.

[95] P. E. Allen, and D. R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press, New York, 2002.

[96] H. P. Forghani-zadeh, and G. A. Rincon-Mora, “An Accurate, Continuous, and Lossless Self-Learning CMOS Current-Sensing Scheme for Inductor-Based DC-DC Converters,” *IEEE Journal of Solid-State Circuits,* vol. 42, no. 3, pp. 665–679, Mar. 2007.

[97] S. Kim, G. A. Rincon-Mora, and D. Kwon, “Extracting the Frequency Response of Switching DC–DC Converters in CCM and DCM from Time-Domain Simulations,” *International SoC Design Conference*, pp. 385–388, Nov. 2011.

[98] Y. Qiu, M. Xu, J. Sun, and F. C. Lee, “A Generic High-Frequency Model for the Nonlinearities in Buck Converters,” *IEEE Transactions on Power Electronics,* vol. 22, no. 5, pp. 1970–1977, Sep. 2007.

[99] R. Redl, and S. Jian, "Ripple-Based Control of Switching Regulators–An Overview," *IEEE Transactions on Power Electronics,* vol. 24, no. 12, pp. 2669–2680, Dec. 2009.

[100] C.-C. Fang, and R. Redl, "Switching Frequency Determination of DC-DC Converters with Hysteretic Control," *IEEE Transactions on Power Electronics,* vol. PP, no. 99, pp. 1–1, DOI: 10.1109/tpel.2017.2695584 2017.

[101] Y. Wen, and O. Trescases, "Analysis and Comparison of Frequency Stabilization Loops in Self-Oscillating Current Mode DC–DC Converters," *IEEE Transactions on Power Electronics,* vol. 28, no. 10, pp. 4753–4766, Oct. 2013.

[102] T. Szepesi, "Stabilizing the Frequency of Hysteretic Current-Mode DC-DC Converters," *IEEE Transactions on Power Electronics*, no. 4, pp. 302–312, Oct. 1987.

[103] J. Doernberg, P. R. Gray, and D. A. Hodges, "A 10-bit 5-Msample/s CMOS Two-Step Flash ADC," *IEEE Journal of Solid-State Circuits,* vol. 24, no. 2, pp. 241–249, Apr. 1989.

[104] S. Kim, and G. A. Rincon-Mora, "Achieving High Efficiency under Micro-Watt Loads with Switching Buck DC-DC Converters," *Journal of Low Power Electronics,* vol. 4, no. 2, pp. 229–240, Aug. 2009.

[105] H. C. Foong, Y. Zheng, Y. K. Tan, and M. T. Tan, "Fast-Transient Integrated Digital DC-DC Converter With Predictive and Feedforward Control," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 59, no. 7, pp. 1567–1576, Jul. 2012.

[106] P. J. Liu, W. S. Ye, J. N. Tai, H. S. Chen, J. H. Chen, and Y. J. E. Chen, "A High-Efficiency CMOS DC-DC Converter With 9-μs Transient Recovery Time," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 59, no. 3, pp. 575–583, Mar. 2012.

[107] R. Redl, B. P. Erisman, and Z. Zansky, "Optimizing the Load Transient Response of the Buck Converter," *Applied Power Electronics Conference and Exposition*, pp. 170–176, Feb. 1998.

[108] A. B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*, John Wiley & Sons, New York, 1984.

[109] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, New York, 2000.

[110] K. Filsoof, and P. W. Lehn, "A Bidirectional Multiple-Input Multiple-Output Modular Multilevel DC–DC Converter and its Control Design," *IEEE Transactions on Power Electronics,* vol. 31, no. 4, pp. 2767–2779, Apr. 2016.

[111] B. Wang, L. Xian, V. R. K. Kanamarlapudi, K. J. Tseng, A. Ukil, and H. B. Gooi, "A Digital Method of Power-Sharing and Cross-Regulation Suppression for Single-Inductor Multiple-Input Multiple-Output DC–DC Converter," *IEEE Transactions on Industrial Electronics,* vol. 64, no. 4, pp. 2836–2847, Apr. 2017.

[112] H. Behjati, and A. Davoudi, "A Multiple-Input Multiple-Output DC–DC Converter," *IEEE Transactions on Industry Applications,* vol. 49, no. 3, pp. 1464–1479, Jun. 2013.

[113] S. Kim, and G. A. Rincón-Mora, "Dual-source hysteretic switched-inductor 0.18 μm complementary metal–oxide–semiconductor charger-supply system," *IET Circuits, Devices & Systems,* vol. 9, no. 4, pp. 275–282, 2015.

[114] Y. Jiang, and A. Fayed, "A 1 A, Dual-Inductor 4-Output Buck Converter With 20 MHz/100 MHz Dual-Frequency Switching and Integrated Output Filters in 65 nm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 51, no. 10, pp. 2485–2500, Oct. 2016.

[115] R. Baker, *CMOS Cricuit Design, Layout, and Simulation - Revised Second Edition*, John Wiley & Sons, New Jersey, 2008.

VITA

CARLOS J. SOLIS

Carlos Solis received the B.S. in Electrical and Computer Engineering in 2010 from the University of Puerto Rico – Mayaguez Campus. In 2012, he received the M.S. from Georgia Institute of Technology in Electrical and Computer Engineering. He joined Georgia Tech Analog, Power, and Energy IC Lab (GTAPE) in 2010, where he started to pursue his Ph.D. degree. He was the recipient of the GEM Fellowship from 2010 to 2012 and from the Goizueta Foundation Fellowship from 2012 to 2016. His research interest includes switched-inductor power converter ICs, stability analysis, analog IC design. Currently, he is working in Analog Devices as a Design Engineer for Power Products.