High Performance AlGaN Heterostructure Field-Effect Transistors

Program Objectives

The primary objectives of this program were to develop materials growth processes and epitaxial device structures for the improved performance of AlGaN/GaN-based heterostructure field-effect transistors (HFETs) and to deliver HFET epitaxial structures on semi-insulating GaN free-standing substrates for device fabrication and testing. We have used metalorganic chemical vapor deposition (MOCVD) for the growth of the device structures on semi-insulating GaN substrates that were provided by Kyma Technologies. Materials growth studies were performed at the Center for Compound Semiconductors of Georgia Institute of Technology (P.I. Dr. R. D. Dupuis).

Research Activity Summary

In this program, we have investigated mainly two effects on HFET performance characteristics: one is the optimization of growth parameters and epitaxial structures on free-standing GaN substrates and the other is the control of an unwanted charge layer near the regrowth interface of the HFET structures by Fe doping and photo-enhanced chemical etching. The materials and epitaxial structures were grown by MOCVD in a reactor system equipped with close-coupled showerhead chamber (manufactured by Thomas Swan Scientific Equipment) using precursors of TMGa (trimethylgallium), TMAl (trimethylaluminum), NH_3, and Cp_2Fe (ferrocene (bis(cyclopentadienyl)iron)) in a H_2 carrier gas ambient. The substrate used for calibration and device structures were sapphire, SiC, (for calibration and reference wafers), and free standing GaN substrates (for device structures for the fabrication).

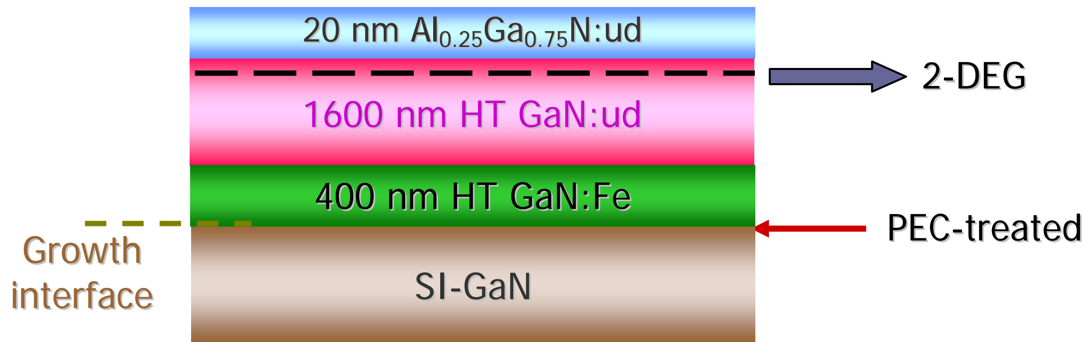


Figure 1: Schematic epitaxial structures of HFETs grown on semi-insulating (SI) free-standing GaN substrates in this study.

Figure 1 shows the schematic epitaxial structures of HFETs used in this study. Note that the structures were grown on free-standing semi-insulating GaN substrates that are Fe-doped and grown and wafer-prepared at Kyma Technologies. The substrates have a significantly lower dislocation density than GaN template on foreign substrates such as the sapphire and SiC substrates. These substrates are expected to provide improved device performance characteristics due to significantly reduced threading dislocation densities in the epitaxial structures. The epitaxial structures are standard typical HFET structures consisting of a GaN buffer layer and an $Al_{0.25}Ga_{0.75}N$ cap layer with a thickness of 20 nm. X-ray diffraction ω-2θ scan and the simulation are show in Figure 2. The structures also have a Fe-doped GaN layer and a photo-enhanced chemically etched surface, as indicated in Figure 1, which will be

described further in detail later. For the optimization of HFET growth parameters and a layer transition scheme, we have performed growth calibrations in terms of (i) a sheet charge concentration and a mobility of 2-dimenstional electron gas; (ii) a surface morphology of AlGaN cap layer; and (iii) C-V characteristics of the epitaxial structure using mercury C-V measurement. From the standard HFET structure (as shown in Figure 1) with optimized growth parameters, ~500 Ω/☐ of sheet resistance was obtained. Figure 3 shows a sheet resistance mapping and a sheet resistance vs. depth profile of a HFET structure grown on a free-standing SI-GaN substrate. In addition, by optimizing the growth parameters of AlGaN cap layer and improving the wafer process of the GaN substrates, excellent step-flow morphology was achieved for the HFETs grown on both sapphire and GaN free-standing substrates (as shown in Figure).

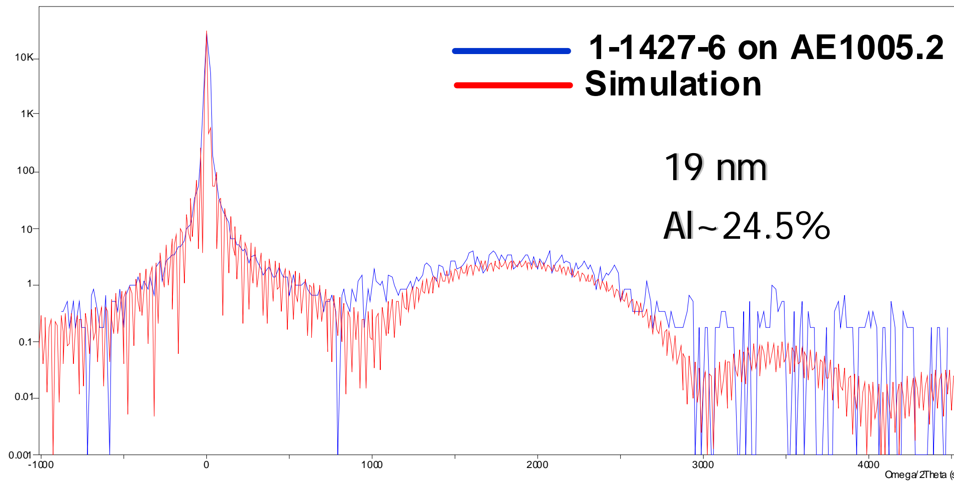
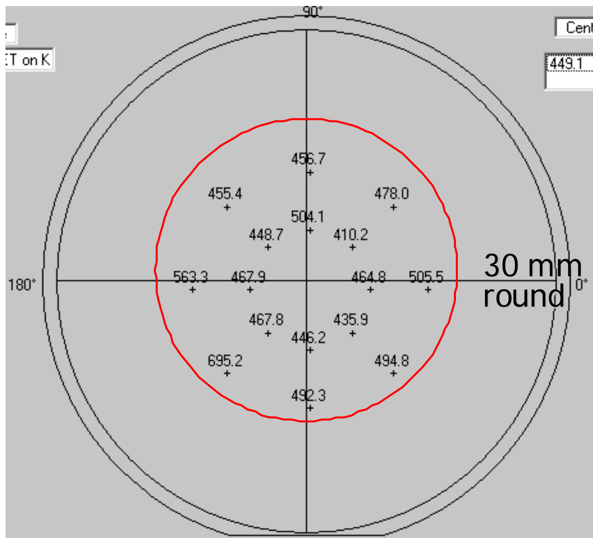


Figure 2: X-ray diffraction ω-2θ scan and simulation of a standard HFET structure grown on a free-standing SI-GaN substrate.



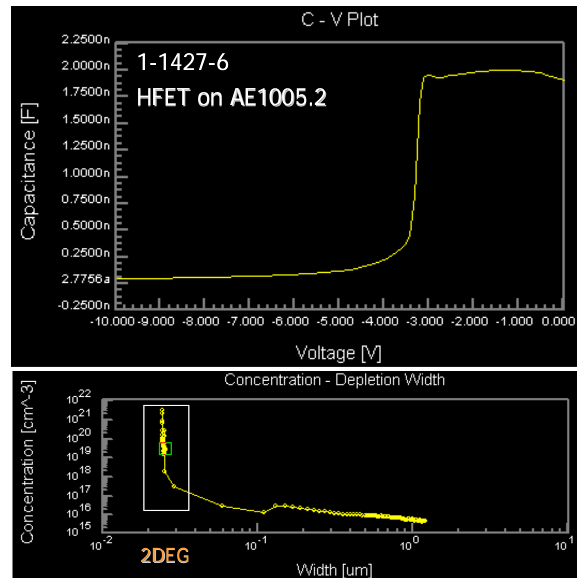


Figure 3: (a) Sheet resistance mapping measured by contactless measurement system and (b) sheet resistance vs. depth profile by mercury C-V measurement of a standard HFET structure grown on a free-standing SI-GaN substrate.

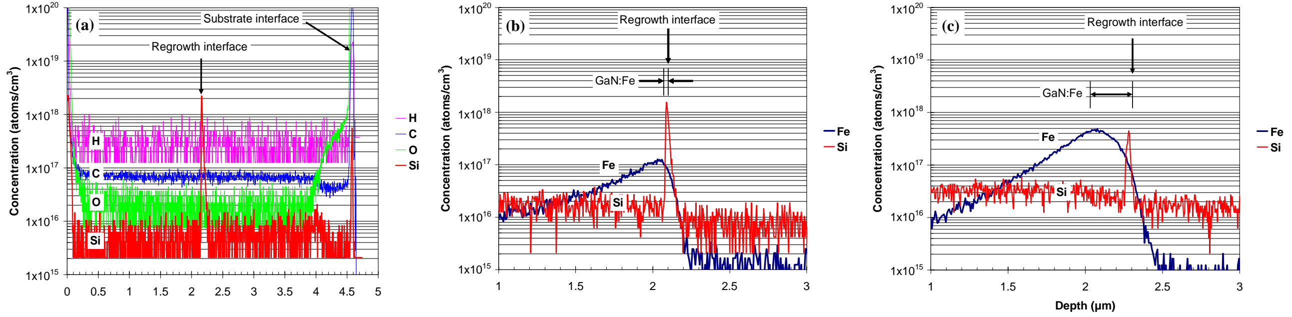


Figure 4: SIMS profiles of Fe, Si, and other impurity concentrations of the HFET structures having different Fe doping schemes: (a) undoped GaN layer (#877), and (b) 50-nm thick Fe-doped layer (#884), and (c) 280-nm thick Fe-doped layer (#885) at the re-growth interface grown on undoped GaN template.

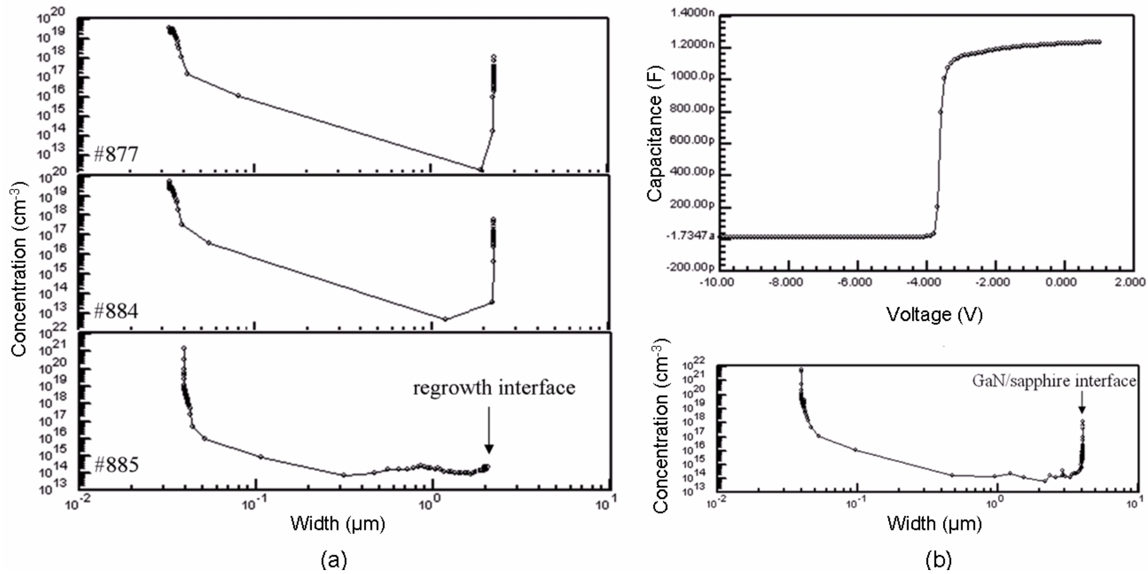


Figure 5: (a) Charge concentration vs. penetration depth profiles as determined by capacitance-voltage (C-V) measurements for the HFET structures with an undoped GaN layer (#877), a 50 nm thick Fe-doped GaN layer (#884), and a 280 nm thick Fe-doped GaN layer (#885) at the re-growth interface with voltage range to -6 V. (b) C-V characteristic of the HFET structure with a 280-nm thick Fe-doped GaN layer (#885) at the re-growth interface with a voltage range to -10.

As described earlier, beneficial effects of reduced threading dislocation density in the epitaxial structure are expected from the HFET grown on the GaN substrates; however, other technical issues that are associated with the HFETs on GaN substrates need to be addressed. First, the GaN substrates prepared from a HVPE-grown thick film are generally intrinsically n-type that make high-speed operation of HFET devices on those substrates difficult. Semi-insulating GaN substrates are required and this was achieved by Fe doping during the growth of HVPE thick film. This technology has been developed at Kyma Technology and these semi-

insulating GaN substrates are used in this study. Second, for the epitaxial growth of HFET structures on the GaN substrates an unwanted charge layer may be introduced near the regrowth interface. This problem is rather unique to the GaN substrates in contrast to SiC substrates on which an AlN buffer layer (that is intrinsically insulating even with an auto-doping effect) was used. This unwanted interface charge layer is suspected to be introduced by auto-doping effect of Si and O during the heating up for the epitaxial structure growth or the preparation of wafers such as the chemo-mechanical polishing. We focused on the control of interface charge with different Fe-doped GaN layers.[1] For the GaN/sapphire template growth, the initial GaN layer is unintentionally doped, that is, Fe doping was not introduced near the GaN-sapphire substrate interface, in order that the charge at the interface of the GaN template and the sapphire substrate can be used as a marker for C-V measurements. In order to investigate the effect of the Fe doping at the re-growth interface, three HFET samples with different Fe doping schemes at the re-growth interface were prepared: GaN:ud (#877), 50-nm thick GaN:Fe (#884), and 280-nm thick GaN:Fe (#885) grown on the ~2-μm GaN:ud templates with same layer thickness (~2 μm) and crystalline quality in the HFET structures. Figure 4 (a) shows the SIMS depth profiles of the HFET structures without a GaN:Fe layer (#877). It is found that Si impurities with a concentration of $\sim 2\times 10^{18}$ cm^{-3} are incorporated at the regrowth interface even though the structure does not have any Si doping in the bottom layer before the growth of the HFET structure. Also, the thickness of the unintentional Si-doped layer is estimated to be ~50 nm. Other impurity-related peaks such as C and O are not detected at the re-growth interface using our surface preparation conditions prior to the re-growth. For the compensation of unintentional Si-doped layer at the re-growth interface, a GaN layer with $[Fe]>2\times 10^{18}$ cm^{-3} having the thickness of 50 and 280 nm was introduced during the initial re-growth of GaN. The influence of different Fe doping at the re-growth interface in the HFET structures as determined by C-V profiling is shown in Figure 5 (a). These C-V profiles show that well-defined 2-DEGs are created at the AlGaN/AlN/GaN interface. Comparing the charge associated with the re-growth interface, the interface charge is observed at a depth of ~2 μm, which corresponds to the re-growth interface, for the HFET structure #877 and #884, while no such charge accumulation is observed for #885. Compensation of the Si impurities by Fe doping was expected for both HFET structures #884 and #885, since both of them, in principle, have a large enough thickness and concentration of the GaN:Fe layer for compensation. To further investigate the difference between #884 and #885, the SIMS depth profiles were measured again and they are shown in Figure 4 (b) and (c). For both profiles, a "delayed turn-on" of Fe is observed, that is, [Fe] gradually increases as the growth proceeds even when using the same precursor inputs from the beginning of the growth. This delayed turn-on can be explained by (i) a "reactor surface saturation effect" as is typically also observed with Cp_2Mg (bis(cyclopentadienyl)magnesium) or by (ii) the segregation of the Cp_2Fe precursor or Fe atoms before being incorporated into the lattice at the growth surface . Also, we believe that the "tailing off" of the Fe profile is not related to the Fe diffusion, since tailing does not go deeper beyond Si-related peak, which is located at re-growth interface. As a result of delayed turn-on, the structure #884 does not have enough Fe doping to fully compensate the Si at the re-growth interface, while wafer #885 has a similar Fe concentration to the Si concentration at the interface. The peaks for the Fe concentration and the Si concentration are not located at the same position but we think that the

[1] The detailed study was published: W. Lee, J. H. Ryou, D. Yoo, J. Limb, R. D. Dupuis, D. Hanser, E. Preble, N. M. Williams, and K. Evans, "Optimization of Fe doping at the re-growth interface of GaN for the applications to III-nitride-based heterostructure field effect transistors," *Appl. Phys. Lett.* **90**, 093509-1-3 (2007).

integrated Fe concentration and the Si peak are approximately within a Debye length so that effective compensation can occur. For complete compensation of the unintentional incorporation of Si at the re-growth interface, proper thickness of Fe-doped layer as well as concentration of Fe is required due to the delayed turn-on effect of the Fe doping. We also note a decreased Si auto-doping at the re-growth interface for HFET structure #885 as compared to #877. This can be ascribed to SIMS calibration issues or reactor condition changes. However, we also consider the possibility that Fe doping, besides affecting the electrical compensation of Si, could also affect the Si dopant incorporation through a lattice site competition mechanism between Fe and Si atoms.

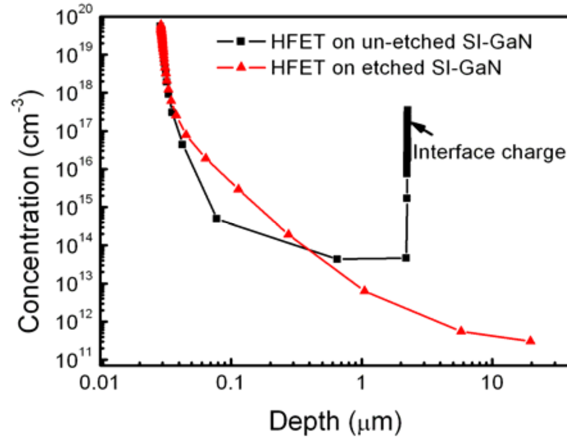


Figure 6: C-V profiles of charge concentration vs. depth for HFETs grown on un-etched and PEC-etched SI-GaN substrates.

The scheme of compensation of the unwanted charge layer by Fe doping was applied to the growth of the HFET structures on the SI-GaN substrates but this scheme did not work, that is, the Fe doping could not remove the interface charge for the HFETs on SI-GaN substrates. The difference between the regrowth interface of GaN template on the sapphire substrate and the growth interface of SI-GaN substrate, and the origin of additional charge from HFET on SI-GaN bulk substrate are not fully understood. We believe, in the case of the SI-GaN substrate, additional charge may be related to the surface preparation of bulk substrate including slicing and chemo-mechanical polishing (CMP), which is suspected to result in the formation of charge layer on the surface. This additional charge layer cannot be removed by other surface treatments such as wet chemical etching, in-situ thermal etching, and plasma dry etching.[2] This additional charge layer can only be removed by photo-enhanced chemical etching of the surface of SI-GaN substrates which is suspected to contain the Si-doped charge layer.[3] Figure 6 shows the capacitance-voltage (C-V) measurement results for HFETs grown on the un-etched GaN substrate and etched GaN substrate. Both charge concentration vs. depth profiles show that well-defined 2-DEGs are created at the AlGaN/GaN interface, and the charge concentrations are

[2] The detailed study was published: J.-H. Ryou, J. P. Liu, Y. Zhang, C. A. Horne, W. Lee, S.-C. Shen, and R. D. Dupuis "Surface treatment on the growth surface of semi-insulating GaN bulk substrate for III-nitride heterostructure field-effect transistors," *Phys. Stat. Sol.* **5**, 1849-1851 (2008).
[3] The detailed study was published: J. P. Liu, J.-H. Ryou, D. Yoo, Y. Zhang, J. Limb, C. A. Horne, S.-C. Shen, R. D. Dupuis, A. D. Hanser, E. A. Preble, and K. R. Evans, "III-nitride heterostructure field-effect transistors grown on semi-insulating GaN substrate without regrowth interface charge," *Appl. Phys. Lett.* **92**, 133513-1-3 (2008).

almost same. The data also show that charge is observed in the HFET structure grown on un-etched GaN substrate at a depth of 2.5 µm, which corresponds to the re-growth interface; whereas, no such charge accumulation is observed for the HFET grown on the PEC-etched GaN substrate, even though the same Fe doping conditions were used for both layers. SIMS measurements were performed on both HFET samples, as shown in Figure 7. Fe concentrations are ~2×10^{18} cm^{-3} corresponding to the semi-insulating GaN:Fe substrates and similar ~7×10^{18} cm^{-3} with "delayed turn-on" and a "tailing off" in epitaxial GaN:Fe by MOCVD. As expected, the Fe incorporation is almost equal, since these two samples were grown in the same run. The data show that the Si impurity concentration at a depth of 2.5 µm, which corresponds to the regrowth interface, is significantly different for these two samples. The Si concentration for the HFET grown on the un-etched SI GaN substrate is ~6.3×10^{18} cm^{-3}, while it is only ~1.2×10^{18} cm^{-3} for the HFET on the PEC-etched SI-GaN substrate. As an indicator of layer thickness containing the Si impurities, the SIMS data show a Si peak full-width at half-maximum (FWHM) ~49.4 nm for the HFET grown on un-etched SI GaN substrate, while it is ~44.3 nm for the HFET grown on the etched SI-GaN substrate. Since the only difference for these two HFET samples is the PEC etching processing, we believe the PEC-etching of the SI-GaN substrate reduces the Si impurity concentration on the surface of SI-GaN substrate, which results in the reduced interface charge after re-growth for the HFET structure grown on the PEC-etched SI-GaN substrate. We also observed a Si impurity peak at the regrowth interface between the HFET structures and the GaN:ud template. However, in that case, the Si peak concentration is between 4.5×10^{17} cm^{-3} and 1.5×10^{18} cm^{-3}, varying with different samples. Moreover, the Si impurity peak FWHM is between 13.1 nm and 17.1 nm. Therefore, both the Si peak concentration and the layer thickness containing Si impurity are much lower than that observed in the HFET grown on the un-etched SI GaN substrate. We believe that the additional Si impurities at the interface originate from the preparation process employed for the SI-GaN substrate. We believe that the additional Si impurities located at the surface of the SI-GaN substrate are the reason why it is found that Fe doping of the epitaxial GaN layer cannot compensate the Si impurities for HFETs grown on un-etched SI-GaN substrates. PEC etching significantly reduces the Si impurity concentration located at the surface of the SI-GaN substrate, and so Fe doping can compensate completely the Si impurities and, consequently, the charge is eliminated at the re-growth interface for the HFET structure grown on the etched SI-GaN substrate.

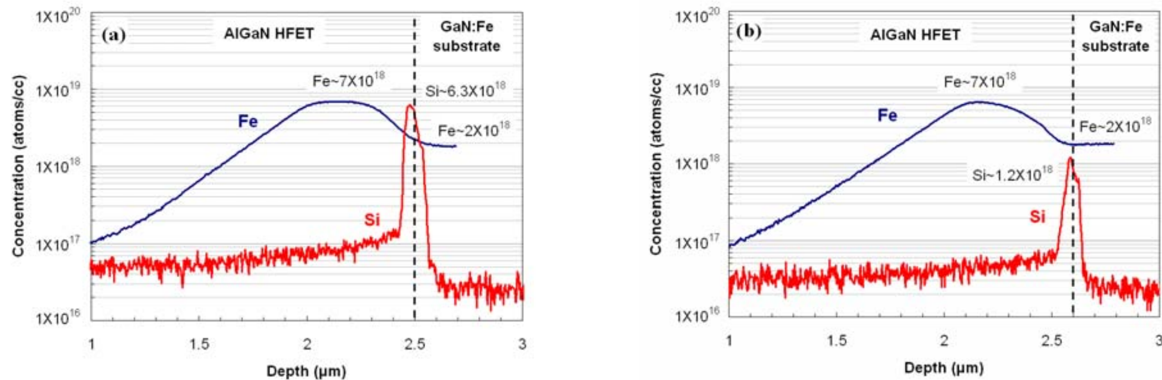


Figure 7: C-V profiles of charge concentration vs. depth for HFETs grown on un-etched and PEC-etched SI-GaN substrates.

Based on the calibration and investigation performed on the growth parameter optimization and the control of the unwanted charge layers, we have grown several batches of HFET structures on the SI-GaN substrates and they were delivered to Kyma Technologies for device fabrication and testing. Some of the epitaxial structures were fabricated to show decent performance characteristics, which will not be discussed in this report and more structures that were delivered recently (and expected to be better than previous batches) will be fabricated.

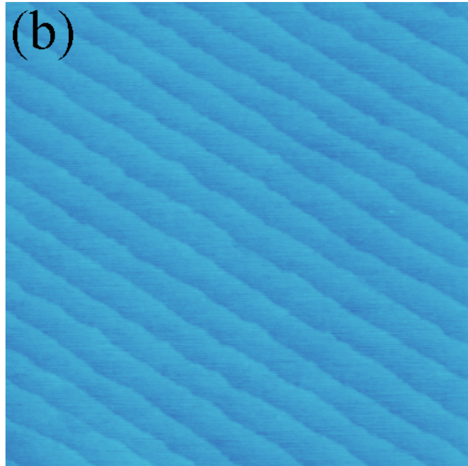


Figure 8: AFM images ($1\times1\ \mu m^2$, z=10nm) of a HFET on a PEC-etched SI-GaN substrate.