

# **High-Performance Organic Field-Effect Transistors and Circuits for 3D-Shape Substrates and Applications**

A Dissertation  
Presented to  
The Academic Faculty

By

Sangmoo Choi

In Partial Fulfillment  
Of the Requirements for the Degree  
Doctor of Philosophy in the  
School of Electrical and Computer Engineering

Georgia Institute of Technology

August 2016

Copyright © 2016 by Sangmoo Choi

**High-Performance Organic Field-Effect Transistors and Circuits for  
3D-Shape Substrates and Applications**

Approved by:

Dr. Bernard Kippelen, Advisor  
School of Electrical and Computer  
Engineering  
*Georgia Institute of Technology*

Dr. Muhannad Bakir  
School of Electrical and Computer  
Engineering  
*Georgia Institute of Technology*

Dr. Elsa Reichmanis  
School of Chemistry and Biochemistry  
*Georgia Institute of Technology*

Dr. Farrokh Ayazi  
School of Electrical and Computer  
Engineering  
*Georgia Institute of Technology*

Dr. Jeffrey A. Davis  
School of Electrical and Computer  
Engineering  
*Georgia Institute of Technology*

Date Approved: April 27<sup>th</sup>, 2016

## **Acknowledgements**

I would like to sincerely thank my advisor, Dr. Bernard Kippelen, for his advice, and willing to support my research as well as my family in the U.S. In the research, he has been the best advisor keeping me persistent and thorough on any details and rational. I also would like to thank Dr. Muhannad Bakir, Dr. Elsa Reichmanis, Dr. Farrokh Ayazi, and Dr. Jeffrey A. Davis for serving on my Ph. D. committee and for their guidance and participation in the review in this program.

I would like to thank all current Kippelen Research Group members, Dr. Canek Fuentes-Hernandez, Cheng-Yin Wang, Dr. Talha M. Khan, Felipe A. Larraín, Wen-Fang Chou, Victor A. Rodriguez-Toro, Xiaoqing Zhang, Xiaojia Jia, Dr. Michael Gaj as well as formal members, particularly Dr. Minseong Yun, Dr. Jaewon Shim, Dr. Sanjeev Singh, and Dr. Do-Kyung Hwang. Especially, I would like to thank Dr. Canek Fuentes-Hernandez for his invaluable guidance, and Cheng-Yin Wang for his support in using the SPECTROS system. Without their guidance and support, I would not be here. I would like to thank Ms. Tina Moseley for her support as an administrative manager in Kippelen Research Group.

This work was funded by Academic Training Program of Samsung Display, Office of Naval Research, and U.S. Department of Agriculture.

Lastly, my deepest gratitude goes to my family. Without them, this dissertation would not have been possible. Special thanks go to my wife, Hyang, for her continuous support and encouragement. This dissertation is dedicated to all of them.

# Table of Contents

Acknowledgements.....	iii
List of Figures.....	vii
List of Symbols and Abbreviations .....	xiii
Summary.....	xiv
CHAPTER 1 Introduction .....	1
1.1. Thin-film transistors.....	1
1.2. Organic field-effect transistors.....	4
1.2.1. Silicon semiconductors.....	4
1.2.2. Organic semiconductors .....	5
1.2.3. Comparisons between organic and inorganic semiconductors.....	7
1.2.4. Device geometry of organic field-effect transistors .....	9
1.2.5. Device operation of p-channel OFETs.....	11
1.2.6. Extraction of electrical parameters of OFETs.....	14
1.2.7. Current and potential applications.....	16
1.3. Recent progress in OFETs.....	16
1.3.1. Performance improvement in organic field-effect transistors .....	16
1.3.2. Operational and environmental stabilities of organic field-effect transistors.....	18
1.3.3. Substrates for organic field-effect transistors.....	19
1.3.4. Integrated circuits and applications of organic field-effect transistors ....	20
1.4. Objective and organization of the dissertation.....	21
CHAPTER 2 Experimental Methods.....	23
2.1. Device fabrication .....	23
2.1.1. Deposition of patterned metal electrodes and dopants .....	24
2.1.2. Deposition of self-assembled monolayer of PFBT .....	24
2.1.3. Solution processing of organic semiconductors .....	26
2.1.4. Deposition of bilayer gate dielectrics .....	27

2.1.5. Fabrication of shape-memory polymer substrates.....	29
2.2. Characterization of thin-films and OFETs .....	31
2.3. Design of OFET circuits .....	32
CHAPTER 3 Top-Gate OFETs with Low Contact Resistance .....	35
3.1. Introduction .....	35
3.1.1. Highly stable top-gate organic field-effect transistors .....	36
3.1.2. Contact resistance in top-gate TIPS-pentacene/PTAA OFETs .....	38
3.1.3. Contact resistance at metal-semiconductor interfaces.....	39
3.1.3.1 Injection resistance in OFETs.....	42
3.1.3.2 Pinning of Fermi level energy .....	45
3.1.3.3 Bulk resistance on the contacts of OFETs.....	47
3.1.4. Evaluation of contact resistance .....	48
3.2. Top-gate OFETs with contact-doped electrodes .....	50
3.2.1. Doping of organic semiconductors.....	50
3.2.2. Device structures of top-gate OFETs with contact-doped electrodes .....	53
3.2.3. Work function of electrodes .....	54
3.2.4. Thin Mo(tfd) <sub>3</sub> film on electrodes.....	56
3.2.5. Current-voltage characteristics of the top-gate OFETs .....	59
3.2.6. Contact resistance of OFETs with contact-doped electrodes .....	63
3.2.6.1 Dependence of contact resistance on the work function of electrodes .....	64
3.2.6.2 Vertical bulk resistance in contact area .....	66
3.2.6.3 Simulation of bulk resistance.....	71
3.2.6.4 Thickness and morphology of semiconductors on contact-doped electrodes .....	73
3.2.7. Contact resistance on low-cost electrodes.....	74
3.2.8. Conclusions .....	78
CHAPTER 4 Circuit Implementation on Shape-Memory Polymers.....	79
4.1. Low-cost patterning method for via-holes .....	79
4.1.1. Introduction .....	79
4.1.2. Reverse stamping method.....	81
4.1.2.1 Process steps .....	81

4.1.2.2 Characterization of via-holes .....	83
4.1.3. Implementation of circuits.....	87
4.1.4. Conclusions .....	90
4.2. Top-gate OFETs on shape-memory polymers .....	91
4.2.1. Introduction .....	91
4.2.2. Top-gate OFETs and circuits on SMPs .....	93
4.2.2.1 Modification of device structure for top-gate OFETs on SMPs.....	94
4.2.2.2 Current-voltage characteristics of the OFETs with the modified structure .....	96
4.2.2.3 Inverter circuits on SMPs .....	99
4.2.3. Conclusions .....	101
CHAPTER 5 Conclusions and Recommendations.....	103
5.1. Conclusions .....	103
5.2. Recommendations for future work.....	105
5.2.1. Contact resistance.....	105
5.2.2. Low-cost via-hole patterning.....	106
5.2.3. OFET circuits on SMPs.....	106
5.3. List of selected publications .....	107
References .....	108

## List of Figures

Figure 1.1. (a) Conceptual illustration of the formation of the energy band in crystalline silicon (inset figure: simplified schematic of an isolated silicon atom), and (b) the energy band diagram of crystalline silicon. ....	4
Figure 1.2 The schematic of the orbitals and bonds for two $sp^2$ hybridized carbon atoms. ....	6
Figure 1.3 (a) Formation of LUMO and HOMO bands in organic molecules and in organic films (adapted from [19]), and (b) the energy band diagram of organic semiconductors in a solid film. ....	7
Figure 1.4. Energy band diagram of (a) n- and p-type silicon semiconductors (b) p-channel, and (c) n-channel organic semiconductors. ....	8
Figure 1.5 cross-sectional views of device geometry for (a) bottom-gate bottom-contact, (b) bottom-gate top-contact, (c) top-gate bottom-contact, and (d) top-gate top-contact OFETs. ....	10
Figure 1.6. Energy level band diagram of an ideal MIS structure at (a) an equilibrium condition and (b) an accumulated condition by a negative gate-voltage bias in p-channel organic semiconductors. ....	11
Figure 1.7 (a) A device geometry and (b) symbols of p-channel, top-gate bottom-contact OFETs. ....	12
Figure 1.8. Typical $I$ - $V$ characteristics of p-channel OFETs: (a) transfer characteristics and (b) output characteristics. ....	13
Figure 1.9. Fitting from the slope of the straight line. ....	15
Figure 1.10. Progress in field-effect mobility values of organic field-effect transistors. .	17
Figure 2.1. Chemical structure of 2,3,4,5,6-Pentafluorothiophenol (Sigma Aldrich). ....	25
Figure 2.2. Formation of a self-assembled monolayer of PFBT on gold electrodes. ....	25
Figure 2.3. Chemical structure of (a) TIPS-pentacene and (b) PTAA (Sigma Aldrich). .	26
Figure 2.4. ALD example cycle for $Al_2O_3$ deposition (Cambridge NanoTech Inc.) ....	28
Figure 2.5. Fabrication procedure of shape-memory polymer substrates. ....	29
Figure 2.6. Dependence of Young's modulus of the SMP substrates on temperature ( $T_g$ : glass transition temperature). Adapted from [93]. ....	30
Figure 2.7. SPICE parameter extraction from transfer characteristics of OFETs. ....	32

Figure 2.8. Screen capture of Virtuoso Schematic Editor (Cadence).....	33
Figure 2.9. (a) Screen capture of Virtuoso ADE-L (Cadence) and (b) simulation results of inverter circuits.....	33
Figure 2.10. Screen capture of Virtuoso Layout Suite (Cadence).....	34
Figure 2.11. (a) Shadow masks used for source/drain and gate electrodes of the circuits and (b) the photograph of fabricated circuits on a 1.5-inch by 1.5-inch glass substrate. .	34
Figure 3.1 Cross-sectional view of top-gate TIPS-pentacene/PTAA OFETs.....	36
Figure 3.2 Degradation of top-gate TIPS-pentacene/PTAA OFETs in air in terms of their threshold voltages and field-effect mobility values for two years. Adapted from [53].....	36
Figure 3.3 Transfer characteristics of the top-gate OFETs in air and in water. Adapted from [56].....	37
Figure 3.4 The changes of the drain current of the top-gate OFET sensors in water by different pH values. Adapted from [56].....	37
Figure 3.5. Transfer characteristics of two different TIPS-pentacene/PTAA OFETs that have (a) high contact resistance and (b) low contact resistance. ....	38
Figure 3.6. Simple model of the contact resistance composition in top-gate OFETs.....	40
Figure 3.7. (a) Cross-sectional view of top-gate OFETs with simplified model of total resistance across the device ( $R_C$ is contact resistance and $R_{CH}$ is channel resistance), and (b) a comparison of drain current of two OFETs with different contact resistance values. ....	40
Figure 3.8. Overestimation of electrical parameters from transfer characteristics of OFETs.....	41
Figure 3.9. Injection energy barrier at the interface of metal and p-channel semiconductors. ....	42
Figure 3.10. Energy band diagram at (a) a source-contact interface and (b) a drain-contact interface.....	43
Figure 3.11. Energy band diagram at metal-p-channel semiconductor interfaces when hole carriers are injected by tunneling.....	44
Figure 3.12. Alignment of Fermi level energy, $E_F$ at the metal-semiconductor interface: (a) before $E_F$ is pinned, (b) when $E_F$ start to be pinned, and (c) after $E_F$ is pinned.....	46



Figure 3.13. Extraction of contact resistance, $R_C$ , from a plot of total resistance, $R_{TOT}$ , of transistors with various channel lengths. ....	49
Figure 3.14. Energy band diagram of $\text{Mo}(\text{tfd})_3$ and hole-transport organic-semiconductor materials. Adapted from [109]. ....	51
Figure 3.15. Energy band diagram of $\text{MoO}_3$ and hole-transport organic-semiconductor materials. Adapted from [102]. ....	52
Figure 3.16. Cross-sectional view of top-gate TIPS-pentacene/PTAA OFETs with (a) bare Au, (b) Au/PFBT, (c) Au/ $\text{Mo}(\text{tfd})_3$ , and (d) Au/ $\text{MoO}_3$ electrodes. ....	53
Figure 3.17. A comparison of work function values of bare Au (24 dev.), Au/PFBT (6 dev.), Au/ $\text{Mo}(\text{tfd})_3$ (11 dev.), and Au/ $\text{MoO}_3$ (11 dev.) from a total of 14 batches. ....	54
Figure 3.18. Histograms of the work function values measured on (a) bare Au, (b) Au/PFBT, (c) Au/ $\text{Mo}(\text{tfd})_3$ , and (d) Au/ $\text{MoO}_3$ electrodes. ....	55
Figure 3.19. Work function shifts as a function of exposure to air. ....	56
Figure 3.20. X-ray photoelectron spectroscopy data of (a) Fluorine and (b) Molybdenum measured from a $\text{Mo}(\text{tfd})_3$ film on electrodes. ....	57
Figure 3.21. Work function values of Au/ $\text{Mo}(\text{tfd})_3$ before and after spin-coating tetralin on top of the electrodes. ....	57
Figure 3.22. Depth profile of silicon, gold, and fluorine in a TIPS-pentacene/PTAA film on Au/ $\text{Mo}(\text{tfd})_3$ measured by XPS. ....	58
Figure 3.23. $I$ - $V$ transfer characteristics measured from top-gate TIPS-pentacene/PTAA OFETs with (a) bare Au, (b) Au/PFBT, (c) Au/ $\text{Mo}(\text{tfd})_3$ , and (d) Au/ $\text{MoO}_3$ electrodes. ....	59
Figure 3.24. Statistics of (a) threshold voltages, (b) field-effect mobility values, and (c) width-normalized off-current of TIPS-pentacene/PTAA OFETs with the four different types of source/drain electrodes. ....	60
Figure 3.25. Histograms of $V_{TH}$ values of top-gate TIPS-pentacene/PTAA OFETs with (a) bare Au, (b) Au/PFBT, (c) Au/ $\text{Mo}(\text{tfd})_3$ , and (d) Au/ $\text{MoO}_3$ electrodes. ....	61
Figure 3.26. Dependence of field-effect mobility values on the channel length. ....	62
Figure 3.27. Comparison of output characteristics of OFETs at $V_G = -6$ V. ....	62
Figure 3.28. Width-normalized contact resistance of OFETs having bare Au, Au/PFBT, Au/ $\text{Mo}(\text{tfd})_3$ , and Au/ $\text{MoO}_3$ electrodes. ....	63

Figure 3.29 Width-normalized contact resistance with respect to the work function values of source/drain electrodes at (a) $V_G = -4$ V, (b) $V_G = -6$ V, and (c) $V_G = -8$ V. ....	64
Figure 3.30. Dependence of TIPS-pentacene/PTAA work function on substrate work function measured by a Kelvin probe in a N <sub>2</sub> -filled glove box. ....	65
Figure 3.31. Device structures (inset figures) and the measured resistance values of thin-film resistors consisting of (a) a pristine, (b) Mo(tfd) <sub>3</sub> -doped, and (c) MoO <sub>3</sub> -doped TIPS-pentacene/PTAA films as a function of their length.....	67
Figure 3.32. (a) Cross-sectional view of a series-connected capacitor between gate and source/drain electrodes in the top-gate OFETs, and (b) calculated conductivity of the semiconductor films on contacts as a function of an applied signal frequency.....	70
Figure 3.33. Device modeling for HSPICE simulation assuming the injection diode at contacts, $D_{INJ}$ , is equally negligible for all cases, (a) cross-sectional view of on-resistance and (b) top view of device; and simulation results, (c) the distributed model of bulk resistance used in the simulation. ....	71
Figure 3.34. (a) The distribution of bulk resistance and (b) simulated bulk resistance values of the OFETs with four different source/drain electrodes. ....	72
Figure 3.35. Comparison of film thickness of TIPS-pentacene/PTAA on electrodes (measured by a confocal microscope).....	73
Figure 3.36. TIPS-pentacene/PTAA film morphologies on (a) Au/PFBT, (b) Au/Mo(tfd) <sub>3</sub> , and (c) Au/MoO <sub>3</sub> .....	74
Figure 3.37. $I$ - $V$ Transfer characteristics of top-gate TIPS-pentacene/PTAA OFETs with (a) bare silver and (b) bare aluminum source/drain electrodes. ....	75
Figure 3.38. Work function changes of silver and aluminum with a PFBT treatment and contact-doping.....	75
Figure 3.39 The transfer characteristics of the top-gate OFETs with (a) PFBT-treated silver, (b) Mo(tfd) <sub>3</sub> -doped silver, and (c) MoO <sub>3</sub> -doped silver for source/drain electrodes .....	76
Figure 3.40. Width-normalized contact resistance, $R_cW$ , of top-gate TIPS-pentacene/PTAA OFETs with PFBT-tread silver electrodes. ....	77
Figure 3.41. $I$ - $V$ transfer characteristics of top-gate TIPS-pentacene/PTAA OFETs with Mo(tfd) <sub>3</sub> -doped aluminum electrodes. ....	77

Figure 4.1. Schematic diagram of reverse stamping process and the final cross-sectional view of the device and circuits. Adapted from [155] by Choi <i>et al.</i> .....	82
Figure 4.2. (a) Optical properties and thickness values of TIPS-pentacene/PTAA films with bilayer gate dielectrics (b) before reverse stamping and (c) after reverse stamping. Adapted from [155] by Choi <i>et al.</i> .....	84
Figure 4.3. (a) Surface profile of an evaporated-pentacene/CYOTP/Al <sub>2</sub> O <sub>3</sub> structure, and (b) microscope images (top-view) of the sample before and after reverse stamping. Adapted from [155] by Choi <i>et al.</i> .....	85
Figure 4.4. Electrical characteristics of via-holes made by reverse stamping: (a) current-voltage characteristics of a 500 μm × 500 μm film area, and (b) measured conductance as a function of patterned via-hole size. Adapted from [155] by Choi <i>et al.</i> .....	86
Figure 4.5. (a) Schematic diagram of a pseudo-complementary inverter circuit, and (b) its transfer characteristics measured from a fabricated sample with the top-gate OFETs (inset figure is the photograph of a fabricated sample).....	87
Figure 4.6. (a) Photograph of the fabricated ring oscillator sample, (b) an output signal waveform captured from an oscilloscope, and (c) the measured oscillation frequency of the circuits with respect to the simulated value. Adapted from [155] by Choi <i>et al.</i> .....	88
Figure 4.7. (a) Block diagram of the designed 2-to-4 decoder circuit, (b) its driving peripheral setup on a perforated circuit board, and (c) the truth table of the circuit with the photograph of controlled LEDs according to the 2-bit input codes. Adapted from [155] by Choi <i>et al.</i> .....	89
Figure 4.8. The transfer characteristics of the top-gate OFETs on (a) PES substrates (adapted from [61]) and (b) CNC substrates (adapted from [65])......	92
Figure 4.9. Electrical characteristics of top-gate OFETs fabricated directly on SMPs: (a) I-V transfer characteristics; and a comparison of (b) $V_{TH}$ values, and (c) field-effect mobility values between the OFETs on glass and SMP substrates. ....	93
Figure 4.10. Transfer characteristics of an OFET with CYTOP/Al <sub>2</sub> O <sub>3</sub> bilayer gate dielectrics on SMP substrates after reshaping with a bending radius of 30 mm. ....	94
Figure 4.11. Cross-sectional view of the modified device geometry for top-gate OFETs on SMPs.....	95

Figure 4.12. $I$ - $V$ transfer characteristics of top-gate OFETs with CYTOP/nanolaminate bilayer gate dielectrics, a PVP buffer layer, and Mo(tfd) <sub>3</sub> -doped source/drain electrodes. ....	96
Figure 4.13. $I$ - $V$ transfer characteristics of top-gate OFETs before and after bending the device at room temperature with a bending radius, $r$ , of 7 mm. ....	96
Figure 4.14. (a) Illustration of bending orientation of SMP substrates with respect to the channel of the OFETs, and the $I$ - $V$ transfer characteristics of the OFETs on SMPs before reshaping, after reshaping the substrate with a bending radius of 7 mm, 14 mm, and 20 mm when the bending orientation is (b) parallel and (b) perpendicular to the channel of the OFETs ( $r$ : bending radius). ....	97
Figure 4.15. Extracted electrical parameters of the OFETs on SMPs with respect to substrate conditions: (a) threshold voltages and (b) normalized field-effect mobility values. ....	98
Figure 4.16. Captured microscope images of the OFETs on SMPs after reshaping: (a) parallel bending to the channel, and (b) perpendicular bending to the channel. ....	99
Figure 4.17. (a) Transfer characteristics of a pseudo-complementary inverter circuit comprises the top-gate OFETs with the modified device geometry in various substrate conditions, and (b) a photograph of the reshaped inverter circuit sample. ....	99
Figure 4.18. Layout design of the pseudo-complementary inverter circuit. ....	100

## List of Symbols and Abbreviations

OFET	Organic field-effect transistors
a-Si TFT	Amorphous silicon thin-film transistors
p-Si TFT	Poly-crystalline silicon thin-film transistors
HOMO	Highest occupied molecular orbital
LUMO	Lowest unoccupied molecular orbital
IE	Ionization energy
EA	Electron affinity
VB	Valence band
CB	Conduction band
CVD	Chemical vapor deposition
PVD	Physical vapor deposition
OLED	Organic light-emitting diodes
OPV	Organic photovoltaics
LCD	Liquid crystal displays
AMOLED	Active matrix OLED
EPD	Electrophoretic display
PCDTPT	Poly[4-(4,4-dihexadecyl-4H-cyclopenta[1,2-b:5,4-b'] dithiophen-2-yl)- <i>alt</i> - [1,2,5] thiadiazolo[3,4-c]pyridine]
SAM	Self-assembled monolayers
Mo(tfd) <sub>3</sub>	Molybdenum tris-[1,2-bis(trifluoromethyl)ethane-1,2-dithiolene]
PET	Poly(ethylene terephthalate)
PEN	Poly(ethylene naphthalate)
PES	Poly(ethersulfone)
SMP	Shape-memory polymer
DNTT	Dinaphtho[2,3- <i>b</i> :2',3'- <i>f</i> ]thieno[3,2- <i>b</i> ]thiophene
PFBT	Pentafluorobenzenethiol
TIPS	Triisopropylsilylethynyl
PTAA	Poly(triarylamine)
CNC	Cellulose nanocrystal
PVP	Poly-4-vinylphenol
TCMDA	Tricyclodecane dimethanol diacrylate
TATATO	1,3,5-triallyl-1,3,5-triazine-2,4,6(1 <i>H</i> ,3 <i>H</i> ,5 <i>H</i> )-trione
DMPA	2,2-dimethoxy-2-phenyl acetophenone
TMTMP	Trimethylolpropane tris(3-mercaptopropionate)
PDMS	Poly(dimethylsiloxane)

## Summary

In recent years, the performance of organic field-effect transistors has significantly improved in terms of their field-effect mobility and threshold voltage as well as their operational/environmental stability. As the current driving capability becomes higher, parasitic contact resistance at the metal-semiconductor interface starts to limit the performance of OFETs. Therefore, low contact resistance in OFETs is one of the key elements realizing high performance OFETs with ideal field-effect transistor characteristics. In addition, fabrication methods that connect transistors on a flexible substrate at room temperature is essential technology in the realization of flexible electronic devices. The traditional micro-fabrication methods are not suitable for use in the fabrication of OFETs because of high process temperatures over 500 °C, and chemical/mechanical damages to organic materials during the process. These methods also compromise the advantages of OFETs, which is low-cost fabrication on a large-area substrate.

In this dissertation, high-performance top-gate organic field-effect transistors comprising a TIPS-pentacene/PTAA film and a CYTOP/metal-oxide bilayer were developed on flexible, shape-memory polymer substrates. In detail, the performance of the top-gate OFETs was improved remarkably by lowering the contact resistance at the metal-semiconductor interface employing a contact-doping method. The fabricated top-gate OFETs presented lowest contact resistance value in TIPS-pentacene-based OFETs ever reported in literature. The OFETs having low contact resistance were used as a backplane of OFET circuits combined with a newly developed patterning method of a CYTOP/metal-

oxide gate dielectric layer, reverse stamping. Finally, high performance top-gate OFET circuits on a shape-memory polymer substrate were first demonstrated based on this dissertation work.

## **CHAPTER 1 Introduction**

The objective of this Ph.D. research is to develop low-cost fabrication methods for organic field-effect transistors (OFETs) and their circuits that have high performance as well as high stability in their operation, particularly on flexible or deformable substrates for electronics with a three-dimensional form factor. This chapter provides a background of the necessity for thin-film transistors (TFTs), particularly, that of organic thin-film transistors, and explains the fundamentals of organic semiconductors with respect to silicon semiconductors. Next, the geometries and operational properties of organic field-effect transistors are reviewed followed by the progress in the improvement of their electrical properties and the approaches using OFETs in circuits and systems. Finally, the objectives and the organization of the research dissertation are specified.

### **1.1. Thin-film transistors**

A thin-film transistor can be defined as a field-effect transistor built on a substrate by depositing an active semiconducting layer [1, 2]. The development of thin-film transistors has been initiated and accelerated by the needs for a backplane technology from the display industry, which have migrated from cathode ray tubes (CRTs) to liquid crystal displays (LCDs) in favor of large-size, thin, and light-weight displays. The revenue of the world-wide display market has been drastically growing, from \$26 billion dollars in 1998 to \$100 billion in 2007 [3, 4], and a projection suggests the estimated revenue in 2020 as \$156 billion [5]. Together with the blooming of display industry, the use of thin-film transistors for in-pixel circuits implementing active-matrix addressing or driving methods for LCDs has driven the evolution of thin-film transistor technologies [2, 6].



Unlike single-crystalline silicon transistors whose substrate size is limited by the size of a silicon wafer up to a diameter of 450 mm, thin-film transistors have been fabricated on a large substrate, such as 10<sup>th</sup> generation glass substrates, which have an area of 2,850 x 3,150 mm<sup>2</sup> [6], leading to a commercialization of 120-inch diagonal LCD panels in 2015 [7].

In addition to the adaption of TFTs in display devices, the emerging of wearable electronics also fuels the development of thin-film transistors, as wearable devices require not only large-area in their size but also high flexibility in their mechanical properties for 3D-shape applications. The market size of wearable electronics is expected to jump up from \$1.4 billion in 2013 to \$19 billion in 2018 [8]. Responding to the needs of flexible devices for wearable applications, substantial research and development have been performed for new materials, fabrication methods in the search for new applications in thin-film transistor technology [9].

Table 1.1. Field-effect mobility values of thin-film transistors [10].

	a-Si transistors	p-Si transistors	Metal-oxide transistors	Organic transistors
Field-effect mobility value [cm <sup>2</sup> /Vs]	< 1	50 - 100	1 - 100	0.1 - 10

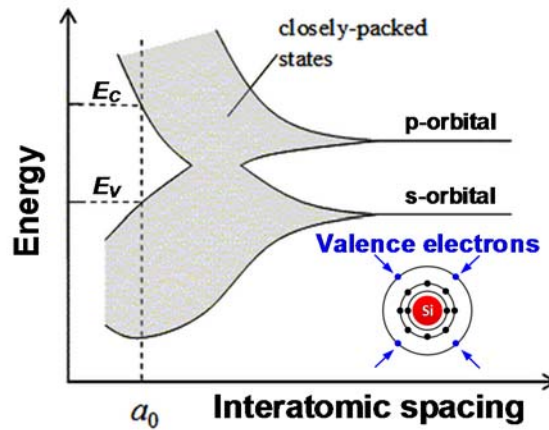
There are four major thin-film transistor technologies that have been intensively developed: amorphous silicon (a-Si) transistors, polycrystalline silicon (p-Si) transistors, metal-oxide transistors, and organic transistors. The a-Si thin-film transistors have been widely used in the display panel industry, especially for liquid crystal displays (LCDs), and currently the largest glass substrate, the 10<sup>th</sup> generation glass substrate, is used for the

fabrication of the a-Si transistors. On the other hand, recently, p-Si transistors have been developed more intensively because of the increasing demand for high pixel-density display panels, such as display panels having their pixel density over 300 pixels per inch (PPI), requiring a high field-effect mobility of the driving transistors in pixels, and active-matrix organic light-emitting diode (AMOLED) displays, which also require both high current driving capability and high operational stability of transistors. Table 1.1 shows the field-effect mobility values of thin-film transistors [10]. Amorphous metal-oxide semiconductors, such as zinc oxide (ZnO), indium-zinc oxide (IZO), and indium-gallium-zinc oxide (IGZO), are emerging semiconducting materials for thin-film transistors that exhibit high electron mobility values ( $> 10 \text{ cm}^2/\text{Vs}$ ) [11, 12], and since the demonstration by Nomura *et al.* of flexible amorphous IGZO thin-film transistors in 2004 [12], many research scientists have been intensively developing amorphous metal-oxide transistors. One of the advantages of metal-oxide transistors is in their fabrication compatibility with the existing a-Si transistors fabrication process, and utilizing those advantages, high field-effect mobility values and a compatibility in the fabrication process, large-size AMOLED displays have already been developed using metal-oxide transistors by Jeong *et al.* [13]. An organic field-effect transistor technology is also emerging for large-area, low-cost flexible electronics. Organic field-effect transistors have shown field-effect mobility values between a-Si transistors and metal-oxide transistors, that is, the advantages of organic transistors over metal-oxide transistors is not on superior field-effect mobility values; instead, the low temperature fabrication accompanying various solution processing methods and the high mechanical flexibility of the OFETs are distinguishing features of this technology [14, 15]. Thanks to the flexibility of OFETs, they have been applied to a

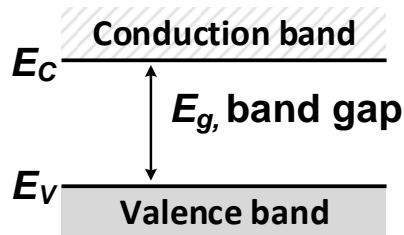
backplane for flexible electronic-paper (e-paper) displays [16], and other applications that need extreme bending stability below a 1 mm-bending radius [17].

## 1.2. Organic field-effect transistors

### 1.2.1. Silicon semiconductors



(a)



(b)

Figure 1.1. (a) Conceptual illustration of the formation of the energy band in crystalline silicon (inset figure: simplified schematic of an isolated silicon atom), and (b) the energy band diagram of crystalline silicon.

The semiconducting property of crystalline silicon is attributed to four valence electrons that are weakly bound to the nucleus in silicon atoms and strongly participate in chemical reactions, while the other ten electrons occupy very deep-lying energy levels and are strongly bound to the nucleus as illustrated in the inset of Figure 1.1. The four weakly

bound electrons can be easily excited by thermal energy and can be free electrons leaving unoccupied states in the silicon atom, therefore changing the electrical conductivity of the material.

When it comes to solid-state crystalline silicon with a particular lattice constant, or distance, by interatomic forces and progressive spread in the allowed energy states, those states form energy bands, known as a conduction band, *CB*, and a valence band, *VB*, with an intervening energy gap, a band gap as shown in Figure 1.1 [18]. The electrons in the valence band are excited by external energy that is large enough to overcome a band gap, move to the conduction band, and become free electrons that increase the conductivity of the crystalline silicon.

### **1.2.2. Organic semiconductors**

Organic semiconductors are made of organic materials that mostly consist of carbon, hydrogen, and oxygen. When carbon atoms, which have four valence orbitals,  $2s$ ,  $2p_x$ ,  $2p_y$ , and  $2p_z$ , covalent-bond with three nearby atoms making a double bond with another carbon atom, it undergoes hybridization of valence orbitals and creates  $sp^2$  hybridized orbitals with  $2s$ ,  $2p_x$  and  $2p_y$  orbitals, and unhybridized  $p_z$  orbitals perpendicular to the plain containing the hybridized  $sp^2$  orbitals, as shown in Figure 1.2. While the hybridized  $sp^2$  orbitals create a strong  $\sigma$ -bond with other atoms, unhybridized  $p_z$  orbitals make a weak  $\pi$ -bond with neighboring carbon atoms.

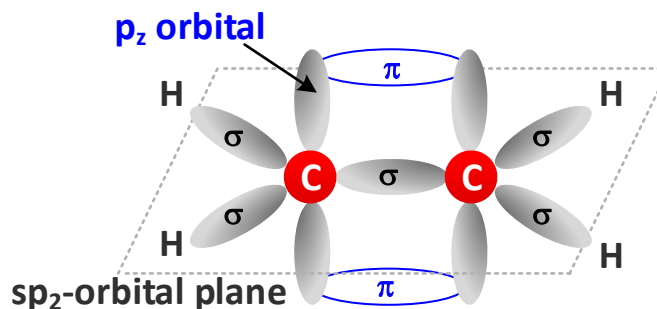


Figure 1.2 The schematic of the orbitals and bonds for two  $sp_2$  hybridized carbon atoms.

The two orbitals that create  $\pi$ -bond split into two different molecular orbitals, a bonding molecular orbital,  $\pi$ , which has lower energy level than the original atomic orbital, and an anti-bonding molecular orbital,  $\pi^*$ , which has higher energy level than the original atomic orbital. When the organic system is composed of several  $\pi$ -bonded carbon atoms as illustrated in Figure 1.3(a), the system creates multiple levels of bonding and anti-bonding molecular orbitals, and the bonding orbital that has the highest energy level in the system is called the highest occupied molecular orbital, HOMO, and the anti-bonding orbital that has the lowest energy level a lowest unoccupied molecular orbital, LUMO. When the molecules are densely packed and form a solid film, the bonding and anti-bonding molecular orbitals generate continuous bands, called HOMO and LUMO bands as displayed in Figure 1.3(b), similar to the energy band diagram of crystalline-silicon semiconductors. The energy level of the bottom of a LUMO band is defined as electron affinity (EA), which is the amount of energy released by adding an electron, and the top of a HOMO band as ionization energy (IE), which is the minimum amount of energy required to remove an electron from the solid film.

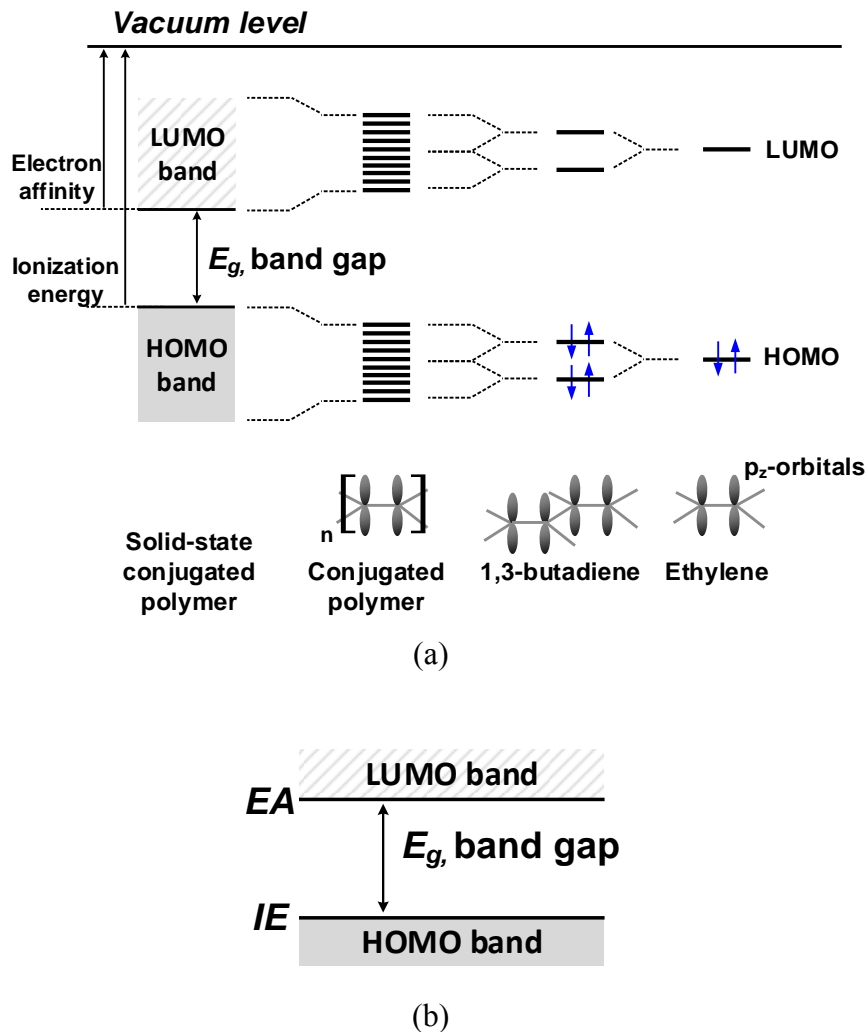


Figure 1.3 (a) Formation of LUMO and HOMO bands in organic molecules and in organic films (adapted from [19]), and (b) the energy band diagram of organic semiconductors in a solid film.

The  $\pi$ -electrons in HOMO band can be easily excited by external stimuli such as heat, move up to the LUMO band, and provide semiconducting properties in the organic material.

### 1.2.3. Comparisons between organic and inorganic semiconductors

The traditional inorganic semiconductors that have fixed energy levels of a valence band and a conduction band based on their crystalline system, IE and the EA of organic systems, can be engineered to preferred values. Therefore, the engineering of the energy

level of the bands has been one of the biggest workhorses of the implementation of high performance organic semiconductors [15]. Another difference between silicon and organic semiconductors is in defining the type of semiconductors, p- or n-channel semiconductors. The intrinsic crystalline silicon has the same number of electrons and holes in the bulk that is thermally created, so the majority carrier and the type of silicon semiconductors is determined by the concentration of dopants, such as donors for n-types and acceptors for p-types, and the associated Fermi level energy of the bulk as shown in Figure 1.4(a). On the other hand, the type of organic semiconductors is defined, in general, by the energy barrier height,  $\phi_b$ , for electrons and holes at the metal-semiconductor interfaces, which is illustrated in Figure 1.4(b) and (c) [20] : when the barrier height for holes to be injected from electrodes or to be collected by electrodes is low, the organic system becomes a p-channel device; in the same manner, a low barrier height for electrons leads to an n-channel device.

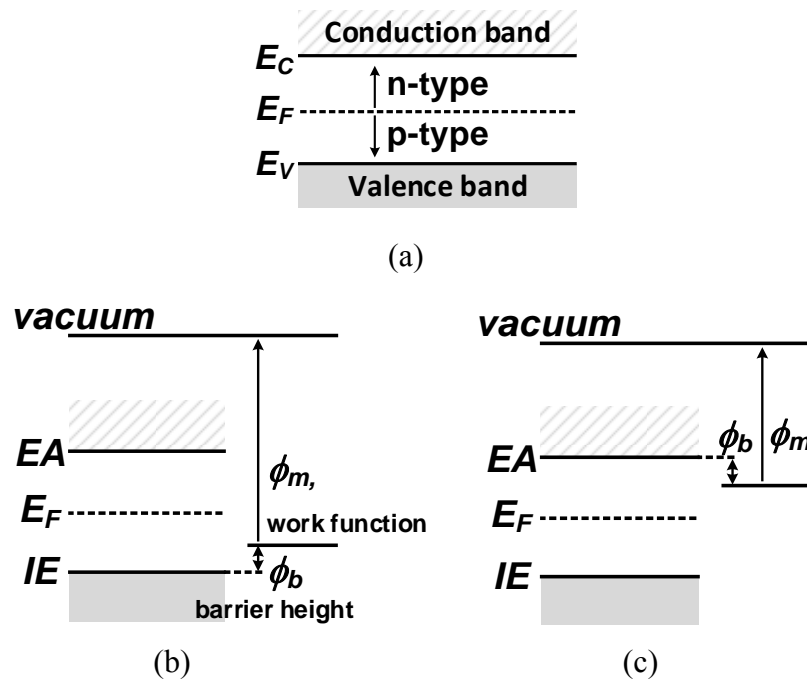


Figure 1.4. Energy band diagram of (a) n- and p-type silicon semiconductors (b) p-channel, and (c) n-channel organic semiconductors.

The difference between silicon semiconductors and organic semiconductors is also in the fabrication process and associated substrate materials. The silicon crystalline transistors are fabricated through multiple vacuum-based process steps, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), thermal oxidation/annealing, photolithography, and wet/dry etching; most of the fabrication methods need a processing temperature higher than 500 °C and the use of harsh chemicals that degrade the electrical characteristics of organic semiconductors upon exposure. Organic semiconductors can also be fabricated by conventional microelectronics technologies, although many limitations exist because of the nature of organic semiconductor materials, such as a low glass transition temperature below 200 °C in general [21] and a high sensitivity to exposure to oxygen and moisture [22]. On the other hand, organic semiconductors can also be fabricated by low-cost, non-vacuum processing methods, such as transfer laminating, spin-coating, and nozzle/inkjet printing at room temperature, and those low-temperature processing methods provide a potential for low-cost fabrication of electronic devices on flexible/large substrates through their simplified processing steps and reduced materials waste [23]. For these reasons, many research scientists have developed low-cost solution-processing methods with organic semiconductors, including the development of solution-processable semiconductor materials, electrodes, and dielectrics as well as low-temperature patterning methods [24-26].

#### **1.2.4. Device geometry of organic field-effect transistors**

Organic field-effect transistors can have four different geometries: bottom-gate bottom-contact, bottom-gate top-contact, top-gate bottom-contact, and top-gate top-contact as shown in Figure 1.5. The bottom-gate structure employs gate electrodes placed on the



bottom of the semiconductor film, and the semiconductor deposition is the last or second last step in the fabrication, which can minimize any impacts on the semiconductor film from following processing steps. This bottom-gate geometry is widely used in investigating the performance of newly developed organic semiconductor materials on highly n-doped silicon wafers, since the silicon wafer and the thermally grown SiO<sub>2</sub> on the surface of the wafer can be used as gate electrodes and gate dielectrics, respectively, in the device structure reducing the number of steps needed for fabricating the transistors and providing a high quality gate dielectric layer [27-29].

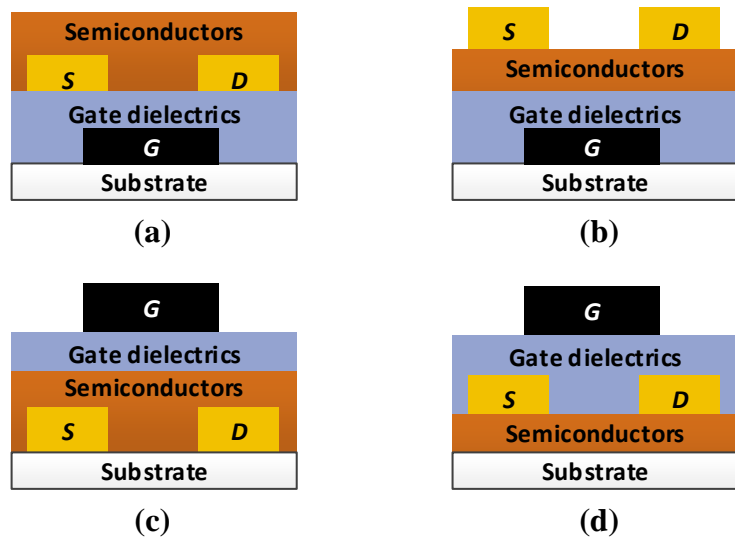


Figure 1.5 cross-sectional views of device geometry for (a) bottom-gate bottom-contact, (b) bottom-gate top-contact, (c) top-gate bottom-contact, and (d) top-gate top-contact OFETs.

The top-gate structures, on the other hand, have gate dielectrics and gate electrodes located on top of the semiconductor film as shown in Figure 1.5(c) and (d). This top-gate geometry generally requires more process steps for dielectrics and electrodes in the fabrication than the bottom-gate one, and has more challenges in the fabrication, such as the deposition of high quality gate dielectrics without damaging the organic materials underneath and a chance of damaging the organic semiconductor layer already deposited

on the substrate. However, once the structure is successfully built, the gate dielectrics and the gate electrodes provide better protection for the semiconductor film against oxygen and moisture than those of the bottom-gate structure.

### 1.2.5. Device operation of p-channel OFETs

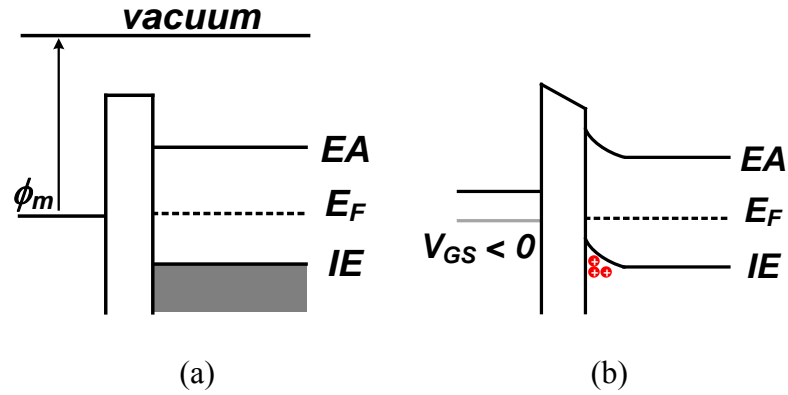


Figure 1.6. Energy level band diagram of an ideal MIS structure at (a) an equilibrium condition and (b) an accumulated condition by a negative gate-voltage bias in p-channel organic semiconductors.

The basic electrical characteristics of OFETs is based on the metal-insulator-semiconductor (MIS) structure, which comprise an insulating layer between metal electrodes and semiconductor films. Providing that the insulator is not conducting, and the Fermi level energy of the electrode,  $\phi_m$ , and the semiconductor are aligned, the energy band diagram of the MIS structure with p-channel organic semiconductors in an equilibrium condition is shown in Figure 1.6(a). Once the negative gate bias is applied to the electrode as shown in Figure 1.6(b), positively charged carriers are accumulated at the interface between the insulator and the semiconductor, inducing a thin conductive layer in the semiconductor film, called a channel. The conductance of the channel is modulated by the electric field across the insulator; that is, the stronger the electric field by either a higher gate-voltage bias or a higher capacitance density of the MIS structure, the higher the

conductance of the channel to be obtained in the structure. In other words, the OFETs based on MIS structures are operating in an accumulation region while silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) are operating in an inversion region using minority carriers of semiconductors as dominant charge carriers in operation of the device [30].

Thin-film transistors, including OFETs, entail three terminals in general: gate ( $G$ ), source ( $S$ ), and drain ( $D$ ) electrodes as shown in Figure 1.5. Figure 1.7 illustrates the top-gate bottom-contact device geometry with a symbol of p-channel transistors. Source electrodes are defined as the electrodes that have higher potential/voltage than that between two electrodes that are directly in contact with the semiconductor even though the two electrodes are physically identical. In the structure, gate electrodes, gate dielectrics, and semiconductor films form the MIS structure that is described above. Once a channel is induced, the OFET provides a conducting current path from source electrodes to drain electrodes through the channel, and the electric current is called drain current,  $I_D$ , in that way,  $I_D$  is modulated by the gate voltage bias.

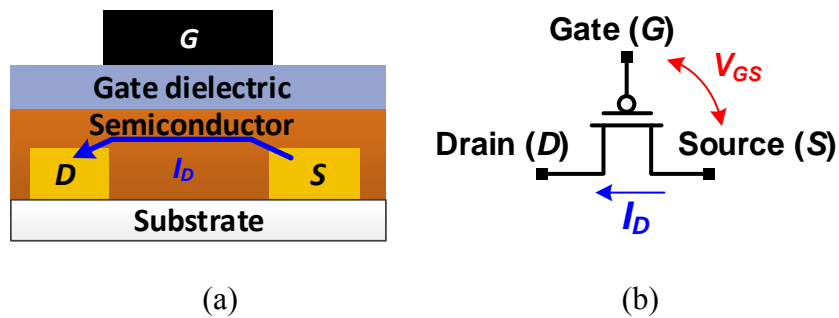


Figure 1.7 (a) A device geometry and (b) symbols of p-channel, top-gate bottom-contact OFETs.

The channel induced by a gate voltage bias is uniformly distributed under gate electrodes when the potential of source electrodes,  $V_S$  and the drain electrodes,  $V_D$  are equal, and associated with the channel; any potential difference between source and drain electrodes induce a drain current. However, once the potential difference between source and drain electrodes,  $V_{DS}$ , increases, the voltage drop across the channel associated with the drain current starts to negate the inverting effect of the gate bias [18]. As the electric field between gate and drain electrodes decreases, the thickness of the channel region in the vicinity of the drain electrode starts to decrease, and eventually, the accumulated charge carriers are depleted, which is referred to as pinch-off. In the current-voltage ( $I$ - $V$ ) characteristics of OFETs, the regime before pinch-off occurs is defined as the linear regime, and after pinch-off since  $I_D$ , which linearly increases before pinch-off, levels out after pinch-off regardless of the increase of the voltage difference between source and drain electrodes.

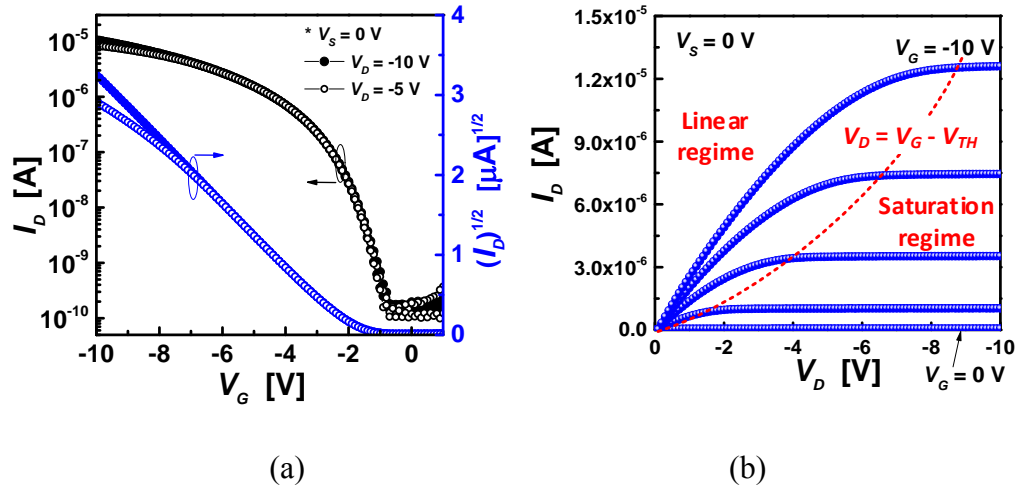


Figure 1.8. Typical  $I$ - $V$  characteristics of p-channel OFETs: (a) transfer characteristics and (b) output characteristics.

The electrical behavior of OFETs has mostly been explained based on the model of traditional inorganic MOSFETs, and the device parameters have also been extracted by the drain current equations of MOSFETs. In a linear regime of  $I$ - $V$  characteristics of p-channel OFETs, in which  $V_{SD} \leq V_{SG} - |V_{TH}|$ , the drain current is described as Equation (1.1):

$$I_{SD} = \frac{W}{L} C_{OX} \mu \left[ (V_{SG} - |V_{TH}|) V_{SD} - \frac{(V_{SD})^2}{2} \right] \quad (1.1)$$

In a saturation regime, in which  $V_{SD} > V_{SG} - |V_{TH}|$ ,  $I_D$  follows equation (1.2):

$$I_{SD} = \frac{1}{2} \frac{W}{L} C_{OX} \mu (V_{SG} - |V_{TH}|)^2 \quad (1.2)$$

where  $W$ ,  $L$ ,  $\mu$ ,  $C_{OX}$ , and  $V_{TH}$  are the channel width, the channel length, the field-effect mobility value, the threshold voltage, and the capacitance density of gate insulators, respectively. Figure 1.8 displays typical  $I_D$ - $V_G$  characteristics, which is referred as transfer characteristics, and  $I_D$ - $V_D$  characteristics, which is referred as output characteristics.

This model assumes that the field-effect mobility values are independent of the gate voltage bias and the geometrical channel length of the OFETs, that is, the channel length modulation, which occurs when the reduction of the effective channel length by pinch-off is comparable to the geometrical channel length, is not accounted for the above equations, and the parasitic contact resistance at the contacts between source/drain metal electrodes and semiconductor films is also ignored.

### 1.2.6. Extraction of electrical parameters of OFETs

The field-effect mobility, which is one of the important electrical parameters being used for evaluating a performance of field-effect transistors, is extracted from the transfer characteristics of OFETs. The square root of  $I_D$  in Equation (1.2) is derived as Equation (1.3):

$$\sqrt{I_D} = \sqrt{\frac{1}{2}\mu C_{OX} \frac{W}{L} (V_G - V_{TH})} \quad (1.3)$$

and the square root of  $I_D$ ,  $\sqrt{I_D}$ , has a linear relationship with  $V_G$  with a slope,  $\frac{\partial\sqrt{I_D}}{\partial V_G}$ , providing that the transfer characteristics are measured in the saturation regime. Once the slope is extracted by linear-fitting  $\sqrt{I_D}$  as displayed in Figure 1.9, because values of all other variables ( $\mu$ ,  $C_{OX}$ ,  $W$ , and  $L$ ) are already known, the field-effect mobility,  $\mu$ , can be calculated as shown in Equation (1.4):

$$\mu = \frac{2L}{W} \frac{1}{C_{OX}} \left( \frac{\partial\sqrt{I_D}}{\partial V_G} \right)^2 \quad (1.4)$$

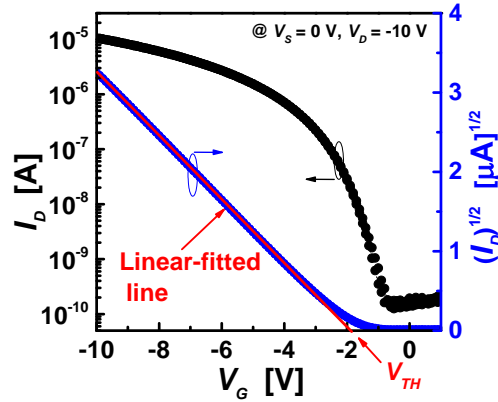


Figure 1.9. Fitting from the slope of the straight line.

In the same manner, the threshold voltage of OFETs is extracted as the intersection of the linear-fitted line with a  $V_G$  axis based on Equation (1.3). Keeping this in mind, it is important to note that all the models and derivations assume that the parasitic contact resistance is negligible and the OFETs are in good compliance with the square law of field-effect transistors.

### **1.2.7. Current and potential applications**

Intensive research has led to the start of the commercialization of organic semiconductor devices including organic light-emitting diodes (OLEDs) that emit light; organic field-effect transistors (OFETs) that operate as switches and amplifiers in circuits; and organic photovoltaics (OPVs) that harvest energy from sunlight. In particular, OLEDs are the leading organic semiconductor device among all, in terms of a commercialization replacing liquid-crystal displays (LCDs) in the flat-panel display market. Now, OLED products can be found everywhere in electronic devices, such as cell phones, cameras, and TVs. Organic transistors have been adapted for a backplane technology of electronic paper (e-paper) displays mimicking traditional flexible paper. For example, Plastic Logics in Germany has developed an electrophoretic display (EPD) on organic transistor backplanes [31]. Organic photovoltaics, or organic solar cells have also been intensively developed as a light-weight, low-cost energy harvesting device, and the energy conversion efficiency of a single OPV cell made in laboratories is getting closer to that of inorganic solar cells [32-34]. Therefore, even though the market for organic electronics is not yet completely open except for OLEDs, the demand for organic electronics is continuously growing

## **1.3. Recent progress in OFETs**

### **1.3.1. Performance improvement in organic field-effect transistors**

The small threshold voltages of field-effect transistors are preferred for low-power consumption and the high performance at a given voltage bias condition. The operating voltages of OFETs in early stage were around 100 V [35] but intensive research has been done in reducing the threshold voltages of OFETs [36-38], and as a result, the threshold voltages found in many recent publications on OFETs are similar to or even smaller than

those of poly-Si TFTs whose threshold voltages are around -1 V for p-channel transistors, and the operating voltages of demonstrated inverter circuits dropped down to 3 V [38, 39]. For example, Hagen *et al.* developed one of the best practices in OFETs having low operating voltages using AlO<sub>x</sub> gate dielectrics combined with self-assembled monolayers (SAMs) as gate dielectrics, in 2007 [37]. The total thickness and the capacitance density of the gate dielectrics were 5.7 nm and 700 nF/cm<sup>2</sup> achieving 3 V of operating voltages in circuits, and implementing ring oscillators and analog-to-digital converters (ADCs) [38]. Zhang *et al.* also developed complementary inverter circuits operating with a 5 V power supply by adapting 200 nm-thick Al<sub>2</sub>O<sub>3</sub> which is atomic-layer deposited [40].

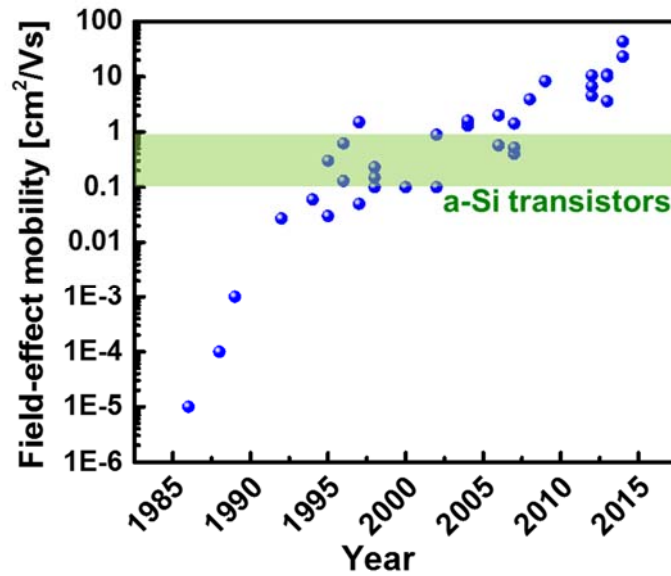


Figure 1.10. Progress in field-effect mobility values of organic field-effect transistors.

The increase of carrier mobility values in OFETs has also been an important and widely studied topic since the current driving capability under a limited footprint and voltage bias conditions determines the range of possible applications for transistors. For example, the in-pixel driving circuits in display panels require the field-effect mobility



values of their transistors to be around  $1 \text{ cm}^2/\text{Vs}$  or less for LCDs, which is the performance of amorphous silicon thin-film transistors (a-Si TFTs), and  $30 - 100 \text{ cm}^2/\text{Vs}$  for AMOLEDs, which are the mobility values of low temperature p-Si TFTs [10]. The mobility values of OFETs, as briefly summarized in Figure 1.10, have drastically increased recently due to the development of high performance organic materials [27, 41], blending polymers with small molecules [42, 43], aligning semiconductor molecules in the bulk of the films [44-46], and so on. The field-effect mobility values of OFETs have been reported up to around  $2 - 3.6 \text{ cm}^2/\text{Vs}$  [41, 47]. As the high mobility values have been extracted and reported with non-ideal transfer characteristics, the overestimation of the mobility values becomes another issue in the research on organic transistor technology [15, 47, 48].

### **1.3.2. Operational and environmental stabilities of organic field-effect transistors**

Together with the improvement in the electrical performance of OFETs, the operational and environmental stability of OFETs has also been enhanced remarkably. The operational stability of OFETs is known to relate to a dipolar orientation and trap sites in and between the semiconductors and the gate dielectrics [49-53]. This stability can be examined by the change or degradation of the electrical parameters of the OFETs, such as mobility values, threshold voltages, and the on- or off-current changes in operation. This environmental stability is also evaluated in a manner similar to the operational stability but with a major difference in terms of the environment for the operation, such as in ambient air with or without moisture and heat involved [54, 55], and in water [56, 57]. Although stability is one of the biggest challenges for OFETs, many recent reports exhibit drastic improvement in stability: Głowacki *et al.* developed highly air-stable organic semiconductors by using hydrogen-bonded organic molecules [54]; Hwang *et al.*

demonstrated top-gate OFETs that are stable in air by applying CYTOP/Al<sub>2</sub>O<sub>3</sub> bilayer dielectrics [55], which are later proved to be stable in water as well by Yun *et al.* [56]; and Kuribara *et al.* demonstrated the stable operation of bottom-gate OFETs when being sterilized in boiling water by encapsulating the OFETs with poly(chloro-para-xylylene), or parylene, and gold [57].

### 1.3.3. Substrates for organic field-effect transistors

The mechanical flexibility of organic materials is one of the biggest advantages of OFETs over traditional inorganic semiconductors [17]. As an effort in realizing the advantages of organic electronics on flexible substrates, various kinds of flexible substrates have been adapted instead of rigid glassy substrates, such as thin metal [58], poly(ethylene terephthalate) (PET) [59, 60], poly(ethylene naphthalate) (PEN) [36], polyethersulfone (PES) [61, 62], and polyimide foil [17, 63, 64]. In addition to the flexible substrates, OFETs have been fabricated on the emerging class of materials that are environment-friendly or deformable, such as cellulosic nanocrystals (CNCs) [65] and shape-memory polymers (SMPs) [66-68]. In particular, the shape-memory polymers show unique features such as a stimulus-controlled Young's modulus, low cure stresses, and biocompatibility. Because of the distinctive mechanical properties, the potential of SMPs as substrates for OFETs in three-dimensional electronic devices has been highlighted by many reports: Reeder *et al.* demonstrated the use of SMP substrates for biomedical applications by building high performance bottom-gate dinaphtho[2,3-*b*:2',3'-*f*]thieno[3,2-*b*]thiophene (DNTT) OFETs on SMPs and the same OFETs on polyimide being coated by SMPs [66]; Wang *et al.* showed self-wrapping organic electronics by attaching SMPs on a pre-fabricated device [69]; Liu *et al.* designed self-folding SMP sheets that transform into three-dimensional

shapes upon a proper stimulus [70]; and Lu *et al.* reported the nanopaper-combined SMPs for an electrical actuation [71].

#### **1.3.4. Integrated circuits and applications of organic field-effect transistors**

As the performance and the stability of individual OFETs have improved rapidly, many research results of the integration of OFETs into circuits have also increasingly been reported. Many of the reports focus on the possibility of using OFETs as a backplane of display panels [16, 31, 58, 63], and small size, highly integrated, low-cost electronics, such as a clocked sequential complementary circuit [72] and an 8-bit microprocessor [73]. In spite of the accomplishments in the remarkable integration of OFETs, many of them have still relied on the traditional micro-fabrication methods in depositing and patterning thin films in the device structure, such as an evaporation, a photolithography, and a lift-off, compromising the cost-effectiveness of organic semiconductors. Therefore, the integration of OFETs into circuits using non-traditional fabrication methods, such as spin-coating and printing, is a part of ongoing research [24, 25, 74-76].

In addition to patterning of organic semiconductor films, the low-cost patterning of gate dielectrics is another imperative part in the circuit integration because the vertical interconnection between top and bottom electrodes through via-holes is one of the essential components in circuits. To date, electrodes, gate dielectrics and semiconductors have been deposited by low-cost solution processing [74, 75, 77], patterned using emerging techniques such as soft-lithography [78], selective physical delamination [79, 80], and printing [75] while low-cost novel patterning method for gate dielectric layers making via-holes in organic transistors has been relatively less studied with few noticeable ideas: area-selectively printing solvent that dissolves a polymeric gate dielectric layer for via-holes

[25], depositing noble metals, such as gold, hindering the growth of inorganic gate dielectrics on a via-hole region [37], and directly patterning of polymeric dielectric films by printing [74].

#### **1.4. Objective and organization of the dissertation**

The primary objective of this dissertation research is to improve the electrical performance of top-gate OFETs by lowering the contact resistance using a contact-doping method. This research employs a high-performance PTAA-blended TIPS-pentacene as an active semiconducting layer with CYTOP/Al<sub>2</sub>O<sub>3</sub> bilayer gate dielectrics for low operating voltages and high operational/environmental stabilities. This dissertation reports drastically improved contact resistance of the top-gate OFETs with respect to the contact resistance of the OFETs with 2,3,4,5,6-Pentafluorothiophenol (PFBT) treated electrodes, which is widely used for a work function modification of source/drain electrodes in p-channel OFETs, and provides a systematic analysis of the mechanism in the contact-doping effects in the OFETs.

The second objective is to implement circuits on 3D-shape substrates, such as shape-memory polymers. By realizing OFET circuits on shape-memory polymers, this research shows that OFETs have high potential to be employed for 3D-shape applications, and can be adapted to wearable electronics as a backplane technology. As a part of the low-cost large-area fabrication of OFET circuits, a low-cost method for patterning gate dielectrics is also suggested and used for a circuit implementation.

According to the motivations and objectives outlined above, the organization of the dissertation is structured as follows: Chapter 1 introduces the basic background of thin-film transistor technologies, and the fundamentals of organic thin-film field-effect

transistors, including their geometrical structure, electrical properties, and recent progress. Chapter 2 describes the fabrication and characterization details of the OFETs used in this research. Chapter 3 presents the results of lowering contact resistance in top-gate OFETs by contact doping, and the analysis with respect to injection barrier engineering and bulk resistance change. Chapter 4 describes the development of top-gate OFET circuits on top of shape-memory polymer substrates. This chapter, first addresses realizing a low-cost patterning method of gate dielectrics for circuit implementation, and the procedure to develop OFET circuits, then report the electrical properties of top-gate OFETs and their circuits on SMPs when the substrates are flat and reshaped. Chapter 5 summarizes the conclusions drawn from this study and presents recommendations for future work.

## CHAPTER 2 Experimental Methods

This chapter describes details of a device fabrication and characterization setups of the OFETs employed in this dissertation. The fabrication methods of OFETs are divided into four parts: a deposition of metals and dopant materials, a PFBT treatment, solution processing of organic semiconductor films, and a deposition of bilayer gate dielectrics. Next, the fabrication of shape-memory polymers being used as a substrate of OFETs is described followed by the characterization methods of thin films. Lastly, the design flow of circuits using a circuit simulator and computer-aided design tools is introduced at the end of this chapter.

### 2.1. Device fabrication

In this dissertation research, the top-gate OFETs and their circuits are fabricated mostly on a glass substrate (Corning® Eagle2000™) although flexible substrates, such as PES (*i*-Components Co. Ltd.), CNC, and SMPs are also adapted in examining the performance of the OFETs on those flexible substrates. The glass and PES substrates were cleaned by sonication in acetone, deionized water, and isopropanol for five min each whereas CNC and SMP substrates were used as prepared without an additional cleaning process. Source/drain and gate electrodes were deposited by a thermal evaporator, and three different types of surface engineering (a PFBT treatment, Mo(tfd)<sub>3</sub>-doping, and MoO<sub>3</sub>-doping) were performed on the surface of the source/drain electrodes. The PTAA-blended TIPS-pentacene solution was spin-coated in a N<sub>2</sub>-filled glove box minimizing the chance of air exposure followed by a deposition of bilayer gate dielectrics, CYTOP/ALD-deposited metal-oxide. Lastly, gate electrodes were thermally evaporated on top of gate dielectrics with a shadow mask to pattern the electrodes.

### **2.1.1. Deposition of patterned metal electrodes and dopants**

The patterned electrodes and dopants for contact doping were deposited by a computer-controlled physical vacuum deposition (PVD) system, SPECTROS, that is designed to deposit both organic and inorganic materials, and manufactured by Kurt J. Lesker Company (KJLC). This deposition system is connected to a N<sub>2</sub>-filled glove box (MBRAUN) preventing the air exposure of samples before and after the deposition, since most organic materials degrade with air/oxygen/moisture exposure. In the evaporator chamber, the samples are fixed on a substrate holder with shadow masks which have patterns for transistor electrodes. The shadow masks are made of 0.12 mm-thick Molybdenum sheet (ASTM-B-386, Eagle Alloys Corp.), and cut by IR laser (Resonetics Corp.) which is operated at two different wavelengths (1047 nm or 524 nm) with a beam size at approximately 50 microns to micro-machine materials such as metals, permanent magnets, alumina, and silicon.

The thin films were deposited in the evaporator at a high vacuum condition with a base pressure  $<10^{-7}$  Torr. The substrate holder in the chamber is rotating during the deposition for enhanced uniformity of film thickness, and the deposition rates are monitored by a standard quartz crystal. The dopant materials, Mo(tfd)<sub>3</sub> and MoO<sub>3</sub>, were also deposited at SPECTROS on top of source/drain electrodes with the same shadow mask that is used for the electrodes.

### **2.1.2. Deposition of self-assembled monolayer of PFBT**

The self-assembled monolayer (SAM) on source/drain electrodes are known to improve the morphology of semiconductor films on top of the SAM-treated electrodes, and enhance OFET performances. In particular, 2,3,4,5,6-Pentafluorothiophenol (PFBT),

whose chemical structure is illustrated in Figure 2.1, has been widely used to treat the surface of electrodes in OFETs. The treatment forms a monolayer of PFBT on metal electrodes, such as gold and silver, by chemisorption as described in Figure 2.2, and improves the wetting properties of substrates, achieves highly ordered packing of organic molecules, and reduces the injection barrier height of hole carriers at the metal-p-channel semiconductor interfaces by creating dipoles and increasing the work function of electrodes at the interface [81-91]. In this dissertation, the OFETs with PFBT-treated gold electrodes were fabricated as a reference in the evaluation of the contact resistance of the OFETs with contact-doped electrodes.

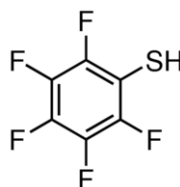


Figure 2.1. Chemical structure of 2,3,4,5,6-Pentafluorothiophenol (Sigma Aldrich).

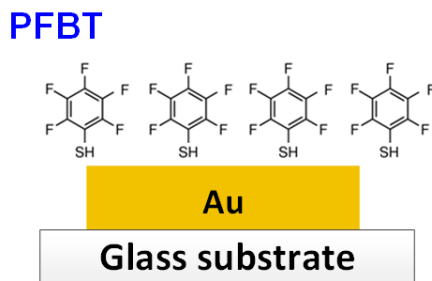


Figure 2.2. Formation of a self-assembled monolayer of PFBT on gold electrodes.

A PFBT treatment was performed with a 10 mM PFBT solution, which is made by adding 67  $\mu\text{L}$  of 97% 2,3,4,5,6-Pentafluorothiophenol (Figure 2.1) from Sigma Aldrich in 50 mL of ethanol in a glass bottle, and stored in a  $\text{N}_2$ -filled glove box. The substrates that have gold and silver electrodes, then, were immersed in the solution for 15 min creating a



PFBT SAM layer on the surface of electrodes by chemisorption. Next, the residues of PFBT on the surface of the substrates were rinsed off in pure ethanol for one min followed by five min of annealing on a hot plate at 60 °C.

### 2.1.3. Solution processing of organic semiconductors

Poly(triarylamine) (PTAA) blended triisopropylsilylethynyl pentacene (TIPS-pentacene) has been reported to have optimum properties in terms of phase segregation in films and electrical performances in OFETs combined with tetralin in the solution [43, 53], and those materials are commercially available chemicals. In addition, top-gate TIPS-pentacene/PTAA OFETs have proven to have high operational and environmental stabilities, and can be fabricated on flexible substrates [61]. For those reasons, we applied the PTAA-blended TIPS-pentacene film as an active semiconducting layer in top-gate OFETs of this dissertation research.

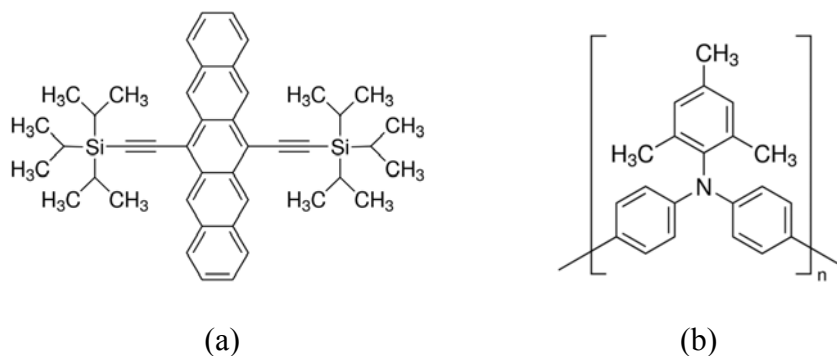


Figure 2.3. Chemical structure of (a) TIPS-pentacene and (b) PTAA (Sigma Aldrich).

TIPS-pentacene and PTAA that are stored in a N<sub>2</sub>-filled glove box, were mixed with a 1:1 weight ratio, and then dissolved in anhydrous 1,2,3,4-tetrahydronaphthalene for a concentration of 30 mg/mL [53]. This solution was filtered with 0.2 μm PTFE filter and spin-coated on the substrate having source/drain electrodes in a N<sub>2</sub>-filled glove box with

two steps: the first step is 500 rpm for 10 s with 500 rpm/s acceleration, and the second step is 2000 rpm for 20 s with 1000 rpm/s acceleration. The spin-coated sample is annealed immediately at 100 °C for 15 min on a hot plate in a N<sub>2</sub>-filled glove box [43].

#### **2.1.4. Deposition of bilayer gate dielectrics**

The amorphous fluoropolymer, CYTOP, provides many attractive properties in organic devices since it is chemically stable, highly hydrophobic, and dissolves in fluorinated solvents that are orthogonal to most organic semiconductor materials [42, 53]. In this research, CYTOP (CTL-809M, Asahi Glass) diluted with a solvent (CT-SOLV180, Asahi Glass) (1:3.5 volume ratio) was spin-coated on top of the semiconductor layer at 3000 rpm for 60 s (acceleration of 10000 rpm/s) to produce ca. 35 nm-thick film followed by an annealing process step at 100 °C for 10 min on a hot plate inside a glove box.

When CYTOP is combined with atomic-layer deposited Al<sub>2</sub>O<sub>3</sub>, which has excellent barrier properties and high capacitance density, as a bilayer gate dielectrics, this gate dielectric layer contributes to making hysteresis-free high performance OFETs that also have high operational/environmental stability [53]. Atomic layer deposition (ALD) is a highly-conformal deposition technique with significantly reduced defects, high barrier properties, and a high capacitance density for dielectric layers grown at relatively low temperature [92]. The deposition process is also simple, low-cost, and compatible with various substrates [65, 92].

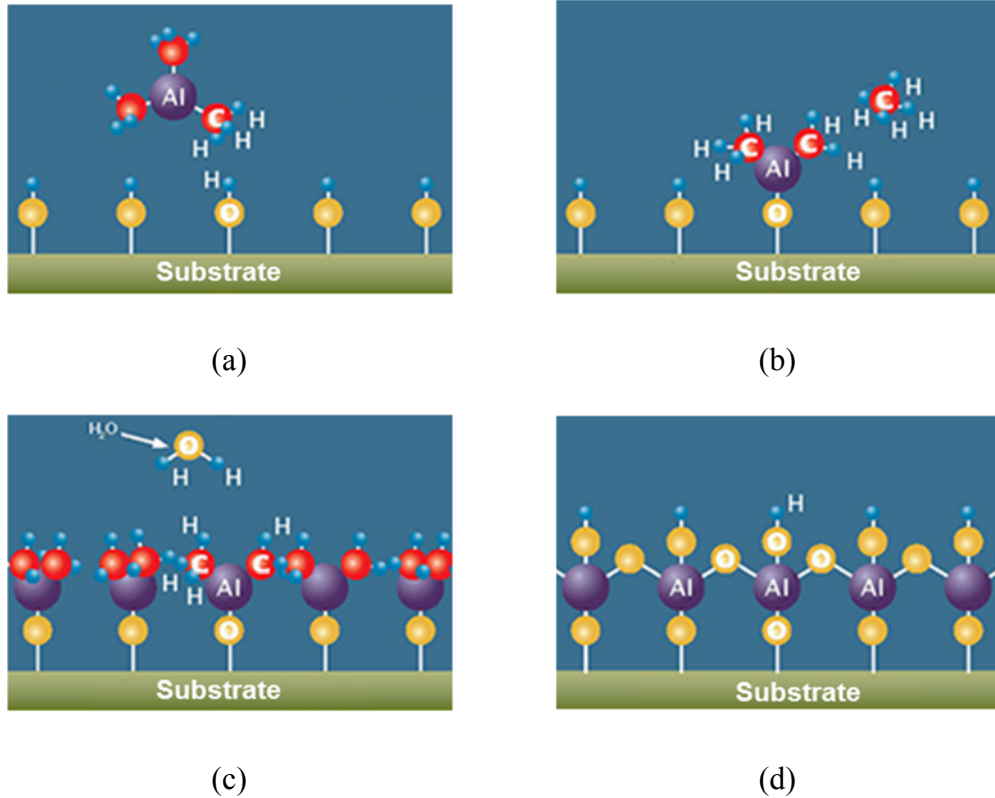


Figure 2.4. ALD example cycle for Al<sub>2</sub>O<sub>3</sub> deposition (Cambridge NanoTech Inc.)

Figure 2.4 illustrates the example of an Al<sub>2</sub>O<sub>3</sub> deposition by ALD. This process involves alternate exposure of two precursors to the substrate surface. First, by pulsing trimethylaluminum (TMA) into the reaction chamber, the precursor reacts with the hydroxyl groups (OH) on the surface until the surface is fully occupied and terminated, in that only one layer of TMA covers the surface. After the excess TMA is pumped out, water vapor is pulsed into the reaction chamber and forms aluminum-oxygen (Al-O) bridges leaving another hydroxyl group on the surface followed by the pumping out of excess water vapor. By repeating the above steps, a thin, ca. 1 angstrom, monolayer of aluminum oxide is deposited during each cycle providing good controllability in the final thickness of the film.

In this research, a Savannah 100 ALD system from Cambridge Nanotech was used for the deposition of a 40 nm-thick Al<sub>2</sub>O<sub>3</sub> film or a 30-nm thick nanolaminate film, that is an alternate stack of Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub>, at a processing temperature of 110 °C and 100 °C, respectively.

### 2.1.5. Fabrication of shape-memory polymer substrates

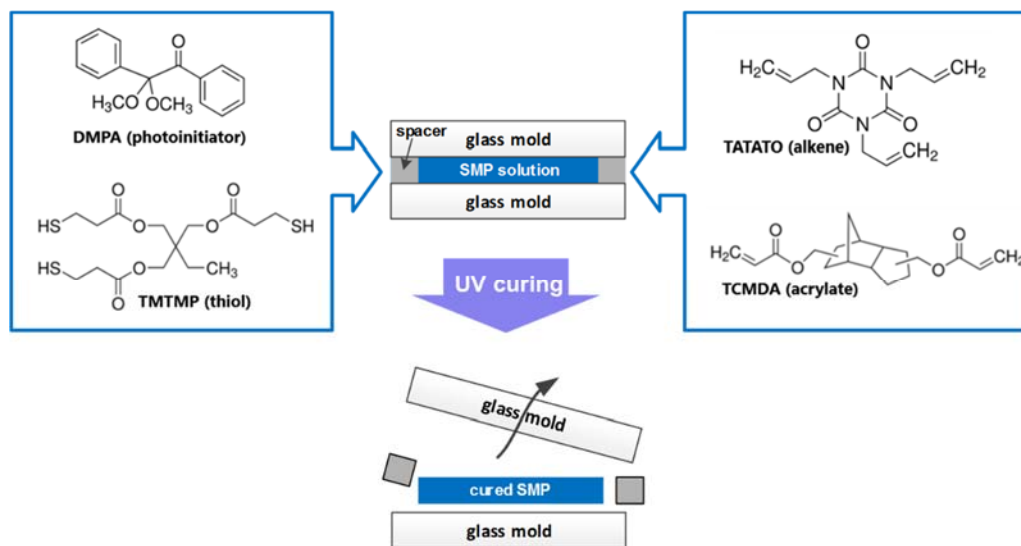


Figure 2.5. Fabrication procedure of shape-memory polymer substrates.

Figure 2.5 illustrates the process steps of fabricating SMP substrates. Tricyclodecane dimethanol diacrylate (TCMDA, Sigma-Aldrich), 1,3,5-triallyl-1,3,5-triazine-2,4,6(1*H*,3*H*,5*H*)-trione (TATATO, Sigma-Aldrich), and 2,2-dimethoxy-2-phenyl acetophenone (DMPA, Sigma-Aldrich), a photocuring agent, were mixed in a vial with a composition ratio of 31 mol%, TCMDA and 0.1 wt.% DMPA followed by vortex mixing for two min. The vial was covered by aluminum foil to shield the solution from light exposure, and trimethylolpropane tris(3-mercaptopropionate) (TMTMP, Sigma-Aldrich) was added into the solution. After another vortex mixing for two min, the vial was sonicated for five min removing air bubbles in the solution. All the chemicals were used

without additional purification after purchase. Microscope glass slides of desired dimensions were cleaned by sonication in acetone, deionized water, and isopropanol for molding. The surface of the glass slides (molds) were coated with Rain-X (Illinois Tool Works Inc.) preventing the polymer from adhering to the glass molds during curing. Two spacers of a desired thickness were placed along opposite sides of the bottom glass slide, and the unreacted polymer solution was applied to the bottom glass slide followed by rolling the top glass slide across the surface of the solution. The two glass slides were, then clamped together with binder clips around the spacers. The mold was placed in the UV chamber for 45 min, spreading the unreacted polymer across the mold, and cured with 365 nm UV radiation for one hour, followed by another one minute of UV curing after removing the binder clips. Once the top glass slide was removed, the SMP substrate was post-cured in a vacuum oven for 12 h at 120 °C. The bottom glass slide was kept under SMPs providing rigid and flat backplane during the transistor fabrication process.

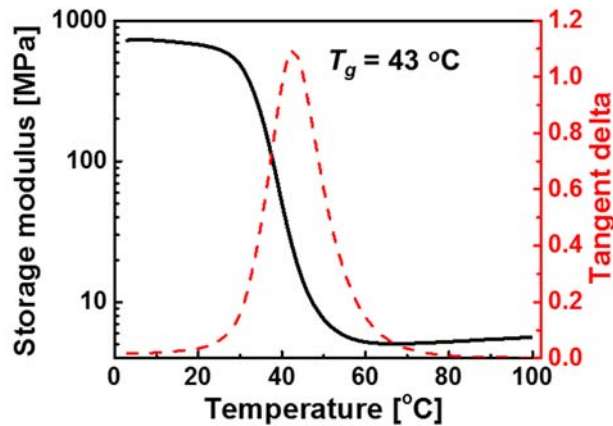


Figure 2.6. Dependence of Young's modulus of the SMP substrates on temperature ( $T_g$ : glass transition temperature). Adapted from [93].

The SMP substrates fabricated by the above procedure display a variable Young's modulus depend on the temperature of the substrate as shown in Figure 2.6. Once the

substrates are heated above the glass transition temperature,  $T_g$ , they become soft and can be deformed easily. By cooling the deformed substrates, SMPs sustain the deformed shape. In addition, the reshaped substrates return to the original shape without any other external force involved by being heated above  $T_g$ .

## **2.2. Characterization of thin-films and OFETs**

The thickness of thin films was measured and modeled by spectroscopic ellipsometry (J.A. Woollam M-2000UI) that acquires data at three angles of incidence: 65°, 70° and 75°, and by a confocal microscope (OLS4100, Olympus LEXT 3D laser microscope). The work function and the water contact angle of the electrodes were measured by a Kelvin probe (Besocke Delta Phi) in a N<sub>2</sub>-filled glove box and by a contact angle analyzer (Phoenix300, SEO), respectively. The material composition of TIPS-pentacene/PTAA film on the electrodes was analyzed on films by an x-ray photoelectron spectroscopy (Thermo K-Alpha, Thermo Scientific, Inc., Waltham, MA, USA) using incident photons of 1486.6 eV from an Al K $\alpha$  monochromatic source. A polarized-light microscope (Olympus BX51) was employed to observe film morphologies. Surface roughness of SMP substrates were measured by a scanning probe microscope (SPM) from Veeco.

Fabricated top-gate OFETs were measured on a Lucas-Signtone H100 series probe station, which consists of micromanipulators that can move probes in three axes and a linear translation stage positioned on a portable air table to lower the vibration, in a N<sub>2</sub>-filled glove box (MBRAUN Labmaster 130). The current-voltage characteristics of OFETs and capacitance were measured with a two-channel source-monitor unit (Agilent E5272A), which is controlled by customized LabView codes (National Instruments), and a precision

LCR meter (Agilent 4284A), respectively. Pseudo-complementary inverter circuits and decoder circuits were operated and measured by an Agilent E5272A source meter and an additional power supply, a DC output power supply (Agilent E3647A), which provides two different levels of voltage sources.

### 2.3. Design of OFET circuits

For the circuit design using TIPS-pentacene/PTAA OFETs, SPICE parameters of the OFETs were extracted by manually fitting the transfer/output characteristics based on the HSPICE RPI model (level 62, Synopsys), which was developed for a SPICE simulation of poly-Si thin-film transistors. Figure 2.7 displays the measured transfer characteristics that are used in the parameter extractions, and the simulated transfer characteristics that are reproduced by HSPICE simulation with the extracted parameters.

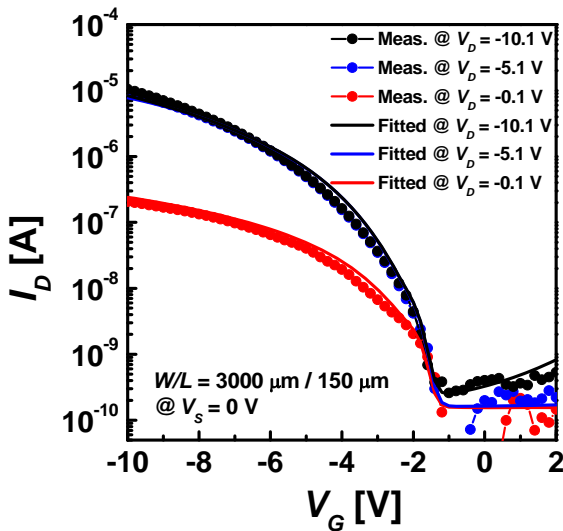


Figure 2.7. SPICE parameter extraction from transfer characteristics of OFETs.

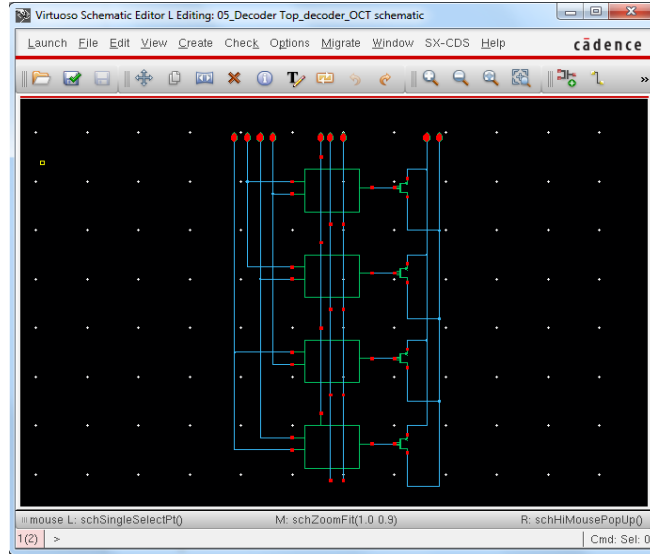
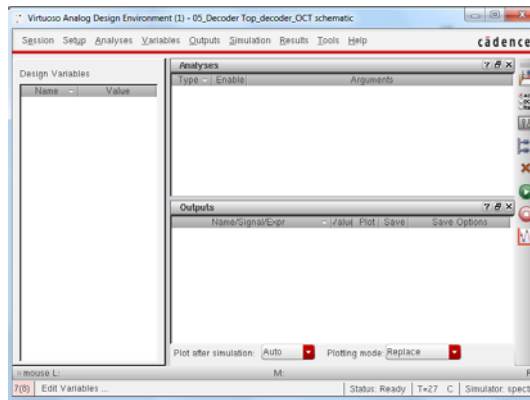
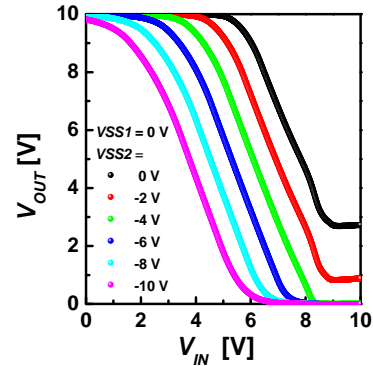


Figure 2.8. Screen capture of Virtuoso Schematic Editor (Cadence).



(a)



(b)

Figure 2.9. (a) Screen capture of Virtuoso ADE-L (Cadence) and (b) simulation results of inverter circuits.

OFET circuits were schematic-designed using Virtuoso Schematic Editor (Cadence, Figure 2.8), and the netlist of the schematics were extracted by Virtuoso Analog Environment (Cadence, Figure 2.9). With the extracted netlist and input stimuli, circuit performances were simulated by HSPICE. After the size of OFETs were optimized by a SPICE simulation, actual patterns of source/drain and gate electrodes were layout-designed



by Cadence Virtuoso Layout Suite, as shown in Figure 2.10, followed by a pattern-code generation, which is to transform the layouts into pattern codes that Resonetics IR laser can interpret for micro-machining shadow masks (Figure 2.11(a)).

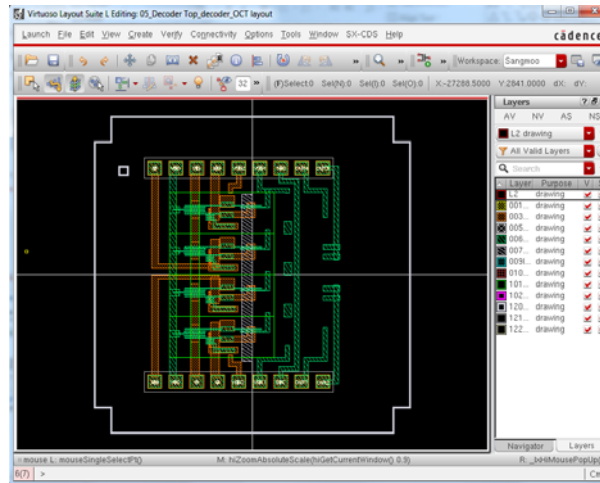


Figure 2.10. Screen capture of Virtuoso Layout Suite (Cadence).

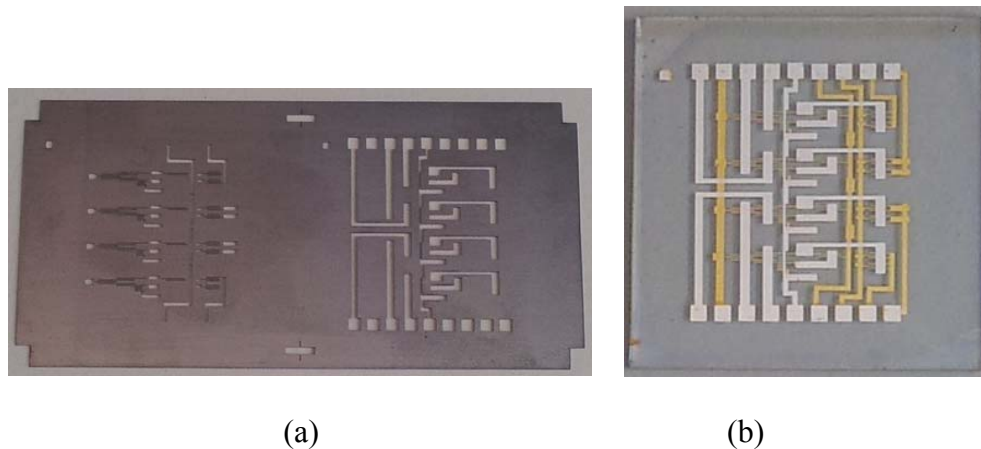


Figure 2.11. (a) Shadow masks used for source/drain and gate electrodes of the circuits and (b) the photograph of fabricated circuits on a 1.5-inch by 1.5-inch glass substrate.

## CHAPTER 3 Top-Gate OFETs with Low Contact Resistance

### 3.1. Introduction

In recent years, the field-effect mobility values of OFETs have increased significantly close to  $10 \text{ cm}^2/\text{Vs}$  [47, 94, 95], and the operating voltages have decreased to 3 V [39, 96]. As the current driving capability becomes higher from the high field-effect mobility and the small threshold voltage, parasitic contact resistance at the metal-semiconductor interface starts to limit the performance of OFETs. In addition, high contact resistance often results in the overestimation of field-effect mobility values; for example, a 23 times higher field-effect mobility value than actual value was extracted from a OFET that shows non-ideal  $I$ - $V$  characteristics [15, 48]. Therefore, low contact resistance in OFETs is one of the key elements realizing high performance OFETs with ideal field-effect transistor characteristics.

In this research, contact doping with  $\text{Mo}(\text{tfd})_3$  and  $\text{MoO}_3$  has been suggested and evaluated in terms of the reduction of contact resistance in top-gate OFETs, and a systematic study of the contact resistance change in top-gate OFETs has been performed with two different approaches to reduce its values. In the first approach, the effect of using source/drain electrodes that have work function values in the range from 4.6 eV to 6.8 eV in the top-gate OFETs was studied with respect to the corresponding contact resistance in the device. In the second approach, the use of a p-dopant,  $\text{Mo}(\text{tfd})_3$ , for contact doping in top-gate OFETs is investigated by area-selectively depositing a thin layer of the dopant on top of source/drain electrodes.

### 3.1.1. Highly stable top-gate organic field-effect transistors

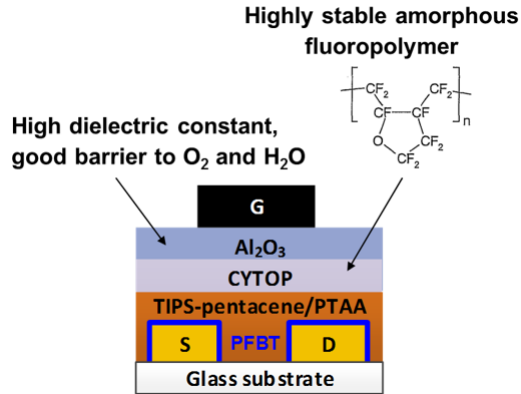


Figure 3.1 Cross-sectional view of top-gate TIPS-pentacene/PTAA OFETs.

Top-gate geometries in OFETs greatly improve their stability, and in particular, by combining a CYTOP/Al<sub>2</sub>O<sub>3</sub> bilayer as a gate dielectric and a TIPS-pentacene/PTAA blend as a semiconductor layer, which was illustrated in Figure 3.1, the top-gate OFETs exhibit not only high performance in their electrical properties, such as a low operating voltage, high field-effect mobility, but also excellent stability [53, 55, 56] as presented in Figure 3.2 and Figure 3.3.

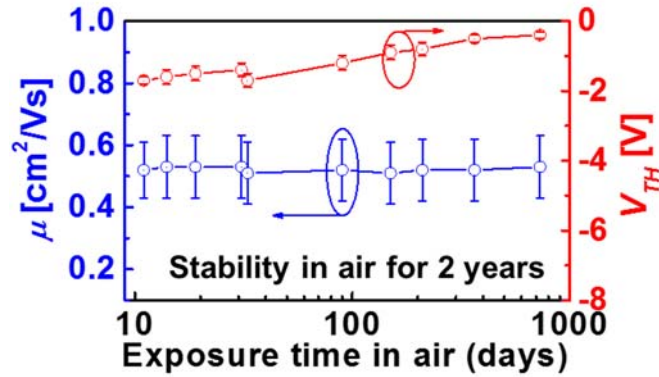


Figure 3.2 Degradation of top-gate TIPS-pentacene/PTAA OFETs in air in terms of their threshold voltages and field-effect mobility values for two years. Adapted from [53].

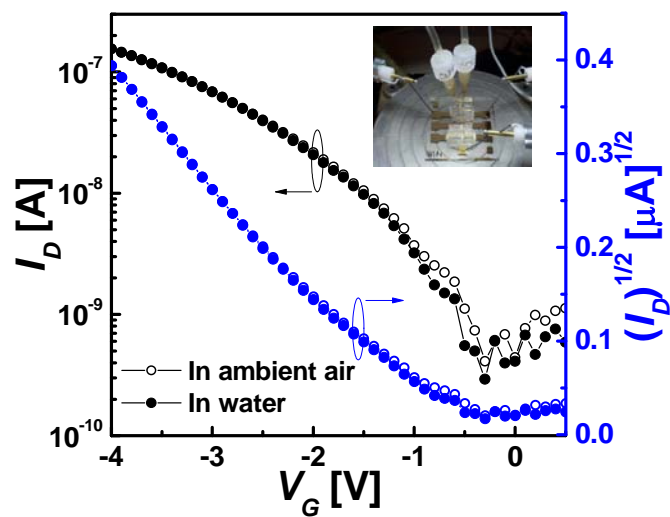


Figure 3.3 Transfer characteristics of the top-gate OFETs in air and in water. Adapted from [56].

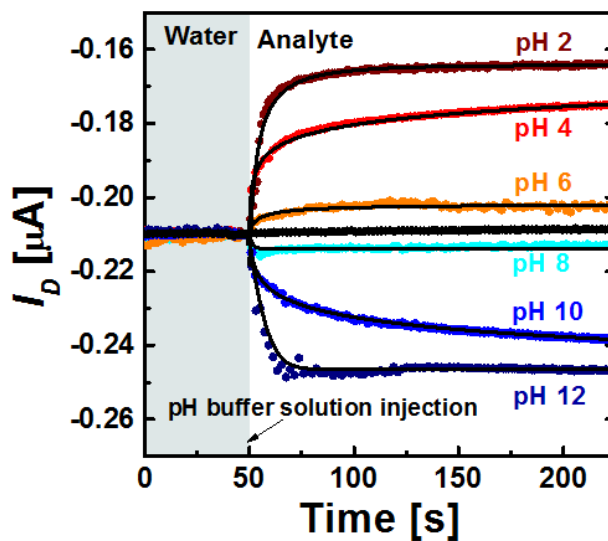


Figure 3.4 The changes of the drain current of the top-gate OFET sensors in water by different pH values. Adapted from [56].

The high environmental stability of the top-gate geometry enables the use of the OFETs as reusable chemical sensors in aqueous conditions using the non-destructive operations of the OFETs in water [56]. Figure 3.4 shows the changes of the drain current,  $I_D$ , of the OFETs which correspond to each pH value of analytes in water. For these reasons,

the top-gate OFETs with the bilayer gate dielectrics are expected to be a good candidate for a backplane technology of OFET circuits and systems.

### 3.1.2. Contact resistance in top-gate TIPS-pentacene/PTAA OFETs

As the top-gate TIPS-pentacene/PTAA OFETs exhibit high field-effect mobility values and low threshold voltages in their electrical properties, the contact properties at the interface between source/drain electrodes and organic semiconductors in the device impair overall performance. For example, Figure 3.5 presents transfer characteristics of two different TIPS-pentacene/PTAA OFETs in the same batch. The transfer characteristics in Figure 3.5(a) show non-linear behavior of the  $(I_D)^{1/2}$  curve when  $V_G$  is smaller than -10 V while that in Figure 3.5(b) presents better compliance to the square law of field-effect transistors. The non-linearity in Figure 3.5(a) occurs when  $I_D$  is limited by the high contact resistance, and the increase of  $I_D$  is dominated by the contact resistance modulation rather than the channel resistance modulation of traditional field-effect transistors.

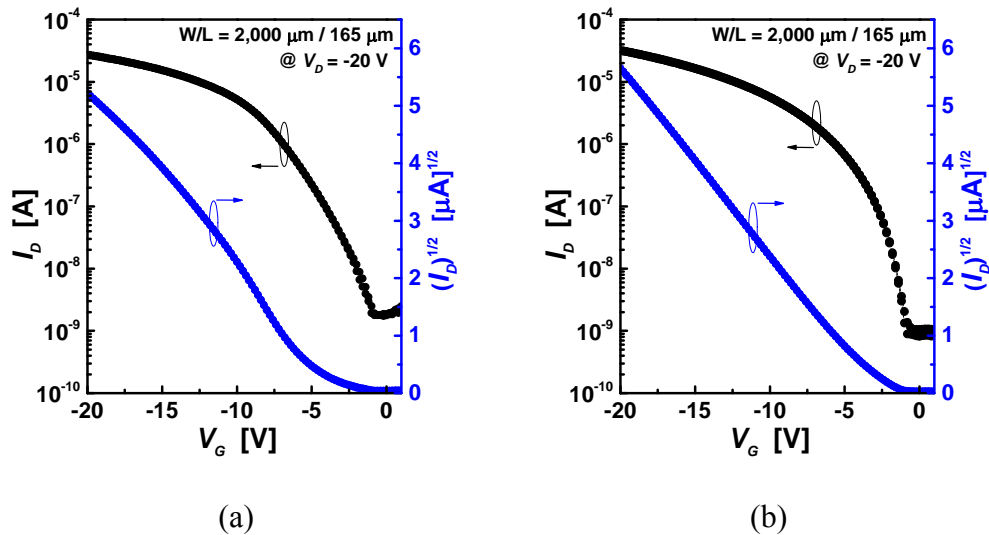


Figure 3.5. Transfer characteristics of two different TIPS-pentacene/PTAA OFETs that have (a) high contact resistance and (b) low contact resistance.

Therefore, to ensure the reproducible device characteristics of the OFETs and to make use of the best performance of the OFET structure, the improvement in the contact resistance of the OFETs is crucial. Particularly, decreasing the operating voltage of the OFETs for low power consumption and using the devices at a low voltage bias make contact resistance issue more apparent in their electrical characteristics.

Therefore, exploiting the advantages of the top-gate OFETs, lowering the contact resistance of the OFETs should be the first step paving the way to the use of this device geometry in low-power and high-performance organic transistor circuits and systems.

### **3.1.3. Contact resistance at metal-semiconductor interfaces**

Unlike crystalline-silicon semiconductors that utilize highly doped silicon wells as a contact with metal electrodes, which in turn enhance the tunneling of charge carriers at the contact and make good ohmic contact in the transistors, organic thin-film transistors suffer from high contact resistance. After all, the metal-semiconductor contact in organic semiconductor devices is composed of heterogeneous materials without, in general, doping the semiconductor side, and the lower carrier mobility in bulk of the semiconductor film induces higher bulk resistance in OFETs. For those reasons, organic field-effect transistors impose the parasitic contact resistance at the interface that consists of two components: injection resistance at a metal-semiconductor interface, and bulk resistance of a semiconductor film that is perpendicular to the channel of transistors. Figure 3.6 displays the simple model of contact resistance,  $R_C$ , in top-gate bottom-contact OFETs where  $R_{CH}$  is the channel resistance,  $R_{INJ}$  is the injection resistance by the potential drop at the interface,  $R_{VBLK}$  is the vertical bulk resistance between the metal electrodes and the channel of OFETs, and  $R_{HBLK}$  is the horizontal bulk resistance which has identical sheet resistance

values to the channel resistance induced by a gate voltage bias. In this simple model,  $R_C$  is modeled as a summation of  $R_{INJ}$ ,  $R_{HBLK}$ , and  $R_{VBLK}$ .

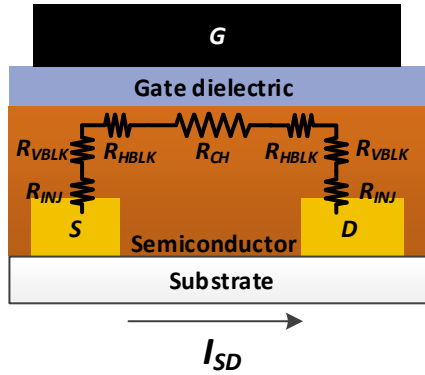


Figure 3.6. Simple model of the contact resistance composition in top-gate OFETs.

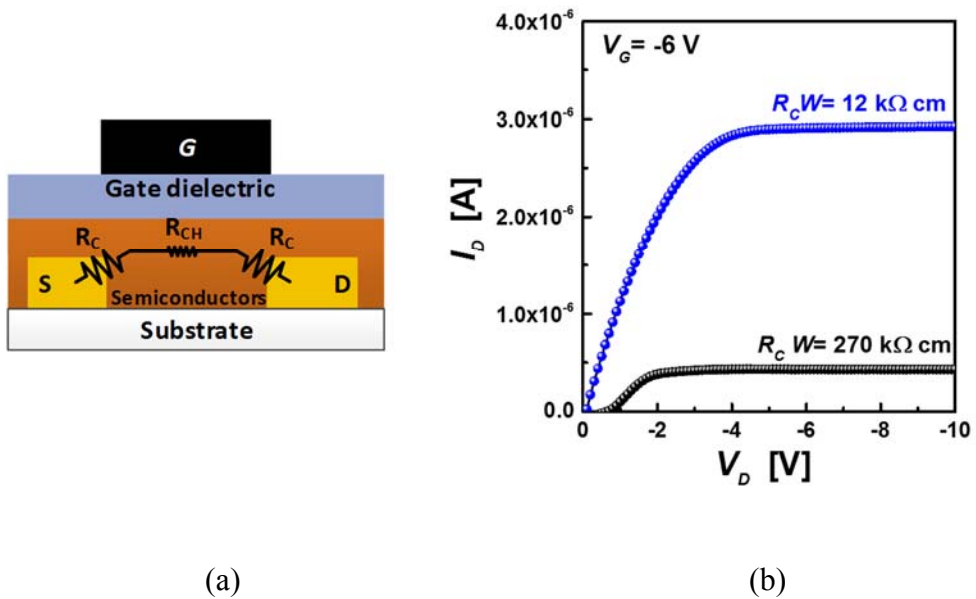


Figure 3.7. (a) Cross-sectional view of top-gate OFETs with simplified model of total resistance across the device ( $R_C$  is contact resistance and  $R_{CH}$  is channel resistance), and (b) a comparison of drain current of two OFETs with different contact resistance values.

When the channel resistance,  $R_{CH}$  in Figure 3.7(a), decreases to near or below that of contact resistance, the amount of drain current,  $I_D$ , in the transistor starts to be limited more by contact resistance than by channel resistance, which is not preferred in field-effect transistors. Figure 3.7(b) presents an example of the limited drain current. Both drain

current values in blue and in black have been measured from top-gate OFETs having the same geometry in the same batch but having different metal-semiconductor contact properties, in turn, the one with 20 times lower contact resistance induces about six times higher drain current at the same voltage bias condition. This example indicates that the difference in the contact resistance results in a drastic change in drain current and the current driving capability of OFETs.

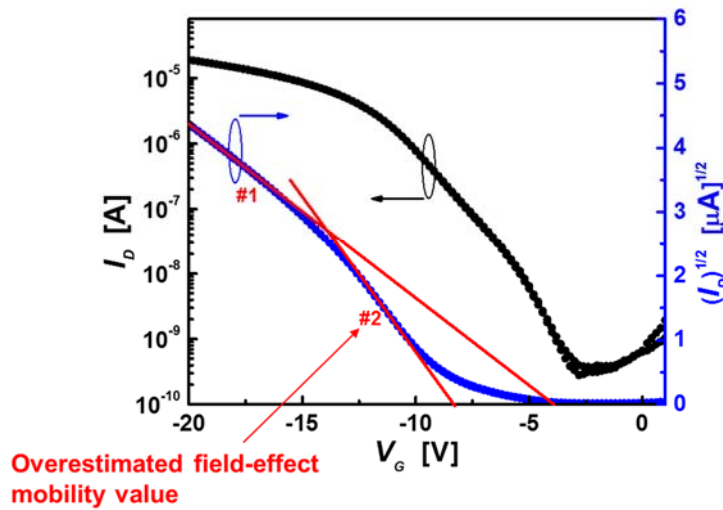


Figure 3.8. Overestimation of electrical parameters from transfer characteristics of OFETs.

Another critical issue resulting from high contact resistance in OFETs is the inaccurate extraction of electrical parameters of transistors. Particularly, the overestimation of field-effect mobility values is often observed in literature [15, 47, 48]. For example, when OFETs impose high contact resistance, they often exhibit transfer characteristics that show non-linear  $(I_D)^{1/2}$  curves as shown in Figure 3.8, which leads to the improper extraction of the slope of the line by linear-fitting  $(I_D)^{1/2}$  at a contact-resistance dominant regime, in the above case fitting with line #2. Then, the extracted field-effect mobility value of the transistor becomes much higher than the actual value that is measured and extracted



at a high  $V_G$  regime, where channel resistance modulation governs the drain current, following line #1.

### 3.1.3.1 Injection resistance in OFETs

Injection resistance results from an energy barrier for charge carriers being injected from metal electrodes to the semiconductor films and vice versa. This injection resistance appears as a voltage drop at the interface and reduces an effective source/drain voltage bias in transistors. The energy barrier originates from the difference between the work function of electrodes and the ionization energy of p-channel organic semiconductors, or the electron affinity of n-channel organic semiconductors [97], and the disorder-broadened density of states of semiconductors also affects the injection properties [98].

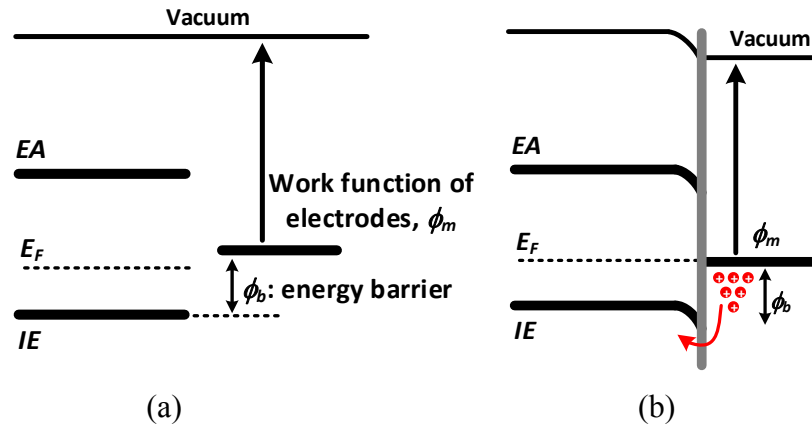


Figure 3.9. Injection energy barrier at the interface of metal and p-channel semiconductors.

Figure 3.9 illustrates an example of an energy barrier height at an interface between metal electrodes and p-channel semiconductor films. The initial injection barrier for hole carriers before making contacts remains at the same height after making contacts aligning their Fermi level energy. Therefore, as the work function value of a metal,  $\phi_m$ , increases and approaches the ionization energy of p-channel semiconductor films, the energy barrier height,  $\phi_b$ , decreases and the field-injection current at the interface exponentially increases

following Schottky-Mott limit [53]. The charge injection through an ideal Schottky barrier is described by thermoionic field-emission that yields:

$$J = J_0 \left( e^{\frac{qV}{kT}} - 1 \right) \quad (3.1)$$

where  $V$  is the applied voltage across the contact,  $k$  is the Boltzmann constant,  $T$  is the absolute temperature,  $q$  is the charge of electrons, and  $J_0$  is the reverse saturation current of the Schottky diode which is described by:

$$J_0 = A^* T^2 e^{\frac{-2\phi_b}{kT}} \quad (3.2)$$

where  $A^*$  is the Richardson constant,  $\phi_b$  is the energy barrier height. This model suggests that the energy barrier height tremendously affects the injection current density,  $J$ , therefore, reducing the barrier height is one of the key factors in lowering contact resistance.

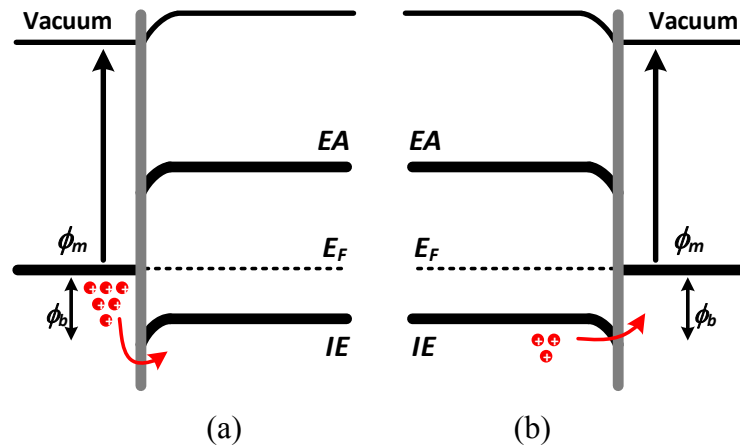


Figure 3.10. Energy band diagram at (a) a source-contact interface and (b) a drain-contact interface.

Regarding the injection barrier height, it is noteworthy that the barrier height and corresponding contact resistance of source electrodes are higher than those of drain electrodes [97, 99, 100]. This difference in contact resistance originates from the direction

of charge injection at two contacts, source and drain contacts. Hole carriers in p-channel OFETs are injected from source electrodes to semiconductors undergoing a high energy barrier while the hole carriers are collected at drain electrodes; in turn, the energy barrier at drain-contacts is lower than that at source contacts as illustrated in Figure 3.10. In addition, the barrier height at drain-contacts decreases as a voltage bias is applied across source and drain electrodes, which further lowers the barrier height at the interface whereas the barrier height at source contacts remains same regardless of the applied voltage bias.

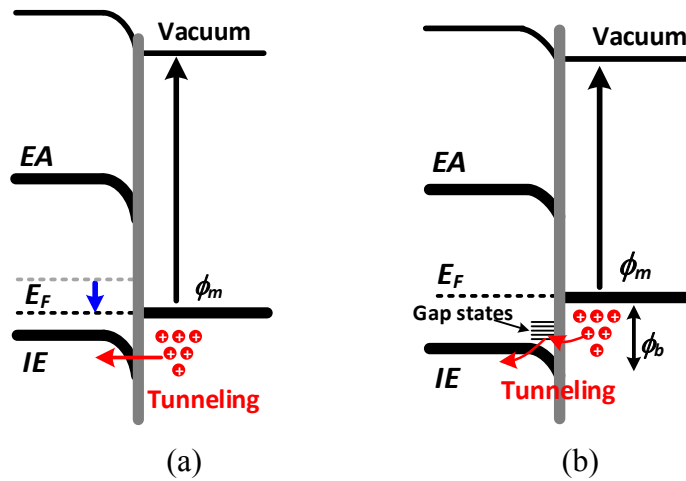


Figure 3.11. Energy band diagram at metal-p-channel semiconductor interfaces when hole carriers are injected by tunneling.

Tunneling is another injection mechanism at a metal-semiconductor interface of transistors. Doping of an organic semiconductor film at contacts enhances the tunneling injection similar to those in crystalline-silicon semiconductors by promoting the tunneling current through a narrow depletion region as illustrated in Figure 3.11(a). The abundant gap states near the interface in organic semiconductors, as shown in Figure 3.11(b), also increase the possibility of tunneling of charge carriers by bridging metal electrodes and a HOMO band of organic semiconductors [101]. Even though the charge carriers pass through the energy barrier at the interface by tunneling, still the probability that the charge

carriers of a specific energy state can tunnel through an energy barrier,  $P(E)$ , exponentially increases not only by increasing the dopant concentration,  $N$ , but also by reducing the energy barrier height,  $\phi_b$ , as described by:

$$P(E) \sim \exp\left(-\frac{2\phi_b}{\hbar} \sqrt{\frac{\epsilon_s m^*}{N}}\right) \quad \text{Equation (3.3)}$$

where  $\hbar$  is Plank's constant,  $\epsilon_s$  is the permittivity of the semiconductor, and  $m^*$  is the effective mass of the charge carriers, resulting in a corresponding increase in the injection current density,  $J$ , as described by:

$$J = \frac{A^*T}{k} \int F_s P(E)(1 - F_m)dE \quad \text{Equation (3.4)}$$

where  $F_s$  and  $F_m$  are the Fermi-Dirac distribution function of semiconductors and metal, respectively.

Since the energy barrier height,  $\phi_b$ , significantly affects both thermoionic and tunneling injection at the interface, decreasing the barrier height has been intensively studied by many research scientists by choosing metal electrodes that have work function values matching either  $IE$  or  $EA$  of semiconductor films, by treating the surface of electrodes with self-assembled monolayer (SAM) [81, 82, 84, 87-91], by inserting high work function transition metal-oxide layers [102-105], and by doping semiconductor films [20, 106-113].

### 3.1.3.2 Pinning of Fermi level energy

Fermi level energy of a semiconductor film shifts according to the carrier concentration in the bulk. Particularly, when the semiconductor film contacts metal electrodes, the two materials having different work function or Fermi level energy

exchange charges at the interface by thermal dynamics until the work function of the electrodes and the Fermi level energy of the semiconductor align, inducing a shift of Fermi level energy of the semiconductor film at the interface [114]. The shift of Fermi level energy is, however, attenuated as the distance from the contact increases, that is, the carrier concentration in the bulk is returning to its intrinsic value.

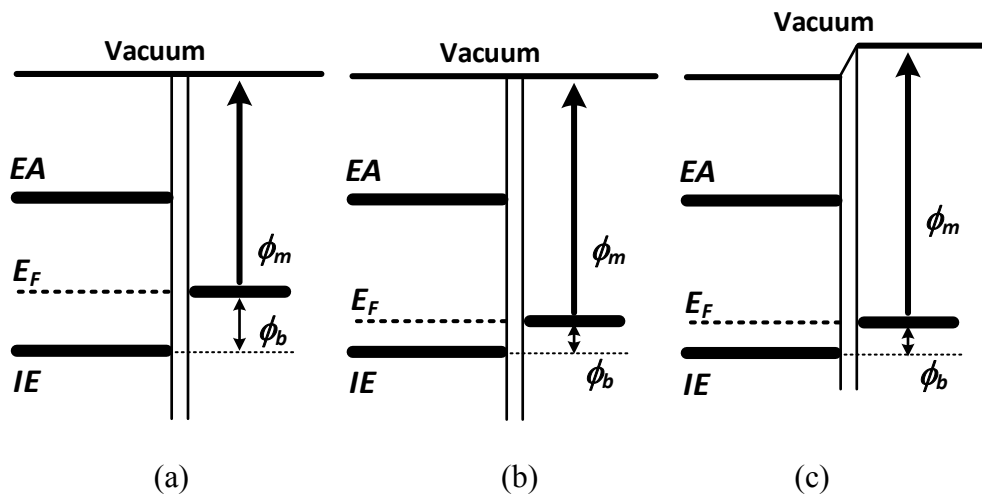


Figure 3.12. Alignment of Fermi level energy,  $E_F$  at the metal-semiconductor interface: (a) before  $E_F$  is pinned, (b) when  $E_F$  start to be pinned, and (c) after  $E_F$  is pinned.

On the other hand, the alignment of Fermi level energy is constrained by dipoles that are formed at the interface when the work function of contacting electrodes exceeds a certain level above a HOMO band or beneath a LUMO band as illustrated in Figure 3.12. The dipoles are understood to be created by the tail states or gap states that are originated from the static and/or dynamic disorder in organic films, and are charged when Fermi level energy approaches to either the HOMO or the LUMO band edge [110, 115-118]. That is, Fermi level energy of semiconductor films is pinned at a certain energy level, which is referred to a pinning level, and using electrodes that have work function higher than the pinning level near the HOMO band, or lower than the pinning level near the LUMO band,

does not further change the Fermi level energy of the neighboring semiconductor film; in turn, the height of the injection energy barrier,  $\phi_b$ , at the interface is also pinned at a certain value and does not further decrease.

### 3.1.3.3 Bulk resistance on the contacts of OFETs

Contact resistance at a metal-semiconductor interface also comprises the semiconductor bulk resistance since the injected charge carriers at the contact region need to transport to the channel of the device which is located at the interface between gate dielectrics and semiconductors. On one hand, the bulk resistance can be higher in staggered geometries, such as top-gate bottom-contact and bottom-gate top-contact structures, than in those coplanar geometries, such as top-gate top-contact and bottom-gate bottom-contact structures, since OFETs with staggered geometries have longer transporting distance for the charge carriers than the others. On the other hand, the OFETs with staggered geometries have a larger effective contact area than the coplanar structured transistors because the gate bias also induces a channel in the contact area, minimizing the current crowding at the edge of the contacts in the OFETs. In addition, the thickness of the bulk and the bulk carrier mobility in contacts affect the bulk resistance [100], which suggests that the morphology, the molecular packing, and the crystallinity of the bulk highly affect the contact resistance values of organic transistors. For these reasons, the transistor geometry and the associated vertical bulk resistance also significantly impact contact resistance together with the injection barrier [119]. Richards *et al.* introduced the relationship of the bulk properties with contact resistance as the following equation [100]:

$$R_C = \frac{A}{V_G - V_{TH}} + R_{CO} \quad (3.5)$$

where  $V_G$  is the gate voltage bias,  $V_{TH}$  is the threshold voltage,  $A$  is the fitting parameter that is related to the bulk mobility and the thickness of the bulk, and  $R_{CO}$  is the portion of contact resistance independent of the gate voltage bias in the region near metal-semiconductor interfaces in which the carrier concentration is mostly governed by the energetics at the interface.

#### **3.1.4. Evaluation of contact resistance**

Contact resistance can be measured by either the direct measurement of voltage drops at contacts or by the extraction of contact resistance in the total resistance across source and drain electrodes. Scanning Kelvin probe microscopy and direct contact atomic force microscopy directly evaluate a voltage drop across a channel and a contact region [97, 100, 120]. However, those methods can be applied only to bottom-gate transistors that expose and allow accessing the entire electric current path of the transistors to the surface of the sample. On the other hand, the indirect extracting methods of contact resistance, such as equivalent circuit models [121], transmission-line methods or transfer-line methods (TLMs) [122, 123], and four-point-probe techniques, are applicable regardless of the geometry of transistors [124]. However, each indirect method also has its own limitations; the equivalent circuit model requires a functional model so that its availability and accuracy rely on the model, both TLMs and four-point-probes are applicable only in the linear regime where the channel resistance of OFETs linearly increases as the length of the channel increases, that is, the gate-voltage bias needs to be high enough to induce the channel of the transistors, and  $V_{DS}$  needs to be small enough to ensure the uniform channel thickness across the entire channel [100]. The four-point-probe has an additional advantage over TLMs; that is, this method is also applicable when the contact resistance is dependent

on the applied electric field across the contact whereas TLMs require an ohmic behavior of contact resistance.

In this dissertation research, TLMs have been applied in evaluating the contact resistance of OFETs since direct potential scanning is not available for top-gate OFETs; the accurate electrical model of top-gate OFETs is not well established; and fine patterning of additional two probes between source and drain electrodes cannot be realized in the top-gate OFETs used in this research.

TLMs basically assume that the channel resistance of transistors,  $R_{CH}$ , is uniform across the entire channel, and that as the length of the channel increases, the channel resistance also increases linearly. In that way, if the channel length reduces to zero, all the remaining resistance in the transistor is attributed to contact resistance,  $R_C$ . In practice, by plotting the total resistance of the transistor across source and drain electrodes,  $R_{TOT}$ , of several transistors having different channel lengths and extrapolating the linearly-fitted line of total resistance to the point of the zero channel length, the contact resistance of the OFET can be extracted as shown in Figure 3.13.

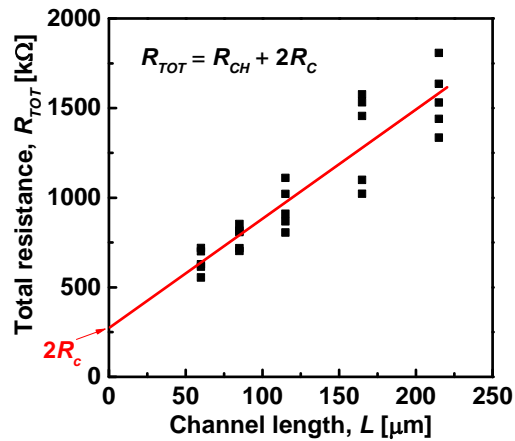


Figure 3.13. Extraction of contact resistance,  $R_C$ , from a plot of total resistance,  $R_{TOT}$ , of transistors with various channel lengths.



As mentioned above, the transistors have to be operated in the linear regime and the lowest possible  $V_{DS}$  is preferred to ensure the uniform distribution of channel thickness in the device in applying TLMs. Therefore, the total resistance,  $R_{TOT}$ , can be described as Equation (3.6), as  $V_{DS}$  approaches 0 V [125-127]:

$$R_{TOT} = \left. \frac{\partial V_{DS}}{\partial I_{DS}} \right|_{V_{DS} \rightarrow 0} = R_{CH} + 2R_C = R_{SH} \frac{L}{W} + 2R_C \quad (3.6)$$

where  $R_{SH}$  is the sheet resistance of the channel.

### 3.2. Top-gate OFETs with contact-doped electrodes

As stated in section 3.1.2, the top-gate TIPS-pentacene/PTAA OFETs still present considerable amount of contact resistance when the source/drain electrodes are treated by PFBT. Therefore, in this dissertation research, contact-doping methods are applied to the device structure reducing the contact resistance of the OFETs and ensuring that the performance of the OFETs are not limited by contact properties.

#### 3.2.1. Doping of organic semiconductors

As one of the solutions to improve the contact properties in organic semiconductors, contact-doping methods have been widely adapted. This method utilizes an interlayer in the vicinity of source/drain electrodes [106, 107, 109-111, 128-141] and provides excess charge carriers into the adjacent semiconductor film. In the case of p-channel OFETs, contact doping has been implemented using: tetrafluoro-tetracyanoquinodimethane (F4TCNQ) [106, 107, 131-134] derivatives, such as 1,3,4,5,7,8-hexafluoro-tetracyanonaphthoquinodimethane (F6TCNNQ) [135]; transition metal-oxides such as  $\text{MoO}_3$  [136-138]; molybdenum tris-[1,2-bis(trifluoromethyl)ethane-1,2-dithiolene]

(Mo(tfd)<sub>3</sub>) [109-111]; and FeCl<sub>3</sub> [128-130]. In the case of n-channel OFETs, polyethylenimine ethoxylated (PEIE) and branched polyethylenimine (PEI) that include aliphatic amine groups have been used to dope the semiconductors on top of electrodes [113].

The contact doping is expected to enhance tunneling of charge carriers at metal-semiconductor interfaces by increasing the concentration of charge carriers near the contact region similar to the effect in silicon, and to decrease the vertical bulk resistance in the contact region by increasing the conductivity of the semiconductor film. However, the mechanism of the improvement in contact resistance by contact doping is still not well established, and the effects of contact doping in top-gate OFETs have been scarcely reported in the literature.

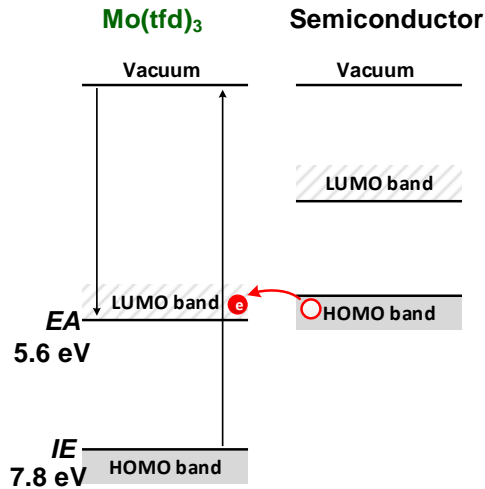


Figure 3.14. Energy band diagram of Mo(tfd)<sub>3</sub> and hole-transport organic-semiconductor materials. Adapted from [109].

In this research, two dopant materials have been adapted for contact-doped electrodes in top-gate OFETs: Mo(tfd)<sub>3</sub> and MoO<sub>3</sub>. Mo(tfd)<sub>3</sub> has been chosen since it has high electron affinity, 5.59 eV; in turn, it attracts electrons from the HOMO band of organic semiconductors to its LUMO band, being an efficient p-dopant material for hole transport

materials as illustrated in Figure 3.14 [108]. While Zhao *et al.* and Tiwari *et al.* reported Mo(tfd)<sub>3</sub>-doped p-channel organic films as an interlayer between metal electrodes and semiconductor films by co-evaporating the dopants and the semiconductor materials for bottom-gate OFETs [111, 112], using the dopant material for contact-doped electrodes has not yet been adapted in OFETs.

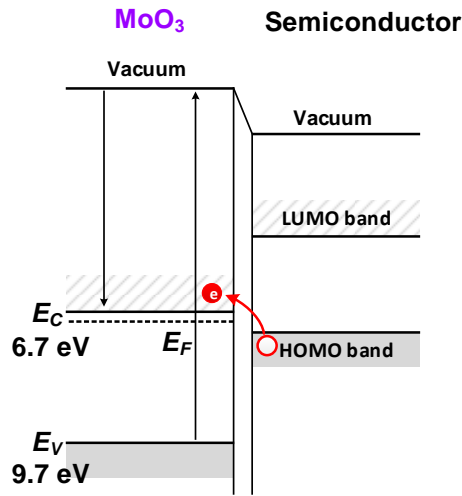


Figure 3.15. Energy band diagram of MoO<sub>3</sub> and hole-transport organic-semiconductor materials. Adapted from [102].

MoO<sub>3</sub> has been widely used as an interlayer incorporated with hole-transport materials in OLEDs and OPVs [102, 142] enhancing hole injection or collection at metal-semiconductor interfaces. Kroger *et al.* reported that the high injection/collection efficiency at the interface associated with MoO<sub>3</sub> is attributed to the high work function and the deep-lying electron affinity of MoO<sub>3</sub>, and the electron extraction from the HOMO band of adjacent semiconductors to the conduction band of MoO<sub>3</sub> induces the hole injection at the interface as presented in Figure 3.15 [102]. MoO<sub>3</sub> has also been adapted for bottom-gate OFETs either by being co-evaporated with semiconductor materials [104] or by being inserted at the interface [105] but has not been adapted for contact-doped electrodes in top-

gate OFETs. In addition, the mechanism of improving contact properties using  $\text{MoO}_3$  is still not well defined.

### 3.2.2. Device structures of top-gate OFETs with contact-doped electrodes

The top-gate OFETs with contact-doped source/drain electrodes are fabricated by evaporating  $\text{Mo}(\text{tfd})_3$  or  $\text{MoO}_3$  on electrodes in a thermal evaporator with shadow masks that are identical to masks for source/drain electrodes before solution processing of active semiconductor films.

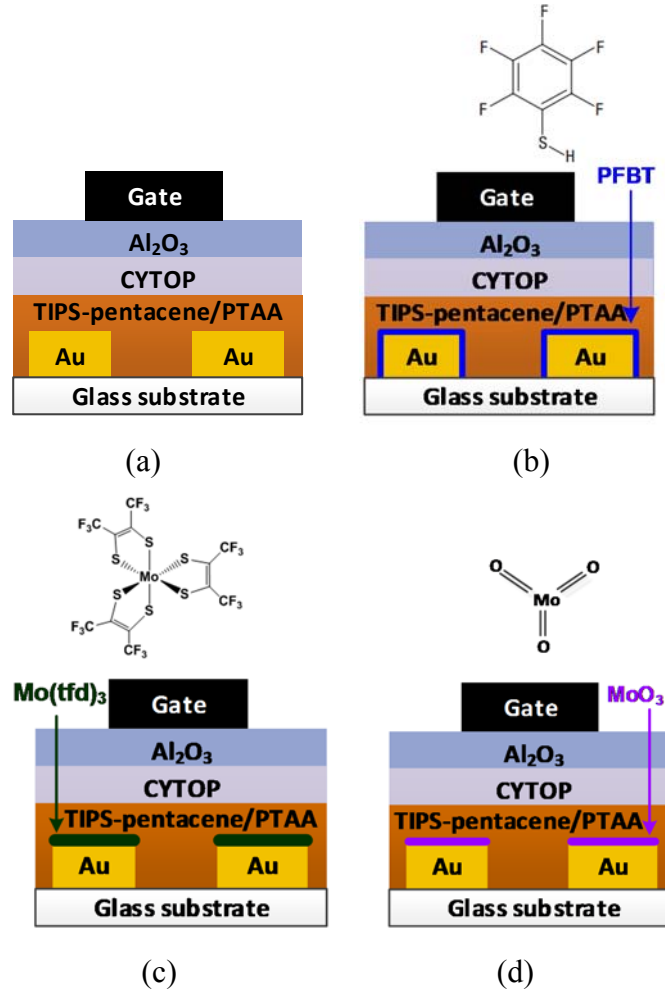


Figure 3.16. Cross-sectional view of top-gate TIPS-pentacene/PTAA OFETs with (a) bare Au, (b) Au/PFBT, (c) Au/ $\text{Mo}(\text{tfd})_3$ , and (d) Au/ $\text{MoO}_3$  electrodes.

In the experiment, top-gate OFETs having four different types of source/drain electrodes were fabricated and characterized for the comparison of their contact properties: bare Au, PFBT-treated Au or Au/PFBT, Mo(tfd)<sub>3</sub>-doped Au or Au/Mo(tfd)<sub>3</sub>, and MoO<sub>3</sub>-doped Au or Au/MoO<sub>3</sub>. The OFETs with bare Au and PFBT-treated Au are reference samples for the comparison of the OFETs with contact-doped electrodes. Figure 3.16 illustrates the cross-sectional view of each type of device structures used in this research.

### 3.2.3. Work function of electrodes

The work function values of four types of electrodes have been measured repeatedly using a Kelvin probe in a N<sub>2</sub>-filled glove box since the work function of electrodes significantly affects the injection barrier height at the interface. The measured work function values of bare Au, Au/PFBT, Au/Mo(tfd)<sub>3</sub>, and Au/MoO<sub>3</sub> are  $4.80 \pm 0.17$ ,  $5.30 \pm 0.24$ ,  $5.40 \pm 0.13$  and  $6.00 \pm 0.48$  eV, respectively, as shown in Figure 3.17 and Figure 3.18, and these work function values of each electrode will be discussed in a later part of this dissertation with the extracted contact resistance values of OFETs.

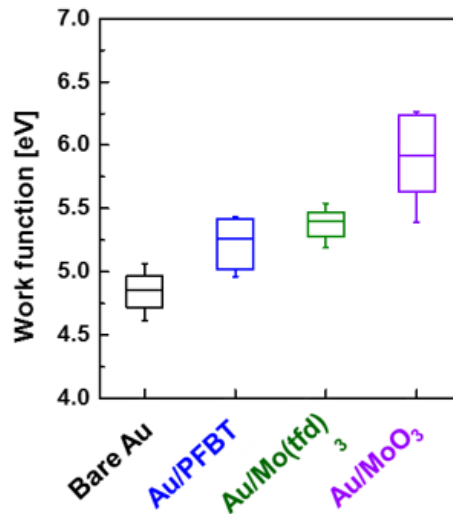


Figure 3.17. A comparison of work function values of bare Au (24 dev.), Au/PFBT (6 dev.), Au/Mo(tfd)<sub>3</sub> (11 dev.), and Au/MoO<sub>3</sub> (11 dev.) from a total of 14 batches.

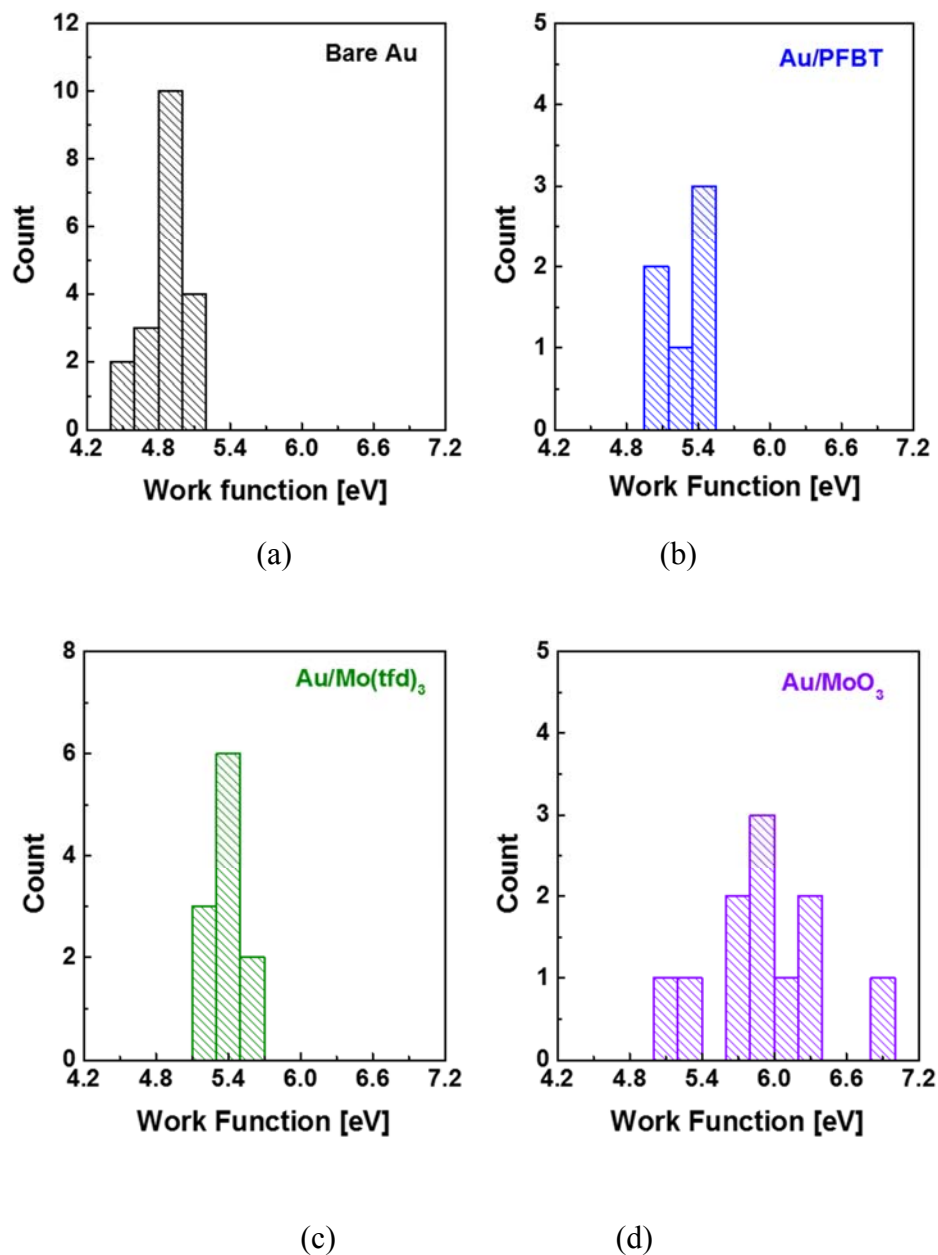


Figure 3.18. Histograms of the work function values measured on (a) bare Au, (b) Au/PFBT, (c) Au/Mo(tfd)<sub>3</sub>, and (d) Au/MoO<sub>3</sub> electrodes.

The higher variability in work function values found in Au/PFBT electrodes can be attributed to differences in electrode coverage of PFBT SAM and that in Au/MoO<sub>3</sub> to an oxygen exposure [143], which is confirmed by the measured work function values of MoO<sub>3</sub> films as a function of air exposure in Figure 3.19. On the other hand, Au/Mo(tfd)<sub>3</sub> showed

lower variability and higher air stability in its work function value with respect to the other structures.

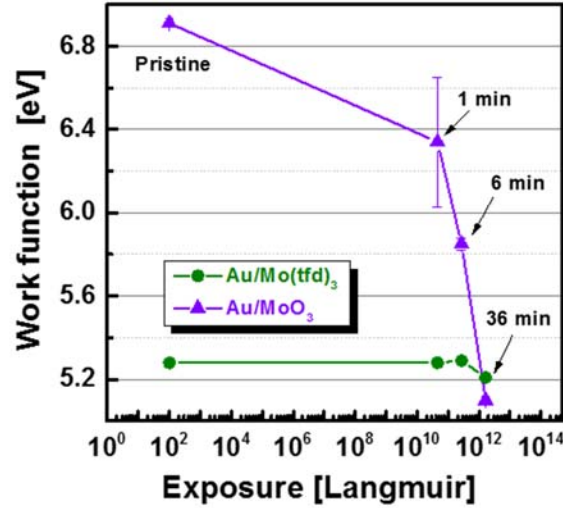


Figure 3.19. Work function shifts as a function of exposure to air.

### 3.2.4. Thin Mo(tfd)<sub>3</sub> film on electrodes

In the fabrication of the top-gate OFETs with Mo(tfd)<sub>3</sub>-doped electrodes, the TIPS-pentacene/PTAA solution is spin-coated on top of a Mo(tfd)<sub>3</sub> film, and this process step may have a chance to dissolve and remove the thin Mo(tfd)<sub>3</sub> film. In order to make sure the dopants exist on the electrodes even after the semiconductor film is solution-processed, the surface properties of the contact-doped electrodes were investigated from two points of view: The element composition on the surface was analyzed by using x-ray photoelectron spectroscopy (XPS), and the work function values of the electrodes were measured right after the dopant film is deposited, and after tetralin, which is the solvent used in the TIPS-pentacene/PTAA solution, is spin-coated on top of it with the same spin-coating recipe for the TIPS-pentacene/PTAA film.

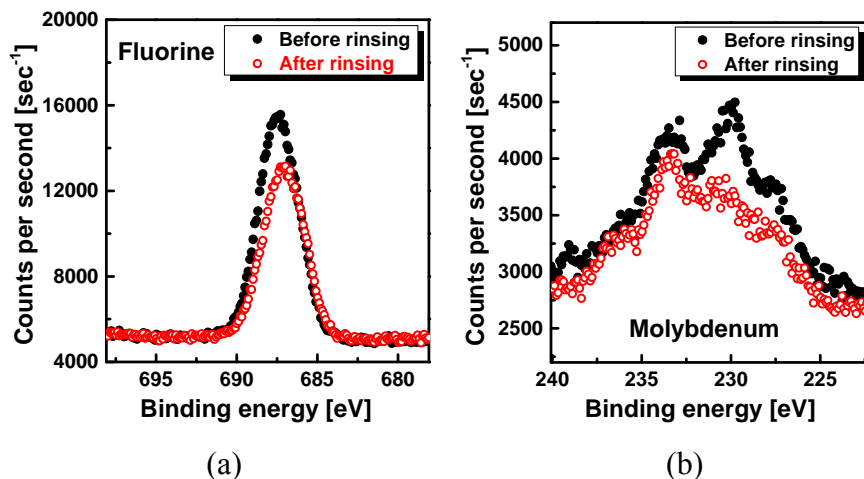


Figure 3.20. X-ray photoelectron spectroscopy data of (a) Fluorine and (b) Molybdenum measured from a  $\text{Mo}(\text{tfd})_3$  film on electrodes.

The XPS data shown in Figure 3.20 indicate that some  $\text{Mo}(\text{tfd})_3$  molecules on the surface are rinsed away by spin-coating tetralin but still a significant amount of  $\text{Mo}(\text{tfd})_3$  stays on the surface of the electrodes. The work function values of the electrodes before and after spin-coating tetralin shown in Figure 3.21 also lead us to the same conclusion since the difference in the values is not noticeable in the result.

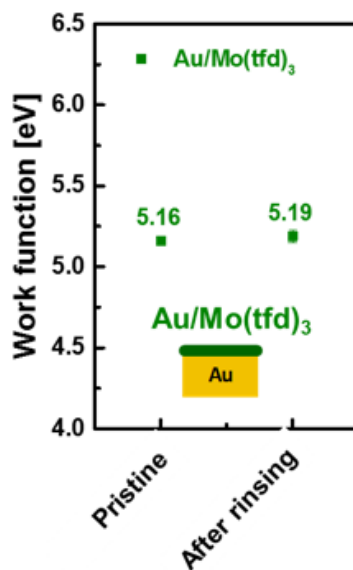


Figure 3.21. Work function values of  $\text{Au}/\text{Mo}(\text{tfd})_3$  before and after spin-coating tetralin on top of the electrodes.



Another observation from these results is that the  $\text{Mo}(\text{tfd})_3$  molecules that come off from the surface may be located in the bulk of host material during the spin-coating and annealing of TIPS-pentacene/PTAA films, resulting in the increase of film conductivity which will be discussed in the later sections.

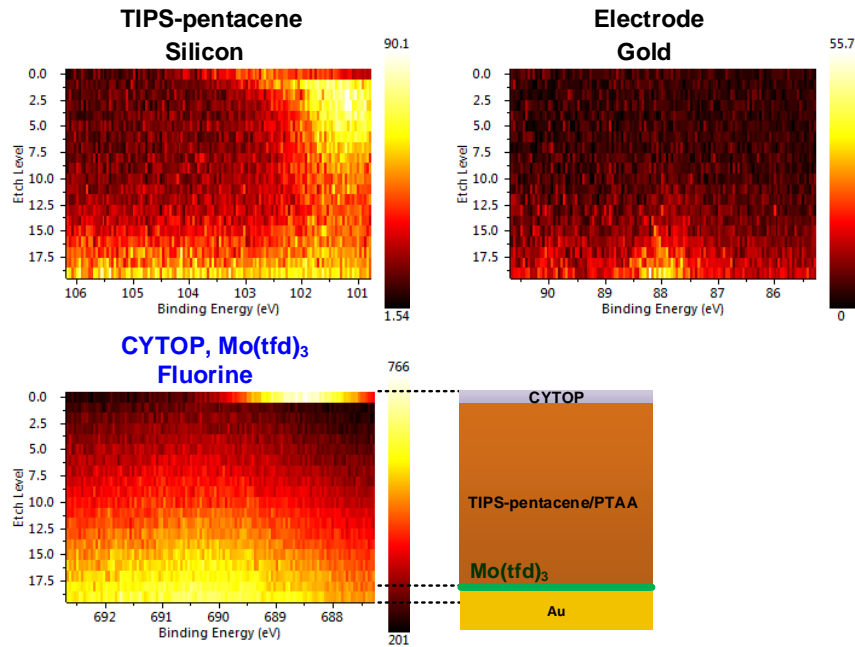


Figure 3.22. Depth profile of silicon, gold, and fluorine in a TIPS-pentacene/PTAA film on  $\text{Au}/\text{Mo}(\text{tfd})_3$  measured by XPS.

However, any solid evidence that indicates  $\text{Mo}(\text{tfd})_3$  molecules are distributed or diffused into the TIPS-pentacene/PTAA film was found from a depth profile measured by XPS, which is presented in Figure 3.22. These results indicate that  $\text{Mo}(\text{tfd})_3$  remains on the surface of the film [109], or that the concentration of  $\text{Mo}(\text{tfd})_3$  in the bulk of the semiconductor film is too low to be detected by an XPS measurement. Even if one assumes that the  $\text{Mo}(\text{tfd})_3$  molecules do not diffuse in the semiconductor film, and are mostly located near contacts, the hole carriers that are generated by doping at the contacts diffuse into the bulk of the host materials, known as the remote-doping effect, which was reported by Zhao *et al.* [112].

### 3.2.5. Current-voltage characteristics of the top-gate OFETs

The current-voltage characteristics of the top-gate OFETs with four types of source/drain electrodes shown in Figure 3.16 have been evaluated from two batches of OFETs (10 dev.) with bare Au, seven batches (138 dev.) of OFETs with Au/PFBT, eight batches of OFETs (61 dev.) with Au/Mo(tfd)<sub>3</sub>, and six batches of OFETs (51 dev.) with Au/MoO<sub>3</sub> electrodes.

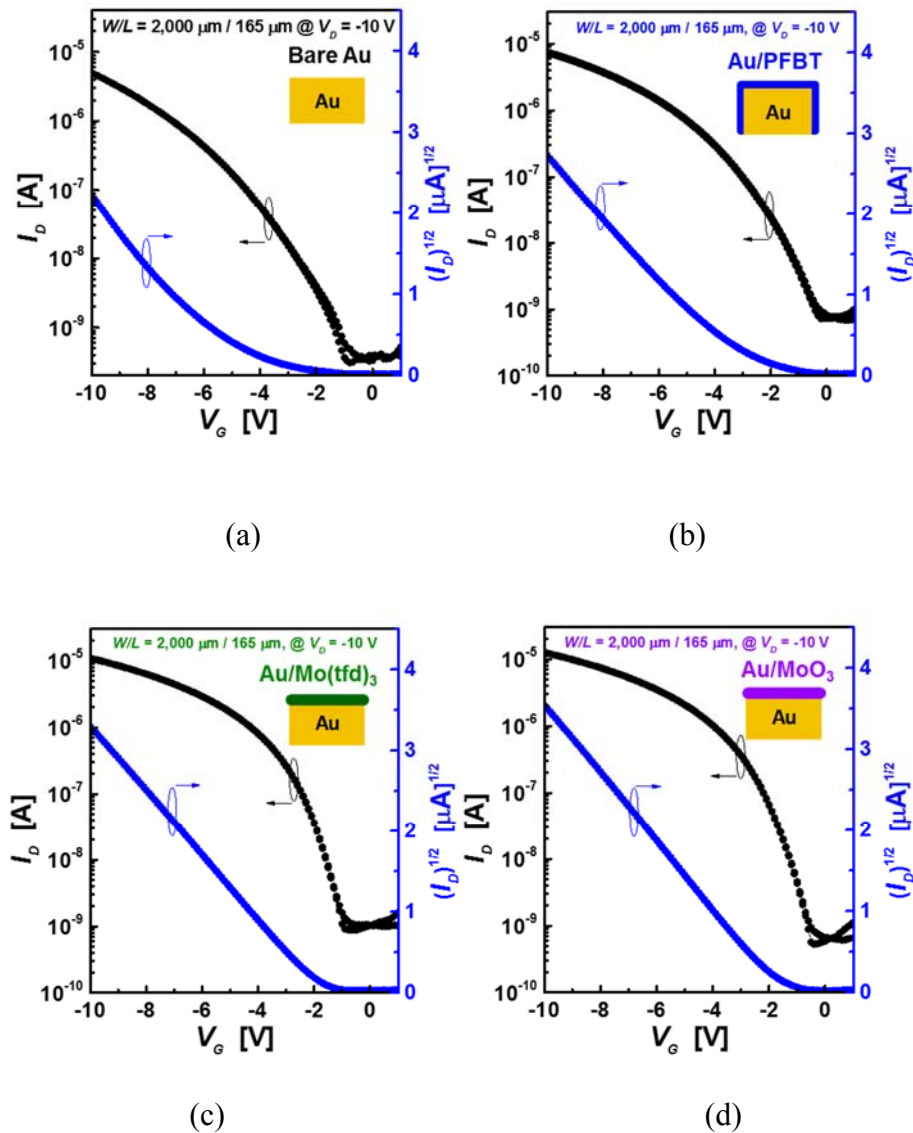


Figure 3.23.  $I$ - $V$  transfer characteristics measured from top-gate TIPS-pentacene/PTAA OFETs with (a) bare Au, (b) Au/PFBT, (c) Au/Mo(tfd)<sub>3</sub>, and (d) Au/MoO<sub>3</sub> electrodes.

Figure 3.23 displays  $I$ - $V$  transfer characteristics measured from OFETs of each device structures in the same batch. In these results, the OFETs with PFBT-treated Au electrodes display better square law behavior (as shown by the straight line behavior in the plot as a function of the square-root curve of  $I_D$  in the saturation region) compared with devices with bare Au electrodes. Note however, that the  $I$ - $V$  characteristics from the OFETs with contact-doped gold electrodes (Au/Mo(tfd)<sub>3</sub> and Au/MoO<sub>3</sub>) comply even better with the square law approximation of ideal field-effect transistors, and the difference is particularly significant at small- $V_G$  bias conditions. In addition, while the field-effect mobility of the OFETs does not show a notable difference in the statistical data shown in Figure 3.24(b), the threshold voltage values of the top-gate TIPS-pentacene/PTAA OFETs with contact-doped electrodes are considerably smaller than the OFETs with PFBT-treated Au electrodes on average by ca. 2 V as shown in Figure 3.24(a) and Figure 3.25.

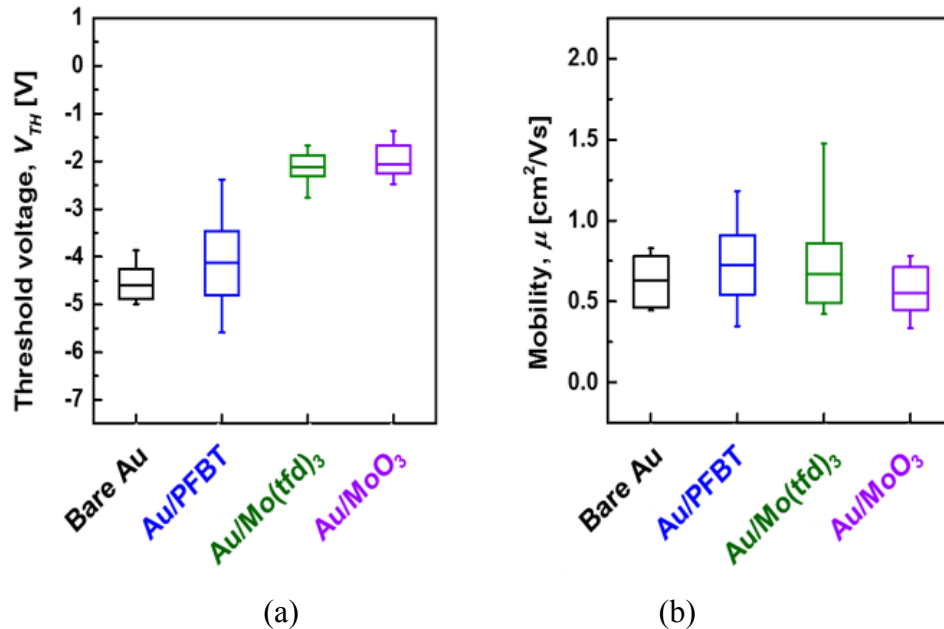


Figure 3.24. Statistics of (a) threshold voltages, (b) field-effect mobility values, and (c) width-normalized off-current of TIPS-pentacene/PTAA OFETs with the four different types of source/drain electrodes.

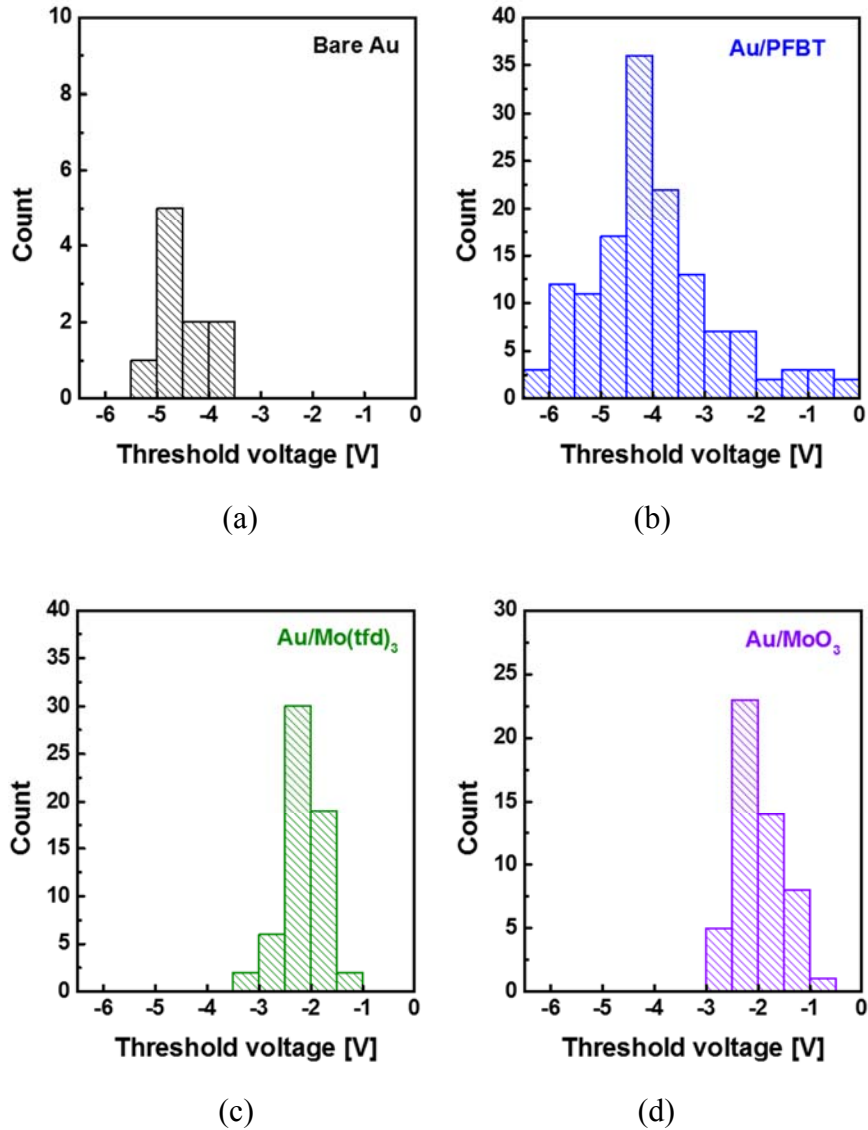


Figure 3.25. Histograms of  $V_{TH}$  values of top-gate TIPS-pentacene/PTAA OFETs with (a) bare Au, (b) Au/PFBT, (c) Au/Mo(tfd)<sub>3</sub>, and (d) Au/MoO<sub>3</sub> electrodes.

The small  $V_{TH}$  values in the OFETs with contact-doped electrodes should decrease the contact resistance at a given  $V_G$  condition, which will be demonstrated at the later part of this study, by increasing the effective gate bias,  $|V_{GS} - V_{TH}|$ . However, it is not yet clear whether the small  $V_{TH}$  induces the lower contact resistance of the OFETs or the doping effects and low contact resistance are leading to the small  $V_{TH}$  values. Another observation is the gradual decrease of the mobility values of the OFETs with bare Au electrodes as the

channel length decreases, which is shown in Figure 3.26. This result suggests that the current driving capability of the OFETs is strongly limited by the contact resistance when the channel length is shorter than 215  $\mu\text{m}$ , whereas the other three types of OFETs do not show the same issue. In addition, the nonlinear dependence of  $I_D$  in the output characteristics of the OFETs with bare Au and Au/PFBT in the batch when  $V_D$  approaches 0 V, as shown in Figure 3.27, also indicates that both bare Au and PFBT-treated Au electrodes create considerable amount of contact resistance in the device.

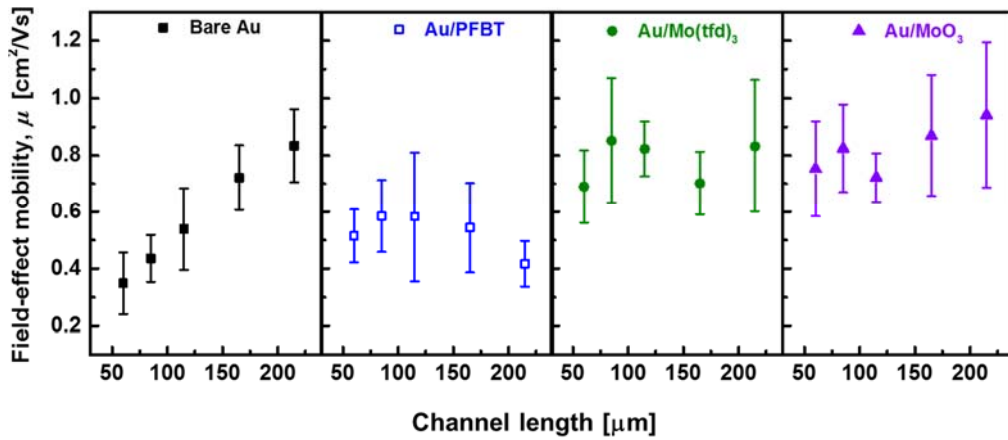


Figure 3.26. Dependence of field-effect mobility values on the channel length.

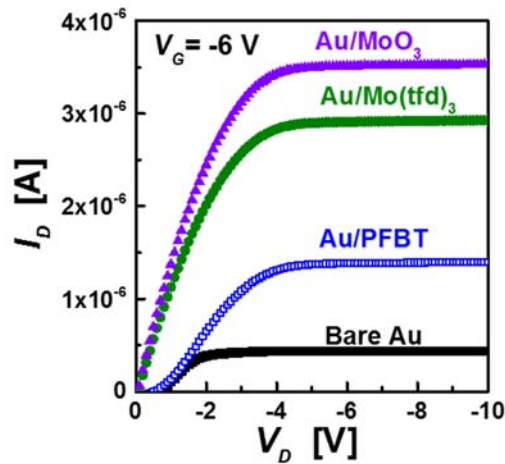


Figure 3.27. Comparison of output characteristics of OFETs at  $V_G = -6\text{ V}$ .

### 3.2.6. Contact resistance of OFETs with contact-doped electrodes

The contact resistance of the OFETs has been extracted by TLMs. The channel length of the OFETs has varied from 60  $\mu\text{m}$  to 215  $\mu\text{m}$  (60, 85, 115, 165, and 215  $\mu\text{m}$ ) with a common channel width of 2,000  $\mu\text{m}$ , and the extraction of the contact resistance has been performed at three different  $V_G$  values, -4, -6, and -8 V.

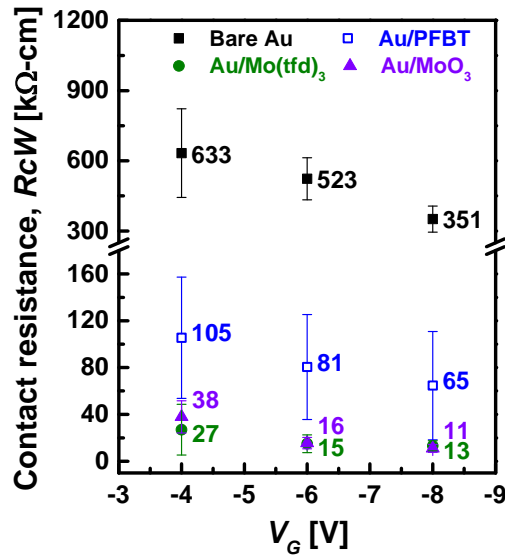


Figure 3.28. Width-normalized contact resistance of OFETs having bare Au, Au/PFBT, Au/Mo(tfd)<sub>3</sub>, and Au/MoO<sub>3</sub> electrodes.

Figure 3.28 displays the width-normalized contact resistance,  $R_{cW}$ , of the OFETs, and this result shows that the devices with Au/PFBT, Au/Mo(tfd)<sub>3</sub>, and Au/MoO<sub>3</sub> electrodes have 6, 35, and 33 times smaller contact resistance than the devices having bare Au electrodes on average values when  $V_G$  is -6 V, respectively. In addition,  $R_{cW}$  of the OFETs with contact-doped electrodes is noticeably lower than those from the OFETs with PFBT-treated electrodes regardless of gate voltage bias, which is in good agreement with the observation from their  $I$ - $V$  characteristics. The contact resistance of OFETs with Mo(tfd)<sub>3</sub>-doped electrodes was found to have the lowest contact resistance on average but

the difference between the effects of Au/Mo(tfd)<sub>3</sub> and Au/MoO<sub>3</sub> is not clear regarding the standard deviation in the result.

### 3.2.6.1 Dependence of contact resistance on the work function of electrodes

The dependence of contact resistance on the work function of electrodes in the OFETs was investigated by fabricating multiple batches of the OFETs and being plotted as a function of work function of electrodes as presented in Figure 3.29.

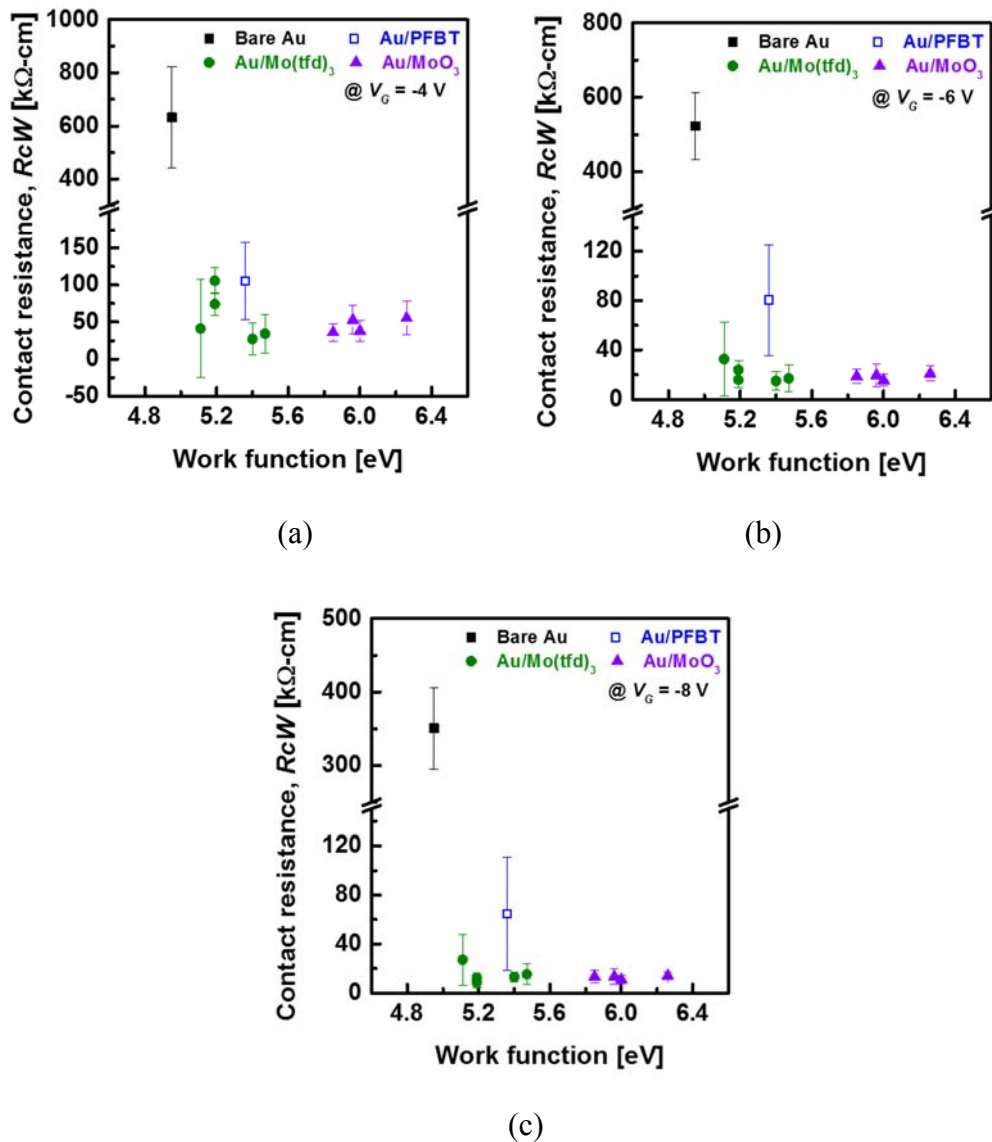


Figure 3.29 Width-normalized contact resistance with respect to the work function values of source/drain electrodes at (a)  $V_G = -4$  V, (b)  $V_G = -6$  V, and (c)  $V_G = -8$  V.

The result shows that the contact resistance decreases significantly as the work function of electrodes increases until it reaches a certain level of a work function value. On the other hand, the contact resistance of OFETs with Au/Mo(tfd)<sub>3</sub> is exceptionally lower than those of OFETs with Au/PFBT even though the work function values of Au/PFBT in the OFETs are higher than that of Au/Mo(tfd)<sub>3</sub>, and we discuss the result with regard to p-doping effects in a later section of this dissertation.

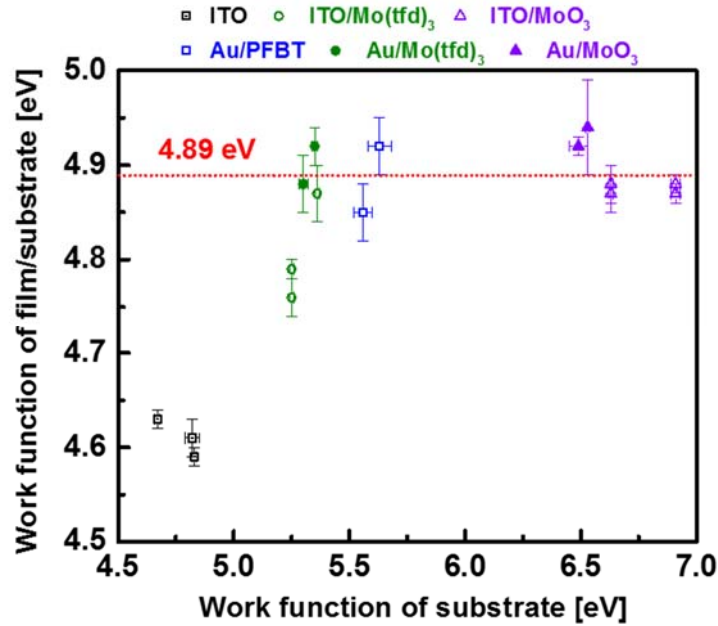


Figure 3.30. Dependence of TIPS-pentacene/PTAA work function on substrate work function measured by a Kelvin probe in a N<sub>2</sub>-filled glove box.

Since the injection barrier height for hole carriers at the interface between metal and p-channel (or hole transport) materials is the energy level difference between the ionization energy (IE) and the work function of electrodes, the higher the work function values, in general, the lower the barrier height is after the energy level alignment at interfaces. However, as stated in section 3.1.3.2, it is well established that if the work function of an electrode is beyond a certain critical value, known as the pinning level, the energetic barrier height at the contact remains fixed. For instance Davis *et al.* [118]



measured the work function of samples comprising a thin TIPS-pentacene film on conductive substrates having different work function values and found that the work function of the TIPS-pentacene/substrate samples remained being pinned at  $4.80 \pm 0.11$  eV. In the same manner, the pinning level of Fermi level energy of a PTAA-blended TIPS-pentacene film in this study has been investigated by measuring the work function values of the films on conductive substrates, ITO, ITO/Mo(tfd)<sub>3</sub>, ITO/MoO<sub>3</sub>, Au/PFBT, Au/Mo(tfd)<sub>3</sub>, and Au/MoO<sub>3</sub> using a Kelvin probe in a N<sub>2</sub>-filled glove box. In this experiment, the Fermi level pinning of TIPS-pentacene/PTAA films occurred at  $4.89 \pm 0.09$  eV as displayed in Figure 3.30. Since the IE of TIPS-pentacene is reported as 5.2 eV [118], and PTAA also reportedly has identical IE values [144], the measured pinning level of a TIPS-pentacene/PTAA in this study is in good agreement with those previously reported values.

Considering Fermi level pinning at the metal-semiconductor interface, the barrier height for hole carriers injected from Au/PFBT, Au/Mo(tfd)<sub>3</sub>, and Au/MoO<sub>3</sub> to TIPS-pentacene/PTAA is expected to be similar, and so does the corresponding contact resistance. Instead, the reduction in contact resistance observed in the OFETs comprising Au/Mo(tfd)<sub>3</sub> and Au/MoO<sub>3</sub> electrodes can be primarily attributed to a combination of increase in work function of the electrode and the decrease of bulk conductivity near the metal-semiconductor contacts by either p-doping of the semiconductor layer or a change of the film morphology.

### 3.2.6.2 Vertical bulk resistance in contact area

The bulk resistance of the top-gate OFETs has been evaluated by three methods: measuring the sheet resistance of TIPS-pentacene/PTAA films, extracting the bulk

conductivity from capacitance-frequency characteristics, and extracting the bulk resistance from the measured contact/channel resistance by HSPICE simulation.

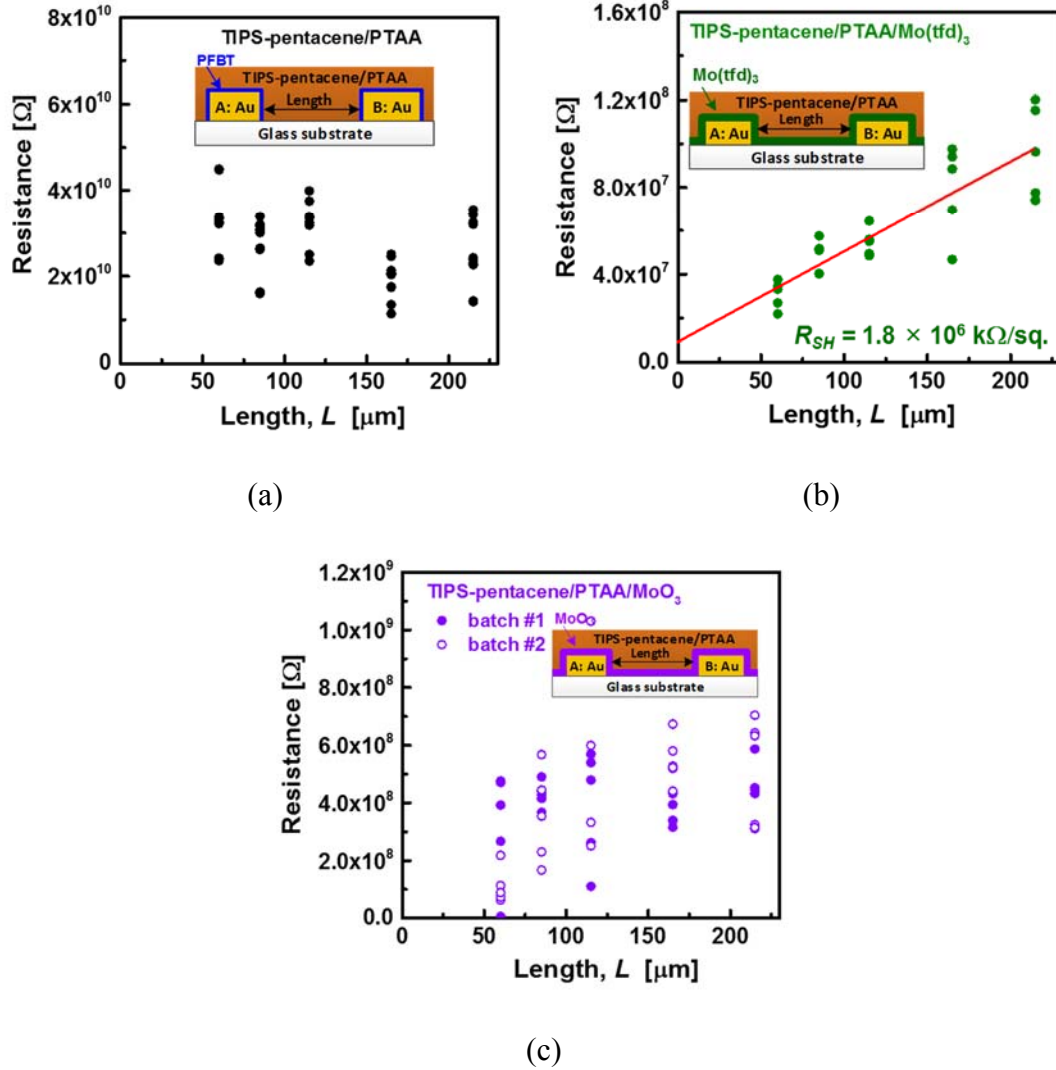


Figure 3.31. Device structures (inset figures) and the measured resistance values of thin-film resistors consisting of (a) a pristine, (b)  $\text{Mo}(\text{tfd})_3$ -doped, and (c)  $\text{MoO}_3$ -doped TIPS-pentacene/PTAA films as a function of their length.

The sheet resistance of a contact-doped TIPS-pentacene/PTAA film has been evaluated from sheet resistors, shown in cross-sectional views, insets of Figure 3.31(b), and (c), by spin-coating TIPS-pentacene/PTAA solution on a substrate covered with  $\text{Mo}(\text{tfd})_3$  or  $\text{MoO}_3$ . From the experiment, the contact-doped films showed about four orders

and two orders of magnitude lower resistance than that of an un-doped TIPS-pentacene/PTAA film shown in Figure 3.31(a). Since the resistance of a thin layer of Mo(tfd)<sub>3</sub> or MoO<sub>3</sub> that does not accompany the host material was measured about five times and 100 times higher resistance than that of an un-doped TIPS-pentacene/PTAA film, respectively, the decrease in resistance of the contact-doped film is attributed to the doping of the semiconductor film. From the result, the sheet resistance of a Mo(tfd)<sub>3</sub>-doped TIPS-pentacene/PTAA film was extracted as  $1.8 \times 10^6$  kΩ/square by TMLs whereas that of a MoO<sub>3</sub>-doped TIPS-pentacene/PTAA and an un-doped film could not be extracted because of the wide spread in their values leading to inaccurate linear-fitting. It is worth to note that, unlike other studies that use doping the bulk of host materials with Mo(tfd)<sub>3</sub> by co-evaporation, this result indicates that contact-doping using Mo(tfd)<sub>3</sub> associated with solution-processed organic semiconductors also increases the bulk conductivity of the host materials. The fact that the resistance of a MoO<sub>3</sub>-doped film is measured relatively higher than that of a Mo(tfd)<sub>3</sub>-doped film suggests the possibility of the bulk doping of host materials by Mo(tfd)<sub>3</sub> molecules that are dissolved by tetralin and relocated in the bulk during the spin-coating process of TIPS-pentacene/PTAA solution, decreasing the sheet resistance in addition to the contact-doping effect.

The carrier concentration of TIPS-pentacene/PTAA films when doped with Mo(tfd)<sub>3</sub> was calculated based on the measured sheet resistance using:

$$\rho = \frac{1}{q(\mu_n n + \mu_p p)} = \frac{1}{q\mu_p p} \quad (3.7)$$

when the hole concentration,  $p$ , is much higher than the electron concentration,  $n$ , by p-doping, where  $\rho$  is the resistivity of the film,  $q$  is the charge of electrons,  $\mu_n$  is the mobility value of electrons,  $\mu_p$  is the mobility value of holes in the bulk, and the hole

concentration of the doped semiconductor film is calculated as ca.  $1 \times 10^{15} /\text{cm}^3$  from the measured resistivity value 12.2 k $\Omega$  cm.

Table 3.1. Values of physical and electrical properties of TIPS-pentacene/PTAA films used in the calculation of the carrier concentration of Mo(tfd)<sub>3</sub>-doped TIPS-pentacene/PTAA films.

Density of film	Molecular weight	Density of state	Hole mobility
1.3 g/cm <sup>3</sup>	639 g	$1.2 \times 10^{21} /\text{cm}^3$	0.5 cm <sup>2</sup> /Vs
Thickness of film	IE	EA	E <sub>F</sub>
70 nm	5.2 eV	3.6 eV	4.4 eV

The Fermi level energy is also calculated from:

$$E_i - E_F = kT \ln \frac{N}{n_i} \quad (3.8)$$

where  $E_i$  is the intrinsic carrier concentration calculated with the approximate values in Table 3.1,  $E_F$  is the Fermi level energy of doped films,  $k$  is the Boltzmann constant,  $T$  is the absolute temperature, and  $N$  is the dopant concentration, which is approximately the same as the hole carrier concentration calculated in Equation (3.7). Using the hole concentration of the film above, the estimated Fermi level energy of the film is derived to be 4.84 eV, which is close to the pinned Fermi level energy presented in Figure 3.30.

The conductivity of TIPS-pentacene/PTAA films on electrodes was also evaluated from their capacitance-frequency ( $C$ - $F$ ) characteristics that are measured from the capacitor structure described in Figure 3.32(a), which is the capacitor formed between gate and source/drain electrodes of the OFETs. From the  $C$ - $F$  characteristics of the series-connected two capacitors ( $C_{INS}$ , which is the gate-dielectric capacitor, and  $C_s$ , which is the depletion capacitor of the semiconductor film illustrated),  $C_s$  was calculated by eliminating

the portion of  $C_{INS}$ , whose value was calculated by the capacitance density of the gate dielectrics,  $30 \text{ nF/cm}^2$ , and the area of a gate-source/drain overlap in the OFET,  $A$ . The conductivity of the semiconductor film at a given frequency,  $\rho(f)$ , was calculated by the following equation:

$$\rho(f) = 2\pi f D(f) \frac{C_S d}{A \epsilon_0} \quad (3.9)$$

where  $f$  is the frequency,  $D(f)$  is the dissipation factor of a given frequency,  $d$  is the thickness of the semiconductor film measured by a confocal microscope on a separate sample, and  $\epsilon_0$  is the permittivity of free space.

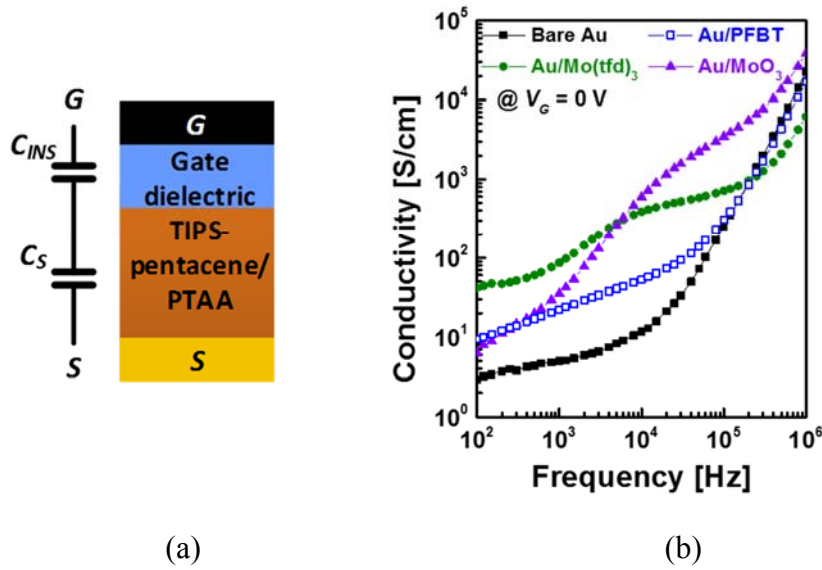


Figure 3.32. (a) Cross-sectional view of a series-connected capacitor between gate and source/drain electrodes in the top-gate OFETs, and (b) calculated conductivity of the semiconductor films on contacts as a function of an applied signal frequency.

Figure 3.32(b) presents the conductivity of TIPS-pentacene/PTAA films that is calculated from the measured  $C$ - $F$  characteristics as a function of an applied signal frequency. In this result, the higher conductivity values of the contact-doped films at lower frequency regime than those of un-doped films qualitatively imply that the contact-doped

films have a higher carrier concentration than the un-doped films, and it is in good agreement with the extracted contact resistance result in Figure 3.29.

### 3.2.6.3 Simulation of bulk resistance

While contact resistance consists of the injection and bulk resistance as explained in section 3.1.3, TLM experiments can be used to extract only the total contact resistance in the device. Therefore, the evaluation of the vertical bulk resistance in the total contact resistance requires extraction of the bulk resistance component from the total contact resistance that was measured from the devices, and in this research HSPICE simulation has been applied for the extraction with a simplified contact resistance model shown in Figure 3.34(a).

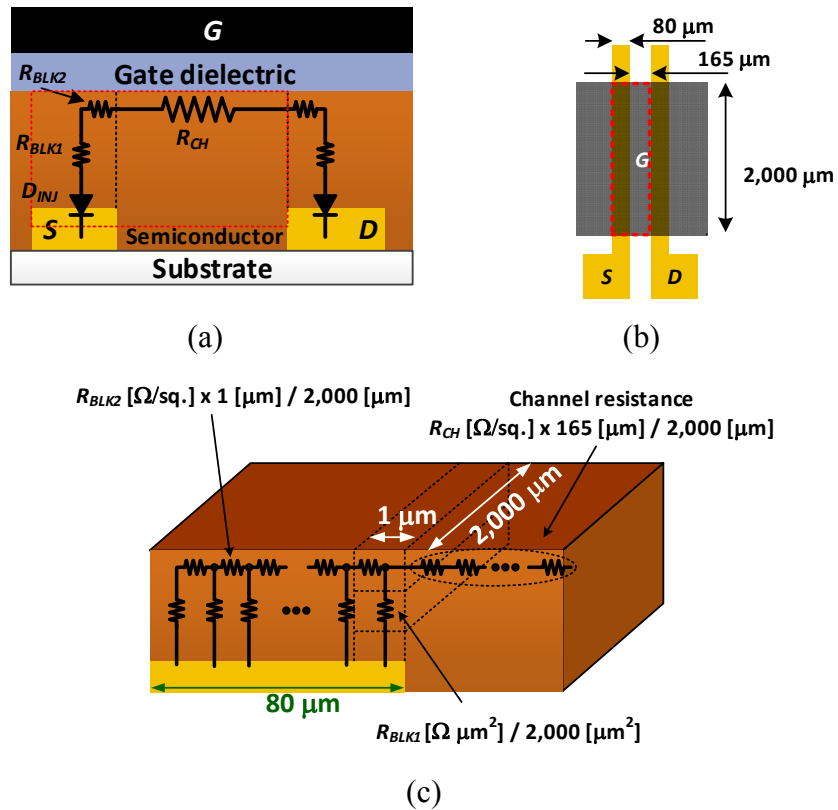


Figure 3.33. Device modeling for HSPICE simulation assuming the injection diode at contacts,  $D_{INJ}$ , is equally negligible for all cases, (a) cross-sectional view of on-resistance and (b) top view of device; and simulation results, (c) the distributed model of bulk resistance used in the simulation.

In the simple model,  $R_{CH}$  is the channel resistance,  $R_{BLK1}$  is the vertical bulk resistance,  $R_{BLK2}$  is the horizontal bulk resistance that is induced by the gate voltage bias, and  $D_{INJ}$  is the injection diode that is induced by the energy barrier height at the interface. The diode is assumed to have a zero series resistance in the simulation, since the work function values of the source/drain electrodes (Au, Au/PFBT, Au/Mo(tfd)<sub>3</sub>, and Au/MoO<sub>3</sub>) are higher than the pinning level of a TIPS-pentacene/PTAA film, 4.89 eV. The distributed element model has been applied in this HSPICE simulation reflecting the gradual change of vertical bulk current,  $I_{BLK}$ , in the contact area as shown in Figure 3.33(c). The contact area is divided into 80 slices of 2,000  $\mu\text{m}$  by 1  $\mu\text{m}$  sub-cells for both  $R_{BLK1}$  and  $R_{BLK2}$ , in which  $R_{BLK2}$  has the same sheet resistance as the channel sheet resistance because both of them are induced by the gate voltage bias. By applying the channel sheet resistance and the total contact resistance at source and drain electrodes, which were extracted from TLMs, the distribution of vertical current,  $I_{BLK\_nth}$ , at  $n$ th position resistor,  $R_{BLK1\_nth}$ , has been extracted, and the vertical bulk resistance,  $R_{BLK1}$ , was derived from the simulation results as shown in Figure 3.34.

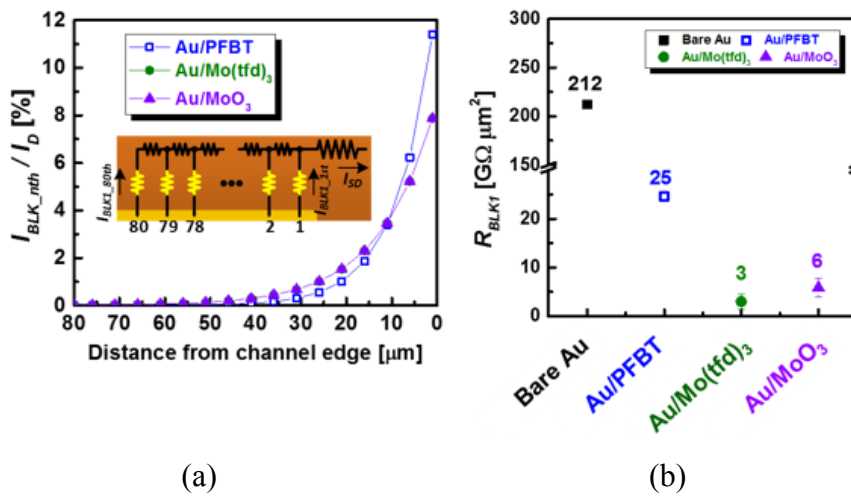


Figure 3.34. (a) The distribution of bulk resistance and (b) simulated bulk resistance values of the OFETs with four different source/drain electrodes.

This simulation result presents that the vertical resistance,  $R_{BLKI}$ , in the semiconductor film on Mo(tfd)<sub>3</sub>-doped, and MoO<sub>3</sub>-doped electrodes are about eight times and four times smaller, respectively, than that on PFBT-treated electrodes.

### 3.2.6.4 Thickness and morphology of semiconductors on contact-doped electrodes

Other important factors that affect bulk resistance at contacts is the thickness and the morphology of the semiconductor film. The water contact angle that was measured on each electrode, which is shown in Table 3.2, shows that bare Au, Au/PFBT, and Au/Mo(tfd)<sub>3</sub> have similar surface energy values while Au/MoO<sub>3</sub> has significantly higher surface energy than other configurations.

Table 3.2. Water contact angle on electrodes.

Bare Au	Au/PFBT	Au/Mo(tfd) <sub>3</sub>	Au/MoO <sub>3</sub>
75 ± 1.6 °	71 ± 4.0 °	73 ± 6.2 °	13 ± 0.4 °

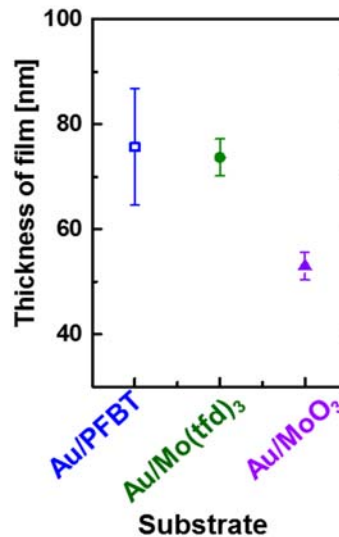


Figure 3.35. Comparison of film thickness of TIPS-pentacene/PTAA on electrodes (measured by a confocal microscope).



As a result, the measured thickness of the TIPS-pentacene/PTAA film deposited on Au/MoO<sub>3</sub> was found to have the lowest thickness among them with a difference ca. 20 nm as presented in Figure 3.35, and this result suggests that the thin layer of TIPS-pentacene/PTAA on contacts, in other words, the short length of vertical bulk resistors contributes to the reduction of contact resistance of the OFETs with Au/MoO<sub>3</sub> electrodes.

The microscope images of the morphologies of TIPS-pentacene/PTAA films on each electrode were captured by a polarized-light microscope as presented in Figure 3.36, and a notable difference in the crystallinity of the film on Au/Mo(tfd)<sub>3</sub> electrodes was observed, which suggests changes in the morphology of the semiconductor film with the Mo(tfd)<sub>3</sub>-doped electrodes in the OFETs. However, it is still unclear what induced the morphology difference on Mo(tfd)<sub>3</sub>-doped electrodes and how much it contributes to the change of contact resistance in the top-gate TIPS-pentacene/PTAA OFETs. Further analysis of the morphology change will be continued in future work.

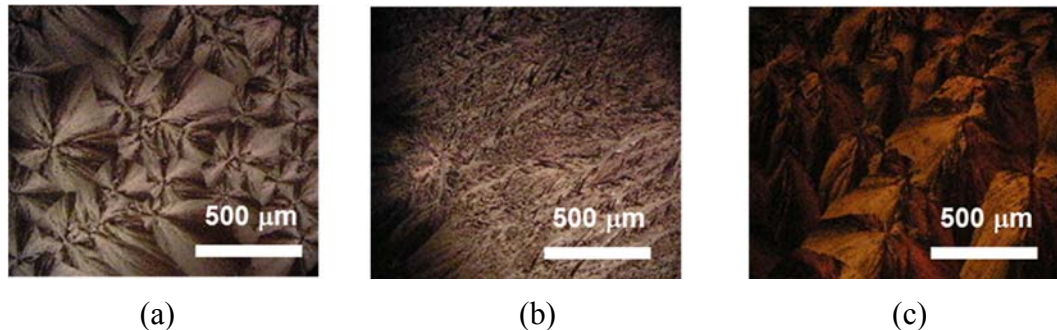


Figure 3.36. TIPS-pentacene/PTAA film morphologies on (a) Au/PFBT, (b) Au/Mo(tfd)<sub>3</sub>, and (c) Au/MoO<sub>3</sub>.

### 3.2.7. Contact resistance on low-cost electrodes

Silver and aluminum have been adapted to top-gate geometry as source/drain electrodes for exploring the possibility of using the relatively low-cost materials instead of gold. In general, silver and aluminum are not proper source/drain electrodes for p-channel

transistors since they have small work function values, 4.7 eV and 3.4 eV, respectively, making a high energy barrier height at the metal-semiconductor interfaces. As a result, p-channel OFETs with bare silver and bare aluminum source/drain electrodes exhibited poor  $I$ - $V$  characteristics as shown in Figure 3.37.

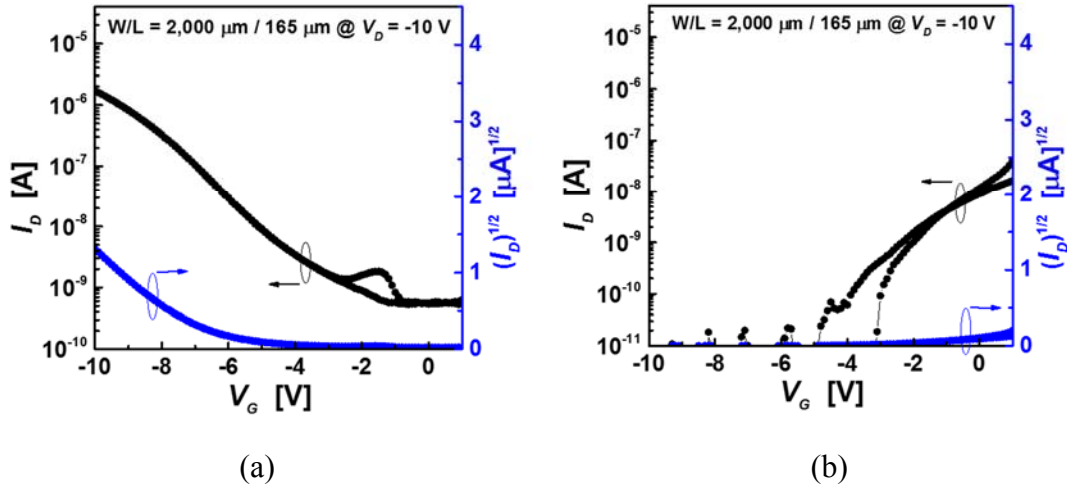


Figure 3.37.  $I$ - $V$  Transfer characteristics of top-gate TIPS-pentacene/PTAA OFETs with (a) bare silver and (b) bare aluminum source/drain electrodes.

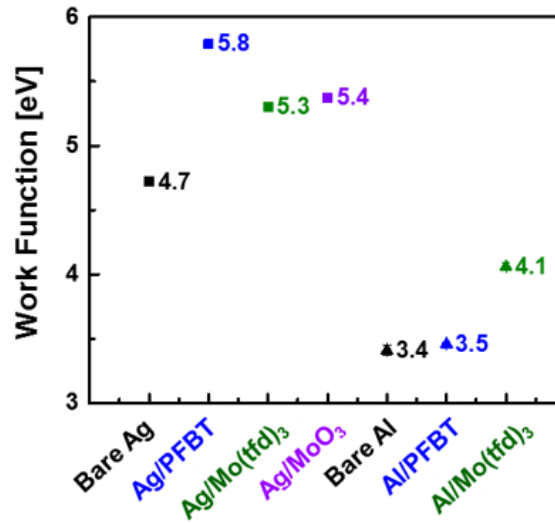


Figure 3.38. Work function changes of silver and aluminum with a PFBT treatment and contact-doping.

The work function values of silver and aluminum with a PFBT treatment and contact doping, which is presented in Figure 3.38, indicate: both a PFBT treatment and contact doping effectively increase the work function of silver electrodes; but the work function values of aluminum do not reach the pinning level of Fermi level energy of TIPS-pentacene/PTAA by either a PFBT treatment or contact doping although Mo(tfd)<sub>3</sub>-doped aluminum electrodes showed increased work function values by about 0.6 eV.

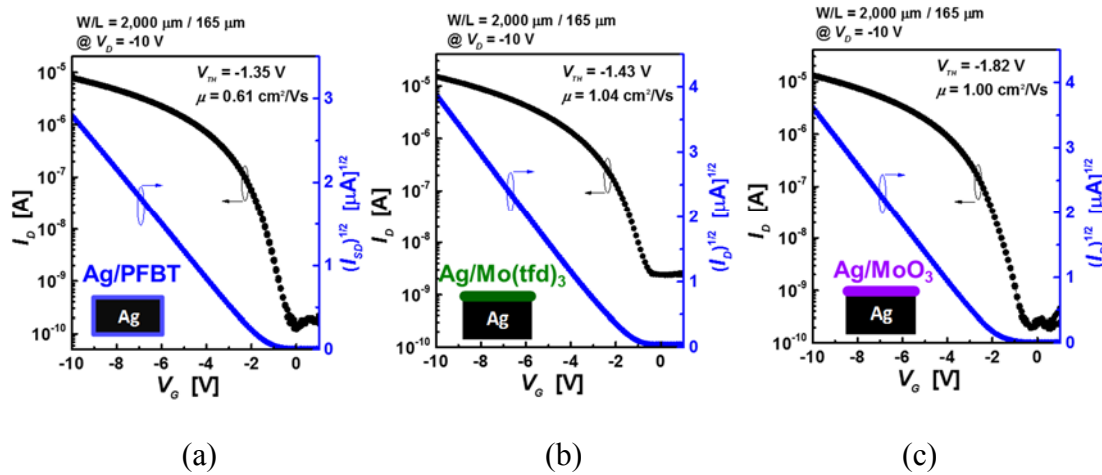


Figure 3.39 The transfer characteristics of the top-gate OFETs with (a) PFBT-treated silver, (b) Mo(tfd)<sub>3</sub>-doped silver, and (c) MoO<sub>3</sub>-doped silver for source/drain electrodes

As expected from the work function values of silver electrodes, both a PFBT-treatment and contact doping improved  $I$ - $V$  characteristics of the OFETs as shown in Figure 3.39. In the case of Ag/PFBT electrodes, the high work function of the electrodes, which is close to that of Au/MoO<sub>3</sub>, is expected to induce doping effects similar to that from MoO<sub>3</sub> at the interface, decreasing the contact resistance to 19 kΩcm when  $V_G$  is -6 V (extracted by TLMs) as presented in Figure 3.40.

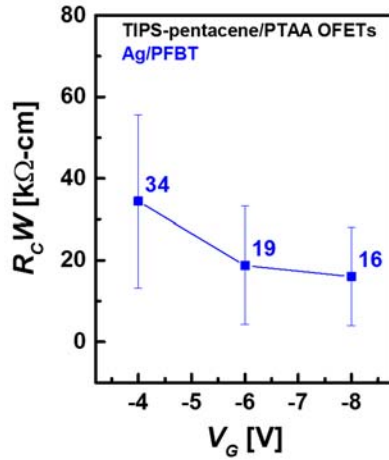


Figure 3.40. Width-normalized contact resistance,  $R_c W$ , of top-gate TIPS-pentacene/PTAA OFETs with PFBT-tread silver electrodes.

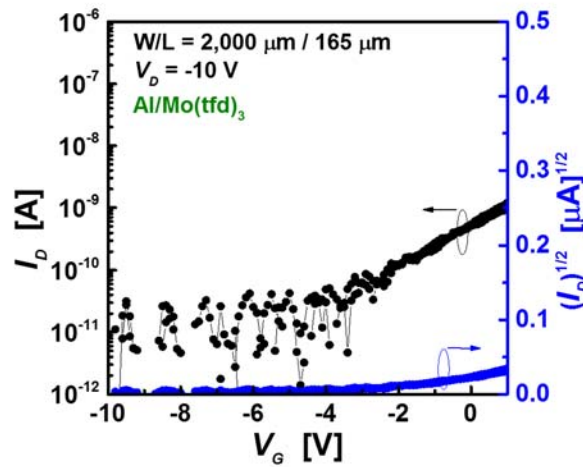


Figure 3.41.  $I$ - $V$  transfer characteristics of top-gate TIPS-pentacene/PTAA OFETs with  $\text{Mo}(\text{tfd})_3$ -doped aluminum electrodes.

On the other hand, the OFETs with contact-doped aluminum electrodes did not perform as p-channel OFETs as shown in Figure 3.41 because of the high energy barrier height at the interface as anticipated from the work function values.

### 3.2.8. Conclusions

The top-gate TIPS-pentacene/PTAA p-channel OFETs that are contact-doped by Mo(tfd)<sub>3</sub> and MoO<sub>3</sub> on source/drain electrodes were suggested and demonstrated in this research. The OFETs display significantly reduced contact resistance in comparison to the OFETs with bare Au and PFBT-treated Au electrodes, and their performance has been presented by demonstrating  $I$ - $V$  characteristics and extracting  $RcW$  values. Regarding Fermi level pinning, the improved contact resistance does not result only from the higher work function values of source/drain electrodes but a combination of lowering barrier height, shrinking  $V_{TH}$  values, and reducing the bulk resistance in the vicinity of contacts by p-doping of the host material. Particularly, the reduction of bulk resistance has been investigated by a direct extraction of the sheet resistance of contact-doped semiconductor films, a conductivity change as a function of an applied signal frequency, and HSPICE simulation. Lastly, the possibility of using low-cost metal electrodes in the top-gate OFETs has been explored.

## **CHAPTER 4 Circuit Implementation on Shape-Memory Polymers**

An individual transistor can be used as a simple electrical switch, a low-gain amplifier, or a sensor. However, when multiple transistors are integrated together, they can be used in building an infinite number of functional systems, such as microprocessors. Therefore, fabrication methods that connect transistors on a substrate is essential technology in the realization of electronic devices. Crystalline-silicon transistors have been interconnected by patterning deposited metals and dielectrics on a silicon wafer using conventional micro-fabrication methods, such as photo-lithography and etching. However, those traditional micro-fabrication methods are not suitable to for use in the fabrication of OFETs because of high process temperatures over 500 °C, and chemical/mechanical damages to organic materials during the process. These methods also compromise the advantages of OFETs, which is low-cost fabrication on a large-area substrate. Therefore, the first part of this chapter explains the development of a low-cost via-hole patterning method associated with a top-gate OFET structure.

The second half of this chapter demonstrates the fabrication of top-gate OFETs and circuits on shape-memory polymers (SMPs), which is one of the emerging flexible substrates exhibiting unique mechanical properties, since making the best use of the high mechanical flexibility of organic semiconductors is necessary to bringing the practical applications to the market.

### **4.1. Low-cost patterning method for via-holes**

#### **4.1.1. Introduction**

OFETs need to be fabricated by scalable, low-cost manufacturing processes for this technology to reach the market. Realization of solution-processed discrete OFETs is the

first step towards developing a scalable technology with low fabrication cost. To date, electrodes, gate dielectric layers and semiconductors have all been processed from solution [74-76] and patterned using techniques such as soft lithography [78], selective physical delamination [79, 80], and printing [75]. However, the realization of integrated circuits and systems using low-cost methods for patterning via-holes, which is essential for vertical interconnections between upper and lower electrodes, has received relatively less attention in the literature. Most reports of OFET circuits with high levels of performance and integration have relied on techniques commonly used in the microelectronic industry such as photolithography and chemical etchings or chemical lift-off processes to make via-holes [145]. However, utilizing the advantages of OFETs, such as using large, flexible substrates and depositing films by non-vacuum processing, alternative patterning methods are required in the fabrication of OFETs. To date, few novel patterning methods have been developed and reported for patterning dielectric films in an organic transistor structure, such as dissolution of polymeric dielectric layers by locally printing a solvent [24, 146], deposition of noble metals selectively defining areas where the growth of self-assembled monolayers (SAM) is hindered [37], and direct patterning by printing polymeric dielectric films [74]. However, these alternative approaches share a common limitation in that they are not capable of patterning inorganic layers, in particular high-quality metal-oxide layers synthesized by atomic layer deposition (ALD).

ALD is an important technique for the development of printed electronic applications because it has already been shown to lead to thin films with unique environmental barrier properties [147]. This is because the ALD method uses self-limiting surface reactions to allow controlled layer-by-layer growth of uniform and highly-

conformal films [148]. In addition, ALD technology is making headways into becoming a widespread industrial technique, as evidenced by recent developments in high-speed or spatial ALD processes, which allow high deposition rates (greater than 1.2 nm/s [149]) and are compatible with roll-to-roll fabrication methods.

ALD-grown metal-oxide films have been typically used as gate dielectrics in bottom-gate OFET geometries showing high-performance and low-voltage operation, both, in discrete devices [150] and circuits [40]. As mentioned in previous chapters, top-gate OFETs with a CYTOP/Al<sub>2</sub>O<sub>3</sub>(by ALD) bi-layer gate dielectric display high environmental and operational stability in air [53] and in water [55]. However, the use of ALD layers as gate dielectrics in top-gate OFET geometries presents a further challenge in that existing methods for patterning via-holes require harsh photolithographic methods [151] or selective-area ALD, via the deposition of blocking layers or inhibitors [152-154], which are not compatible with top-gate OFET fabrication methods. Hence, a need exists to develop alternative methods to pattern ALD-synthesized films to be used in electronic devices.

In order to address the challenge, patterning ALD-synthesized films, a new low-cost via-hole patterning method for top-gate TIPS-pentacene/PTAA OFETs, which is referred as a reverse stamping method in this dissertation, has been developed and applied to realize OFET circuits.

#### **4.1.2. Reverse stamping method**

##### 4.1.2.1 Process steps

The top-gate OFETs have been fabricated as described in CHAPTER 2 with one additional step, the reverse stamping. Before deposition of a gate metal, a reverse stamping



step was performed making vertical interconnections (via-holes) between lower source/drain electrodes and upper gate electrodes. Figure 4.1 illustrates the process steps of the reverse stamping method and a final cross-sectional view of an OFET with a via-hole on a substrate. In advance of the reverse stamping, a poly(dimethylsiloxane) (PDMS) stamp with embossed patterns at the position of the via-holes was fabricated as follows: the base was first mixed with agent (Gelest OE<sup>TM</sup> 41) in a weight ratio of 1:1 and the solution was then gently poured onto the pre-defined mold made of glass without trapped air bubbles in it. The pre-defined mold was then transferred to an oven for curing at 80 °C for an hour under atmospheric pressure and then cooled before the PDMS stamp was peeled off the mold. To perform the reverse stamping, first, the embossed PDMS stamp was aligned with the OFET substrate. Since the via-hole area on the stamp has the embossed parts, the stamp only contacts at the via-hole area. After being softly pressed onto the CYTOP/Al<sub>2</sub>O<sub>3</sub> bilayer surface, the stamp is lifted, peeling off parts of the films on the substrate on the via-hole area where the embossed pattern of the stamp landed. The gate metal is deposited after reverse stamping making an electrical short between gate electrodes and source/drain electrodes through the via-holes.

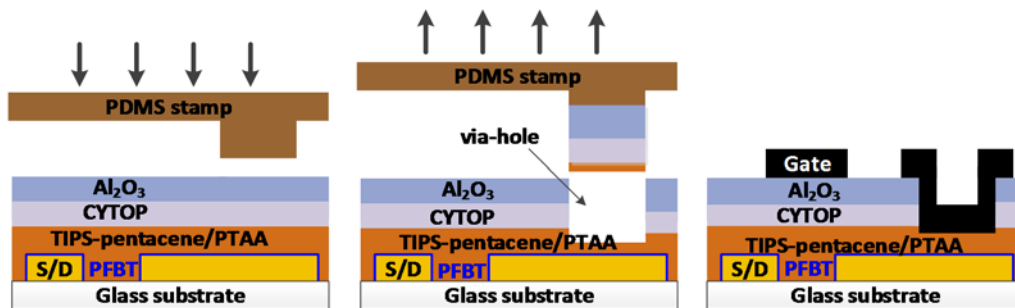


Figure 4.1. Schematic diagram of reverse stamping process and the final cross-sectional view of the device and circuits. Adapted from [155] by Choi *et al.*

In contrast to additive soft lithography, wherein a stamp is used to add up a patterned material or film to a substrate, the reverse stamping method removes a targeted area of a film off the substrate. This dry patterning method does not require vacuum-process steps or chemical etching and can be generally applied to OFET structures with high dielectric constant inorganic insulators.

#### 4.1.2.2 Characterization of via-holes

The layer structure at the via-hole area, which is made by the reverse stamping method was characterized by spectroscopic ellipsometry studies (J.A. Woollam M-2000UI). The optical properties of all layers and their thickness values were derived by modeling of spectroscopic ellipsometry data acquired at three angles of incidence: 65°, 70° and 75°, on samples before and after reverse stamping, and Figure 4.2 presents the details of this analysis. This analysis reveals that before reverse stamping, the semiconductor layer can be modeled as a 70 nm-thick effective medium layer (using Bruggeman's approximation) of 45% TIPS-pentacene and 55% PTAA, and a 34 nm-thick CYTOP/ 41 nm –thick Al<sub>2</sub>O<sub>3</sub> bilayer. It is noteworthy that the proportion between TIPS-pentacene and PTAA derived through this analysis correlates well with the 1:1 weight percent ratio solution used to deposit this film. After reverse stamping, the bilayer dielectric is completely removed and the semiconductor layer is best modeled by a 54 nm-thick effective medium layer (Bruggeman's approximation) of 19% TIPS-pentacene and 81% PTAA. This result indicates two things: first, about 20% of the semiconductor film is removed by reverse stamping; and second, the remaining layer is PTAA dominant, consistent with the expected phase segregation profile upon annealing, wherein a TIPS-pentacene rich region at the semiconductor/air interface is expected [43].

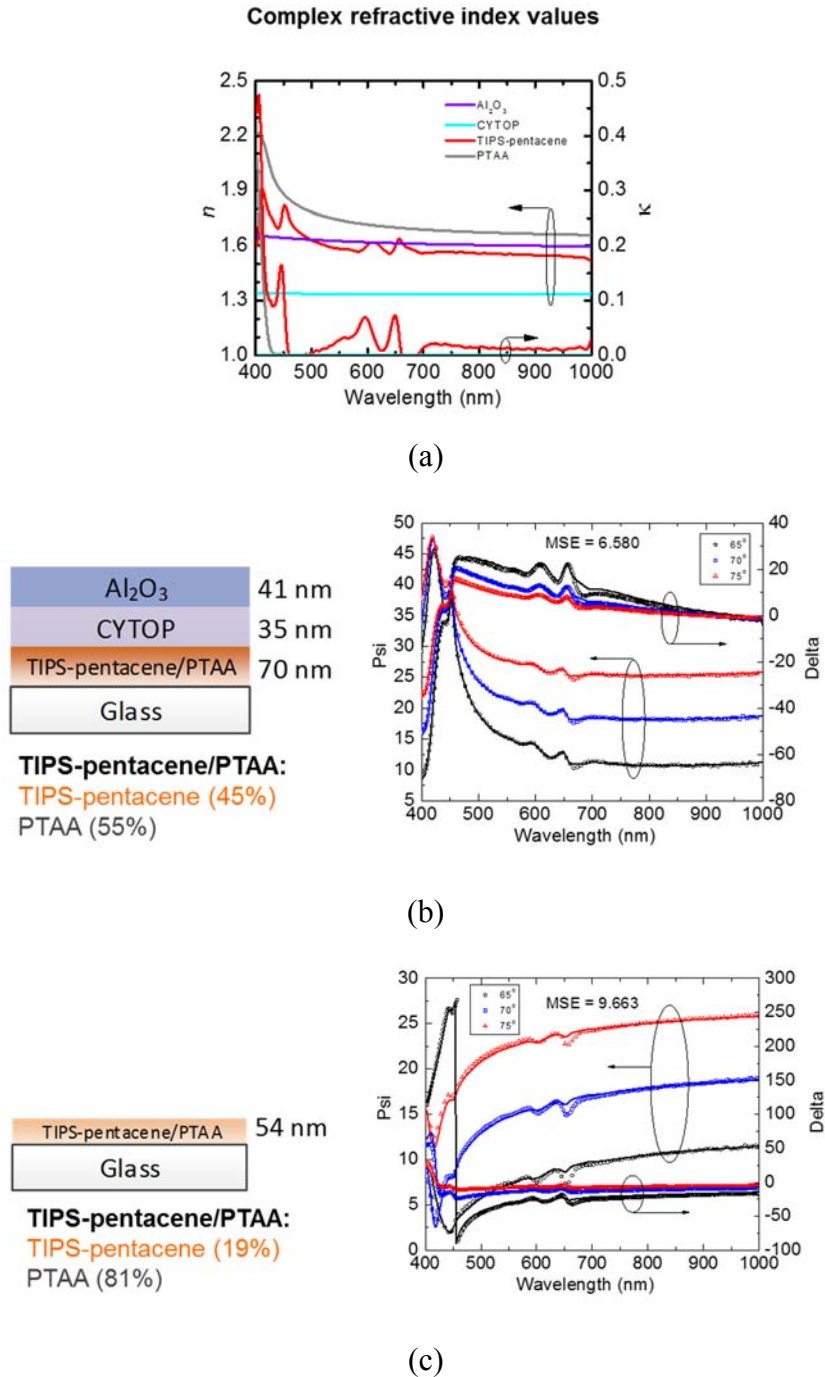


Figure 4.2. (a) Optical properties and thickness values of TIPS-pentacene/PTAA films with bilayer gate dielectrics (b) before reverse stamping and (c) after reverse stamping. Adapted from [155] by Choi *et al.*

These results also imply that the adhesive force between the small-molecule, TIPS-pentacene, and polymer, PTAA, is the weakest of all interfaces formed in the OFET

structure prior to delamination of the gate-dielectric bilayer by reverse stamping, PDMS/ $\text{Al}_2\text{O}_3$ /CYTOP/(TIPS-pentacene:PTAA)/glass (or PFBT/Au). When the reverse stamping method was conducted on samples comprising the bilayer dielectric deposited directly on glass, the bilayer was not delaminated from glass, indicating that the adhesive force between CYTOP and glass, and CYTOP and  $\text{Al}_2\text{O}_3$ , is stronger than that between PDMS and  $\text{Al}_2\text{O}_3$ .

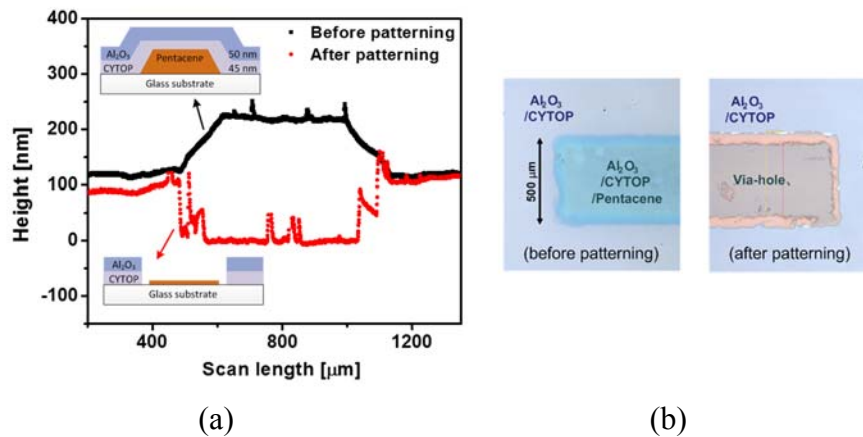


Figure 4.3. (a) Surface profile of an evaporated-pentacene/CYTOP/ $\text{Al}_2\text{O}_3$  structure, and (b) microscope images (top-view) of the sample before and after reverse stamping. Adapted from [155] by Choi *et al.*

Since the presence of the small molecule acene film plays a key role in enabling the reverse stamping method, we also fabricated an  $\text{Al}_2\text{O}_3$ /CYTOP/pentacene (thermally evaporated)/glass sample and applied the reverse stamping method. Figure 4.3 displays the surface profiles before and after reverse stamping on a thermally evaporated pentacene area (patterned through a shadow mask), showing clear lift-off of the bilayer in the region with patterned pentacene. Hence, the presence of small-molecule TIPS-pentacene in top-gate OFETs enables electrical transport and effective use of reverse stamping for the removal of the bilayer gate dielectrics. The reverse stamping method applied to the proposed device geometry is different from previously reported physical delamination

techniques in that it does not require an additional material, used as a sacrificial layer [79], and in that it does not remove the gold bottom electrode during patterning [80].

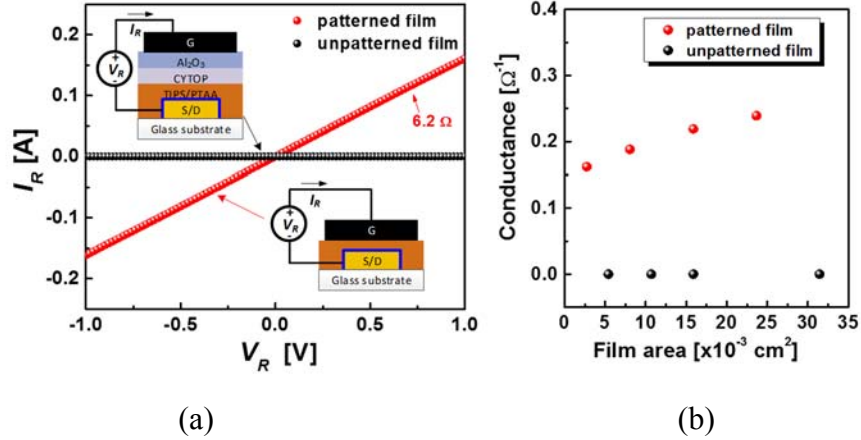


Figure 4.4. Electrical characteristics of via-holes made by reverse stamping: (a) current-voltage characteristics of a  $500 \mu\text{m} \times 500 \mu\text{m}$  film area, and (b) measured conductance as a function of patterned via-hole size. Adapted from [155] by Choi *et al.*

The electrical characteristics of  $Al_2O_3$ /CYTOP/(TIPS-pentacene:PTAA) films on bottom electrodes were studied before and after lamination by measuring the resistance of the film across different areas defined by the overlap between the bottom electrode and top electrodes having different widths. This approach was deemed more accurate for measuring the resistance of patterned films than direct measurements over patterned via holes. Figure 4.4(a) displays the current-voltage characteristics of a  $500 \mu\text{m} \times 500 \mu\text{m}$  film area before and after patterning. Figure 4.4(b) displays the conductance of patterned films as a function of the area of electrode overlap. Despite the presence of a remnant TIPS-pentacene/PTAA film on the Au bottom electrode, the current-voltage characteristics of patterned films display ohmic behavior with resistance values in the range between  $4.1 \Omega$  and  $6.1 \Omega$ , which is low enough to be used as an electrical interconnection between two electrodes.

These results demonstrate the effectiveness of the reverse stamping technique on a top-gate OFET geometry having a bilayer dielectric layer and a small-molecule semiconductor layer comprising acenes, such as a pentacene or TIPS-pentacene, that are one of the widely-used class of organic semiconductors in OFET applications. Caution must be exercised in generalizing this concept to other classes of small-molecule semiconductors since the strength of the interfacial forces between two layers of dissimilar materials can depend on other physical properties such as their polarity, molecular size, or chemical affinity. However, these results offer insight into the realization of via-hole interconnects in top-gate OFET geometries and suggest that with proper selection of materials reverse stamping could be used as a cost-effective method for patterning ALD-based layers.

#### 4.1.3. Implementation of circuits

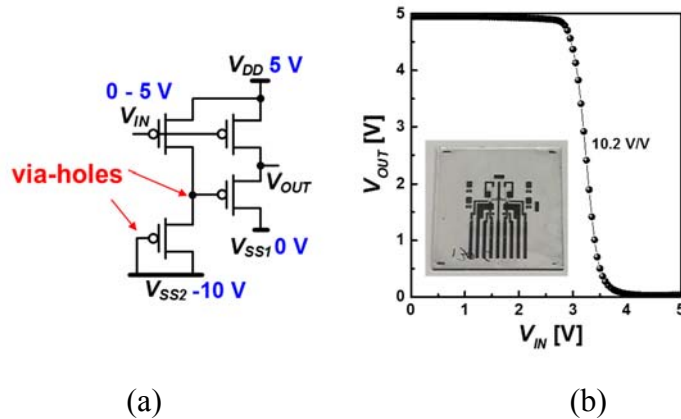


Figure 4.5. (a) Schematic diagram of a pseudo-complementary inverter circuit, and (b) its transfer characteristics measured from a fabricated sample with the top-gate OFETs (inset figure is the photograph of a fabricated sample).

Using the reverse stamping method in the fabrication of top-gate OFETs, several simple logic circuits have been implemented, such as inverters, NOR2 gates, ring oscillators, and 2-to-4 decoder circuits.

Figure 4.5(a) displays the schematic of a pseudo complementary inverter circuit and Figure 4.5(b) is an output transfer curve measured on one of the inverter circuits fabricated on a glass substrate with via-holes made by the reverse stamping method. Using a 5 V peak-to-peak input voltage sweep, a peak-to-peak 5 V output signal was measured and a DC voltage/voltage gain of 10.2 V/V was observed.

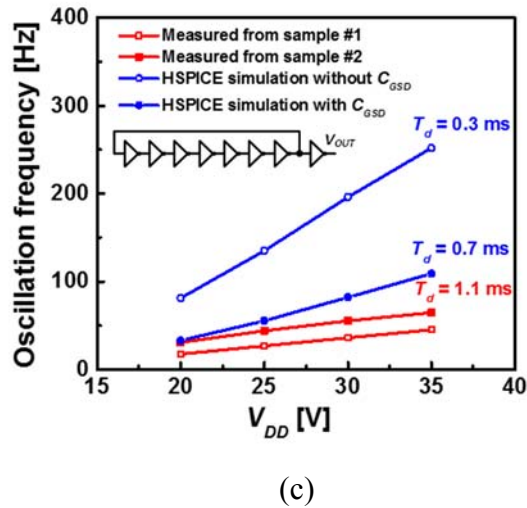
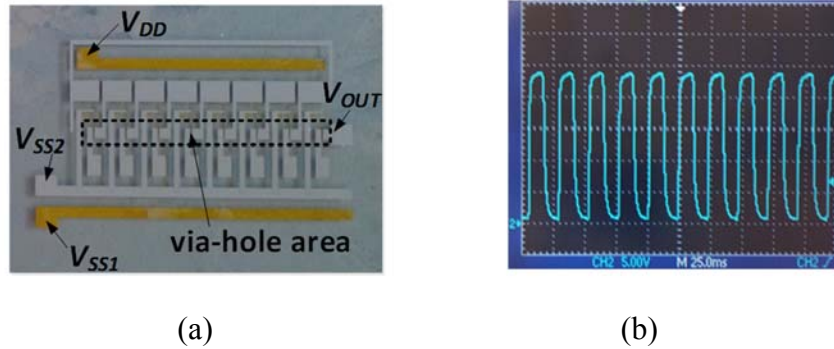


Figure 4.6. (a) Photograph of the fabricated ring oscillator sample, (b) an output signal waveform captured from an oscilloscope, and (c) the measured oscillation frequency of the circuits with respect to the simulated value. Adapted from [155] by Choi *et al.*

A 7-stage ring oscillator was also fabricated on 1.5-inch by 1.5-inch glass substrate as shown in Figure 4.6(a), and Figure 4.6(b) displays a screen-capture of an oscilloscope displaying the output waveform generated by the 7-stage ring oscillator. The oscillation frequency of the fabricated ring oscillator circuits was evaluated as a function of applied

power supply,  $V_{DD}$ , and the measured value exhibited considerably lower values than those from HSPICE simulation, when the parasitic capacitance between gate and source/drain electrodes are not counted in the simulation schematics (blue empty symbol in Figure 4.6(c)). This discrepancy is suppressed when the calculated parasitic capacitance,  $C_{GSD}$ , is applied to each nodes in the schematics (blue filled symbol in Figure 4.6(c)). The remaining gap between the HSPICE-simulated and the measured values is attributed to the device-to-device variation in on-current of the OFETs, and the accuracy of  $C_{GSD}$  applied in the simulation. It is noteworthy that the gate-source/drain capacitance in OFETs should be counted in the circuit simulation as presented above since OFETs, in general, have a large area of an overlapped region between gate and source/drain electrodes in the device geometry, in turn, the capacitance is considerably higher, affecting the circuit operation.

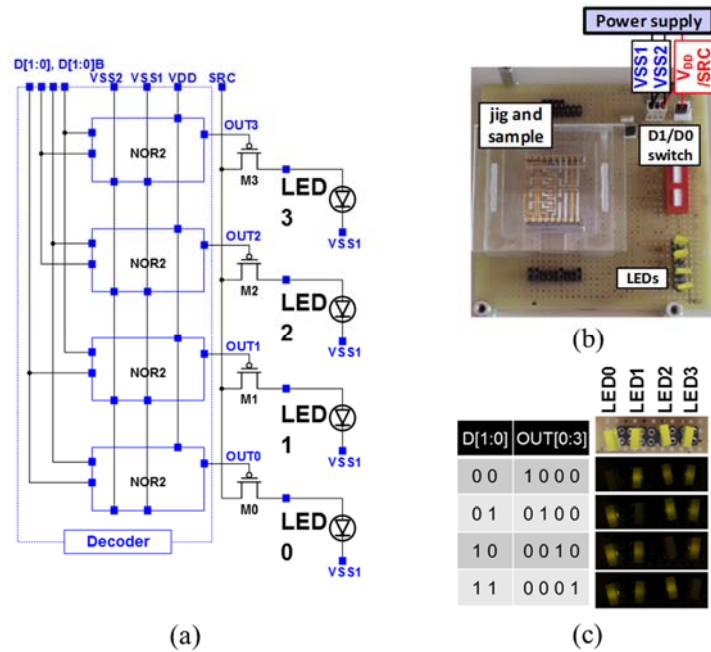


Figure 4.7. (a) Block diagram of the designed 2-to-4 decoder circuit, (b) its driving peripheral setup on a perforated circuit board, and (c) the truth table of the circuit with the photograph of controlled LEDs according to the 2-bit input codes. Adapted from [155] by Choi *et al.*



Implementation of large-scale applications using OFETs requires a matrix addressing method. This method seeks to address a cell or a line of cells in a two-dimensional array with the smallest number of read-out lines possible. A decoder circuit is one of the essential parts used in a matrix driving method [156] and is commonly located at the end of each row-line receiving and interpreting binary-encoded digital signals, and sending activation signals to the line of cells connected to it. For the reason, a 2-to-4 decoder, which follows the truth table in Figure 4.7(c), has been designed and fabricated by combining four NOR2 gates as displayed in Figure 4.7(a). By using custom-made jig and peripheral components, shown in Figure 4.7(b), the circuit was operated and its function was evaluated; the fabricated sample was placed upside down in the jig to contact the jig's pins with the sample's pads. Two-bit binary coded input signals (D[1:0]) were generated by dual in-line package (DIP) switches and the decoder circuit and driving OFETs (M0 - M3) selectively turn on and off LEDs mounted on a PCB according to the binary inputs. The results show the successful operation of the decoder in addressing one of the four LEDs according to the inputs. Figure 4.7(c) shows the photograph of the four LEDs on the PCB selected and turned off according to the two bit decoder input signals as designed.

#### **4.1.4. Conclusions**

In summary, a simple reverse stamping method for making via-holes for top-gate OFET circuits having an ALD processed metal-oxide/polymer bilayer gate dielectric was proposed and demonstrated. The reverse stamping method effectively removed the bilayer gate dielectrics and enabled the demonstration of simple circuits such as inverters, NOR2 gates, ring oscillators, and decoders based on top-gate TIPS-pentacene/PTAA OFETs with

a CYTOP/Al<sub>2</sub>O<sub>3</sub> bilayer gate dielectric. Further improvement in the resolution of the patterns is expected to be achieved by patterning the semiconductor layer, and will be pursued in the future to optimize OFET and circuit performance. The use of ink-jet-printed semiconductor patterns, used as semiconductor channels as well as sacrificial layers is expected to further increase the resolution of this technique and to allow the production of denser and more complex top-gate OFET circuits.

## **4.2. Top-gate OFETs on shape-memory polymers**

### **4.2.1. Introduction**

As the electrical performances of OFETs are approaching the requirements for the realization of commercially viable products, applications of OFETs have become an important topic of OFET research. One of the desirable properties of OFETs is mechanical flexibility which is an essential characteristic for flexible electronic devices, and research scientists have been exploring new flexible substrate materials, such as polyimide, poly(dimethylsiloxane) (PDMS), and polyestersulfone (PES) [17, 36, 58-64].

The top-gate TIPS-pentacene/PTAA OFETs have also been fabricated on various kinds of flexible substrates, such as PES substrates as reported by Hwang *et al.* [61] and cellulosic nanocrystal (CNC) substrates as reported by Wang *et al.* [65]. The top-gate OFETs on PES and CNC substrates demonstrated *I-V* characteristics comparable to those on glass substrates as shown in Figure 4.8, as well as high operational stability when appropriate buffer layers cover the surface of the substrates, such as poly-4-vinylphenol (PVP) on PES substrates and Al<sub>2</sub>O<sub>3</sub> on CNC substrates.

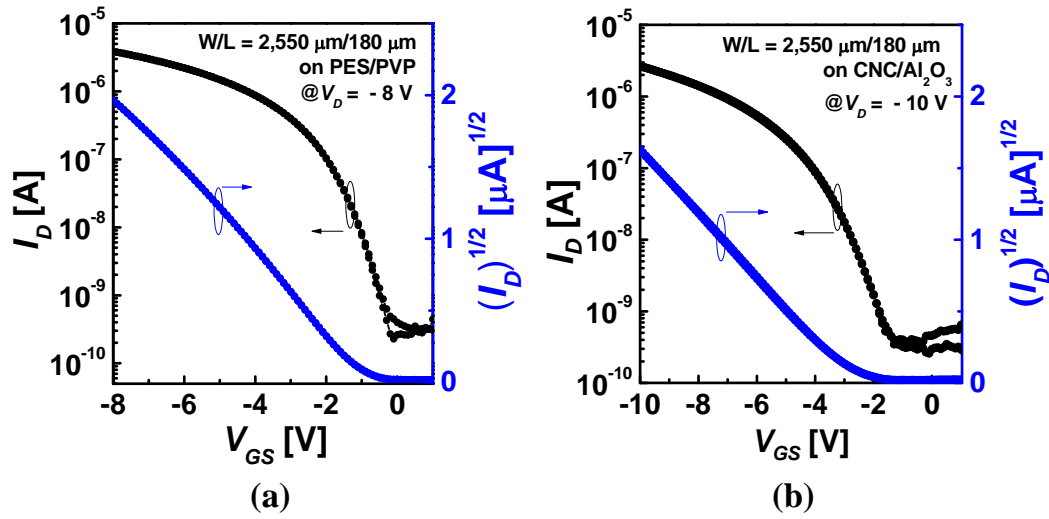


Figure 4.8. The transfer characteristics of the top-gate OFETs on (a) PES substrates (adapted from [61]) and (b) CNC substrates (adapted from [65]).

Shape-memory polymers (SMPs) – part of an emerging class of materials – that have shown unique features, such as a variable Young’s modulus dependent on temperature, low cure stresses, biocompatibility, and the capability of transfer-by-polymerization [157-159], have also been adapted as a flexible substrate for OFETs [66, 67, 69, 70]. Because of the reshaping feature of the polymer, SMPs are expected to be a good candidate as a substrate material for three-dimensional shape applications; for example, human body-embedded sensors can be inserted, using a variety of stimuli-responsive SMPs [159]. Reeder *et al.* demonstrated the biomedical applications by building bottom-gate dinaphtho[2,3-*b*:2',3'-*f*]thieno[3,2-*b*]thiophene (DNTT) OFETs on SMPs [66]. The property of returning to a permanent shape in response to stimuli (shape recovery) of SMPs was also exploited for self-assembly electronics as reported by Wang *et al.* showing self-wrapping polymers [69], Liu *et al.* demonstrating self-folding polymer sheets [70], and Lu *et al.* developing the electrical actuation with nanopaper-combined SMPs [71].

In this research, the direct fabrication of TIPS-pentacene/PTAA OFETs and their circuits on biocompatible, low cure stress SMP substrates is demonstrated.

#### 4.2.2. Top-gate OFETs and circuits on SMPs

Although the top-gate OFETs with CYTOP/Al<sub>2</sub>O<sub>3</sub> dielectrics have presented both high performance and stable operations [53], and unchanged  $I$ - $V$  characteristics when bent with a 13.5 mm bending radius at room temperature on PES substrates [61], the OFETs showed impaired electrical performances when fabricated directly on top of SMPs. The fabrication yield of the OFETs on SMPs was less than a half of those on glass substrates in the same batch because of severe dewetting problems in spin-coating TIPS-pentacene/PTAA solution on the surface of SMPs; hysteresis of their drain current in a low- $V_G$  bias regime was observed as shown in Figure 4.9(a), and impaired threshold voltage and field-effect mobility by around half was measured as shown in Figure 4.9(b) and (c).

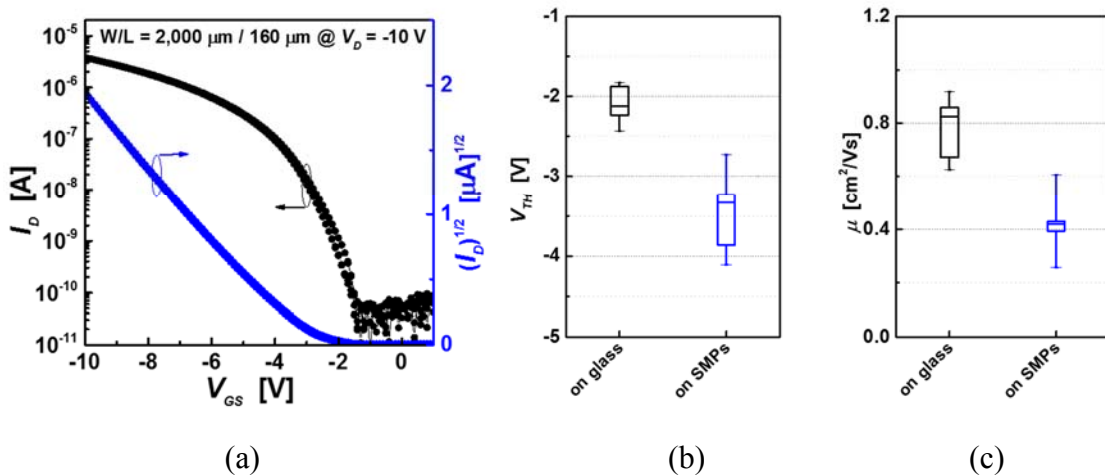


Figure 4.9. Electrical characteristics of top-gate OFETs fabricated directly on SMPs: (a)  $I$ - $V$  transfer characteristics; and a comparison of (b)  $V_{TH}$  values, and (c) field-effect mobility values between the OFETs on glass and SMP substrates.

More importantly, when the substrates were reshaped on a 60 °C hot plate with a 30 mm bending radius, a much smaller bending stress level than the stress applied to the same structure of OFETs on a PES substrate at room temperature [61], the OFETs suffered from severe cracks in gate dielectrics, CYTOP/Al<sub>2</sub>O<sub>3</sub>, resulting in an electrical short between gate and source/drain electrodes in the device. In addition, the OFETs that did not show the electrical short after the reshaping exhibited critically degraded performance, as presented in Figure 4.10. After all, reshaping in this experiment is distinguished from bending at room temperature, in terms of the test temperature.

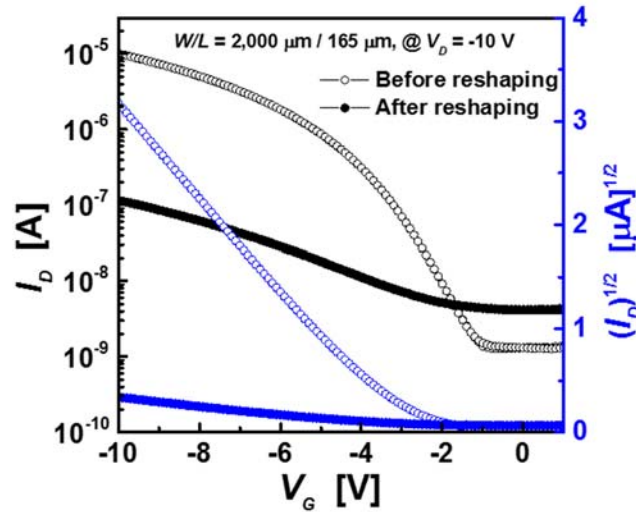


Figure 4.10. Transfer characteristics of an OFET with CYTOP/Al<sub>2</sub>O<sub>3</sub> bilayer gate dielectrics on SMP substrates after reshaping with a bending radius of 30 mm.

#### 4.2.2.1 Modification of device structure for top-gate OFETs on SMPs

In order to ensure as high performance and stable operation of the OFETs on SMPs as those on glass substrates, a 50 nm-thick PVP buffer layer was spin-coated on top of SMP substrates protecting TIPS-pentacene/PTAA films from any possible chemical reactions with elements on the surface of SMPs, such as residue of Rain-X which was used on glass molds.

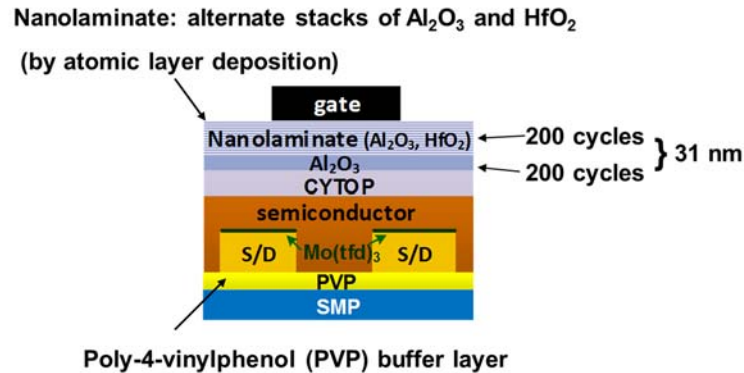


Figure 4.11. Cross-sectional view of the modified device geometry for top-gate OFETs on SMPs.

In addition, the modified structure replaced the CYTOP/ $\text{Al}_2\text{O}_3$  in the bilayer gate dielectrics with a CYTOP/nanolaminate in which the nanolaminate is an alternately stacked  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$  by ALD after 200 cycles of  $\text{Al}_2\text{O}_3$  deposition [160] addressing the poor reshaping tolerance at 60 °C. After all, while  $\text{Al}_2\text{O}_3$  films deposited by ALD are a good gate dielectric layer for top-gate OFETs at ambient temperature, the film is known to degrade in its mechanical/chemical stability under exposure to high temperatures [161, 162]. Nanolaminate films have also been adapted in other research enhancing the stability of ALD-deposited  $\text{Al}_2\text{O}_3$  films at an elevated temperature, as reported by Bulusu *et al.* [160] in the context of a high performance encapsulation structure; and the OFETs using nanolaminate instead of a  $\text{Al}_2\text{O}_3$  layer in the structure on a glass substrate also exhibited significantly increased stability during the immersion experiment in 95 °C water, which will be reported in future research.

Lastly,  $\text{Mo}(\text{tfd})_3$ -doped source/drain electrodes, which improve the electrical characteristics of the top-gate OFETs as stated in CHAPTER 3, were adapted instead of PFBT-treated electrodes in the OFETs. Figure 4.11 shows the final device geometry applied for the fabrication of the top-gate OFETs on SMP substrates.

#### 4.2.2.2 Current-voltage characteristics of the OFETs with the modified structure

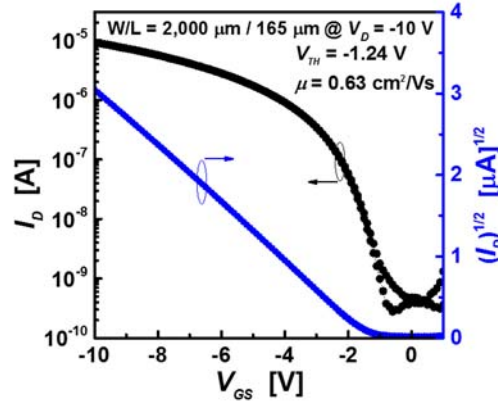


Figure 4.12.  $I$ - $V$  transfer characteristics of top-gate OFETs with CYTOP/nanolaminate bilayer gate dielectrics, a PVP buffer layer, and Mo(tfd)<sub>3</sub>-doped source/drain electrodes.

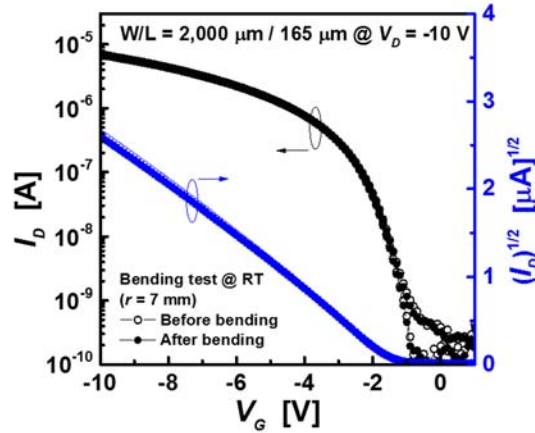


Figure 4.13.  $I$ - $V$  transfer characteristics of top-gate OFETs before and after bending the device at room temperature with a bending radius,  $r$ , of 7 mm.

Figure 4.12 shows the measured  $I$ - $V$  transfer characteristics of the OFETs with the modified structure. The hysteresis effect has been suppressed, and  $V_{TH}$ ,  $-1.1 \pm 0.36$  V (averaged over three devices), and  $\mu$  values,  $0.9 \pm 0.59$  cm<sup>2</sup>/Vs (averaged over three devices), of the OFETs are comparable to those of OFETs with the conventional structure on glass substrates. The transfer characteristics also comply with the square law of field-

effect transistors due to a low contact resistance from the contact-doped electrodes in the device.

For the evaluation of the potential of using the OFETs on SMP substrates in 3D-shape applications, the behavior of the OFETs after bending at room temperature and reshaping at 60 °C has been examined. Bending and reshaping tests were performed in a N<sub>2</sub>-filled glove box preventing any effects resulting from air exposure, and the SMP substrates were reshaped on a 60 °C hot plate since the SMPs have a 43 °C glass transition temperature,  $T_g$ , shown in Figure 2.6.

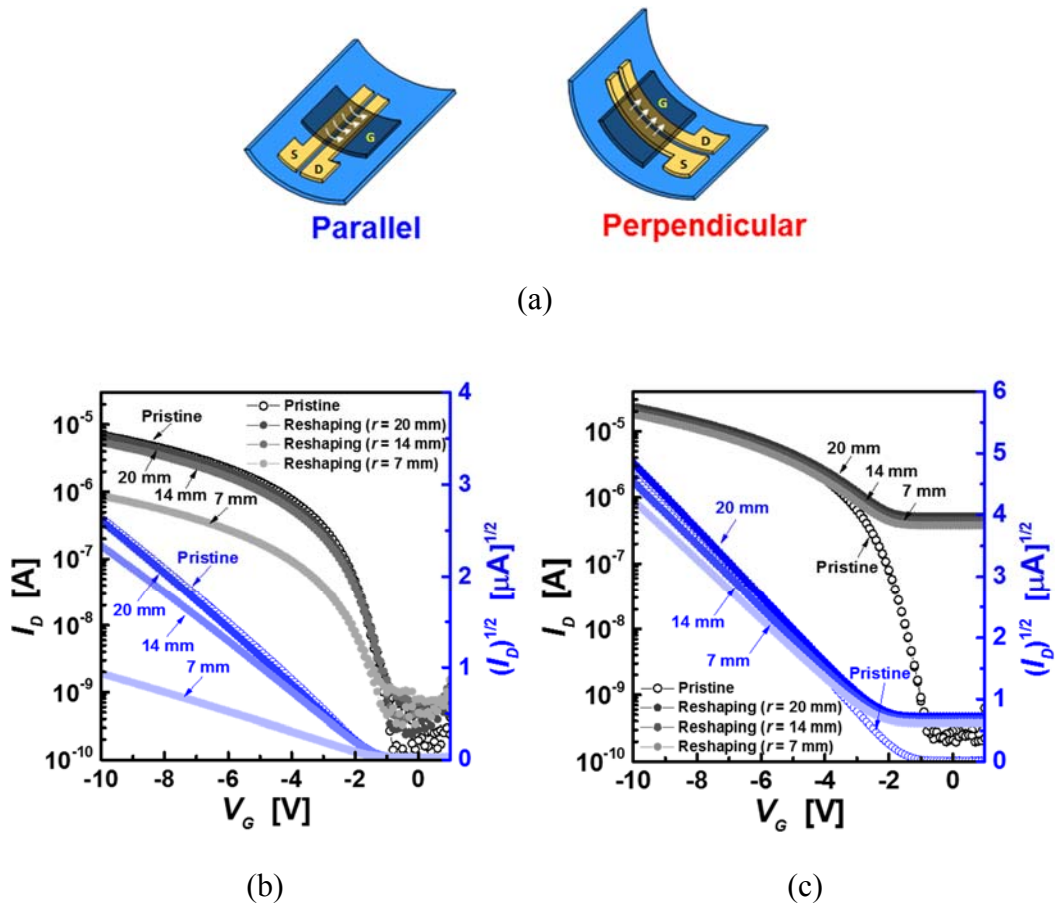


Figure 4.14. (a) Illustration of bending orientation of SMP substrates with respect to the channel of the OFETs, and the  $I$ - $V$  transfer characteristics of the OFETs on SMPs before reshaping, after reshaping the substrate with a bending radius of 7 mm, 14 mm, and 20 mm when the bending orientation is (b) parallel and (b) perpendicular to the channel of the OFETs ( $r$ : bending radius).



At the room temperature bending test shown in Figure 4.13, the top-gate OFETs displayed negligible changes in the  $I$ - $V$  transfer characteristics after compressive bending with a 7 mm bending radius. Upon reshaping of the substrates with heat, the OFETs with the modified structure also exhibited improved tolerance on reshaping together with a limitation in the bending radius as shown in Figure 4.14; with bending orientation that is parallel to the channel of OFETs,  $V_{TH}$  and off-current remained steady after reshaping while  $\mu$  values dropped significantly by decreasing the bending radius to 7 mm; with perpendicular bending to the channel of OFETs,  $V_{TH}$  remained steady and the changes in  $\mu$  values is much less than those in the parallel bending, but the off-current surged up after reshaping.

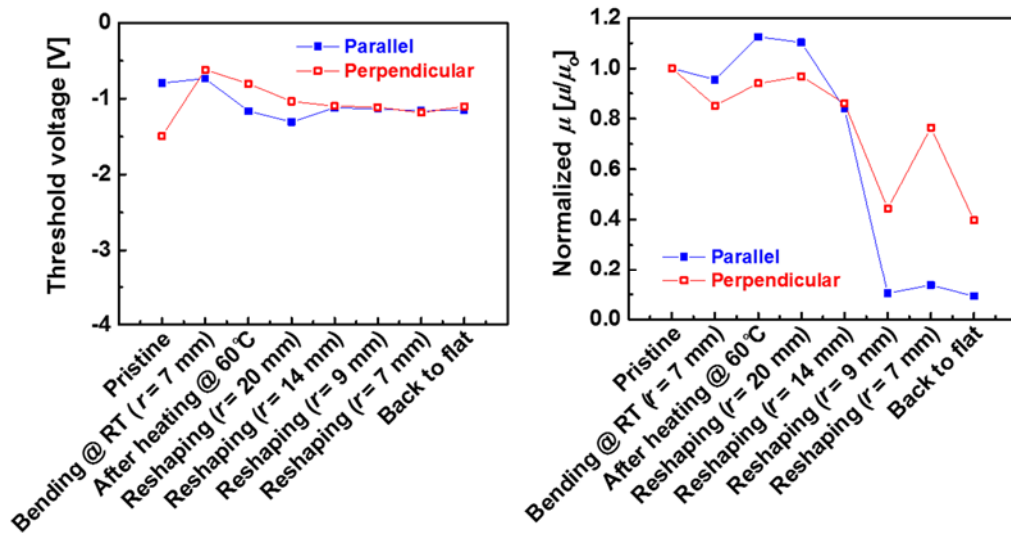


Figure 4.15. Extracted electrical parameters of the OFETs on SMPs with respect to substrate conditions: (a) threshold voltages and (b) normalized field-effect mobility values.

After the reshaping test with the sample, many cracks were found in the area where the gate dielectric layer is covered as shown in Figure 4.16 whereas the cracks were not observed in the area where the gate dielectrics have been removed, which suggests the major performance decreases still result from the cracks of gate dielectrics in the device.

Another observation from the images and the device performances in the figures is that the cracks are aligned perpendicular to the bending orientation, leading us to the hypothesis that the cracks cause a leakage current along them, increasing the off-current shown in Figure 4.14(c).

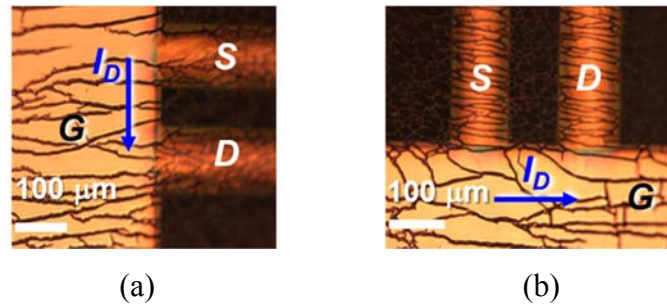


Figure 4.16. Captured microscope images of the OFETs on SMPs after reshaping: (a) parallel bending to the channel, and (b) perpendicular bending to the channel.

#### 4.2.2.3 Inverter circuits on SMPs

Using reverse stamping, a pseudo-complementary inverter circuit, which has a schematic in inset of Figure 4.17(a), was fabricated on a SMP substrate with the modified top-gate OFET geometry.

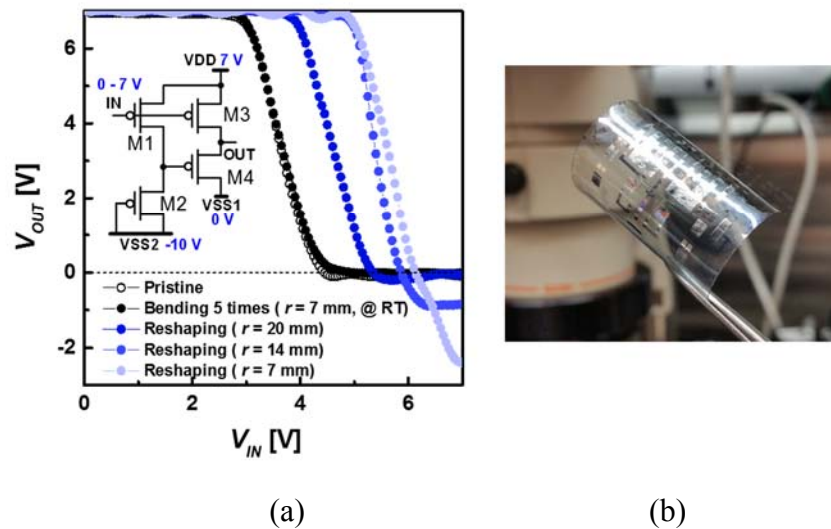


Figure 4.17. (a) Transfer characteristics of a pseudo-complementary inverter circuit comprises the top-gate OFETs with the modified device geometry in various substrate conditions, and (b) a photograph of the reshaped inverter circuit sample.

Similar to the circuit on a glass substrate, the pseudo-complementary inverter circuit that comprises the top-gate OFETs on a SMP substrate displayed a well-balanced threshold voltage and a rail-to-rail swing in  $V_{OUT}$  with 7 V operating voltages with a voltage gain of 8.3 V/V, and the transfer characteristics remained stable after bending and releasing five times with a 7 mm bending radius at room temperature. However, applying heat and reshaping the substrate impacted the inverter properties; the transfer curve shifted, and it eventually failed to keep the designed output voltage range, 0 - 7 V, when reshaped with a 14 mm bending radius.

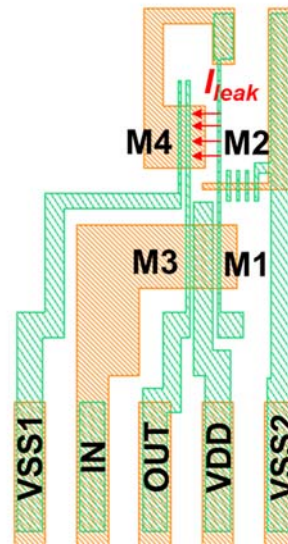


Figure 4.18. Layout design of the pseudo-complementary inverter circuit.

The shift of transfer characteristics and the change of the low-end level of output voltages can be explained with the increased leakage current path along the cracks in the gate dielectrics: The top-gate OFETs in the circuit are all oriented in the same direction, and the bending orientation in the test is perpendicular to the channel, which is the same condition shown in Figure 4.14(c). Therefore, the TIPS-pentacene/PTAA film and the gate-dielectrics, that are not patterned in the device and covered the entire surface, make

large leakage current,  $I_{leak}$ , path between the output node of the inverter,  $OUT$  (simulated  $V_{OUT} = 0$  V), and the source electrode of transistor M2 (simulated  $V_{S\_M2} \sim -8$  V) as illustrated in Figure 4.18 when cracks are created. As a result, the mid voltage of the two electrodes appears as the measured  $V_{OUT}$  in the inverter circuit. Therefore,  $V_{OUT}$  is closer to the ideal value, 0 V, at high  $V_{IN}$  without bending or with a large bending radius, however, as the bending radius decreases, the cracks and leakage current,  $I_{leak}$ , increase resulting in  $V_{OUT}$  values approaching  $V_{S\_M2}$ , -8 V. When  $V_{IN}$  is low, M1 and M3 are dominating in the circuit, and  $V_{OUT}$  keeps the  $V_{DD}$  level, 7 V, while a small instability on the high voltage level of  $V_{OUT}$  is observed.

#### 4.2.3. Conclusions

In summary, top-gate TIPS-pentacene/PTAA OFETs that comprise CYTOP/nanolaminate gate dielectrics and doped contacts with Mo(tfd)<sub>3</sub> have been fabricated on shape-memory polymers. The fabricated top-gate OFETs exhibited  $I$ - $V$  characteristics comparable to those on a glass substrate. By replacing a CYTOP/Al<sub>2</sub>O<sub>3</sub> bilayer with a CYTOP/nanolaminate bilayer, the bending tolerance of the OFETs has been improved not only in the bending test at room temperature but also in the reshaping test at 60 °C. However, the cracks originating from polymer/inorganic gate dielectrics are still observed in the modified structure when reshaped above the glass transition temperature of the SMP substrate though they are less severe than those in the OFETs comprising a CYTOP/Al<sub>2</sub>O<sub>3</sub> bilayer. Inverter circuits were also fabricated on SMP substrates, and the fabricated circuits exhibited as high voltage gain as those fabricated on glass substrates with 7 V operating voltages. As the operational failure of the OFETs and circuits are attributed to the leakage current in the semiconductor film along the cracks of gate

dielectrics, patterning and reducing the surface area that are covered by the layers need to be integrated into the fabrication of the OFETs for better system robustness. In addition, for the applications that requires high mechanical flexibility but low current driving capability, employing polymeric dielectrics that have relatively lower dielectric constant but higher mechanical robustness could further mitigate the cracking problem when combined with the SMP substrates.

## CHAPTER 5 Conclusions and Recommendations

### 5.1. Conclusions

In this dissertation, the device structure and fabrication of high-performance top-gate OFETs comprising a TIPS-pentacene/PTAA film as an active layer and a CYTOP/metal-oxide bilayer as a gate dielectric layer developed previously by members of our group have been adopted and further improved. Particularly, the top-gate OFETs have been fabricated on a shape-memory polymer substrate demonstrating the potential of the device being used for 3D-shape applications, such as wearable electronics. In detail, the performance of the top-gate OFETs has been improved by significantly lowering the contact resistance of the OFETs at the metal-semiconductor interface by developing a contact-doping method, which inserts a thin layer of dopants on source/drain electrodes before the solution processing of an organic semiconductor layer. The OFETs having low contact resistance have been used as a backplane of OFET circuits combined with a newly developed patterning method of a CYTOP/metal-oxide gate dielectric layer, by reverse stamping. Finally, high performance top-gate OFET circuits on SMPs have been developed and demonstrated based on this dissertation work. The summary and the conclusions of each of the chapters are as follows.

Chapter 3 focused on developing top-gate OFETs having low contact resistance. Using two approaches, the insertion of excessively high work function electrodes over the pinning-level of a semiconductor film and the deposition of a thin-layer of p-dopants, the contact resistance of the top-gate TIPS-pentacene/PTAA OFETs significantly decreased. For example, the width-normalized contact resistance of the OFETs dropped from 81 k $\Omega$ cm with conventional PFBT-treated Au electrodes to 15 k $\Omega$ cm with Mo(tfd)<sub>3</sub>-doped Au

electrodes. Regarding the measured pinning level of Fermi level energy of a TIPS-pentacene/PTAA film and the investigation of bulk resistance on contacts, this reduction of contact resistance of the OFETs is attributed to the combination of the lowered injection barrier height for charge carriers at the interface as well as the doping of the semiconductor bulk with the contact-doped electrodes.

Chapter 4 targeted the fabrication of high performance OFETs and their circuits on shape-memory polymers. In this chapter, reverse stamping, the low-cost, non-vacuum processed patterning method making via-holes through the bilayer gate dielectrics, was introduced, and the electrical and structural properties of the via-holes made by reverse stamping were examined, revealing that the proposed method can be adapted for interconnections between top and bottom electrodes in the top-gate TIPS-pentacene/PTAA OFETs. The second half of Chapter 4 demonstrated the fabrication of top-gate OFETs on SMP substrates. The top-gate OFETs were successfully fabricated on SMPs with electrical performances that are comparable to those of the OFETs on glass substrate by two modifications in the device structure; a CYTOP/ $\text{Al}_2\text{O}_3$  gate dielectric layer has been replaced by a CYTOP/nanolaminate film for higher tolerance against a bending stress at temperature higher than the glass transition temperature of the SMPs, and a PVP buffer layer has been employed on SMP substrates prior to the fabrication of the OFETs on the substrate. The OFETs with the modified structure exhibited a stable operation in terms of their field-effect mobility and threshold voltage down to a 20 mm bending radius in the reshaping test that was performed at 60 °C, and then gradually degraded as the bending radius decreased while the electrical short that has been observed in the OFETs with CYTOP/ $\text{Al}_2\text{O}_3$  dielectrics did not occur with the modified structure down to a 7 mm

bending radius. Lastly, by combining the contact-doping method explored in Chapter 3 and the reverse stamping method, the circuits that are integrated with OFETs having the modified top-gate structure have been designed and fabricated on SMP substrates.

## **5.2. Recommendations for future work**

### **5.2.1. Contact resistance**

In this research, contact resistance in top-gate OFETs with contact-doped electrodes has been investigated primarily from the point of view of lowered energy barrier height and reduced bulk resistance by carrier doping. However, the contact properties in OFETs are also influenced by the morphology of the semiconductor films near contacts [81, 83-86]. Therefore, the contact resistance of OFETs should also be explored from the morphology point of view in a later work on this topic.

In addition, using contact-doped electrodes in OFETs accompanying printed metal electrodes, such as a printed silver electrode, should increase the adoption of the method to pursuing a realization of large-area, printed electronics. However, unlike contact doping in this dissertation research that has been performed by thermally evaporating dopant materials using a shadow mask, depositing dopants on printed electrodes can require another kind of fabrication method, such as screen printing both electrodes and dopants. Hence, alternate deposition methods and dopant materials should be developed and examined for printed organic transistors with low contact resistance adapting the contact-doping method.



### **5.2.2. Low-cost via-hole patterning**

This dissertation research focused on the low-cost patterning of via-holes in top-gate OFETs and introduced reverse stamping. Even though logic circuits have been demonstrated using the proposed method, reverse stamping still has a limitation in a patterning resolution since the sacrificial layer, a TIPS-pentacene/PTAA film, is deposited on an entire surface of a substrate; in turn, the area of a via-hole is defined only by the embossed pattern on the PDMS stamp, and the resolution of the patterning method is limited by the molding precision of the stamp. Moreover, the space between via-holes that should be electrically isolated and between a via-hole and an OFET should be wide enough to prevent electrical shorts among terminals. Therefore, for the increase of the resolution of the method, patterning of the sacrificial layer, which is the semiconductor layer in this OFET geometry, by using printed semiconductor films should be the future work in the context of the realization of highly functional OFET circuits.

### **5.2.3. OFET circuits on SMPs**

As stated in Chapter 4, the increase of off-current and the decrease of field-effect mobility values in the top-gate OFETs on SMP substrates when they are reshaped, is attributed to the cracks in a gate dielectric layer. While the use of an inorganic metal-oxide layer, such as  $\text{Al}_2\text{O}_3$  and nanolaminate of  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$ , improves the electrical performances and stability of the OFETs, it also limits the mechanical robustness of the structure. Therefore, two approaches are recommended for top-gate OFETs on SMPs: first, for the applications that require high current driving capability of transistors, the degradation of OFETs and their circuits can be alleviated by patterning gate dielectric and semiconductor layers reducing a potential leakage current path, and by placing the device

in a neutral position sandwiched between two layers of polymers. Second, for the applications that do not require high performance of OFETs, using polymeric dielectric materials for gate dielectrics instead of inorganic materials should improve the structural stability of the device. For both approaches, proper materials need to be selected with a low-cost fabrication method, and mechanical modeling and calculation in determining thickness of each layer are also required.

### 5.3. List of selected publications

1. **S. Choi**, C. Fuentes-Hernandez, M. Yun, A. Dindar, T. M. Khan, C.-Y. Wang, and B. Kippelen, "Organic Field-Effect Transistor Circuits Using Atomic Layer Deposited Gate Dielectrics Patterned by Reverse Stamping," *Organic Electronics*, vol. 15, p. 3780, 2014.
2. M. Yun, A. Sharma, C. Fuentes-Hernandez, D. K. Hwang, A. Dindar, S. Singh, **S. Choi**, and B. Kippelen, "Stable Organic Field-Effect Transistors for Continuous and Nondestructive Sensing of Chemical and Biologically Relevant Molecules in Aqueous Environment," *ACS Applied Materials & Interfaces*, vol. 6, p. 1616, 2014.
3. C.-Y. Wang, C. Fuentes-Hernandez, J.-C. Liu, A. Dindar, **S. Choi**, J. P. Youngblood, R. J. Moon, and B. Kippelen, "Stable Low-Voltage Operation Top-Gate Organic Field-Effect Transistors on Cellulose Nanocrystal Substrates," *ACS Applied Materials & Interfaces*, vol. 7, p. 4804, 2015.
4. **S. Choi**, C. Fuentes-Hernandez, M. Yun, A. Dindar, T. M. Khan, C.-Y. Wang, and B. Kippelen, "Organic Field-Effect Transistor Circuits with Electrode Interconnections Using Reverse Stamping," *Proceedings of the SPIE*, p. 918511, 2014
5. **S. Choi**, C. Fuentes-Hernandez, C.-Y. Wang, A. Wei, W. Voit, Y. Zhang, S. Barlow, S. R. Marder, and B. Kippelen, "Top-Gate Organic Field-Effect Transistors Fabricated on Shape-Memory Polymer Substrates," *Proceedings of the SPIE*, p. 95680A, 2015.

## References

- [1] "Thin-Film Transistors," [https://en.wikipedia.org/wiki/Thin-film\\_transistor](https://en.wikipedia.org/wiki/Thin-film_transistor), 2015
- [2] T. P. Brody, "The Thin Film Transistor: A Late Flowering Bloom," *IEEE Transactions on Electron Devices*, vol. 31, p. 1614, 1984.
- [3] P. Semenza, "The Display Industry: Fast to Grow, Slow to Change," <http://informationdisplay.org>, 2012
- [4] "Display market overview," <http://www.amorphyx.com/market/overview>
- [5] "Display Market Worth \$155.54 Billion by 2020," <http://www.marketsandmarkets.com>, 2015
- [6] Y. Kuo, "Thin Film Transistor Technology - Past Present and Future," *Electrochemical Society Interface*, vol. 22, p. 55, 2013.
- [7] "Sharp Meets the Press at CES 2015," Sharp Corporation, 2015.
- [8] J. Wei, "How Wearables Intersect with the Cloud and the Internet of Things: Considerations for the Developers of Wearables," *IEEE Consumer Electronics Magazine*, vol. 3, p. 53, 2014.
- [9] A. Nathan, A. Ahnood, M. T. Cole, S. Lee, Y. Suzuki, P. Hiralal, F. Bonaccorso, T. Hasan, L. Garcia-Gancedo, A. Dyadyusha, S. Haque, P. Andrew, S. Hofmann, J. Moultrie, D. Chu, A. J. Flewitt, A. C. Ferrari, M. J. Kelly, J. Robertson, G. A. J. Amaratunga, and W. I. Milne, "Flexible Electronics: The Next Ubiquitous Platform," *Proceedings of the IEEE*, vol. 100, p. 1486, 2012.
- [10] E. Fortunato, P. Barquinha, and R. Martins, "Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances," *Advanced Materials*, vol. 24, p. 2945, 2012.
- [11] E. M. C. Fortunato, P. M. C. Barquinha, A. C. M. B. G. Pimentel, A. M. F. Gonçalves, A. J. S. Marques, L. M. N. Pereira, and R. F. P. Martins, "Fully Transparent ZnO Thin-Film Transistor Produced at Room Temperature," *Advanced Materials*, vol. 17, p. 590, 2005.
- [12] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-Temperature Fabrication of Transparent Flexible Thin-Film Transistors Using Amorphous Oxide Semiconductors," *Nature*, vol. 432, p. 488, 2004.
- [13] J. K. Jeong, J. H. Jeong, H. W. Yang, T. K. Ahn, M. Kim, K. S. Kim, B. S. Gu, H.-J. Chung, J.-S. Park, Y.-G. Mo, H. D. Kim, and H. K. Chung, "12.1-in. WXGA AMOLED Display Driven by InGaZnO Thin-Film Transistors," *Journal of the Society for Information Display*, vol. 17, p. 95, 2009.
- [14] H. Klauk, "Organic Thin-Film Transistors," *Chemical Society Reviews*, vol. 39, p. 2643, 2010.
- [15] H. Sirringhaus, "25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon," *Advanced Materials*, vol. 26, p. 1319, 2014.
- [16] H. Edzer, A. Huitema, G. H. Gelinck, P. J. G. Van Lieshout, E. Van Veenendaal, and F. J. Touwslager, "Flexible Electronic-Paper Active-Matrix Displays," *Journal of the Society for Information Display*, vol. 14, p. 729, 2006.
- [17] T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya, "Flexible Organic Transistors and Circuits with Extreme Bending Stability," *Nature Materials*, vol. 9, p. 1015, 2010.
- [18] R. F. Pierret, *Semiconductor device fundamentals*: Pearson Education India, 1996.
- [19] M. Rehahn, "Elektrisch Leitfähige Kunststoffe: Der Weg zu Einer Neuen Materialklasse," *Chemie in Unserer Zeit*, vol. 37, p. 18, 2003.
- [20] D. Khim, K.-J. Baeg, M. Caironi, C. Liu, Y. Xu, D.-Y. Kim, and Y.-Y. Noh, "Control of Ambipolar and Unipolar Transport in Organic Transistors by Selective Inkjet-Printed Chemical Doping

- for High Performance Complementary Circuits," *Advanced Functional Materials*, vol. 24, p. 6252, 2014.
- [21] S. Park, *Large Area and Flexible Electronics*: Wiley-vch.
- [22] H. Sirringhaus, "Reliability of Organic Field-Effect Transistors," *Advanced Materials*, vol. 21, p. 3859, 2009.
- [23] M. L. Chabinyo and A. Salleo, "Materials Requirements and Fabrication of Active Matrix Arrays of Organic Thin-Film Transistors for Displays," *Chemistry of Materials*, vol. 16, p. 4509, 2004.
- [24] T. Kawase, H. Sirringhaus, R. H. Friend, and T. Shimoda, "Inkjet Printed Via-Hole Interconnections and Resistors for All-Polymer Transistor Circuits," *Advanced Materials*, vol. 13, p. 1601, 2001.
- [25] K.-J. Baeg, D. Khim, D.-Y. Kim, S.-W. Jung, J. B. Koo, I.-K. You, H. Yan, A. Facchetti, and Y.-Y. Noh, "High Speeds Complementary Integrated Circuits Fabricated with All-Printed Polymeric Semiconductors," *Journal of Polymer Science*, vol. 49, p. 62, 2011.
- [26] S. Khan, L. Lorenzelli, and R. S. Dahiya, "Technologies for Printing Sensors and Electronics Over Large Flexible Substrates: A Review," *IEEE Sensors Journal*, vol. 15, p. 3164, 2015.
- [27] S. S. Lee, C. S. Kim, E. D. Gomez, B. Purushothaman, M. F. Toney, C. Wang, A. Hexemer, J. E. Anthony, and Y. L. Loo, "Controlling Nucleation and Crystallization in Solution-Processed Organic Semiconductors for Thin-Film Transistors," *Advanced Materials*, vol. 21, p. 3605, 2009.
- [28] Y. Chen, B. Lee, H. T. Yi, S. S. Lee, M. M. Payne, S. Pola, C. H. Kuo, Y. L. Loo, J. E. Anthony, Y. T. Tao, and V. Podzorov, "Dynamic Character of Charge Transport Parameters in Disordered Organic Semiconductor Field-Effect Transistors," *Physical Chemistry Chemical Physics*, vol. 14, p. 14142, 2012.
- [29] J. Li, Y. Zhao, H. S. Tan, Y. Guo, C.-A. Di, G. Yu, Y. Liu, M. Lin, S. H. Lim, Y. Zhou, H. Su, and B. S. Ong, "A Stable Solution-Processed Polymer Semiconductor with Record High-Mobility for Printed Transistors," *Scientific Reports*, vol. 2, p. 754, 2012.
- [30] C. D. Dimitrakopoulos and P. R. L. Malenfant, "Organic Thin Film Transistors for Large Area Electronics," *Advanced Materials*, vol. 14, p. 99, 2002.
- [31] G. Gelinck, P. Heremans, K. Nomoto, and T. D. Anthopoulos, "Organic Transistors in Optical Displays and Microelectronic Applications," *Advanced Materials*, vol. 22, p. 3778, 2010.
- [32] F. C. Krebs, N. Espinosa, M. Hösel, R. R. Søndergaard, and M. Jørgensen, "25th Anniversary Article: Rise to Power—OPV-Based Solar Parks," *Advanced Materials*, vol. 26, p. 29, 2014.
- [33] Y. Shao, Z. Xiao, C. Bi, Y. Yuan, and J. Huang, "Origin and Elimination of Photocurrent Hysteresis by Fullerene Passivation in  $\text{CH}_3\text{NH}_3\text{PbI}_3$  Planar Heterojunction Solar Cells," *Nature Communications*, vol. 5, p. 1, 2014.
- [34] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, "Solar Cell Efficiency Tables (Version 45)," *Progress in Photovoltaics: Research and Applications*, vol. 23, p. 1, 2015.
- [35] B. K. Crone, A. Dodabalapur, R. Sarpeshkar, R. W. Filas, Y.-Y. Lin, Z. Bao, J. H. O'Neill, W. Li, and H. E. Katz, "Design and Fabrication of Organic Complementary Circuits," *Journal of Applied Physics*, vol. 89, p. 5125, 2001.
- [36] H. Klauk, M. Halik, U. Zschieschang, F. Eder, D. Rohde, G. Schmid, and C. Dehm, "Flexible Organic Complementary Circuits," *Electron Devices, IEEE Transactions on*, vol. 52, p. 618, 2005.
- [37] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, "Ultralow-Power Organic Complementary Circuits," *Nature*, vol. 445, p. 745, 2007.

- [38] U. Zschieschang, R. Rodel, U. Kraft, K. Takimiya, T. Zaki, F. Letzkus, J. Butschke, H. Richter, J. N. Burghartz, W. Xiong, B. Murmann, and H. Klauk, "Low-Voltage Organic Transistors for Flexible Electronics," presented at the Proceedings of the conference on Design, Automation & Test in Europe, Dresden, Germany, 2014.
- [39] U. Zschieschang, F. Ante, M. Schlörholz, M. Schmidt, K. Kern, and H. Klauk, "Mixed Self-Assembled Monolayer Gate Dielectrics for Continuous Threshold Voltage Control in Organic Transistors and Circuits," *Advanced Materials*, vol. 22, p. 4489, 2010.
- [40] X.-H. Zhang, W. J. Potscavage, C. Seungkeun, and B. Kippelen, "Low-Voltage Flexible Organic Complementary Inverters with High Noise Margin and High DC Gain," *Applied Physics Letters*, vol. 94, p. 043312, 2009.
- [41] K. Takimiya, H. Ebata, K. Sakamoto, T. Izawa, T. Otsubo, and Y. Kunugi, "2,7-Diphenyl[1]benzothieno[3,2-b]benzothiophene, A New Organic Semiconductor for Air-Stable Organic Field-Effect Transistors with Mobilities up to  $2.0 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ," *Journal of the American Chemical Society*, vol. 128, p. 12604, 2006.
- [42] R. Hamilton, J. Smith, S. Ogier, M. Heeney, J. E. Anthony, I. McCulloch, J. Veres, D. D. C. Bradley, and T. D. Anthopoulos, "High-Performance Polymer-Small Molecule Blend Organic Transistors," *Advanced Materials*, vol. 21, p. 1166, 2009.
- [43] D. K. Hwang, C. Fuentes-Hernandez, J. D. Berrigan, Y. Fang, J. Kim, W. J. Potscavage, H. Cheun, K. H. Sandhage, and B. Kippelen, "Solvent and Polymer Matrix Effects on TIPS-pentacene/Polymer Blend Organic Field-Effect Transistors," *Journal of Materials Chemistry*, vol. 22, p. 5531, 2012.
- [44] Y. Diao, B. C. K. Tee, G. Giri, J. Xu, D. H. Kim, H. A. Becerril, R. M. Stoltenberg, T. H. Lee, G. Xue, S. C. B. Mannsfeld, and Z. Bao, "Solution Coating of Large-Area Organic Semiconductor Thin Films with Aligned Single-Crystalline Domains," *Nature Materials*, vol. 12, p. 665, 2013.
- [45] Y. Yuan, G. Giri, A. L. Ayzner, A. P. Zoombelt, S. C. B. Mannsfeld, J. Chen, D. Nordlund, M. F. Toney, J. Huang, and Z. Bao, "Ultra-High Mobility Transparent Organic Thin-Film Transistors Grown by an Off-Centre Spin-Coating Method," *Nature Communications*, vol. 5, p. 1, 2014.
- [46] H.-R. Tseng, L. Ying, B. B. Y. Hsu, L. A. Perez, C. J. Takacs, G. C. Bazan, and A. J. Heeger, "High Mobility Field-Effect Transistors Based on Macroscopically Oriented Regioregular Copolymers," *Nano Letters*, vol. 12, p. 6353, 2012.
- [47] X. Zhang, H. Bronstein, A. J. Kronemeijer, J. Smith, Y. Kim, R. J. Kline, L. J. Richter, T. D. Anthopoulos, H. Sirringhaus, K. Song, M. Heeney, W. Zhang, I. McCulloch, and D. M. DeLongchamp, "Molecular Origin of High Field-Effect Mobility in an Indacenodithiophene–Benzothiadiazole Copolymer," *Nature Communications*, vol. 4, p. 1, 2013.
- [48] T. Okachi, T. Kashiki, and K. Ohya, "Device Operation Mechanism of Field-Effect Transistors with High Mobility Donor-Acceptor Polymer Semiconductors," *Proceedings of the SPIE*, vol. 9568, p. 95680I, 2015.
- [49] H. Sirringhaus, "Reliability of Organic Field-Effect Transistors," *Advanced Materials*, vol. 21, p. 3859, 2009.
- [50] X.-H. Zhang, S. P. Tiwari, and B. Kippelen, "Pentacene Organic Field-Effect Transistors with Polymeric Dielectric Interfaces: Performance and Stability," *Organic Electronics*, vol. 10, p. 1133, 2009.
- [51] S. H. Kim, S. Nam, J. Jang, K. Hong, C. Yang, D. S. Chung, C. E. Park, and W.-S. Choi, "Effect of the Hydrophobicity and Thickness of Polymer Gate Dielectrics on the Hysteresis

- Behavior of Pentacene-Based Field-Effect Transistors," *Journal of Applied Physics*, vol. 105, p. 104509, 2009.
- [52] D. K. Hwang, M. S. Oh, J. M. Hwang, J. H. Kim, and S. Im, "Hysteresis Mechanisms of Pentacene Thin-Film Transistors with Polymer/Oxide Bilayer Gate Dielectrics," *Applied Physics Letters*, vol. 92, p. 013304, 2008.
- [53] D. K. Hwang, C. Fuentes-Hernandez, J. Kim, W. J. Potscavage, S.-J. Kim, and B. Kippelen, "Top-Gate Organic Field-Effect Transistors with High Environmental and Operational Stability," *Advanced Materials*, vol. 23, p. 1293, 2011.
- [54] E. D. Głowacki, M. Irimia-Vladu, M. Kaltenbrunner, J. Gsiorowski, M. S. White, U. Monkowius, G. Romanazzi, G. P. Suranna, P. Mastrorilli, T. Sekitani, S. Bauer, T. Someya, L. Torsi, and N. S. Sariciftci, "Hydrogen-Bonded Semiconducting Pigments for Air-Stable Field-Effect Transistors," *Advanced Materials*, vol. 25, p. 1563, 2013.
- [55] D. K. Hwang, C. Fuentes-Hernandez, M. Fenoll, M. Yun, J. Park, J. W. Shim, K. A. Knauer, A. Dindar, H. Kim, Y. Kim, J. Kim, H. Cheun, M. M. Payne, S. Graham, S. Im, J. E. Anthony, and B. Kippelen, "Systematic Reliability Study of Top-Gate p- and n-Channel Organic Field-Effect Transistors," *ACS Applied Materials & Interfaces*, vol. 6, p. 3378, 2014.
- [56] M. Yun, A. Sharma, C. Fuentes-Hernandez, D. K. Hwang, A. Dindar, S. Singh, S. Choi, and B. Kippelen, "Stable Organic Field-Effect Transistors for Continuous and Nondestructive Sensing of Chemical and Biologically Relevant Molecules in Aqueous Environment," *ACS Applied Materials & Interfaces*, vol. 6, p. 1616, 2014.
- [57] K. Kuribara, H. Wang, N. Uchiyama, K. Fukuda, T. Yokota, U. Zschieschang, C. Jaye, D. Fischer, H. Klauk, T. Yamamoto, K. Takimiya, M. Ikeda, H. Kuwabara, T. Sekitani, Y.-L. Loo, and T. Someya, "Organic Transistors with High Thermal Stability for Medical Applications," *Nature Communications*, vol. 3, p. 723, 2012.
- [58] Y. Chen, J. Au, P. Kazlas, A. Ritenour, H. Gates, and M. McCreary, "Electronic Paper: Flexible Active-Matrix Electronic Ink Display," *Nature*, vol. 423, p. 136, 2003.
- [59] M. Zirkl, A. Haase, A. Fian, H. Schon, C. Sommer, G. Jakopic, G. Leising, B. Stadlober, I. Graz, and N. Gaar, "Low-Voltage Organic Thin-Film Transistors with High-k Nanocomposite Gate Dielectrics for Flexible Electronics and Optothermal Sensors," *Advanced Materials*, vol. 19, p. 2241, 2007.
- [60] M. Drack, I. Graz, T. Sekitani, T. Someya, M. Kaltenbrunner, and S. Bauer, "An Imperceptible Plastic Electronic Wrap," *Advanced Materials*, vol. 27, p. 34, 2015.
- [61] D. K. Hwang, C. Fuentes-Hernandez, J. Kim, W. J. Potscavage Jr, and B. Kippelen, "Flexible and Stable Solution-Processed Organic Field-Effect Transistors," *Organic Electronics*, vol. 12, p. 1108, 2011.
- [62] D. K. Hwang, R. R. Dasari, M. Fenoll, V. Alain-Rizzo, A. Dindar, J. W. Shim, N. Deb, C. Fuentes-Hernandez, S. Barlow, and D. G. Bucknall, "Stable Solution-Processed Molecular n-Channel Organic Field-Effect Transistors," *Advanced Materials*, vol. 24, p. 4445, 2012.
- [63] G. H. Gelinck, H. E. A. Huitema, E. van Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. P. H. van der Putten, T. C. T. Geuns, M. Beenhakkers, J. B. Giesbers, B.-H. Huisman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. van Rens, and D. M. de Leeuw, "Flexible Active-Matrix Displays and Shift Registers Based on Solution-Processed Organic Transistors," *Nature Materials*, vol. 3, p. 106, 2004.
- [64] T. Someya, Y. Kato, T. Sekitani, S. Iba, Y. Noguchi, Y. Murase, H. Kawaguchi, and T. Sakurai, "Conformable, Flexible, Large-Area Networks of Pressure and Thermal Sensors with Organic Transistor Active Matrixes," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 102, p. 12321, 2005.

- [65] C.-Y. Wang, C. Fuentes-Hernandez, J.-C. Liu, A. Dindar, S. Choi, J. P. Youngblood, R. J. Moon, and B. Kippelen, "Stable Low-Voltage Operation Top-Gate Organic Field-Effect Transistors on Cellulose Nanocrystal Substrates," *ACS Applied Materials & Interfaces*, vol. 7, p. 4804, 2015.
- [66] J. Reeder, M. Kaltenbrunner, T. Ware, D. Arreaga-Salas, A. Avendano-Bolivar, T. Yokota, Y. Inoue, M. Sekino, W. Voit, T. Sekitani, and T. Someya, "Mechanically Adaptive Organic Transistors for Implantable Electronics," *Advanced Materials*, vol. 26, p. 4967, 2014.
- [67] A. Avendano-Bolivar, T. Ware, D. Arreaga-Salas, D. Simon, and W. Voit, "Mechanical Cycling Stability of Organic Thin-Film Transistors on Shape-Memory Polymers," *Advanced Materials*, vol. 25, p. 3095, 2013.
- [68] S. Choi, C. Fuentes-Hernandez, C.-Y. Wang, A. Wei, W. Voit, Y. Zhang, S. Barlow, S. R. Marder, and B. Kippelen, "Top-Gate Organic Field-Effect Transistors Fabricated on Shape-Memory Polymer Substrates," *Proceedings of the SPIE*, vol. 9568, p. 95680A, 2015.
- [69] H. Wang, Y. Wang, B. C. K. Tee, K. Kim, J. Lopez, W. Cai, and Z. Bao, "Shape-Controlled, Self-Wrapped Carbon Nanotube 3D Electronics," *Advanced Science*, p. 1, 2015.
- [70] Y. Liu, J. K. Boyles, J. Genzer, and M. D. Dickey, "Self-Folding of Polymer Sheets Using Local Light Absorption," *Soft Matter*, vol. 8, p. 1764, 2012.
- [71] H. Lu, F. Liang, Y. Yao, J. Gou, and D. Hui, "Self-Assembled Multi-Layered Carbon Nanofiber Nanopaper for Significantly Improving Electrical Actuation of Shape Memory Polymer Nanocomposite," *Composites Part B: Engineering*, vol. 59, p. 191, 2014.
- [72] B. Crone, A. Dodabalapur, Y. Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz, and W. Li, "Large-Scale Complementary Integrated Circuits Based on Organic Transistors," *Nature*, vol. 403, p. 521, 2000.
- [73] K. Myny, E. van Veenendaal, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "An 8-Bit, 40-Instructions-Per-Second Organic Microprocessor on Plastic Foil," *IEEE Journal of Solid-State Circuits*, vol. 47, p. 284, 2012.
- [74] H. Yan, Y. Zheng, R. Blache, C. Newman, S. Lu, J. Woerle, and A. Facchetti, "Solution Processed Top-Gate n-Channel Transistors and Complementary Circuits on Plastics Operating in Ambient Conditions," *Advanced Materials*, vol. 20, p. 3393, 2008.
- [75] H. Yan, Z. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dotz, M. Kastler, and A. Facchetti, "A High-Mobility Electron-Transporting Polymer for Printed Transistors," *Nature*, vol. 457, p. 679, 2009.
- [76] K. Sung Hoon, L. Sun Hee, K. Youn Goo, and J. Jin, "Ink-Jet-Printed Organic Thin-Film Transistors for Low-Voltage-Driven CMOS Circuits With Solution-Processed AlO<sub>x</sub> Gate Insulator," *Electron Device Letters, IEEE*, vol. 34, p. 307, 2013.
- [77] K. Sung Hoon, L. Sun Hee, K. Youn Goo, and J. Jin, "Ink-Jet-Printed Organic Thin-Film Transistors for Low-Voltage-Driven CMOS Circuits With Solution-Processed AlO<sub>x</sub> Gate Insulator," *IEEE Electron Device Letters*, vol. 34, p. 307, 2013.
- [78] J. Henzie, J. E. Barton, C. L. Stender, and T. W. Odom, "Large-Area Nanoscale Patterning: Chemistry Meets Fabrication," *Accounts of Chemical Research*, vol. 39, p. 249, 2006.
- [79] J.-F. Chang and H. Sirringhaus, "Patterning of Solution-Processed Semiconducting Polymers in High-Mobility Thin-Film Transistors by Physical Delamination," *Advanced Materials*, vol. 21, p. 2530, 2009.
- [80] S. Liu, H. A. Becerril, M. C. LeMieux, W. M. Wang, J. H. Oh, and Z. Bao, "Direct Patterning of Organic-Thin-Film-Transistor Arrays via a "Dry-Taping" Approach," *Advanced Materials*, vol. 21, p. 1266, 2009.
- [81] D. J. Gundlach, J. E. Royer, S. K. Park, S. Subramanian, O. D. Jurchescu, B. H. Hamadani, A. J. Moad, R. J. Kline, L. C. Teague, O. Kirillov, C. A. Richter, J. G. Kushmerick, L. J. Richter, S.

- R. Parkin, T. N. Jackson, and J. E. Anthony, "Contact-Induced Crystallinity for High-Performance Soluble Acene-Based Transistors and Circuits," *Nature Materials*, vol. 7, p. 216, 2008.
- [82] J.-P. Hong, A.-Y. Park, S. Lee, J. Kang, N. Shin, and D. Y. Yoon, "Tuning of Ag Work Functions by Self-Assembled Monolayers of Aromatic Thiols for an Efficient Hole Injection for Solution-Processed Triisopropylsilylethynyl Pentacene Organic Thin Film Transistors," *Applied Physics Letters*, vol. 92, p. 143311, 2008.
- [83] S. K. Park, D. A. Mourey, S. Subramanian, J. E. Anthony, and T. N. Jackson, "High-Mobility Spin-Cast Organic Thin-Film Transistors," *Applied Physics Letters*, vol. 93, p. 043301, 2008.
- [84] M. H. Choi, S. H. Lee, S. H. Kim, J. Jang, and S. K. Kwon, "79.3: Effect of Surface Treatment on the Performance of TIPS Pentacene TFT by Inkjet Printing," *SID Symposium Digest of Technical Papers*, vol. 41, p. 1180, 2010.
- [85] H. Kang, N.-S. Lee, E. Ito, M. Hara, and J. Noh, "Formation and Superlattice of Long-Range-Ordered Self-Assembled Monolayers of Pentafluorobenzenethiols on Au(111)," *Langmuir*, vol. 26, p. 2983, 2010.
- [86] J. Smith, R. Hamilton, Y. Qi, A. Kahn, D. D. Bradley, M. Heeney, I. McCulloch, and T. D. Anthopoulos, "The Influence of Film Morphology in High-Mobility Small-Molecule: Polymer Blend Organic Transistors," *Advanced Functional Materials*, vol. 20, p. 2330, 2010.
- [87] S. H. Kim, I. Kang, Y. G. Kim, H. R. Hwang, Y.-H. Kim, S.-K. Kwon, and J. Jang, "High Performance Ink-Jet Printed Diketopyrrolopyrrole-Based Copolymer Thin-Film Transistors Using a Solution-Processed Aluminium Oxide Dielectric on a Flexible Substrate," *Journal of Materials Chemistry C*, vol. 1, p. 2408, 2013.
- [88] J. Chang, X. Zhang, T. Ge, and J. Zhou, "Fully Printed Electronics on Flexible Substrates: High Gain Amplifiers and DAC," *Organic Electronics*, vol. 15, p. 701, 2014.
- [89] X. Hou, Y. Xia, S. C. Ng, J. Zhang, and J. S. Chang, "Formulation of Novel Screen-Printable Dielectric Ink for Fully-Printed TIPS-pentacene OFETs," *RSC Advances*, vol. 4, p. 37687, 2014.
- [90] A. Risteska, S. Steudel, M. Nakamura, and D. Knipp, "Structural Ordering Versus Energy Band Alignment: Effects of Self-Assembled Monolayers on the Metal/Semiconductor Interfaces of Small Molecule Organic Thin-Film Transistors," *Organic Electronics*, vol. 15, p. 3723, 2014.
- [91] O. Fenwick, C. Van Dyck, K. Murugavel, D. Cornil, F. Reinders, S. Haar, M. Mayor, J. Cornil, and P. Samori, "Modulating the Charge Injection in Organic Field-Effect Transistors: Fluorinated Oligophenyl Self-Assembled Monolayers for High Work Function Electrodes," *Journal of Materials Chemistry C*, vol. 3, p. 3007, 2015.
- [92] J. E. Crowell, "Chemical Methods of Thin Film Deposition: Chemical Vapor Deposition, Atomic Layer Deposition, and Related Technologies," *Journal of Vacuum Science & Technology A*, vol. 21, p. S88, 2003.
- [93] M. P. Gaj, A. Wei, C. Fuentes-Hernandez, Y. Zhang, R. Reit, W. Voit, S. R. Marder, and B. Kippelen, "Organic Light-Emitting Diodes on Shape-Memory Polymer Substrates for Wearable Electronics," *Organic Electronics*, vol. 25, p. 151, 2015.
- [94] L. Zhang, A. Fonari, Y. Liu, A.-L. M. Hoyt, H. Lee, D. Granger, S. Parkin, T. P. Russell, J. E. Anthony, J.-L. Brédas, V. Coropceanu, and A. L. Briseno, "Bistetracene: An Air-Stable, High-Mobility Organic Semiconductor with Extended Conjugation," *Journal of the American Chemical Society*, vol. 136, p. 9248, 2014.
- [95] J. Smith, W. Zhang, R. Sougrat, K. Zhao, R. Li, D. Cha, A. Amassian, M. Heeney, I. McCulloch, and T. D. Anthopoulos, "Solution-Processed Small Molecule-Polymer Blend Organic Thin-



- Film Transistors with Hole Mobility Greater than  $5 \text{ cm}^2/\text{Vs}$ ," *Advanced Materials*, vol. 24, p. 2441, 2012.
- [96] X. H. Zhang, W. J. Potscavage, S. Choi, and B. Kippelen, "Low-Voltage Flexible Organic Complementary Inverters With High Noise Margin and High DC Gain," *Applied Physics Letters*, vol. 94, p. 043312, 2009.
- [97] L. Bürgi, T. J. Richards, R. H. Friend, and H. Sirringhaus, "Close Look at Charge Carrier Injection in Polymer Field-Effect Transistors," *Journal of Applied Physics*, vol. 94, p. 6129, 2003.
- [98] V. I. Arkhipov, E. V. Emelianova, Y. H. Tak, and H. Bässler, "Charge Injection into Light-Emitting Diodes: Theory and Experiment," *Journal of Applied Physics*, vol. 84, p. 848, 1998.
- [99] L. Bürgi, H. Sirringhaus, and R. H. Friend, "Noncontact Potentiometry of Polymer Field-Effect Transistors," *Applied Physics Letters*, vol. 80, p. 2913, 2002.
- [100] T. J. Richards and H. Sirringhaus, "Analysis of the Contact Resistance in Staggered, Top-Gate Organic Field-Effect Transistors," *Journal of Applied Physics*, vol. 102, p. 094510, 2007.
- [101] C. Liu, Y. Xu, and Y.-Y. Noh, "Contact Engineering in Organic Field-Effect Transistors," *Materials Today*, vol. 18, p. 79, 2015.
- [102] M. Kröger, S. Hamwi, J. Meyer, T. Riedl, W. Kowalsky, and A. Kahn, "Role of the Deep-Lying Electronic States of  $\text{MoO}_3$  in the Enhancement of Hole-Injection in Organic Thin Films," *Applied Physics Letters*, vol. 95, p. 123301, 2009.
- [103] J. Meyer, R. Khalandovsky, P. Görrn, and A. Kahn, " $\text{MoO}_3$  Films Spin-Coated from a Nanoparticle Suspension for Efficient Hole-Injection in Organic Electronics," *Advanced Materials*, vol. 23, p. 70, 2011.
- [104] Z. Wang, M. Waqas Alam, Y. Lou, S. Naka, and H. Okada, "Enhanced Carrier Injection in Pentacene Thin-Film Transistors by Inserting a  $\text{MoO}_3$ -Doped Pentacene Layer," *Applied Physics Letters*, vol. 100, p. 043302, 2012.
- [105] M. Kano, T. Minari, and K. Tsukagoshi, "Improvement of Subthreshold Current Transport by Contact Interface Modification in p-Type Organic Field-Effect Transistors," *Applied Physics Letters*, vol. 94, p. 143304, 2009.
- [106] Y. Abe, T. Hasegawa, Y. Takahashi, T. Yamada, and Y. Tokura, "Control of Threshold Voltage in Pentacene Thin-Film Transistors Using Carrier Doping at the Charge-Transfer Interface with Organic Acceptors," *Applied Physics Letters*, vol. 87, p. 153506, 2005.
- [107] T. Minari, T. Miyadera, K. Tsukagoshi, Y. Aoyagi, and H. Ito, "Charge Injection Process in Organic Field-Effect Transistors," *Applied Physics Letters*, vol. 91, p. 053508, 2007.
- [108] A. Davison, R. H. Holm, R. E. Benson, and W. Mahler, "Metal Complexes Derived from Cis-1,2-dicyano-1,2-ethylenedithiolate and Bis(Trifluoromethyl)-1,2-dithiete," *Inorganic Syntheses*, p. 8, 1967.
- [109] Y. Qi, T. Sajoto, S. Barlow, E.-G. Kim, J.-L. Brédas, S. R. Marder, and A. Kahn, "Use of a High Electron-Affinity Molybdenum Dithiolene Complex to p-dope Hole-Transport Layers," *Journal of the American Chemical Society*, vol. 131, p. 12530, 2009.
- [110] Y. Qi, T. Sajoto, M. Kröger, A. M. Kandabarow, W. Park, S. Barlow, E.-G. Kim, L. Wielunski, L. C. Feldman, R. A. Bartynski, J.-L. Brédas, S. R. Marder, and A. Kahn, "A Molybdenum Dithiolene Complex as p-Dopant for Hole-Transport Materials: A Multitechnique Experimental and Theoretical Investigation," *Chemistry of Materials*, vol. 22, p. 524, 2010.
- [111] S. P. Tiwari, W. J. Potscavage Jr, T. Sajoto, S. Barlow, S. R. Marder, and B. Kippelen, "Pentacene Organic Field-Effect Transistors with Doped Electrode-Semiconductor Contacts," *Organic Electronics*, vol. 11, p. 860, 2010.

- [112] W. Zhao, Y. Qi, T. Sajoto, S. Barlow, S. R. Marder, and A. Kahn, "Remote Doping of a Pentacene Transistor: Control of Charge Transfer by Molecular-level Engineering," *Applied Physics Letters*, vol. 97, p. 123305, 2010.
- [113] Y. Zhou, C. Fuentes-Hernandez, J. Shim, J. Meyer, A. J. Giordano, H. Li, P. Winget, T. Papadopoulos, H. Cheun, J. Kim, M. Fenoll, A. Dindar, W. Haske, E. Najafabadi, T. M. Khan, H. Sojoudi, S. Barlow, S. Graham, J.-L. Brédas, S. R. Marder, A. Kahn, and B. Kippelen, "A Universal Method to Produce Low-Work Function Electrodes for Organic Electronics," *Science*, vol. 336, p. 327, 2012.
- [114] J. Hwang, A. Wan, and A. Kahn, "Energetics of Metal–Organic Interfaces: New Experiments and Assessment of the Field," *Materials Science and Engineering R*, vol. 64, p. 1, 2009.
- [115] C. Tengstedt, W. Osikowicz, W. R. Salaneck, I. D. Parker, C.-H. Hsu, and M. Fahlman, "Fermi-Level Pinning at Conjugated Polymer Interfaces," *Applied Physics Letters*, vol. 88, p. 053502, 2006.
- [116] J. Hwang, E.-G. Kim, J. Liu, J.-L. Brédas, A. Duggal, and A. Kahn, "Photoelectron Spectroscopic Study of the Electronic Band Structure of Polyfluorene and Fluorene-Arylamine Copolymers at Interfaces," *The Journal of Physical Chemistry C*, vol. 111, p. 1378, 2007.
- [117] M. Oehzelt, N. Koch, and G. Heimel, "Organic Semiconductor Density of States Controls the Energy Level Alignment at Electrode Interfaces," *Nature Communications*, vol. 5, p. 1, 2014.
- [118] R. J. Davis, M. T. Lloyd, S. R. Ferreira, M. J. Bruzek, S. E. Watkins, L. Lindell, P. Sehati, M. Fahlman, J. E. Anthony, and J. W. P. Hsu, "Determination of Energy Level Alignment at Interfaces of Hybrid and Organic Solar Cells under Ambient Environment," *Journal of Materials Chemistry*, vol. 21, p. 1721, 2011.
- [119] D. J. Gundlach, L. Zhou, J. A. Nichols, T. N. Jackson, P. V. Necliudov, and M. S. Shur, "An Experimental Study of Contact Effects in Organic Thin-Film Transistors," *Journal of Applied Physics*, vol. 100, p. 024509, 2006.
- [120] K. Seshadri and C. D. Frisbie, "Potentiometry of an Operating Organic Semiconductor Field-Effect Transistor," *Applied Physics Letters*, vol. 78, p. 993, 2001.
- [121] G. Horowitz, P. Lang, M. Mottaghi, and H. Aubin, "Extracting Parameters from the Current–Voltage Characteristics of Organic Field-Effect Transistors," *Advanced Functional Materials*, vol. 14, p. 1069, 2004.
- [122] Y. Xu, R. Gwoziecki, I. Chartier, R. Coppard, F. Balestra, and G. Ghibaudo, "Modified Transmission-Line Method for Contact Resistance Extraction in Organic Field-Effect Transistors," *Applied Physics Letters*, vol. 97, p. 063302, 2010.
- [123] C. Liu, Y. Xu, G. Ghibaudo, X. Lu, T. Minari, and Y.-Y. Noh, "Evaluating Injection and Transport Properties of Organic Field-Effect Transistors by the Convergence Point in Transfer-Length Method," *Applied Physics Letters*, vol. 104, p. 013301, 2014.
- [124] P. V. Pesavento, R. J. Chesterfield, C. R. Newman, and C. D. Frisbie, "Gated Four-Probe Measurements on Pentacene Thin-Film Transistors: Contact Resistance as a Function of Gate Voltage and Temperature," *Journal of Applied Physics*, vol. 96, p. 7312, 2004.
- [125] H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C. D. Sheraw, J. A. Nichols, and T. N. Jackson, "Contact Resistance in Organic Thin-Film Transistors," *Solid-State Electronics*, vol. 47, p. 297, 2003.
- [126] E. J. Meijer, G. H. Gelinck, E. van Veenendaal, B.-H. Huisman, D. M. de Leeuw, and T. M. Klapwijk, "Scaling Behavior and Parasitic Series Resistance in Disordered Organic Field-Effect Transistors," *Applied Physics Letters*, vol. 82, p. 4576, 2003.

- [127] S. P. Tiwari, X.-H. Zhang, W. J. Potscavage, and B. Kippelen, "Study of Electrical Performance and Stability of Solution-Processed n-Channel Organic Field-Effect Transistors," *Journal of Applied Physics*, vol. 106, p. 054504, 2009.
- [128] F. Fujimori, K. Shigeto, T. Hamano, T. Minari, T. Miyadera, K. Tsukagoshi, and Y. Aoyagi, "Current Transport in Short Channel Top-Contact Pentacene Field-Effect Transistors Investigated with the Selective Molecular Doping Technique," *Applied Physics Letters*, vol. 90, p. 193507, 2007.
- [129] T. Minari, P. Darmawan, C. Liu, Y. Li, Y. Xu, and K. Tsukagoshi, "Highly Enhanced Charge Injection in Thienoacene-Based Organic Field-Effect Transistors with Chemically Doped Contact," *Applied Physics Letters*, vol. 100, p. 093303, 2012.
- [130] P. Darmawan, T. Minari, Y. Xu, S.-L. Li, H. Song, M. Chan, and K. Tsukagoshi, "Optimal Structure for High-Performance and Low-Contact-Resistance Organic Field-Effect Transistors Using Contact-Doped Coplanar and Pseudo-Staggered Device Architectures," *Advanced Functional Materials*, vol. 22, p. 4577, 2012.
- [131] C. Vanoni, S. Tsujino, and T. A. Jung, "Reduction of the Contact Resistance by Doping in Pentacene Few Monolayers Thin-Film Transistors and Self-Assembled Nanocrystals," *Applied Physics Letters*, vol. 90, p. 193119, 2007.
- [132] C. Vanoni, T. A. Jung, and S. Tsujino, "Temperature Dependent Charge-Injection at the Metal-Organic Semiconductor Interface and Density of States in Pristine and Doped Pentacene," *Applied Physics Letters*, vol. 94, p. 253306, 2009.
- [133] Y. Yamagishi, K. Noda, H. Yamada, and K. Matsushige, "Organic Field-Effect Transistors with Molecularly Doped Polymer Gate Buffer Layer," *Synthetic Metals*, vol. 162, p. 1887, 2012.
- [134] S. Nicht, H. Kleemann, A. Fischer, K. Leo, and B. Lüssem, "Functionalized p-Dopants as Self-Assembled Monolayers for Enhanced Charge Carrier Injection in Organic Electronic Devices," *Organic Electronics*, vol. 15, p. 654, 2014.
- [135] T. Menke, D. Ray, H. Kleemann, M. P. Hein, K. Leo, and M. Riede, "Highly Efficient p-Dopants in Amorphous Hosts," *Organic Electronics*, vol. 15, p. 365, 2014.
- [136] M. Kröger, S. Hamwi, J. Meyer, T. Riedl, W. Kowalsky, and A. Kahn, "P-Type Doping of Organic Wide Band Gap Materials by Transition Metal Oxides: A Case-Study on Molybdenum Trioxide," *Organic Electronics*, vol. 10, p. 932, 2009.
- [137] M. C. Gwinner, R. D. Pietro, Y. Vaynzof, K. J. Greenberg, P. K. H. Ho, R. H. Friend, and H. Sirringhaus, "Doping of Organic Semiconductors Using Molybdenum Trioxide: a Quantitative Time-Dependent Electrical and Spectroscopic Study," *Advanced Functional Materials*, vol. 21, p. 1432, 2011.
- [138] T. H. Lee, B. Lüssem, K. Kim, G. Giri, Y. Nishi, and Z. Bao, "p-Channel Field-Effect Transistors Based on C<sub>60</sub> Doped with Molybdenum Trioxide," *ACS Applied Materials & Interfaces*, vol. 5, p. 2337, 2013.
- [139] J. H. Oh, P. Wei, and Z. Bao, "Molecular n-Type Doping for Air-Stable Electron Transport in Vacuum-Processed n-Channel Organic Transistors," *Applied Physics Letters*, vol. 97, p. 243305, 2010.
- [140] S. Guo, S. K. Mohapatra, A. Romanov, T. V. Timofeeva, K. I. Hardcastle, K. Yesudas, C. Risko, J.-L. Brédas, S. R. Marder, and S. Barlow, "n-Doping of Organic Electronic Materials Using Air-Stable Organometallics: A Mechanistic Study of Reduction by Dimeric Sandwich Compounds," *Chemistry – A European Journal*, vol. 18, p. 14760, 2012.
- [141] S. Singh, S. K. Mohapatra, A. Sharma, C. Fuentes-Hernandez, S. Barlow, S. R. Marder, and B. Kippelen, "Reduction of Contact Resistance by Selective Contact Doping in Fullerene n-

- Channel Organic Field-Effect Transistors," *Applied Physics Letters*, vol. 102, p. 153303, 2013.
- [142] A. Kyaw, X. Sun, C. Jiang, G. Lo, D. Zhao, and D. Kwong, "An Inverted Organic Solar Cell Employing a Sol-Gel Derived ZnO Electron Selective Layer and Thermal Evaporated MoO<sub>3</sub> Hole Selective Layer," *Applied Physics Letters*, vol. 93, p. 221107, 2008.
- [143] J. Subbiah and F. So, "Energy Level Evolution of Air and Oxygen Exposed Molybdenum Trioxide Films," *Applied Physics Letters*, vol. 96, p. 243307, 2010.
- [144] S. Logan, J. E. Donaghey, W. Zhang, I. McCulloch, and A. J. Campbell, "Compatibility of Amorphous Triarylamine Copolymers with Solution-Processed Hole Injecting Metal Oxide Bottom Contacts," *Journal of Materials Chemistry C*, vol. 3, p. 4530, 2015.
- [145] G. Gutierrez-Heredia, V. H. Martinez-Landeros, F. S. Aguirre-Tostado, P. Shah, B. E. Gnade, M. Sotelo-Lerma, and M. A. Quevedo-Lopez, "Full Bridge Circuit Based on Pentacene Schottky Diodes Fabricated on Plastic Substrates," *Semiconductor Science and Technology*, vol. 27, p. 085013, 2012.
- [146] K.-J. Baeg, J. Kim, D. Khim, M. Caironi, D.-Y. Kim, I.-K. You, J. R. Quinn, A. Facchetti, and Y.-Y. Noh, "Charge Injection Engineering of Ambipolar Field-Effect Transistors for High-Performance Organic Complementary Circuits," *ACS Applied Materials & Interfaces*, vol. 3, p. 3205, 2011.
- [147] J. R. Bakke, K. L. Pickrahn, T. P. Brennan, and S. F. Bent, "Nanoengineering and Interfacial Engineering of Photovoltaics by Atomic Layer Deposition," *Nanoscale*, vol. 3, p. 3482, 2011.
- [148] X.-H. Zhang, B. Domercq, X. Wang, S. Yoo, T. Kondo, Z. L. Wang, and B. Kippelen, "High-Performance Pentacene Field-Effect Transistors Using Al<sub>2</sub>O<sub>3</sub> Gate Dielectrics Prepared by Atomic Layer Deposition (ALD)," *Organic Electronics*, vol. 8, p. 718, 2007.
- [149] P. Poodt, A. Lankhorst, F. Roozeboom, K. Spee, D. Maas, and A. Vermeer, "High-Speed Spatial Atomic-Layer Deposition of Aluminum Oxide Layers for Solar Cell Passivation," *Advanced Materials*, vol. 22, p. 3564, 2010.
- [150] X.-H. Zhang and B. Kippelen, "High-Performance C<sub>60</sub> n-Channel Organic Field-Effect Transistors Through Optimization of Interfaces," *Journal of Applied Physics*, vol. 104, p. 104504, 2008.
- [151] G. Gutiérrez-Heredia, L. A. González, H. N. Alshareef, B. E. Gnade, and M. Quevedo-López, "A Flexible Organic Active Matrix Circuit Fabricated Using Novel Organic Thin-Film Transistors and Organic Light-Emitting Diodes," *Semiconductor Science and Technology*, vol. 25, p. 115001, 2010.
- [152] M. Yan, Y. Koide, J. R. Babcock, P. R. Markworth, J. A. Belot, T. J. Marks, and R. P. H. Chang, "Selective-Area Atomic Layer Epitaxy Growth of ZnO Features on Soft Lithography-Patterned Substrates," *Applied Physics Letters*, vol. 79, p. 1709, 2001.
- [153] A. Sinha, C. Henderson, and D. W. Hess, "Area Selective Atomic Layer Deposition of Titanium Dioxide," *ECS Transactions*, vol. 3, p. 233, 2007.
- [154] D. H. Levy, C. R. Ellinger, and S. F. Nelson, "Metal-Oxide Thin-Film Transistors Patterned by Printing," *Applied Physics Letters*, vol. 103, p. 043505, 2013.
- [155] S. Choi, C. Fuentes-Hernandez, M. Yun, A. Dindar, T. M. Khan, C.-Y. Wang, and B. Kippelen, "Organic Field-Effect Transistor Circuits Using Atomic Layer Deposited Gate Dielectrics Patterned by Reverse Stamping," *Organic Electronics*, vol. 15, p. 3780, 2014.
- [156] T. Someya, A. Dodabalapur, J. Huang, K. C. See, and H. E. Katz, "Chemical and Physical Sensing by Organic Field-Effect Transistors and Related Devices," *Advanced Materials*, vol. 22, p. 3799, 2010.

- [157] T. Ware, D. Simon, D. E. Arreaga-Salas, J. Reeder, R. Rennaker, E. W. Keefer, and W. Voit, "Fabrication of Responsive, Softening Neural Interfaces," *Advanced Functional Materials*, vol. 22, p. 3470, 2012.
- [158] P. T. Mather, X. Luo, and I. A. Rousseau, "Shape Memory Polymer Research," *Annual Review of Materials Research*, vol. 39, p. 445, 2009.
- [159] H. Meng and G. Li, "A Review of Stimuli-responsive Shape Memory Polymer Composites," *Polymer*, vol. 54, p. 2199, 2013.
- [160] A. Bulusu, A. Singh, C. Y. Wang, A. Dindar, C. Fuentes-Hernandez, H. Kim, D. Cullen, B. Kippelen, and S. Graham, "Engineering the Mechanical Properties of UltrabARRIER Films Grown by Atomic Layer Deposition for the Encapsulation of Printed Electronics," *Journal of Applied Physics*, vol. 118, p. 085501, 2015.
- [161] P. F. Carcia, R. S. McLean, Z. G. Li, M. H. Reilly, and W. J. Marshall, "Permeability and Corrosion in  $ZrO_2/Al_2O_3$  Nanolaminate and  $Al_2O_3$  Thin Films Grown by Atomic Layer Deposition on Polymers," *Journal of Vacuum Science & Technology A*, vol. 30, p. 041515, 2012.
- [162] A. Bulusu, H. Kim, D. Samet, and J. S. Graham, "Improving the Stability of Atomic Layer Deposited Alumina Films in Aqueous Environments with Metal Oxide Capping Layers," *Journal of Physics D: Applied Physics*, vol. 46, p. 084014, 2013.