A New Method for Fault Current Limiting and Voltage Compensating in Power Systems Using Active Superconducting Current Controller

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Abstract

In this paper, a new method for both fault current limiting and voltage compensating using Active Superconducting Current Controller (ASCC) is proposed. The main objective of this paper is to present an appropriate control strategy for ASCC to achieve both the fault current limiting and voltage compensation purposes. Three different operating modes are defined for ASCC including normal mode, fault current limiting mode, and voltage compensation mode and a proper control strategy is designed for each mode. For the fault current limiting, the model of a typical three-phase system with ASCC is simulated and different states for current limiting in different levels are defined. Also, for the voltage compensating mode, the PI model for the line is considered and the line transmission matrix is obtained when the ASCC is connected at the sending end and middle of the line. Finally, proper settings for ASCC are determined such that the magnitude of the receiving end and the sending end voltages become equal. Simulation results using MATLAB software confirm the proper performance of the proposed method.

Keywords: active superconducting current controller, fault current limiters, reactive power control, series voltage compensator

1. Introduction

The recent growth of power generation capacity and application of the new distributed generation units in the micro-grids have increased the short circuit capacity of power systems. Increasing the short circuit level can cause damage to the circuit breakers and other protection devices on the power system [1]. Application of the fault current limiters (FCLs) can be an effective solution for this problem [2]. Different types of FCLs have been introduced in the literature such as superconducting type [3], transformer type [4-6], ferromagnetic materials type [7], saturated core type [8] and active superconducting type [9]. The performance of these FCLs is such that they provide a very low series impedance in the normal condition and suddenly apply large series impedance to the network when a fault occurs.

Active superconducting current controller (ASCC), as a new generation of series compensators, is a combination of superconductor technology and power electronic devices [10]. This type of FCL is not only able to decrease the fault current continuously at different levels but also can compensate the reactive powers in the power system. According to Fig. 1, the ASCC consists of three air-core superconducting transformers and one three-phase PWM converter. The air-core superconducting transformer has some advantages such as the absence of iron losses and magnetic saturation, and it has a greater possibility of a reduction in size and weight than the conventional and the iron-core superconducting transformer. In the normal state, the primary voltage is compensated to zero, but in the fault conditions, it is controlled through the output voltage of the converter. Consequently, the fault current can be limited to different levels [11].

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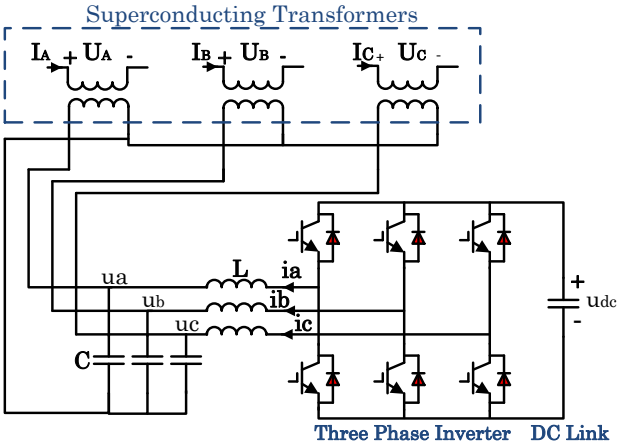


Fig. 1 Equivalent circuit of a three-phase ASCC [9]

In recent years, several methods have been presented in the literature for adjusting the ASCC to reduce the fault current at different levels. An experimental investigation of an active superconducting current controller has been studied in [11]. This reference presents parts of the important test results, including the capability of voltage regulation of the voltage source converter, and the characteristic of the system current controller in a laboratory power system. Analysis of an active SFCL by designing of control strategies for fault detection and PWM converter of ASCC is investigated in [12]. In this paper, only two operational modes, including normal mode and fault mode are defined for ASCC and the reference signals corresponding to these 2 modes are applied to the controller. Analysis of the effect of ASCC on the transient stability and the operation of the overcurrent relays (OCRs) operation has been studied in [13]. The operation principle of an active superconducting fault current limiter (SFCL) by defining the proper normal and fault operating modes is presented in [15]. The control strategy for the three-phase PWM converter of the active SFCL has been designed in [16] using a double-loop control strategy, consisting of an outer voltage loop and an inner current loop. In [19], improvement of protection coordination of overcurrent relays using a unidirectional fault current limiter has been studied. The objective is to estimate the optimal value of the FCL resistance which provides proper coordination time intervals between overcurrent relays in a distribution system.

In previous studies, the hybrid performance of ASCC in both modes of the current limiting and reactive power control has not been considered. In this paper, the current limiting, as well as the line compensation, is done only with the presence of ASSC and without using the line compensators. In the proposed method, the ASCC is controlled such that in the fault condition, the fault current is reduced to the acceptable levels by generating the appropriate limiting impedances. On the other hand, in the normal condition, the ASCC dynamically compensates the voltage drop caused by the loads. Fault current limitation, reactive power control in power transmission and distribution systems, and protective coordination of overcurrent relays in the grid-connected micro-grid without changing the setting parameters of relays are some applications of the proposed method in power systems.

This paper is organized as follows. Section 2 describes the different operating modes which are defined for ASCC and the design of the control strategies for each mode. In Section 3, the simulation results are presented and discussed. Finally, the conclusions are presented in Section 4.

2. Modeling and Simulation of the Proposed Method

2.1. Design of the ASCC operating modes

Fig. 2 shows the equivalent circuit of an ASCC, which is employed in a typical three-phase circuit [1]. The equivalent circuit of the air-core superconducting transformer with the controllable output current source of the ASCC converter is shown in Fig. 3.

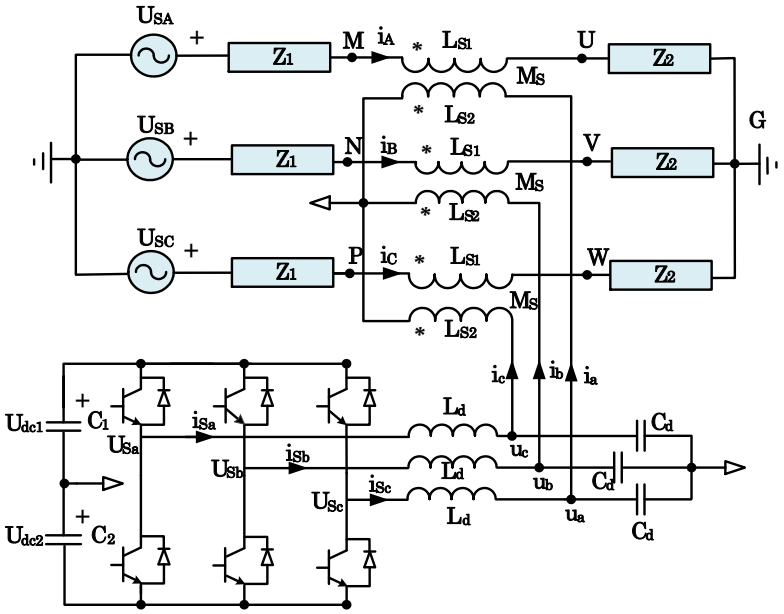


Fig. 2 Structure of a typical three-phase circuit with ASCC [10]

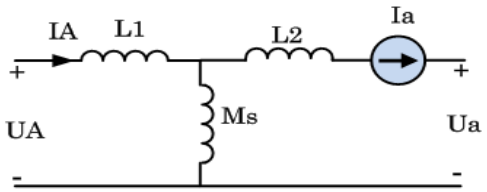


Fig. 3 The equivalent circuit of the air-core superconducting transformer [11]

By neglecting the losses of the air-core superconducting transformer, the primary voltage of the transformer (in phase A) can be expressed as follows:

$$\hat{U}_A = j\omega L_{S1}\hat{I}_A - j\omega M_S\hat{I}_a \tag{1}$$

$$\hat{U}_a = j\omega L_{S2}\hat{I}_a - j\omega M_S\hat{I}_A \tag{2}$$

$$L_{S1} = L_1 + M_S \tag{3}$$

where L_1 is the self-inductance of the primary winding of the superconducting transformer and M_S is the mutual inductance between the primary and secondary windings. Also $\hat{I}_A$ and $\hat{I}_a$ are the current phasors at the primary and secondary windings of the transformer, respectively. The value of $\hat{U}_A$ is controlled depending on the ASCC operating mode. The ASCC operating modes are defined as follow:

(A) *Normal operating mode*

In the normal condition, the converter is controlled such that the ASCC does not affect the main circuit. Therefore, $\hat{I}_a$ should be adjusted as:

$$\hat{I}_a = \frac{L_{S1}}{M_S}\hat{I}_A = \frac{L_{S1}}{M_S}\left(\frac{\hat{U}_{SA}}{Z_1 + Z_2}\right) \tag{4}$$

(B) *Fault operating mode*

When a short circuit fault occurs in the network, e.g. a three-phase fault right after the ASCC which leads to the highest fault current, the line current will rise from $\hat{I}_A$ to $\hat{I}_{Af}$:

$$\hat{I}_{Af} = \frac{\hat{U}_{SA} - \hat{U}_{Af}}{Z_1} \tag{5}$$

where $\hat{U}_{Af}$ is the primary voltage of the superconducting transformer during the fault. By inserting $\hat{U}_{Af}$ in Eq. (5) we have:

$$\hat{I}_{Af} = \frac{\hat{U}_{SA} + j\omega M_S \hat{I}_a}{Z_1 + j\omega L_{S1}} \tag{6}$$

The limiting impedance of ASCC (Z_{ASCC}) is defined as:

$$Z_{ASCC} \triangleq \frac{\hat{U}_{Af}}{\hat{I}_{Af}} \tag{7}$$

By inserting $\hat{U}_{Af}$ and $\hat{I}_{Af}$ in Eq. (7), Z_{ASCC} can be calculated as:

$$Z_{ASCC} = j\omega L_{S1} - \frac{j\omega M_S \hat{I}_a (Z_1 + j\omega L_{S1})}{\hat{U}_{SA} + j\omega M_S \hat{I}_a} \tag{8}$$

According to above equations, by adjusting the secondary winding current ($\hat{I}_a$), the fault current can be controlled at different levels. Two different states are defined regard as follows:

State 1

This state is activated in the first cycles of the fault and before the fault detection and converter operation time. In this state $\hat{I}_a$ is kept equal to its pre-fault value. The fault current in this state (I_{Af-1}) can be achieved as:

$$\hat{I}_{Af-1} = \frac{\hat{U}_{SA} + j\omega L_{S1} \hat{I}_A}{Z_1 + j\omega L_{S1}} \tag{9}$$

where $\hat{I}_A$ is the pre-fault primary current of the superconducting transformer.

State 2

This state is activated after the fault detection and converter operation time. In this state, the phase angle of I_a is regulated such that to make the angle difference between $\hat{U}_{SA}$ and $j\omega M_S \hat{I}_a$ becomes 180^0, so the amplitude of the fault current in this state $(\hat{I}_{Af-2})$ can be achieved as:

$$\left|\hat{I}_{Af-2}\right| = \frac{\left|\hat{U}_{SA} + \omega M_S \hat{I}_a\right|}{\left|Z_1 + j\omega L_{S1}\right|} \tag{10}$$

According to Eqs. (9)-(10), it is clear that $I_{Af-2} < I_{Af-1}$. Therefore the fault current limiting is done at a higher level in State 2.

(C) *Voltage compensating mode*

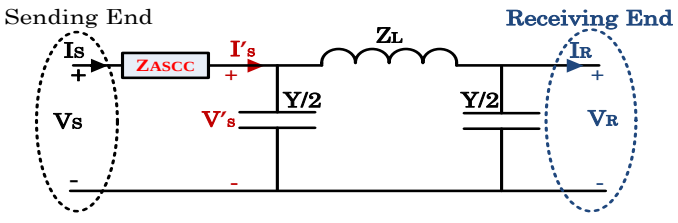


Fig. 4 Equivalent circuit of transmission line with ASCC in sending end of the line

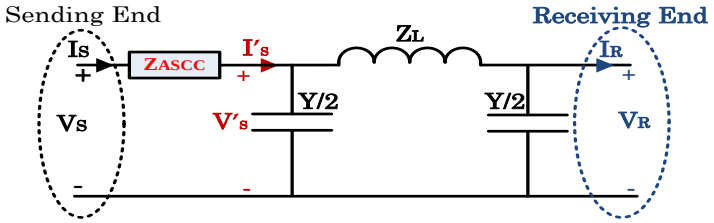


Fig. 5 Equivalent circuit of transmission line with ASCC in the middle of the line

To describe the voltage compensating mode of ASCC, it is assumed that the ASCC is used at the sending end or middle of the transmission line as shown in Figs. (4)-(5).

The system transmission matrix without and with ASCC at the sending end and middle of the line are obtained according to Eqs. (11)-(15) respectively.

$$\begin{bmatrix}\hat{V}_S\\ I_s\end{bmatrix}=\begin{bmatrix}1+\frac{YZ_L}{2} & Z_L\\ Y(1+\frac{YZ_L}{4}) & 1+\frac{YZ_L}{2}\end{bmatrix}*\begin{bmatrix}\hat{V}_R\\ I_R\end{bmatrix} \tag{11}$$

$$\begin{bmatrix}\hat{V}_S\\ I_s\end{bmatrix}=\begin{bmatrix}(1+\frac{YZ_L}{2}+YZ_{ASCC}(1+\frac{YZ_L}{4}) & Z_L+Z_{ASCC}(1+\frac{YZ_L}{2})\\ Y(1+\frac{YZ_L}{4}) & 1+\frac{YZ_L}{2}\end{bmatrix}*\begin{bmatrix}\hat{V}_R\\ I_R\end{bmatrix} \tag{12}$$

$$\begin{bmatrix}\hat{V}_S\\ I_s\end{bmatrix}=\begin{bmatrix}1 & \frac{Z_L}{2}+Z_{ASCC}\\ \frac{Y}{2} & 1+\frac{Y(\frac{Z_L}{2}+Z_{ASCC})}{2}\end{bmatrix}*\begin{bmatrix}\hat{V}_m\\ I_m\end{bmatrix} \tag{13}$$

$$Y=y*L \tag{14}$$

$$Z_L=z*L \tag{15}$$

where L is the length of the line and z and y are the impedance and admittance values per unit length of the line respectively. To investigate the over-voltage compensating of ASCC the no-load condition of the line is considered. By inserting $I_R=0$, the sending end voltage of the line is obtained as:

$$\hat{V}_S=\left[\left(1+\frac{YZ_L}{2}\right)+YZ_{ASCC}\left(1+\frac{YZ_L}{2}\right)\right]*\hat{V}_R \tag{16}$$

To control the receiving end voltage of the line at no-load condition, the value of Z_{ASCC} is determined such that the magnitudes of the receiving end and the sending end voltages become equal. Therefore, by inserting $\hat{V}_S=\hat{V}_R$ in Eq. (16), the proper impedance is calculated as:

$$Z_{ASCC}=\frac{-\frac{Z_L}{2}}{1+\frac{YZ_L}{4}} \tag{17}$$

On the other hand, to investigate the low-voltage compensating of ASCC, the full-load condition of the line is considered. In this case, equivalent load impedance Z_{load} is modeled at the end of the line. The system voltage equations when ASCC is inserted at the sending end and middle of the line are given as follow:

$$\hat{V}_S = \left[\left(1+\frac{YZ_L}{2}\right) + YZ_{ASCC}\left(1+\frac{YZ_L}{4}\right) + \frac{Y_L + Z_{ASCC}\left(1+\frac{YZ_L}{2}\right)}{Z_{load}} \right] * \hat{V}_R \tag{18}$$

$$\hat{V}_S = \hat{V}_m + \left(\frac{Z_L}{2} + Z_{ASCC}\right) * \hat{I}_m \tag{19}$$

By inserting $\hat{V}_S = \hat{V}_R$ in to Eq. (18) and $\hat{V}_S = \hat{V}_m$ in Eq. (19), the proper impedance of ASCC for voltage compensating at the receiving end and middle of the line are calculated as Eqs. (20)-(21) respectively.

$$Z_{ASCC} = \frac{-Z_L\left(\frac{Y}{2}+\frac{1}{Z_{load}}\right)}{Y + \left(1+\frac{YZ_L}{4}\right) + \frac{1}{Z_{load}}\left(1+\frac{YZ_L}{2}\right)} \tag{20}$$

$$Z_{ASCC} = \frac{-Z_L}{2} \tag{21}$$

According to Eqs. (20)-(21), the proper setting of ASSC can compensate for the reduced voltage under loading conditions. In this state, by measuring the receiving end voltage and current, the load impedance is determined and the value of the ASCC impedance is calculated. Finally, the proper setting of the ASCC converter is obtained for this case.

2.2. Control strategy for ASCC converter

In this section, a double-loop control strategy is briefly described, and the reader is referred to [12] for more details. According to Fig. 2 and assuming that the switching devices are ideal and the split DC link capacitances are the same $(C_1 = C_2)$, the current and voltage equations can be achieved as:

$$\begin{cases} L_d \dfrac{di_{sa}}{dt} = u_{sa} - i_a \\ C_d \dfrac{du_{sb}}{dt} = u_{sb} - i_b \\ C_d \dfrac{du_{sc}}{dt} = u_{sc} - i_c \end{cases} \tag{22}$$

$$\begin{cases} C_d \dfrac{du_a}{dt} = i_{sa} - i_a \\ C_d \dfrac{du_b}{dt} = i_{sb} - i_b \\ C_d \dfrac{du_c}{dt} = i_{sc} - i_c \end{cases} \tag{23}$$

Further, the mathematical equations in dq0 reference frame can be obtained by:

$$\begin{cases} L_d \dfrac{di_{sd}}{dt} = \omega L_d i_{sq} + u_{sd} - u_d \\ L_d \dfrac{di_{sq}}{dt} = -\omega L_d i_{sd} + u_{sq} - u_q \\ L_d \dfrac{di_{s0}}{dt} = u_{s0} - u_0 \end{cases} \tag{24}$$

$$\begin{cases} C_d \dfrac{du_d}{dt} = \omega C_d u_q + i_{sd} - i_d \\ C_d \dfrac{du_q}{dt} = -\omega C_d u_d + i_{sq} - i_q \\ C_d \dfrac{du_0}{dt} = i_{s0} - i_0 \end{cases} \tag{25}$$

The DC link voltage equation can be achieved by:

$$u_{dc1} + u_{dc2} = u_{dc} \tag{26}$$

$$C_2 \frac{du_{dc2}}{dt} - C_1 \frac{du_{dc1}}{dt} = 3\left(i_0 + C_d \frac{du_0}{dt} \right) \tag{27}$$

Based on Eqs. (22)-(27), the control system diagram of the three-phase PWM converter is shown in Fig. 6. According to the operating state of the main circuit and the current-limiting state of the ASCC, the current reference signals $(I_{abc-ref})$ can be known. Further, the reference signals $(U_{abc-ref})$ will be obtained, and then the voltage reference signals of the converter $(U_{dq0-ref})$ can be achieved by the ABC to dq0 conversion matrix according to Eq. (28).

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \omega t & \sin \omega t & 0 \\ -\sin \omega t & \cos \omega t & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{28}$$

When an asymmetrical fault occurs, the 0 axes current reference i_{s0} will be generated by the difference between the controllers of U_{dc2} and U_{dc1}. Since $U_{dc} = U_{dc1} + U_{dc2}$ will be controlled to stay the same, the variation trends of U_{dc2} and U_{dc1} will be opposite with each other, to keep the voltage balance of the split DC link capacitors.

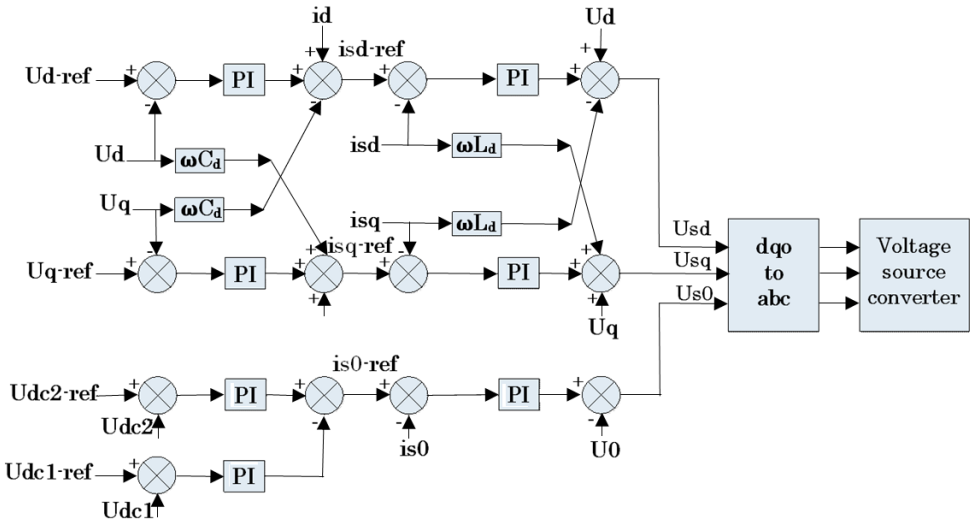


Fig. 6 Control strategy for a three-phase PWM converter [12]

2.3. Flowchart of the proposed method

Fig. 7 shows the flowchart of the proposed method. By comparing the system and reference current in the dq0 reference frame according to Eq. (29) Δi is calculated and when Δi exceeds the threshold value, the fault is detected.

$$\Delta i = \sqrt{\left(i_d - i_{d-ref} \right)^2 + \left(i_q - i_{q-ref} \right)^2} \tag{29}$$

The values of $\Delta i_{threshold}$ and $i_{a,b,c-ref}$ are calculated considering an overload factor for the system currents concerning the nominal currents, e.g. 50%.

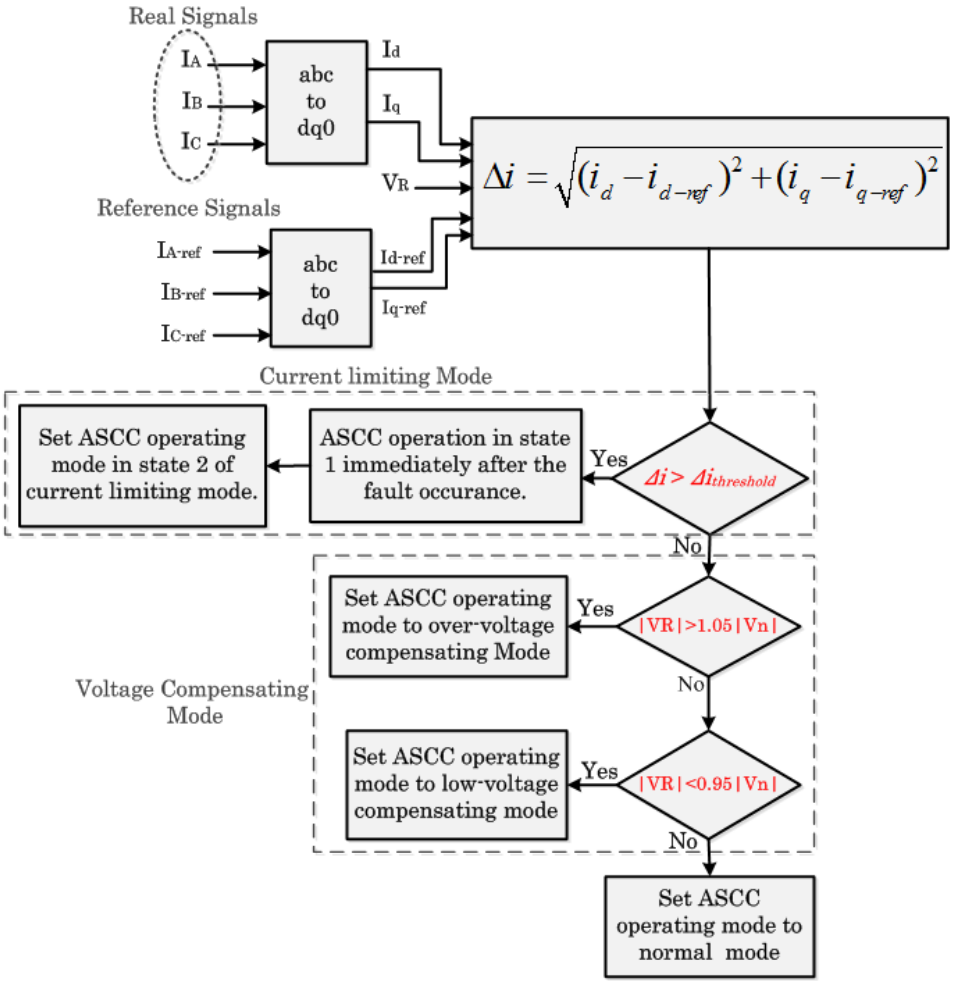


Fig. 7 Flowchart of the proposed method

If the fault state is not detected, the no-load and full-load state of the line is detected by measuring the receiving end voltage of the line and ASCC is adjusted to the proper voltage compensating mode.

2.4 Feasibility of implementation

One of the main issues in the development of the ASCC will be the cost. The power electronic converters as well as the superconducting transformers used in the ASCC, especially at high voltage levels, can result in the high cost of using this equipment. On the other hand, the high costs caused by replacing the existing circuit breakers with higher power types as well as the use of the separate voltage compensator equipment can reduce when ASCC is applied in the power system. Coordination of protective relays and proper placement of ASCC are other issues that should be considered when ASCC is used in power systems. In this paper, the feasibility of implementing the proposed method is investigated by simulating a 500 kV sample transmission line with ASCC. The simulation of ASCC in the KEPCO distribution system by considering the current limiting and OCRs coordination is carried out in our other work in [13-14]. Also, a laboratory prototype of 800V/30A active superconducting current controller is tested in [11].

3. Simulation Results

In this section, simulation results for evaluating the performance of the ASCC in different modes, including the fault current limiting mode and the voltage compensation mode are presented.

3.1. Testing the current limiting mode

At first, to assess the performance of three aforementioned states of the current limiting mode, the model shown in Fig. 2 with the parameters in Table 1 is simulated in MATLAB.

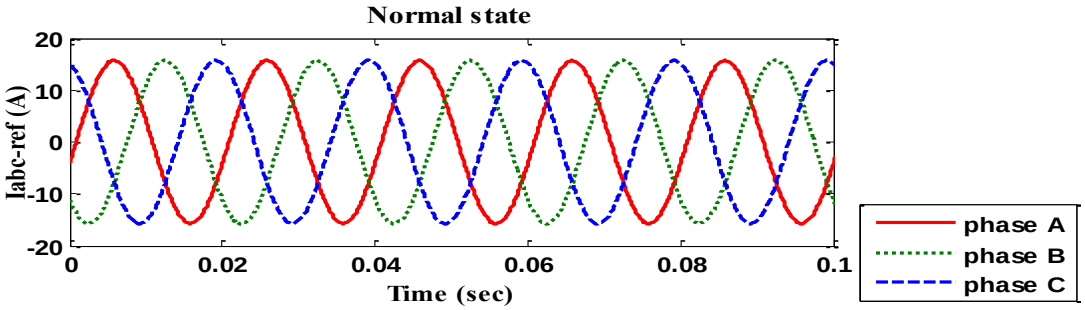
Table 1 Parameters of ASCC and simulated system [1]

Parameter	Value
Tape	Bi2223/Ag(0.3mmt*4.3mmw)
Inner diameter	88mm
Outer diameter	154mm
Turns of the double pancake	265
The Self-inductance and mutual- inductance of the primary and secondary windings	[10, 9] (mH)
Source voltage and DC link voltage	USA=220(V), Udc=600(V)
Source and load impedances	Z1=0.19 + 2.16 i (Ω), Z2=15 + 2 i (Ω)
Filtering capacitor and inductance	Ld=6(mH), Cd=30 (μF)
DC link capacitors	C1=C2=2000 (μF)

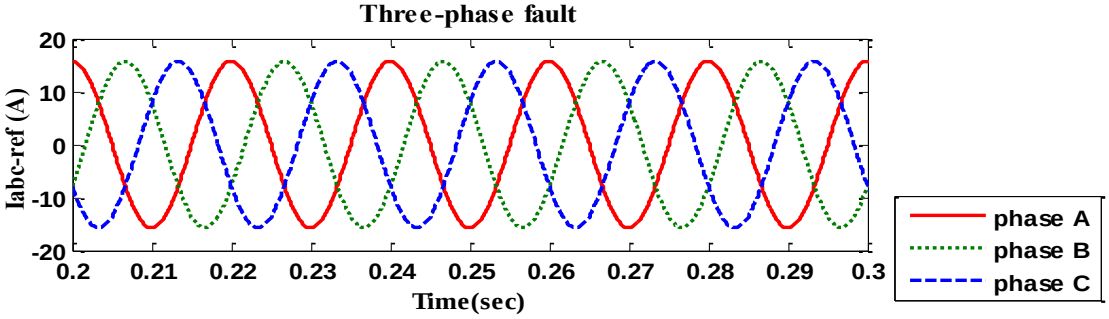
Table 2 and Fig. 8 show the voltage and current reference signals of the converter for the normal state, a three-phase and a single-phase fault at the load location in Fig. 2. These signals are used as inputs of the control strategy shown in Fig. 6. As illustrated in Fig. 8 following the occurrence of the single-phase fault, the AC components of U_{dc1} and U_{dc2} are opposite to each other, and the total DC voltage is kept constant at the level of 600 V.

Table 2 Control parameters for the cases of normal operation, three-phase fault and single-phase fault [16]

Single-Phase Fault	Three-Phase Fault	Normal state	Reference signals
15.7sin(ωt+90)	15.7sin(ωt+90)	15.7sin(ωt-15.3)	$I_{a\text{-}ref}$ (A)
15.7sin(ωt-135.3)	15.7sin(ωt-30)	15.7sin(ωt-135.3)	$I_{b\text{-}ref}$ (A)
15.7sin(ωt+104.7)	15.7sin(ωt-150)	15.7sin(ωt+104.7)	$I_{c\text{-}ref}$ (A)
4.7	3.1	-8.6	$U_{d\text{-}ref}$ (V)
-45.4	-142.4	3.1	$U_{q\text{-}ref}$ (V)
48.7sin(ωt+4.6)	0	0	$U_{0\text{-}ref}$ (V)
300+20sin(ωt-143)	300	300	$U_{dc2\text{-}ref}$ (V)
K_P=0.03, K_I=1.5, f=60, ω=2πf, L_d=6e-3, C_d=30e-6			

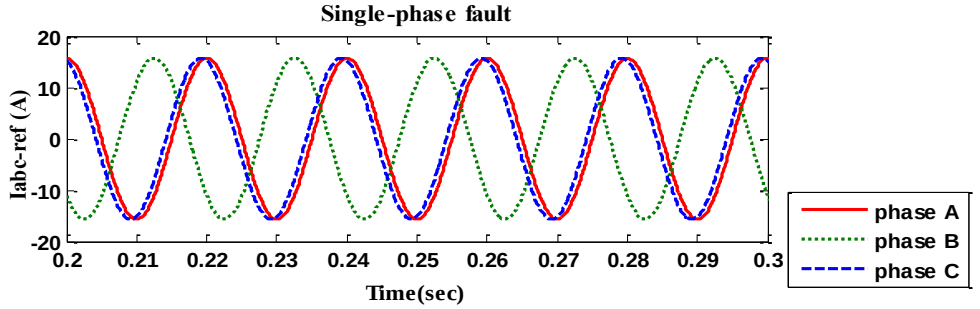


(a) The reference currents for normal state

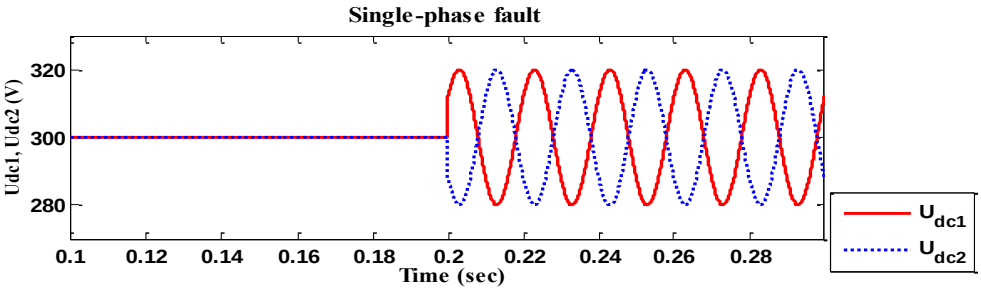


(b) The reference currents for three phase fault state

Fig. 8 Reference parameters for the cases of normal operation, three-phase fault and single-phase fault



(c) The reference currents for single phase fault state



(d) DC link voltages for single phase fault state

Fig. 8 Reference parameters for the cases of normal operation, three-phase fault and single-phase fault (continued)

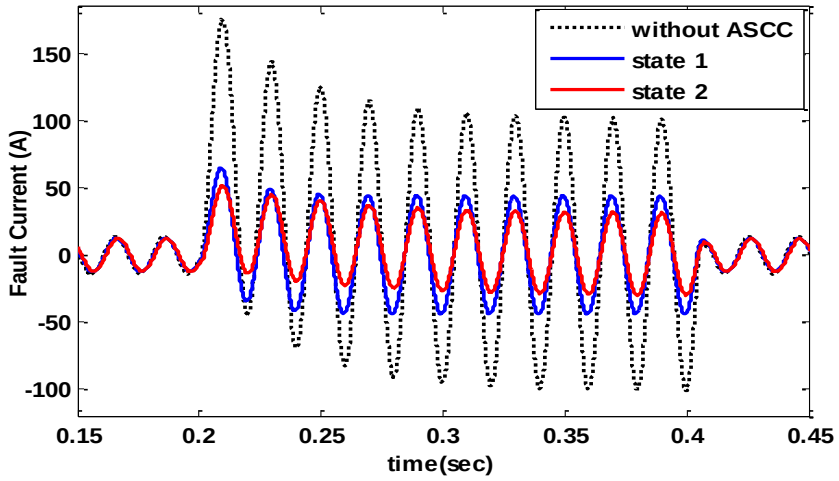


Fig. 9 Comparison of the fault current levels for different operating state

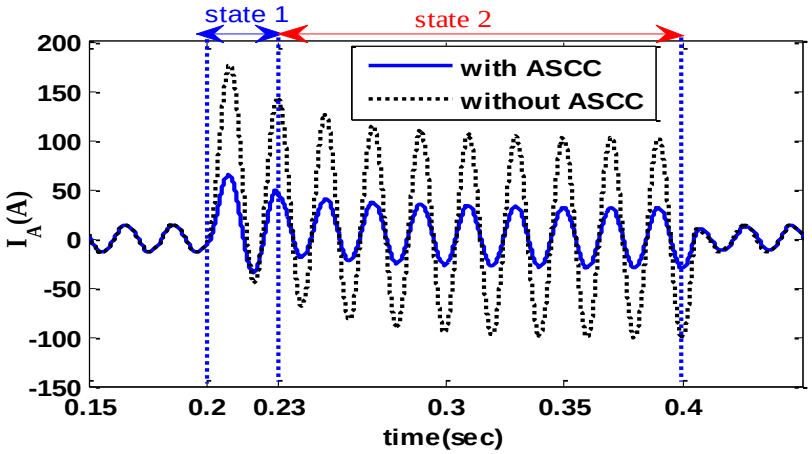


Fig. 10 Fault current without and with ASCC operation in current limiting mode

A comparison of the fault current levels without ASCC and with ASCC in different states of current limiting mode is shown in Fig. 9. As can be observed in Fig. 9, state 2 which is based on the phase angle regulation has the best performance in fault current suppression. Fig. 10 shows the amplitude of the fault current when ASCC operates in current limiting mode.

Interval t = 0.2 (Sec) to t = 0.23 (Sec) is the time which is considered to detect the fault for the operation of the converter and the line current is reduced to 44.38 (A) since the ASCC operates in state 1. Similarly, from t = 0.23 (Sec) to t = 0.4 (Sec), by setting the phase angle of compensating current (I_a) to 90 °, defined as state 2, the fault current is reduced to 30.76 (A).

Fig. 11 shows the magnitude and angle of the compensating current $\hat{I}_a$ during fault current limiting. The best limiting performance is obtained for the phase angle of 90° for $\hat{I}_a$. Besides, increasing the magnitude of compensating current or voltage improves the effect of fault current limiting.

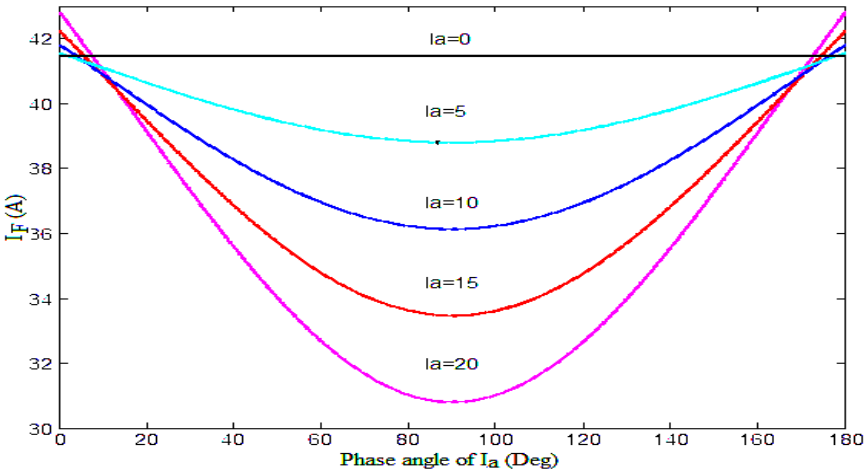


Fig. 11 IA-peak vs. the Ia phase angle characteristic

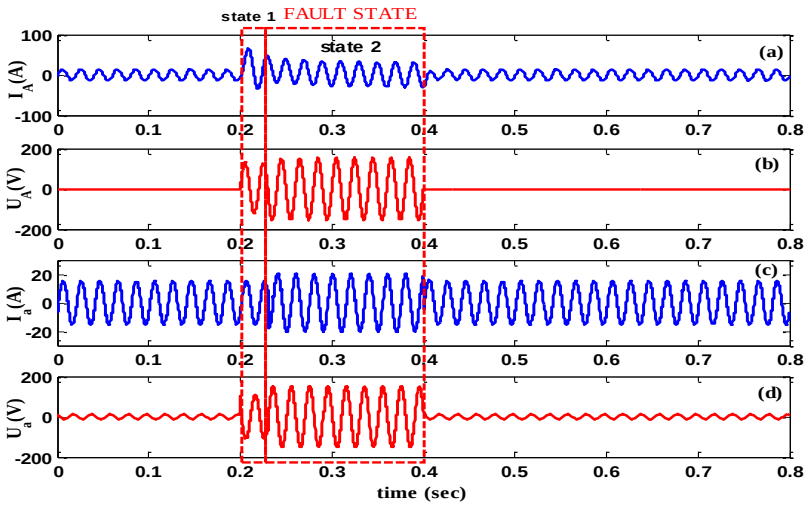


Fig. 12 ASCC response for current limiting mode

The voltages and currents of the primary and secondary winding of the superconducting transformer in the fault current limiting mode are shown in Fig. 12. As can be observed in Fig. 12, in the normal operating mode, by proper setting of ASSC converter, the primary series voltage is compensated to zero and thus ASCC does not affect the main circuit in this mode. Immediately after the fault occurrence, in the first state of current limiting mode, the output voltage of the ASCC converter is increased and the fault current is reduced. After that (in t=0.23s), the ASSC setting of the second state of the current limiting mode increases the output voltage of the converter and decreases the fault current at the higher level.

Since the power electronic devices have been used in the ASCC structure, this equipment will generate some harmonics in the power system. However, according to Fig. 12(d) it can be seen that, in the normal operation mode, the output voltage of the converter is set to a small amount to compensate the effect of ASCC in the main circuit. Therefore the effect of harmonics generated with the ASCC converter can be negligible. Also the filtering capacitors and inductors used in the ASCC structure (L_d and C_d in Fig. 2) can reduce the effect of these generated harmonics.

3.2. Testing the voltage compensating mode

To evaluate the performance of the voltage compensation mode of ASCC in the proposed method, a three-phase transmission line and ASCC with the parameters listed in Table 3 is simulated.

Table 3 The line and ASCC parameters for the voltage compensating test [13]

Line parameters		ASCC parameters	
Nominal Voltage	Vn=500kV	Nominal Voltage	Vn=500kV
Nominal Frequency	f=60Hz	Nominal Frequency	f=60Hz
Length of the line	L=300km	Rated power	S=100MV.A
Line resistance	r =0.016Ω/km	DC link nominal voltage	Vdc=40000V
Line inductance	l=0.97 mH/km	DC link total equivalent capacitance	C= 375μF
Line capacitance	C=0.0115μF/km	Self and mutual inductances	Ls_1=100mH Ms=90mH

3.2.1 Over-voltage compensation

To investigate the effect of ASCC on over-voltage compensating, a typical transmission line with the parameters in Table 3 is considered at no- load condition. Fig. 13 shows the receiving end voltage of phase A without compensation and with compensation in the presence of ASCC. As can be seen in Fig. 13 and referring to Eq. (17), the proper setting of ACCC can compensate for the over-voltage created in the no-load condition at the receiving end of the line.

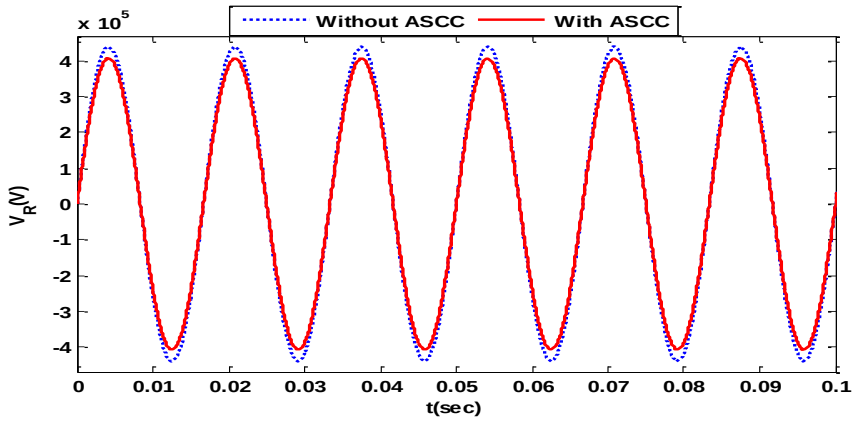


Fig. 13 Receiving end voltage in no-load condition without and with ASCC

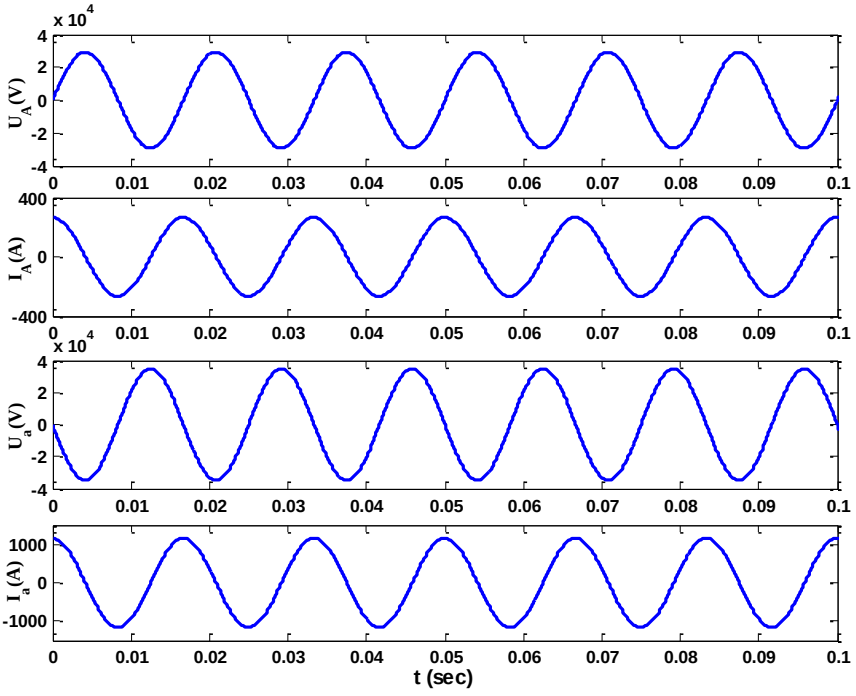


Fig. 14 ASCC response for the no-load condition of the line

The setting parameters of ASCC in this case including the primary and secondary current and voltage are shown in Fig. 14. According to Fig. 14, it is observed that the ASCC setting in this state generates a series lagging voltage with the network and thus creates negative impedance according to Eq. (17) for the voltage compensating at the no-loaded condition. Fig. 15 shows the voltage profile diagram along the transmission line at no-load condition.

It can be observed in Fig. 15 that in the no-load state using ASCC, the line voltage profile is improved and the increased voltage at the receiving end of the line is compensated and reaches its value on the sending end side.

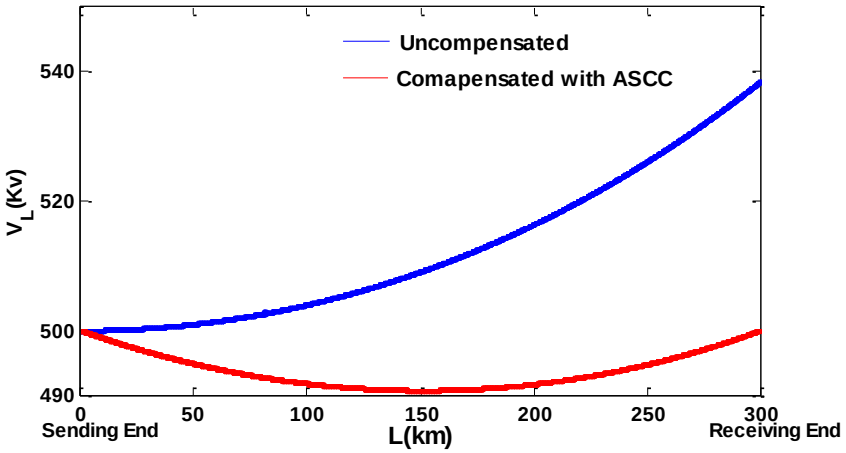


Fig. 15 Voltage profile with and without ASCC for the no-load condition of the line

3.2.2. Low-voltage state

In this case, it is assumed that the three phase load with the parameters listed in Table 4 is connected to the receiving end of the line.

Table 4 Load parameters for the full-load compensating mode [13]

Load Parameters		
V=500kV	P=800MW	PF=0.8Lag

Fig. 16 shows the receiving end voltage of the line at full-load condition. As can be observed, in the full-load condition of the line, the receiving end voltage is lower than its acceptable range, thus the voltage compensating mode of ASCC is activated. As can be seen, by ASCC proper setting, the dropped voltage at the receiving end is compensated and reaches its value on the sending end side.

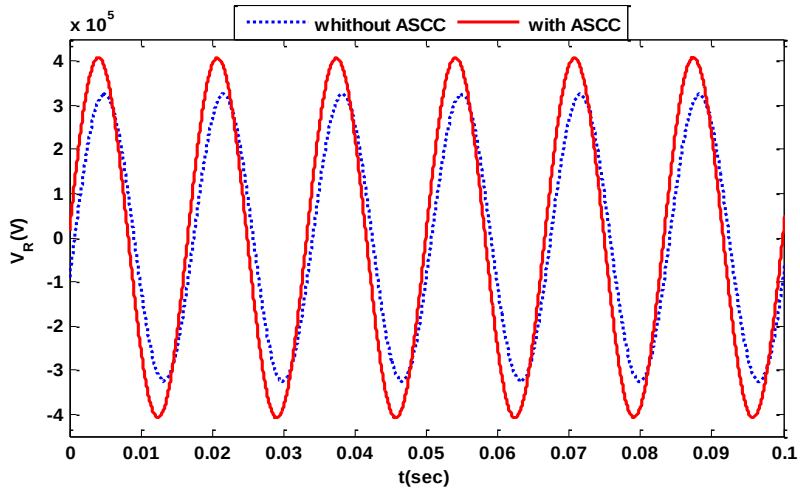


Fig. 16 The receiving end voltage at full-load condition without and with ASCC

The setting parameters of ASCC for two states of compensation, including the receiving end voltage compensation and the middle voltage compensation in the full-load condition are shown in Fig. 17.

According to Fig. 17, it can be seen that the voltage compensation in the middle of the line requires less voltage injection from the ASCC converter and so the power of the ASCC converter is reduced significantly. To compare the voltage compensation in these two states, the voltage profiles of the line in different condition including without compensation, the receiving end voltage compensation and the middle voltage compensation are shown in Fig. 18.

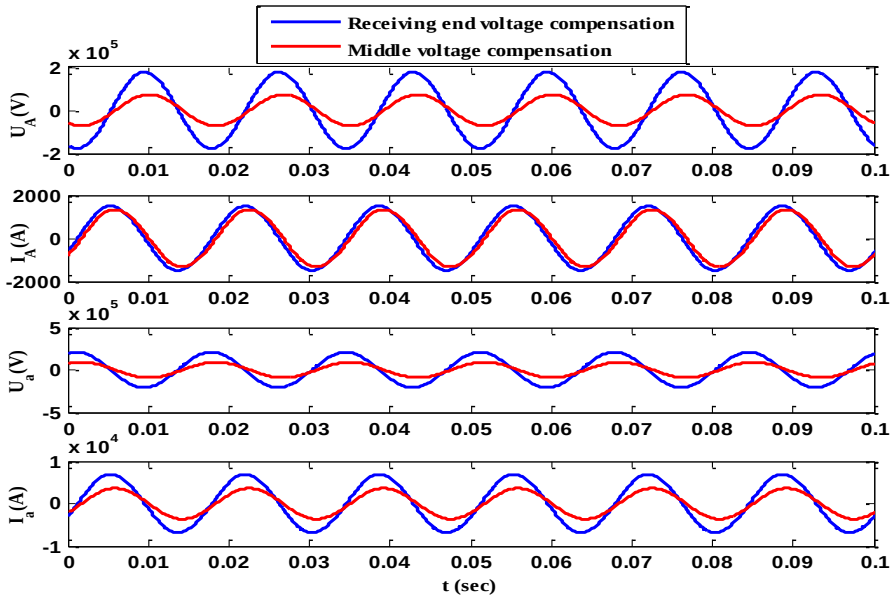
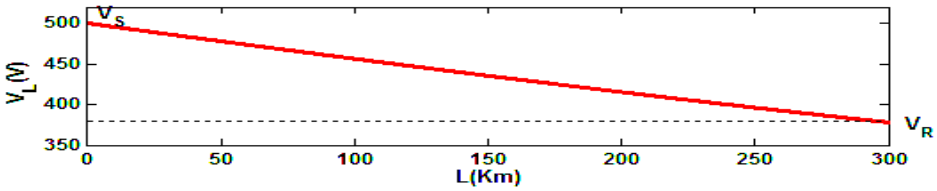
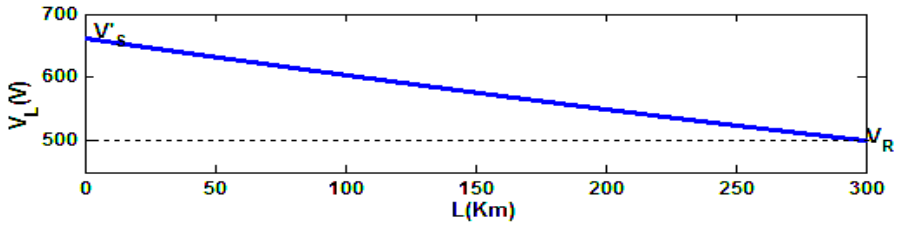


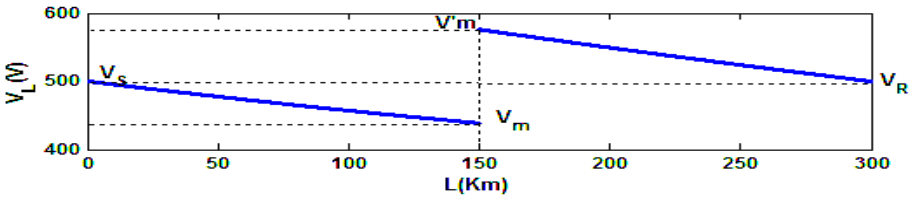
Fig. 17 ASCC response for the full-load condition of the line



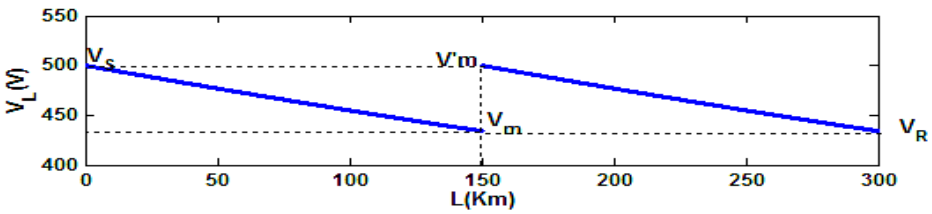
(a) Voltage profile of the line at full-load condition without ASCC



(b) Voltage profile of the line at full-load condition with ASCC in sending end of the line



(c) Voltage profile of the line with ASCC in middle of the line by setting for receiving end voltage compensation



(d) Voltage profile of the line with ASCC in middle of the line by setting for middle end voltage compensation

Fig. 18 Voltage profile of the line at full-load condition

According to Fig. 18(a), in the non-compensating state, the magnitude of the voltage at the receiving end of the line is reduced by about 75% of the nominal voltage. By inserting the ASCC at the sending end of the line (Fig. 18(b)), although the voltage at the receiving end is compensated, the voltage increasing at the sending end, in this case, can have adverse effects on the equipment at the sending side. By placing the ASCC in the middle of the line, the voltage profile can be improved in two different cases. In the first case, according to Fig. 18(c) ASCC is adjusted to keep the receiving end voltage at its nominal value. Increasing the voltage in the middle of the line and increasing the ASCC converter power are some problems in this case. Finally, Fig. 18(d) shows the voltage profile of the line when the ASCC is inserted in the middle of the line and compensates for the voltage in the middle of the line. According to Fig. 18(d), it can be seen that in this case, the voltage at the receiving end will be reduced by about 50% of the non-compensating state and also there will be no increase in the voltage along the line. So, this case can perform the best operation in the full-load condition.

4. Conclusion

In this paper, a proposed method for the fault current limiting and voltage compensating using an active superconducting current controller is presented. In this method, different operating modes of ASCC including normal mode, short circuit fault mode, over-voltage, and low-voltage compensating mode were defined. The simulation results show that in the case of a short circuit fault, ASCC rapidly suppresses the fault current in the first cycles of the fault immediately after the fault occurrence by adjusting the amplitude and the phase angle of the compensation current. The results also confirmed that application of the ASCC with the proposed operating modes can improve the line voltage profile in over-voltage and low-voltage states without using the conventional shunt compensators. Therefore, according to the proposed method, the unique ability of the ASCC in the simultaneous operation of the fault current limitation and line voltage compensation was presented and shows the superiority of this equipment compared with other conventional type FCLs.

Symbols and Abbreviations

ASCC	Active Superconducting Current Controller
FCL	Fault Current Limiters
SFCL	Superconducting Fault Current Limiter
PWM	*Pulse Width Modulation*
OCR	Over-Current Relay
(L_1, L_2)	The primary and secondary self- inductance of superconducting transformer
M_S	The mutual-inductances of superconducting transformer
(C_1, C_2)	The split DC link capacitors
(L_d, C_d)	The inductance and capacitor for filtering the harmonics generated by the PWM converter
(U_A, U_a)	The primary and secondary voltages of superconducting transformer
(I_A, I_a)	The primary and secondary current of superconducting transformer
(Z_1, Z_2)	The line and load impedances
I_{AF}	The phase A fault current
$(I_{AF1}, I_{AF2}, I_{AF3})$	The fault current in the three operation modes ASCC
Z_{ASCC}	The limiting impedance of ASCC
Δi	The difference between actual and desirable currents
$\Delta i_{threshold}$	The threshold value for Δi
(i_{abc}, i_{dq0})	The three phase currents in the abc and dq0 reference frame
Z	The model of line Impedance
Y	The model of line capacitor admittance
(V_S, V_R)	The sending end and receiving end voltages of the line
(I_S, I_R)	The sending end and receiving end currents of the line

Conflicts of Interest

The authors declare that there is no conflict of interest.

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