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Invited Paper

Silicon-on-insulator technology by crystallization on quartz substrates

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Abstract

The purpose of the novel zone-melting recrystallization process (ZMR) is to produce single crystalline Si films on SiO_2 of high crystalline perfection, which are suitable for device fabrication and subsequent industrial applications. However, silicon films grown on amorphous insulating substrates without seeding contain regularly spaced subgrain boundaries as their predominant growth defect and to a lesser degree twin boundaries and some grain boundaries. Detailed materials studies have revealed the core structure of these extended defects and the fundamental mechanisms responsible for subgrain boundary formation. The nature and origin of subgrain boundaries is reviewed and a model for polygonization of the initial dislocation arrays is presented. In addition to subgrain boundary formation, silicon films on quartz are subject to microcracking due to thermal mismatch with the substrate. The influence of these residual growth defects and the inherent tensile stress on device performance is evaluated.

Introduction

The rapidly increasing activity in Silicon-on-Insulator (SOI) research we have witnessed during the last 5 years reflects the need for better technologies to achieve dielectric isolation of Si. Research in this field has been motivated by the potential advantages of isolated thin film devices over bulk single crystal Si devices. Thin Si films which are dielectrically isolated from the substrate can be used for high speed, radiation-hard integrated circuits. Latch-up in CMOS devices and parasitic capacitance can be reduced by dielectrically isolating individual devices from each other. Furthermore, SOI is one of the few technologies with good prospects for accomplishing 3-dimensional integration of electronic circuits. The potential for flat panel displays has stimulated a lot of work on recrystallization of Si films deposited on transparent substrates.

Historically, Silicon-on-Sapphire (SOS) was the first among several technologies, which were developed to utilize these attractive features. One of the driving forces is to improve radiation hardness which requires decreasing the Si film thickness in order to minimize the semiconductor volume for electron-hole pair generation by ionizing radiation. SOS, however, suffers from a very high density of misfit defects. Since the defect density increases towards the silicon/sapphire interface, there is a limit to Si film thickness reduction. These inherent defect problems plus the high cost of sapphire substrates have led to renewed interest in the development of alternative novel Silicon-on-Insulator technologies. Most of the new SOI technologies use SiO_2 as the insulating layer and deposited polycrystalline Si films on top of it. Their relative advantages are discussed in two recent conference proceedings on SOI and thin film transistor technologies.[1,2] One of the more successful approaches has been the technique of zone-melting recrystallization (ZMR). Zone-melting recrystallization is accomplished by the passage of a molten zone through the Si film. This novel crystal growth technique has proved very effective in producing large areas of single crystal Si films on amorphous insulating substrates like fused silica or SiO_2 coated Si wafers. Although the SOI films obtained by zone-melt recrystallization are single crystalline over large areas, they are not free from lattice imperfections, and contain characteristic residual growth defects in the form of subgrain boundaries. There is a strong incentive to reduce and control electrically active defects and to increase the uniformity of the material. A key element for a deeper understanding of the basic lateral melt growth process in thin Si films on insulators is detailed information about the nucleation process of subgrain boundaries in addition to knowledge about the kinetics of the growth interface. In this paper unseeded growth of thin Si films on amorphous quartz substrates by laser induced zone-melting recrystallization is discussed. The resulting crystal quality of the SOI films and the growth defect formation mechanism and their influence on thin film device performance are reviewed.

Experimental procedure

Realization of the zone-melting principle requires radiative heating and melting of a narrow zone of the deposited Si film. Zone-melting recrystallization has been demonstrated with a variety of techniques since polycrystalline Si films are readily melted with an intense photon flux. Graphite strip heaters,[3,4,5] electron beams,[6,7] focussed halogen

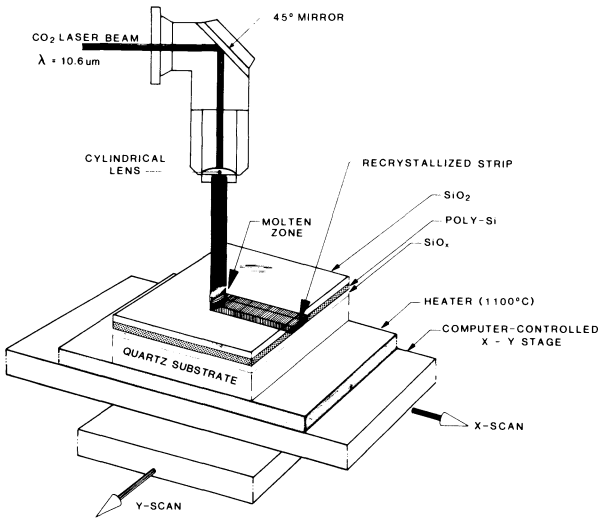
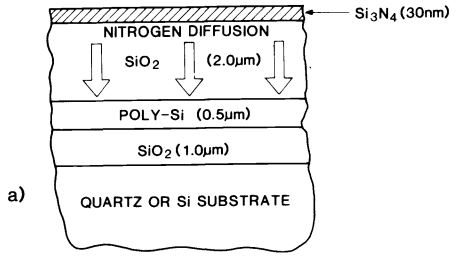


Figure 1. Schematic showing the experimental set-up for laser induced zone-melting recrystallization of thin Si films on quartz. In the laboratory the graphite substrate heater and the SOI sample are enclosed by a water cooled stainless steel recrystallization chamber.

lamps[8,9] and lasers[10] have been successfully used for recrystallization purposes. The thin film crystal growth work reported here was performed by Argon ion laser or CO_2 laser induced zone-melting. A schematic configuration of our experimental recrystallization system is shown in Figure 1. In this arrangement the laser beam was focussed with a cylindrical lens into a strip which formed a several mm long molten zone in the Si film. The SOI wafer was first heated to a background temperature of 1100°C by a bottom graphite strip heater which uses resistive heating by ac currents. Then the additional radiative heating from the laser beam elevates the temperature to the melting point of Si in the line focus area of the beam. The molten zone is scanned across the sample by moving the recrystallization chamber with the wafer under a stationary laser beam. The lower graphite strip heater and the SOI wafer are enclosed by a water cooled stainless steel recrystallization chamber which is evacuated during the experiments and can be backfilled with inert gases such as Ar. A typical sample consists of a 4" wafer of fused silica or a bulk Si wafer. The Si wafers were prepared by thermally oxidizing them to grow a 1.0 μm SiO_2 layer. The polycrystalline Si films were then deposited by low pressure chemical vapor deposition (LPCVD) from SiH_4 at 625°C to a thickness of 0.5 μm. Because of non-wetting problems of molten Si with SiO_2 the encapsulation layer usually consists of SiO_2 and Si_3N_4 composites. Molten Si has only a marginal wetting angle of 87° with SiO_2 while the wetting angle with Si_3N_4 is drastically improved to 25°.[11] In case the molten Si film is only sandwiched between SiO_2 encapsulating layers some degree of dewetting always occurs. This process is accompanied by agglomeration of the Si film into numerous little droplets and break-up of the capping structure. Utilization of the superior wetting characteristics of Si_3N_4 can prevent this. In Figure 2a a widely used configuration for a composite encapsulation layer is shown. Here a thin Si_3N_4 is deposited on top of the capping SiO_2 of a typical SOI sample. This capping structure relies on the fact, that



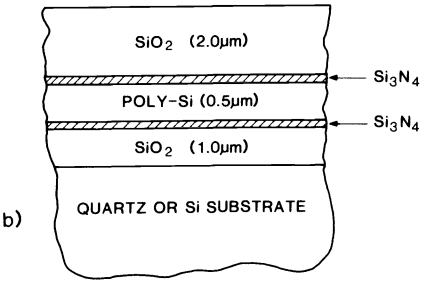


Figure 2. Schematic cross section showing the various layers of a silicon-on-insulator sample. (a) Encapsulation layer with a Si_3N_4 film on top relying on nitrogen diffusion.

(b) Alternative encapsulation, where the Si film is sandwiched between two CVD deposited Si_3N_4 layers.

nitrogen from the top can diffuse through the SiO_2 cap to the upper SiO_2-Si interface, where it lowers the wetting angle.[12] The other approach shown in Figure 2b does not rely on nitrogen diffusion. Here instead the Si_3N_4 layers are directly deposited at the interfaces of the Si film.[13] Since a lower Si_3N_4-Si interface is often undesirable for device applications[14] several variations of these basic approaches are in use. Besides promoting better wetting the Si_3N_4 films add mechanical strength to the encapsulation structure and help maintain a good surface morphology.

Materials properties

Surface morphology

Zone-melt recrystallization like the other novel thin film crystal growth techniques such as ribbon growth for solar cells produces single crystalline Si films with some imperfections in the form of residual growth defects. Even without any seeding, laser induced zone-melting results in well oriented thin film growth and the formation of (100) texture. For the in-plane orientation of the growth front the <100> direction is also preferred. The reason is that occlusion, as a result of natural growth velocity competition among different crystallographic directions, is responsible for this preferred growth orientation.[15] On the other hand the reason for the (100) surface texture in the solidified Si films on SiO_2 is less well understood. It is known that the interfacial energy between Si and SiO_2 is lowest for the (100) planes. Thus growth of (100) oriented Si films is energetically most favorable. But there are additional mechanisms at work. The coexistence of solid Si islands and ribbons in liquid Si heated by laser radiation has been established experimentally.[16] Subsequent theoretical work has predicted that (100) oriented grains in the transition region are preferentially retained in the melt due to a slightly higher melting temperature.[17] These retained crystallites can then act as oriented seeds during solidification. From an application's point of view this represents the ideal surface texture, since the (100) interface has the lowest densities of fixed oxide charge and interface electronic states.

Subgrain boundary generation

During crystal growth when the molten zone is scanned across the sample, polycrystalline Si is melted at the leading edge of the molten zone and solidified at the trailing edge. Profound microstructural changes accompany this recrystallization of the originally fine grain polycrystalline Si film. In order to characterize the crystalline quality of the Si film following the zone-melting recrystallization process, the composite encapsulation was stripped off by etching. The exposed surface of the Si film was treated with Schimmel defect etch to reveal any imperfections that occurred during the growth process. The optical micrograph of Figure 3 shows a typical surface morphology. Characteristic lineage structures with "fish-hook" like features are displayed, which are referred to as subgrain boundaries. Aside from occasional grain boundaries these subgrain boundaries form the only major residual growth defect in SOI films. The transmission electron microscope (TEM) permits lattice defects to be studied at high resolution, and the dark field TEM micrograph in Figure 4 reveals the core structure of a subgrain boundary. Essentially these boundaries are composed of long parallel arrays of dislocations, as illustrated in Figure

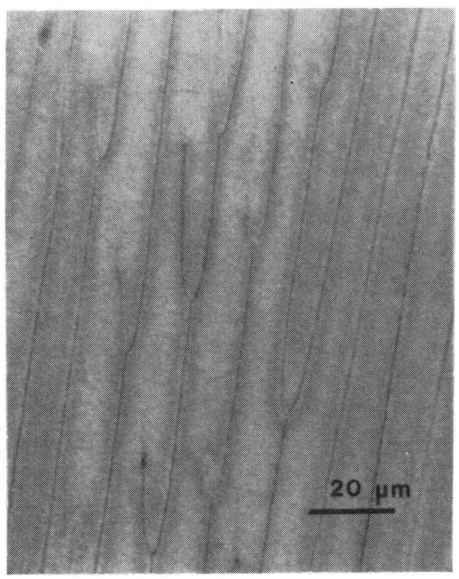


Figure 3. Optical micrograph of (100) textured recrystallized Si film with characteristic subgrain boundary structure.

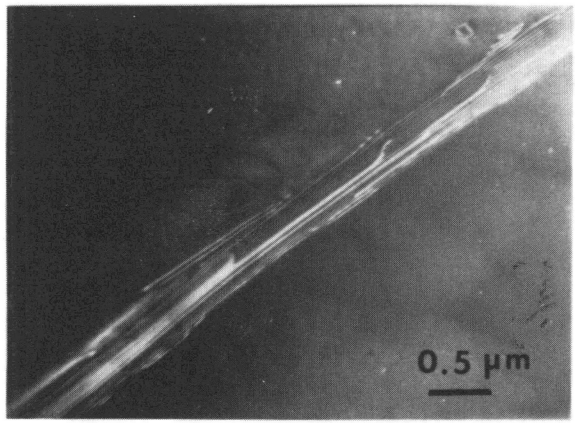


Figure 4. Dark field TEM micrograph of dislocation array forming a subgrain boundary.

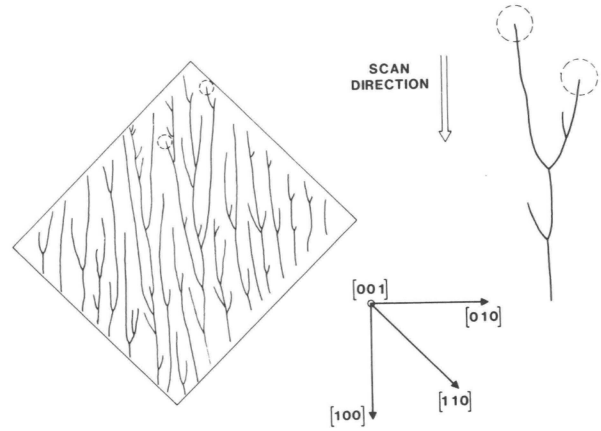
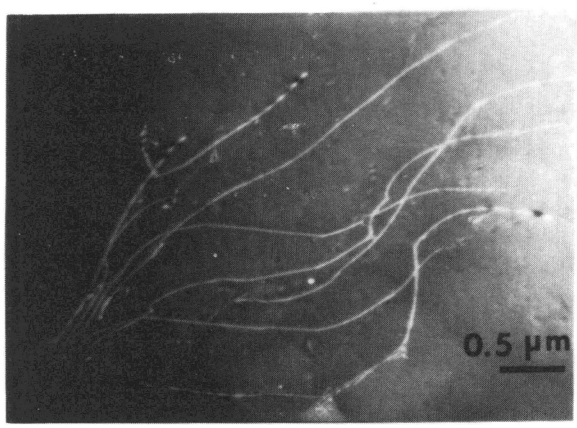


Figure 5. Schematic of SOI surface morphology illustrating the abrupt emergence of subgrain boundaries and their randomly branched pattern.

4. In order to resolve the dislocation configuration the specimen had to be rotated by 45° with the $(11\bar{1})$ diffraction vector as rotation axis. Dislocation separation in the subgrain boundary in Figure 4 is approximately 25 nm. This structure happens to conform exactly to the textbook definition of a low angle grain boundary or tilt boundary.[18,19] The misorientation introduced into the Si film by the low angle grain boundaries (or tilt boundaries) varied between 0.8 and 1.2° according to TEM analysis. TEM analysis has thus identified the nature of the predominant defect. But that still leaves open the question of the origin of these low angle grain boundaries.

Any model for subgrain boundary formation must be able to explain the dislocation nucleation first, and all the precursor stages to the final stable subgrain boundary configuration. From the schematic in Figure 5 it is apparent that all subgrain boundaries start abruptly somewhere in the crystalline Si film. Generally, the subgrain boundaries follow the scan direction for a while until, sooner or later, they coalesce with a second boundary in a characteristic hook like mode. Indeed, superposition with other subgrain boundaries occurs very frequently along the path of a subgrain boundary. In order to determine the underlying mechanism of subgrain boundary formation it is necessary to search for the precursor of this defect and to analyze the details of its nucleation process. In Figure 5 the area of interest for materials analysis is encircled just before the first appearance of individual subgrain boundaries in the surface etch pattern. What is happening in the crystal before the point where the etched boundary lineage emerges, is of crucial importance for the clarification of the origin and nature of this peculiar defect



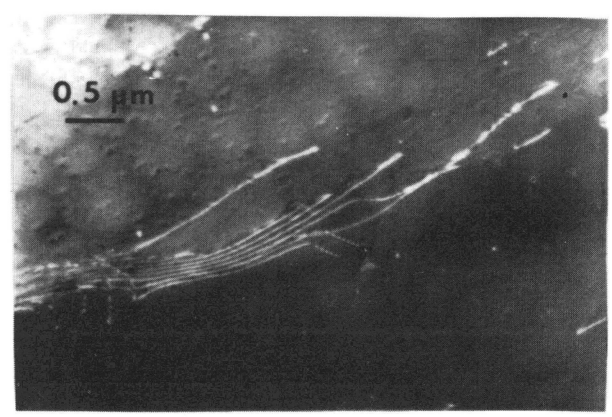


Figure 6 (a) & (b). High magnification TEM micrographs of two different initiation sites of subgrain boundaries, revealing typical random dislocation tangle.

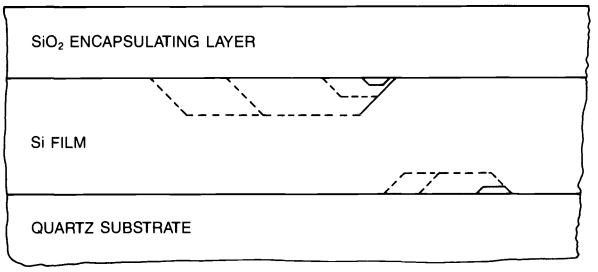
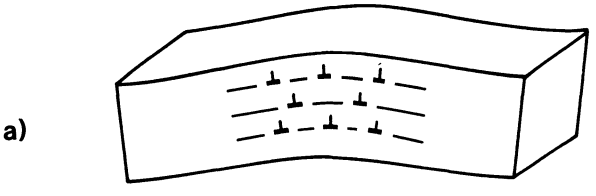


Figure 7. Schematic of dislocation nucleation showing early stage of expanding dislocation half loops.

structure. Figure 6a and 6b shows a TEM darkfield image of the source of a low angle grain boundary. Typical initiation sites of subgrain boundaries in zone-melting grown Si films consist of such high density random tangles of slip dislocations.[20] The nucleation of these slip dislocations takes place at discrete surface steps or other irregularities, which are believed to be uniformly distributed over the surfaces of both the front and backside interface of the recrystallized Si film. It is well established that such surfaces are not planar on an atomic scale but do contain a multitude of surface steps of varying height. These surface steps act as dislocation nucleation sites, whenever local stress concentrations exceed a critical value of about G/30, where G is the shear modulus of the material. In order to reduce the high internal stress concentration local plastic deformation of the solidifying crystal is initiated by nucleation of dislocation half loops.[21] Figure 7 demonstrates the mechanism of stress relief by nucleation of small prismatic dislocation half loops at an activated surface nucleation site. One segment of the dislocation half loop gets pinned at the surface, while the other free segment propagates into the crystalline Si film by thermally activated glide. The pinning points occur at both front and backside interface, as depicted in Figure 7. During the zone-melting process the free segment of the dislocation loop then follows the trailing edge of the moving solid-liquid interface front through the Si film. Our experimental results lead to the conclusion, that the nucleation of slip dislocations at the subgrain boundary sources is the result of high internal stress concentrations occurring periodically in the growing Si film. Basically this periodic plastic deformation accounts for the initial nucleation of the subgrain boundary precursor form, while the subsequent transformation of the random tangle of slip dislocations into a low angle grain boundary is caused by the mechanism of polygonization.

In this recovery process the energy of the crystal containing slip dislocations can be reduced if the dislocations line up one above the other, producing a more stable dislocation wall. The polygonization mechanism is schematically explained in Figure 8. Initiation of plastic deformation by random nucleation of slip dislocation at a stress point of the locally bent crystalline film is depicted in Figure 8a. The dislocations will be randomly distributed on the available glide planes in the thin film. This corresponds to the subboundary precursor stage shown in Figure 6a and 6b. Subsequently, Figure 8b illustrates the rearrangement of individual dislocations by the polygonization recovery process to form the more stable low angle boundary. Glide is a necessary but not



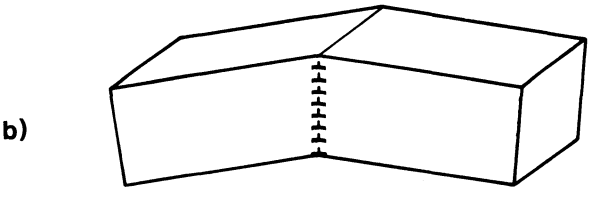


Figure 8. Schematic representation of the formation of a subgrain boundary by polygonization. (a) Plastic deformation of stressed region of bent crystal causing nucleation of random dislocations.

(b) Rearrangement of dislocations by glide and climb processes to form the energetically more favorable subgrain boundary configuration.

sufficient process for the rearrangement of dislocations into a vertical wall configuration. Since the plastically deformed SOI film is heated to a bias temperature of ≈ 1100°C there is sufficient thermal activation for local diffusion of point defects, which enables dislocation climb to change glide planes. Low angle boundaries are configurations of lower energy because stored elastic strain energy is released by the dislocation rearrangement. Equally important, it results in an absence of long range stress fields due to mutual cancellation of the stress contribution of individual dislocations in the boundary configuration. Dislocations outside the attractive potential of the low angle boundary tend to be excluded, but can climb by vacancy diffusion processes into the region of attraction to be incorporated into the boundary. Thus low angle grain boundaries form to accommodate those dislocations which are not annihilated by reactions with other dislocations or at free surfaces. Furthermore the internal changes caused by polygonization are accompanied by a certain softening of the dislocation hardened Si crystal.

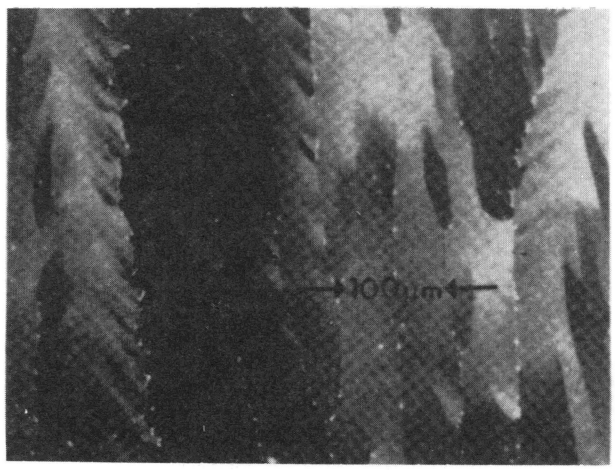


Figure 9. Scanning electron micrograph of recrystallized Si film in the electron channeling contrast mode. Slight crystallographic misorientation between subgrains is revealed by the variations in grey level.

As mentioned before the crystalline regions on each side of the boundary are rotated by equal and opposite amounts about the Z-axis and differ in orientation. That small angular misorientation in the SOI film can easily be made visible in the scanning electron microscope (SEM). Figure 9 shows a SEM micrograph of the surface morphology of recrystallized Si, where the misorientation between the subgrains results in a distinct contrast pattern due to electron channeling.

Plastic deformation

The model presented here basically accounts for the formation and propagation of subgrain boundaries, which are the most characteristic and predominant lattice imperfections in zone-melting grown Si films. There remains the question, what are the possible causes for the high internal stress concentrations in the Si film. Several authors have confirmed the existence of a non-uniform solidification front.[22,23,24] Faceted growth fronts are predicted with the slowest growing (111) crystallographic planes facing the melt. This has indeed been experimentally verified and recently molecular dynamics computer simulations have lent theoretical support to that concept.[25,26] In fact, all possible interfacial instabilities have been observed ranging from a pure faceted growth front to a cellular and dendritic interface. Figure 10 shows an optical reflection

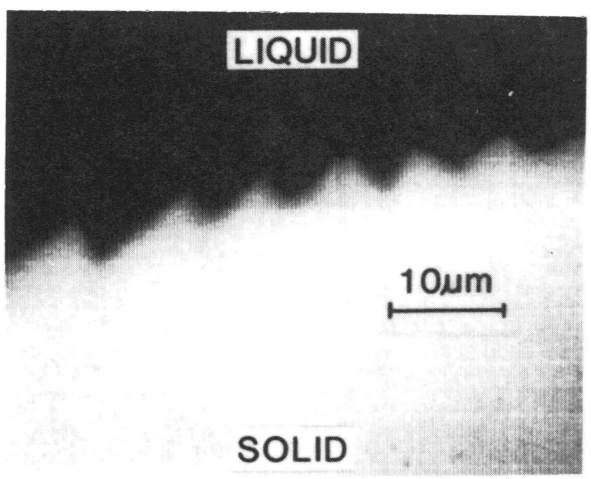


Figure 10. Optical micrograph of the growth front during micro-zone melting of Si film, exhibiting faceted interface.

micrograph of melt front faceting, obtained during in-situ microscopic observation of the laser induced zone-melting recrystallization process. Figure 10 is photographed in light emitted from the hot material and the liquid silicon appears dark because of its lower emissivity compared to the surrounding hot solid Si film. When the Si_3N_4 layers are deposited at both Si interfaces for better wetting characteristics, only a straight planar solid-liquid interface is found and no facets could be optically resolved. In those cases where faceting of the liquid-solid interface does occur, the stress concentration sites in the growing Si crystal coincide with the interior corners of the facets or cells for obvious reasons of crystal growth morphology. It is well known that growth on an atomistic level occurs by the addition of new atoms from the melt to suitable nucleation sites such as edges of steps as illustrated in Figure 11a. Subsequently crystal growth proceeds by lateral growth of ledges. Figure 11b shows the case when the solidification front is bounded by the close packed (111) lattice planes. These facets are not atomically flat but do contain enough steps and ledges to enable lateral microscopic growth to proceed. The nucleation rate depends on the degree of undercooling of the Si melt. Consequently ledge nucleation occurs primarily at the interior corners of facets, the points of highest undercooling. Microscopic facet growth proceeds by the lateral motion of these growth steps and ledges. As a consequence of this growth mode, impurity inhomogeneity and microsegregation may develop. Such a situation can lead to impingement of growth ledges, and in the case of cellular and dendritic solidification fronts, to entrapment of undercooled liquid. When liquid silicon freezes, it will expand by 9%.[27] This large change in volume of the last to freeze liquid exerts large compressive stresses on the surrounding Si film. Naturally this leads to a periodically occurring localization of the internal stressing concentrations at the interior corners of facets or cells. The correspondence between the spacings of subgrain boundaries and facet corners leaves no doubt about the points of stress generation. A good confirmation of these experimental findings was provided by Pfeiffer, et. al.,[28] who numerically simulated the paths of the interior corners as a function of time and obtained patterns very similar to those of actual subgrain boundaries such as in Figure 3. While anomalous freezing of entrapped Si and preferential incorporation of oxygen impurities at interior corners is certainly playing an important role in the build-up of internal stress sites, it probably is not its major cause. Since periodic stress concentrations and its accompanying subgrain boundaries are also observed when no faceting is present, there must be additional mechanisms at work. Non-uniform heat flow and the accompanying lateral temperature gradients during zone-melting recrystallization certainly play an important role. It has been estimated that at 1000°C deviations of about 10°C from a point on a linear temperature gradient curve will result in the onset of plastic deformation in the SOI film.[29] In summary, some of the several causes of dislocation formation and plastic deformation in zone-melting growth of Si films on insulators include: differential volume expansion of Si upon freezing, impurity point defect condensation, growth front impingement and lateral thermal gradients.

All of the above mentioned factors contribute to the strictly localized and periodic internal stress concentrations. But it appears that the last one, lateral thermal gradients caused by non-uniform heat flow, is one of the more important effects.

For completeness sake it should be pointed out that besides subgrain boundaries, which form the major residual growth defect, twin boundaries have been found to occur. Their formation depends to a large degree on the growth velocity and control of the thermal profile. Details of the twin boundary analysis have been described elsewhere.[30]

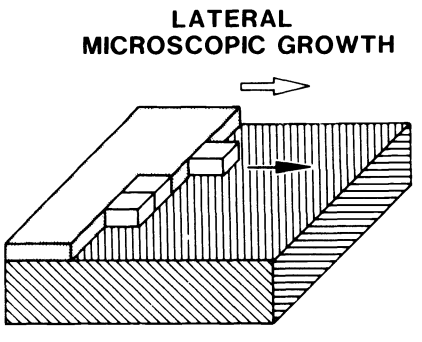
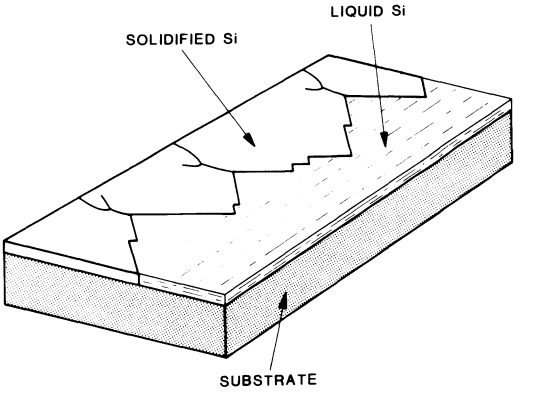


Figure 11. (a) Simplified model of lateral microscopic thin film growth by attachments of atoms at the edges of steps.



(b) Representation of (111) faceted instantaneous growth front, where small growth ledges generate new facets.

Control of residual defects

So far none of the numerous laboratories engaged in SOI research has been able to grow stress-free thin Si films on insulators, which explains the presence of subgrain boundaries in all those films. But important advances have taken place in the continuing effort to control and reduce those residual defects. Based on the detailed understanding of subgrain boundary generation and its relation to the periodically occurring initial stress concentrations in the Si film, techniques have been developed, which effectively control the boundaries. The first techniques used the concept of spatially modulating the temperature profile during crystal growth.[31,32] This is accomplished by photolithographically defining optical absorber stripes on the SOI wafer running parallel to the direction of zone motion as illustrated in Figure 12. Now the optical absorber stripe pattern controls the location, where the internal stress concentration will arise, and thereby controls the locations of subgrain boundaries. This localization technique is also known as subgrain boundary entrainment. The main benefit to be derived from a predefined periodic boundary position is the enlarged defect free area between the gratings, which can be utilized for the fabrication of electronic devices. Also the subgrain boundaries align themselves under the gratings and appear as a straight line in contrast to their otherwise multi-branched random appearance. Presently there are various entrainment techniques in use, but they are all guided by the basic principle of confining random subgrain boundaries to predetermined locations by photolithographical means. As a recent example of a new localization technique the "heat-sink" structure from the C.N.E.T. group[33] should be mentioned, where an artificial periodic relief in the form of stripes is etched in the underlying isolation oxide of an SOI wafer. The LPCVD polysilicon hugs the relief pattern and the constriction keeps the area between the strips defect free. Presently areas free of random defects of 50 μm - 70 μm width between entrained subgrain boundaries have been obtained. In addition the presence of entrained subgrain boundaries in fixed locations can be utilized as gettering centers for the active device areas in between.

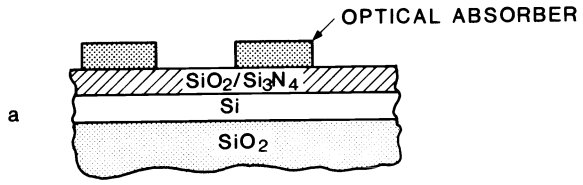


Figure 12. Schematic illustration of grating of optical absorber stripes used to entrain subgrain boundaries along the hottest and most stressed zones.

Thermal expansion matching

When Si films are recrystallized on transparent substrates like quartz, additional material problems have to be addressed. This application is of interest because recrystallized Si films on quartz are attractive for large area active matrix addressed flat panel displays. Since silicon and quartz have different linear expansion coefficients and elastic moduli very large stresses and micro cracks are generated. The linear thermal expansion coefficient α of quartz is $0.5 \times 10^{-6}\ K^{-1}$, which is five times smaller than that of Si with $\alpha = 2.6 \times 10^{-6}\ K^{-1}$. As the silicon cools from melt, its faster contraction relative to the quartz substrate produces tensile stresses, that exceed the yield point of silicon and lead to random micro-cracking of the recrystallized Si film. These cracks make circuit fabrication impractical. As long as the encapsulating SiO_2 and Si_3N_4 layers remain on the sample, crack formation is suppressed and the underlying Si film remains intact. However, as soon as the encapsulating layers are completely removed, micro cracks are inevitably formed. In order to deal with this problem some efficient crack suppression techniques have been developed. The main idea is that sufficiently small islands can withstand the stress without cracking. In this approach the poly-Si film is photolithographically patterned into islands prior to recrystallization as shown schematically in Figure 13.[34] In a variation of this technique deep moats are patterned, which define relatively long hour glass shaped device islands of 100 μm x 25 μm dimension. The moats have been created to prevent cracks from the surrounding Si film to propagate into the device island.[35] Although these techniques are quite successful in crack suppression, they are restricted to very small device islands. In order to enlarge the useable area for device fabrication, we have selected a buffer layer between the quartz substrate and the Si film, whose thermal expansion closely matches that of SiO_2 and Si.[36,37] The buffer layer consists of silicon rich SiO_2 and is also known under the acronym SIPOS, which stands for semi-insulating polycrystalline silicon. SIPOS is an

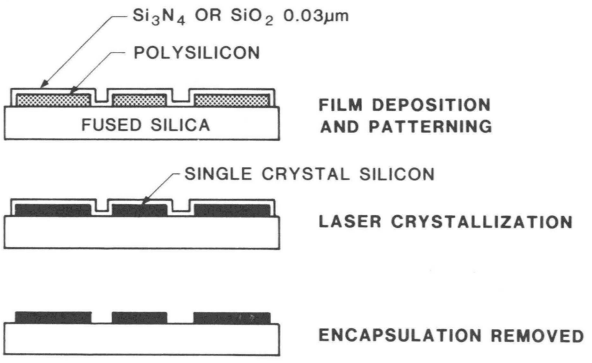


Figure 13. Schematic showing patterning of the Si film on quartz substrates into small device islands.

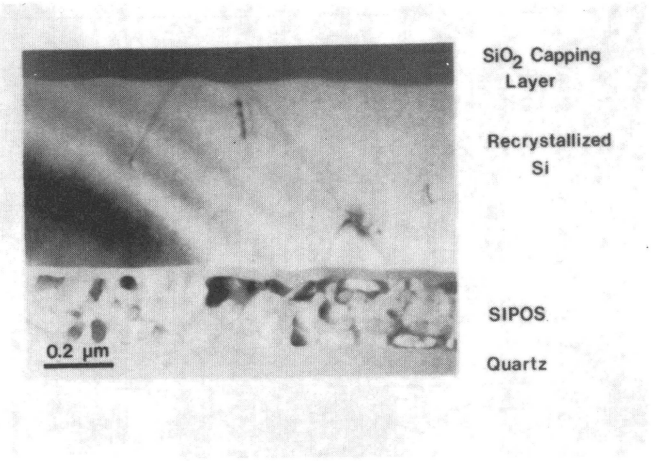


Figure 14. TEM cross section of SOI film with a SIPOS buffer layer to match the different thermal expansion coefficient of substrate and Si film. The laser induced restructuring and microsegregation in the SIPOS film is revealed.

excellent candidate for a thermal matching layer because its linear thermal expansion coefficient can be adjusted to any value between that of Si and SiO_2 as a function of its oxygen content. Furthermore, the fact that the stress in the SIPOS film changes from tensile to compressive following thermal annealing, significantly improves its usefulness as a matching layer. Internal microstructural changes in the SIPOS layer taking place at ≈ 1000°C annealing temperature are responsible for the sudden change in stress behavior. Initially after chemical vapor deposition SIPOS is composed of a homogeneous mixture of amorphous Si and SiO_x. However the material is thermally unstable and subject to structural changes and densification. Upon annealing extensive phase segregation occurs as demonstrated in the cross-sectional TEM micrograph of Figure 14. The combined effects of stress reversal and a matching thermal expansion coefficient α help to reduce the interfacial stress in the recrystallized Si and increase the useable area of device islands. Having extensively discussed the materials properties of the novel silicon-on-insulator (SOI) technology we will proceed to briefly address the question how those materials characteristics and residual lattice defects affect device applications.

Applications

One potentially important application of recrystallized silicon on amorphous transparent substrates, such as quartz, is the fabrication of active matrix-addressed flat panel displays. For a display medium such as liquid crystals, a large area, transparent, inexpensive substrate is required. That implies that for reasons of cost reduction the thin film transistor (TFT) matrix will eventually have to be made on cheap glass substrates. At the same time, there is serious competition from amorphous silicon TFTs and polycrystalline silicon TFTs, which have considerable cost advantages. In this paper, however, we will exclusively focus on single crystalline silicon films grown on quartz substrates. Because of its high purity, thermal shock resistance and melting point far above that of Si, quartz substrates are fully compatible with conventional Si MOS technology, and thus well suited for first feasibility studies. Other applications include large area integrated circuits for image sensors.

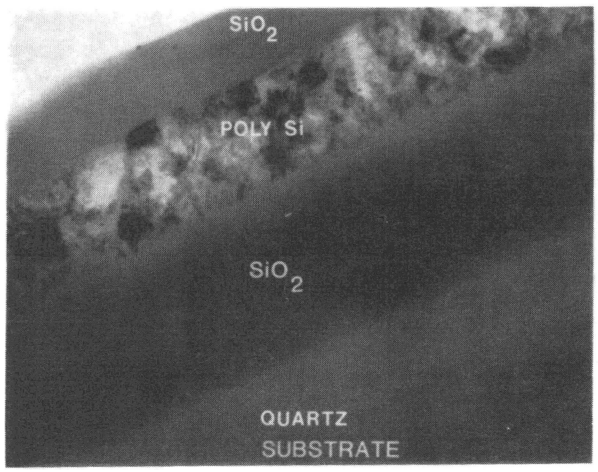
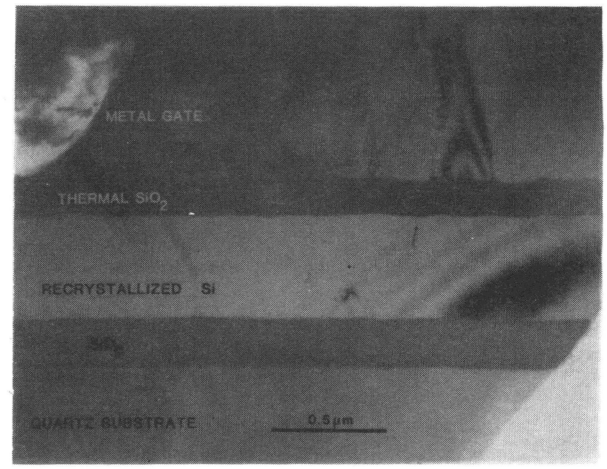


Figure 15. (a) TEM cross section of SOI multilayer structure prior to ZMR processing showing the original fine grained polycrystalline Si film.



(b) TEM cross section of a completed MOSFET thin film device in recrystallized single crystal Si on quartz.

The electrical characteristics of zone-melting recrystallized Si on quartz substrates have been characterized using MOSFET thin film transistors. Aluminum gate field effect transistors were fabricated in the SOI material by standard IC processing with a thermally grown oxide layer for the gate dielectric and conventional ion implantation for channel and source-drain implants. Figure 15 illustrates the profound differences between the starting material and the finished device grade material. In Figure 15a the TEM cross-section of the LPCVD deposited poly-Si film shows the material to be dominated by randomly oriented small grains of less than 100nm in size and large angle grain boundaries. In contrast to that, the recrystallized Si on quartz in Figure 15b reveals single crystalline material with no defects between the periodically occurring dislocation walls (subgrain boundaries). Figure 15b is actually a high magnification cross section through the gate area of a finished thin film transistor and reveals some oxidation induced stacking faults in the Si film. But these faults were introduced at a later stage during device processing and high temperature oxide growth for the gate dielectric. Figure 16 shows a plot of the I-V characteristics of a p-channel MOS transistor. The insert in Figure 15 shows an optical micrograph of the actual transistor. It has been verified by optical inspection that the gate region of the transistor was intersected by several subgrain boundaries. Nevertheless, the field effect mobility in these devices suffers no degradation and averaged around 180 cm^2/V sec. This value is comparable to that obtained in transistors

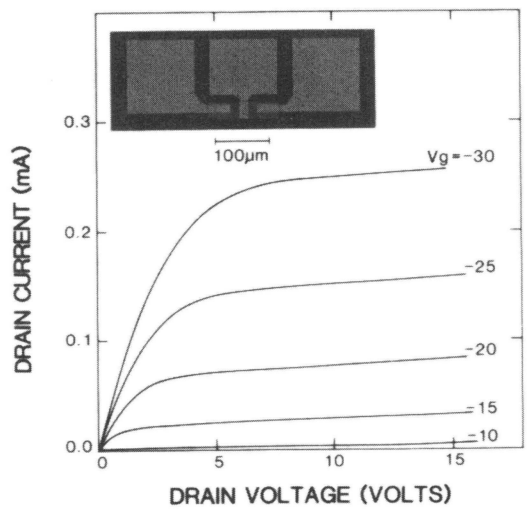


Figure 16. Electrical characteristics of a p-channel MOSFET thin film transistor fabricated in recrystallized Si on quartz.

fabricated in dislocation free bulk silicon substrates. At MIT Lincoln Laboratory the effect of subgrain boundaries, the predominant defect, on majority carrier transport has been studied using n-channel MOSFETs with electron transport either parallel or perpendicular to the subgrain boundaries. Both cases show nearly identical surface electron mobility.[38] A wealth of experimental data suggests that subgrain boundaries in ZMR silicon-on-insulator films do not have a significant effect on majority carrier transport and MOSFET performance. The trapping state density of subgrain boundaries is approximately 7 x 10^{11} cm^{-2}, which is low enough and does not produce a large potential barrier to impede carrier transport.[38] This can be understood on the basis of the core structure of a subgrain boundary shown in Figure 17. As explained earlier, it consists of a wall of dislocations, representing the energetically most favorable defect configuration. Between the individual dislocations, which are separated by typically 20-25 nm, there are significant regions of perfect, undisturbed lattice, where carrier transport can take place unimpeded.

While subgrain boundaries have little effect on MOS field effect transistor performance the large tensile stress in silicon films recrystallized on quartz substrates does. X-ray diffraction data suggest that tensile stresses as large as 9.6 Kbar are present in SOI films on quartz.[39] The Hall electron mobility can be ≈ 70% higher and the hole mobility 14% lower than the corresponding mobility values in unstressed Si films. In fact the large stress enhanced mobility for electrons in n-channel MOSFETs on quartz is a positive feature that helps to improve device performance.

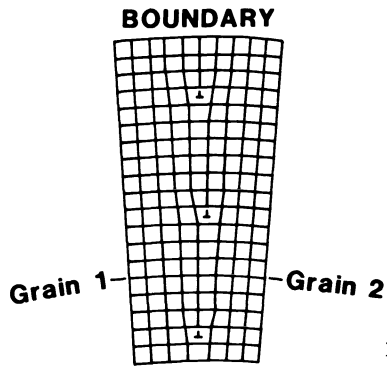


Figure 17. Geometrical model of vertical array of dislocations, which forms a subgrain boundary.

Conclusion

The current status of zone-melting recrystallization (ZMR) for SOI applications has been reviewed. In recent years this successful approach to dielectric isolation of Si has been developed from an advanced technique to a fairly mature technology. With the newer composite Si_3N_4/SiO_2 encapsulation layers the yield is very good so that entire 4" or 5" SOI wafers can be recrystallized without any seeding on a routine basis. The level of understanding the physics of residual growth defect generation has sufficiently progressed to allow effective and reproducible control of the predominant subgrain boundaries, twins and grain boundaries by entrainment techniques.

Subgrain boundaries as the major remaining lattice imperfection turn out to have only negligible effects on majority carrier transport and MOSFET performance. In a direct comparison with the other competing SOI technologies the zone-melting technique looks even better. Dielectric isolation can also be achieved by high dose oxygen implantation to create a buried oxide layer underneath a thin surface film. This approach is widely known by the acronym SIMOX (separation by implanted oxygen). SIMOX technology produces SOI films with an extremely high density of random defects typically of the order of 10^8 - 10^9 cm^{-2}. In contrast to this, ZMR Si films have a much lower defect density of 10^4 - 10^5 cm^{-2}.

The ZMR technology has the added advantage that the residual defects occur only periodically and can be confined to strictly predetermined locations. This cannot be achieved in SIMOX films, where the lattice defects are completely randomly distributed throughout the Si film. A similar problem is encountered in the hetero-epitaxial technology of Silicon-on-Sapphire (SOS): very high defect densities (≈ 10^8 cm^{-2}) of randomly occurring misfit dislocations and stacking faults. The defect density even increases with increasing proximity to the silicon-sapphire interface.

In summary, in terms of crystal quality and residual defect densities, zone-melting recrystallizated (ZMR) Si films on insulators have clear advantages over the SIMOX and SOS technologies and remain in a good position to compete with them. The ZMR material is sufficiently good to support the fabrication of large area integrated circuits and could make an impact on flat panel displays and future 3 dimensional integrated circuits.

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