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Air-gap gating of MgZnO/ZnO heterostructures

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The adaptation of "air-gap" dielectric based field-effect transistor technology to controlling the MgZnO/ZnO heterointerface confined two-dimensional electron system (2DES) is reported. We find it possible to tune the charge density of the 2DES via a gate electrode spatially separated from the heterostructure surface by a distance of 5 μm. Under static gating, the observation of the quantum Hall effect suggests that the charge carrier density remains homogeneous, with the 2DES in the 3 mm square sample the sole conductor. The availability of this technology enables the exploration of the charge carrier density degree of freedom in the pristine sample limit. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4894155]

I. INTRODUCTION

The development of a new material platform requires advances in both sample fabrication and means of experimentally controlling the systems parameters. In the case of two-dimensional electron systems (2DES) confined at heterointerfaces, molecular-beam epitaxy (MBE) has made tremendous contributions by suppressing scattering origins and hence improving the quality of the 2DES[1–3] while access to electrostatic gating then unlocks the carrier density (n) degree of freedom to be explored experimentally. For this, the prevailing technique ubiquitous in the semiconductor industry and fundamental research realms alike is the formation of metal-oxide-semiconductor field-effect transistors (MOSFET) and Schottky metal semiconductor FET, where by a thin dielectric or depletion layer between the conducting channel and gate electrode facilitates tuning of the system's Fermi energy.[4,5] Owing to such prevalence, many gate dielectric materials have now been studied to extract optimal transport properties.[6–8] However, the employment of such solid-state dielectrics inevitably has drawbacks including inducing disorder at the interface with the device under investigation as well the presence of trapped/mobile charges resulting in hysteretic electrostatic response. To circumvent such problems, a technique involving the use of an "air-gap" dielectric has recently emerged in fundamental research studies. First explored in the field of organic semiconductors,[9–12] the fruits of adapting such techniques to two-dimensional (2D) materials are now seen notably in state-of-the-art graphene devices. In separating the graphene flake from the solid-state dielectric of SiO_2 and mitigating the surface roughness and/or impurity potential disorder it imposes, so-called "suspended graphene" devices are now clean enough to reveal the previously masked fragile physical details.[13–15] The application of the "air-gap" structure hence possesses great potential for preserving pristine quality of a wide range of 2D materials and heterostructure confined 2DES.

In this letter, we report the adaptation of air-gap field-effect transistor (AFET) technology to controlling the electrical characteristics of a MBE grown solid-state 2DES. The prototype system we explore is the MgZnO/ZnO heterointerface which has emerged in recent years as the host of a high mobility 2DES.[16,17] Since this 2DES is on the order of 200 nm below the sample surface, this study may seem rather removed from the AFET reports on 2D materials which are inherently exposed, and hence susceptible to the surrounding environment. However, it is acutely obvious that even in buried 2DES, long-range Coulombic disorder can severely affect fragile electronic ground states observed at low temperatures.[18,19] Hence, this technology is aimed at superseding the standard MOSFET devices which have been previously reported,[20,21] enabling access to the charge carrier density degree of freedom in the pristine sample limit by eliminating unnecessary sample processing steps and surface disorder. The device we present is measured in van der Pauw geometry which enhances the simplicity of design, while simultaneously acting as a particularly useful tool in evaluating the uniformity of transport. Using the AFET technology, we find it experimentally possible at low temperature to tune the 2DES across the wide range of $\Delta n = 3 \times 10^{11}\,\mathrm{cm}^{-2}$ within ± 200 V gate voltages (V_G) while retaining electron mobility values close to that of a raw piece of the same wafer. Simultaneously, the electric-field controlled n remains homogeneous as illustrated through the observation of the integer and fractional quantum Hall effects.

II. AIR-GAP FET

Figure 1(a) shows a schematic representation of the AFET device, which consists of two components. One is the MBE-grown sample to be measured and the other is the stage on which the sample is placed, resulting in the gate electrode being spatially separated from the sample surface. Based on

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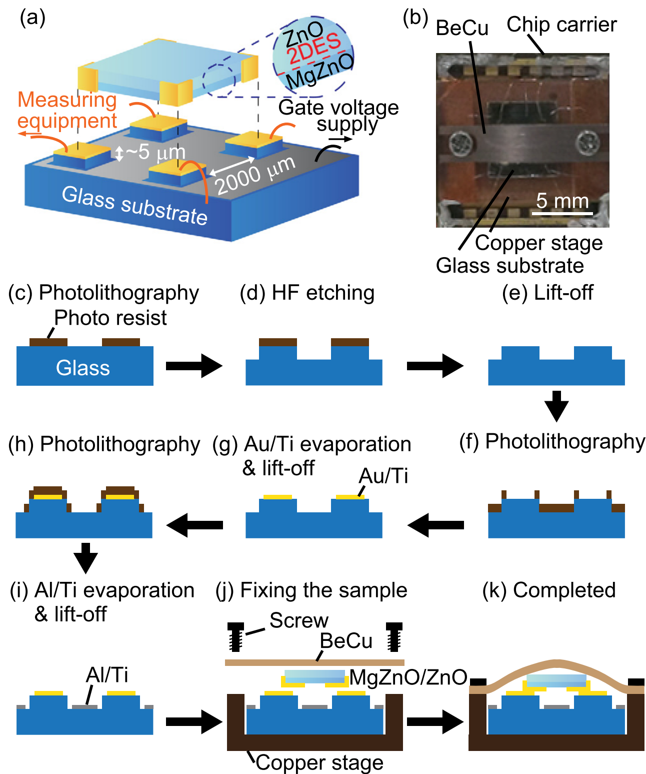

FIG. 1. (a) A bird's-eye view of the MgZnO/ZnO heterostructure placed upside down on a stage with four Au/Ti capped pillars, contacting the ohmic contacts on the sample, and hence the 2DES. The gate electrode is isolated by an air-gap dielectric. Both the pillars and the gate are then wire bonded individually. The distance between pillars is 2 mm and their height $\approx 5\,\mu$m. (b) A microscope image of the air-gap device from the top after fixing the MgZnO/ZnO sample to the glass stage with the BeCu spring, which is placed on a copper stage. (c)-(k) Flow of the air-gap device fabrication. The dimensions are not accurately drawn in (c)-(k).

this design, the sample itself requires few processing steps and the gating structure is an independent, reusable unit, thus allowing efficient characterization by exchanging only the sample. These units are fabricated independently as detailed below and combined just before measurements are performed. In order to keep the distance between the ohmic electrodes and gate electrode constant from room to low temperatures, a BeCu flat spring is used to fix the sample. As shown in Fig. 1(b), the 0.3 mm thick BeCu is cut to roughly the same size as the sample, and then screwed to the copper stage, which is fixed to the chip carrier by varnish. In this geometry, the difference of thermal expansions between the glass substrate and other parts (ZnO, BeCu, screws, etc.) is buffered by the BeCu spring, which keeps pressing the MgZnO/ZnO sample to the glass substrate with an appropriate pressure. As introduced above, the conducting channel in this structure is found at the MgZnO/ZnO heterointerface, some 200 nm below the sample surface. This necessitates the 2DES being contacted at the sample edges and results a macroscopic size device at the current technological level. This potentially has the following negative drawbacks: increased leakage currents and non-uniformity in the gate-induced electric field. To mitigate such risks, we have designed the air-gap thickness to be 5 μm, much thicker than other reports which typically utilize $\approx$ 100 nm.[10,12]

To begin with, the gate unit is made of a glass substrate with four pillars defined by optical lithography (Fig. 1(c)) and then etched by hydrofluoric acid (Fig. 1(d)). This etching is performed at room temperature by immersing the glass substrate in 47% concentration hydrofluoric acid for 70 s, resulting in 5 μm high pillars. A short etching time is desirable as the sticking of the photoresist to the glass substrate deteriorates with time, leading to poorly defined pillars. After etching, the stage is then washed in acetone to remove the photoresist (Fig. 1(e)). Without this step, acid which penetrates beneath the photoresist remains resilient to rinsing, resulting in non-uniformity in the etched depth. After the pillars are defined, 100 nm Au/10 nm Ti is evaporated on the top of these pillars to form the bonding pads and to make contacts to the electrodes on the sample (Figs. 1(f) and 1(g)), while 20 nm Al/10 nm Ti is evaporated on the remaining surface area, to form the gate electrode (Figs. 1(h) and 1(j)). Finally, the ohmic electrodes of the MgZnO/ZnO 2DES sample are contacted to the Au/Ti electrodes of the glass stage by fixing the sample down with the BeCu spring and two screws.

The sample, a 3 mm square chip, is cut from a wafer of MgZnO/ZnO grown on a single crystal ZnO substrate. Four ohmic contacts consisting of 100 nm Au/10 nm Ti and roughly 0.5 mm square in size are evaporated at the edge of the sample on its surface using a metal mask, contacting the 2DES and yielding a device measurable in van der Pauw geometry. Finally, the heterostructure is exposed to O_2 plasma for 30 s. This treatment has the effect of reducing the 2DES charge carrier density, which may be later compensated by gating, presumably through the formation of charged defects at the surface.[22] This is a commonly used method to improve rectification behavior in ZnO Schottky junctions[23–25] and empirically without such a treatment the gating efficiency was observed to be poor.

III. RESULTS AND DISCUSSIONS

Electrical measurements are performed at $T = 500$ mK in a 15 T superconducting magnet equipped ^{3}He cryostat. At such low temperatures, the ZnO bulk substrate is insulating leading to the 2DES being the sole conducting channel. Two measurement techniques are utilized. First, direct current measurements performed using a semiconductor parameter analyser (4156C and 41501B, Agilent Technologies) with 1 mV drain voltage establish the V_G dependence of the device. To explore the effect of static gating on magnetotransport, alternating current lock-in measurements were performed with a current of 100 nA, (14 Hz) after the V_G dependence is characterized. During each magnetic field sweep, V_G is fixed. Leakage current is negligibly small (<50 pA) for all measurements. In order to evaluate the carrier modulation efficiency, a LCR meter (4284 A, Agilent Technologies) is used to measure the capacitance between the gate and 2DES.

The conductance, G, of the 2DES as a function of gate voltage V_G is shown in Fig. 2. Note that the G in Fig. 2 is only for one pair of contacts in the van der Pauw geometry. With increasing V_G, G increases linearly along the line

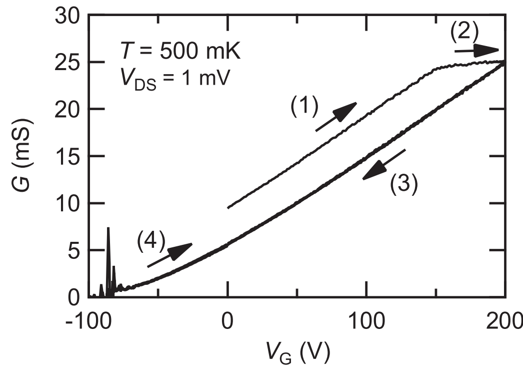

FIG. 2. The transfer characteristics of conductance (G) between one set of contacts in the van der Pauw geometry as a function of gate voltage (V_G) for the MgZnO/ZnO AFET device. (1) At first, G linearly increases with positive V_G. (2) Saturation occurs above $V_G = 150$ V from which (3) G reduces linearly with decreasing V_G, ultimately returning (4) to $V_G = 0$ V from -100 V.

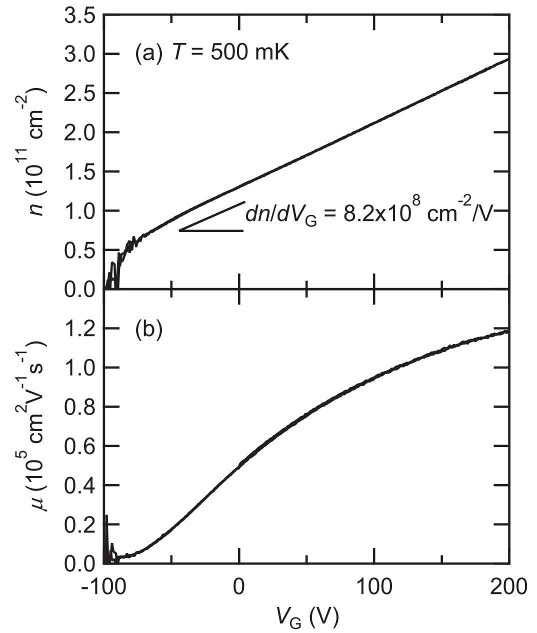

FIG. 3. Gate voltage dependence of the device. (a) Carrier density n and (b) electron mobility μ as a function of V_G. (a) n is seen to increase linearly as a function of V_G above -50 V at a rate of $8.2 \times 10^8 \mathrm{cm}^{-2}$/V. Carriers in the heterostructure are completely depleted around -100 V. (b) Mobility μ as a function of V_G. The maximum μ of 120 000 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ is achieved at maximum accumulation of n.

labelled (1). At a positive bias of 150 V, G is seen to saturate as shown in region (2). From here, when decreasing V_G, we observe a reduction in G, not along the original trace, but immediately, as shown in region (3). Finally, while going back to $V_G = 0$ V (4), G increases along same trace on (3) with no hysteresis. Once this loop is established, it is reproducible over multiple sweeps along same trace on (3) and (4). In region (2) where saturation in G occurs, it is evident that the electric-field no longer acts to accumulate electrons into the 2DES. Rather, immobile charges are likely formed near the surface of MgZnO capping layer, which in turn screen the gate induced electric-field, effectively weakening its effect on the 2DES.[26] In fact, we observe a similar saturation of G also in the case of conventional MOSFETs using Al_2O_3 gate dielectric.[21] While this concisely explains the shift in the required V_G after saturation, entering such a regime should be avoided in final device operation. In any case, the sample may be "reset" by heating to room temperature, resulting in a return to the original conductivity behavior.

As G is a product of both the charge density n and mobility μ of the 2DES, the respective contributions are quantified in Fig. 3 for the section corresponding to (3) of Fig. 2. Working under the assumption that at each V_G the Hall resistance $R_{xy}(B)$ is linearly dependent at low magnetic field B as given below

$$n = \frac{1}{e\left(R_{xy}(+0.5\mathrm{T}) - R_{xy}(-0.5\mathrm{T})\right)}, \quad (1)$$

where e is the elementary charge, n is deduced. This is then used to calculate $\mu = G_{\mathrm{sheet}}/ne$. From being completely depleted at around $V_G = -100$ V, n increases linearly above -50 V to 200 V, ultimately saturating at $n = 2.9 \times 10^{11}$ cm^{-2}. This is the maximum number of charge carriers which may be accommodated by the spontaneous polarization mismatch at the heterointerface. The carrier density modulation constant is 8.2×10^8 cm^{-2}/V. This value is about one-third of the expected value of 2.3×10^9 cm^{-2}/V calculated from the measured capacitance of the device $C = 370$ $\mathrm{pF/cm}^2$. This reduced modulation ratio may be related with charged defects at the MgZnO surface screening the electric field. If fact, conductivity cannot be modulated at all without the O_2 plasma treatment as noted above, and the modulation ratio much depends on sample to sample. This observation indicates that, while an air-gap transistor is defect-free in the gate dielectric, the operation is still susceptible to the defects at the surface of the channel or capping layer. In the measurements, the largest mobility of 120,000 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ is achieved at 200 V with carrier density of 2.9×10^{11} cm^{-2}. These values are limited by the saturation in G as discussed above and are close to the values observed in a separately measured raw chip of the same wafer without gate unit.

Finally, we explore the techniques compatibility with typical magnetotransport measurements performed on low dimensional systems. Figure 4 displays the magnetotransport data at $T = 500$ mK of the device under applied static gate voltages, corresponding to a range of $n = 0.87 \times 10^{11}$ cm^{-2} to 2.9×10^{11} cm^{-2}. In these traces, we follow the filling factor (ν), given by $\nu = nh/eB$, where h is the Planck constant, indicating how many Landau levels are populated at a certain B. Prominent integer and fractional quantum Hall states are seen at $\nu = 2$ (circle), $\nu = 1$ (triangle), and $\nu = 2/3$ (square) and are observed to shift systematically as described by the relationship above. The most robust state, $\nu = 1$, is noted to remain zero resistance throughout the voltages applied. This non-dissipative transport confirms the two dimensional nature of the conducting channel without any parasitic conduction, even when the sample surface is exposed to high voltages. In the dilute limit of the measurement ($n = 0.87 \times 10^{11}$ cm^{-2}), we begin to encounter the limitations of the technique application to this sample. As seen in the red curve of Fig. 4(b), the R_{xy} displays non-monotonic behavior with increasing B. While mixing in this van der Pauw geometry likely plays a role as the R_{xx} and R_{xy} become

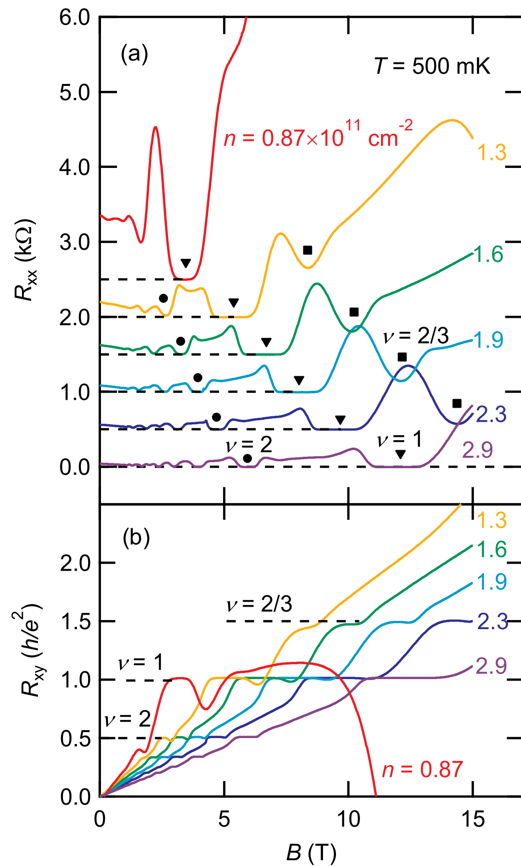

FIG. 4. Magnetotransport at $T = 500$ mK of the 2DES under static gating. (a) The longitudinal resistance R_{xx} curves correspond to carrier density of 0.87, 1.3, 1.6, 1.9, 2.3, 2.9 $\times 10^{11}$ cm^{-2}, respectively, from top to bottom with offset of 0.5 kΩ. (b) The Hall resistance R_{xy} curves for the same carrier densities. Notable quantum Hall states of $\nu = 2$, 1, and 2/3 are identified by closed circles, triangles and squares in (a), respectively.

similar in magnitude, such dramatic behavior beyond $\nu = 1$ suggests that depletion around the ohmic contacts affects the contact to 2DES edge channels. Further optimization of contacts is therefore likely to be a generic but crucial requirement for material systems adopting this design to enhance the versatility of the gate unit described.

Despite this limitation, the AFET has the advantage over conventional MOSFET devices in maintaining clear signals of the quantum Hall effect into the dilute regime. In Refs. 20 and 21, the quantum Hall effects were observed with varying the carrier density via gating across an Al_2O_3 dielectric. However, under slight depletion fractional states rapidly were degraded already at carrier densities of 3.7×10^{11} cm^{-2} in a sample of comparable quality to the one in the current study.[20] Even with a higher quality sample in Ref. 21, the fractional states suffer significantly by $n = 1.6 \times 10^{11}$ cm^{-2}. As we describe here, the current AFET structure allows us to maintain clear fractional quantum Hall features to carrier densities as low as 10^{11} cm^{-2}.

IV. SUMMARY

In conclusion, we have developed the technology which enables the use of an air-gap dielectric to electrostatically tune the electrical characteristics of a solid state 2DES confined in MgZnO/ZnO heterostructures in van der Pauw geometry. The method has the advantage of using a reusable gating unit separate from the sample under investigation, providing relatively easy and fast turn-around between experiments. We find tunability of n over an order of magnitude while retaining μ values close to that of a raw pristine sample from the same wafer. This technique is therefore complimentary to the ability to tune the charge density through controlled doping regimes, for example the Mg content in MgZnO. Under static gating, the electric field acting on the 2DES in MgZnO/ZnO remains homogenous enough to allow the observation of zero resistance quantum Hall states when applying a large perpendicular magnetic field and evidences that compared to previous studies which utilized solid-state gating,[20,21] disorder is suppressed in the magnetotransport data approaching $n \approx 1.0 \times 10^{11}$ cm^{-2}. Future efforts to realize more contacts while reducing the thickness of air-gap itself to increase the electrostatic tuning efficiency will yield a versatile technique for enabling the exploration of the carrier density degree of freedom in various heterostructures, surfaces and 2D materials.

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