University of Nevada, Reno

Boost Matrix Converters in Clean Energy Systems

A dissertation submitted in partial fulfillment of the
requirements for the degree of Doctor of Philosophy in
Electrical Engineering

by

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ABSTRACT

This dissertation describes an investigation of novel power electronic converters, based on the ultra-sparse matrix topology and characterized by the minimum number of semiconductor switches. The Z-source, Quasi Z-source, Series Z-source and Switched-inductor Z-source networks were originally proposed for boosting the output voltage of power electronic inverters. These ideas were extended here on three-phase to three-phase and three-phase to single-phase indirect matrix converters.

For the three-phase to three-phase matrix converters, the Z-source networks are placed between the three-switch input rectifier stage and the output six-switch inverter stage. A brief shoot-through state produces the voltage boost. An optimal pulse width modulation technique was developed to achieve high boosting capability and minimum switching losses in the converter.

For the three-phase to single-phase matrix converters, those networks are placed similarly. For control purposes, a new modulation technique has been developed. As an example application, the proposed converters constitute a viable alternative to the existing solutions in residential wind-energy systems, where a low-voltage variable-speed generator feeds power to the higher-voltage fixed-frequency grid.

Comprehensive analytical derivations and simulation results were carried out to investigate the operation of the proposed converters. Performance of the proposed converters was then compared between each other as well as with conventional converters. The operation of the converters was experimentally validated using a laboratory prototype.

To my beloved wife Maria and my son Ersan…

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Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Background

Penetration of clean energy, mainly the wind and photovoltaic (PV) generated electrical energy, in the power grid is increasing exponentially. Both the wind and PV power plants are connected to the grid through converters, transferring the generated DC power in PV applications and AC power in wind power (WP) applications to the AC grid. The aim of the dissertation is to propose new topologies, modulation techniques, and control of grid converters for WP applications. Throughout the various types of proposed topologies, non-grid cases are explained and then followed by grid applications.

Parameters of the output voltage of most renewable energy sources tend to fluctuate with the varying supply of input power. A wind turbine driving a synchronous generator represents a typical example of the disparity between the voltage of the generator and that of the utility grid, and an appropriate power electronic interface is needed to reconcile that disparity. The required ac-ac power conversion is usually performed indirectly as ac-dc-ac conversion in a back-to-back converter, shown in Fig. 1.1.

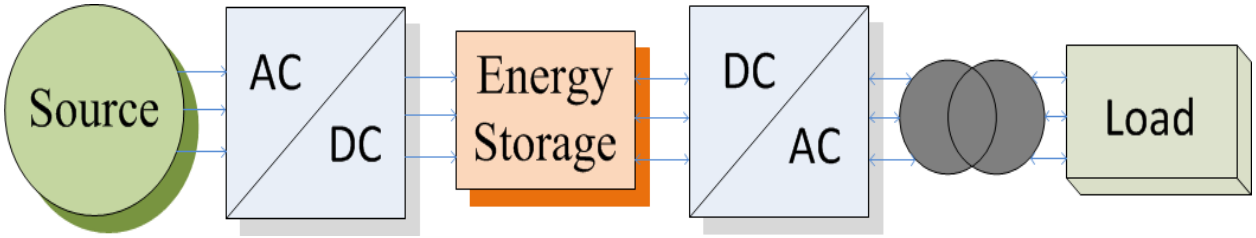


Fig. 1.1 Ac-dc-ac conversion in a back-to-back converter.

In recent years, matrix converters have awakened the interest of researchers as an alternative solution. Aside of small LC filters, direct matrix converters do not need the high-capacitance dc link typical for the back-to-back converters, provide a unity input power factor and sinusoidal input and output currents, but their voltage gain is inherently limited to 0.866 with direct ac-ac conversion as shown in Fig. 1.2. Having several bidirectional switches increases the cost of the converter as well as the conduction losses.

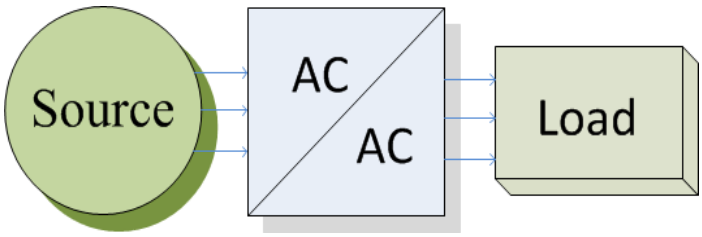


Fig. 1.2 Transformerless direct ac-ac conversion.

A classic three-phase to three-phase matrix converter is based on nine bidirectional switches. Each switch is composed of two unidirectional switches and two diodes or a single switch and four diodes although certain manufacturers, e.g., Fuji Electric, have developed integrated bidirectional switches for their products [1]. Recently, sparse and ultra-sparse matrix converter topologies have been introduced to reduce the switch count [2].

High reliability and power density are important features of power electronic converters, affecting the total cost of many applications [3]. This issue is particularly relevant in the context of residential wind energy systems, whose popularity has been hampered by real and perceived expenses. A typical wind-energy system consists of a turbine, a gearbox, a three-phase ac generator, a power converter, and an optional step-up transformer connecting the system to the grid. The gearbox/transformer tradeoff is necessary, as slow-motion generators tend to produce low voltages. The gearbox or the transformer increase the cost, weight, and volume of the

system, and reduce its overall reliability. Therefore, a possibly simple matrix converter with voltage-boosting capability would represent a promising solution.

Because of the limited voltage gain and complex control algorithms, matrix converters have not yet been commonly used in industry [4]. To overcome these drawbacks various control algorithms and topologies have been proposed. In [5] application of a direct matrix converter connected to a step up-down transformer is proposed for a wind-turbine system. Alas, the use of transformer increases the system's weight, volume, and cost, and reduces the reliability system. Another solution for increasing the voltage gain to unity and beyond is the indirect matrix topology, where a voltage-boosting network is inserted between the input rectifier and output inverter stages. The recently popular Z-source network, first proposed in [6], is well-suited for that role [7]-[9]. Current modulation techniques for indirect Z-source matrix converters are investigated in [10]. An optimal modulation approach provides high buck-boost flexibility, minimum commutation count, and ease of implementation. In [11], a grid interface for wind turbine generators based on an ultra-sparse matrix converter is described. The system integrates a generator-side three-switch buck-type rectifier and a grid-side Z-source inverter. The Z-source network allows boosting the voltage two to three times. Expansions of the Z-source dc link for buck-boost inverters, called Quasi Z-source network, Series Z-source network and Switched-inductor Z-source, were recently proposed in [12-14].

In practical applications, in order to provide a high boost factor for a low-voltage dc power source, the Z-source converter would have to operate under extreme conditions of long shoot-through zero states. The constraints of a low modulation index and a long shoot-through state cause a conflict between the output power quality and system boost ability. Therefore, the practical boost factor of Z-source impedance network is restricted. The Quasi Z-source network,

Series Z-source network and Switched-inductor Z-source networks aim at a solution of that problem.

1.2 Dissertation Objectives

This dissertation proposes a number of converters, all based on the ultra-sparse matrix topology characterized by the minimum number of semiconductor switches. Z-source network, quasi Z-source network, series Z-source network and switched-inductor Z-source network were originally developed for boosting the output voltage of power electronic inverters. These ideas are extended here on a three-phase indirect matrix converters and three-phase to single-phase indirect matrix converters. For three-phase matrix converters, these circuits are placed between the three-switch input rectifier stage and the output six-switch inverter stage. A brief shoot-through state produces the voltage boost. An optimal pulse width modulation technique was developed to achieve high boosting flexibility and minimum switching losses in the converter. Similarly, for three-phase to single-phase matrix converters, these networks are placed between the three-switch input rectifier stage and the output four-switch inverter stage. To control them, a new modulation technique has been developed. As an example application, the proposed converters constitute a viable alternative to the existing solutions in residential wind-energy systems, where a low-voltage variable-speed generator feeds power to the higher-voltage fixed-frequency grid.

1.3 Content of the Dissertation

This dissertation contains seven chapters, which address different aspects of the project objectives:

Chapter 1 is the introduction to the dissertation. It describes research motivation and the outlines of the project.

Chapter 2 gives a technology overview of the matrix converter topologies and their control methods. It discusses in detail the concept of the direct matrix converter, indirect matrix converter, sparse matrix converter, and boost matrix converter topologies. A combined space vectors based indirect modulation technique is widely discussed.

Chapter 3 gives a technology overview of the boost type inverter networks that include Z-source inverter, series Z-source inverter, quasi Z-source inverter, and switched inductor Z-source inverter. The circuit analysis and operation principle are discussed with analytical derivations.

Chapter 4 proposes three different types of three-phase boost matrix converters based on ultra-sparse matrix converters and series Z-source, quasi Z-source, and switched inductor Z-source networks. A new control technique is provided to maximize the efficiency of these converters. Experiment and simulation results are shown to confirm the ability of the converters to overcome the voltage gain disadvantage of the classic matrix converters.

Chapter 5 extends above considerations on single-phase boost matrix converters. Simulation results are provided to illustrate capabilities of those converters.

Chapter 6 presents the hardware implementation and experimental setups for the boost matrix converters. Structures of the prototype converters are described and design of each circuit is explained in detail. Control firmware based on Texas Instruments microprocessor is discussed.

Chapter 7 contains the conclusion of the dissertation. It summarizes the work done and the main findings of the PhD research. Possibilities for improving the investigated topologies are outlined for future work.

Chapter 2

Topologies and Modulation Techniques of Matrix Converters

2.1 Matrix Converter Topologies

Matrix converter (MC) topologies are based on semiconductor, usually bidirectional, power switches. In most cases, an MC consists of nine bi-directional switches. The name of the converter comes from the arrangement of these switches in a matrix pattern. Gate signals are modulated to achieve sinusoidal input and output currents.

Matrix converters first appeared in a book by Gyugui and Pelly [15] and in a journal publication by Daniels and Slatery in 1976 [16]. The concept was presented as AC-AC direct power conversion [17]. Since then various types of MC topologies have been studied. Classification of MCs is shown in Fig. 2.1.

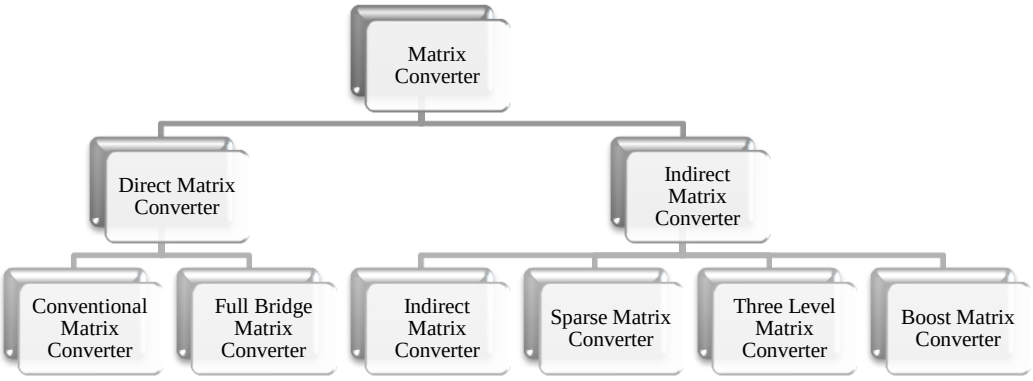


Fig. 2.1 Classification of matrix converters [18].

As no energy is present in the MC, the output voltages have to be generated from the input voltages. Output voltages need to fit in the envelope curve. The minimum envelope curve

is the 0.866 times the peak input balanced line voltages. Thus the minimum envelope curve is 0.866 times the peak input balanced line voltages. This is a gain limitation of most matrix converters.

Another aspect of the output voltage is the harmonic content. Compared to two level voltage source inverters, matrix converters can be considered as three level converters since the input three-phase voltages appears at the output with varying levels. This reduces the harmonic loss [18]. The input current of the MC is directly related to the switching control of the converter and MC can control the phase angle of the input currents. Besides the fundamental component, the input current has a high harmonic content around the switching frequency. A filter is therefore used to average the chopped current [19].

One of the critical issues when investigating a converter topology is efficiency. An analysis of the efficiency is carried out in Table 2.1 that shows the semiconductor loss in the matrix converter compared back-to-back converters. The analysis demonstrates that the MC has lower switching loss and larger conduction loses than the back-to-back converter. Back-to-back converters are hard commutated, but with proper selection of bi-directional switches and commutation strategy MCs can be semi-soft commutated [20] or semi-natural commutated [21].

It is necessary to place filter capacitors at the input of the MCs to draw sinusoidal input currents. To avoid a short circuit of the impressed input voltages, a simultaneous connection of two input phases to the same output phase must be avoided. On the other hand, due to the load currents, one output phase must, be connected to one input phase. It is also permissible to connect all outputs to the same input.

	Back-to-back Converter	Conventional Matrix Converter
Commutation	Hard Switch	Semi-Soft Switch
Switch Voltage	1x	$(2/\pi)$x
Switch Current	1x	$(2/\sqrt{3})$x
# Switching	4x	8x
Switch Losses	4x	2.94x
Semiconductors in current path	4x	4x
Conduction Losses	4x	4.61x

Table 2.1 Comparison of the back-to-back converters and conventional MCs [36].

2.1.1 Direct Matrix Converters

Each of the input phases of the conventional, direct MC, can be directly connected with each output phase. It can therefore be represented as a switching matrix. A four-quadrant switch can be implemented by a regular power switch with anti-parallel freewheeling diodes as the input stage of the MC as shown on Fig. 2.2. A functional representation of the direct MC is depicted in Fig. 2.3. With respect to the conduction losses, an even better solution is to use an anti-parallel connection of RB-IGBTs [22]-[24].

Full bridge matrix converter (for open motor winding) was presented in [25]-[27] which is suitable for variable speed AC drives, because it generates no sub-harmonic components in the output voltage and hence the output frequency is limited.

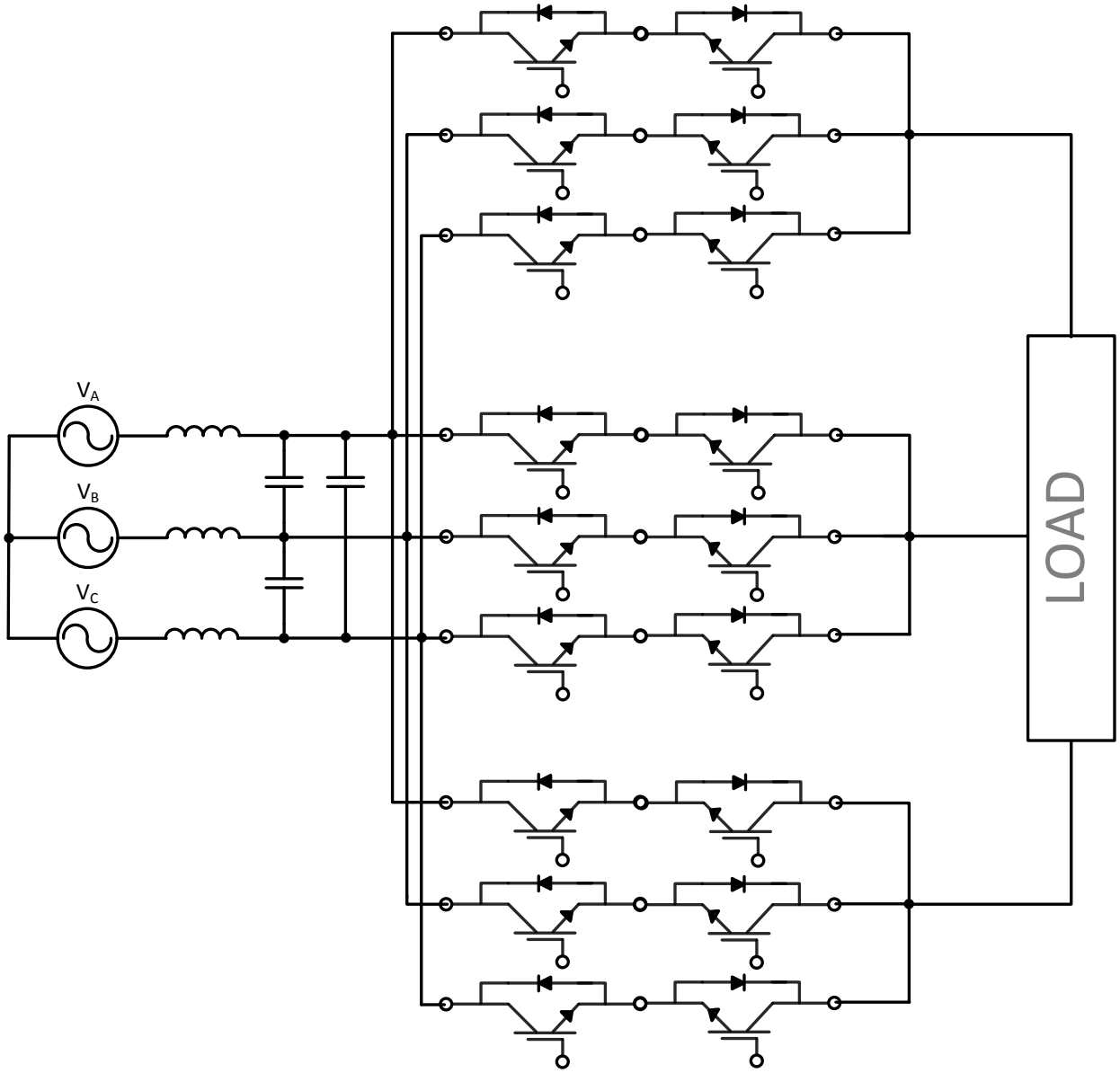


Fig. 2.2 Direct matrix converter.

As there is direct connection with voltage sources, the input phase shall never be shorted. If the switches cause a short circuit between the input voltage sources, a large current flows through the switches and damages the phase in which the short circuit occurs. Also, due to the inductive nature of typical loads, the output terminals must not be open-circuited. If any output terminal is open-circuited, the voltage across the inductor (and consequently across the switches)

is infinite and switches will be damaged due to the over-voltage. Switches for each output phase must be controlled based on the following expression:

$$S_{jA} + S_{jB} + S_{jC} = 1, \quad j \in \{a, b, c\} \tag{2.1}$$

$$\text{where} \quad S_{jk} \begin{cases} 1 & closed \\ 0 & open \end{cases}, j \in \{a, b, c\}, \; k \in \{A, B, C\} \tag{2.2}$$

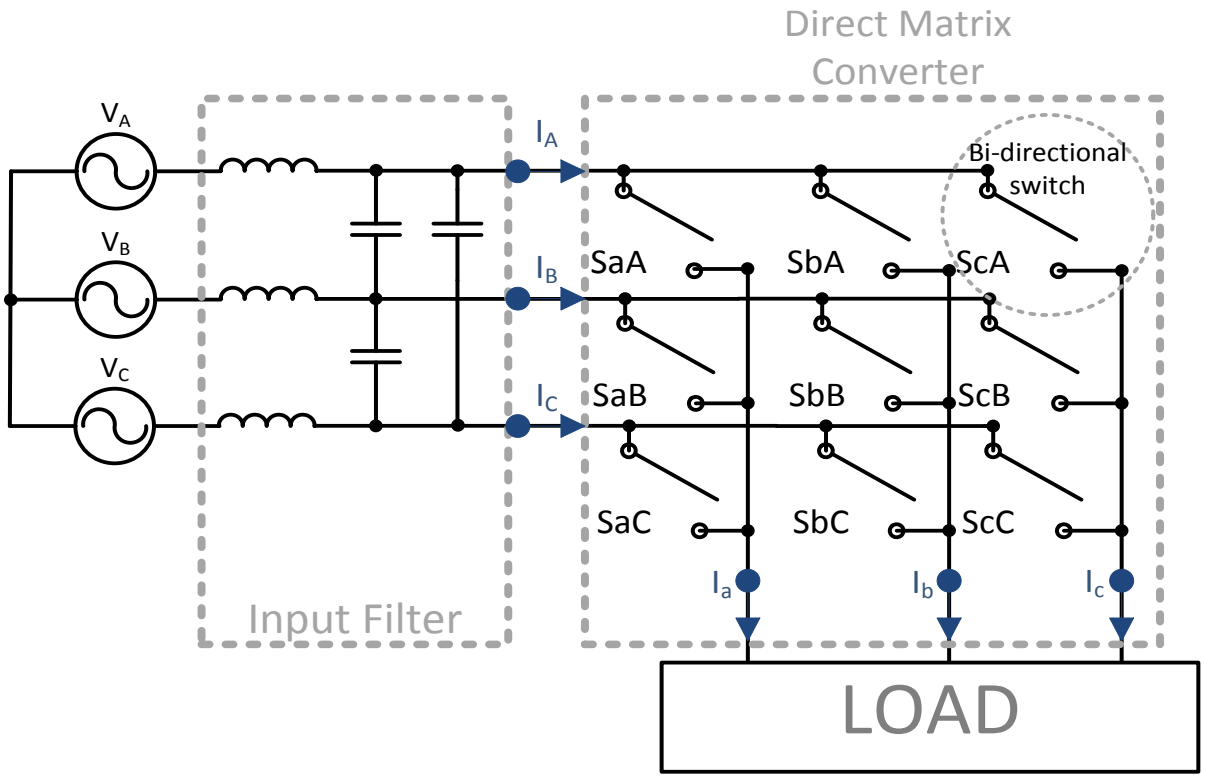


Fig. 2.3 Connection diagram of the direct matrix converter.

Power switches in the converter are divided into two groups. There are 27 allowable converter states including active states and zero states. Instantaneous values of the output voltages and the input currents produced by each switching combination can be determined using

the instantaneous transfer matrices, where T_{LL} is the instantaneous input phase to output line-to-line transfer matrix and T_{ph} is the instantaneous input phase to output phase matrix:

$$T_{LL} = \begin{bmatrix} S_{aA} - S_{bA} & S_{aB} - S_{bB} & S_{aC} - S_{bC} \\ S_{bA} - S_{cA} & S_{bB} - S_{cB} & S_{bC} - S_{cC} \\ S_{cA} - S_{aA} & S_{cB} - S_{aB} & S_{cC} - S_{aC} \end{bmatrix},\ T_{ph} = \begin{bmatrix} S_{aA} & S_{aB} & S_{aC} \\ S_{bA} & S_{bB} & S_{bC} \\ S_{cA} & S_{cB} & S_{cC} \end{bmatrix} \tag{2.3}$$

From the line to line transfer matrix the instantaneous output voltages, V_{LL} and input phase currents, i_{ph} can be determined:

$$V_{LL} = \begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = T_{LL} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = T_{LL} V_i\ ,\quad i_{ph} = \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = T_{LL}^T \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} \tag{2.4}$$

To generate balanced and sinusoidal input and output waveforms with variable input displacement angle, matrix converters are controlled using modulation techniques. Over each switching period, the modulation strategy controls duty cycles of the switches so that the input voltages and output currents are applied to the output and input terminals, respectively, that generates reference voltages and currents.

$$0 \le m_{jk} = \frac{t_{jk}}{T_S} \le 1,\ j \in \{a, b, c\},\ k \in \{A, B, C\} \tag{2.5}$$

where m_{jk} and t_{jk} denote the duty cycle and on-time of switch S_{jk}, respectively, and T_S is the switching period. Then,

$$\begin{bmatrix} v(t)_{o,a} \\ v(t)_{o,b} \\ v(t)_{o,c} \end{bmatrix} = \begin{bmatrix} m(t)_{aA} & m(t)_{aB} & m(t)_{aC} \\ m(t)_{bA} & m(t)_{bB} & m(t)_{bC} \\ m(t)_{cA} & m(t)_{cB} & m(t)_{cC} \end{bmatrix} \begin{bmatrix} v(t)_{in,A} \\ v(t)_{in,B} \\ v(t)_{in,C} \end{bmatrix} \tag{2.6}$$

$$\begin{bmatrix} i(t)_{in,A} \\ i(t)_{in,B} \\ i(t)_{in,C} \end{bmatrix} = \begin{bmatrix} m(t)_{aA} & m(t)_{aB} & m(t)_{aC} \\ m(t)_{bA} & m(t)_{bB} & m(t)_{bC} \\ m(t)_{cA} & m(t)_{cB} & m(t)_{cC} \end{bmatrix} . \begin{bmatrix} i(t)_{o,a} \\ i(t)_{o,b} \\ i(t)_{o,c} \end{bmatrix} \tag{2.7}$$

For balanced input lines,

$$\begin{bmatrix} m(t)_{aA} & m(t)_{aB} & m(t)_{aC} \\ m(t)_{bA} & m(t)_{bB} & m(t)_{bC} \\ m(t)_{cA} & m(t)_{cB} & m(t)_{cC} \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \tag{2.8}$$

while $\frac{V_o}{V_{in}} \leq \frac{\sqrt{3}}{2}$;

$$\begin{bmatrix} v(t)_{o,a} \\ v(t)_{o,b} \\ v(t)_{o,c} \end{bmatrix} = \begin{bmatrix} V_o \cos(w_o t + \theta_o) \\ V_o \cos\left(w_o t + \theta_o - \frac{2\pi}{3}\right) \\ V_o \cos\left(w_o t + \theta_o + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2.9}$$

$$\begin{bmatrix} v(t)_{in,A} \\ v(t)_{in,B} \\ v(t)_{in,C} \end{bmatrix} = \begin{bmatrix} V_{in} \cos(w_{in} t) \\ V_{in} \cos\left(w_{in} t - \frac{2\pi}{3}\right) \\ V_{in} \cos\left(w_{in} t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2.10}$$

$$\begin{bmatrix} i(t)_{in,A} \\ i(t)_{in,B} \\ i(t)_{in,C} \end{bmatrix} = \begin{bmatrix} I_{in} \cos(w_{in} t + \varphi_{in}) \\ I_{in} \cos\left(w_{in} t + \varphi_{in} - \frac{2\pi}{3}\right) \\ I_{in} \cos\left(w_{in} t + \varphi_{in} + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2.11}$$

$$\begin{bmatrix} i(t)_{o,a} \\ i(t)_{o,b} \\ i(t)_{o,c} \end{bmatrix} = \begin{bmatrix} I_o \cos(w_o t + \theta_o + \varphi_o) \\ I_o \cos\left(w_o t + \theta_o + \varphi_o - \frac{2\pi}{3}\right) \\ I_o \cos\left(w_o t + \theta_o + \varphi_o + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2.12}$$

where, V_o is the output voltage, V_{in} is the input voltage, θ_o is the output reference angle, w_{in} is the input angular frequency, w_o is the output angular frequency, φ_{in} is the input displacement angle and φ_o is the output displacement angle. To obtain the maximum voltage transfer ratio, third harmonic components of input and output signals are injected into the output voltages and the output voltage becomes as in Eq. (2.13) and the extended voltage transfer ratio is in Eq. (2.14):

$$\begin{bmatrix} v(t)_{o,a} \\ v(t)_{o,b} \\ v(t)_{o,c} \end{bmatrix} = V_o \begin{bmatrix} \cos(w_o t + \theta_o) \\ \cos\left(w_o t + \theta_o - \frac{2\pi}{3}\right) \\ \cos\left(w_o t + \theta_o + \frac{2\pi}{3}\right) \end{bmatrix} + \frac{V_{in}}{4} \begin{bmatrix} \cos(3w_{in} t) \\ \cos(3w_{in} t) \\ \cos(3w_{in} t) \end{bmatrix} - \frac{V_o}{6} \begin{bmatrix} \cos(3w_o t + 3\theta_o) \\ \cos(3w_o t + 3\theta_o) \\ \cos(3w_o t + 3\theta_o) \end{bmatrix} \quad (2.13)$$

$$\begin{bmatrix} v(t)_{o,a} \\ v(t)_{o,b} \\ v(t)_{o,c} \end{bmatrix} = V_o \begin{bmatrix} \cos(w_o t + \theta_o) \\ \cos\left(w_o t + \theta_o - \frac{2\pi}{3}\right) \\ \cos\left(w_o t + \theta_o + \frac{2\pi}{3}\right) \end{bmatrix} + \frac{V_o}{2\sqrt{3}} \begin{bmatrix} \cos(3w_{in} t) \\ \cos(3w_{in} t) \\ \cos(3w_{in} t) \end{bmatrix} - \frac{V_o}{6} \begin{bmatrix} \cos(3w_o t + 3\theta_o) \\ \cos(3w_o t + 3\theta_o) \\ \cos(3w_o t + 3\theta_o) \end{bmatrix} \quad (2.14)$$

The solution of the matrix of the low-frequency modulation function is

$$[m(t)] = \frac{1}{3}[I] + [X] + [Y] + [Z] \quad (2.15)$$

where,

$$[I] = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \quad (2.16)$$

$$[\mathrm{X}] = \frac{\beta_1}{3} \begin{bmatrix} m_+(1) & m_+(2) & m_+(3) \\ m_+(2) & m_+(3) & m_+(1) \\ m_+(3) & m_+(1) & m_+(2) \end{bmatrix} + \frac{\beta_2}{3} \begin{bmatrix} m_-(1) & m_-(2) & m_-(3) \\ m_-(2) & m_-(3) & m_-(1) \\ m_-(3) & m_-(1) & m_-(2) \end{bmatrix} \quad (2.17)$$

$$[\mathrm{Y}] = \frac{\gamma_1}{3} \begin{bmatrix} n_+(1) & n_+(2) & n_+(3) \\ n_+(2) & n_+(3) & n_+(1) \\ n_+(3) & n_+(1) & n_+(2) \end{bmatrix} + \frac{\gamma_2}{3} \begin{bmatrix} n_-(1) & n_-(2) & n_-(3) \\ n_-(2) & n_-(3) & n_-(1) \\ n_-(3) & n_-(1) & n_-(2) \end{bmatrix} \quad (2.18)$$

$$[\mathrm{Z}] = \frac{\delta_1}{3} \begin{bmatrix} q_+(1) & q_+(2) & q_+(3) \\ q_+(2) & q_+(3) & q_+(1) \\ q_+(3) & q_+(1) & q_+(2) \end{bmatrix} + \frac{\delta_2}{3} \begin{bmatrix} q_-(1) & q_-(2) & q_-(3) \\ q_-(2) & q_-(3) & q_-(1) \\ q_-(3) & q_-(1) & q_-(2) \end{bmatrix} \quad (2.19)$$

where,

$$\mathrm{m}_+(\mathrm{i}) = \cos[(w_o + w_{in})t + \theta_o - (i-1)\frac{2\pi}{3}] \quad (2.20)$$

$$\mathrm{m}_-(\mathrm{i}) = \cos[(w_o - w_{in})t + \theta_o - (i-1)\frac{2\pi}{3}] \quad (2.21)$$

$$\beta_1 = \frac{V_o}{V_{in}}\left[1 - \frac{\tan(\varphi_{in})}{\tan(\varphi_{in})}\right] \tag{2.22}$$

$$\beta_2 = \frac{V_o}{V_{in}}\left[1 + \frac{\tan(\varphi_{in})}{\tan(\varphi_{in})}\right] \tag{2.23}$$

$$\mathrm{n}_+(\mathrm{i}) = \cos[4w_{in}t - (i-1)\frac{2\pi}{3}] \tag{2.24}$$

$$\mathrm{n}_-(\mathrm{i}) = \cos[2w_{in}t - (i-1)\frac{2\pi}{3}] \tag{2.25}$$

$$\gamma_1 + \gamma_2 = \frac{1}{\sqrt{3}}\frac{V_o}{V_{in}} \tag{2.26}$$

$$\mathrm{q}_+(\mathrm{i}) = \cos[(3w_o + w_{in})t + 3\theta_o - (i-1)\frac{2\pi}{3}] \tag{2.27}$$

$$\mathrm{q}_-(\mathrm{i}) = \cos[(3w_o - w_{in})t + 3\theta_o - (i-1)\frac{2\pi}{3}] \tag{2.28}$$

$$\delta_1 + \delta_2 = \frac{1}{3}\frac{V_o}{V_{in}} \tag{2.29}$$

The coefficients γ and δ not violating the "0.866" maximum voltage transfer ratio are

$$\gamma_1 = \frac{-1}{6\sqrt{3}}\frac{V_o}{V_{in}}, \gamma_2 = \frac{7}{6\sqrt{3}}\frac{V_o}{V_{in}}, \ \delta_1 = \delta_2 = \frac{-1}{6}\frac{V_o}{V_{in}} \tag{2.30}$$

2.1.2 Indirect Matrix Converters

An alternative MC exists as the indirect matrix converter (IMC). The IMC has two separate stages, the front end and the back end, but without any energy storage in the intermediate link. The analysis of MC circuits is based on the basic functionality and modulation of the ac–dc converter with impressed output current and the dc–ac converter with impressed input voltage. The IMC is based on the current source rectifier and voltage source inverter topologies [18].

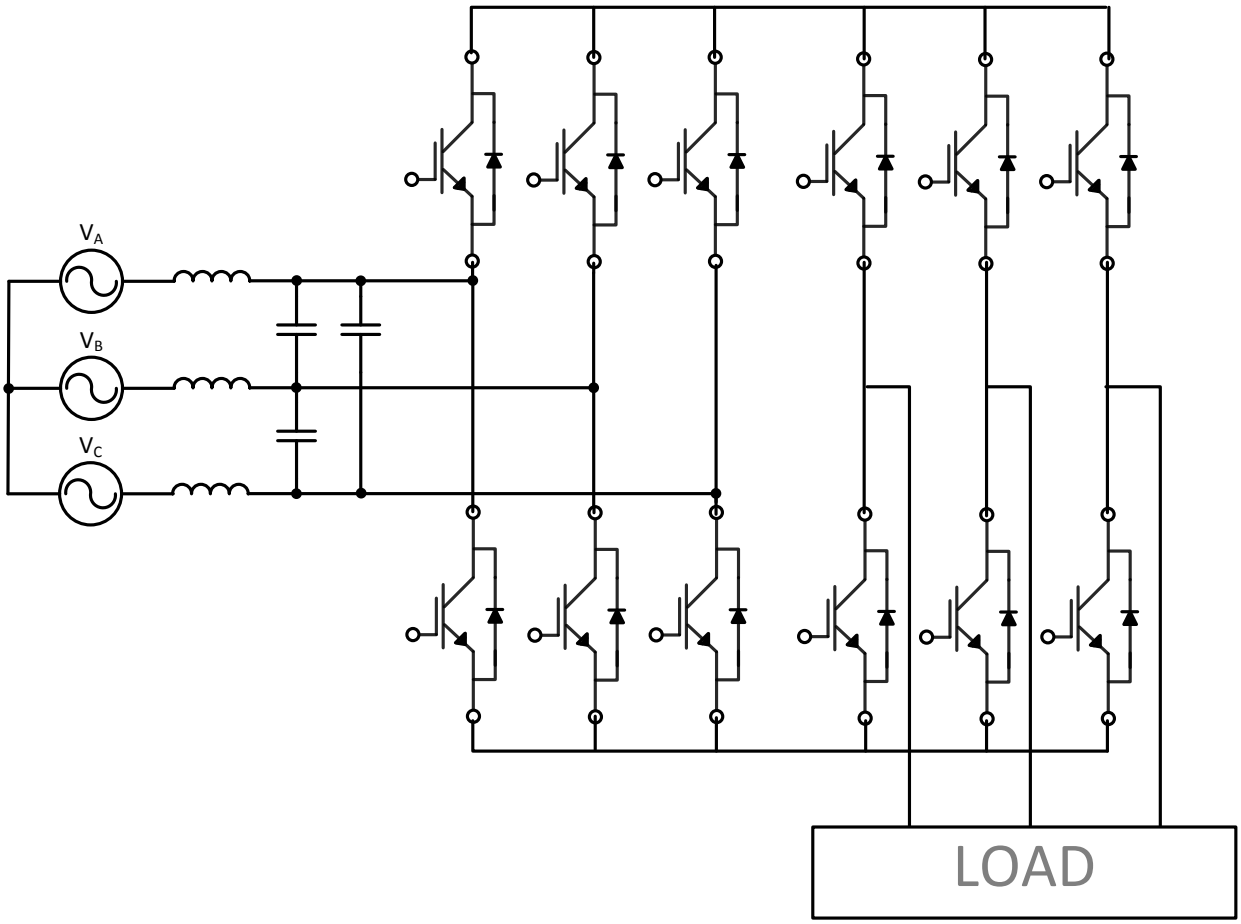


Fig. 2.4 Indirect matrix converter ($\pi/6$ displacement angle).

In order to derive a MC topology from the ac–ac converter with a dc-link capacitor, Fig.2.4 is considered first as the indirect ac–ac converter with an intermediate link where the energy-storage dc-link capacitor is omitted. Such a converter system was suggested in [28] and investigated in more detail in [29]–[31]. The input filter capacitors are required to provide impressed voltages at the input due to the impressed load currents at the output. The input stage of the converter system represents a synchronous three-phase rectifier. Its conductive state is directly defined by the mains voltage, and it cannot be influenced through the control. The load line current segments in the link, which are generated by the PWM output stage, are supplied by the input stage through the diodes with the highest instantaneous mains line-to-line voltage across them. This type of matrix converters allows only $\pi/6$ degrees of displacement angle [18].

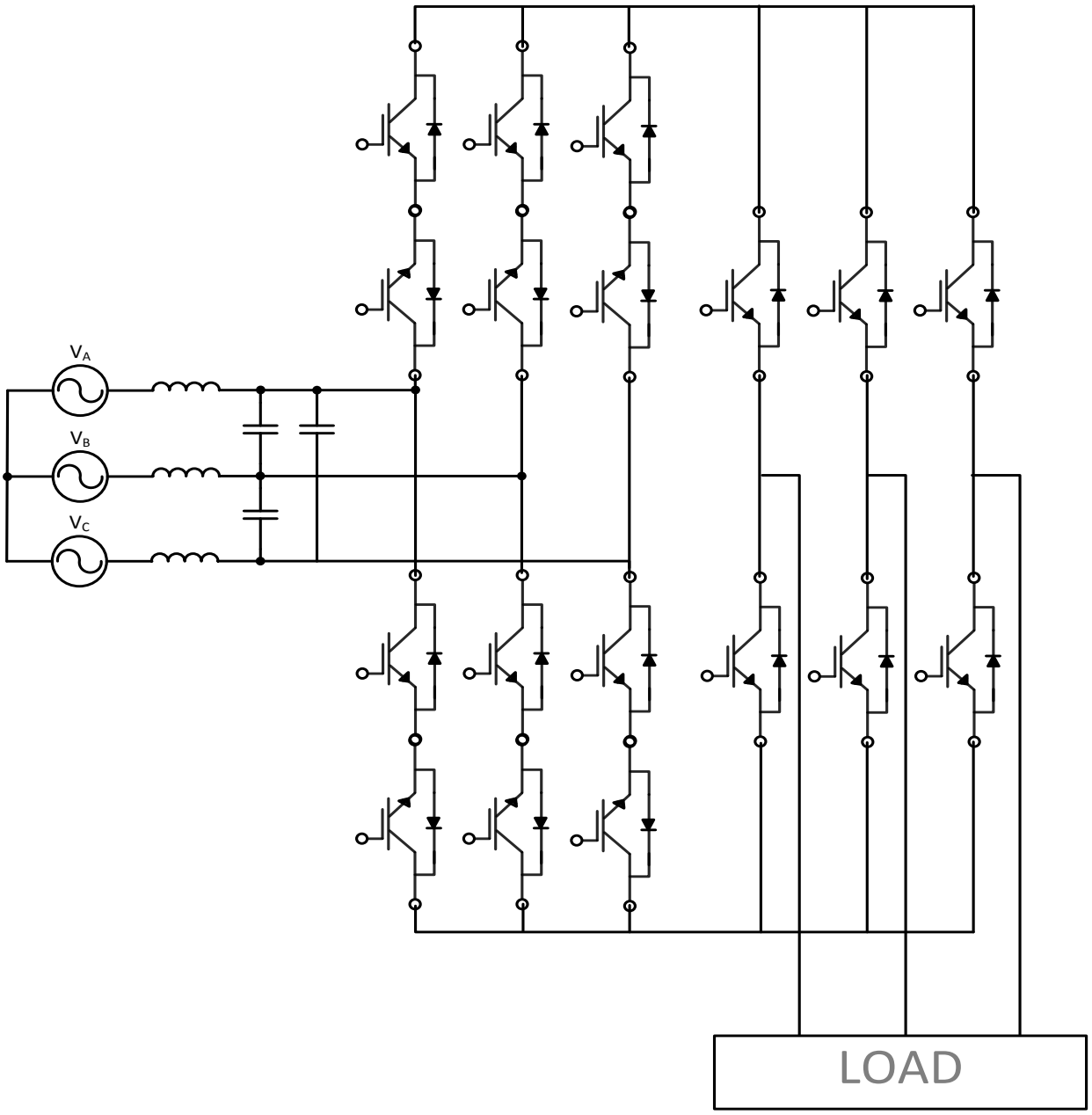


Fig. 2.5 Indirect matrix converter (full range displacement angle).

The further presented indirect matrix converters provide a full range of the displacement angle, shown in Fig.2.5. It is essential to place a power switch in series with each diode, to maintain the front end conductivity. However, when this series switch is blocking, a forward voltage can occur, which must not appear across the anti-parallel switches and which is mainly desirable for the reverse power flow. The input stage now consists of two anti-parallel connected

PWM rectifier stages on the front end followed by traditional PWM inverter on the back end. Fig.2.6 shows indirect matrix converter block diagram.

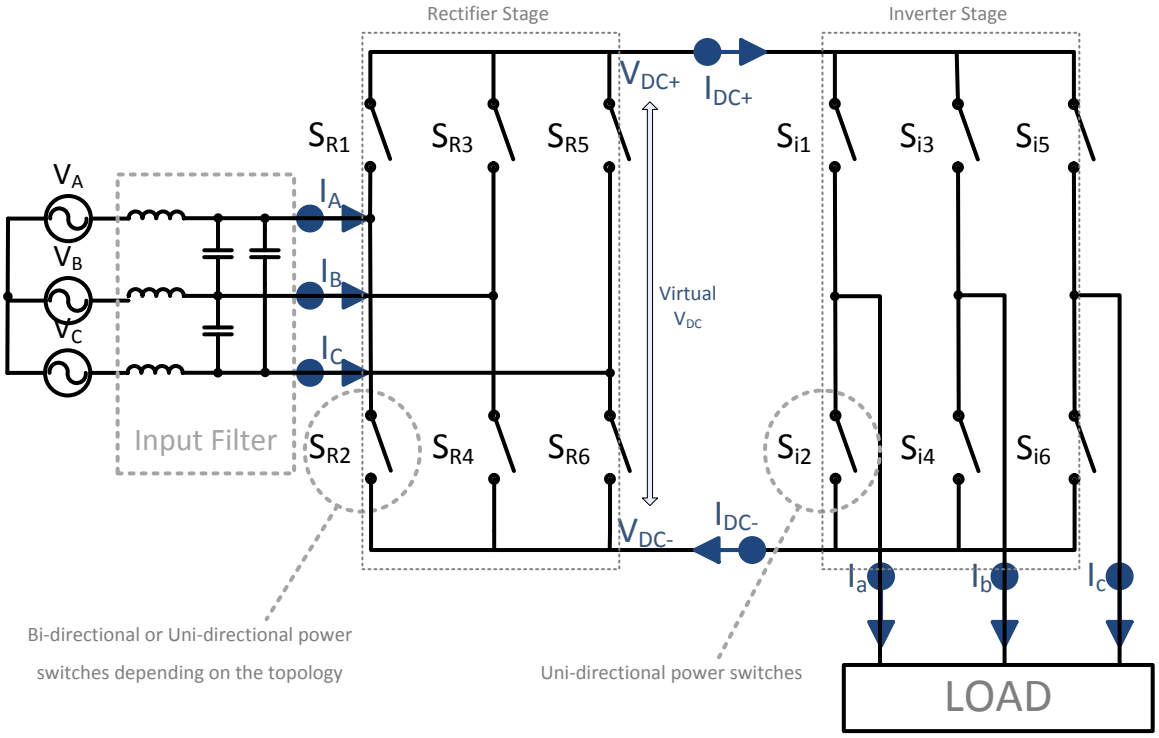


Fig. 2.6 Circuit diagram of the indirect matrix converter.

As in direct matrix converters, short circuit of two main phases would result from simultaneously turning on two power switches of the upper or lower bridge legs and must therefore be avoided. The fundamental of IMC is based on decoupling the control of the rectifier and inverter stages. The instantaneous input phase to output phase matrix, T_{ph}, from Eq. 2.3 can be divided into rectifier and inverter transfer functions:

$$T_{ph} = I * R \tag{2.31}$$

$$\begin{bmatrix} S_{aA} & S_{aB} & S_{aC} \\ S_{bA} & S_{bB} & S_{bC} \\ S_{cA} & S_{cB} & S_{cC} \end{bmatrix} = \begin{bmatrix} S_{i1} & S_{i2} \\ S_{i3} & S_{i4} \\ S_{i5} & S_{i6} \end{bmatrix} * \begin{bmatrix} S_{R1} & S_{R3} & S_{R5} \\ S_{R2} & S_{R4} & S_{R6} \end{bmatrix} \tag{2.32}$$

where the matrix I is the inverter transfer function and the matrix R is the rectifier transfer function. The resultant transfer function allows combining current source PWM rectifier with voltage source PWM inverter without any energy storage components between the positive and negative rails.

By combining Eq. (2.4) and Eq. (2.32), we obtain

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \begin{bmatrix} S_{i1} & S_{i2} \\ S_{i3} & S_{i4} \\ S_{i5} & S_{i6} \end{bmatrix} * \begin{bmatrix} S_{R1} & S_{R3} & S_{R5} \\ S_{R2} & S_{R4} & S_{R6} \end{bmatrix} * \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{2.33}$$

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \begin{bmatrix} (S_{i1} * S_{R1} + S_{i2} * S_{R2}) & (S_{i1} * S_{R3} + S_{i2} * S_{R4}) & (S_{i1} * S_{R5} + S_{i2} * S_{R6}) \\ (S_{i3} * S_{R1} + S_{i4} * S_{R2}) & (S_{i3} * S_{R3} + S_{i4} * S_{R4}) & (S_{i3} * S_{R5} + S_{i4} * S_{R6}) \\ (S_{i5} * S_{R1} + S_{i6} * S_{R2}) & (S_{i5} * S_{R3} + S_{i6} * S_{R4}) & (S_{i5} * S_{R5} + S_{i6} * S_{R6}) \end{bmatrix} * \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{2.34}$$

Eq. (2.34) shows that the output phases represent the product and sum of the input phases through inverter switches and rectifier switches. If the equivalent circuit is seen from the inverter's output phase a, two switches S_{i1} and S_{i2} of phase a half bridge are directly connected to input phases a, b and c through six rectifier switches $S_{R[1,6]}$. Fig.2.7 shows the transformation of an indirect matrix converter into the direct matrix converter by realizing Eq. (2.34).

In [32] sparse matrix-equivalent three-phase ac-dc-ac converter topologies are developed based on the structure of an IMC. The converter topologies exhibit a reduced number of power transistors compared to the CMC or IMC and are therefore designated as (a) sparse matrix converter (SMC), shown in Fig.2.8, (b) very sparse matrix converter (VSMC), shown in Fig.2.9, and (c) ultra sparse matrix converter (USMC), shown in Fig.2.10. SMC employs 15 IGBTs, compared to 18 IGBTs of the IMC, and therefore the converter topology is called a sparse converter. The functional equality of the CMC/IMC and SMC is proven in [33], where the CMC

and SMC line-to-line output voltages and input phase currents resulting for the different switching state combinations are composed.

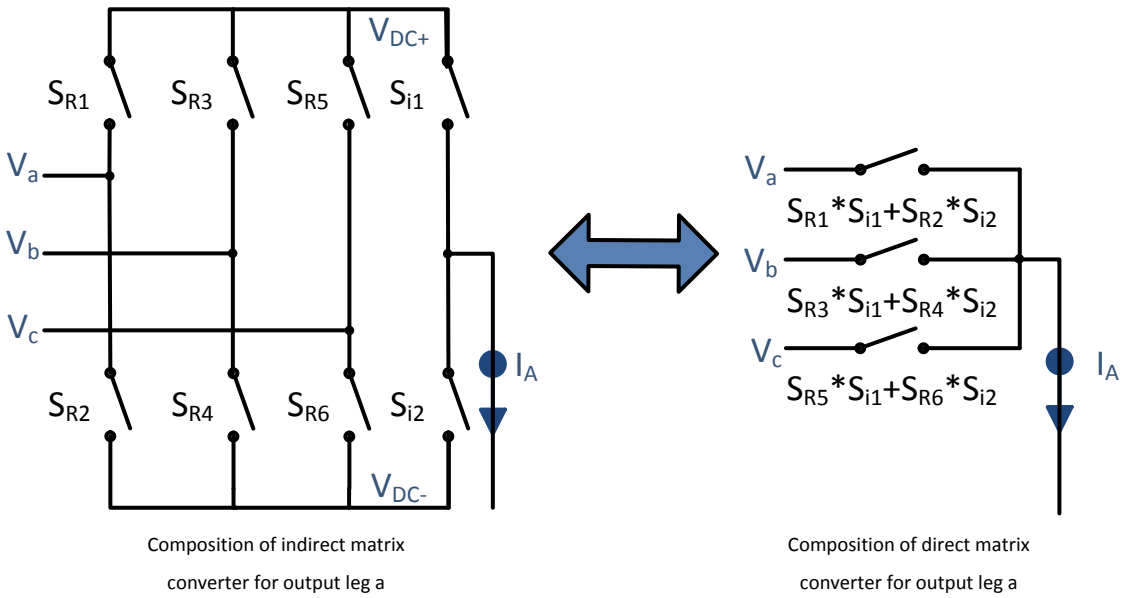


Fig. 2.7 Indirect matrix converter to direct matrix converter transformation.

If simple functionality of a unidirectional buck-type PWM rectifier system, as described in [34] and [35], is desired, then SMC can be reduced by omitting the power switches in each bridge leg. This causes blocking the reverse flow of the dc-link current and restricts the circuit operation to a unidirectional power flow. Controllability of the phase displacement of input voltage and input current fundamental is also limited, while the phase displacement of load current and load voltage fundamental is not allowed to exceed $\pi/6$. Down to the lowest number of power switches (nine IGBTs), this circuit topology is called the USMC. Converters that are presented in Chapters 4 and 5 are based on the USMC type converters.

Since the USMC has a unidirectional power flow, the load must not be allowed to feed energy back into the dc-link since there are no energy storage capacitors, and excessive dc-link voltages would be generated. Therefore, an addition of a clamp circuit to the USMC is needed. The clamp can be as simple as a series connection of a diode and capacitor across the dc-link

[36], [37] and/or as a braking resistor with a series connected controllable switch, which provides braking capability in case of a mains failure [32].

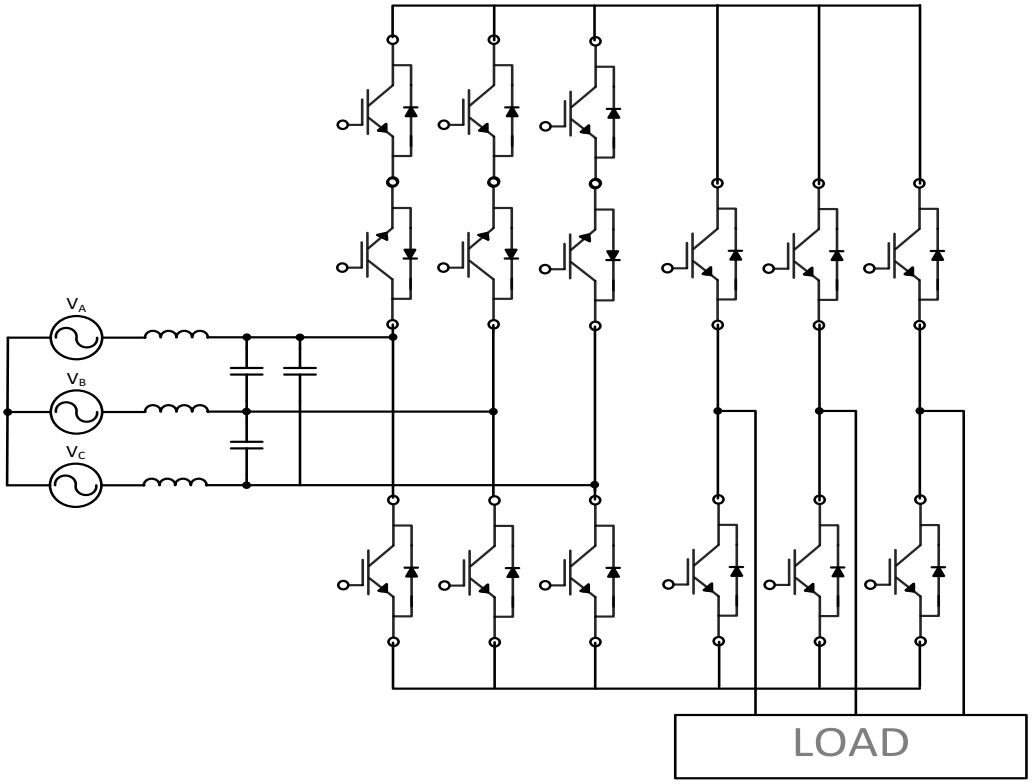


Fig. 2.8 Sparse matrix converter.

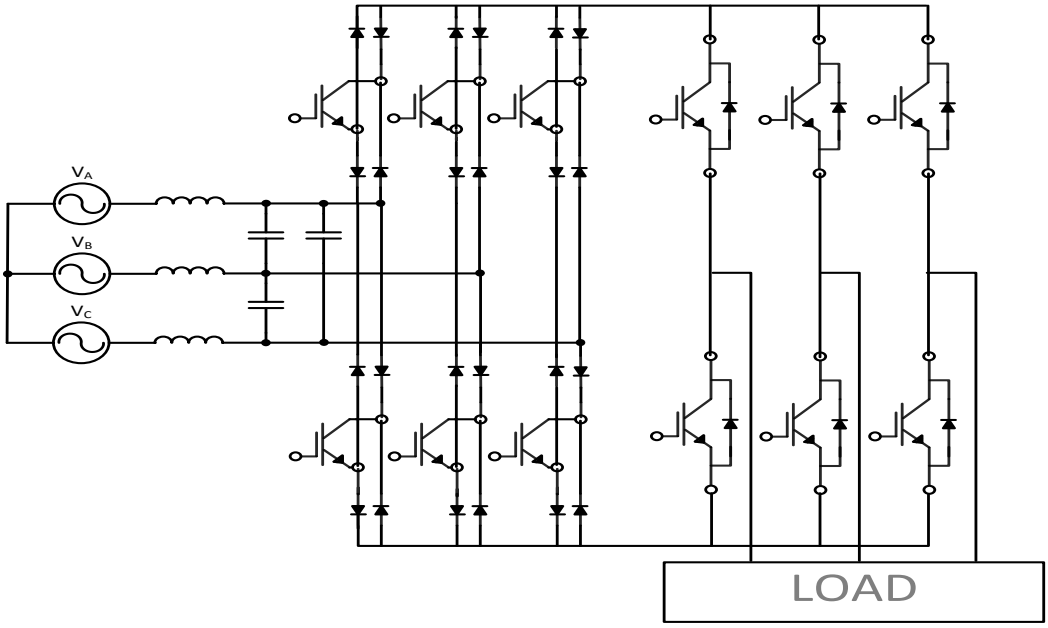


Fig. 2.9 Very sparse matrix converter.

The front-end rectifier, whose one leg is depicted in Fig.2.11, draws sinusoidal input currents and controls the input displacement angle. For a unity input power factor, the reference input phase current vector is aligned with that of the input phase voltage. For example, (S_{ap}, S_{cn}) indicates that the input phase "a" is connected to the positive (top) rail "p" and phase "c" is connected to the negative (bottom) rail "n".

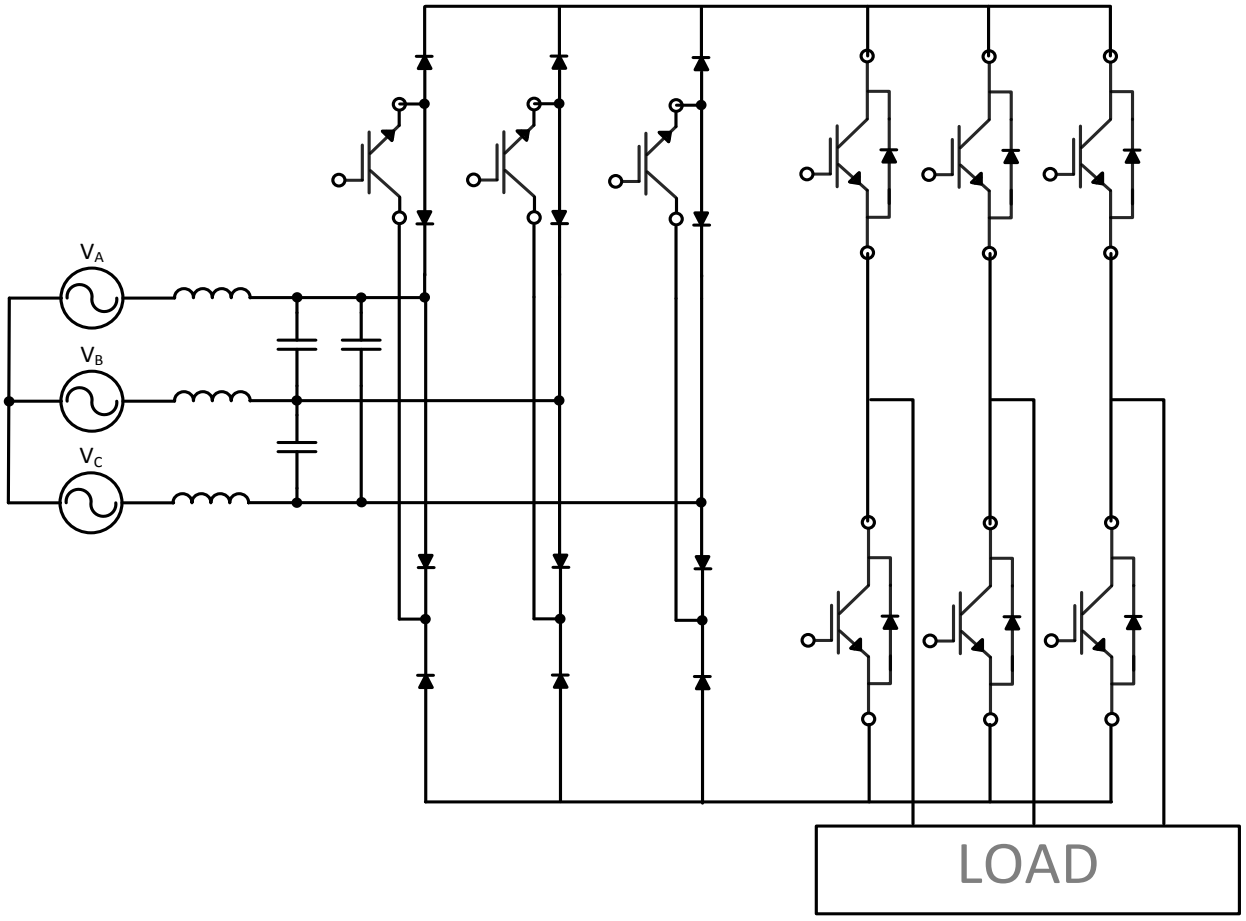


Fig. 2.10 Ultra sparse matrix converter.

To avoid short circuit of a dc link voltage in a given switching period of the rectifier input stage, the commutation of the inverter output stage must be performed in a way identical to the commutation of a traditional IMC. There, a dead time between the turn-on of the power switches of a bridge leg must be implemented. Control design must ensure that there is no bidirectional connection between any two input lines, i.e., no short-circuiting of an input line-to-

line voltage terminal. Additionally a current path must be continuously provided. Therefore multistep commutation schemes are required, using voltage independent and current independent commutation as known for the CMC [38].

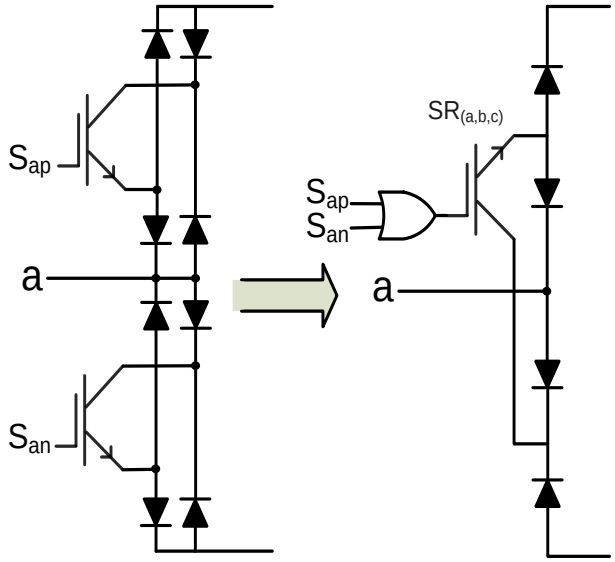


Fig. 2.11 Legs of the front-end rectifier. Left: sparse matrix converter, right: ultra sparse matrix converter.

Multi-step commutation is demanding on the microprocessor, but on the other hand indirect matrix converters can provide a degree of control freedom that is not available in the CMC. Complex commutation problems can be avoided. For instance, as proposed in [39], the inverter stage could be switched into a free-wheeling state and then the rectifier stage could commutate with zero dc-link current. This has the additional benefit of a reduction of switching losses of the input stage. By employing the zero dc-link current commutation strategy the topology of the IMC can be reduced to that of the very sparse matrix converter [32].

The maximum voltage gain of MCs is limited to 0.866 due to its buck conversion characteristic. To overcome this limitation, various modulation techniques, such as over-modulation methods, have been investigated for improvement in the output voltage quality and

voltage transfer ratio. However, these methods tend to compromise system input or output operating performance [41]-[43]. To avoid such deterioration, a hybrid direct power converter that incorporates an auxiliary voltage source in the DC-link of the IMC was presented in [44]. Auxiliary power devices can support the unity voltage transfer ratio of the IMC. However, these additional switches increase the complexity of control and size and weight of the converter, which is a major disadvantage. A Z-source AC-DC matrix converter was studied in [45]. The Z-source provides a buck-boost conversion from the low DC battery voltage to an AC motor load, and exhibits good line-side current modulation. In [42] and [46] Z-source MC shown in Fig.2.12 was shown to boost the input voltage up to 2.35 times.

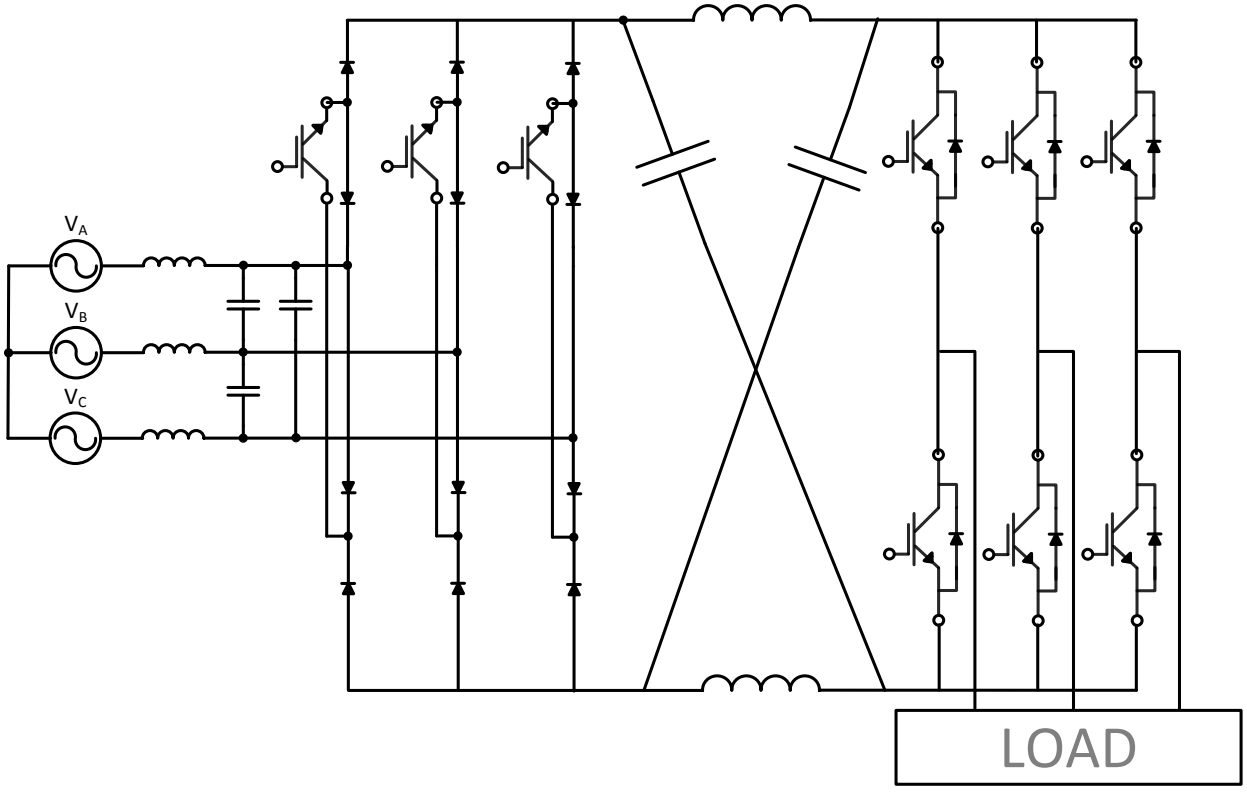


Fig. 2.12 Z source ultra sparse matrix converter.

Usually, the output stage of the IMC is a two-level PWM inverter. A three-level inverter can be employed at the back end of the MC, as shown in Fig.2.13, to reduce the switching

frequency harmonics of the output voltage. Such a topology, in which the center point for the output stage is provided by the star point of the input filter capacitors, was proposed in [47]. It enables formation of the output voltage by the phase and line-to-line input voltages. As the input stage of an SMC can be used, this topology was later designated as three-level SMC (USMC3).

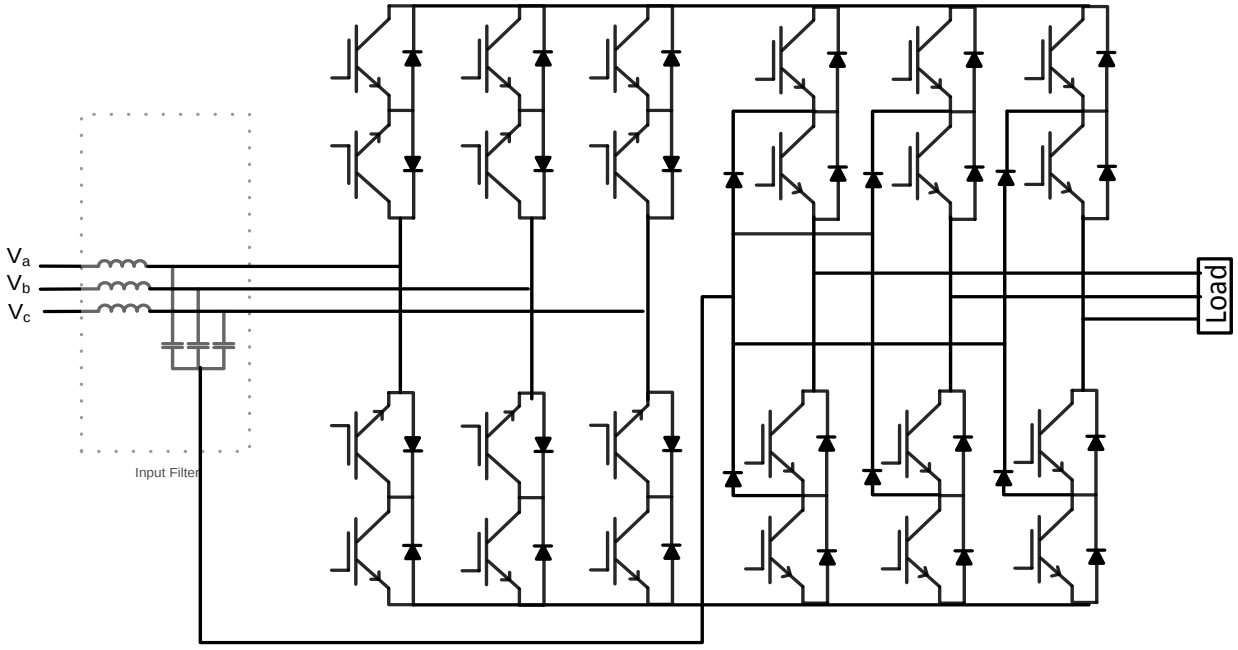


Fig. 2.13 IMC with a three-level PWM output stage.

The same functionality can be achieved with the topology shown in Fig.2.14, which has the advantage of having a reduced number of switches [48]. Instead of using additional diodes to generate the fifth voltage level, using these two extra switches to move the voltage on positive rail, neutral point (star cap center) and negative rail achieves the same attribute. It can thus be called a three level indirect matrix converter (IMC3).

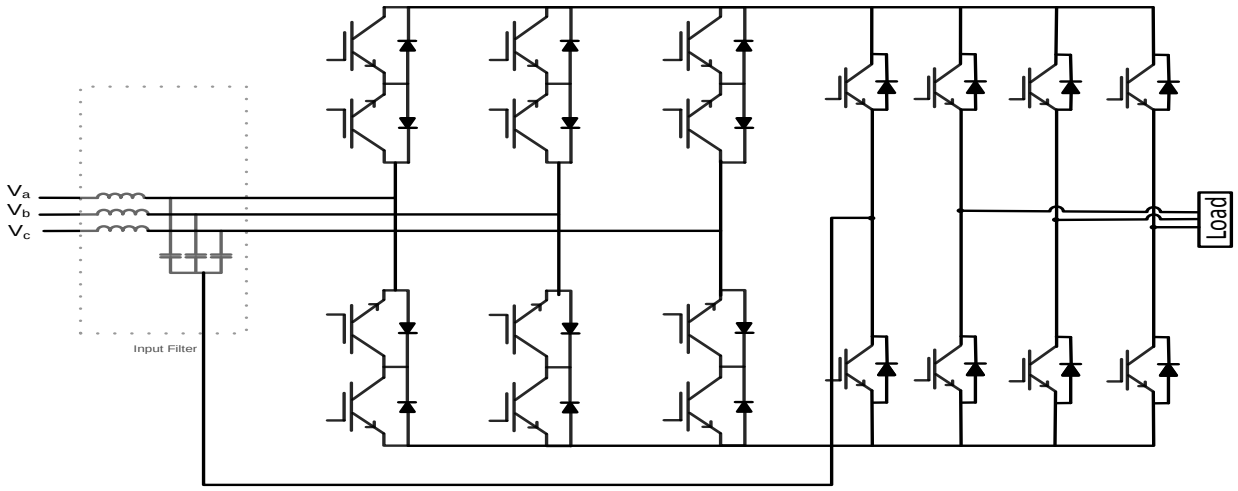


Fig. 2.14 IMC with additional single stage three-level PWM output stage.

Significant simplification of the indirect three-level MC circuits can be achieved by assuming the unidirectional power flow shown in Fig.2.15 [49]. The front end of this topology reveals the structure of a Vienna rectifier [50]. The main attribute of such converters is that the front end power switches are turning on and off only two times the fundamental frequency. This leads to high efficiency due to low switching losses in the corresponding power switches.

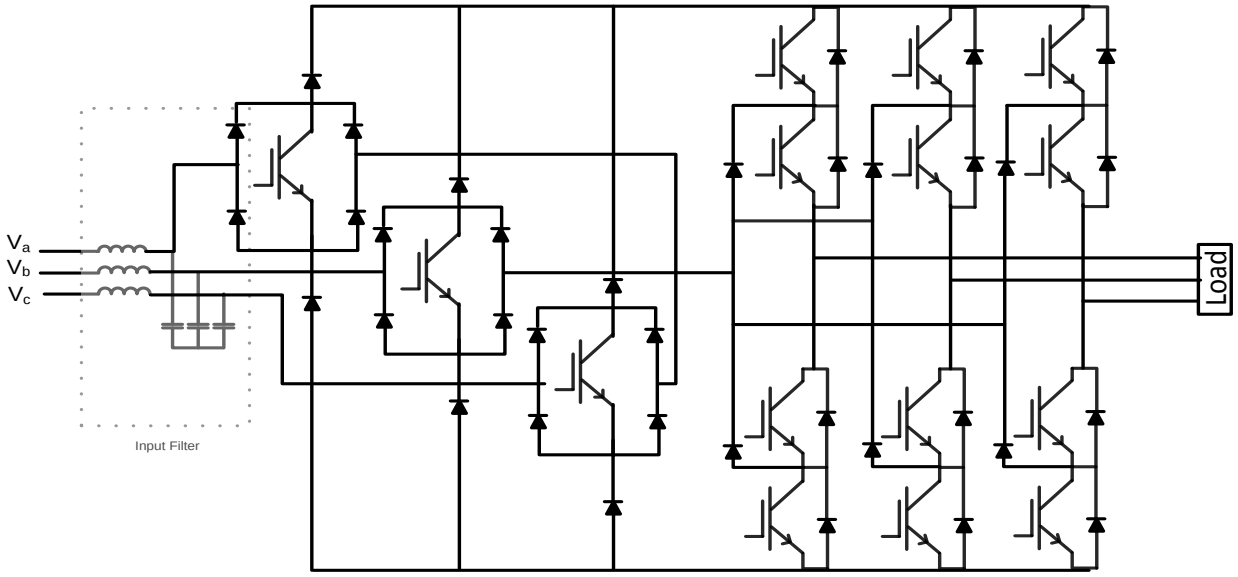


Fig. 2.15 Unidirectional IMC with a three-level PWM output stage.

There are other topologies related to matrix converters in the literature that can be considered as basic classes of MCs. Table 2.2 shows the number of transistors, diodes and gate driver sources are needed for such topologies. It is hard to tell which converter is better than the others, and the selection must be based on the specific application.

	CMC	IMC	SPMC	VSMC	USMC	ZSMC	SMC3	IMC3	USMC3
Transistors	18	18	15	12	9	9	24	20	15
Diodes	18	18	18	30	18	18	30	20	36
Gate drives	9	8	7	19	7	7	8	8	7

Table 2.2 Comparison of MC topologies.

2.2 Modulation Techniques for Matrix Converters

Venturini and Alesina in [51] provided the rigorous mathematical background and introduced the name “matrix converter,” elegantly describing how the low frequency behaviors of the voltages and currents are generated at the load and the input [52]. Fig.2.16 shows the summary of the popular modulation techniques of matrix converters. Besides those shown, there are many other application specific techniques, which can be found in [55]-[64].

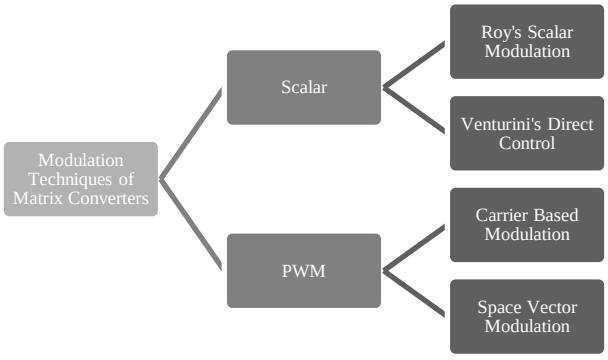


Fig. 2.16 Major specification of modulation techniques for matrix converters.

The first versatile modulation method is called direct control is also known as Venturini's modulation. Output voltages are formed from the fixed amplitude and fixed frequency input voltages. However, as a golden rule to matrix converters, output voltages have variable amplitude and variable frequency. Venturini's first technique had the voltage transfer ratio (VTR) of 0.5 only. He then proposed the third harmonic technique to reach the value of 0.866 [53].

A scalar method was proposed by Roy in the late 1980s. The main difference of the Roy's method from Venturini's is the scalar comparison of input voltages and the instantaneous value of output voltage. This technique is similar to Venturini's third harmonic insertion technique but fails at low switching frequencies. In both techniques, adjusting the power factor reduces the VTR.

Carrier based modulation method is commonly used in many applications and is based on the sinusoidal pulse width modulation (PWM). The high frequency carrier signal (triangle or sawtooth) with an offset voltage and fixed amplitude is compared with a sinusoidal reference signal. The amplitude of the reference signal specifies the modulation index and the frequency specifies the frequency of output voltages. The same process can be employed for either the three-phase or single-phase applications. In [54], a variable displacement angle for the power factor is applied to a carrier based method. The main drawback of this method is generation of high frequency reference sinusoidal and triangular waveforms in microprocessor based applications. Normally reference signals are generated in hardware and this brings extra cost, complexity and space issues.

Space vector modulation (SVM) is a very popular method for matrix converters. This method features full control of frequency, amplitude and phase angle of the output voltage, as well as a controllable phase angle displacement of the input line currents. This type of

modulation technique was first presented in [55] and has since acquired many extensions. The control method is based on rectification and inversion: the rectification stage forms the input sinusoidal currents and the inversion stage generates output voltages. The control method proposed in Chapter 4 is based on such cascaded SVM stages.

2.2.1 Space Vector Rectifier Control

Active and zero states of the rectifier are utilized in the space vector modulation. The control algorithm must result in input currents that are sinusoidal with a controllable displacement angle with respect to the input voltages. To get unity power factor, input voltage has to be synchronized with input currents. A virtual dc link is formed by the chopped input voltages. The input currents are represented as the virtual dc-link current, I_{DC}, multiplied by the switch states of the rectifier stage with a transfer function described by Eq. (2.32).

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} S_{R1} & S_{R2} \\ S_{R3} & S_{R4} \\ S_{R5} & S_{R6} \end{bmatrix} * \begin{bmatrix} I_{DC+} \\ I_{DC-} \end{bmatrix} \tag{2.34}$$

$$\begin{bmatrix} V_{DC+} \\ V_{DC-} \end{bmatrix} = \begin{bmatrix} S_{R1} & S_{R3} & S_{R5} \\ S_{R2} & S_{R4} & S_{R6} \end{bmatrix} * \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \tag{2.35}$$

Space vector modulation is based on transformation of the time-varying values of input currents and output voltages. The three-phase systems are transformed into two phase systems.

$$V_{out} = \frac{2}{3}(V_A + V_B e^{\frac{j2\pi}{3}} + V_C e^{j4\pi/3}) \tag{2.36}$$

$$I_{in} = \frac{2}{3}(I_a + I_b e^{\frac{j2\pi}{3}} + I_c e^{j4\pi/3}) \tag{2.37}$$

$$V_{in} = \frac{2}{3}(V_a + V_b e^{\frac{j2\pi}{3}} + V_c e^{j4\pi/3}) \tag{2.38}$$

$$I_{out} = \frac{2}{3}(I_A + I_B e^{\frac{j2\pi}{3}} + I_C e^{j4\pi/3}) \tag{2.39}$$

Only nine states are allowed to avoid the open circuit of the dc links. Six of these are active states and three are zero states. The nine combinations can be divided into active vectors $I_{[1,6]}$ and three zero vectors I_0. These discrete vectors can be associated with the dc link current value. For example, $I_{2,ac}$ can be derived as:

$$I_2 = \frac{2}{3}(I_a + I_b e^{\frac{j2\pi}{3}} + I_c e^{j4\pi/3}) \tag{2.40}$$

$$I_2 = \frac{2}{3}(I_{DC} + I_{DC} e^{j4\pi/3}) \tag{2.41}$$

$$I_2 = \frac{2}{\sqrt{3}} I_{DC} e^{j\pi/6}) \tag{2.42}$$

State	Vector	$\begin{bmatrix} S_{R1} & S_{R3} & S_{R5} \\ S_{R2} & S_{R4} & S_{R6} \end{bmatrix}^T$	I_a	I_b	I_c	$\lvert I_{in} \rvert$	$\angle I_{in}$	V_{out}	V_{DC}
Active	$I_{1,ab}$	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}^T$	I_{DC+}	I_{DC-}	0	$\frac{2}{\sqrt{3}} I_{DC}$	$\frac{-\pi}{6}$	$\frac{2}{\sqrt{3}} V_{ab}$	V_{ab}
Active	$I_{1,ac}$	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}^T$	I_{DC+}	0	I_{DC-}	$\frac{2}{\sqrt{3}} I_{DC}$	$\frac{-\pi}{6}$	$\frac{2}{\sqrt{3}} V_{ca}$	$-V_{ca}$
Active	$I_{1,bc}$	$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}^T$	0	I_{DC+}	I_{DC-}	$\frac{2}{\sqrt{3}} I_{DC}$	$\frac{\pi}{2}$	$\frac{2}{\sqrt{3}} V_{bc}$	V_{bc}
Active	$I_{1,ba}$	$\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix}^T$	I_{DC-}	I_{DC+}	0	$\frac{2}{\sqrt{3}} I_{DC}$	$\frac{5\pi}{6}$	$\frac{2}{\sqrt{3}} V_{ab}$	$-V_{ab}$
Active	$I_{1,ca}$	$\begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}^T$	I_{DC-}	0	I_{DC+}	$\frac{2}{\sqrt{3}} I_{DC}$	$\frac{-5\pi}{6}$	$\frac{2}{\sqrt{3}} V_{ca}$	V_{ca}
Active	$I_{1,cb}$	$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}^T$	0	I_{DC-}	I_{DC+}	$\frac{2}{\sqrt{3}} I_{DC}$	$\frac{-\pi}{2}$	$\frac{2}{\sqrt{3}} V_{bc}$	$-V_{bc}$
Zero	$I_{0,aa,bb.cc}$	$\begin{bmatrix} 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix}^T \begin{bmatrix} 0 & 1 & 0 \\ 0 & 1 & 0 \end{bmatrix}^T \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 1 \end{bmatrix}^T$					0	0	0

Table 2.3 Switching vector states for rectification stage.

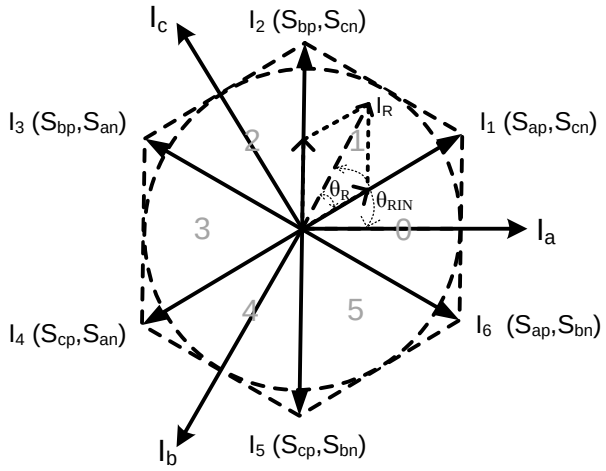


Fig. 2.17 Diagram of input-current space vectors.

Fig.2.17 shows the reference input space vector $I_R{}^*$ within the current switching hexagon. For simplicity the current switching vectors are referred to the input phase potentials connected to the dc bus. Only two switches are turned on simultaneously.For instance $I_6(S_{ap}, S_{bn})$ means that V_{dc+} is connected to input phase a and V_{dc-} is connected to input phase c.

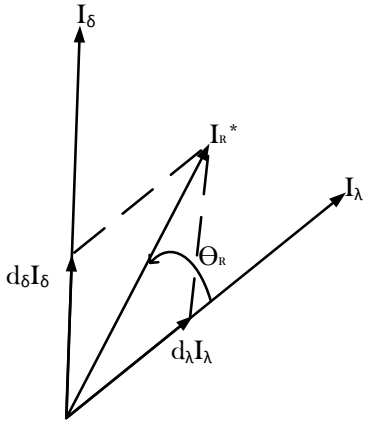


Fig. 2.18 Reference input current space vector with the adjacent vectors.

Location of the reference vector within one of the 60^o sectors defines the framing vectors I_λ and I_δ as seen Fig 2.18. For example, in Fig. 2.17 the current reference angle is in the first

sector. If the input currents are considered constant during the short switching intervals of T_s then the reference vector can be expressed as seen in Fig. 2.18:

$$I_R{}^* = I_\delta d_\delta + I_\lambda d_\lambda \tag{2.43}$$

The duration of the active vectors (I_δ, I_λ) determines the direction and the zero vector adjusts the amplitude of $I_R{}^*$. Angle $\theta_R$is the angle of the reference current space vector within the considered hexagon sector:

$$\theta_R = \theta_{RIN} - \frac{\pi}{3} N_{sector[0-5]} \tag{2.44}$$

where N_{sector} is a number indicating actual hexagon sector where its range is between 0 to 5. Then, the duty ratios of the active,d_λ, d_δ, and zero, d_{0R}, vectors are calculated as:

$$d_\lambda = \frac{T_\lambda}{T_s} = m_c \sin\left(\frac{\pi}{3} - \theta_R\right) \tag{2.45}$$

$$d_\delta = \frac{T_\delta}{T_s} = m_c \sin(\theta_R) \tag{2.46}$$

$$d_{0R} = \frac{T_{0\mathrm{R}}}{T_s} = 1 - (d_\lambda + d_\delta) \tag{2.47}$$

where, m_c is the current modulation index. The current modulation index is the peak value of the input current divided by the dc current, that is,

$$m_c = \frac{\hat{I}_{in}}{I_{DC}} \tag{2.48}$$

The value of dc voltage, V_{DC} can be derived as follows:

$$P_{DC} = P_{in} \tag{2.49}$$

$$V_{DC} I_{DC} = 3 I_{in} V_{in} \cos(\varphi_i) \tag{2.50}$$

$$V_{DC}I_{DC} = 3\frac{1}{2}\hat{I}_{in}\hat{V}_{in}\cos(\varphi_i) \tag{2.51}$$

$$V_{DC} = 3\frac{1}{2}\hat{V}_{in}\frac{\hat{I}_{in}}{I_{DC}}\cos(\varphi_i) \tag{2.52}$$

$$V_{DC} = \frac{3}{2}m_c\hat{V}_{in}\cos(\varphi_i) \tag{2.53}$$

where φ_i is the input displacement angle. Under steady state conditions, the dc link voltage is constant and the maximum dc voltage occurs when the displacement angle is set to zero. When the displacement angle is increased the dc voltage decreases.

2.2.2 Space Vector Inverter Control

The magnitudes of switching voltage vectors depend on the dc link voltage and the states of the rectifier stage. The magnitudes of the voltage switching vectors become $\frac{2}{\sqrt{3}}$ times of the dc voltage value. The inverter stage switches are only allowed to form eight states to avoid a short circuit. Six of the active vectors $V_{[1-6]}$ and two zero vectors V_o and V_7 form these eight states. Table 2.4 lists the switch states of the inversion stage. For instance, space vector $V_5[001]$ specifies that V_C is connected to V_{DC+} and the other two phase V_A and V_B are connected to V_{DC-}.

$$V_5 = \frac{2}{3}(V_A + V_B e^{\frac{j2\pi}{3}} + V_C e^{j4\pi/3}) \tag{2.54}$$

$$V_5 = \frac{2}{3}(\frac{-1}{3}V_{DC} - \frac{1}{3}V_{DC}e^{\frac{j2\pi}{3}} + \frac{2}{3}V_{DC}e^{\frac{j4\pi}{3}}) \tag{2.55}$$

$$V_5 = \frac{2}{3}V_{DC}e^{j7\pi/6}) \tag{2.56}$$

Symbols p and n in Fig. 2.19 refer to the upper and lower switches of the inverter. For example, pnn means that the upper switch in branch A and the lower switches in branches B and C are turned on.

State	Vector	$\begin{bmatrix} S_{I1} & S_{I3} & S_{I5} \\ S_{I2} & S_{I4} & S_{I6} \end{bmatrix}^T$	V_A V_{AB}	V_B V_{BC}	V_C V_{CA}	$\angle V_{out}$	$\lvert V_{out} \rvert$	I_{DC}
Active	$V_1[100]$	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix}^T$	$^2/_3 V_{DC}$ V_{DC}	$-$ 0	$^{-1}/_3 V_{DC}$ $-V_{DC}$	0	$\frac{2}{3}V_{DC}$	I_A
Active	$V_2[110]$	$\begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}^T$	$^1/_3 V_{DC}$ 0	$^1/_3 V_{DC}$ V_{DC}	$^{-2}/_3 V_{DC}$ $-V_{DC}$	$\frac{\pi}{3}$	$\frac{2}{3}V_{DC}$	$-I_C$
Active	$V_3[010]$	$\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix}^T$	$^{-1}/_3 V_{DC}$ $-V_{DC}$	$^2/_3 V_{DC}$ V_{DC}	$^{-1}/_3 V_{DC}$ 0	$\frac{2\pi}{3}$	$\frac{2}{3}V_{DC}$	I_B
Active	$V_4[011]$	$\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \end{bmatrix}^T$	$^{-2}/_3 V_{DC}$ $-V_{DC}$	$^1/_3 V_{DC}$ 0	$^1/_3 V_{DC}$ V_{DC}	π	$\frac{2}{3}V_{DC}$	$-I_A$
Active	$V_5[001]$	$\begin{bmatrix} 0 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix}^T$	$^{-1}/_3 V_{DC}$ 0	$-$ $-V_{DC}$	$^2/_3 V_{DC}$ V_{DC}	$\frac{-2\pi}{3}$	$\frac{2}{3}V_{DC}$	I_C
Active	$V_6[101]$	$\begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}^T$	$^1/_3 V_{DC}$ V_{DC}	$-$ $-V_{DC}$	$^1/_3 V_{DC}$ 0	$\frac{-\pi}{3}$	$\frac{2}{3}V_{DC}$	$-I_B$
Zero	$V_{[0,0,0],[1,1,1]}$	$\begin{bmatrix} 0 & 0 & 0 \\ 1 & 1 & 1 \end{bmatrix}^T \begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 0 \end{bmatrix}^T$					0	0

Table 2.4 Switching vector states of the inversion stage.

Modulation of the active vectors decides the angular position of the averaged output voltage vector, while a zero vector is employed to adjust its magnitude. The shoot-through state, that is, simultaneous turn-on of both switches in a leg, produces the voltage boost. The reference vector of output voltage is defined as

$$\vec{V}_o^* = V_{out} e^{j\omega_o t} \tag{2.57}$$

where V_{out} is the desired output line voltage and ω_o is the output radian frequency.

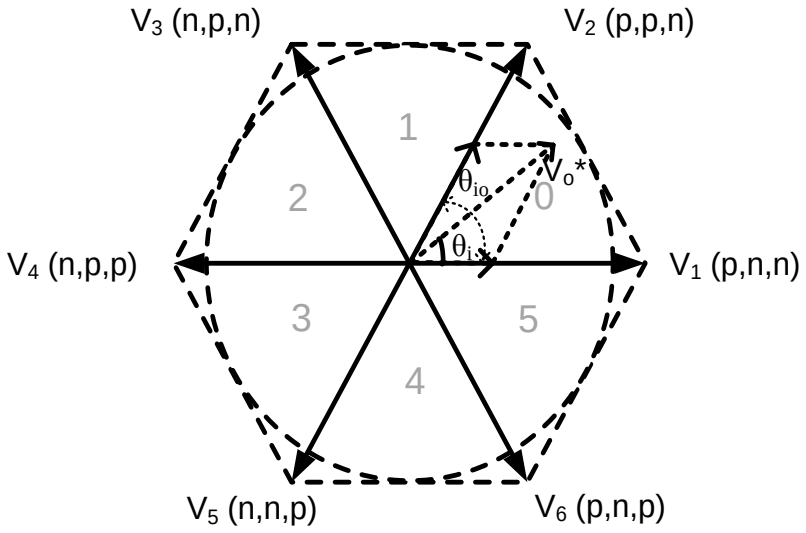


Fig. 2.19 Diagram of output-voltage space vectors.

The location of the reference vector within one of the 60° sectors defines the framing vectors V_α and V_β , as illustrated in Fig. 2.20. For example, in Fig. 2.19, the reference vector of output voltage is in the zero sector.

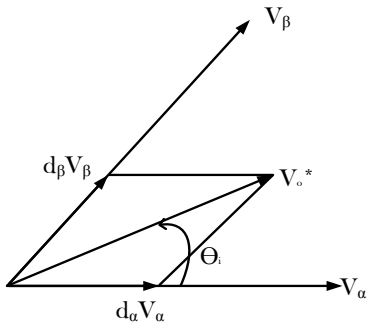


Fig. 2.20 Reference output voltage space vector with the adjacent vectors.

The duration of the active vectors (V_α, I_β) determines the direction and the zero vector adjust the amplitude of the $V_o{}^*$. The angle θ_i is the angle of the reference voltage space vector within the considered hexagon sector.

$$\theta_i = \theta_{io} - \frac{\pi}{3} N_{sector[0-5]} \tag{2.58}$$

Then, the duty ratios of the active, d_λ, d_δ, and zero, d_{0R}, vectors are calculated as:

$$d_\alpha = \frac{T_\alpha}{T_s} = m_v \sin\left(\frac{\pi}{3} - \theta_i\right) \tag{2.59}$$

$$d_\beta = \frac{T_\beta}{T_s} = m_v \sin(\theta_i) \tag{2.60}$$

$$d_{0i} = \frac{T_{0\mathrm{i}}}{T_s} = 1 - (d_\lambda + d_\delta) \tag{2.61}$$

where m_v is the voltage modulation index. The voltage modulation index is the peak value of the output voltage divided by the dc voltage. The value of dc output current can be found as follows:

$$P_{DC} = P_{in} \tag{2.62}$$

$$V_{DC} I_{DC} = 3 I_{out} V_{out} \cos(\varphi_o) \tag{2.63}$$

$$I_{DC} = \frac{\sqrt{3}}{2} m_v \hat{I}_{out} \cos(\varphi_o) \tag{2.64}$$

where φ_o is the load displacement angle.

2.2.3 Indirect Modulation of Matrix Converter

The time-averaged power outputs from the three-switch rectifying stage and the inverter stage are equal. This allows combining the two modulation strategies. The combined duty ratios are given by

$$d_{\lambda\alpha} = d_\lambda * d_\alpha = m_c m_v \sin\left(\frac{\pi}{3} - \theta_R\right) \sin\left(\frac{\pi}{3} - \theta_i\right) \tag{2.65}$$

$$d_{\lambda\beta} = d_\lambda * d_\beta = m_c m_v \sin\left(\frac{\pi}{3} - \theta_R\right) \sin(\theta_i) \tag{2.66}$$

$$d_{\delta\alpha} = d_\delta * d_\alpha = m_c m_v \sin(\theta_R) \sin\left(\frac{\pi}{3} - \theta_i\right) \tag{2.67}$$

$$d_{\delta\beta} = d_\delta * d_\beta = m_c m_v \sin(\theta_R) \sin(\theta_i) \tag{2.68}$$

$$d0 = 1 - (d_{\lambda\alpha} + d_{\lambda\beta} + d_{\delta\alpha} + d_{\delta\beta}) \tag{2.69}$$

$$\begin{Bmatrix} T_{\lambda\alpha} \\ T_{\delta\alpha} \\ T_{\lambda\beta} \\ T_{\delta\beta} \end{Bmatrix} = T_S \begin{Bmatrix} d_{\lambda\alpha} \\ d_{\delta\alpha} \\ d_{\lambda\beta} \\ d_{\delta\beta} \end{Bmatrix} \tag{2.70}$$

The selection of zero vectors in the sequence is important for the minimization of the number of switchings and the related switching losses. For the minimum switching number, the following rules must be applied:

(1) The rectifier modulation follows the $d_\lambda d_\delta d_0$ sequence.

(2) For an even sector of the output hexagon, the output zero vector is 000. Otherwise, it is 111. In this sequence, zero vectors are combined and applied with any order. There is no need to calculate the zero vectors separately, which saves microprocessor's memory.

Duty ratios of the zero vectors are given by:

$$d_{0R} = m_c * m_v * \left(1 - \cos\left(\frac{\pi}{6} - \theta_R\right)\right) \tag{2.71}$$

$$d_{0i\alpha} = m_c * m_v * \left(\sin\left(\frac{\pi}{6} - \theta_R\right)\right) * \left(1 - \cos\left(\frac{\pi}{6} - \theta_i\right)\right) \tag{2.72}$$

$$d_{0i\beta} = m_c * m_v * (\sin(\theta_R)) * \left(1 - \cos\left(\frac{\pi}{6} - \theta_i\right)\right) \tag{2.73}$$

To sum up, the combined duty ratios have to be applied in the $T_{\lambda\alpha}T_{\lambda\beta}T_{\delta\beta}T_{\delta\alpha}\mathrm{T}_0T_{\delta\alpha}T_{\delta\beta}T_{\lambda\beta}T_{\lambda\alpha}$ sequence to obtain the optimal modulation. The optimization criterion is to minimize the number of switching in the matrix converter. The modulator operates in the domain of vector states and not that of switch states. The switching sequence ensures that the number of switching in the matrix converter is kept at minimum.

Since both the rectifier stage and the inverter stage have six vectors, the combined stage has a total of 36 operation modes. For example if the reference output voltage and reference input currents are both in the same zero sector then the combination can be derived as:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \left(d_\alpha . \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 1 & 0 \end{bmatrix} + d_\beta . \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 1 \end{bmatrix} \right) . \left(d_\lambda . \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} + d_\delta . \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \right) . \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{2.74}$$

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \left(d_\alpha . d_\beta . \left(\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} + \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \right) + d_\delta . d_\lambda . \left(\begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \right) \right) . \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{2.75}$$

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \left(d_\alpha . d_\beta . \begin{bmatrix} V_b \\ V_a \\ V_b \end{bmatrix} + d_\alpha . d_\beta . \begin{bmatrix} V_b \\ V_a \\ V_a \end{bmatrix} + d_\delta . d_\lambda . \begin{bmatrix} V_c \\ V_a \\ V_c \end{bmatrix} + d_\delta . \begin{bmatrix} V_c \\ V_a \\ V_a \end{bmatrix} \right) \tag{2.76}$$

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \left(d_\lambda . \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 0 \end{bmatrix} + d_\delta . \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 1 \end{bmatrix} \right) . \left(d_\alpha . \begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} + d_\beta . \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix} \right) . \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \tag{2.77}$$

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \left(d_\alpha . d_\lambda . \left(\begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} + \begin{bmatrix} 1 & 0 & 1 \\ 0 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \right) + d_\alpha . d_\delta . \left(\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \\ 0 & 0 & 0 \end{bmatrix} + \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix} \right) \right) . \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \tag{2.78}$$

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \left(d_\alpha . d_\lambda . \begin{bmatrix} -I_B \\ I_B \\ 0 \end{bmatrix} + d_\alpha . d_\beta . \begin{bmatrix} -I_B \\ 0 \\ I_B \end{bmatrix} + d_\delta . d_\lambda . \begin{bmatrix} I_A \\ -I_A \\ 0 \end{bmatrix} + d_\delta . \begin{bmatrix} I_A \\ 0 \\ -I_A \end{bmatrix} \right) \tag{2.79}$$

Indirect modulation can be applied to both direct matrix converter and indirect matrix converter. For instance, if the desired state of the rectifier is to connect input phase "a" to V_{DC+} and input phase "c" to V_{DC-}. The rectifier control matrix is shown as $R = [1,0,-1]$, where "1" yields to top on switch and "-1" is the bottom on switch

For the inverter stage, the control matrix I is used to determine whether output phases are connected either to the positive or to the negative dc link rail. If the desired state of the inverter is to connect output phase "A" to V_{DC+} and input phase "B" to V_{DC-}. The inverter control matrix has $I^T = [2,2,1]$. Here "2" yields to the top switch and "1" yields to the bottom switch. The resultant matrix converter shows as:

$$T = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} * [R_1\ R_2\ R_3] = \begin{bmatrix} 2 & 2 & 1 \\ 0 & 0 & 0 \\ -2 & -2 & -1 \end{bmatrix} = \begin{bmatrix} S_{aA} & S_{bA} & S_{cA} \\ S_{aB} & S_{bB} & S_{bC} \\ S_{aC} & S_{bC} & S_{cC} \end{bmatrix} \tag{2.80}$$

At the resultant transfer function "2" and "-1" represents the "on" switches for direct matrix converter. For this example, $(S_{aA}S_{bA}, S_{cC})$ must be turned on for the current switching sequence.

Fig. 2.21 through Fig 2.29 show an example optimum sequence where the inverter space vector is in sector 2 and rectifier space vector in sector 4. The switching sequence is $T_{\lambda\alpha} - T_{\lambda\beta} - T_{\delta\alpha} - T_{\delta\beta} - T_0 - T_{\delta\beta} - T_{\delta\alpha} - T_{\lambda\beta} - T_{\lambda\alpha}$. Red switches are the "on" switches:

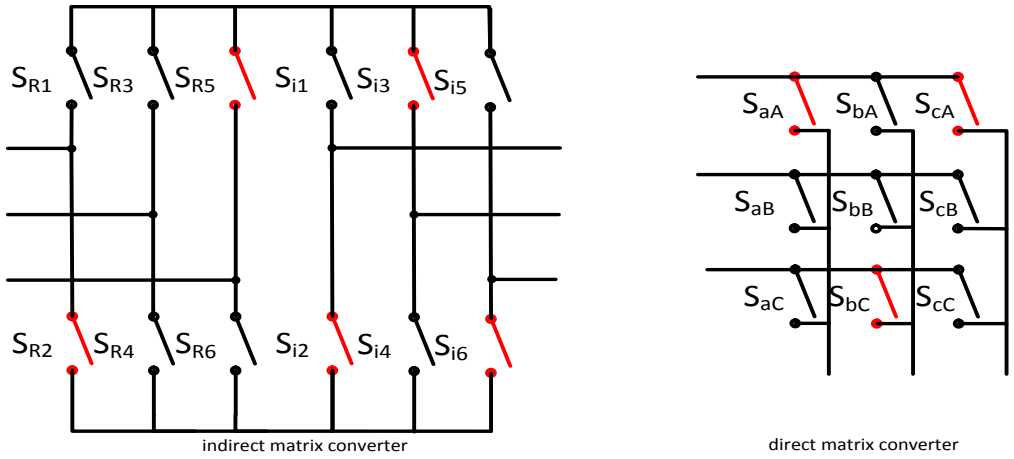


Fig. 2.21 Step 1: $T_{\lambda\alpha}$ where $\lambda = ca$ and $\alpha = 010$.

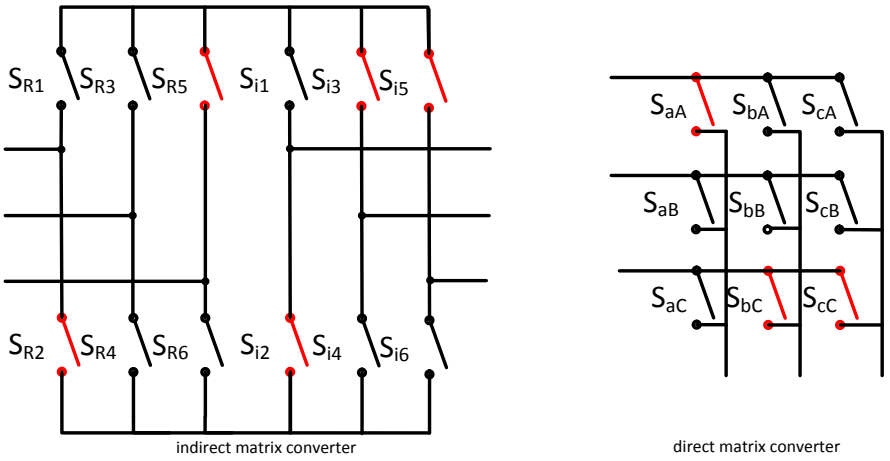


Fig. 2.22 Step 2: $T_{\lambda\beta}$ where $\lambda = ca$ and $\beta = 011$.

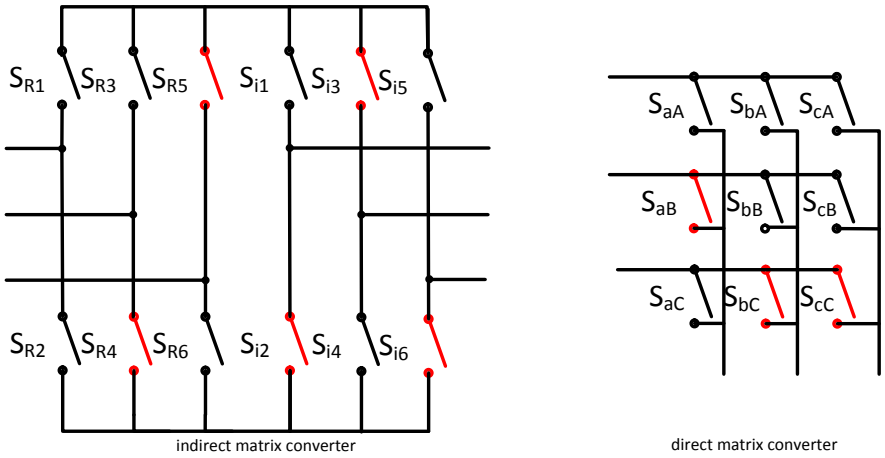


Fig. 2.23 Step 3: $T_{\delta\beta}$ where $\delta = cb$ and $\beta = 011$.

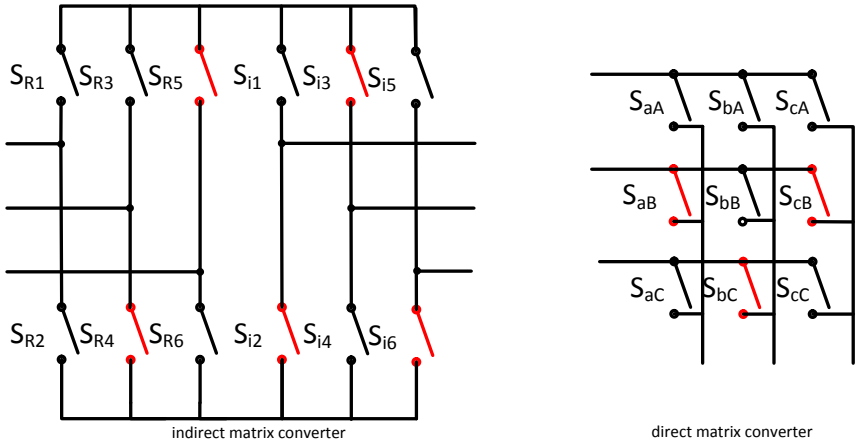


Fig. 2.24 Step 4: $T_{\delta\alpha}$ where $\delta = cb$ and $\alpha = 010$.

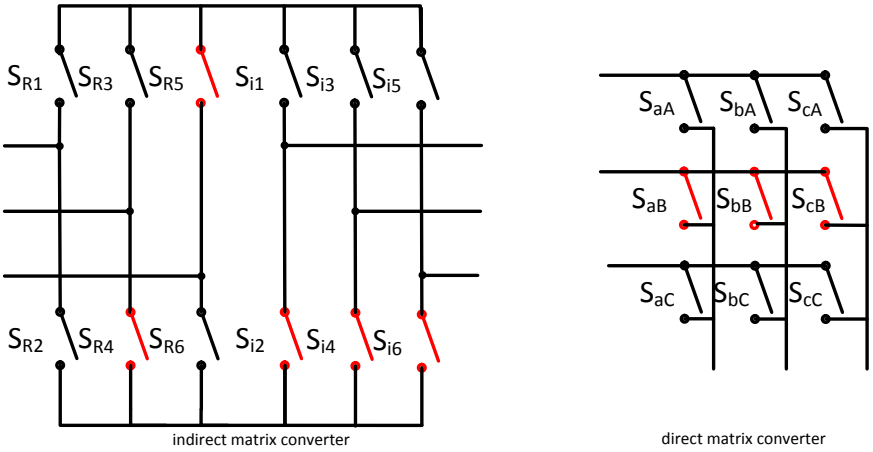


Fig. 2.25 Step 5: T_0 where $\delta = cb$ and $\alpha = 000$.

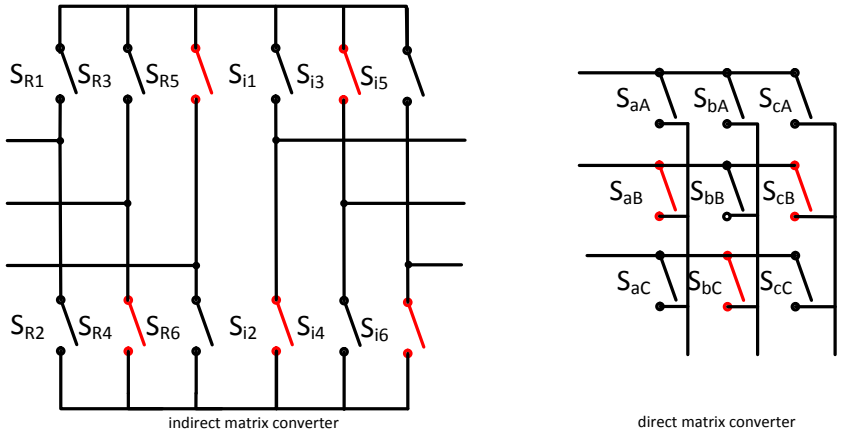


Fig. 2.26 Step 6: $T_{\delta\alpha}$ where $\delta = cb$ and $\alpha = 010$.

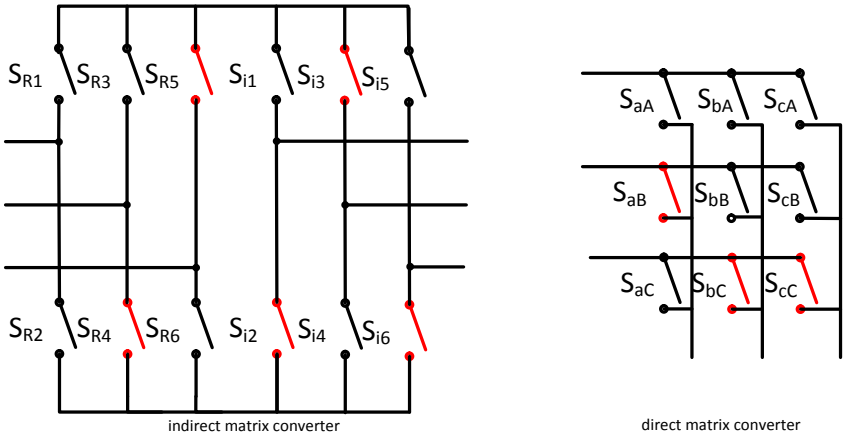


Fig. 2.27 Step 7: $T_{\delta\beta}$ where $\delta = cb$ and $\beta = 011$.

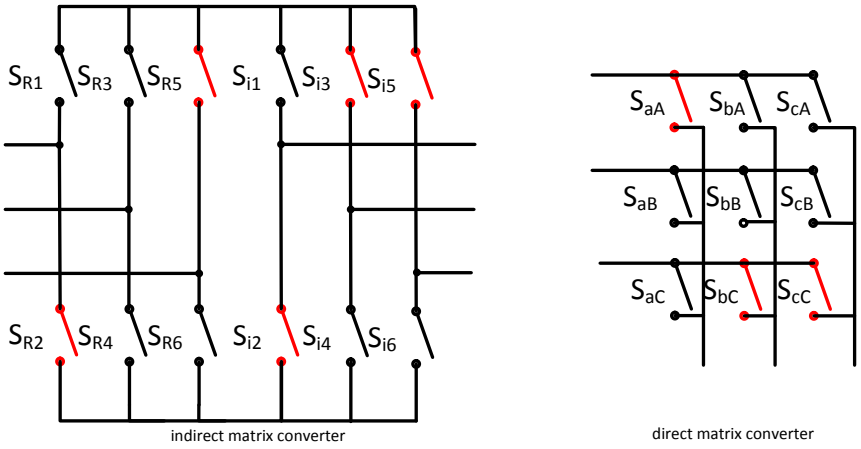


Fig. 2.28 Step 8: $T_{\lambda\beta}$ where $\lambda = ca$ and $\beta = 011$.

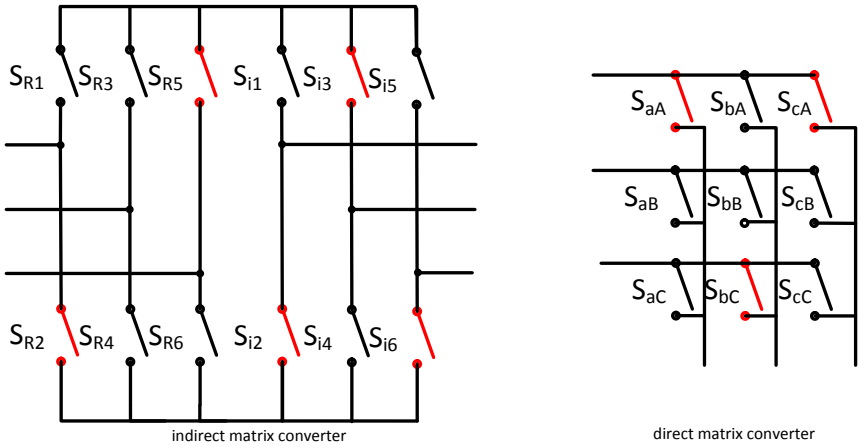


Fig. 2.29 Step 9: $T_{\lambda\alpha}$ where $\lambda = ca$ and $\alpha = 010$.

2.3 Conclusion

In this chapter, various topologies of matrix converters were investigated. Sparse type converters provide excellent solution to direct and indirect matrix converters that suffer from high number of power switches and control drivers. Also, the operating principles and space vector modulation for the matrix converter have been reviewed. By applying the space vectors concept to compute the duty cycles for the switches, the matrix converter is modulated so that its averaged output voltages and currents represent balanced sinusoidal waveforms.

Chapter 3

Boost Network Topologies

In common practice, a transformer at line frequency is utilized to boost the voltage following by the dc-ac conversion. Line frequency transformers result in large size, loud acoustic noise, and high costs. In addition, the inverter may need to be oversized to withstand the wide input voltage variations. The apparent power ratings of the inverter need to be doubled if the input voltage varies in the 1:2 range.

To avoid the transformer and minimize the required apparent power ratings of the inverter, a high frequency dc-dc converter is employed to step up the voltage. However, the additional power stage conversion plus the drivers bring additional costs. The cost of the converters is higher in high power applications; therefore an additional power stage may not affect drastically affect the cost-profit ratio. On the other hand, the cost of lower power capability converters increased in drastically with an additional power stage.

There are alternative solutions utilized to realize the inversion and boost functions in a single stage. This chapter describes four networks that employ inductors and capacitors in an X shape arrangement and which are called Z-sources. The inductors and capacitors in Z-sources are energy devices and can be optimally designed to ensure small size and low cost. Inverters incorporating these networks inherit the advantages of the traditional voltage source inverters. As no dead time is needed, the control accuracy and harmonic content can be improved. Furthermore, Z-sources reduce the apparent power requirements.

3.1 Z-source Network

A Z-source inverter (ZSI), shown in Fig. 3.1, utilizes shoot-through states to boost the output voltage that improves the inverter reliability and improves the dc-ac conversion [6]. For applications that have variable inputs, ZSI represents a highly competitive topology.

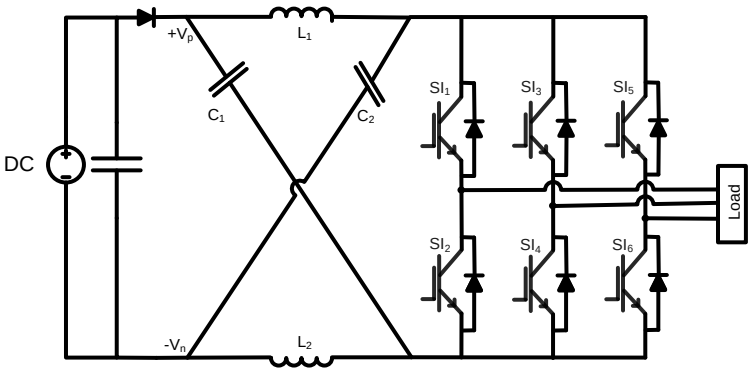


Fig. 3.1 Z-source inverter.

The ZSI employs an X shape LC network between the input voltage and the inverter bridge. An additional shoot-through state is employed together with traditional eight switching states, that is, six active states (SV [1-6]) and two zero states (SV0, SV7). They are illustrated in Fig. 3.2. One can intentionally insert the shoot-through state to boost the voltage, overcoming the voltage limitations of the traditional voltage source inverter (VSI) or the current source inverter (CSI).

The reliability of the ZSI is high due to its ability to handle shoot-through. In practical applications, a dead time has to be applied to the power switches of the VSI to avoid short circuits. Dead time is absent from Z-source converters as the shoot-through is actually desirable for boosting the voltage [56-62].

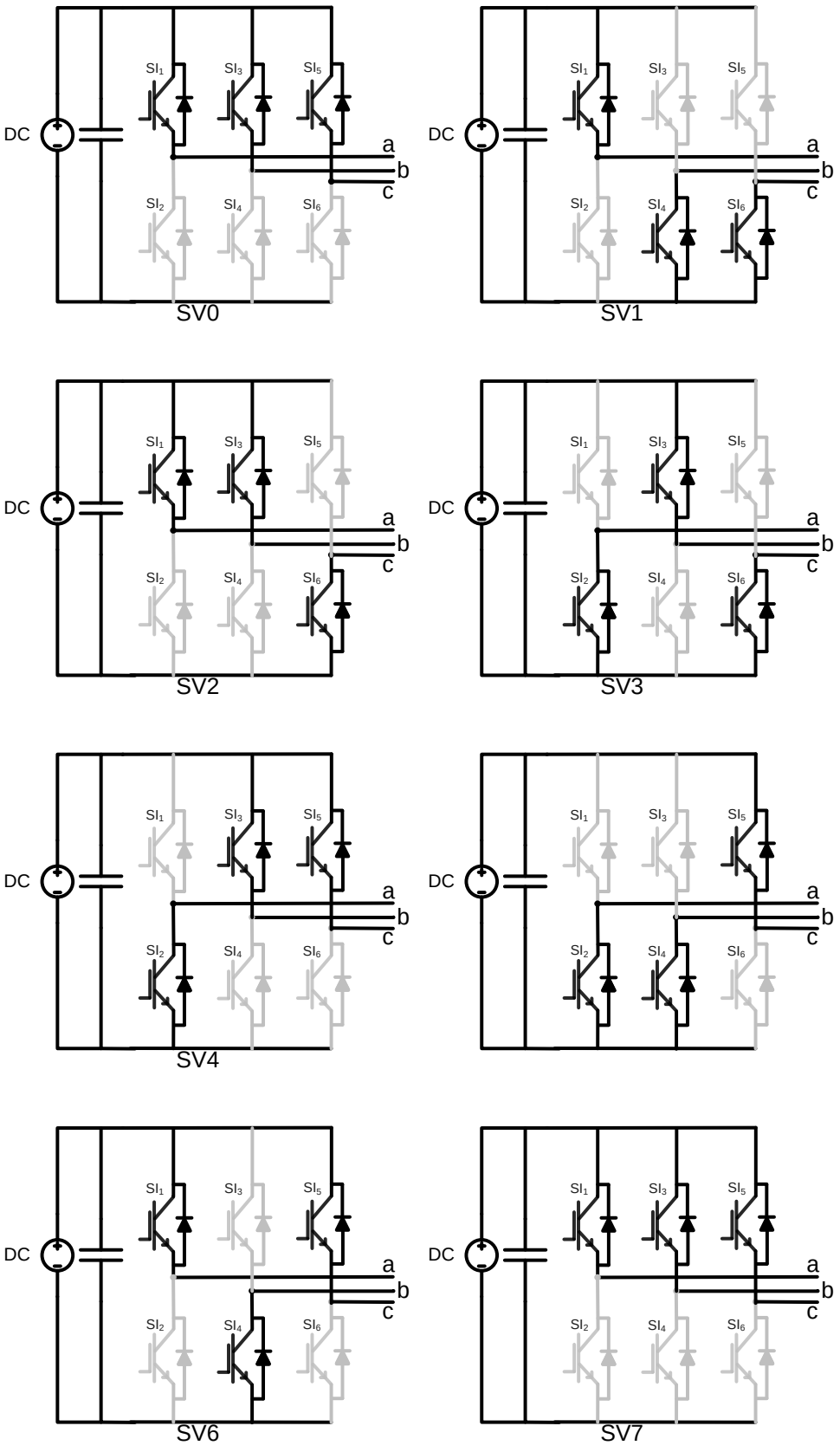


Fig. 3.2 States of the VSI (dark power switches are on, grey switches are off).

Shoot-through can occur in any of the three ways shown in Fig. 3.3. Any phase leg can be shorted as needed. However, a trade off in the control must be made. One can either reduce the switching frequency by shorting one or two phase legs or reduce the current stress on each device by shorting all phase legs during short through state.

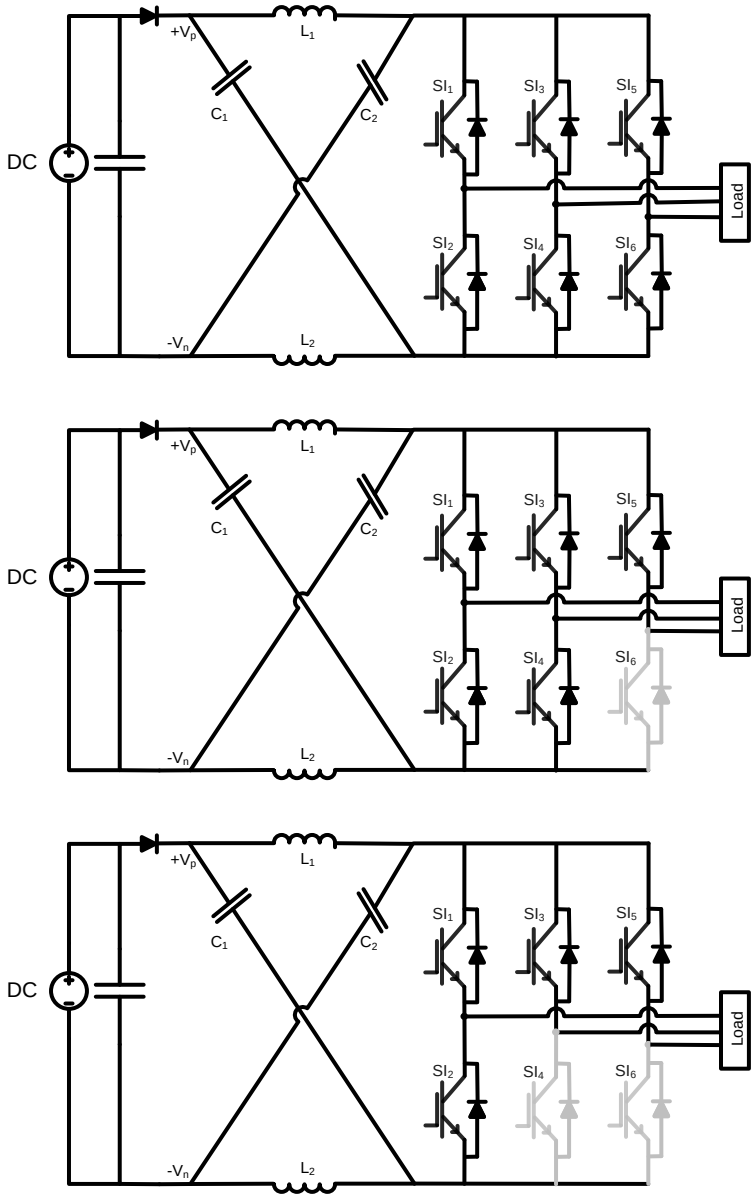


Fig. 3.3 Instances of shoot-through states. From top to bottom (a) three legs shoot-through (b) two legs shoot-through (c) one leg shoot-through.

3.1.1 Operation Principle

Figs. 3.4(a) and (b) illustrate the non-shoot-through state and the shoot-through state of the Z-source, respectively. In the non-shoot-through states, capacitors C_1 and C_2 are charged by the input voltages. In 3.4(b), the inverter is operating under the shoot-through condition to provide the voltage boost. The duration of the shoot-through state depends on the desired voltage boost factor. Due to the reverse-biased input diode, the coupling between the rectifier and inverter stages is broken. Inductor L_1 is charged by C_1 and inductor L_2 is charged by C_2.

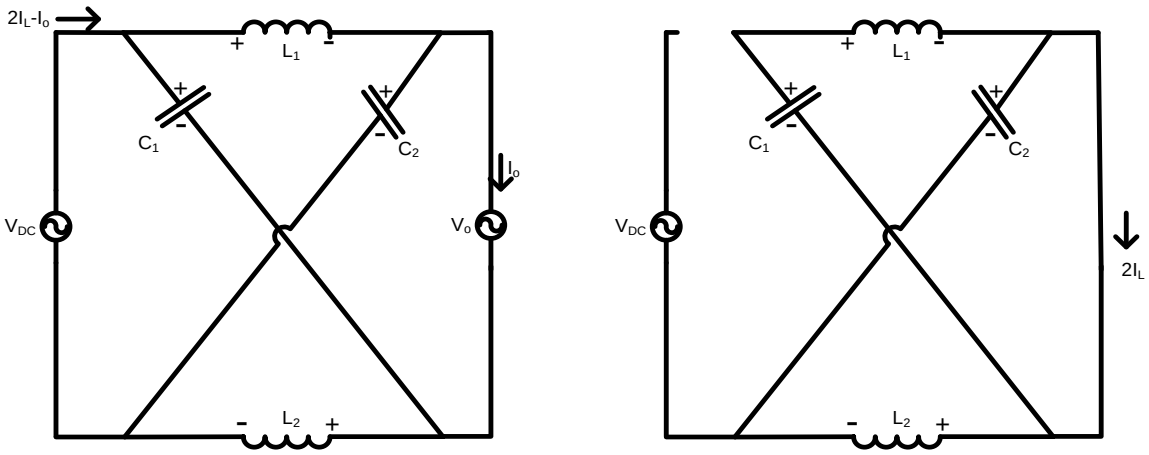


Fig. 3.4 Equivalent circuits of the Z-source: (a) non-shoot-through state, (b) shoot-through state.

3.1.2 Circuit Analysis

Assuming the same inductance (L) and capacitance for the inductors L_1 and L_2 and capacitors $C_1$and C_2, the symmetry of the Z-source network yields:

$$V_C = V_{C_1} = V_{C_2} \tag{3.1}$$

$$V_L = V_{L1} = V_{L2} \tag{3.2}$$

The capacitor voltage V_C remains steady within one switching cycle T if the capacitance selected properly. In practice, capacitances have tolerances that can cause slight voltage distortions across the capacitors.

The total time of all the intervals of the shoot-through switching state within one switching cycle T is T_0 and v_{pn} denotes the voltage over the inverter legs. The circuit in the short through state are

$$\left\{\begin{array}{c|c} v_{pn}=0 & v_{pn}=0 \\ v_L=v_d-V_C & v_L=V_C \\ v_d=2V_C & v_d=2V_C \end{array}\right\}, v_L=V_C \tag{3.3}$$

$$\left\{\begin{array}{c|c} i_p=I_L-i_C & i_p=2I_L \\ i_C=i_d-I_L & i_C=-I_L \\ I_d=0 & I_d=0 \end{array}\right\}, i_C=-I_L \tag{3.4}$$

Whenever the inverter falls into one of the eight non-shoot-through states, the total time of all the intervals of the states within the switching cycle is T_1, where

$$T_1=T-T_0 \tag{3.5}$$

In the steady state, we have

$$\left\{\begin{array}{l|l} v_{pn}=2V_C-v_d & v_{pn}=2V_C-V_{dc} \\ v_L=v_d-V_C & v_L=V_{dc}-V_C \\ v_d=V_C & v_d=V_C \end{array}\right\}, v_L=V_{dc}-V_C \tag{3.6}$$

$$\left\{\begin{array}{l|l} i_p=I_L-i_C & i_p=2I_L-I_{dc} \\ i_C=i_d-I_L & i_C=I_{dc}-I_L \\ I_d=I_{dc} & I_d=I_{dc} \end{array}\right\}, i_C=I_{dc}-I_L \tag{3.7}$$

where I_{dc} denotes the magnitude of DC source current.

From the volt-second balance law the average inductor voltage drop $< v_L >$ within one switching cycle is zero:

$$< v_L >= \frac{T_0V_C+T_1(V_{dc}-V_C)}{T} \tag{3.8}$$

As $v_L=v_d-V_C$ at all times, then

$$< v_L > \int_0^T \frac{1}{T}(v_d-V_C)dt = < v_d > -V_C = 0 \tag{3.9}$$

From the ampere-second balance law the average capacitor current within one switching cycle is zero, so that

$$< i_C >= \frac{T_0(-I_L)+T_1(I_{dc}-I_L)}{T} = 0 \tag{3.10}$$

As $i_C = i_d - I_L$ at all times, then

$$< i_C >= \frac{1}{T}\int_0^T (i_d - I_L)dt = < I_d > -I_L = 0 \tag{3.11}$$

The relation between capacitor voltage V_C and DC source voltage V_{dc} is

$$\frac{V_C}{V_{dc}} = \frac{T_1}{T_1 - T_0} \tag{3.12}$$

The average input voltage to Z-source network is

$$< v_d >= V_C \tag{3.13}$$

And the average dc-link voltage v_{pn} is given by

$$< v_{pn} >= \frac{T_1}{T_1 - T_0} V_{dc} = V_C \tag{3.15}$$

The relation between the inductor current I_L and DC source current I_{dc} is obtained as:

$$\frac{I_L}{I_{dc}} = \frac{T_1}{T_1 - T_0} \text{ or } I_L = \frac{T_1}{T} I_{dc} = D I_{dc} \tag{3.16}$$

where, D is the non-shoot-through duty ratio. The average input current $< i_d >$ to Z-source network is given by

$$< i_d >= I_L \tag{3.17}$$

The average dc-link current $< i_p >$ is then given by

$$< i_p > = 2I_L = \frac{T_1}{T} I_{dc} = I_L \tag{3.18}$$

and, from Eqs. (3.17) and (3.18), the average current into the Z-source network is the inductor current, that is

$$< i_d >=< i_p >= I_L = DI_{DC}. \tag{3.19}$$

3.1.3 Boost Factor and Voltage Gains

If the boost factor *B* is defined as

$$B = \frac{v_{pn}}{V_{dc}} = \frac{1}{1-2d_{sh-th}} \tag{3.20}$$

where, d_{sh-th} is the shoot-through duty ratio, then the peak voltage of the DC link voltage $v_{pn,pk}$ is given by

$$v_{pn,pk} = BV_{dc} \tag{3.21}$$

The relation between V_C and V_{dc} is

$$V_C = (1 + B)\frac{V_{dc}}{2} \tag{3.22}$$

The peak voltage between p and n is only available within the intervals of the non-shoot-through switching states of the inverter bridge, and only within such intervals can the bridge operate as a VSI inverter. So the peak voltage between p and n is equivalent to the dc link voltage of the classic VSI inverter. If the peak phase AC voltage is denoted by $V_{ac,pk}$, then

$$V_{ac,pk} = m\frac{V_{pn}}{2} \tag{3.23}$$

where, *m* is the modulation index and $0 < m \leq 1$ constraint must be satisfied. From Eqs. (3.21) and (3.23),

$$V_{ac,pk} = mB\frac{V_{dc}}{2} \tag{3.24}$$

It can be seen that the boost factor affects the ratio of input and output voltages. It can be adjusted by varying the shoot-through duty ratio. In control of the converter output voltage, the modulation index and the shoot-through ratio play an essential role. Table 3.1 shows the effect of

the shoot-through duty ratio on Z-source inductor and capacitor voltages and currents. Here D is the input current blocking diode and S_D is the shoot-through switching function (e.g. if $S_D = 1$ shoot-through states, else $S_D = 0$ active and zero states)

Voltage ratios	**Duty ratio effect**	**Current relations**	**Duty ratio effect**
$\boldsymbol{\frac{V_{C1}}{V_{IN}}}$	$\frac{1 - d_{sh-th}}{1 - 2d_{sh-th}}$	$\boldsymbol{I_{C1}}$	$-I_{pn} - I_{L1}$
$\boldsymbol{\frac{V_{C2}}{V_{IN}}}$	$\frac{1 - d_{sh-th}}{1 - 2d_{sh-th}}$	$\boldsymbol{I_{C2}}$	$-I_{pn} - I_{L2}$
$\boldsymbol{\frac{V_{L1}}{V_{IN}} = \frac{V_{L2}}{V_{IN}}}$	$\frac{d_{sh-th}}{1 - 2d_{sh-th}} - S_D * \frac{1}{1 - 2d_{sh-th}}$	$\boldsymbol{I_{L1} = I_{L2}}$	$\frac{P}{V_{IN}}$
$\boldsymbol{\frac{V_{pn}}{V_{IN}}}$	$\overline{S_D} * \frac{1}{1 - 2d_{sh-th}} \geq 0$	$\boldsymbol{I_D}$	$I_{L1} + I_{L2} + I_{pn}$
$\boldsymbol{\frac{V_D}{V_{IN}}}$	$S_D * \frac{1}{1 - 2d_{sh-th}} \geq 0$	$\boldsymbol{I_{in}}$	I_D

Table 3.1 Governing functions of ZSI.

3.1.4 Design Guideline

The maximum current stress in the device can be calculated from the following equation:

$$I_{max} = \frac{P_{max}}{2V_{pn}} + 2I_L = \frac{P_{max}}{2V_{pn}} + 2\frac{P_{avg}}{V_{dc}} \tag{3.25}$$

where P_{max} is the maximum transient output power and P_{avg} is the average output power. The current stress can be reduced by turning two or all phase legs during shoot-through for three-phase systems in order to distribute $2I_L$ into different phase legs.

To determine the inductance and capacitance of the Z-source network the input power is assumed to be constant. The ripple power is absorbed by the capacitors of the Z-source network. The ripple power absorbed by the capacitors is calculated as:

$$\Delta P = \int_{-1/Vin}^{1/V_{in}} \cos(120 * 2 * \pi)\, tdt = \frac{1}{2}C(V + \Delta V)^2 - \frac{1}{2}CV^2 \quad (3.26)$$

where V is the average voltage across the capacitor, C is the total capacitance of the two capacitors in Z-source. Thus, the capacitance can be chosen to limit the voltage ripple to be less then $x\%$. Based on the voltage ripple across the capacitors, the ripple voltage across the inductor is the voltage difference between the capacitor and the voltage between p and n. As the capacitor voltage is known with $x\%$ ripple, the voltage between p and n is zero during shoot-through and $2V_C - V_{dc}$ for the non-shoot-through states. Therefore, the voltage ripple across the inductor is:

$$V_{Lripple} = \left(1 - \frac{2T_0}{T}\right) * \ x\% * V \quad (3.27)$$

Limitations of the ripple can be application specific or design specific. Energy holding inductors are costly, depending on their size. The higher ripple smoothing ability brings additional costs and size. The optimum voltage ripple should also be obtained considering the power efficiency of the converter; mainly including the conduction and switching losses, and the stability due to the dynamic load.

3.2 Series Z-source Network

Together with all the merits of Z-source inverters there are also some drawbacks. To perform the voltage boost, Z source capacitors voltage is larger than the input voltage. Thus, high voltage capacitors are needed in the network. Also due to high rated capacitors, converter cannot hold back the rush current and resonance between the capacitors and the inductors. To solve these problems series Z-source networks were proposed in [13].

In the ZSI, the Z-source network influences the system weight and volume. The system's power density can also be improved by minimizing the size of Z-source network. The size of the

Z-source capacitors can be minimized by improving the series ZSI topology as well. The power source is in series with the inverter bridge, and displays reduced voltage across both capacitors and the soft start capability. Compared to traditional ZSI, the improved ZSIs can reduce the size and cost of the capacitor in a Z-source network with higher power density. All the ZSIs utilize the shoot-through state to boost the voltage and can therefore be modulated with the same PWM strategies [63], [65].

The series Z -source inverter (SZSI) is shown in Fig. 3.5. The components used are the same as in the Z-source inverter. The difference is that the positions of the bridge and diode are interchanged and their connection direction is reversed. The voltage polarity of the Z -capacitors in the topology keeps the same input voltage polarity. Therefore, the Z -capacitor voltage stress can be greatly reduced and get the same boost voltage across the inverter bridge. In addition, there is no current path at startup which reduces the inrush current.

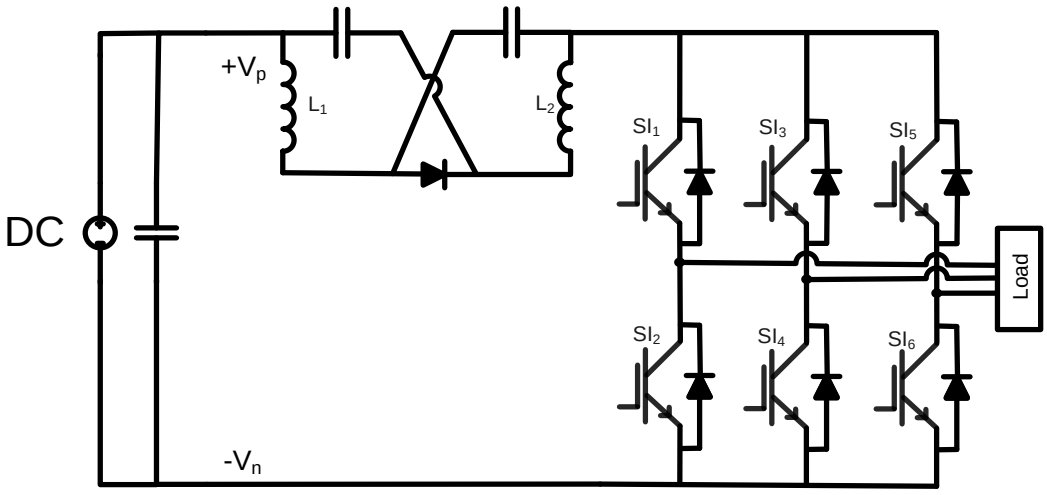


Fig. 3.5 Series Z-source inverter.

The SZSI can be derived directly for the traditional ZSI within six stages. By exchanging the position of the DC source and the diode, the capacitor voltage is replaced by the voltage

source V1, the traditional ZSI shown in Fig.3.6 exists a voltage triangle ABC that is composed of V_{dc}, V_1 and a virtual voltage source of V_2.

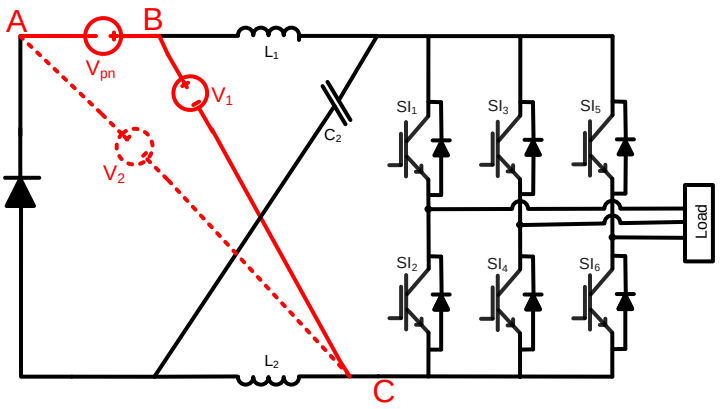


Fig. 3.6 Derivation stage 1 of series Z-source inverter.

The voltage triangle ABC can also be composed of V_{dc}, V_2 and a virtual voltage source V_1 shown in Fig.3.7

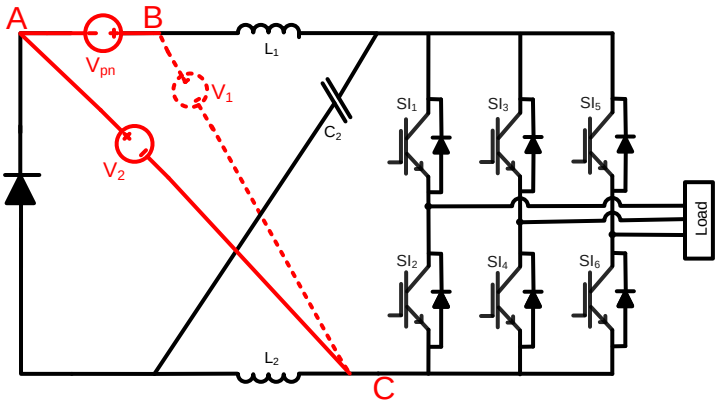


Fig. 3.7 Derivation stage 2 of series Z-source inverter.

Replacing V_2 with the capacitor voltage shown in Fig 3.8 results in power source in series with the inductor.

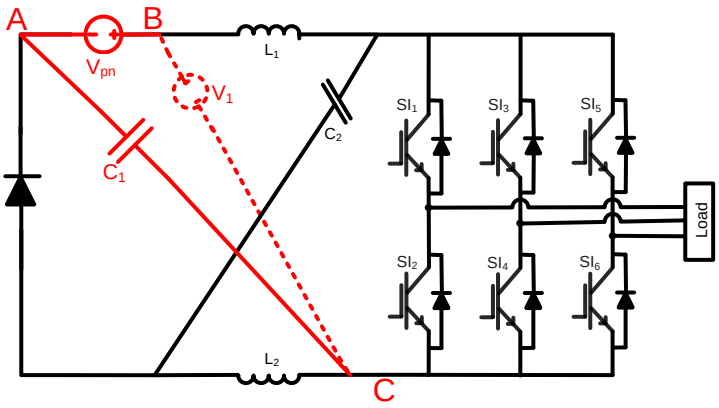


Fig. 3.8 Derivation stage 3 of series Z-source inverter.

Exchanging the position of the power source and inductor the voltage triangle DEF composed of V_{dc}, V_1 and a virtual voltage source V_2 is seen in Fig.3.9.

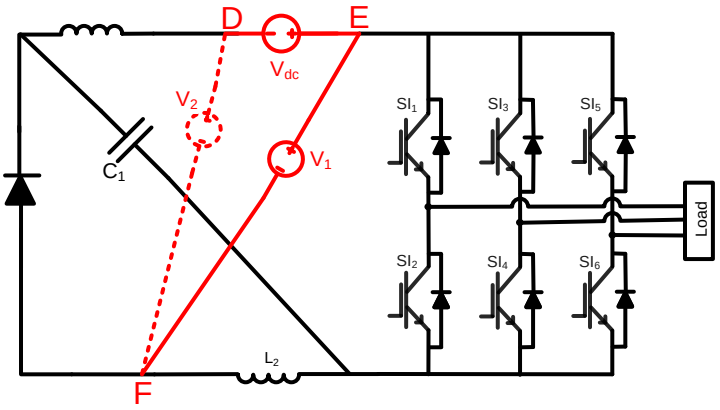


Fig. 3.9 Derivation stage 4 of series Z-source inverter.

The voltage triangle DEF can also be composed of V_{dc}, V_2 and a virtual voltage source V_1, shown in Fig.3.10.

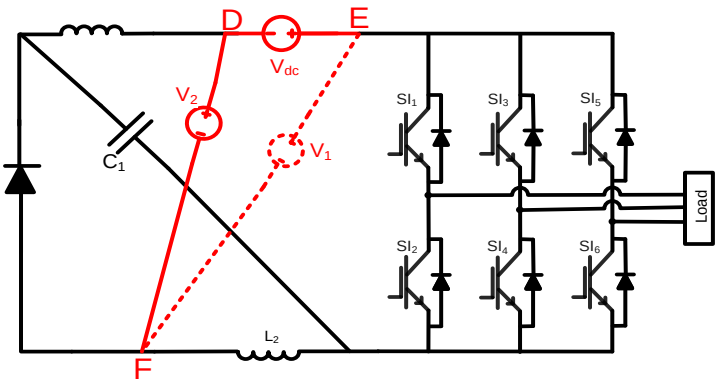


Fig. 3.10 Derivation stage 5 of series Z-source inverter

Finally, voltage V_2 can be replaced with the capacitor voltage shown in Fig. 3.11 and this topology is the series ZSI in which the power source is in series with the inverter bridge.

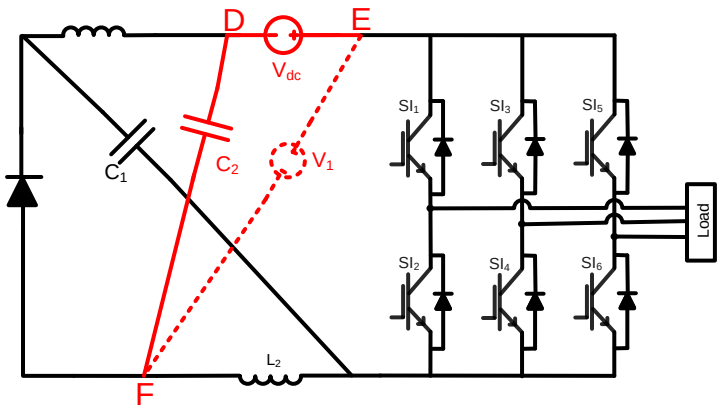


Fig. 3.11 Derivation stage 5 of series Z-source inverter.

3.2.1 Operation Principle

An equivalent circuit of the series Z-source, placed between the input and inverter stages, is shown in Fig. 3.12(a) during the non-shoot-through states and in Fig. 3.12(b) during the shoot-through states. In the non-shoot-through states, capacitors C_1 and C_2 are charged by the input voltage.

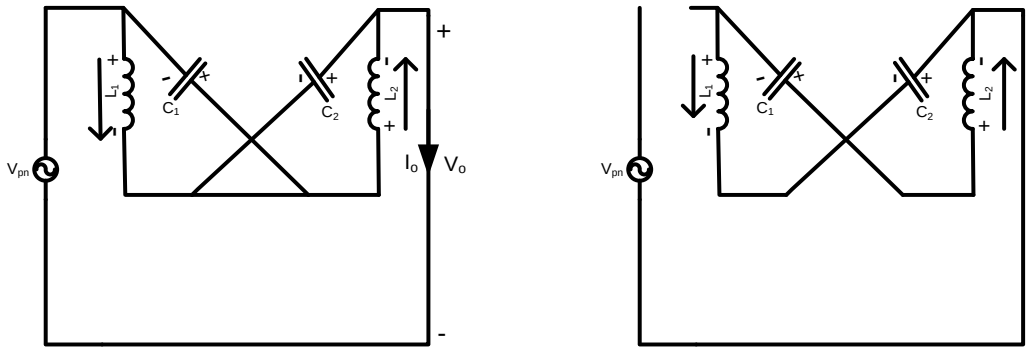


Fig. 3.12 From left to right (a) non-shoot-through states (b) shoot-through states.

Duration of the shoot-through state depends on the desired voltage boost factor. Due to the reverse-biased diode, the coupling between the input and inverter stages is broken. Inductor L_1 is charged from C_1 and inductor L_2 from C_2. When there is no shoot-through, capacitor

voltages are zero. When the converter is in the soft starting stage, capacitor voltages increase gradually, which reduces the excessive inrush current.

3.2.2 Circuit Analysis

The derivation of the circuit is similar to the ZSI. Assuming that Eq. (3.1) and Eq. (3.2) are valid, in the shoot-through state,

$$v_L = V_o + V_C \tag{3.28}$$

When in the non-shoot-through state the inverter stage turns out to be a current source where current is zero in zero states. Then,

$$v_L = -V_C \tag{3.29}$$

The average value of inductor voltage over one switching period is

$$V_C = \frac{d_{sh-th}}{1-2d_{sh-th}} V_o \tag{3.30}$$

The above derivation shows that when the shoot-through duty ratio is zero then the capacitor voltage is zero, too. This leads to the ability of soft-starting by increasing the shoot-through duty ratio gradually.

The peak dc-link voltage over the output phase legs and the output phase voltage can be expressed as

$$V_{pn} = V_o + 2V_C = \frac{1}{1-2d_{sh-th}} V_o = BV_o \tag{3.31}$$

$$V_p = M\frac{V_{in}}{2} = MB\frac{V_o}{2} \tag{3.32}$$

From (3.25), it can be seen that V_C decreases while the voltage boost remain the same. Since the Z-inductor current discharges the Z-capacitor, the ripple of the capacitors in the inverter is expressed as

$$\Delta V_C = \frac{I_L d_{sh-th} T_s}{C} \tag{3.33}$$

where, I_L is the average inductor current.

In non-shoot-through states, the Z-source inductor current decreases, but the inductor current increases, and the resultant current ripple is the same as in the traditional Z-source inverter and it can be expressed as

$$\Delta i_L = \frac{(1-d_{sh-th}) T_s V_C}{L} = \frac{d_{sh-th}(1-d_{sh-th}) T_s V_o}{(1-2di_{sh-th}) L} \tag{3.34}$$

Relative equations of the series Z-source inverter that can be used for advanced control systems are provided in Table 3.2.

Voltage ratios	**Duty ratio effect**	**Current relations**	**Duty ratio effect**
$\boldsymbol{\frac{V_{C1}}{V_{IN}}}$	$\frac{d_{sh-th}}{1-2d_{sh-th}}$	$\boldsymbol{I_{C1}}$	$-I_{pn} - I_{L1}$
$\boldsymbol{\frac{V_{C2}}{V_{IN}}}$	$\frac{d_{sh-th}}{1-2d_{sh-th}}$	$\boldsymbol{I_{C2}}$	$-I_{pn} - I_{L2}$
$\boldsymbol{\frac{V_{L1}}{V_{IN}} = \frac{V_{L2}}{V_{IN}}}$	$\frac{d_{sh-th}}{1-2d_{sh-th}} - S_D * \frac{1}{1-2d_{sh-th}}$	$\boldsymbol{I_{L1} = I_{L2}}$	$\frac{P}{V_{IN}}$
$\boldsymbol{\frac{V_{pn}}{V_{IN}}}$	$\overline{S_D} * \frac{1}{1-2d_{sh-th}} \geq 0$	$\boldsymbol{I_D}$	$I_{L1} + I_{L2} + I_{pn}$
$\boldsymbol{\frac{V_D}{V_{IN}}}$	$S_D * \frac{1}{1-2d_{sh-th}} \geq 0$	$\boldsymbol{I_{in}}$	I_D

Table 3.2 Governing equations of series Z-source inverter.

3.3 Quasi Z-source Network

The quasi Z-source network, which was first introduced in [12], constitutes a voltage-boosting dc link based on two capacitors, two inductors and a diode. The output stage, a classic three-phase inverter, contains six switches and six diodes. The equivalent circuits of the quasi Z-source with continuous input current under the non-shoot-through and shoot-through conditions are shown in Fig. 3.13.

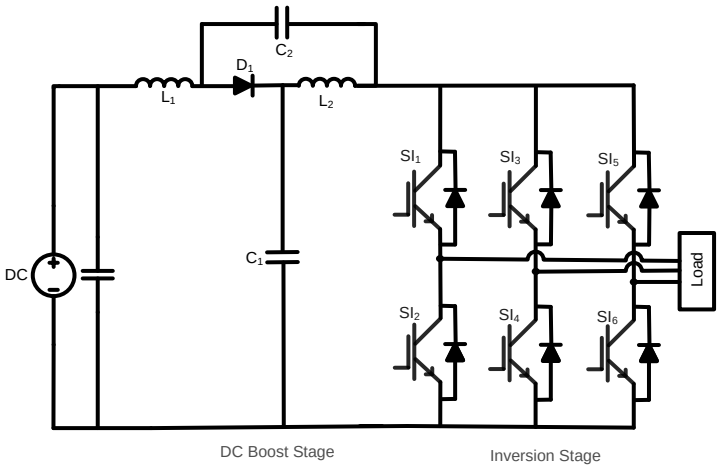
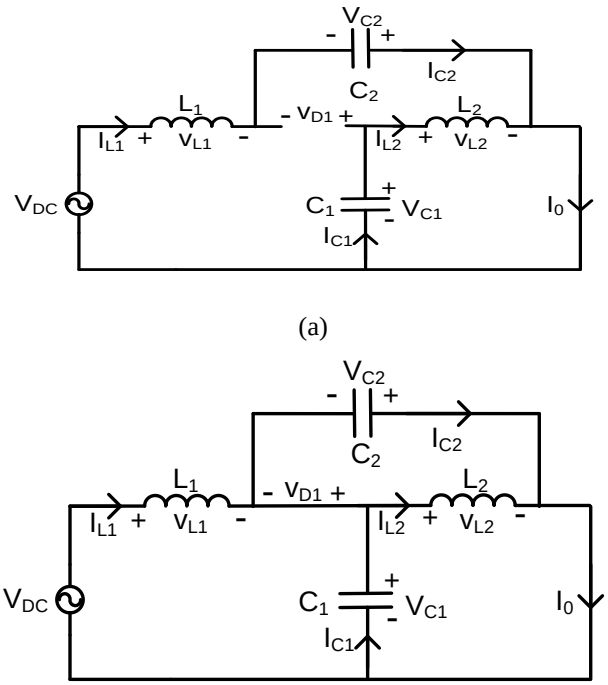


Fig. 3.13 Quasi Z-source inverter.

Compared to traditional Z-source inverters, quasi Z-source inverters have several advantages, including lower component ratings, reduced source stress and wider range of gain [65]-[68]. The system has two modes as shown in Fig.3.14.

The first mode will make the inverter short circuit via any one phase leg, combinations of any two phase legs, and all three-phase legs in Fig.3.13, As before, that is referred to as the shoot-through state. As a result, the diode D_1 is turned off due to the reverse-bias voltage. Its equivalent circuit is shown in Fig.3.14 (a). The second mode mode will make the inverter operate in one of the six active states and two traditional zero states, which are referred to the non-shoot-through state. A continuous current flows through the diode D_1 and its equivalent circuit.



(a)

(b)

Fig. 3.14 Inverter states: (a) shoot-through states (b) non-shoot-through states.

3.3.1 Circuit Analysis

The system equations are almost identical to those of the Z-source inverter. Table 3.2 lists the essential equations that are required to implement any kind of control of this type of inverters. During non-shoot-through states, we get

$$V_{L1} = V_{DC} - V_{C1} \tag{3.35}$$

$$V_{L2} = -V_{C2} \tag{3.36}$$

$$V_{D1} = 0 \tag{3.37}$$

$$V_0 = V_{C1} - v_{L2} = V_{C1} + V_{C2} \tag{3.38}$$

During the shoot-through state; we have

$$V_{L1} = V_{C2} + V_{DC} \tag{3.39}$$

$$V_{L2} = V_{C1} \tag{3.40}$$

$$V_{D1} = V_{C1} + V_{C2} \tag{3.41}$$

$$V_0 = 0 \tag{3.42}$$

At steady state, the average inductor voltage is zero. Thus,

$$V_{L1} = \frac{T_0(V_{C2}+V_{DC})+T_1(V_{in}-V_{C1})}{T} \tag{3.43}$$

$$V_{L2} = \frac{T_0(V_{C1})+T_1(-V_{C2})}{T} \tag{3.44}$$

From Eqs. (3.41) and (3.43), the capacitor voltages are

$$V_{C1} = \frac{T1}{T1-T0} V_{DC} \tag{3.45}$$

$$V_{C2} = \frac{T0}{T1-T0} V_{DC} \tag{3.46}$$

Finally the peak dc link voltage over the inverter bridge is

$$V_o = V_{C1} + V_{C2} = \frac{T}{T1-T0} V_{DC} = 1 = \frac{1}{1-2\frac{T_0}{T}} V_{DC} = BV_{DC} \tag{3.47}$$

The following equations are derived for the selection of the network inductor and capacitor from the ripple equations:

$$L_1 = L_2 = \frac{V_L \Delta T}{\Delta I} = \frac{\left(1 d_{sh-th}\right) V_{in}}{I_L r_c\%} . \frac{1}{2} T_0 \tag{3.47}$$

$$C_1 = C_2 = \frac{I_C \Delta T}{\Delta(V_{C1}+V_{C2})} = 2 \frac{I_L}{BV_{DC} r_v\%} . \frac{1}{2} T_0 \tag{3.48}$$

where, r_c is the inductor's allowable current ripple ratio and r_v is the capacitors allowable voltage ripple ratio. The system equations are provided in Table 3.3.

Voltage ratios	Duty ratio effect	Current relations	Duty ratio effect
$\frac{V_{C1}}{V_{IN}}$	$\frac{1-d_{sh-th}}{1-2d_{sh-th}}$	I_{C1}	$-I_{pn}-I_{L1}$
$\frac{V_{C2}}{V_{IN}}$	$\frac{d_{sh-th}}{1-2d_{sh-th}}$	I_{C2}	$-I_{pn}-I_{L2}$
$\frac{V_{L1}}{V_{IN}}=\frac{V_{L2}}{V_{IN}}$	$\frac{d_{sh-th}}{1-2d_{sh-th}}-S_D*\frac{1}{1-2d_{sh-th}}$	$I_{L1}=I_{L2}$	$\frac{P}{V_{IN}}$
$\frac{V_{pn}}{V_{IN}}$	$\overline{S_D}*\frac{1}{1-2d_{sh-th}}\geq 0$	I_D	$I_{L1}+I_{L2}+I_{pn}$
$\frac{V_D}{V_{IN}}$	$S_D*\frac{1}{1-2d_{sh-th}}\geq 0$	I_{in}	I_{L1}

Table 3.3 Governing equations of quasi Z-source inverter [12].

3.4 Switched Inductor Z-source Network

An expansion of the Z-source dc link for buck-boost inverters, called a switched-inductor Z-source, shown in Fig.3.15, was recently proposed in [14]. In practical applications, in order to provide a high boost factor for a low-voltage dc power source, the Z-source converter operates under extreme conditions of long shoot-through zero states.

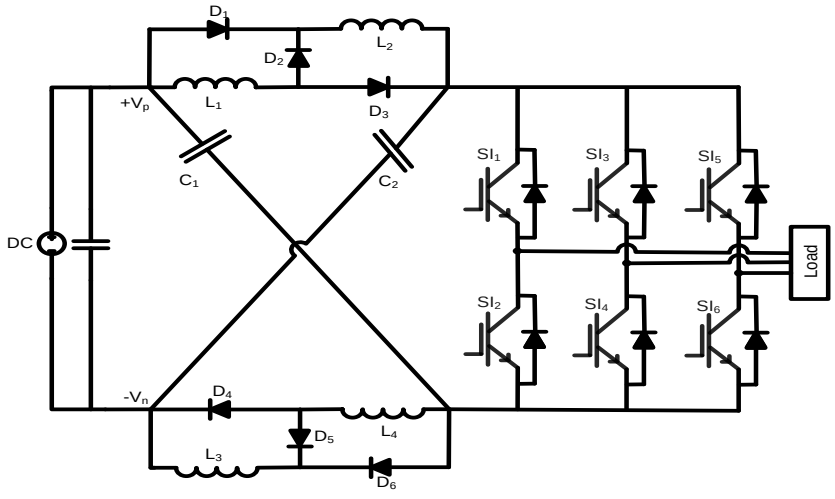


Fig. 3.15 Switched inductor Z-source

The constraints of a low modulation index and a long shoot-through state cause a conflict between the output power quality and system boost ability. Therefore, the practical boost factor of Z-source impedance network is restricted. The switched-inductor Z-source network aims at a solution of that problem. The condition of low modulation index will result in poor inversion ability at the fundamental frequency with high total harmonic distortion values, and consequently, the final ac output performance will be degraded significantly. For an optimum system design of the Z-source inverter, the practical values of modulation index must be close to unity [71], [72].

Equivalent circuits of the switched-inductor Z-source under the non-shoot-through and shoot-through conditions are shown in Fig. 3.16 (a). It illustrates situation when diodes D_2 and D_5 are on and the other ones are off. Inductors L_1 and L_2 are in series, as are inductors L_3 and L_4. Capacitors C_1 and C_2 are simultaneously charged by the rectified input voltages. In Fig.3.16 (b), the inverter is operating under the shoot-through condition to boost the output voltage. Now, diodes D_1, D_3, D_4, and D_6 are on while D_2 and D_5 are off. The parallel inductors L_1 and L_2 are charged by C_1 and L_3 and L_4 by C_2.

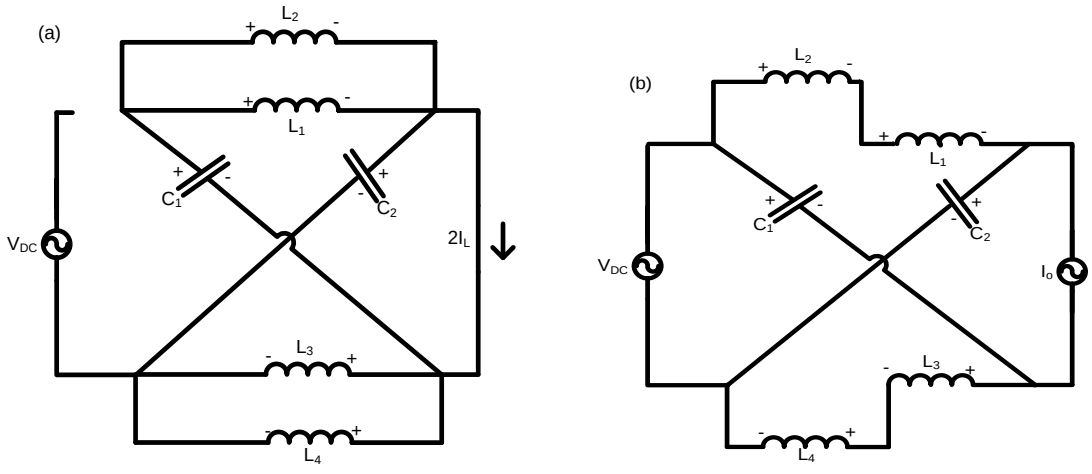


Fig. 3.16 Equivalent circuits of the switched-inductor Z-source: (a) non-shoot-through states, (b) shoot-through states.

3.4.1 Circuit Analysis

As all the inductors have the same inductance and all capacitors the same capacitance, the symmetry of the switched-inductor network yields

$$V_C = V_{C_1} = V_{C_2} \tag{3.49}$$

Similarly, in the non-shoot-through states of the converter, inductor voltages are

$$V_{l_1} = V_{l_2} = V_{l_3} = V_{l_4} = V_C \tag{3. 50}$$

In the shoot-through states, the top-side inductors and bottom-side inductors are connected in series. It can be shown that their voltages are

$$V_{l_{sh\_th}} = V_{l_1} = -\frac{d_{sh\_th}}{(1-d_{sh\_th})} V_C \tag{3.51}$$

In the non-shoot-through states, the top-side inductors and bottom-side inductors are connected in series. It can be shown that their voltages are

$$V_{l_3} = V_{C1} = V_{C2} - V_o - V_{l_1} \tag{3.52}$$

The averaged voltage of inductors over a switching period should be zero. Thus, combining Eqs. (3.51) and (3.52) gives

$$d_{sh\_th} * T_s * V_{pn} = \left(1 - d_{sh_{th}}\right) * T_s * (V_C - V_{pn} - \frac{d_{sh\_th}}{(1-d_{sh\_th})} V_C) \tag{3.53}$$

$$V_c = V_{c1} = V_{c2} = \frac{1-d_{sh\_th}}{1-3d_{sh\_th}} V_{in} \tag{3.54}$$

Then the boost factor can be found as follows:

$$V_o = \frac{1+d_{sh\_th}}{1-3d_{sh\_th}} V_{in} = BV_{in}, \quad B = \frac{1+d_{sh\_th}}{1-3d_{sh\_th}} \tag{3.55}$$

The equations of the switched inductor Z-source inverter are provided in Table 3.2.

Voltage ratios	Duty ratio effect	Current relations	Duty ratio effect
$\frac{V_o}{V_{IN}}$	$\frac{1+d_{sh-th}}{1-3d_{sh-th}}$	I_{C1}	$-I_{pn}-2I_{L1}$
$\frac{V_C}{V_o}$	$\frac{1-d_{sh-th}}{1+d_{sh-th}}$	I_o	$-I_{pn}-2I_{L2}$
$V_D = V_{in}$	1	$I_{L1} = I_{L2}$	$\frac{P}{V_{IN}}$
$\frac{V_{pn}}{V_{IN}}$	$\frac{1+d_{sh-th}}{1-3d_{sh-th}}$	I_D	$2I_{L2}+I_o$
$\frac{V_D}{V_{IN}}$	$S_D * \frac{1+d_{sh-th}}{1-3d_{sh-th}} \geq 0$	I_{in}	I_{L1}

Table 3.4 Governing equations of switched inductor Z-source inverter.

3.5 Conclusion

The chapter reviewed the major boost type inverters. The operation principles, circuit analysis and theoretical results were researched. The inverters are similar but has significant advantage over the conventional inverters. The level of boosting the voltage, lower component ratings, reduced voltage stress, reduced component count and simplified control strategies are the main comparison parameters.

A grid-connected PV power generation system is one of the most promising applications of such converters. For instance, a Z-source based PV power generation system is intended as a grid connected system and transfers the maximum power from the PV array to the grid by maximum power point tracking technology. This implies the efficiency and reduces the cost of the one stage power conversion system.

Chapter 4

Three Phase to Three Phase Matrix Converters with Z-sources

In spite of extensive research over the last two decades, matrix converters have rarely been employed in commercial products due to their complex modulation techniques, low voltage gain, and high number of semiconductor switches. Recently, sparse and ultra-sparse matrix converter topologies, often categorized as indirect matrix converters, have been proposed to reduce the switch count. To increase the voltage gain, various control algorithms and topologies was developed. One of the most effective solutions is the use of the Z-source concept. As described in [6], the Z-source network has been originally proposed as the dc link for boost voltage-source inverters. In such an inverter, the dead time is not needed, which improves the quality of output power and reliability of the converter.

Work on matrix converters has been focused on modeling and control, pulse-width modulation (PWM), applications and alternative topologies. However, Z-source matrix converters have found very limited coverage in the literature. In [40], the Z-source concept is extended on direct matrix converters, a family of Z-source matrix converters is explored, and their operating principles and characteristics are analyzed. In [11], a grid interface for wind turbine generators based on an ultra-sparse matrix converter is described. The system integrates a generator-side three-switch buck-type rectifier and a grid-side Z-source inverter. Aforementioned topologies, often designated for renewable-energy systems, integrate a source-side buck-type rectifier and a load-side inverter. The Z-source, placed in a cascade arrangement between those the rectifier and the inverter, allows boosting the voltage two to three times. It has drawbacks. Firstly the voltage across Z-source capacitors is larger than the input voltage. This require the use

of larger capacitors, which increases the overall cost and volume. Secondly, the inrush current and resonance in the Z-source network at startup are not suppressed.

We propose a three-phase/three-phase ultra-sparse matrix converter utilizing a series Z-source, quasi Z-source and switched inductor Z-source. Series Z-source, quasi Z-source and switched inductor Z-source is inserted in either rail of the indirect matrix converter. A newly developed optimal PWM technique is employed in the converters. The operating principles and comparison with the traditional topology are discussed. The novel converters constitute an improvement over the cascaded Z-source matrix converter by reducing the voltage across Z-source's capacitor limiting the inrush current at startup for series Z-source and widening the boost ratio for quasi Z-source and very high boost ratio for switched inductor Z-source matrix converter. Here, experimental results of investigation of those converters are presented to verify the effectiveness of the proposed topologies and control strategies in providing a high boosting capability. Also, the quality of input/output currents is assessed via the fast Fourier transform (FFT) analysis.

The switched-inductor Z-source inverter increases the boost factor of a classical ZSI by adding six diodes and two inductors while solving the conflict between the modulation index and shoot-through duty ratio to improve the power quality and boost ability. With the additional LC impedance network, the quasi-Z-source inverter utilizes the shoot-through states to boost the DC bus voltage by turning on both the upper and lower switches of a phase leg. This can reduce or boost the voltage to a desired level, usually higher than the available DC bus voltage.

Certain clean-energy systems, such as residential wind-power, often employ low-voltage gearless generators. The overall simplicity of proposed converters makes them viable alternatives to existing solutions [73]-[77].

4.1 Topologies

4.1.1 Series Z-source Matrix Converter

Series Z-source network, an expansion of the popular concept of Z-source dc link, was originally proposed for boosting the output voltage of power electronic inverters. In this paper, it is extended on a three-phase indirect matrix converter. The converter is based on the ultra-sparse matrix topology characterized by the minimum number of semiconductor switches. The series Z-source network is placed between the three-switch input rectifier stage and the six-switch output inverter stage in either the positive or negative rail.

The proposed converter is based on the ultra-sparse matrix topology. In the indirect-matrix topologies, the basic function of the converter is realized by splitting the ac-to-ac conversion into the ac-to-dc and dc-to-ac stages shown in Fig.4.1. The enhanced Z-source network in the latter converter forms a voltage-boosting dc link with reduced input current inrush.

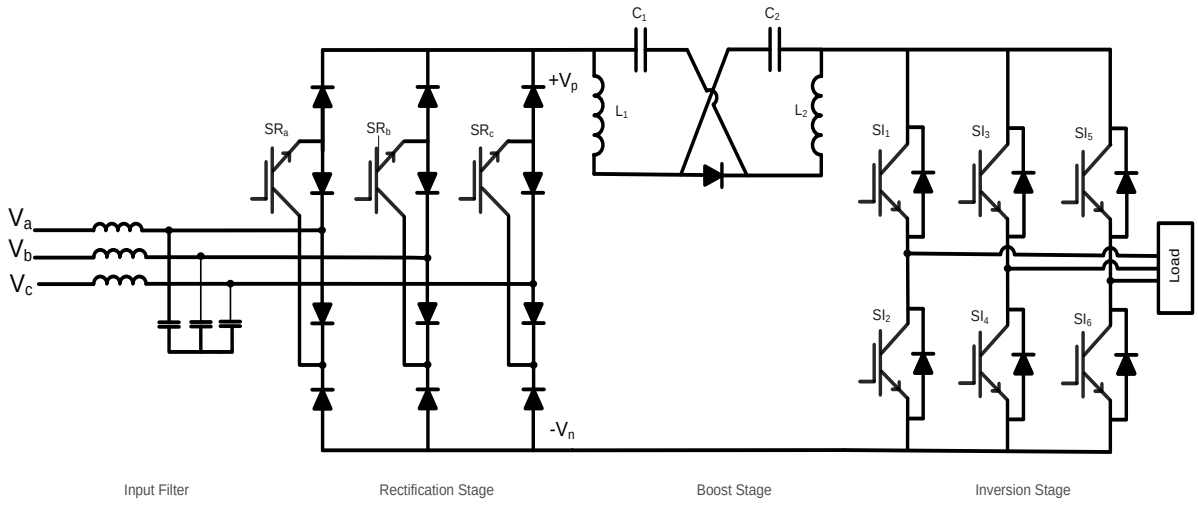


Fig. 4.1 Series Z-source matrix converter.

4.1.2 Quasi Z-source Matrix Converter

A circuit diagram of the quasi Z-source matrix converter is shown in Fig.4.2. The input stage is based on the ultra-sparse matrix converter topology and consists of three switches and twelve diodes, and it rectifies the three-phase input voltages.

The quasi Z-source network constitutes a voltage-boosting dc link based on two capacitors, two inductors and a diode. The output stage, a classic three-phase inverter, contains six switches and six diodes. Thus, not counting the blocking diode in the dc link, the converter is comprised of nine switches and eighteen diodes. For comparison, the classic three-phase to three-phase matrix converter employs nine bi-directional switches, that is, nine unidirectional switches and thirty-six diodes or eighteen switches and eighteen diodes.

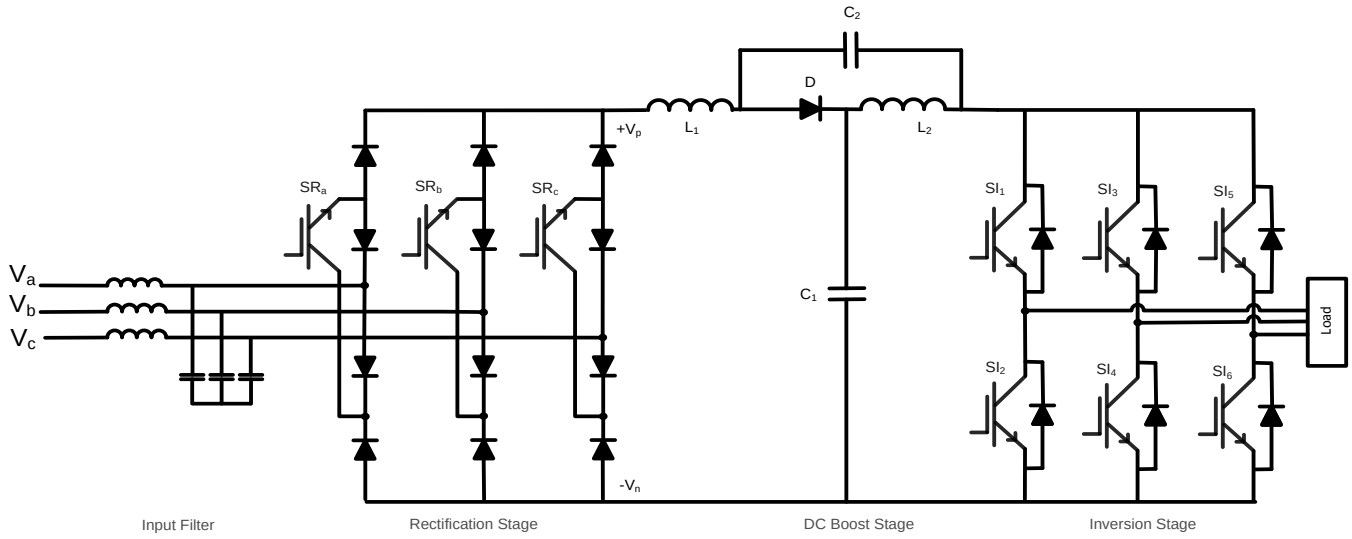


Fig. 4.2 Quasi Z-source matrix converter.

4.1.3 Switched Inductor Z-source Matrix Converter

Circuit diagrams of the switched-inductor Z-source matrix converter are shown in Fig.4.3. The main limitations of the front end rectifier stages are the unidirectional power flow and the $\pi/6$ displacement angle of the input current. The switched-inductor network constitutes

voltage-boosting DC links that including 6 diodes, four inductors and two capacitors. The output stage, a classic three-phase inverter, contains six switches and six diodes.

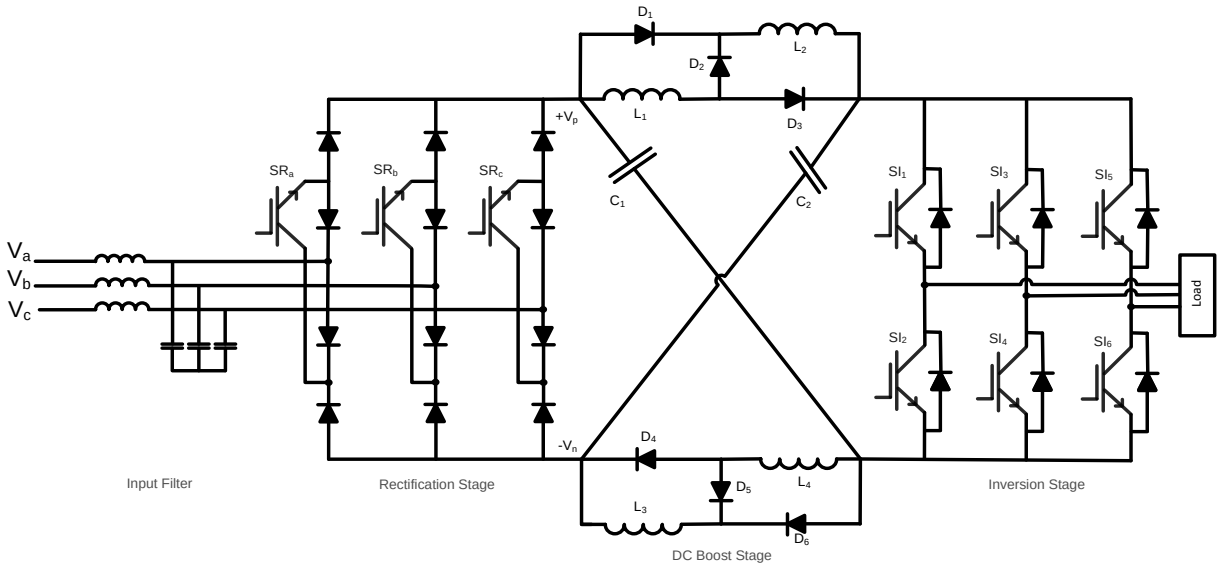


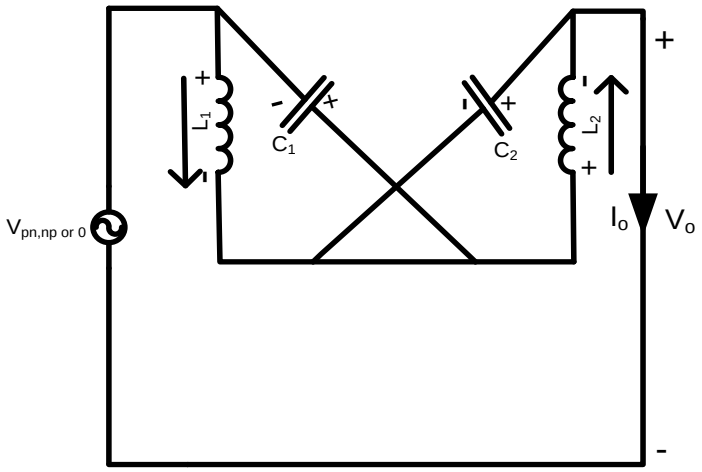
Fig. 4.3 Switched inductor Z-source matrix converter.

4.2 Operation

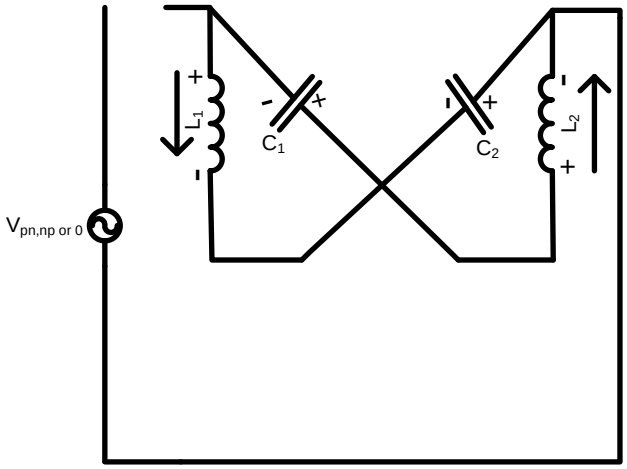
4.2.1 Series Z-source Matrix Converter

An equivalent circuit of the series Z-source, placed on the positive rail between the rectifier and inverter stages, is shown in Fig. 4.4 (a) during the non-shoot-through states and in Fig. 4.4 (b) during the shoot-through states. In the non-shoot-through states, the rectifier stage produces V_{pn}, V_{np} or zero, depending on the position of the input current vector. Capacitors C_1 and C_2 are charged by any of the rectified input voltages. In Fig. 4.4 (b) the inverter is operating under the shoot-through condition to provide the voltage boost.

The duration of the shoot-through state depends on the desired voltage boost factor. Due to the reverse-biased rectifier diodes, the coupling between the rectifier and inverter stages is broken. Inductor L_1 is charged from C_1 and inductor L_2 from C_2.



(a)



(b)

Fig. 4.4 Top to bottom (a) non-shoot-through states (b) shoot-through states.

When there is no shoot-through, capacitor voltages are zero. When the converter is in the soft starting stage, capacitor voltages increase gradually, which reduces the excessive inrush current.

4.2.2 Quasi Z-source Matrix Converter

Fig.4.5 (a) illustrates situation when diode D_1 is on. Capacitors C_1 and C_2 are simultaneously charged by the rectified input voltages. In Fig.4.5 (b), the inverter is operating under the shoot-through condition, boosting the output voltage and diode D_1 is off.

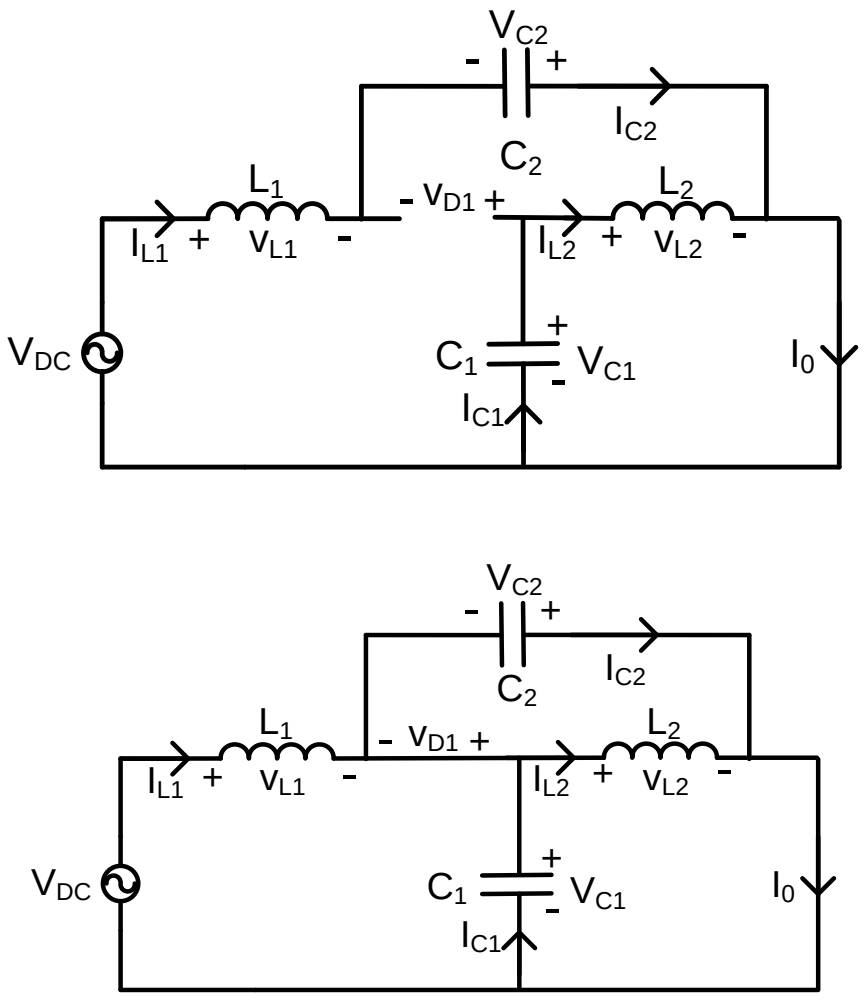
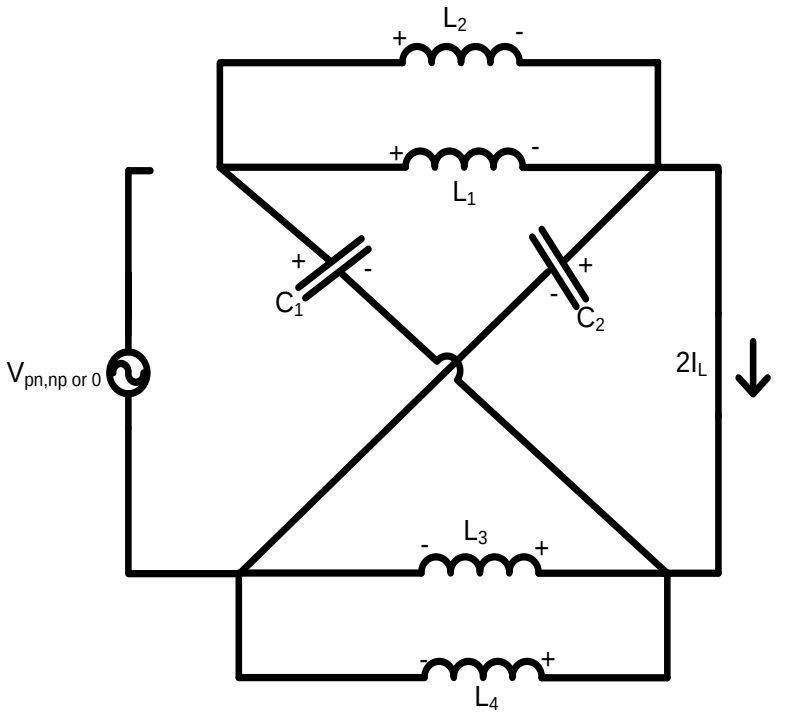


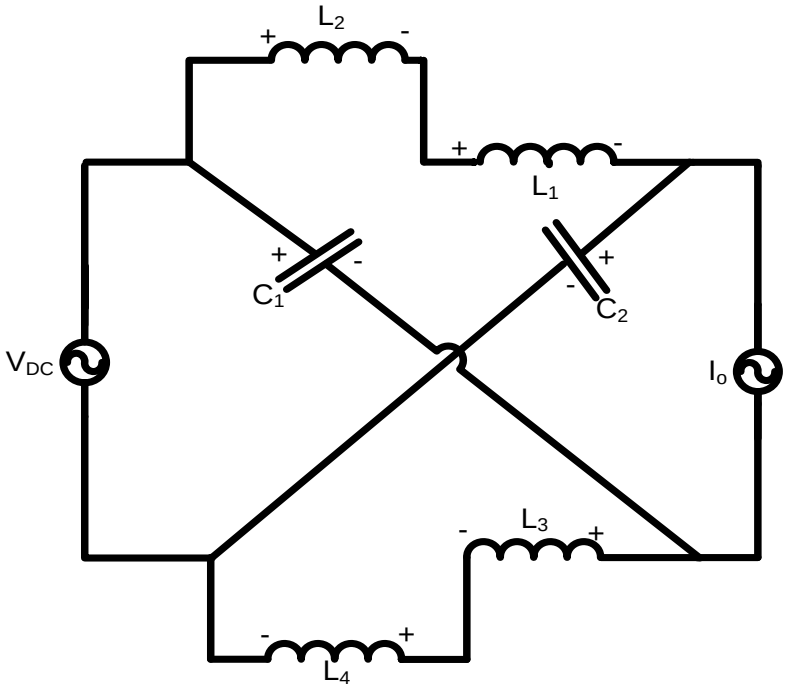
Fig. 4.5 (a) shoot-through states (b) non-shoot-through states.

4.2.3 Switched Inductor Z-source Matrix Converter

Equivalent circuits of the switched-inductor Z-source under the non-shoot-through and shoot-through conditions are shown in Fig.4.6. Fig.4.6 (a) illustrates the situation when diodes D_2 and D_5 are on and the other ones are off. Inductors L_1 and L_2 are in series, as are inductors L_3 and L_4. Capacitors C_1 and C_2 are simultaneously charged by the rectified input voltages. In Fig.4.6 (a), the inverter is operating under the shoot-through condition to boost the output voltage. Now, diodes D_1, D_3, D_4, and D_6 are on while D_2 and D_5 are off. The parallel inductors L_1 and L_2 are charged by C_1 and L_3 and L_4 by C_2.



(a)



(b)

Fig. 4.6 The equivalent circuits are (a) shoot-through states (b) non-shoot-through states.

4.3 Circuit Analysis

4.3.1 Series Z-source Matrix Converter

Considering that all the inductors have the same inductance and all capacitors the same capacitance, the symmetry of the series Z-source network yields

$$V_C = V_{C_1} = V_{C_2}, \quad V_L = V_{L1} = V_{L2} \tag{4.1}$$

In the shoot-through states, as the inverter side is shorted, inductor voltages are

$$V_L = V_C + V_{vir} \tag{4.2}$$

Here, V_{vir} is the virtual dc link voltage (V_{pn}, V_{np}, or 0) produced by the rectification stage. In the non-shoot-through states of the converter, inductor voltages are

$$V_L = -V_c \tag{4.3}$$

Applying the volt-second balance principle to inductor voltages yields

$$d_{sh-th} * T_s * (V_{vir} + V_c) + (1 - d_{sh-th}) * T_s * (-V_c) = 0 \tag{4.4}$$

where T_s is the switching period and d_{sh_th} is the shoot-through duty ratio. Therefore,

$$V_c = \frac{d_{sh-th}}{1-2d_{sh-th}} V_{vir} \tag{4.5}$$

From this deviation, we can see that in the series Z-source matrix converter, when the shoot-through duty ratio is zero, the Z-source capacitor voltage is zero. When the converter is in the soft starting stage, V_c is zero naturally, so if we control d_{sh-th} to increase gradually from zero, V_c can increase from zero gradually and soft start can be achieved.

In the non-shoot-through state, the KVL in the closed loop can be written as

$$V_{dc} = V_{vir} + V_c - V_L \tag{4.6}$$

where V_{dc} is the voltage at the output of the Z-source network. This voltage is the input of the inversion stage. Finally, the boost factor, *B*, can be calculated using Eqs. (4.3), (4.5), (4.6), and the following equation

$$V_{dc} = \frac{1}{1-2d_{sh-th}} V_{vir} = BV_{vir} \tag{4.7}$$

Summarizing the results, the average value of capacitor voltages, V_c

$$V_c = \frac{1-d_{sh-th}}{1-2d_{sh-th}} V_{vir} \tag{4.8}$$

and the boost factor is given by

$$B = \frac{1}{1-2d_{sh-th}} \tag{4.9}$$

The fundamental component of the output voltage, $\hat{V}_{out}$, for the matrix converters under consideration can be written as

$$\hat{V}_{out} = \frac{1}{\sqrt{3}} m_v B V_{vir} \tag{4.10}$$

where m_v is the voltage modulation index.

Neglecting the power losses in the rectification stage, the input power, P_{in}, can be assumed equal to the output power of the front side of the matrix converters. Thus,

$$P_{vir} = P_{in} \Rightarrow V_{vir} I_{vir} = 3V_{in} I_{in} cos\phi_i = \frac{3}{2} \hat{V}_{in} \hat{I}_{in} cos\phi_i \tag{4.11}$$

Here, P_{vir}, and I_{vir} are the output power and current of the rectification stage, respectively, $\hat{V}_{in}$ and $\hat{I}_{in}$ are the fundamental components of the input current and voltage, respectively, and ϕ_i is the desired input current displacement angle. For unity power factor,ϕ_i should be zero.

The rectifier stage modulates the input current with a modulation index, m_c, defined as

$$m_c = \frac{\hat{I}_{in}}{I_{vir}} \tag{4.12}$$

From Eqs. (4.11) and (4.12),

$$V_{vir} = \frac{3}{2} m_c \hat{V}_{in} cos\phi_i \tag{4.13}$$

and substituting Eq. (4.13) in Eq. (4.10) yields,

$$\hat{V}_{out} = \frac{\sqrt{3}}{2} m_v m_c B \hat{V}_{in} \cos(\varphi_i) \tag{4.14}$$

Eq. (4.14) describes the relation between the output and input voltages of the proposed matrix converters. The shoot-through duty ratio cannot be greater than the voltage modulation index, so for the maximum boosting the following two rules are obeyed in the switching strategy

$$m_c = 1, d_{sh-th} = 1 - m_v \text{ and } \varphi_i = 0 \tag{4.15}$$

4.3.2 Quasi Z-source Matrix Converter

A similar analysis as that of the series Z-source network can be carried out for the quasi Z-source network. Summarizing the results, the average values of capacitor voltages V_{C1} and V_{C2} in the quasi-Z-source network are:

$$V_{C_1} = \frac{1-d_{sh-th}}{1-2d_{sh-th}} V_{vir} \tag{4.16}$$

$$V_{C_2} = \frac{d_{sh-th}}{1-2d_{sh-th}} V_{vir} \tag{4.17}$$

and the boost factor is given by

$$B = \frac{1}{1-2d_{sh-th}} \tag{4.18}$$

The fundamental component of the output voltage, $\hat{V}_{out}$, for the matrix converters under consideration can be written as

$$\hat{V}_{out} = \frac{1}{\sqrt{3}} m_v B V_{vir} \tag{4.19}$$

where m_v is the voltage modulation index. Neglecting the power losses in the rectification stage, the input power, P_{in}, can be assumed equal to the output power of the front side of the matrix converters. Thus,

$$P_{vir} = P_{in} \Rightarrow V_{vir} I_{vir} = 3 I_{in} V_{in} \cos(\varphi_i) = \frac{3}{2} \hat{I}_{in} \hat{V}_{in} \cos(\varphi_i) \tag{4.20}$$

Here, P_{vir}, and I_{vir} are the output power and current of the rectification stage, respectively, $\hat{V}_{in}$ and $\hat{I}_{in}$ are the fundamental components of the input current and voltage, respectively, and φ_i is the desired input current displacement angle. For unity power factor, φ_i should be zero.

From Eqs. (4.19) and (4.20),

$$V_{vir} = \frac{3}{2} m_c \hat{V}_{in} \cos(\varphi_i) \tag{4.21}$$

and substituting Eq. (4.21) in Eq. (4.19) yields,

$$\hat{V}_{out} = \frac{\sqrt{3}}{2} m_v m_c B \hat{V}_{in} \cos(\varphi_i) \tag{4.22}$$

4.3.3 Switched Inductor Matrix Converter

Considering all the inductors have the same inductance and all capacitors the same capacitance, the symmetry of the switched-inductor network yields

$$V_C = V_{C_1} = V_{C_2} \tag{4.23}$$

In the shoot-through state, voltage across L_1 is equal to V_c. Applying the volt-second balance principle, voltage across L_1 in the non-shoot-thorough state can be found as

$$V_{L_1} = -\frac{d_{sh-th}}{1-d_{sh-th}} V_C \tag{4.24}$$

where d_{sh-th} is the shoot-through duty ratio.

Applying the volt-second balance principle to L_2 yields

$$d_{sh-th} * T_s * V_C = (1 - d_{sh-th}) * T_s * \ (V_C - V_{vir} + V_{L_1}) \tag{4.25}$$

where T_s is the switching period. Substituting (4.24) in (4.25) gives

$$d_{sh-th} * T_s * V_C = (1 - d_{sh-th}) * T_s * \ (V_C - V_{vir} - \frac{d_{sh-th}}{1-d_{sh-th}} V_C) \tag{4.26}$$

Therefore, the capacitance voltage is

$$V_c = \frac{1-d_{sh-th}}{1-3d_{sh-th}} V_{vir} \tag{4.27}$$

In the non-shoot-through state, the KVL in the closed loop can be written as

$$V_c = V_{dc} + V_{L_1} + V_{L_2} \tag{4.28}$$

where V_{dc} is the voltage at the output of the switched inductor Z-source network. This voltage is the input of the inversion stage. Finally, the boosting factor, *B*, can be calculated from the following equation:

$$V_{dc} = \frac{1+d_{sh-th}}{1-3d_{sh-th}} V_{vir} = BV_{vir} \tag{4.29}$$

As in the other two proposed converters, Eq. (4.22) is valid for switched inductor Z-source matrix converter.

4.4 Design of Passive Components

The traditional matrix converter is often referred to as an all silicon solution to the ac-ac power conversion. In addition to the network components in boost matrix converters, there are other passive elements, mainly input filter needed to realize the matrix converter. Furthermore, an optional overvoltage clamp circuit is desirable as well, but it increases the number of reactive elements in the overall topology.

4.4.1 Input Current Filter

For the proposed converters, the load is assumed to be inductive, that is, of the current-source type. For the highest possible boost ratio converters are controlled to achieve a high input power factor. If $\cos(\varphi_i) = 1$ then the grid supplies to the load only the active power. The commutation of matrix converters requires a capacitor bank near the input terminals. This can decouple the line inductance from the commutation circuit and the leakage inductance can cause problem during commutation. The input capacitors along with the inductors form a second-order filter for the input current. To assure the appropriate low cut-off frequency an additional inductance must be inserted in series with the line inductors.

As shown in the proposed converters, the filter capacitors are Y-connected to virtual neutral point. This connection is preferable to the delta connected capacitors, because of the resultant reduction of voltage ratings of the capacitors. The total input inductance in the filter is the line inductance and filter inductance. For the minimum loss in the filter and the cost efficiency, the filter components should be minimized.

The performance of the input filter is mainly evaluated from the input voltage frequency. Due to the capacitors, the filter draws reactive currents. This current is determined as:

$$I_o = \frac{V_{IN}}{X_T} = \frac{V_{IN}}{j(L_F w_{in} - 1/C_F w_{in})} \cong jV_{in} w_{in} C_F \tag{4.30}$$

where I_o is the no load current, X_T is the total impedance, V_{IN} is the input voltage and w_{in} is the angular frequency of the input voltages. The approximation neglects the voltage drop across the inductors due the no load current.

The fundamental component of the current drawn by the proposed converters I_{in} is determined by the output power of the converter and the input voltage level. With another approximation here, considering the lossless converters:

$$I_{in} \cong \frac{P_{out}}{3(V_{in} - L_F w_{in} I_{in})} = \frac{\pm 3V_{in} + \sqrt{9{V_{in}}^2 - 4L_F w_{in} P_{out}}}{-2L_F w_{in}} \tag{4.31}$$

where P_{out} is the output power of the converter. The total input current of the converter and the filter is the no load current and the active current drawn from the converter

$$I_{inT} = I_{in} + I_o = \frac{\pm 3V_{in} + \sqrt{9{V_{in}}^2 - 4L_F w_{in} P_{out}}}{-2L_F w_{in}} + jV_{in} w_{in} C_F \tag{4.32}$$

Eq. (4.31) shows that the input current has a leading phase angle and a constant reactive current decided by the choice of the filter capacitor. The active part of the current is determined by the output power. The choice of the capacitors depends upon the rated power of the converter [76]. From Eq. (4.32), the phase angle can be calculated as

$$\varphi_i = \tan^{-1}\left[\frac{I_o}{I_{in}}\right] \tag{4.33}$$

and the capacitance is

$$C_F \cong \frac{P_{out}\tan\varphi_i}{3{V_{in}}^2 w_{in}} \tag{4.34}$$

The choice of inductance should be linked to the chosen capacitor by the desired capacitor cut-off frequency of the filter. The filter design is a compromise between the inductor and the capacitor design. A small capacitor assures high $\cos(\varphi_i)$ but requires a large inductor to ensure an appropriate cut-off frequency. The size of the inductor is limited by the input voltage drop [19].

4.4.2 Network Components

Based on the circuit analysis, the average current through the inductor equals that of the rectifier in the steady state. Therefore, the average current through the rectifier and inductor is

$$I_L = \frac{P_{out}}{V_{vir}} = \frac{P_{out}}{\left(\frac{3}{2}\right)\widehat{V}_{in}cos\phi_i} \tag{4.35}$$

The Z-source network capacitor value is selected according to the desired voltage ripple and the capacitor current. During the shoot-through the network inductor current flows through the capacitors and discharges them. Therefore, the voltage ripple across the capacitors can be expressed as

$$\Delta V_C = \frac{I_L}{C}.d_{sh-th}.T_s \tag{4.36}$$

If ΔV_C is selected as $\Delta V_C \leq k_v\%V_C$, then

$$C \geq \frac{d_{sh-th}T_s}{k_v\%V_C} I_L = \frac{(1-2d_{sh-th})T_s}{k_v\%V_{vir}} I_L \tag{4.37}$$

Substituting Eq. (4.35) into Eq. (4.37) yields,

$$C \geq \frac{(1-2d_{sh-th})d_{sh-th}T_s}{2.25\times(1-d_{sh-th})k_v\%V_{in}^2\cos^2\phi_i} P_{out} \tag{4.38}$$

The network inductor value is selected with respect to a specified current ripple. During the non-shoot-through state, the network inductor current decreases, and the inductor voltage equals the Z-source capacitor voltage; therefore, the inductor current ripple can be expressed as

$$\Delta I_L = \frac{V_C}{L}.(1-d_{sh-th}).T_s \tag{4.39}$$

If ΔI_L is selected as $\Delta I_L \leq k_i\%I_L$, then

$$L \geq \frac{(1-d_{sh-th})T_s}{k_i\%I_L} V_C = \frac{d_{sh-th}(1-d_{sh-th})T_S}{(1-2d_{sh-th})k_i\%I_L} V_{vir} \tag{4.40}$$

$$L \geq 2.25\frac{d_{sh-th}(1-d_{sh-th})T_S}{(1-2d_{sh-th})k_i\%P_{out}} V_{in}^2\cos^2\phi_i \tag{4.41}$$

The presented analysis has been done for the series Z-source matrix converter. Similar analyses can be carried out for the all the other network. The inductor current ripple can be the same in these topologies. However, the capacitor value should be selected individually, due to the different capacitor voltages between the topologies.

4.5 Switching Strategy

Control of the Z-source matrix converters is based on the combined space vector rectification (SVR) and space vector inversion (SVI) pulse width modulation techniques. The control strategy for the front end rectifier is shown in Fig. 4.7. Switches of the rectifier are controlled using the SVR technique. Regarding the input-current vectors shown in Fig. 4.7, a reference angle is in the first sextant, so S_{Ra} must be turned on at all times, S_{Rb} and S_{Rc} must be turned on and off to draw sinusoidal input currents. Only two switches are turned on simultaneously. Location of the reference vector within one of the sextants defines the framing vectors I_λ and I_δ as seen in Fig. 4.8. For example, in Fig. 4.7 the current reference angle is in the first sextant.

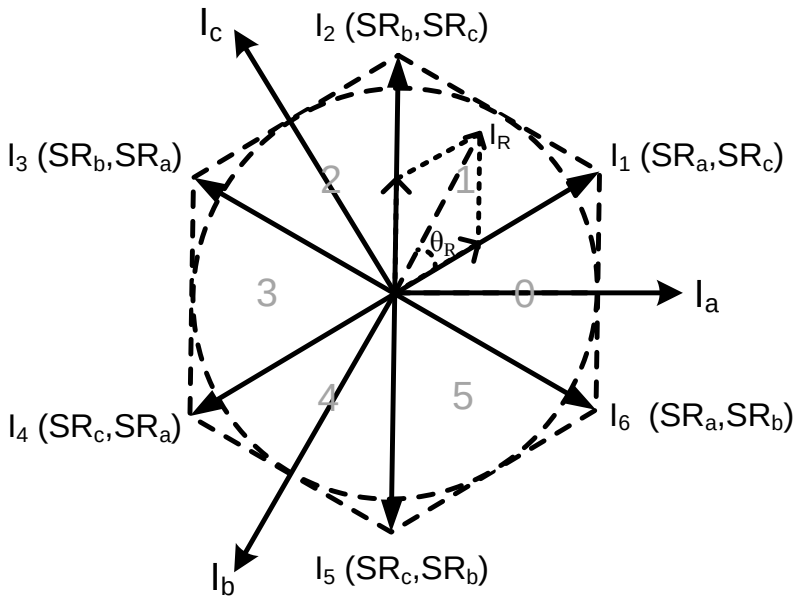


Fig. 4.7 Diagram of input-current space vectors.

The reference current vector is synthesized from the adjacent vectors and a zero vector. Denoting the local angle of the reference current by θ_R, the duty ratios of the active, d_λ, d_δ and zero, d_{0R}, vectors are calculated from the classic formulas for space vector PWM:

$$d_\lambda = m_c \sin\left(\frac{\pi}{3} - \theta_R\right) \tag{4.42}$$

$$d_\delta = m_c \sin(\theta_R) \tag{4.43}$$

$$d_{0R} = 1 - (d_\lambda + d_\delta) \tag{4.44}$$

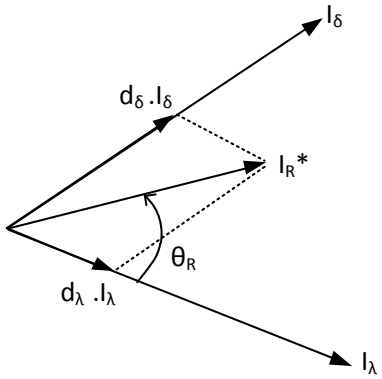


Fig. 4.8 Reference input-current space vector with the adjacent vectors.

The back-end inverter switches are controlled using the SVI technique. Fig. 4.9 shows the output-voltage vectors where symbols *p* and *n* refer to the upper and lower switches of the inverter. For example, *pnn* means that the upper switch in branch A and the lower switches in branches B and C are turned on, while *ppn* indicates that the upper switches in branch A and B and the lower switch in branch B are on. The back-end inverter utilizes two zero voltage vectors, six active voltage vectors, and one shoot-through state, which is forbidden in conventional matrix converters and inverters.

The location of the reference vector within one of the sextants defines the framing vectors V_α and V_β, as illustrated in Fig. 4.10. For example, in Fig. 4.9, the reference vector of output voltage is in the zero sextant.

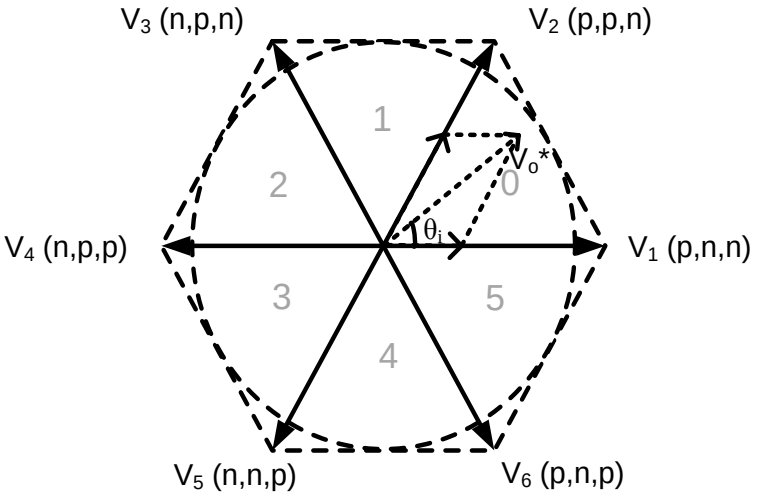


Fig. 4.9 Diagram of output voltage space vectors.

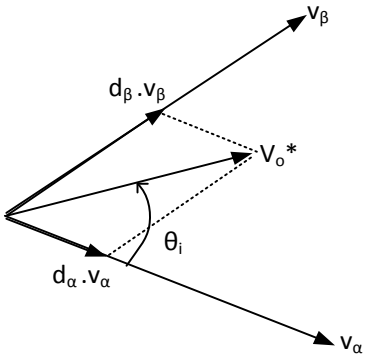


Fig. 4.10 Reference output voltage space vector with the adjacent vectors.

The modulation of the active vectors decides the angular position of the averaged output voltage vector, while a zero vector is employed to adjust its magnitude. The reference vector of output voltage is defined as

$$\vec{V}_o^* = V_{out} e^{j\omega_o t} \tag{4.45}$$

where V_{out} is the desired output line voltage and ω_o is the output radian frequency.

Denoting the local (in-sextant) angle of the reference voltage by θ_i, the duty ratios of the active, d_α, d_β and zero, d_{0i}, vectors are calculated as:

$$d_\alpha = m_v \sin\left(\frac{\pi}{3} - \theta_i\right) \tag{4.46}$$

$$d_{\beta} = m_v \sin(\theta_i) \tag{4.47}$$

$$d_{sh-th} = \begin{cases} (B-1)/\,(3B+1) & for\ SIZMC \\ (B-1)/(2B) & for\ QZMC, SZMC \end{cases} \tag{4.48}$$

$$d_{0i} = 1 - \left(d_{\alpha} + d_{\beta} + d_{sh-th}\right) \tag{4.49}$$

The values of m_v and $d_{sh\text{-}th}$ are dependent. If m_v is set close to one, then the voltage gain approaches zero because of the limited zero vectors. The time-averaged power outputs from the three-switch rectifying stage and the inverter stage are equal. This allows combining the two modulation strategies. Assuming the input displacement angle of zero (unity power factor), the combined duty ratios are given by

$$d_{\lambda\alpha} = m_c m_v \sin\left(\frac{\pi}{3} - \theta_R\right) \sin\left(\frac{\pi}{3} - \theta_i\right) \tag{4.50}$$

$$d_{\lambda\beta} = m_c m_v \sin\left(\frac{\pi}{3} - \theta_R\right) \sin(\theta_i) \tag{4.51}$$

$$d_{\delta\alpha} = m_c m_v \sin(\theta_R) \sin\left(\frac{\pi}{3} - \theta_i\right) \tag{4.52}$$

$$d_{\delta\beta} = m_c m_v \sin(\theta_R) \sin(\theta_i) \tag{4.53}$$

The switching ratios are then calculated as

$$\begin{Bmatrix} T_{\lambda\alpha} \\ T_{\delta\alpha} \\ T_{\lambda\beta} \\ T_{\delta\beta} \end{Bmatrix} = \frac{T_s}{2} \begin{Bmatrix} d_{\lambda\alpha} \\ d_{\delta\alpha} \\ d_{\lambda\beta} \\ d_{\delta\beta} \end{Bmatrix} \tag{4.54}$$

where $$T_{sh-th} = T_s * d_{sh-th} \tag{4.55}$$

Typically for the space vector modulation, selection of zero vectors in the sequence is important for minimization of the number of switchings and the related switching losses. For the minimum switching number, the following rules must be applied

(1) The rectifier modulation follows the $T_\lambda T_\delta T_o T_{sh-th}$ sequence.

(2) For an even-number sextant, the output zero vector is 000. Otherwise, it is 111. In this sequence, zero vectors are combined and applied in any order. There is no need to calculate the duty ratios of zero vectors, which saves microprocessor's memory.

(3) Shoot-through is executed in the complementary switch x the same leg, where $x = mod(y, 6)$ for an even-number sextant, and $x = mod((y + 2), 6)$ for an odd-number sextant. Here, "y" is the sextant number and "mod" is an operator that yields the residual of y over 6. For example, if the output sextant is 5, then $x = mod\big((5 + 2), 6\big) = 1$. Therefore, the switch in which the shoot-through occurs is the complementary switch in the same leg, that is, $SI2$. If the output sextant is 4, then $x = mod(4,6)$. Therefore, the switch with the shoot-through is the one opposite to $SI4$, which is $SI3$. If the output voltage space vector is in sector 0, i.e., $y = 0$, then $x = 0$ and the switch in which shoot-through is executed is $SI5$.

Even though the indirect modulation scheme tends to decouple the input current and output voltage modulation, this is true if considering the fundamental components. The input displacement angle affects the switching waveforms of the output voltage and thus the output voltage modulation quality.

Figs. 4.11 through 4.17 show the possible switching of the power switches within the one full cycle of the any phase voltage. Figs.4.18 through 4.27 show an example switching sequence for a one switching cycle (T_s) of Fig. 4.11 for the all converters considered.

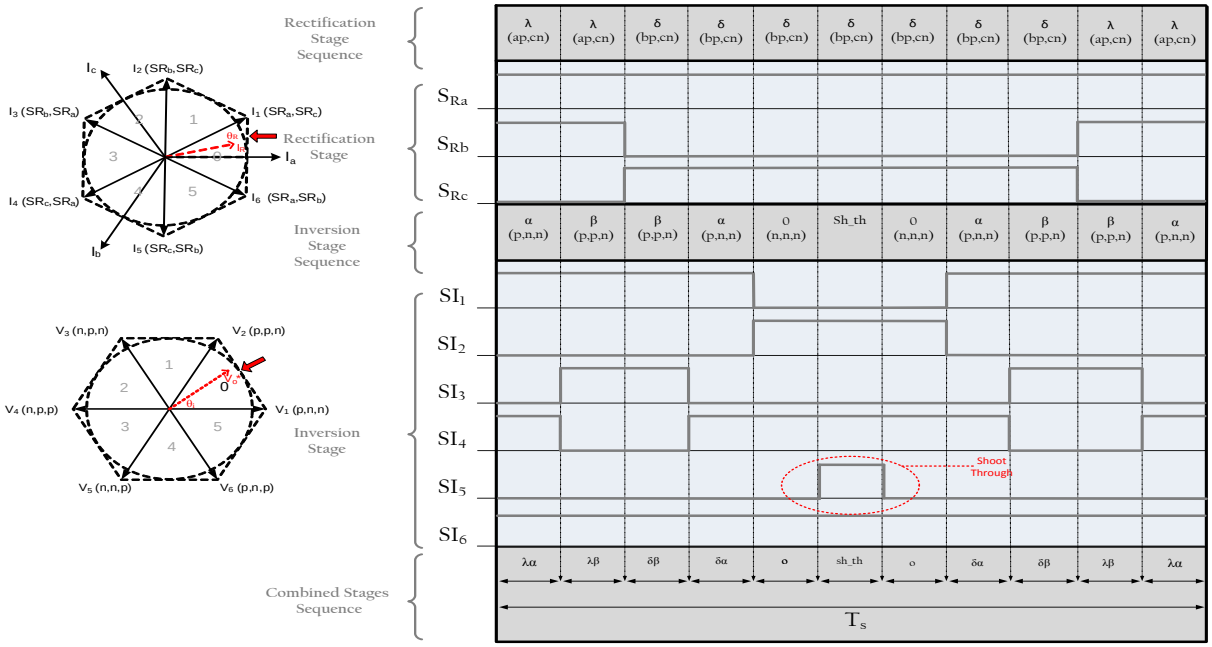


Fig. 4.11 Switching signals and sequences. Top to bottom: rectification stage (input-current space vector in sector 0), inversion stage (output voltage space vector in sector 0).

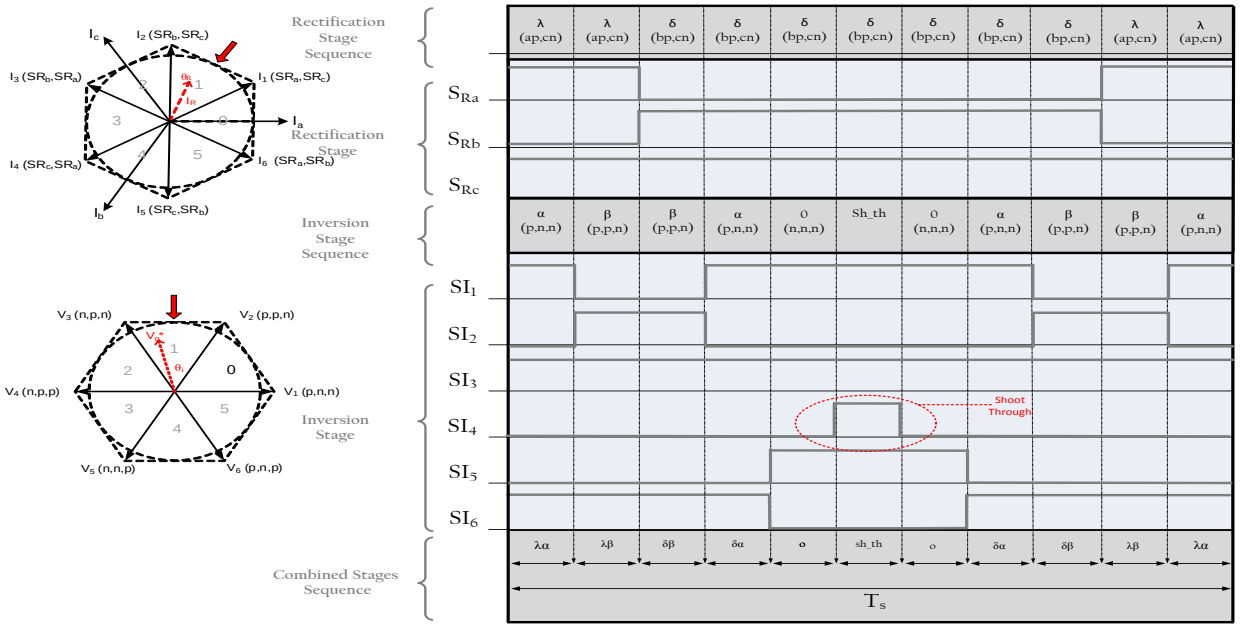


Fig. 4.12 Switching signals and sequences. Top to bottom: rectification stage (input-current space vector in sector 1), inversion stage (output voltage space vector in sector 1).

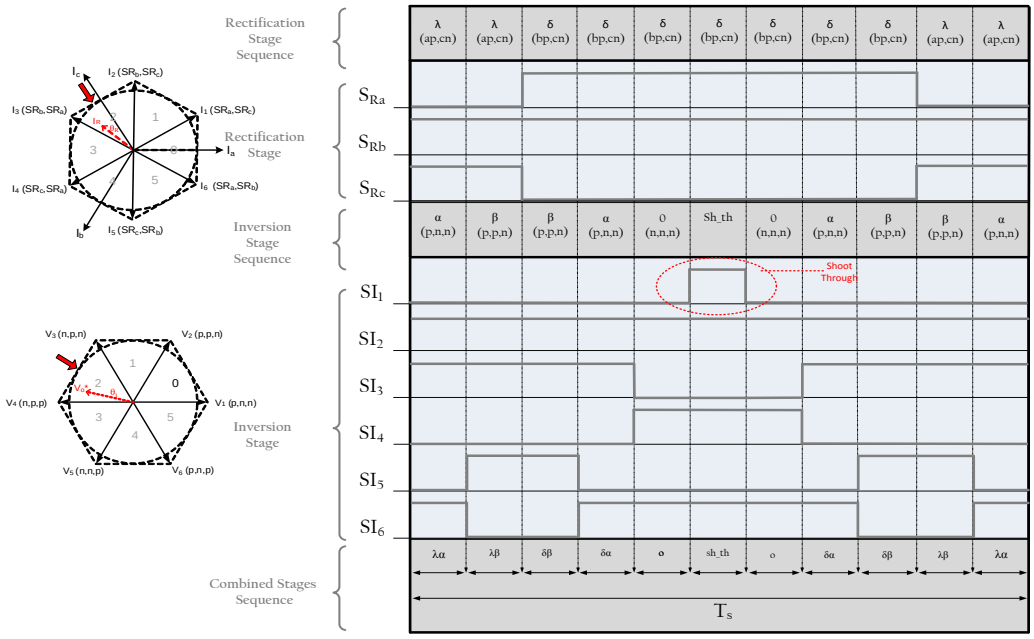


Fig. 4.13 Switching signals and sequences. Top to bottom: rectification stage (input-current space vector in sector 2), inversion stage (output voltage space vector in sector 2).

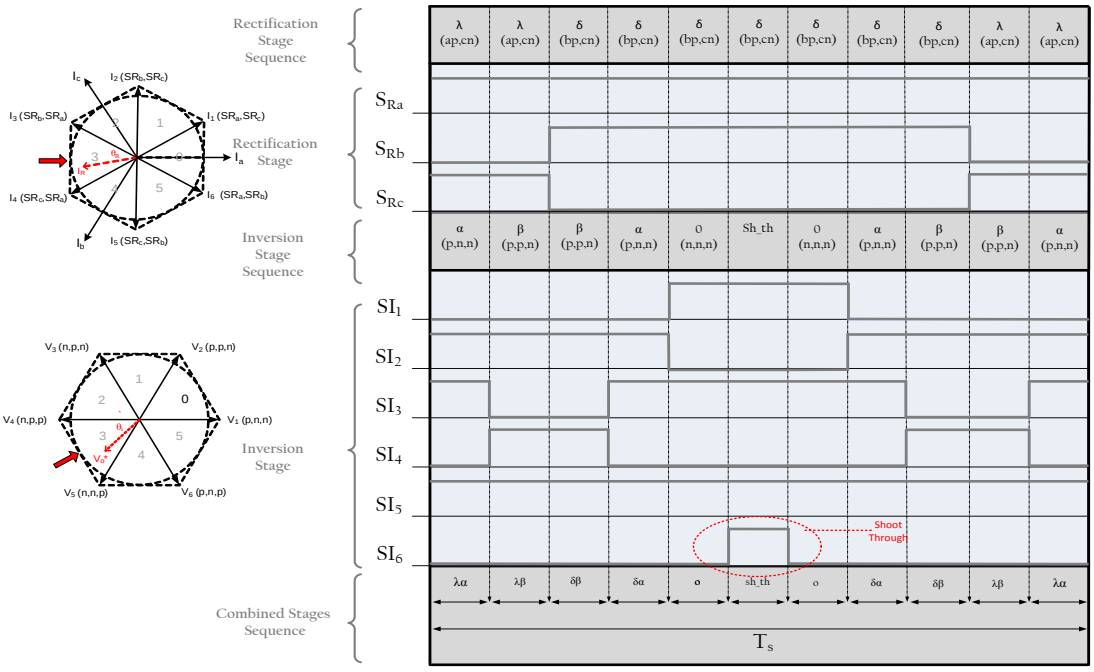


Fig. 4.14 Switching signals and sequences. Top to bottom: rectification stage (input-current space vector in sector 3), inversion stage (output voltage space vector in sector 3).

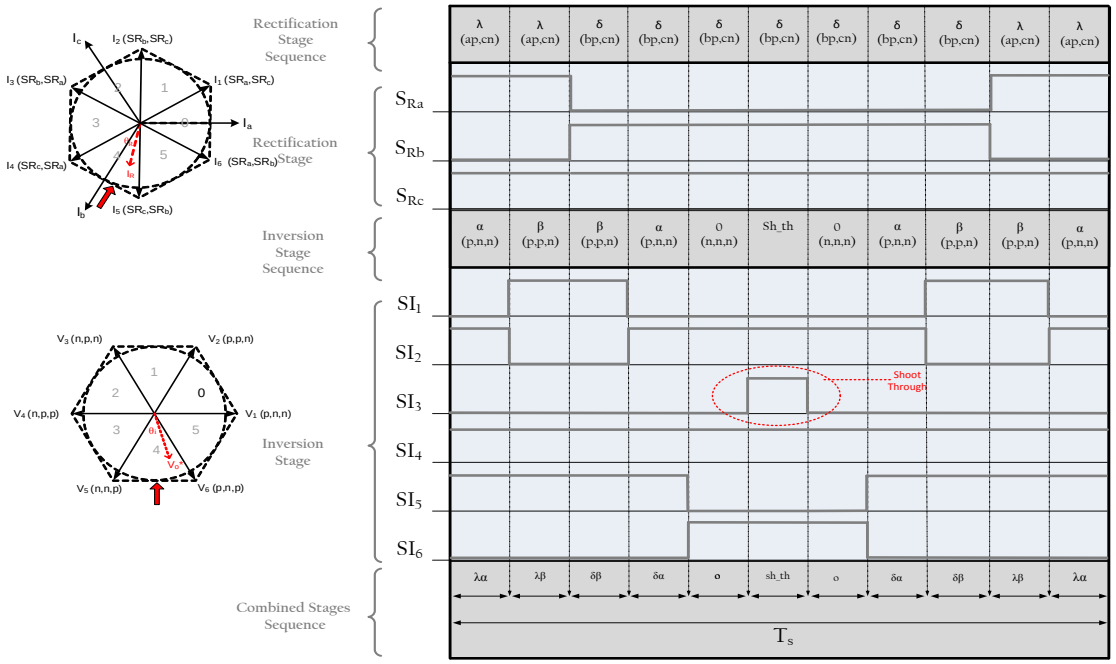


Fig. 4.15 Switching signals and sequences. Top to bottom: rectification stage (input-current space vector in sector 4), inversion stage (output voltage space vector in sector 4).

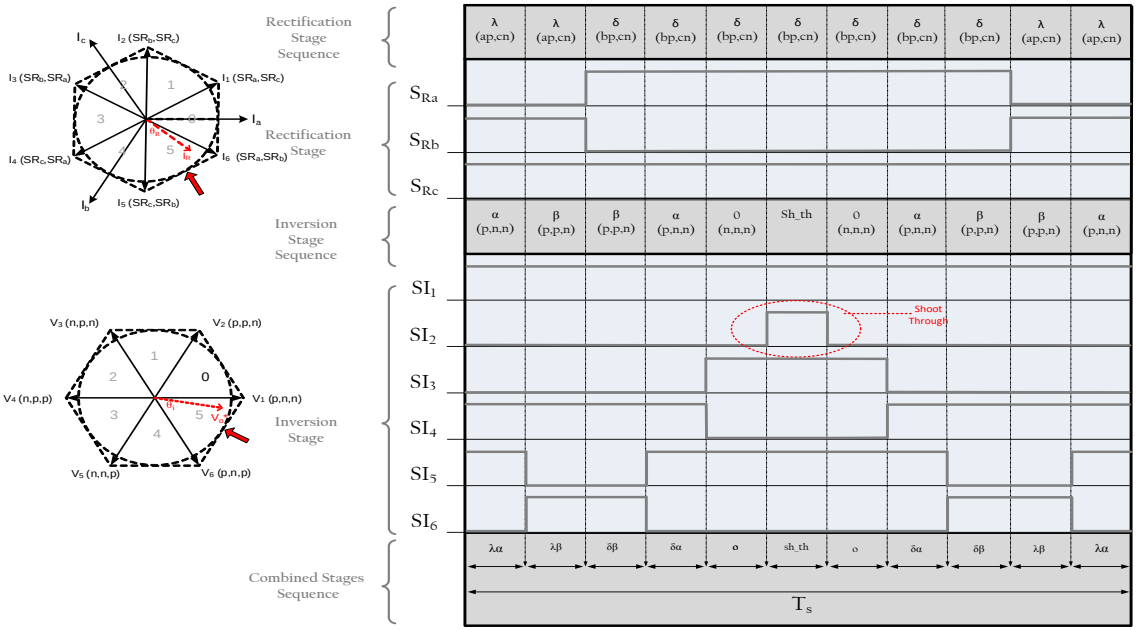


Fig. 4.16 Switching signals and sequences. Top to bottom: rectification stage (input-current space vector in sector 5), inversion stage (output voltage space vector in sector 5).

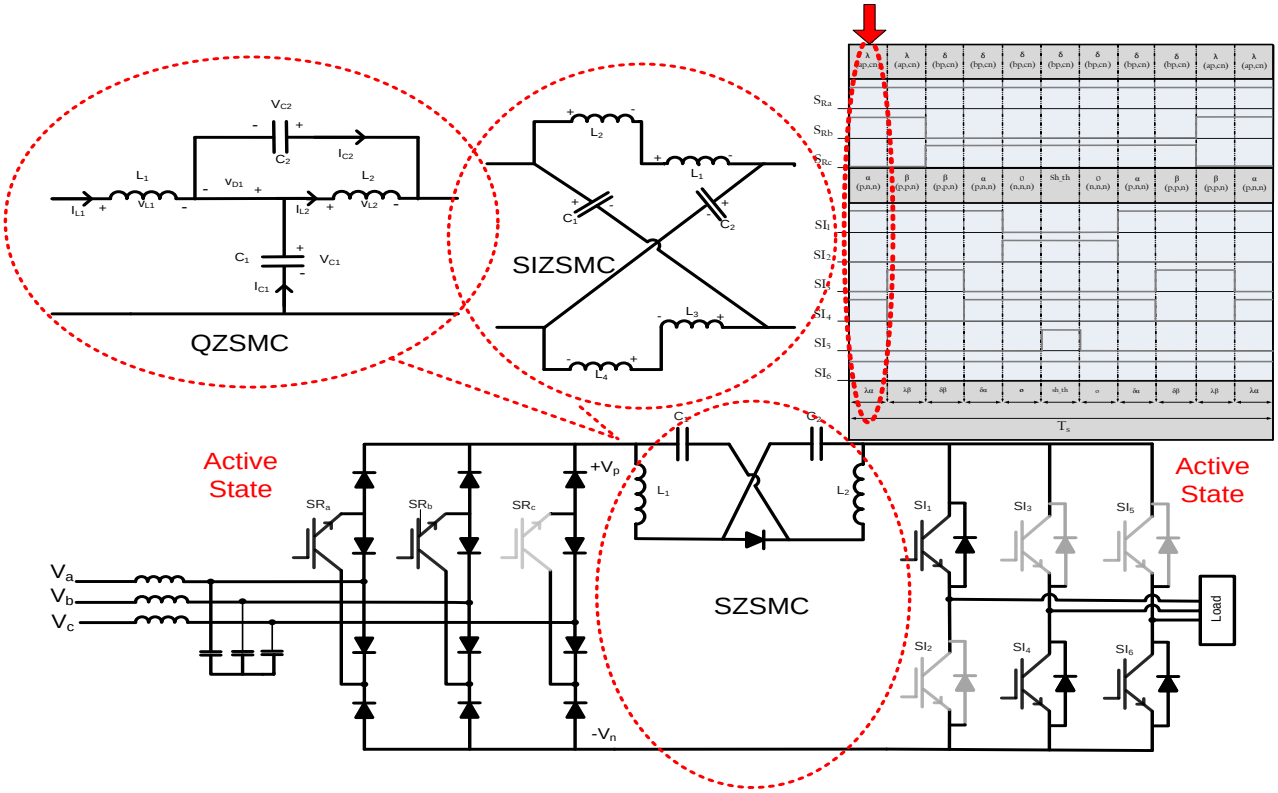


Fig. 4.17 Boost matrix converter's switching sequence. Step 1: During $T_{\lambda\alpha}$. θ_R and θ_i are both in zero sector

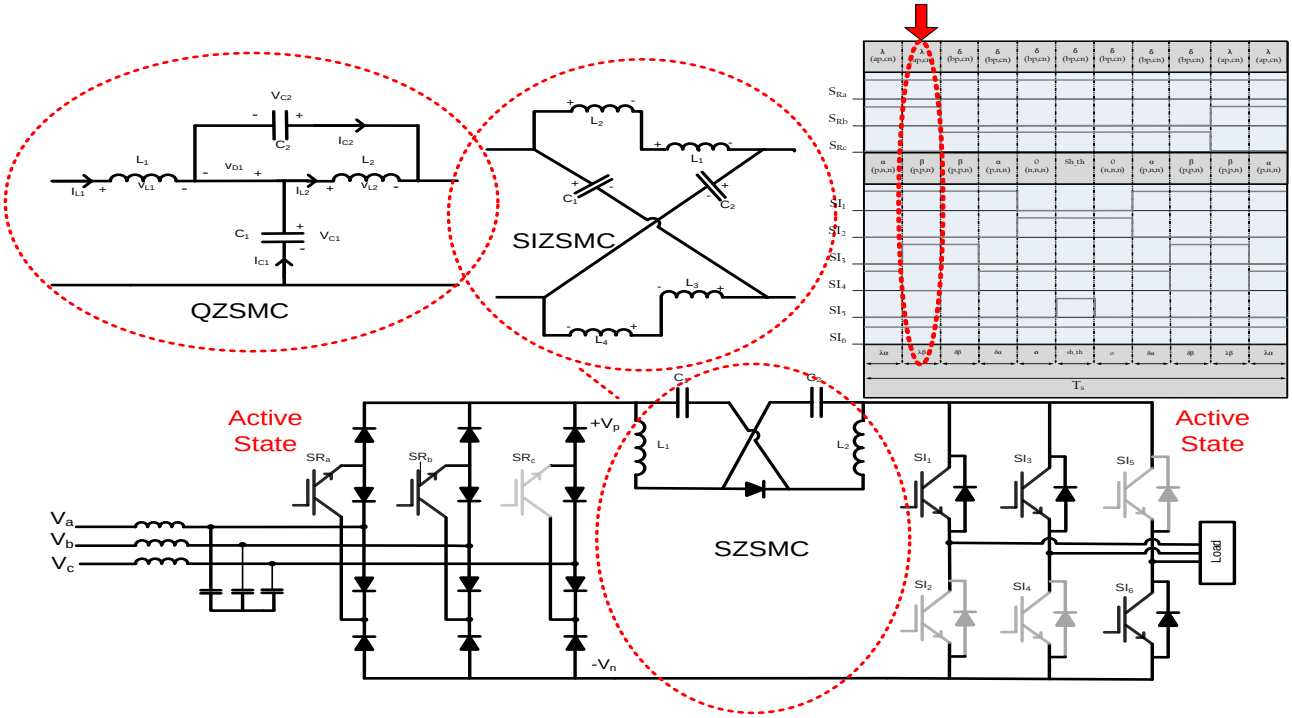


Fig. 4.18 Boost matrix converter's switching sequence. Step 2: During $T_{\lambda\beta}$. θ_R and θ_i are both in zero sector

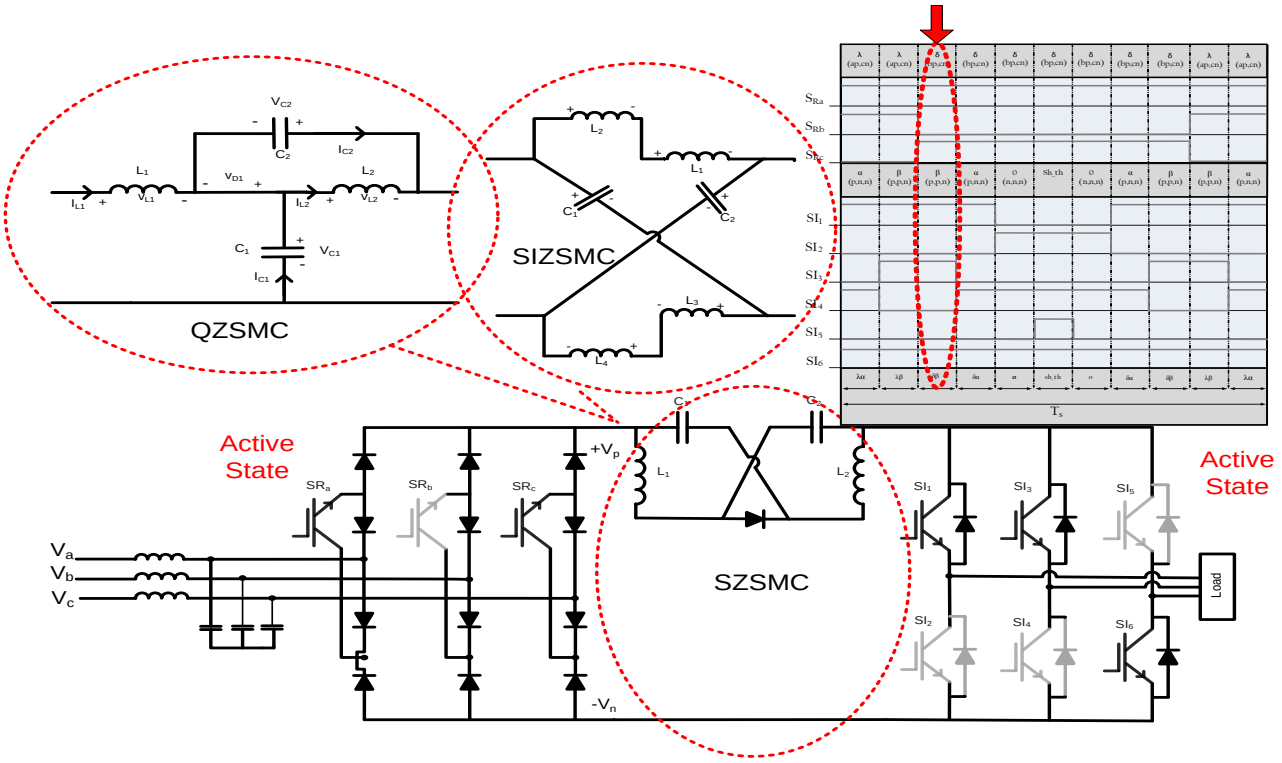


Fig. 4.19 Boost matrix converter's switching sequence. Step 3: During $T_{\delta\beta}$. θ_R and θ_i are both in zero sector.

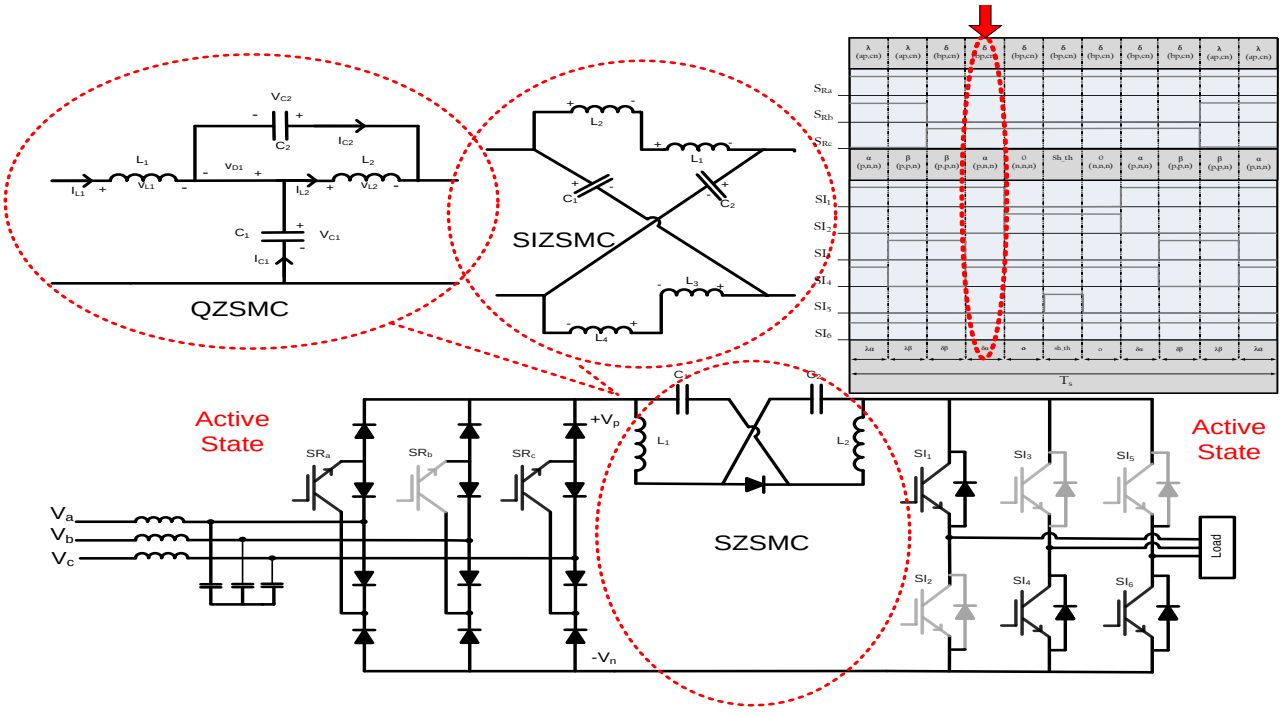


Fig. 4.20 Boost matrix converter's switching sequence. Step 4: During $T_{\delta\alpha}$. θ_R and θ_i are both in zero sector.

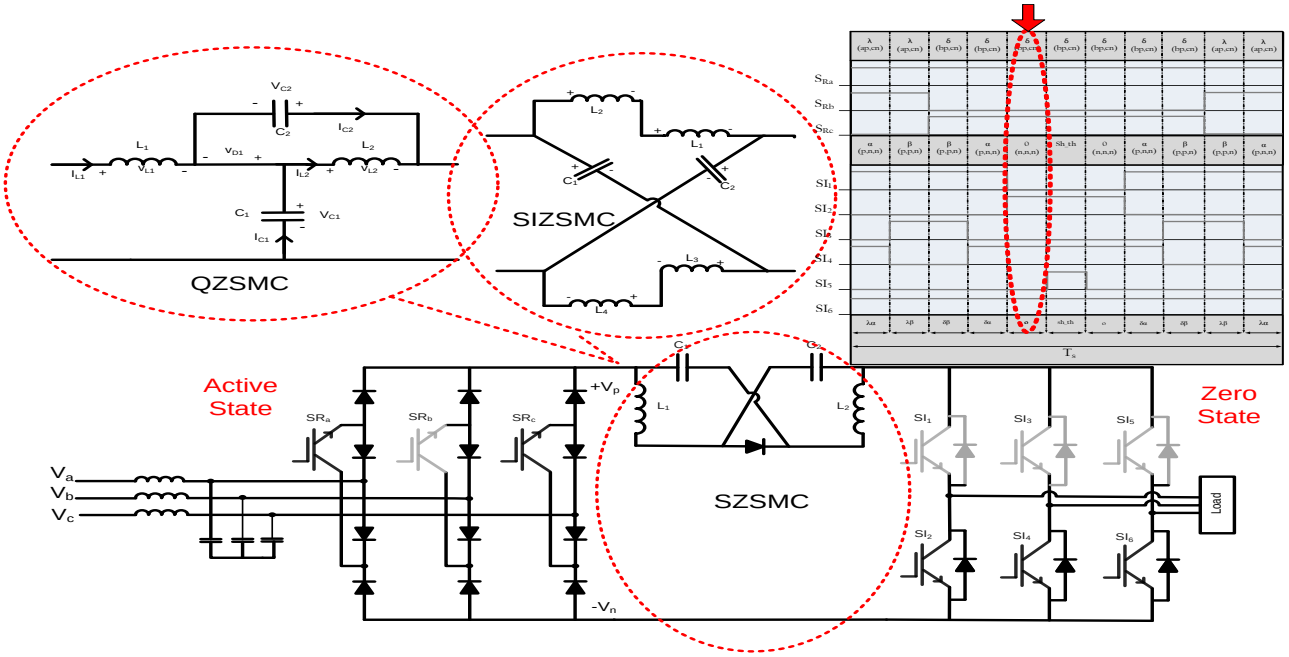


Fig. 4.21 Boost matrix converter's switching sequence. Step 5: During T_o. θ_R and θ_i are both in zero sector.

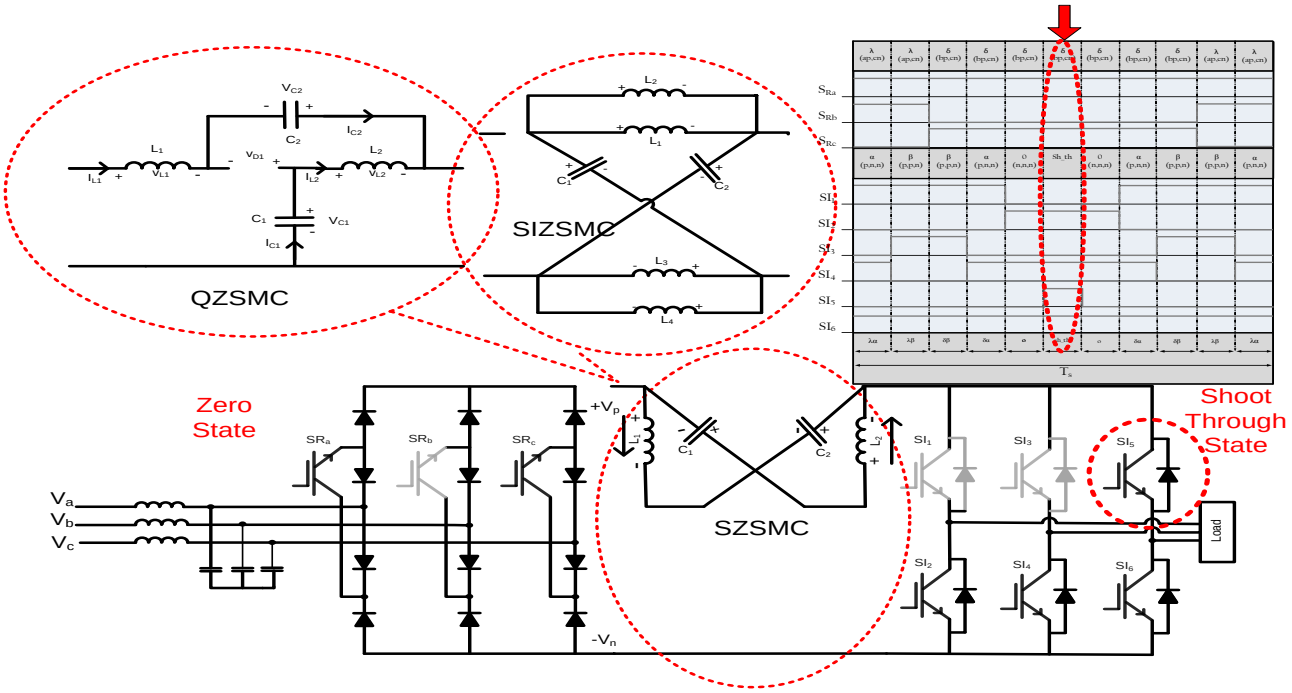


Fig. 4. 22 Boost matrix converter's switching sequence. Step 6: During $T_{(sh\text{-}th)}$. θ_R and θ_i are both in zero sector.

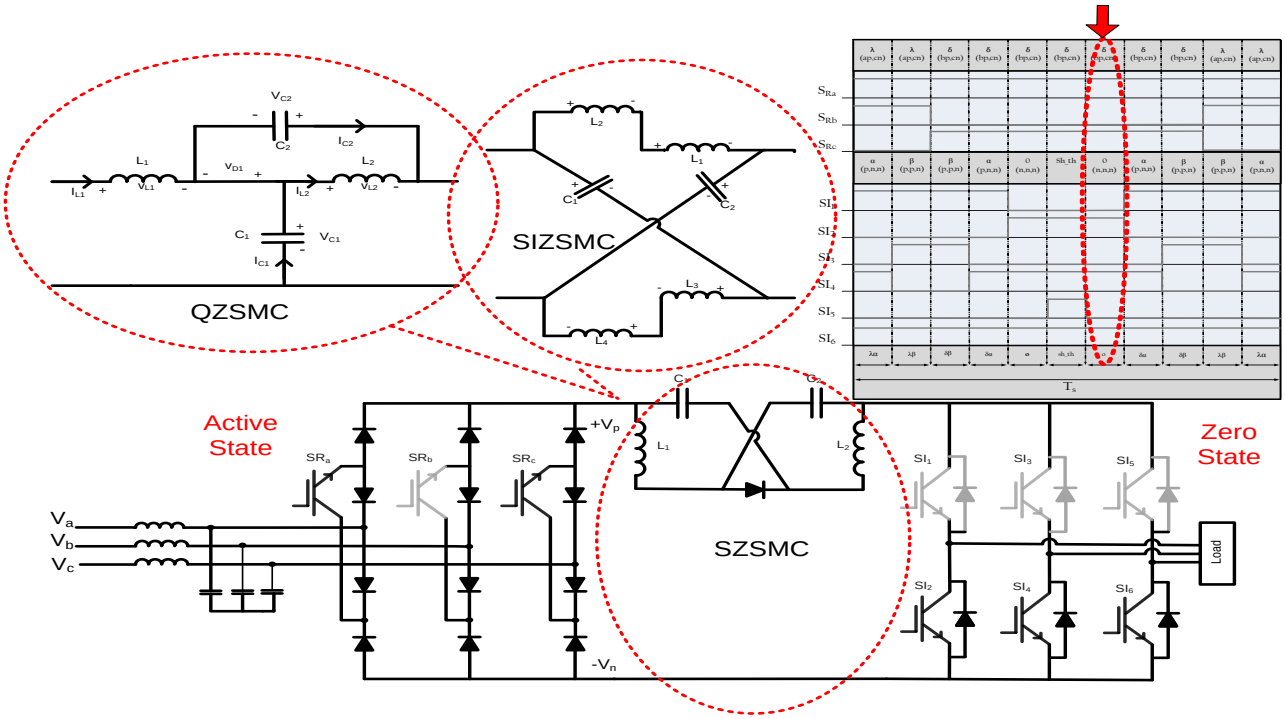


Fig. 4.23 Boost matrix converter's switching sequence. Step 7: During T_o. θ_R and θ_i are both in zero sector.

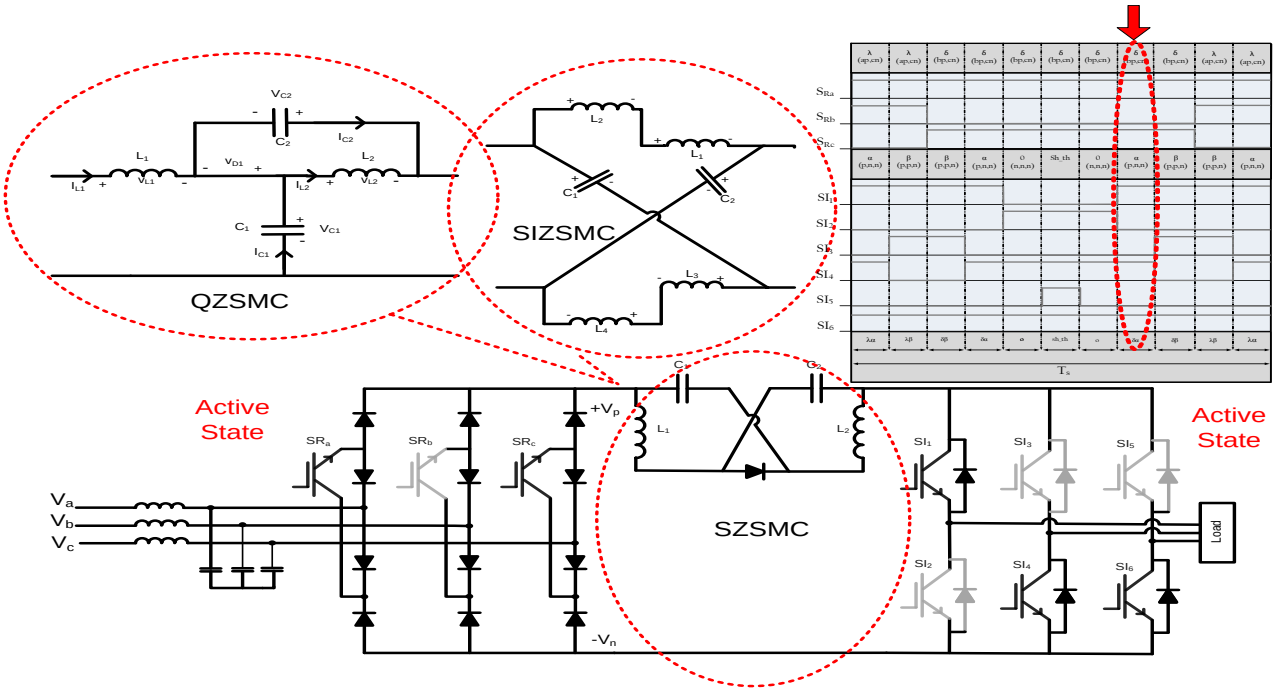


Fig. 4.24 Boost matrix converter's switching sequence. Step 8: During $T_{\delta\alpha}$. θ_R and θ_i are both in zero sector.

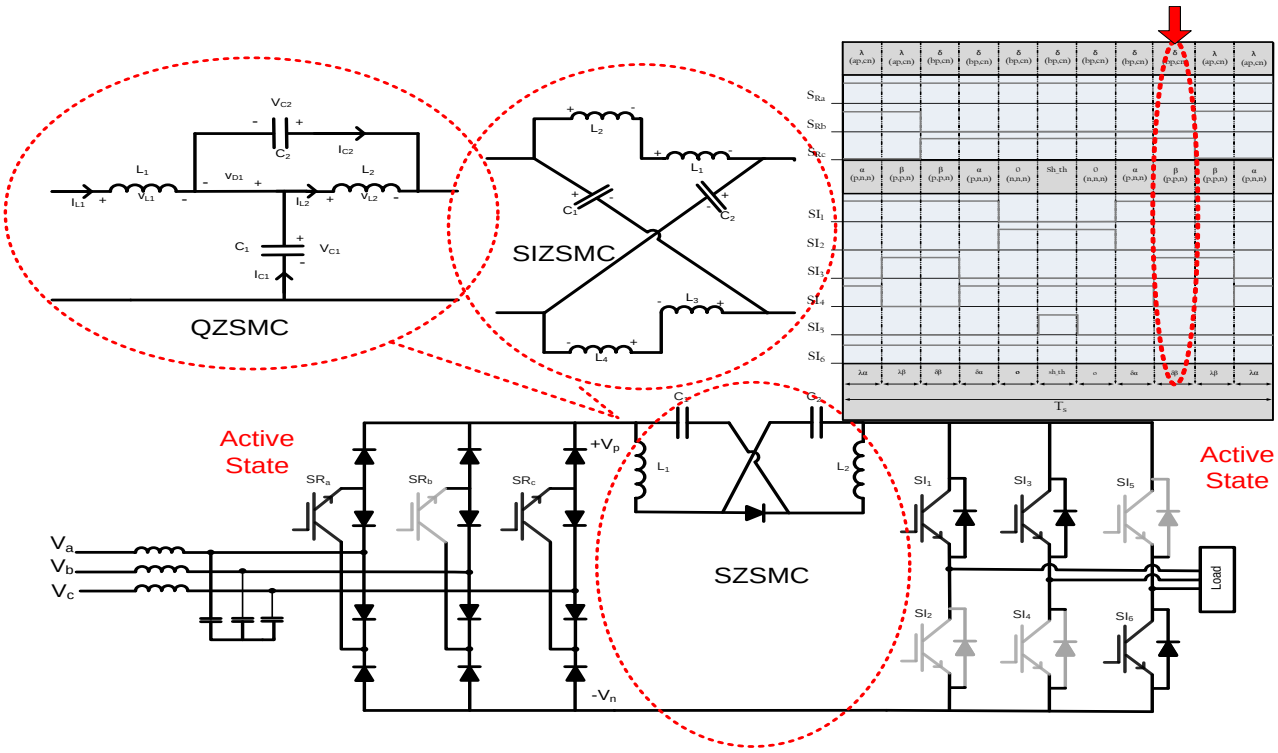


Fig. 4.25 Boost matrix converter's switching sequence. Step 9: During $T_{\delta\beta}$. θ_R and θ_i are both in zero sector.

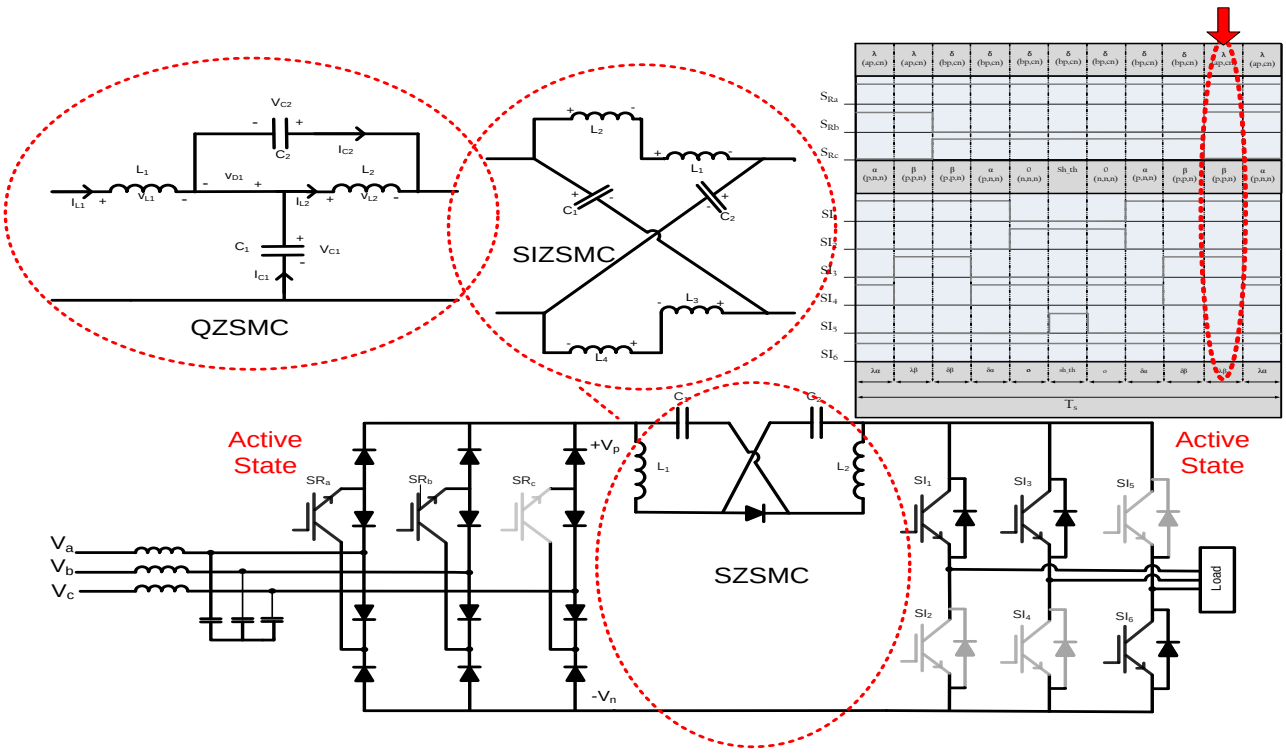


Fig. 4.26 Boost matrix converter's switching sequence. Step 10: During $T_{\lambda\beta}$. θ_R and θ_i are both in zero sector.

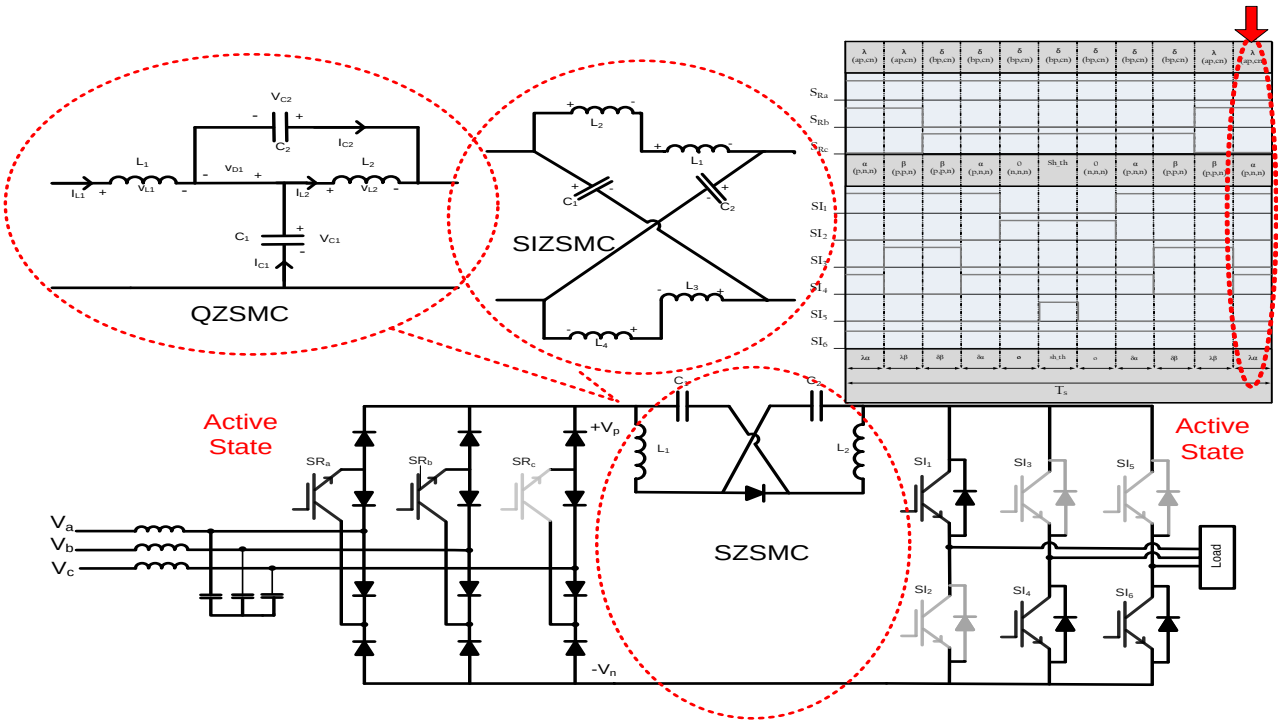


Fig. 4.27 Boost matrix converter's switching sequence. Step 11: During $T_{\lambda\alpha}$. θ_R and θ_i are both in zero sector.

4.6 Results

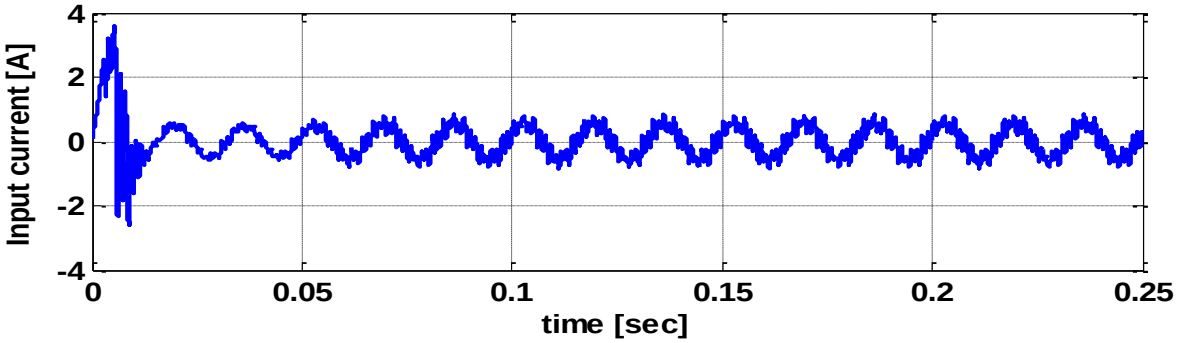
4.6.1 Series and Cascaded Z-source Matrix Converters – Simulation Results

The series Z-source and the cascaded Z-source matrix converters were simulated for comparative analysis in system 1. In the simulations the converters were fed from a 20-V, 60-Hz three-phase source and supplied a three-phase RL load with boosted output voltage of 40 Hz. The modulation index was set to 0.7 and the boost ratio to 2. Optimal switching sequence was employed. Parameters of the converters are selected based on the considerations in previous section, and are given in Table 4.1. In this work, the components were selected for a rated output power of 2 kW, switching period of 100 μsec, input voltage of 120 V, 60 Hz, and a unity input power factor.

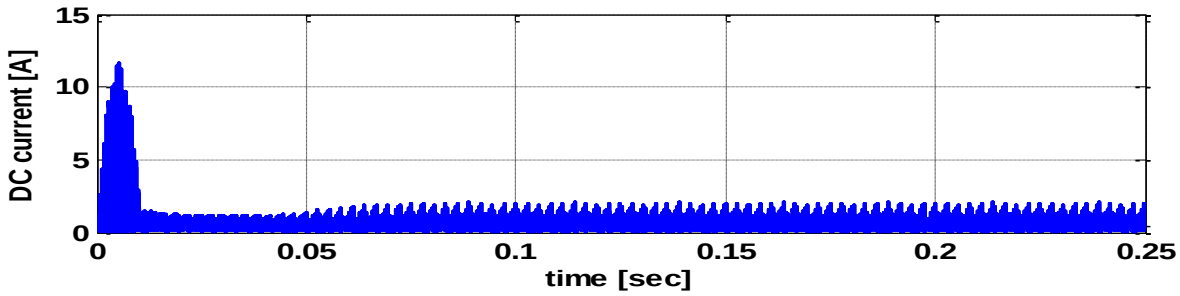
Furthermore, the boost factor was considered to vary from 1 to 6. The desired ripples of capacitor voltage and inductor current were taken as less than 1% of their rated values. The inrush current at the startup occurs in all converters. It can be seen in Figs. 4.27(b)-(c) that the peak of the inrush current in the series Z-source matrix converters equals 12 A in the dc link and 6A in the network inductor. As seen in Figs. 4.28(b)-(c), in the cascaded Z-source matrix converters the peak reaches as much as 41 A in the dc link and 9 A in the network inductor. Also, the current stress in the series Z-source network inductors is remarkably lower than the cascaded Z-source network.

Input AC Source	20 V / 60Hz
Output	40 V / 40 Hz
Load, R/L	10 mH / 50 Ω
Input Filter, L/C	2 mH / 18 μF
Z-source, L/C	2 mH / 1000 μF
Series Z-source, L/C	2 mH / 1000 μF
Switching Frequency	10 kHz

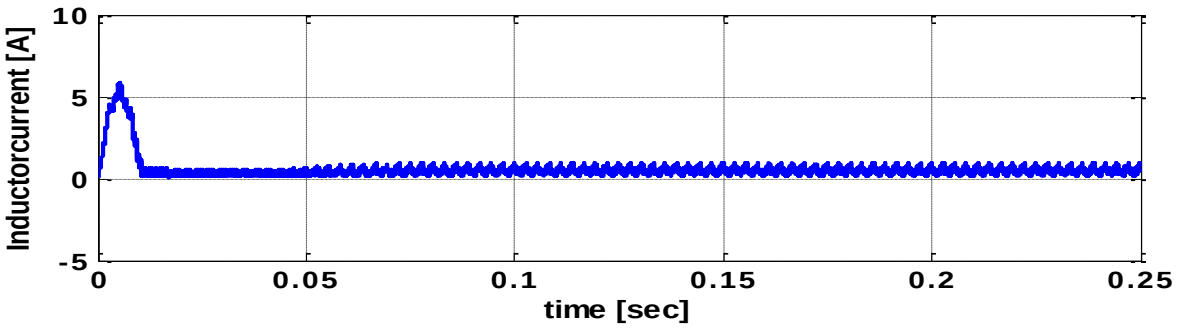
Table 4.1 System 1 parameters.



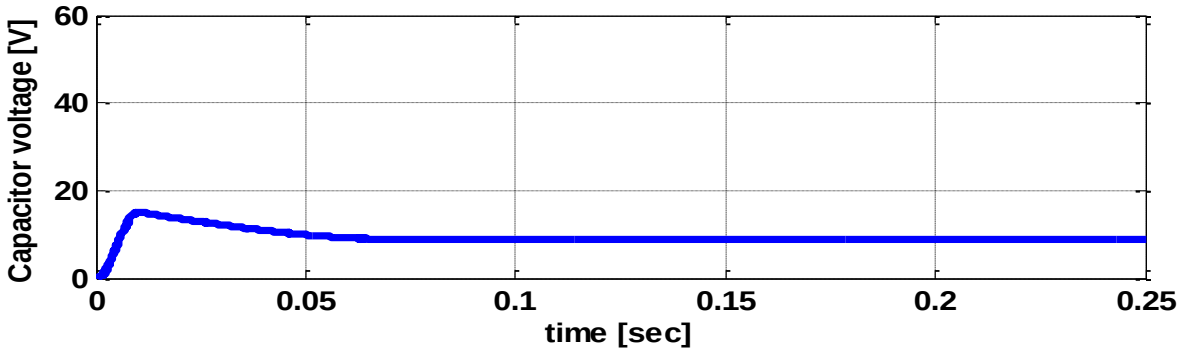
(a)



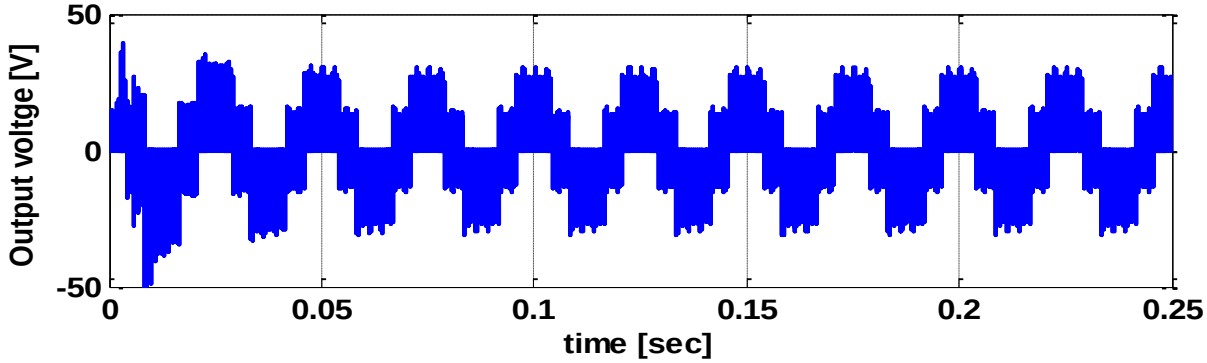
(b)


Inductorcurrent [A]
10
5
0
-5
0
0.05
0.1
0.15
0.2
0.25
time [sec]

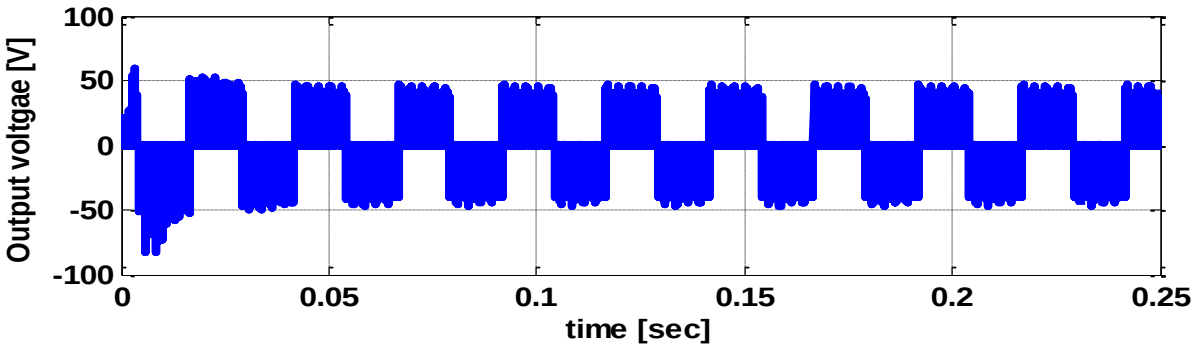
(c)


Capacitor voltage [V]
60
40
20
0
0
0.05
0.1
0.15
0.2
0.25
time [sec]

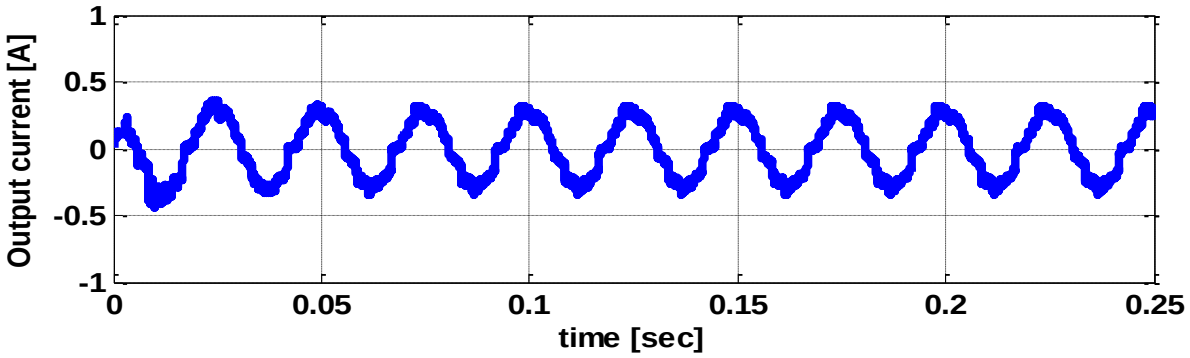
(d)


Output voltge [V]
50
0
-50
0
0.05
0.1
0.15
0.2
0.25
time [sec]

(e)


Output voltgae [V]
100
50
0
-50
-100
0
0.05
0.1
0.15
0.2
0.25
time [sec]

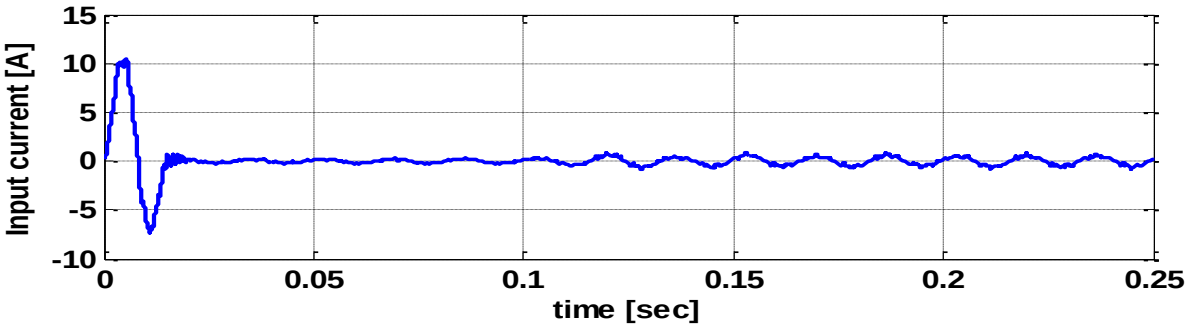
(f)



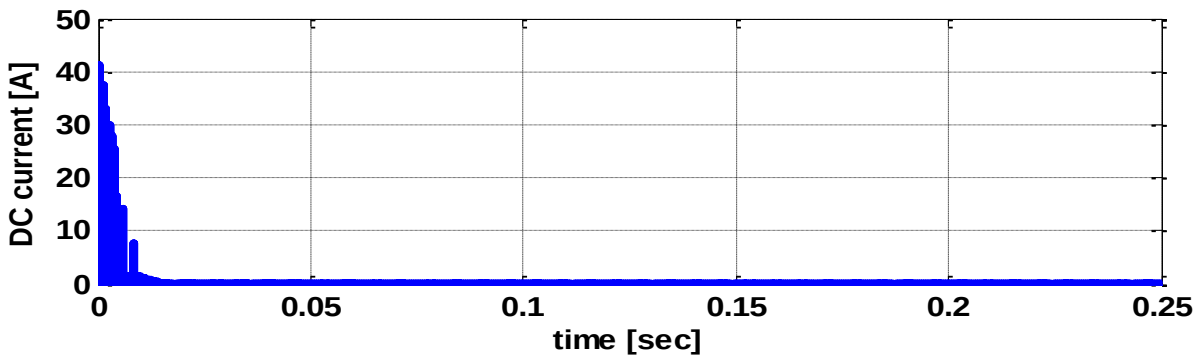
(g)

Fig. 4.28 Series Z-source matrix converter: (a) input phase current, (b) dc link current, (c) series Z-source inductor current, (d) series Z-source capacitor voltage, (e) output phase voltage, (f) output line-to-line voltage, (g) output phase current.

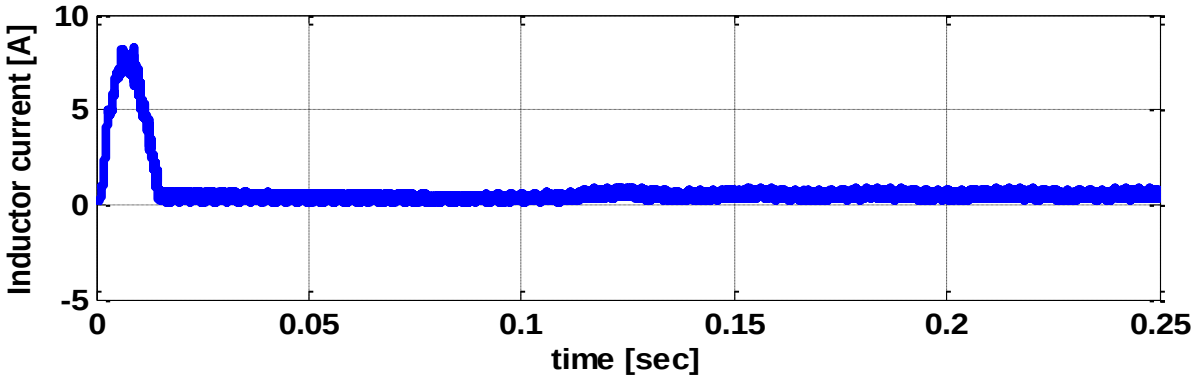
The network capacitor voltage in the series Z-source converter is about 12 V. This voltage in the cascaded Z-source matrix converter is about 35 V. Clearly, the improved topology reduces the voltage stress on the converter components.



(a)



(b)


Inductor current [A]
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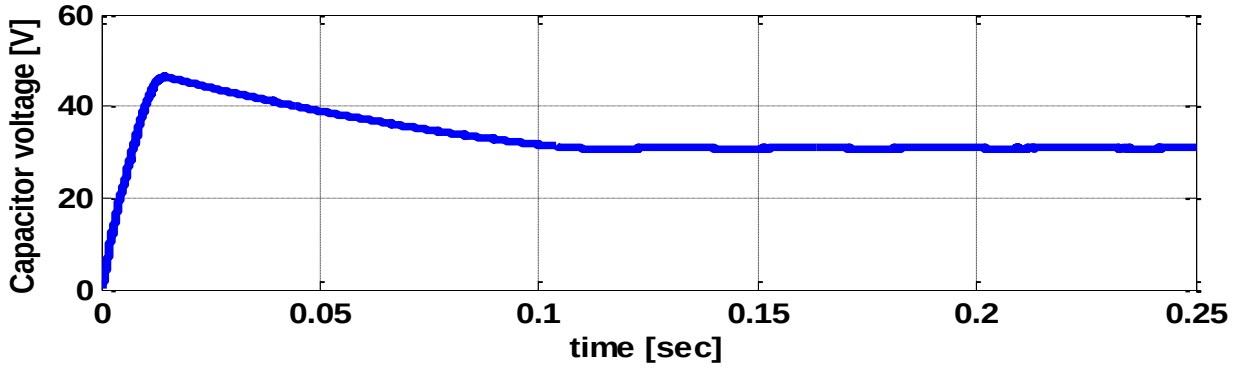
5
0
-5
0
0.05
0.1
0.15
0.2
0.25
time [sec]

(c)


Capacitor voltage [V]
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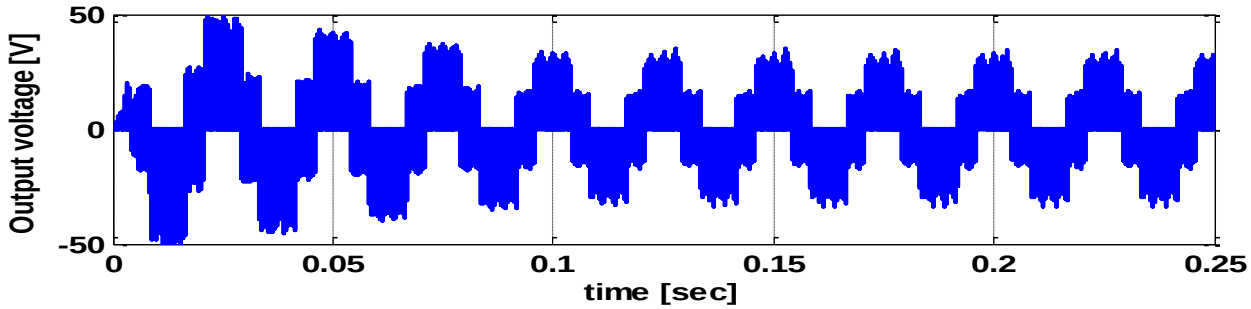
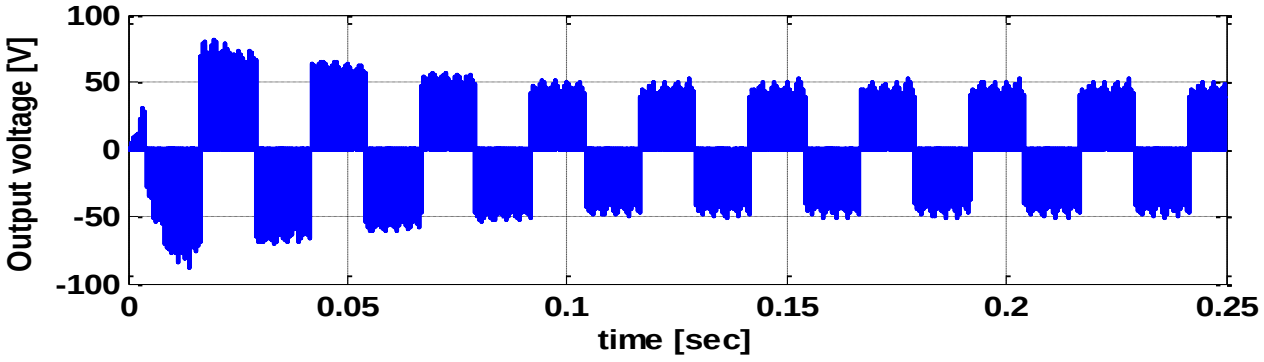
40
20
0
0
0.05
0.1
0.15
0.2
0.25
time [sec]

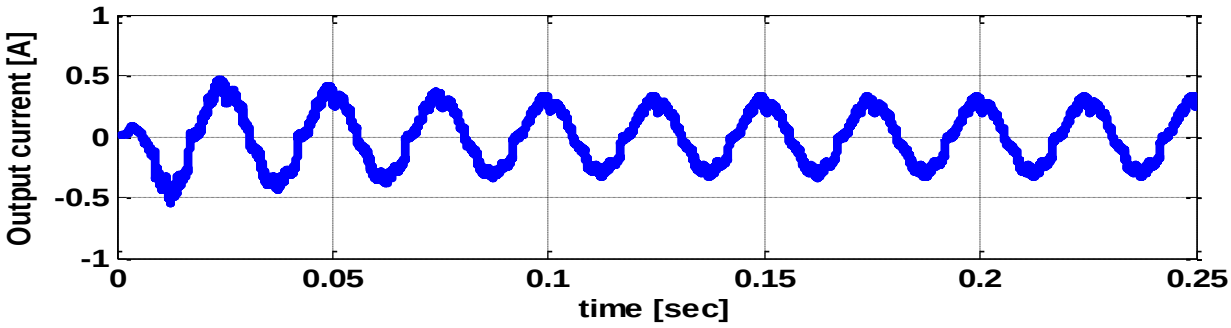
(d)


Output voltage [V]
50
0
-50
0
0.05
0.1
0.15
0.2
0.25
time [sec]

(e)


Output voltage [V]
100
50
0
-50
-100
0
0.05
0.1
0.15
0.2
0.25
time [sec]

(f)



(g)

Fig. 4.29 Cascaded Z-source matrix converter: (a) input phase current, (b) dc link current, (c) series Z-source inductor current, (d) series Z-source capacitor voltage, (e) output phase voltage, (f) output line-to-line voltage, (g) output phase current.

Similar analyses were carried out in larger input voltages and boost ratio for further investigations in system 2. In this set of simulations the converters were fed from a 60-V, 40-Hz three-phase source this time and supplied the same RL load. The modulation index was set to 0.7 and the boost ratio to 3 this time. Same switching sequence was employed. The converters parameters are given in Table 4.2 Selected waveforms of voltages and currents for three converters are shown in Figs. 4.29 and 4.30.

It can be seen that the input voltages and currents of phase A are in phase, resulting in a unity power factor. The inrush current at the startup occurs in all converters as it was in System 1. Fig. 4.31 shows that the peak of the inrush current in the series Z-source matrix converters equals 35 A in the dc link and 17.5 A in the network inductor. As seen in Fig.4. 32, in the cascaded Z-source matrix converters the peak reaches as much as 250 A in the dc link and 21.5 A in the network inductor. Also, the current stress in the series Z-source network inductors is remarkably lower than the cascaded Z-source network.

It is also important to analyze whether I_o affects the input currents, especially at low modulation indexes which is possible for higher boost factors. Referring to the input current

waveforms, the modulation strategy can modulate the converter to generate a set of sinusoidal, balanced input currents. Referring to the spectra shown in Fig. 4.29, there are obviously some current ripples around fundamental frequency and the ripples are of significant magnitude (> 2% of fundamental at high modulation indexes). The input current is main disadvantage of the series and cascaded Z-source matrix converters.

The network capacitor and dc link voltages in the series Z-source converter are about 80 V and 150 V, respectively. These voltages in the Z-source matrix converter are about 118 V and 220 V. Clearly, the improved topology reduces the voltage stress on the converter components. The dc link voltage ripple is directly related to the size of the capacitors. To reduce the ripple higher capacitance is needed. However the higher capacitance creates a larger inrush current. Series Z-source matrix converter is not limited to capacitor value settings due to the inrush current. Large capacitors can be chosen without additional calculations for the front end current peaks.

Input AC Source	60 V / 40Hz
Output/Switching Frequency	60 Hz / 10 kHz
Load, R/L	10 mH / 50 Ω
Input Filter, L/C	2 mH / 2.2 μF
Z-source, L/C	2 mH / 1000 μF
Series Z-source, L/C	2 mH / 1000 μF
Switching Frequency	10 kHz

Table 4.2 System 2 parameters.

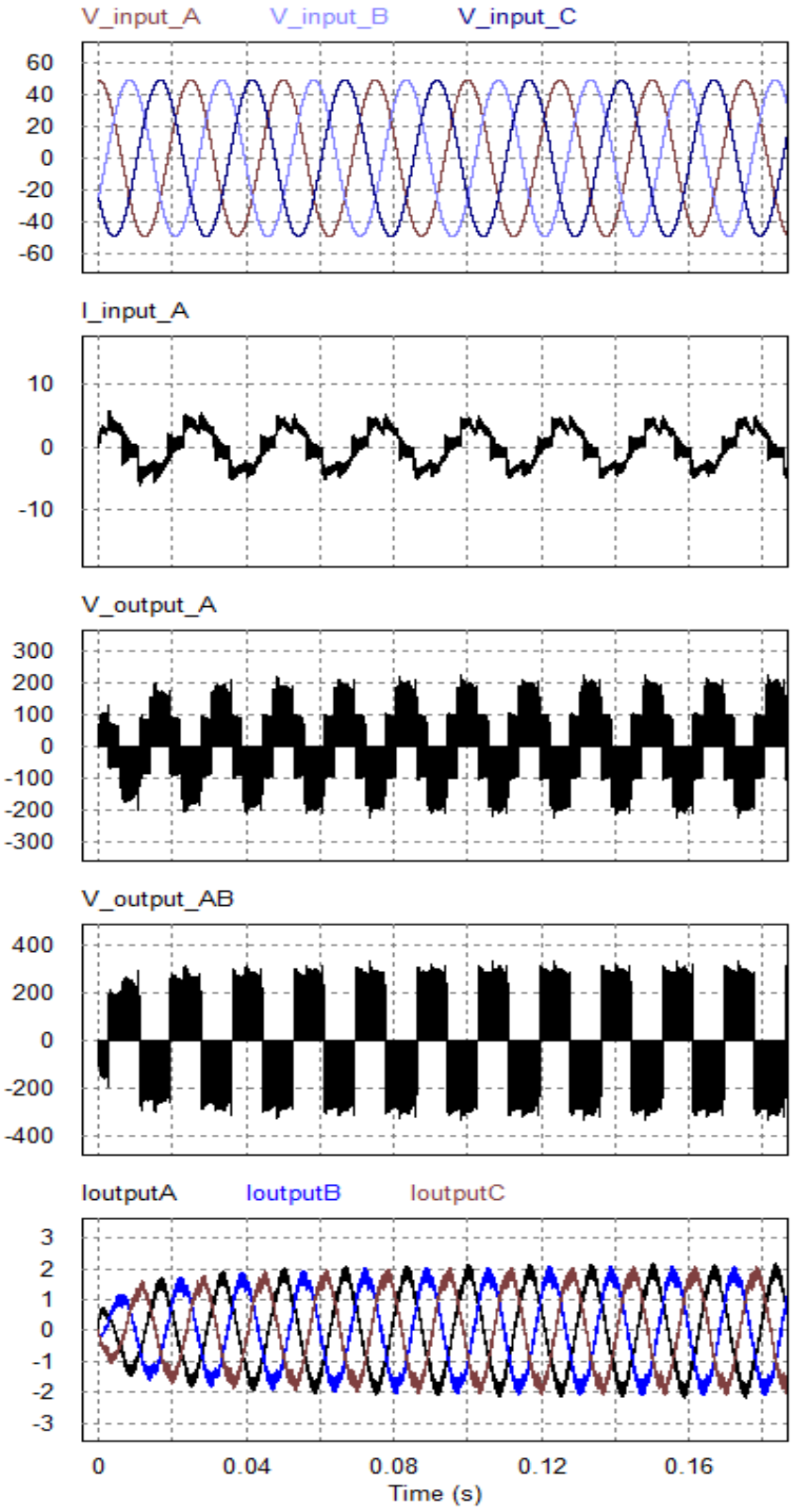


Fig. 4.30 Series Z-source, top to bottom: input phase voltages, input phase A current, output phase A voltage, output line-to-line AB voltage, output phase currents.

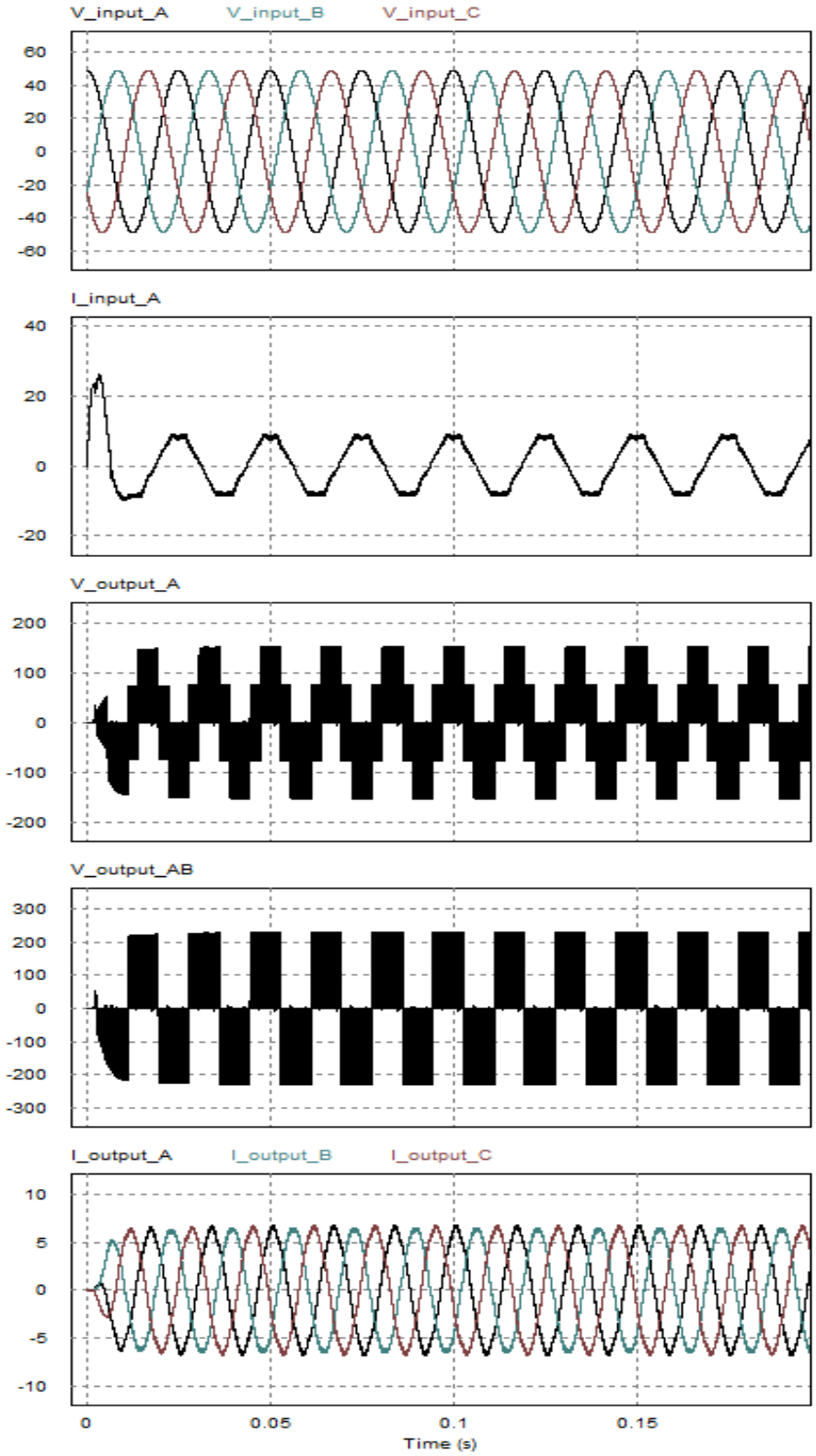


Fig. 4.31 Cascaded Z-source, top to bottom: input phase voltages, input phase A current, output phase A voltage, output line-to-line AB voltage, output phase currents.

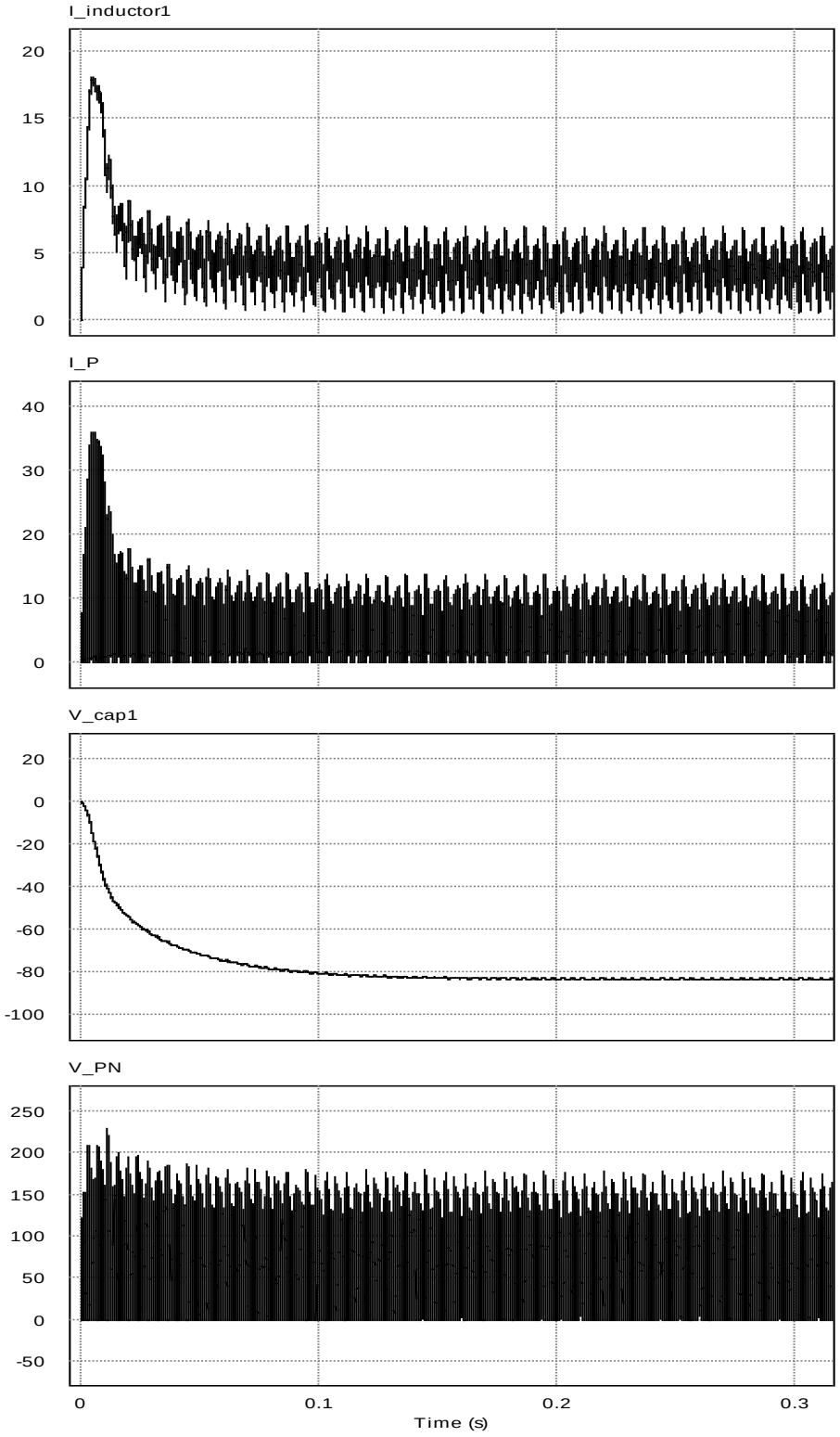


Fig. 4.32 Series Z-source, top to bottom: series Z-source inductor (L1) current, dc link current, series Z-source capacitor (C1) voltage, dc link voltage.

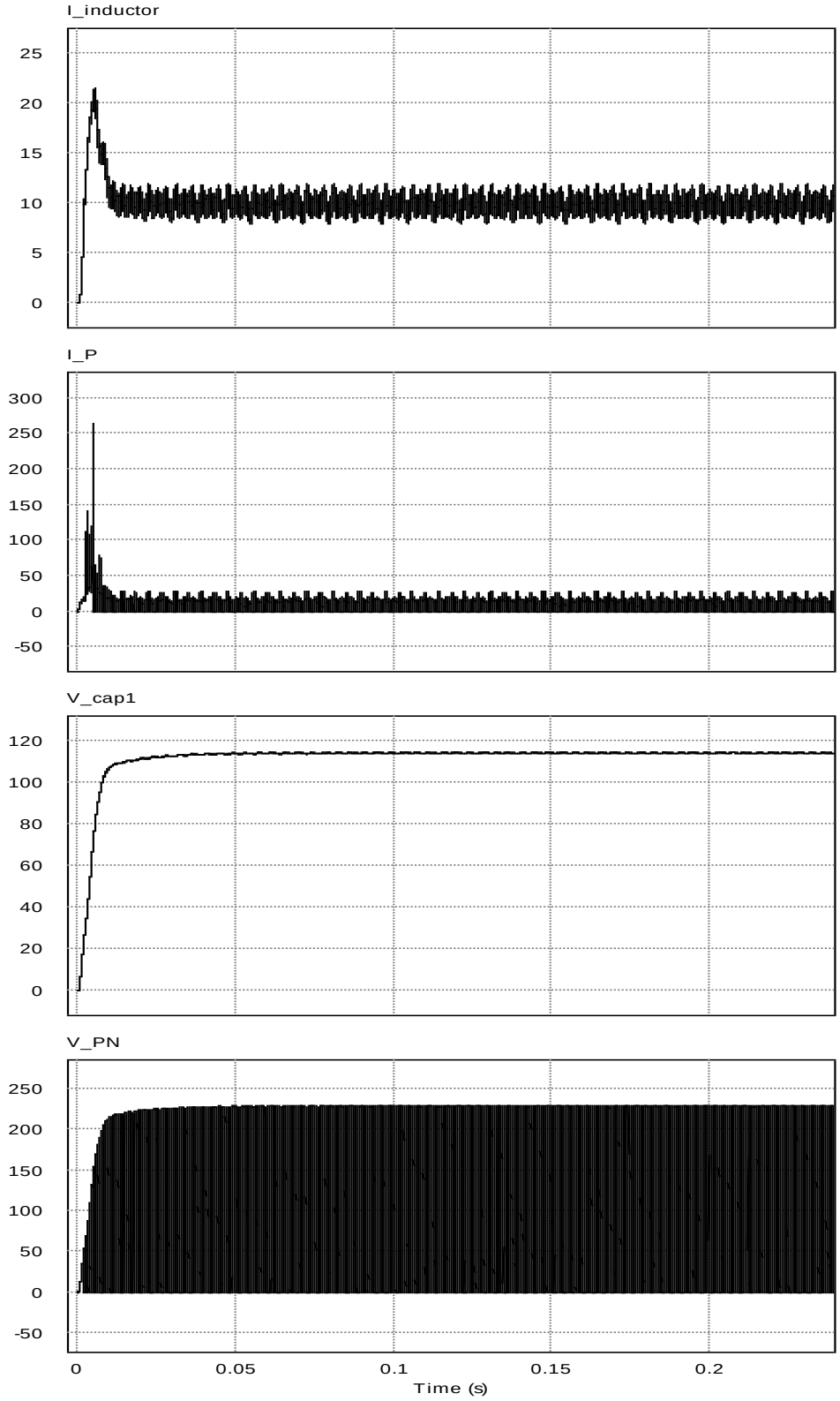


Fig. 4.33 Cascaded Z-source, top to bottom: Z-source inductor (L1) current, dc link current, Z-source capacitor (C1) voltage, dc link voltage.

4.6.2 Series Z-Source Matrix Converter - Experimental Results

In the experiments, the converters were fed from an AC supply with variable amplitude and constant frequency of 60 Hz and supplied an RL load with boosted output voltages of 40 Hz. System parameters were the same as in the simulations. The results of the experiments for the series Z-source matrix converter are shown in Figs. 4.34 to 4.38 and, for comparison, those for the cascaded Z-source converter in Figs. 4.39 to 4.41.

The boost factor and modulation index were set to 2 and 0.7, respectively. The line-line input voltage amplitude is boosted from 40 V peak-peak to 80 V peak-peak. The input and output current amplitudes are around 2 A peak-peak and 1 A peak-peak, respectively.

The relation between V_c and V_{dc} can be obtained using equations (4.5) and (4.7) as $V_{dc} = 1/d_{sh-th}V_c$. In this case, in order to achieve a boost factor of 2, the shoot-through duty ratio should be 0.25, which results in $V_{dc} = 4V_c$. As can be seen, V_c is 12 V, and V_{dc} is boosted to about 50 V.

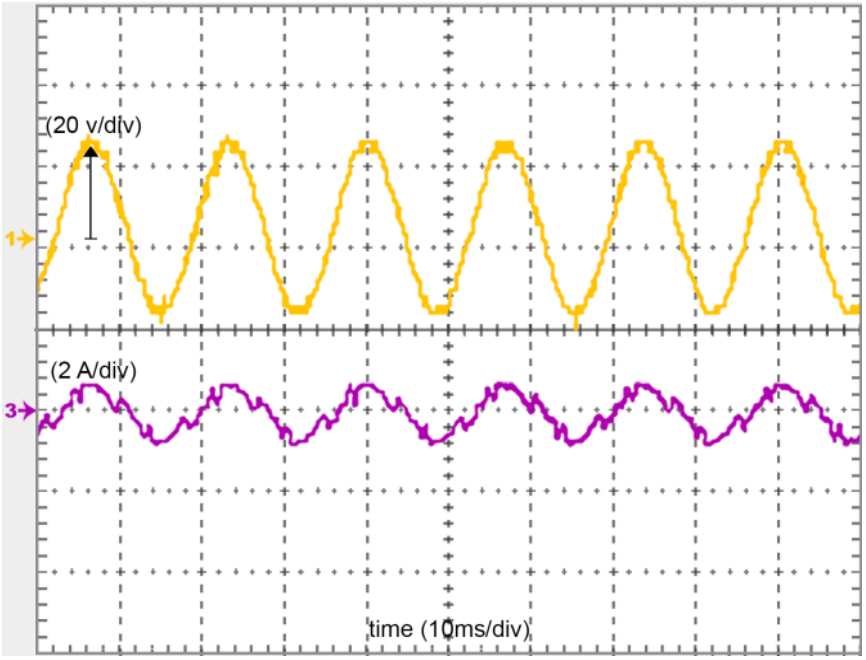


Fig. 4.34 Series Z-source matrix converter. Top: line-line input voltage, bottom: phase input current.

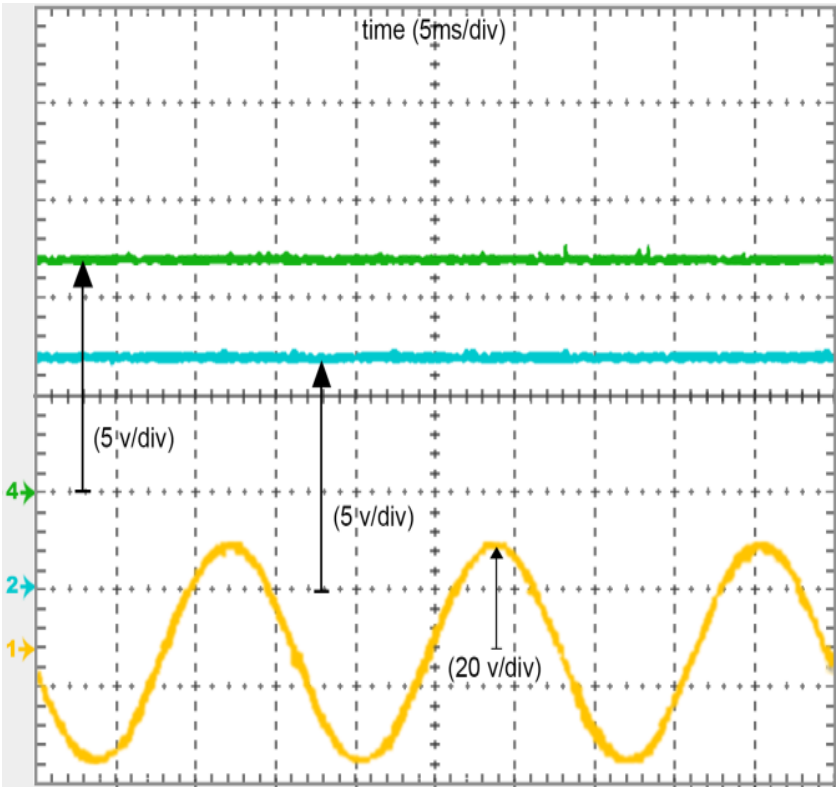


Fig. 4.35 Series Z-source matrix converter. Top: Z-source network capacitor voltages, bottom: line-line input voltage.

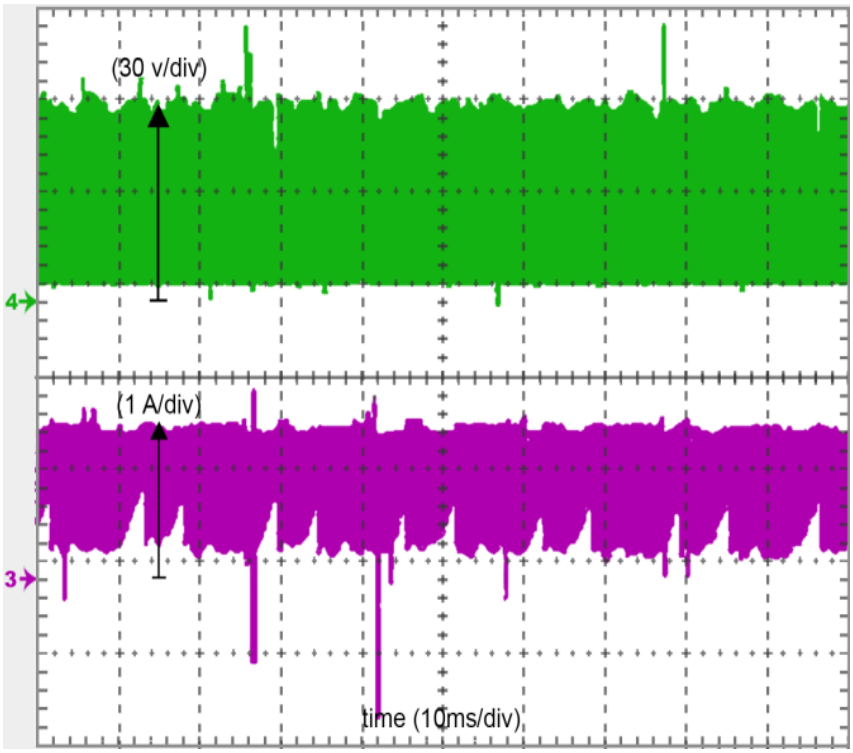


Fig. 4.36 Series Z-source matrix converter. Top: Z-source network output voltage, bottom: Z-source network inductor current.

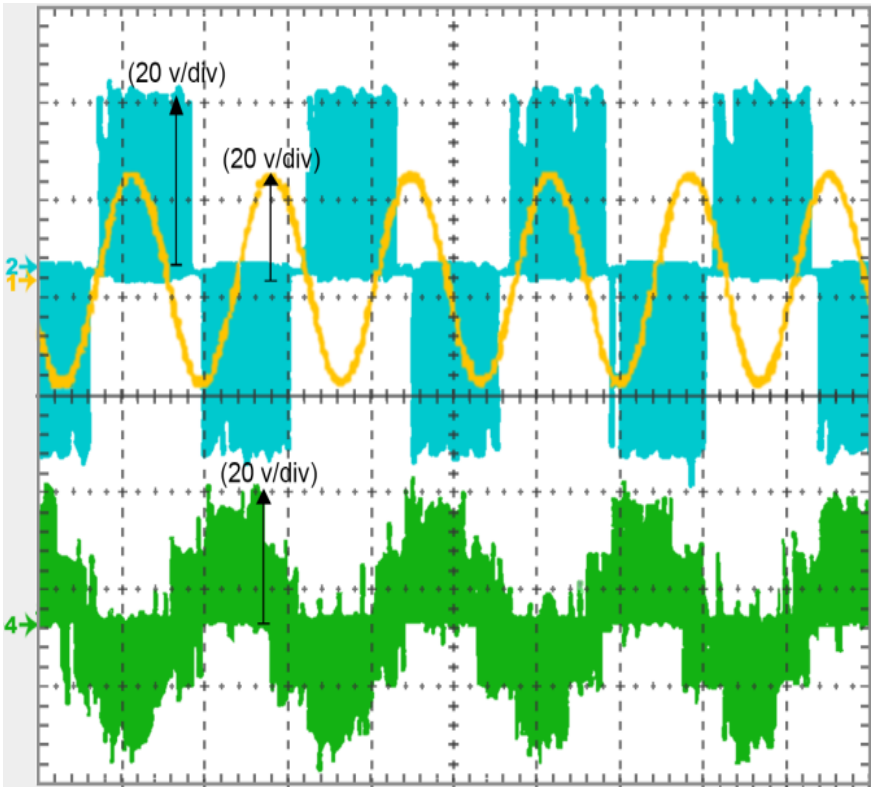


Fig. 4.37 Series Z-source matrix converter. Top: line-line input and output voltages, bottom: output phase voltage.

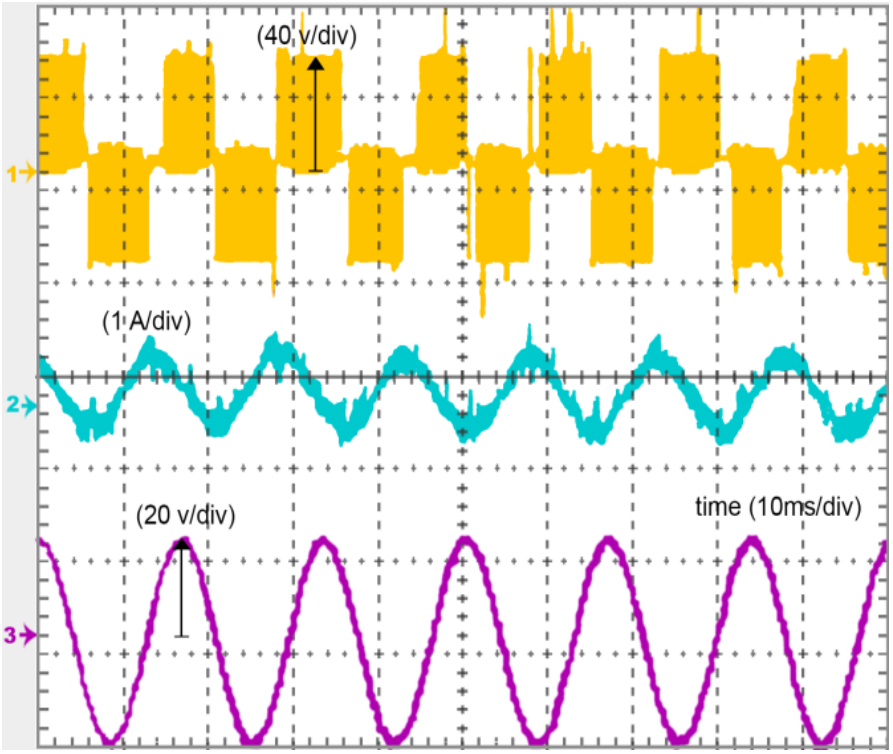


Fig. 4.38 Series Z-source matrix converter. Top to bottom: line-line output voltage, output phase current, line-line input voltage.

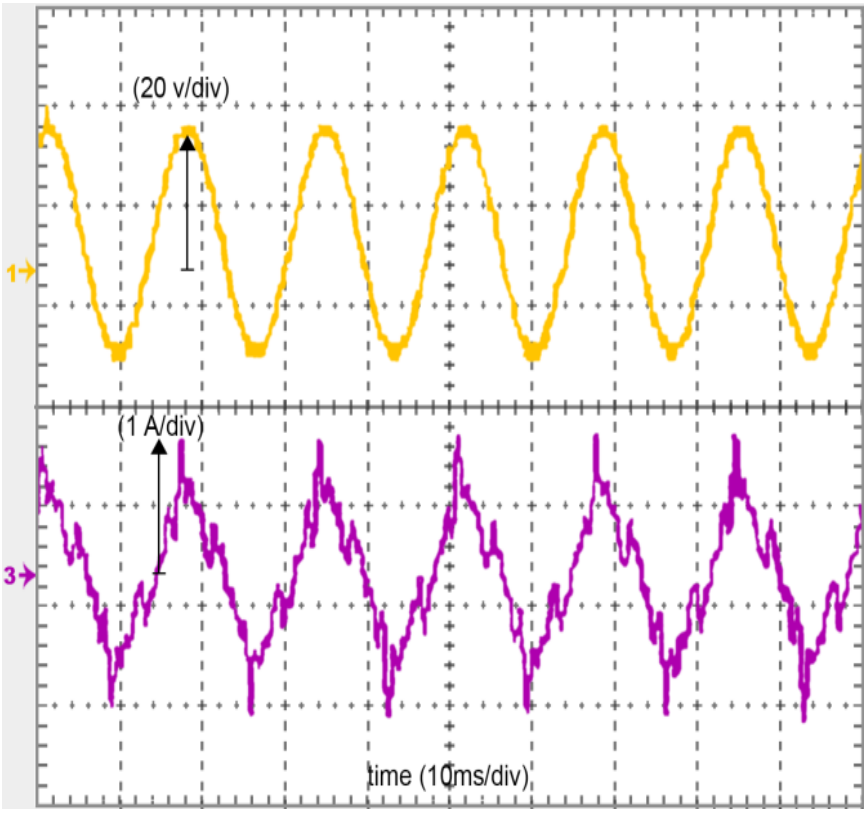


Fig. 4. 39 Cascaded Z-source matrix converter. Top: line-line input voltage, bottom: phase input current.

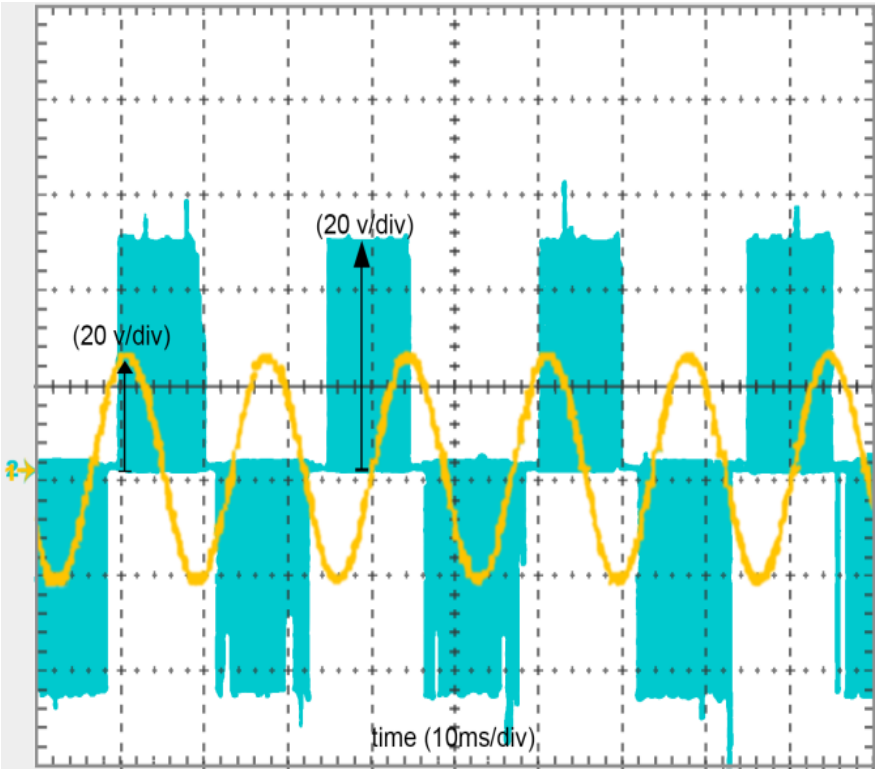


Fig. 4.40 Cascaded Z-source matrix converter: line-line input and output voltages.

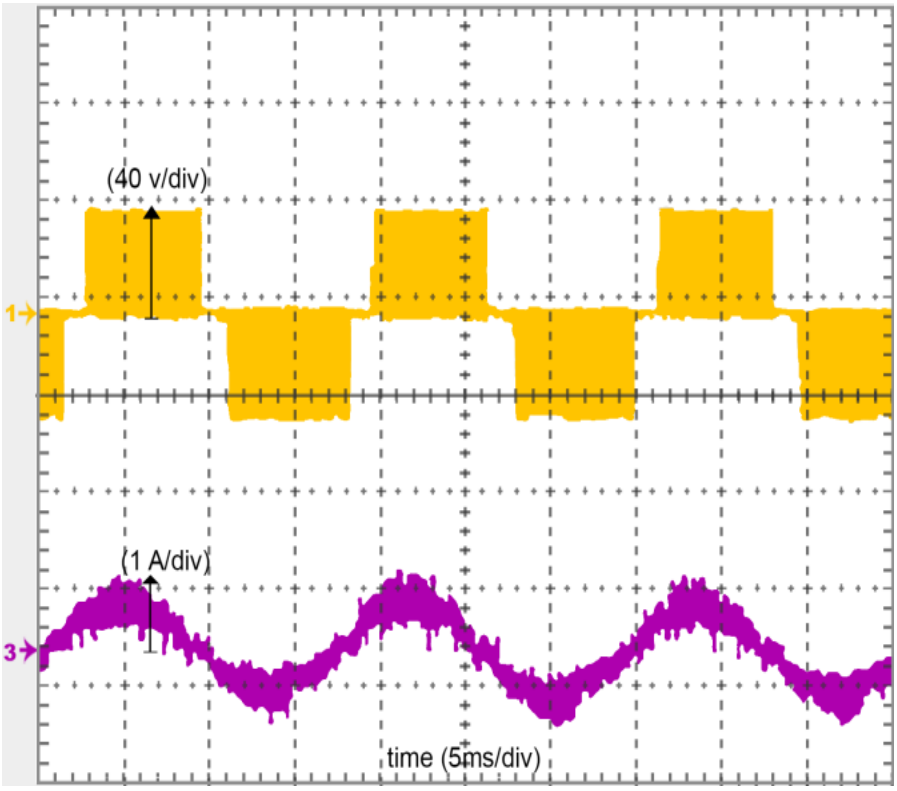


Fig. 4.41 Cascaded Z-source matrix converter. Top: line-line output voltage, bottom: output phase current.

4.6.3 Quasi Z-Source Matrix Converter - Simulation Results

In the simulations, the quasi Z-source matrix converter was fed from a 60-V, 40-Hz three-phase source and supplied a three-phase RL load ,or the grid, with boosted output voltage of 60 Hz. The modulation index was set to 0.7 and the boost ratio to 6. The optimal switching sequence was employed. The parameter values are given in Table 4.3. The components are selected for a rated output power of 2 kW, switching period of 100 µsec, input voltage of 120 V, 60 Hz, and a unity input power factor.

The simulated results confirm the validity and superiority of the proposed control strategies, indicating a significant progress in enhancing the gearless performances of wind power generation systems. Low-pass LC filters were placed at the input of the converter to reduce the ripple of input currents.

Input AC Source	60 V / 40Hz
Reference Output Voltage	60 Hz
Load, R/L	10 mH / 40 Ω
Input Filter, L/C	2 mH / 2.2 μF
Quasi Z-source, L/C	1 mH / 800 μF
Switching Frequency	10 kHz

Table 4.3 System parameters.

The performance of the proposed converter was evaluated for two operating conditions. In the first case, the converter was fed from a 60-V, three-phase source and supplied an RL load. The voltage was boosted up to six times. Selected waveforms of voltages and currents are shown in Figs. 4.42 and 4.43.

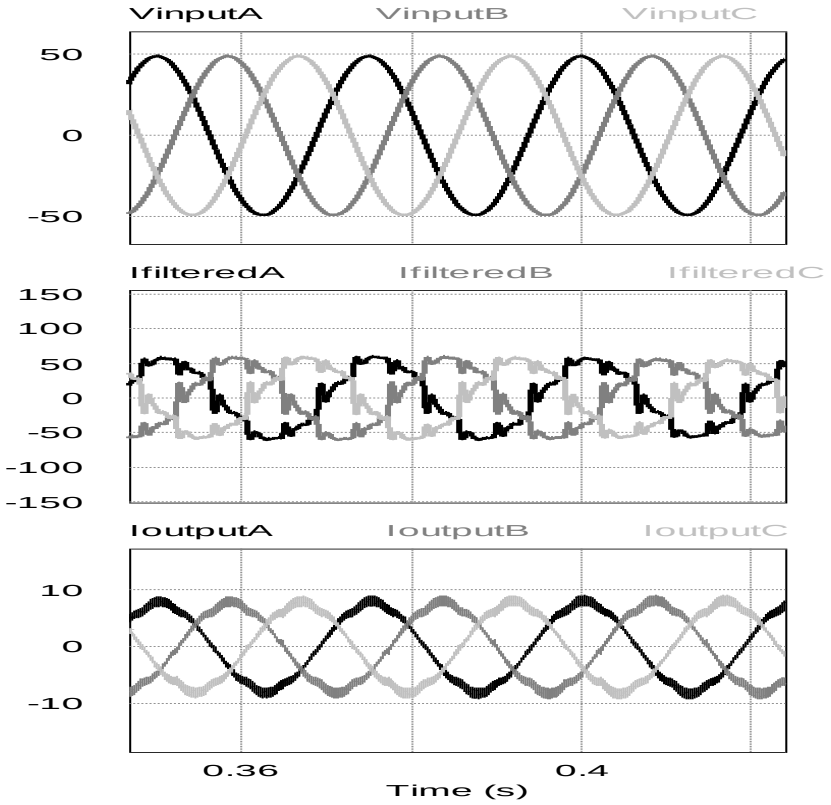


Fig. 4.42 RL load. Top to bottom: input phase voltages, filtered input currents, output currents.

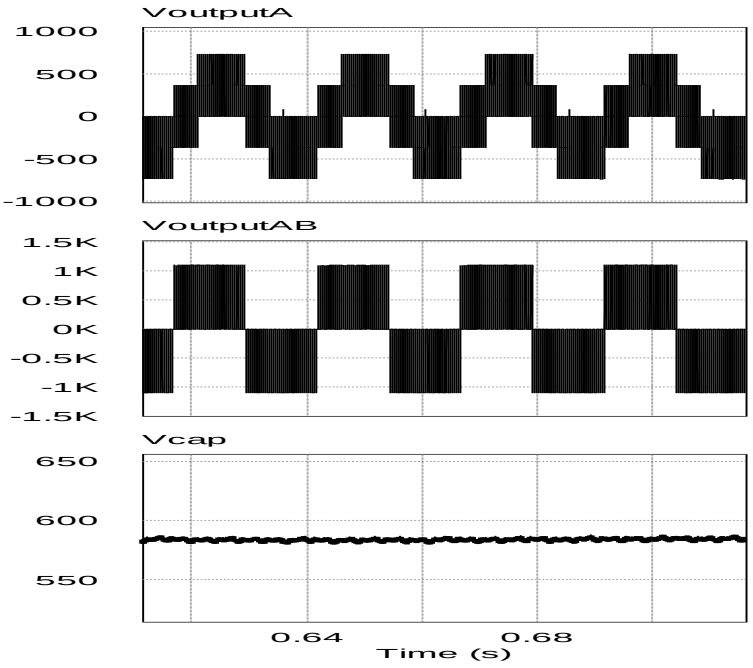


Fig. 4.43 RL load. Top to bottom: output phase voltage, output line-to-line voltage, capacitor-1 voltage.

In the second case, the converter was fed from a 60-V, 60-Hz three-phase source and connected to a 230-V grid through a 10-mH inductance. Selected waveforms are shown in Fig. 4.44 and 4.45.

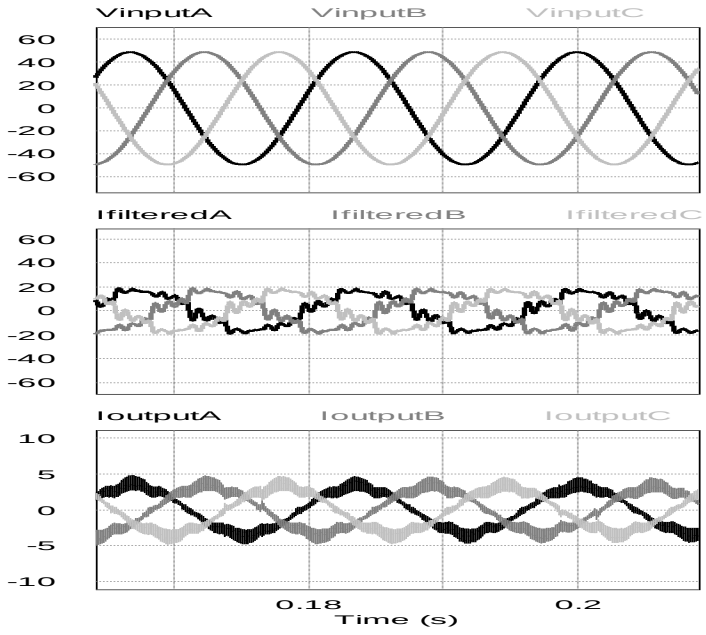


Fig. 4.44 Grid-connected converter. Top to bottom: input phase voltages, filtered input currents, output currents.

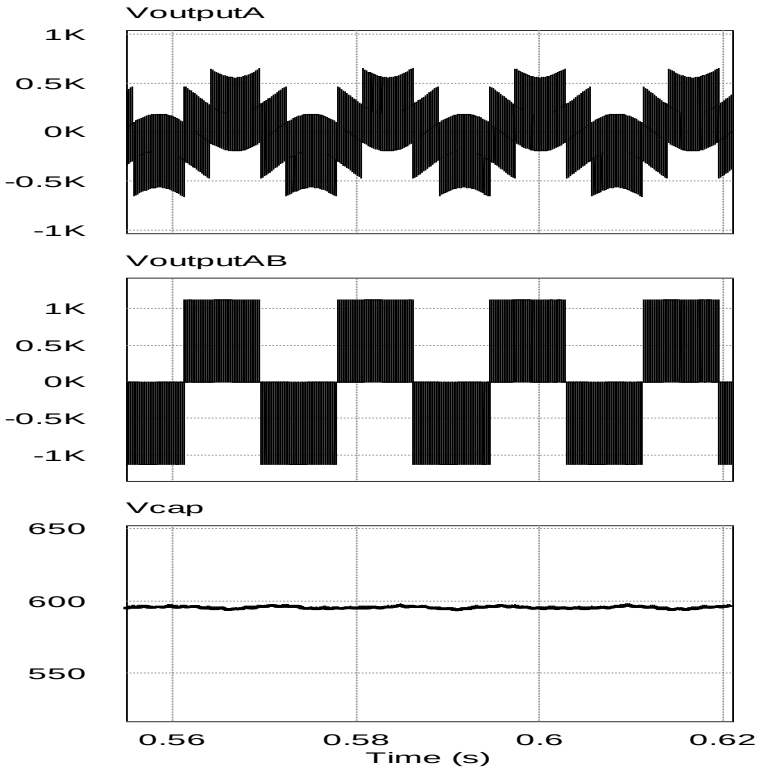


Fig. 4.45 Grid-connected converter. Top to bottom: voltage across the interface inductor, output line-to-line voltage, capacitor-1 voltage.

For further investigation, the boost factor was first set to 2 and increased to 4 at t = 0.25 s. and the results are depicted in Fig.4.46 to Fig.4.48. It can be seen that converter could follow the reference boost command without any voltage and current distortion.

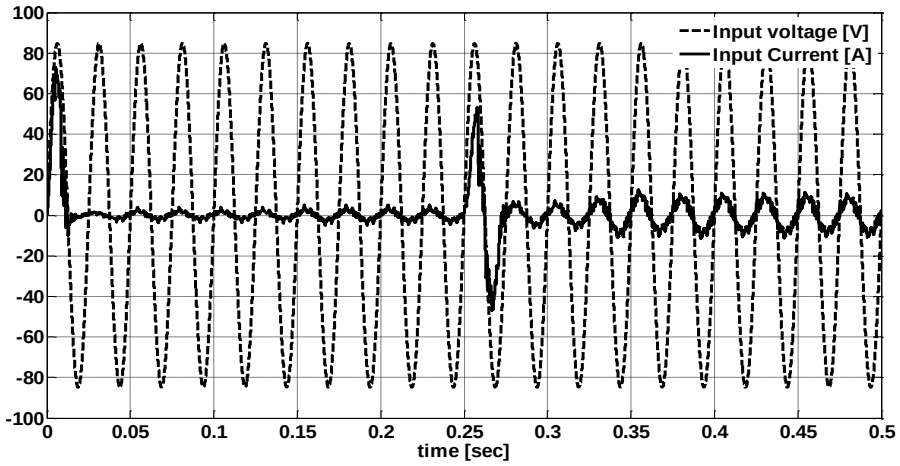


Fig. 4.46 Quasi Z-source matrix converter: phase A input voltage and current.

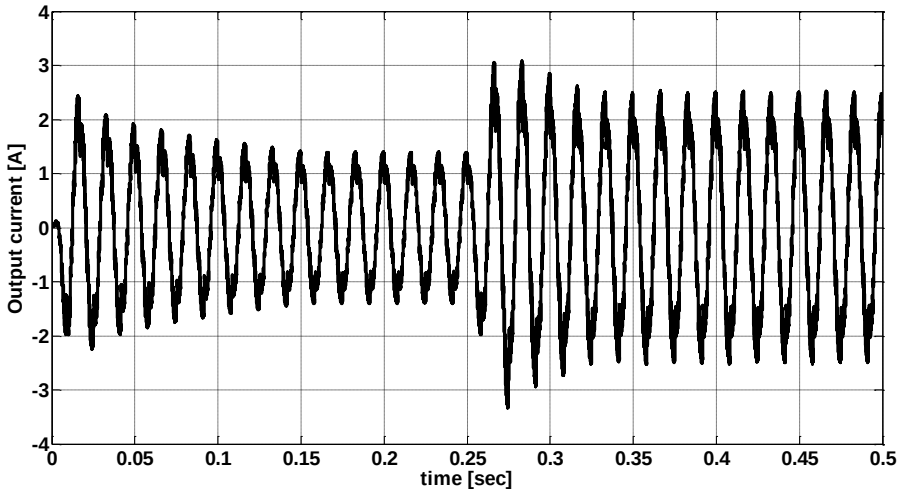


Fig. 4.47 Quasi Z-source matrix converter: phase A output current.

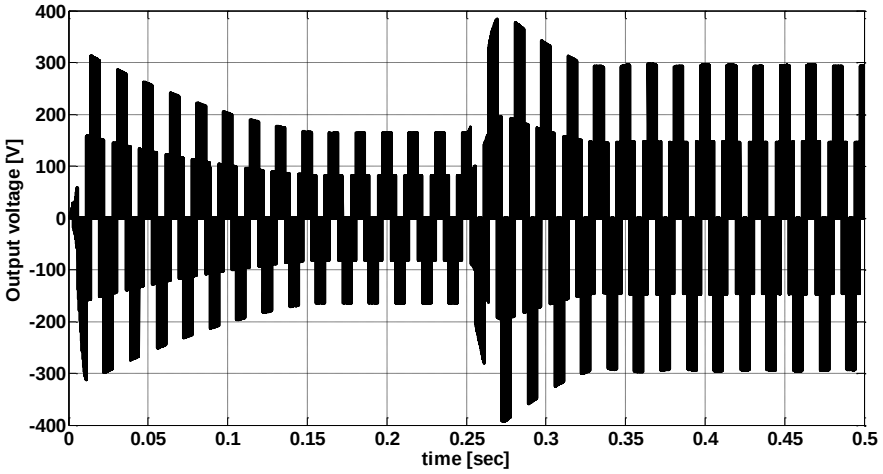


Fig. 4 48 Quasi Z-source matrix converter: phase A output voltage.

4.6.4 Quasi Z-Source Matrix Converter – Experimental Results

In the experiments, the quasi Z-source matrix converter was fed from an AC supply with variable amplitude and constant frequency of 60 Hz and supplied an RL load with boosted output voltages of 40 Hz. System parameters were the same as in the simulations. The results of the experiments for quasi Z-source matrix converter are shown in Figs.4.49 to 4.53.

The modulation index and the boost factor were set to 0.7 and 2.3, respectively. It should be noted that in Figs. 4.49 and 4.50 the input current is shown along the line-line input voltage

which leads the phase voltage by 30°. Consequently, the unity input factor operation is satisfied in the experiments as well.

At high voltage transfer ratios the output line-to-line voltage for the converter has a distorted waveform. The magnitude is limited to the input line-to-line voltages. The input current waveforms presented in Figs. 4.49 and 4.50 is sinusoidal and balanced, proving the effectiveness of the modulation strategy in controlling the converter. The rectification stage is also modulated to generate maximum dc link voltage V_{pn} and provide two voltage levels, so that at any instant, the inversion stage can be operated with the voltage levels. Therefore, according to the selected voltage vectors, the rectification stage is switched as to provide the required voltage levels to the inversion stage.

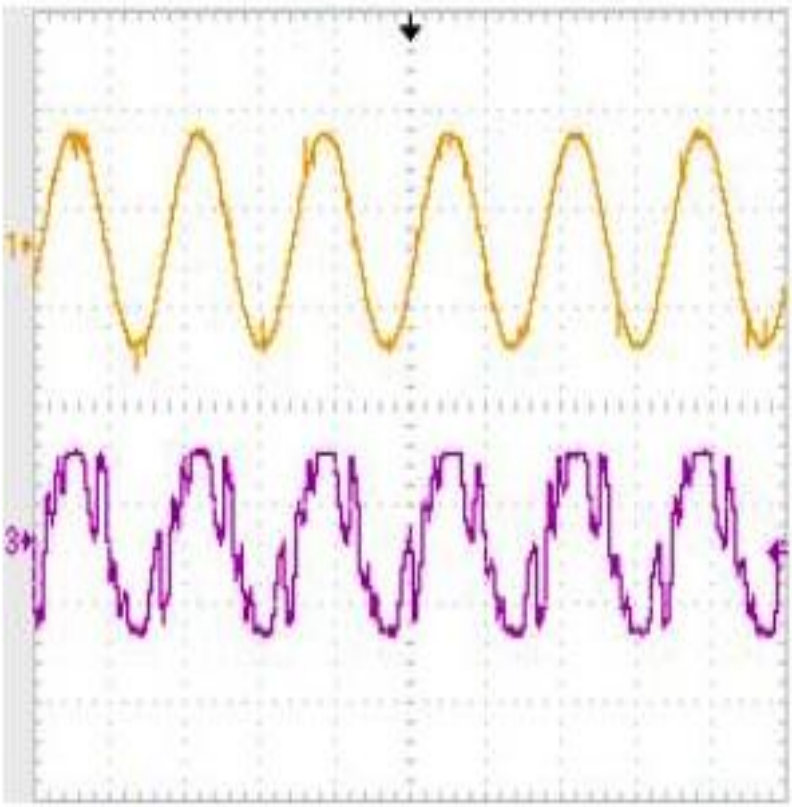


Fig. 4.49 Quasi Z-source matrix converter.Top: line-line input voltage, bottom: phase input current.

Referring to Fig. 4.50, the increase in V_{pn} when the voltage transfer ratio is 2.3 occurs because the rectification stage constantly connects the input line-to-line voltages V_{AB}, V_{BC} and V_{CA} to the inverter terminals, enabling the inversion stage to generate higher output voltages at high voltage transfer ratios.

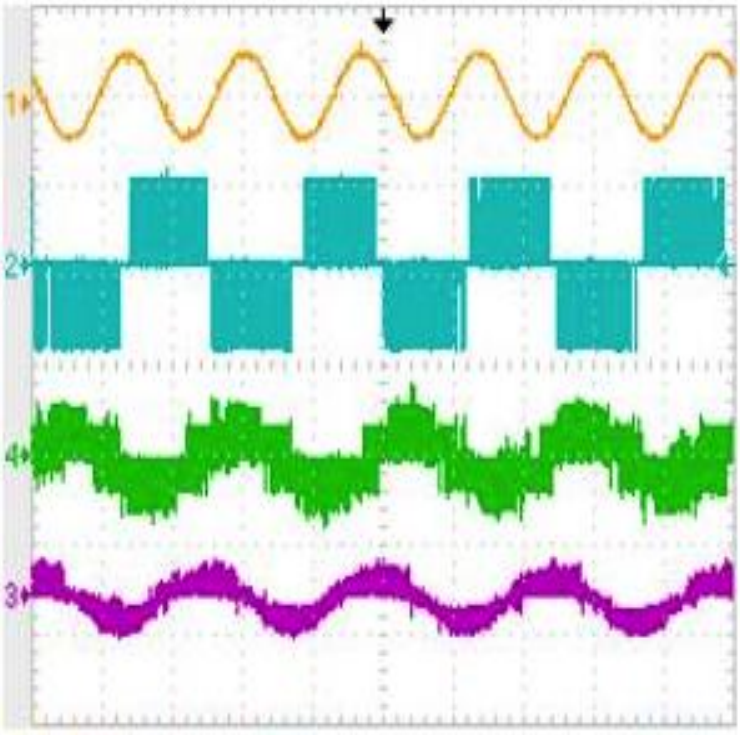


Fig. 4.50 Quasi Z-source matrix converter. Top to bottom: line-line input voltage, line-line output voltage, phase output voltage, output phase current.

At low voltage transfer ratios the quality of the waveforms are increasing and this is valid for the other converters. In Figs. 4.51 to 4.53, the combination of the modulation index and the boost ratio is kept in such a way that the overall voltage transfer is 1.15. It reveals the operation of the rectification stage to control the voltage levels supplied to the inversion stage is superior. The output line to line voltage shows the ability of the quasi Z-source inverter to generate two distinct voltage levels at the output terminal. The modulation strategy is able to control the inverter to generate a set of sinusoidal and balanced output waveforms.

The waveforms of the output line to line voltages for the quasi Z-source inverter are similar to the cascaded Z-source inverter. But the voltage magnitude levels are limited by the boost ratio. Therefore the output switching frequency harmonics for the quasi Z-source inverter is significantly reduced.

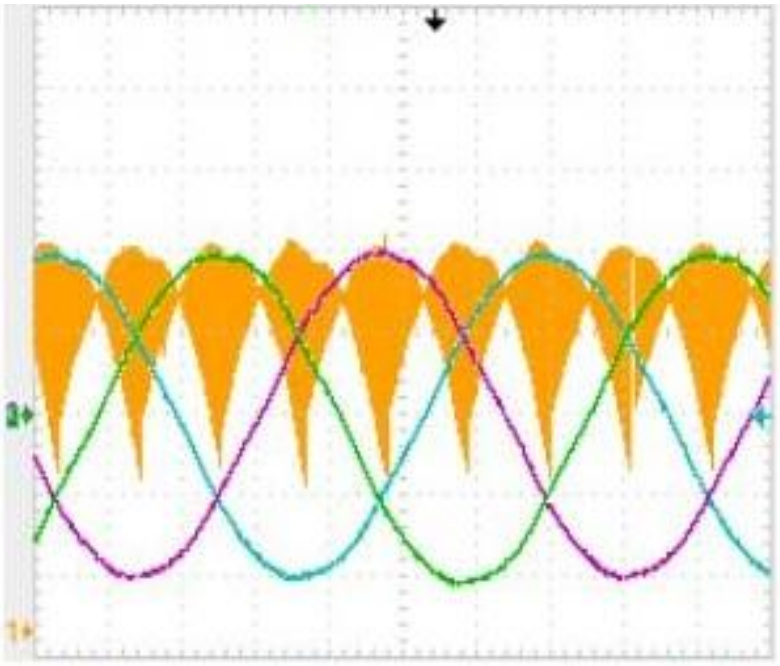


Fig. 4.51 Quasi Z-source inverter: line-line input voltages and dc-link voltage.

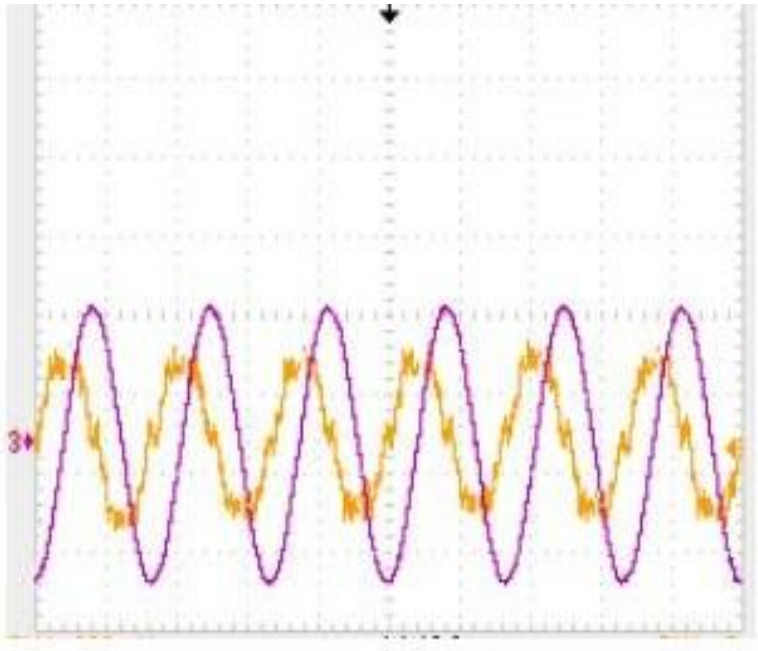


Fig. 4.52 Quasi Z-source inverter: line-line input voltages and input phase current.

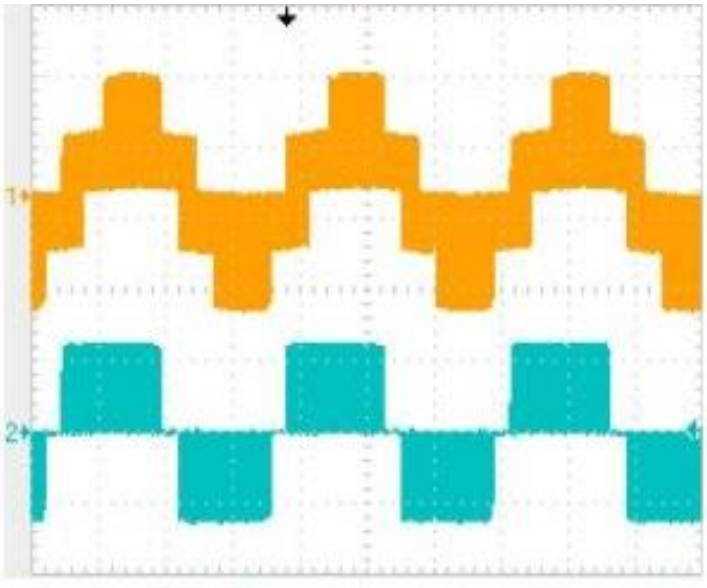


Fig. 4.53 Quasi Z-source inverter: Top to bottom: output phase voltage, output line to line voltage.

4.6.5 Switched Inductor Z-Source Matrix Converter - Simulation Results

In the simulations of the switched inductor Z-source matrix converters, they were fed from a 60-V, 40-Hz three-phase source and supplied a three-phase RL load, or the grid, with a boosted output voltage of 60 Hz. The modulation index was set to 0.7 and the boost ratio to 8. Optimal switching sequence was employed. The parameter values of the system are given in Table 4.4. The components were selected for a rated output power of 2 kW, switching period of 100 μsec, input voltage of 120 V, 60 Hz, and a unity input power factor.

Input AC Source	60 V / 40Hz
Reference Output Voltage	60 Hz
Load, R/L	10 mH / 40 Ω
Input Filter, L/C	2 mH / 2.2 μF
SIZC network, L/C	1 mH / 800 μF
Switching Frequency	10 kHz

Table 4.4 System parameters.

The performance of the investigated converter was evaluated for two operating conditions. In the first simulation, the converter was fed from a 30-V, 40-Hz three-phase source

and supplied a three-phase RL load. The modulation index was set to 0.7. It can be seen that the input voltage and current of phase A are in phase, resulting in a unity power factor. The converter boosts the 30-V input voltage to a 230-V output voltage. Selected voltages and currents waveforms are shown in Fig. 4.54.

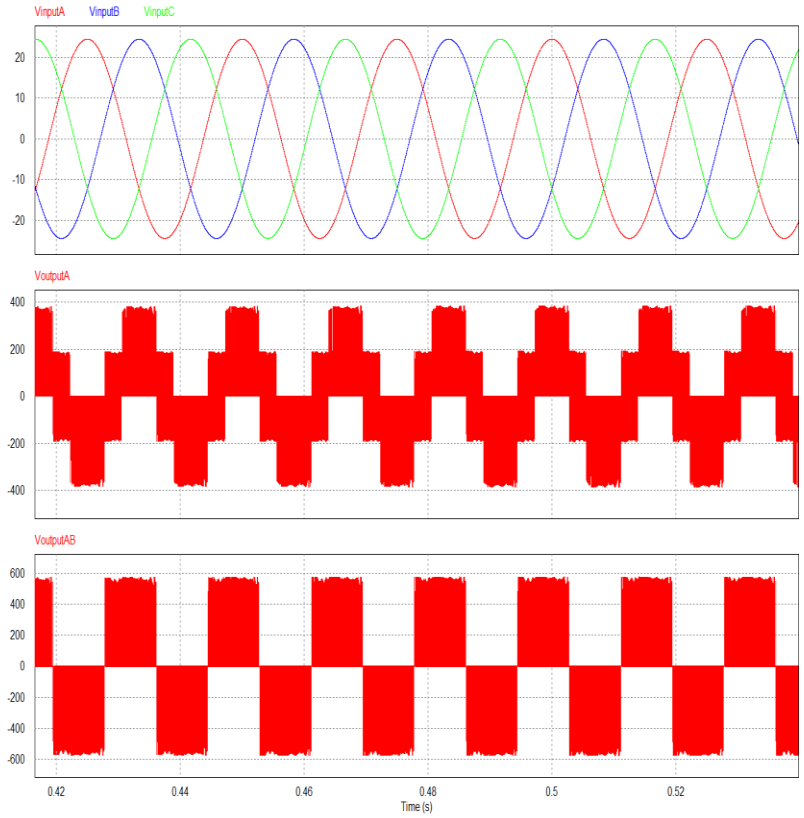


Fig. 4.54 Switched inductor Z-source matrix converter. RL load: input phase voltages, output phase voltage, output line to line voltage.

The effectiveness of the control method can be seen in Fig. 4.55 as all the balanced input and output currents are in phase with the phase voltages. The quality of the input currents is higher than in any other boost converter, and the boost command agrees with the theoretical derivation. The ripple of the capacitor voltage is proportional to the capacitance. High capacitances of the capacitor yield lower ripple. However, high capacitance causes large inrush currents. Fig. 4.56 focuses on selected waveforms.

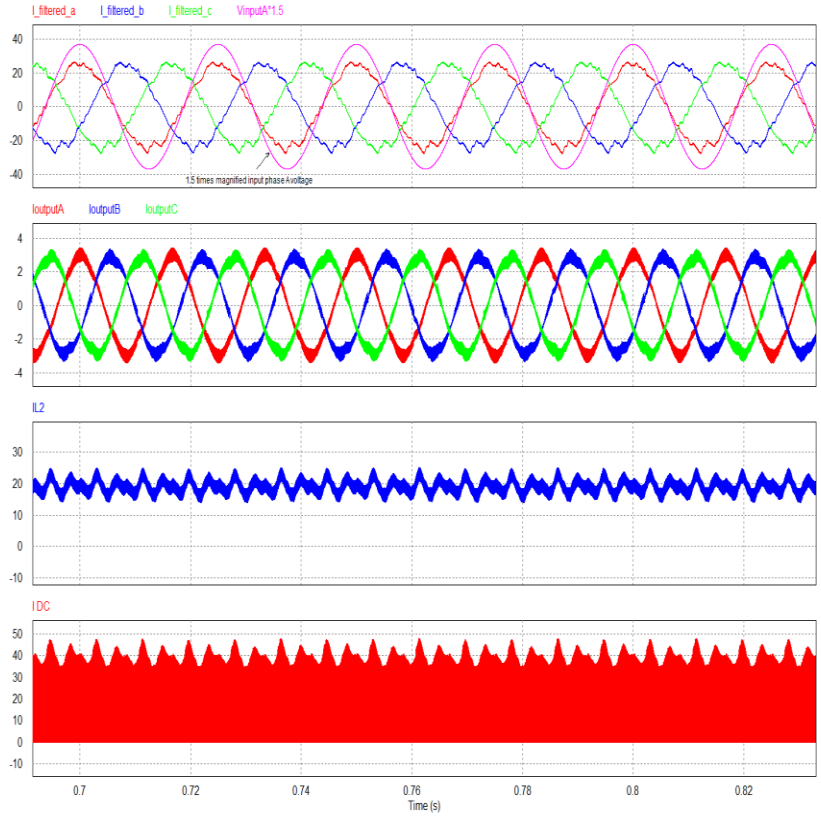


Fig. 4.55 RL load. filtered input currents and the input phase A voltage, output currents, inductor 2 current, dc-link current.

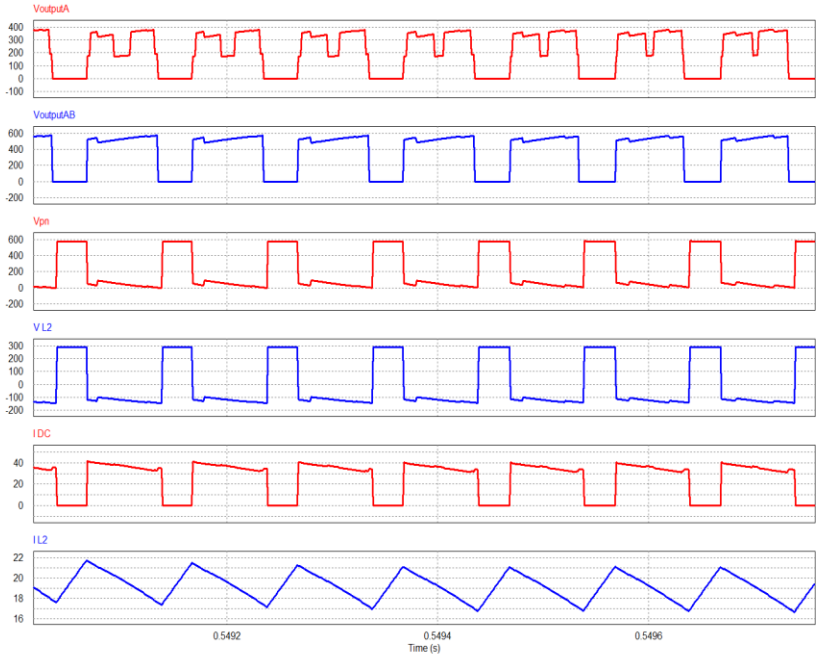


Fig. 4.56 RL load – zoom-in. output phase voltage, output line-to-line voltage, dc-link voltage, inductor 2 voltage, dc-link current, inductor 2 current.

The second set of simulations was carried out for the converter connected to the grid through a 10-mH inductance. The grid was modeled as an ideal 230-V, 60-Hz three-phase ac voltage source. Selected waveforms are shown in Fig. 4.57.

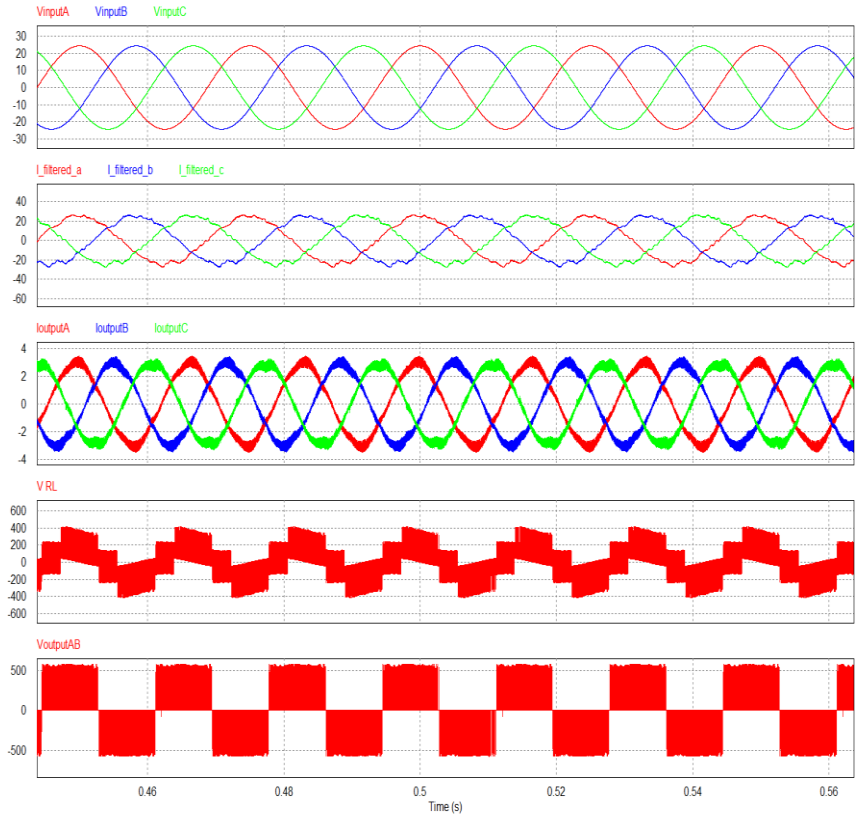


Fig. 4.57 Grid connected switched inductor Z-source matrix converter: input phase voltages, input phase currents, output currents, phase-A voltage across the interface inductor, converter output voltage before the inductor

The main advantage of this converter is its high voltage boosting ability. The proposed converter is suitable for all applications with unidirectional power flow. Bidirectional power flow can be obtained by employing three more switches in the rectifier part, converting the ultra-sparse matrix input stage to a sparse matrix one. The converter's reliability is high thanks to a low number of semiconductor devices and a non-hazardous shoot-through state in the output stage.

The performance of the proposed converters was evaluated for two values of the boost factor. It was set to 3 and increased to 6 at t = 0.25 s. The results are depicted in Figs. 4.58 to 4.60. It should be noted that the input voltage and current of phase A are in phase, resulting in a unity input power factor.

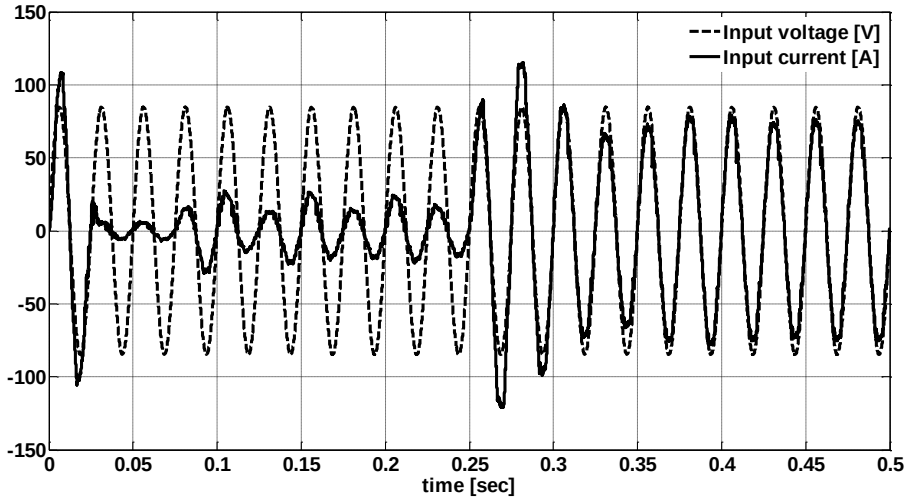


Fig. 4.58 Switched inductor Z-source matrix converter: phase A input voltage and current.

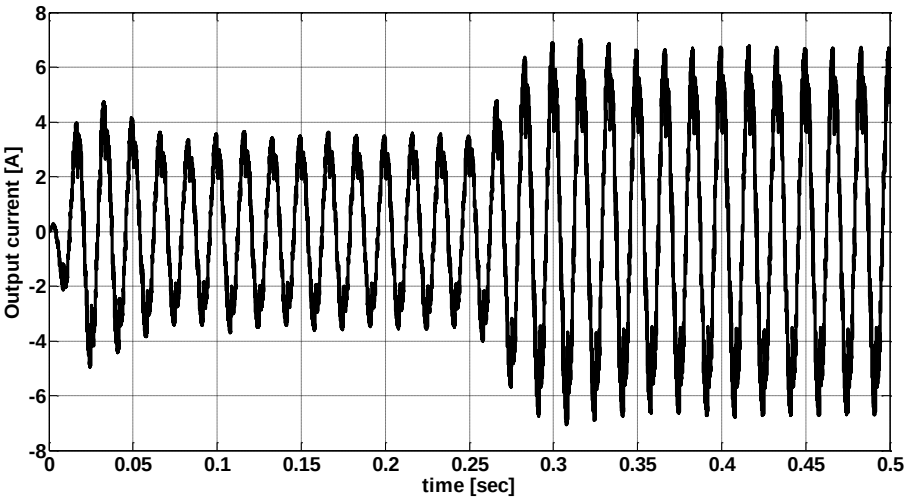


Fig. 4.59 Switched inductor Z-source matrix converter: phase A output current.

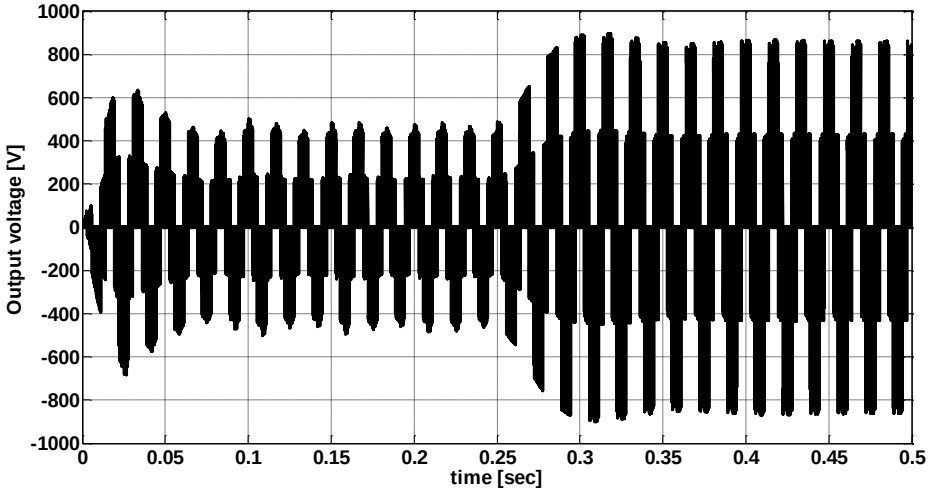


Fig. 4.60 Switched inductor Z-source matrix converter: phase A output voltage.

4.6.6 Switched Inductor Z-Source Matrix Converter - Experimental Results

In the experiments, the converters were fed from an AC supply with variable amplitude and constant frequency of 60 Hz, and supplied an R-L load with boosted 40 Hz output voltages. The system parameters were the same as in the simulations.

Selected waveforms of the switched inductor Z-source matrix converter are shown in Figs. 4.61 to 4.65. The modulation index and the boost factor were set to 0.7 and 3, respectively. It should be noted that in Fig. 4.61 the input current is depicted along the line-line input voltage, which leads the phase voltage by 30°. Consequently, the unity input factor condition is satisfied in the experiments.

Here, the modulation index *m* is generally reduced, which means the shoot-through duration is increased, until the output voltage meets the commands. From Figs. 4.62 and 4.62 it can be found that the Z-source capacitor voltage has been boosted three times. Thus, this brings the output voltage to the reference voltage level. In Fig. 4.64 the output current is still sinusoidal and has the required frequency. Thus, the switched inductor Z-source matrix converter successfully operates as a boost AC-AC converter.

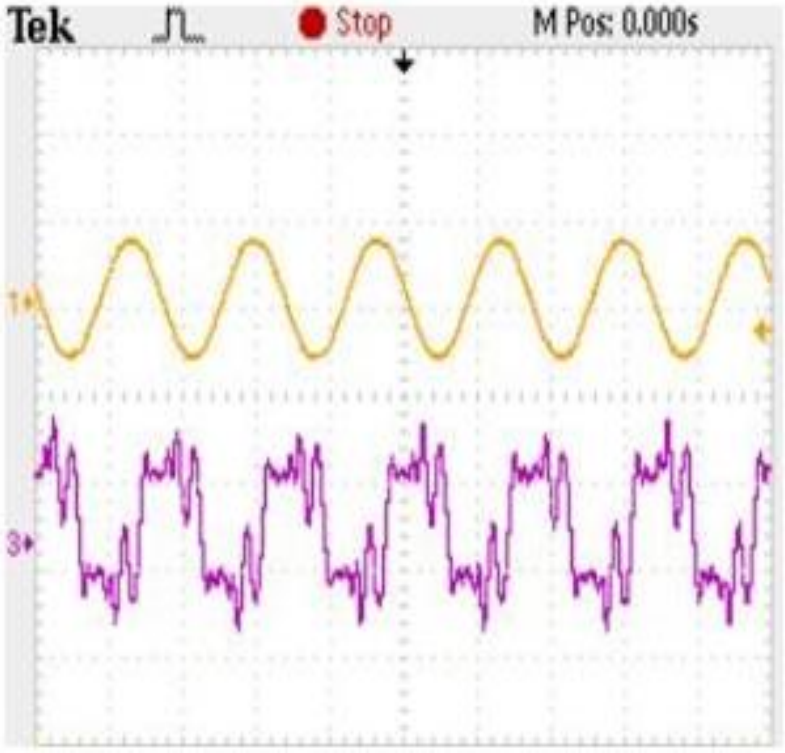


Fig. 4.61 Switched inductor Z-source matrix converter. Top: line-line input voltage, bottom: phase input current.

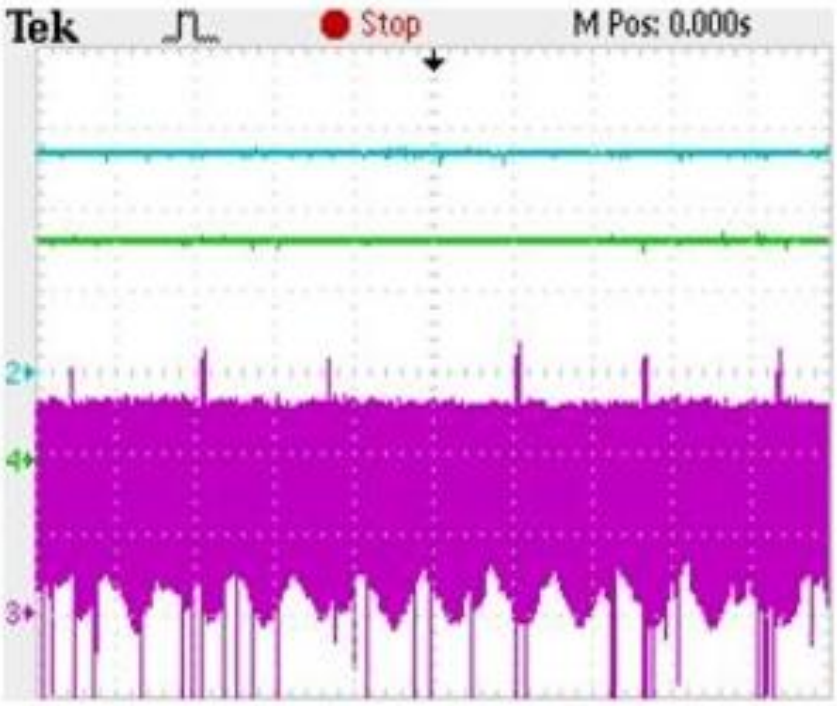


Fig. 4.62 Switched inductor Z-source matrix converter. Top: Z-source network capacitor voltages, bottom: line-line input voltage.

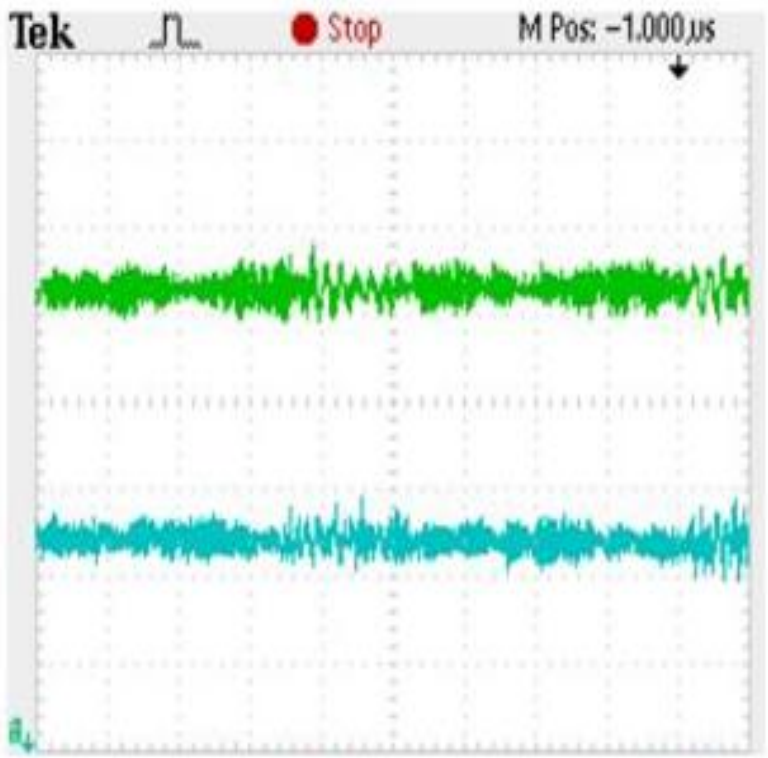


Fig. 4.63 Switched inductor Z-source matrix converter. Top: Zoomed Z-source network capacitor voltages, bottom: line-line input voltage.

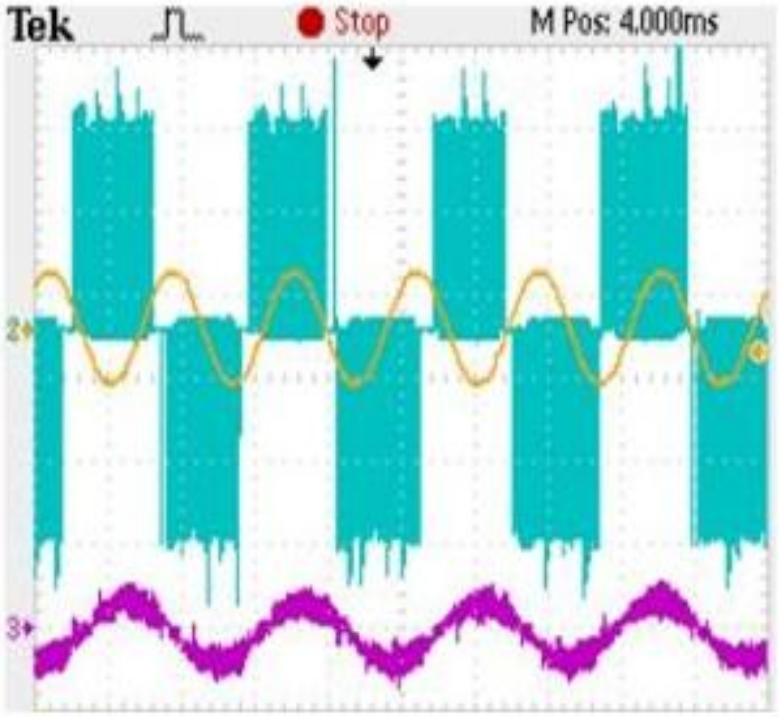


Fig. 4.64 Switched inductor Z-source matrix converter. Top: Line to line output voltage and input voltage, bottom: phase output current.

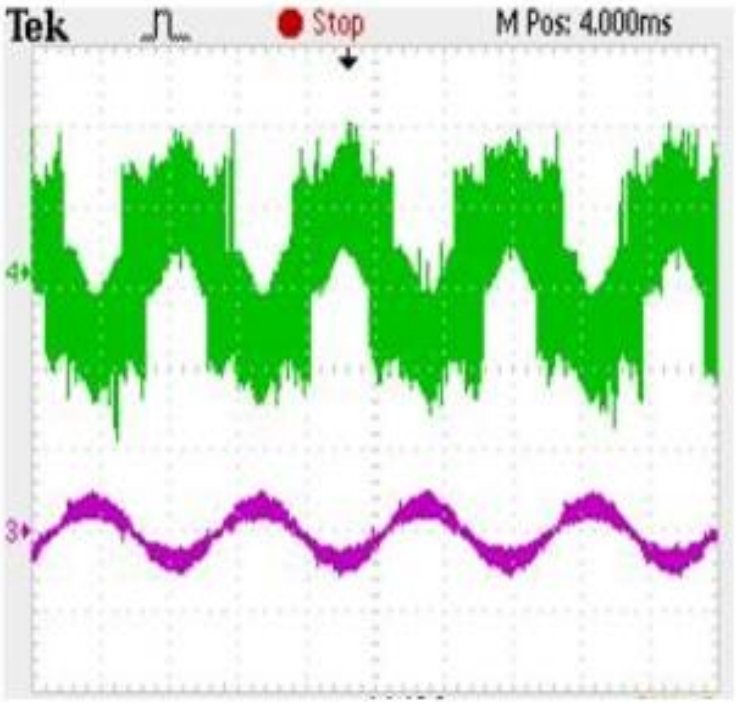


Fig. 4.65 Switched inductor Z-source matrix converter. Top: Output phase voltage bottom: phase output current.

4.7 FFT Analysis of Input and Output Currents

To compare the quality of output currents of the converters, the fast Fourier transform (FFT) analysis was carried out and the total harmonic distortion (THD) of the currents was calculated for the fundamental output frequency of 60-Hz, modulation index of 0.7, and boost factors of 1 to 6. Figs. 4.66 and 4.67 show the harmonic spectra of output currents of the series Z-source and cascaded Z-source matrix converters for B = 3, respectively. In the series Z-source converter, the THD of the output current is 4.1 %, while the output current of the cascaded Z-source converter has a THD of 4.6 %. Fig 4.68 summarizes the THD of the series Z-source and the cascaded Z-source matrix converter currents versus various boost factors. The maximum THD for the cascaded Z-source matrix converter occurs at B = 1, while B = 3 gives the highest THD in the series Z-source converter.

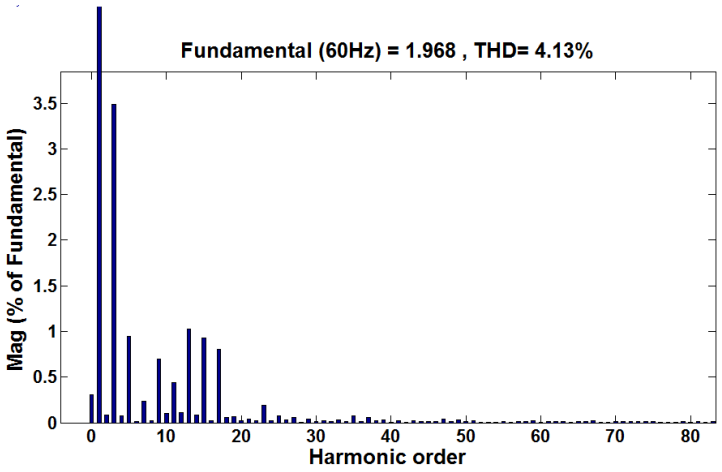


Fig. 4.66 Harmonic spectrum of the output current of series Z-source matrix converter with B = 3, m = 0.7 and f_{out} = 60 Hz.

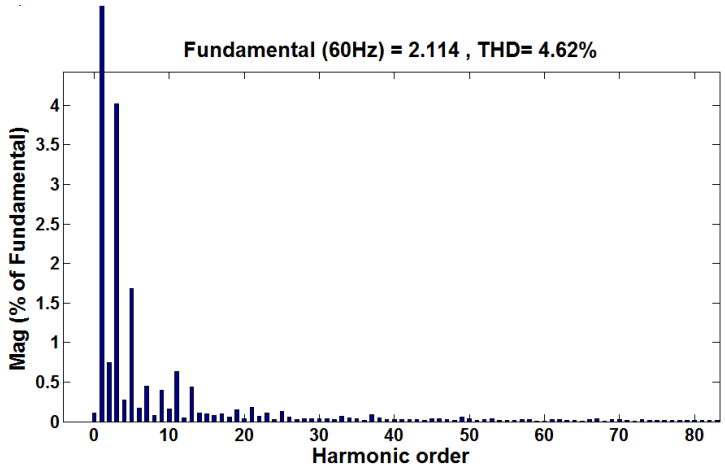


Fig. 4.67 Harmonic spectrum of the output current of cascaded Z-source matrix converter with B = 3, m = 0.7 and f_{out} = 60 Hz.

A similar analysis was carried out for the switched inductor Z-source matrix converter. The FFT and THD were calculated for the input frequency of 40 Hz, output frequency of 60 Hz, modulation index of 0.7 and boost factors of 1 to 6. Figs. 4.69 and 4.70 show the harmonic spectra of the input and output currents of the converter for B = 3. The THD of the input current is 10.6% and that of the output current is 4.9%.

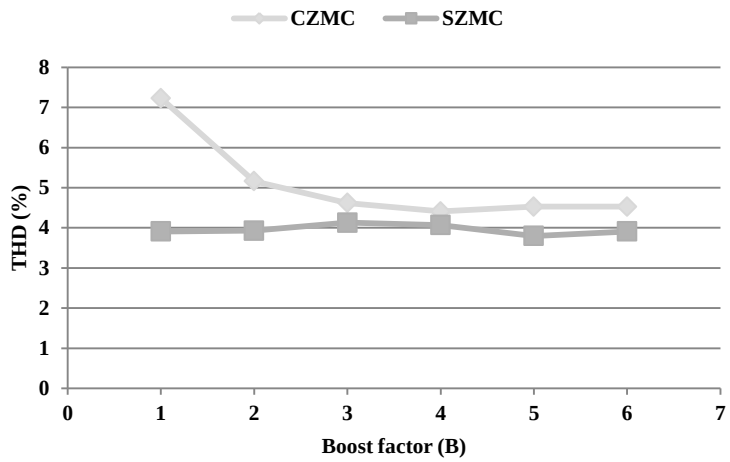


Fig. 4.68 THD of the output current of cascaded Z-source and series Z-source matrix converters vs. the boost factor.

The diagram in Fig.4.69 relates the THD of the converter's currents to the boost factors. It can be seen that the maximum THD for both the input and output currents occurs at the lowest boost factor i.e., unity. When the boost factor increases the current waveforms improve.

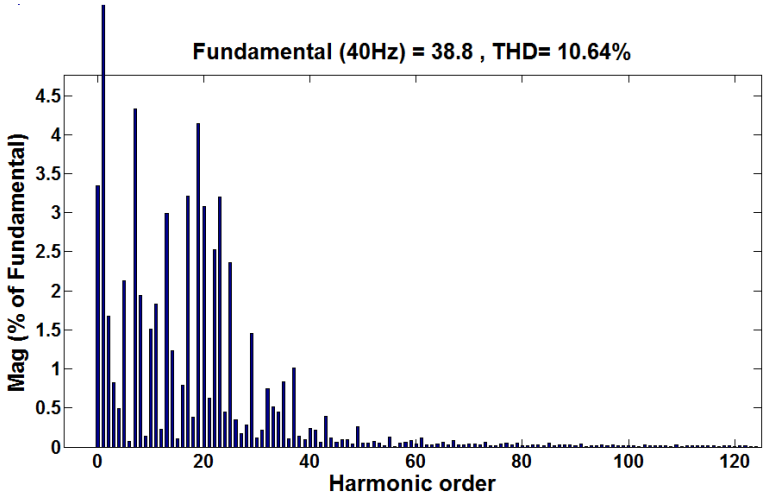


Fig. 4.69 Harmonic spectrum of the input current of switched inductor Z-source matrix converter with B = 3, m = 0.7 and f_{in} = 40 Hz.

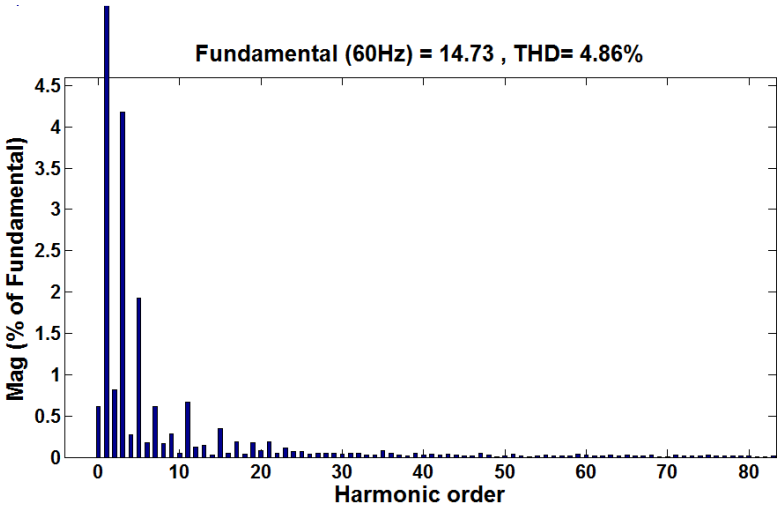


Fig. 4.70 Harmonic spectrum of the output current of switched inductor Z-source matrix converter with B = 3, m = 0.7 and f_{out} = 60 Hz.

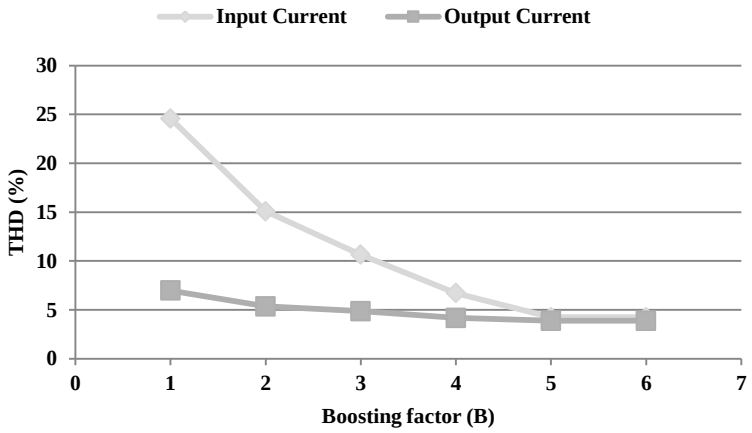


Fig. 4.71 THD of input and output currents in the switched inductor Z-source matrix converter with B = 3, m = 0.7 and f_{in} = 40 Hz.

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The same analysis was performed for the quasi Z-source matrix converter, and the results are shown in Figs.4.72 and 4.73. For B = 3, THD of the converter input current is 10.8 %, while the output current has a THD of 4.2%. As in the switched inductor Z-source converter, the maximum THD for both input and output currents occurs at B = 1.

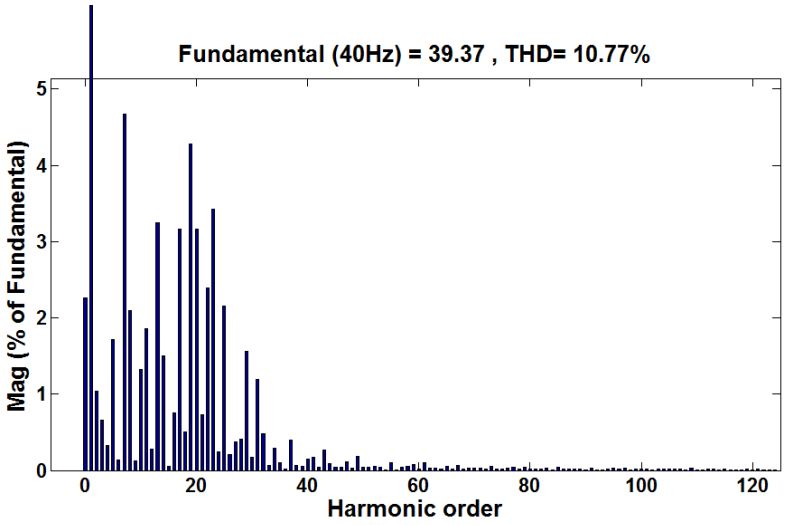

Fig. 4.72 Harmonic spectrum of the input current of quasi Z-source matrix converter with B = 3, m = 0.7 and f_{in} = 40 Hz.

Comparing Figs. 4.69 and 4.72, it can be concluded that the switched inductor Z-source matrix converter draws currents with lower harmonic distortion while both converters produce load currents of the same quality.

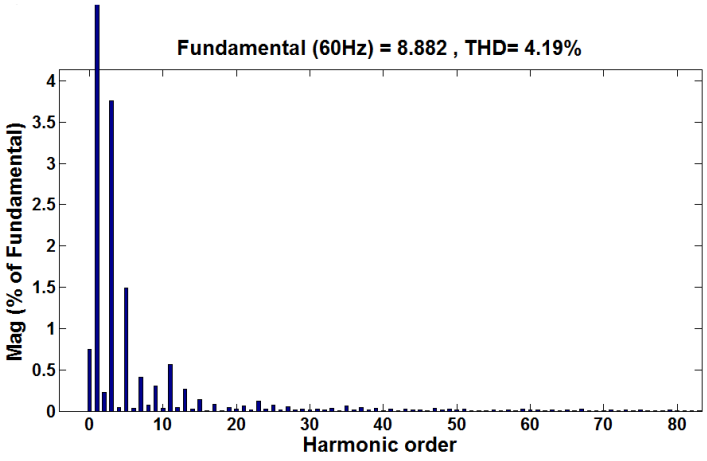

Fig. 4.73 Harmonic spectrum of the output current of quasi Z-source matrix converter with B = 3, m = 0.7 and f_{out} = 60 Hz.

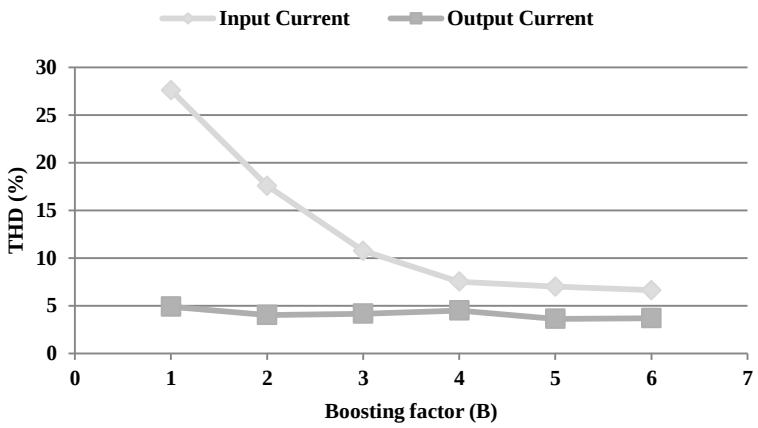

Fig. 4.74 Total harmonic distortion of the quasi Z-source matrix converter's input and output currents.

4.8 Conclusion

The series, quasi, and switched-inductor Z-source circuits have been combined with the ultra-sparse matrix converter topology to create novel three-phase to three-phase matrix converters with voltage-boosting capability and a unity power factor. The converters are suitable for all applications with unidirectional power flow.

Bidirectional power flow can be made possible by adding three more switches to the rectifier part, converting the ultra-sparse matrix input stage to a sparse-matrix one. The Converter's reliability is high due to a low number of semiconductor devices and a non-hazardous shoot-through state in the output stage. As such, it is particularly well suited for residential energy systems with gearless synchronous generators, where the power electronic generator-grid interface must reconcile a significant voltage disparity between those two systems.

The modulation of the boost matrix converter is attractive because the input currents and the output voltages are controlled within one algorithm. In traditional indirect drives, the dc link

provides a link to decouple of the two controls. The combined space vector strategies has been focused with three states: active, zero and shoot-through states.

The Space vector modulation utilizes the voltage transfer ratio of the boost matrix converter to its full theoretical extent. The input currents are sinusoidal with controllable displacement angle. This gives the opportunity to control the input power factor to unity. This is especially important if the converters are connected to the utility grid directly: in heavy industries the input lines are in parallel with capacitors to control the reactive power. In such cases the converter needs to control the input power factor under varying conditions.

An optimized modulation strategy was presented. Based on minimizing the number of switchings in the converter. Supportive rules were provided. The fast Fourier transform analysis of the converters input/output currents was carried out, indicating slight superiority of the switched inductor Z-source matrix converter over the quasi Z-source converter and the series Z-source matrix converter over the cascaded Z-source converter with respect to the quality of input currents.

Chapter 5

Single-Phase Boost Matrix Converters

5.1 Introduction

Research on matrix converters, including the sparse ones, has been mostly focused on three-phase to three-phase topologies, PWM strategies, applications, and performance improvement. Papers on three-phase to single-phase matrix converters are relatively scarce. This chapter proposes two three-phase to single-phase matrix converters, namely:

1. Super-sparse Z-source matrix converter for buck-boost type voltage conversion.
2. Super-sparse switched-inductor Z-source matrix converter for high-boost type voltage conversion.

A novel PWM technique has been developed for control of these converters, and described in this chapter.

5.2 Topologies

The proposed power converters are based on the concept of super-sparse matrix topology, having the minimum number of semiconductor switches. With the novel modulation technique, the output voltage is unipolar, reducing the stress on the load-side switches and losses in these switches. The limited output voltage constitutes the well-known disadvantage of classic matrix converters. To overcome this shortcoming, various control algorithms and topologies have been proposed. In particular, as already explained in the Chapter 4, use of the Z-source network allows increasing the voltage transfer ratio to unity and above. In those indirect-matrix topologies, the basic function of the converter is realized by splitting the ac-to-ac conversion into the ac-to-dc

and dc-to-ac stages. A Z-source network is placed between the line-side rectifier stage and the load-side inverter stage, allowing boosting the voltage by two to three times. It allows boosting the voltage several times.

A super-sparse single-phase to three-phase matrix converter, shown in Fig. 5.1, has been obtained by eliminating one leg from the end stage of the similar traditional three-phase to three-phase converter. Figs. 5.2 and 5.3 show how the Z-source and switched-inductor Z-source have been employed to obtain a voltage-boosting capability. The three-dimensional inductive-capacitive topologies of these sources allow boosting the voltage by varying the change rate of current in the inductors.

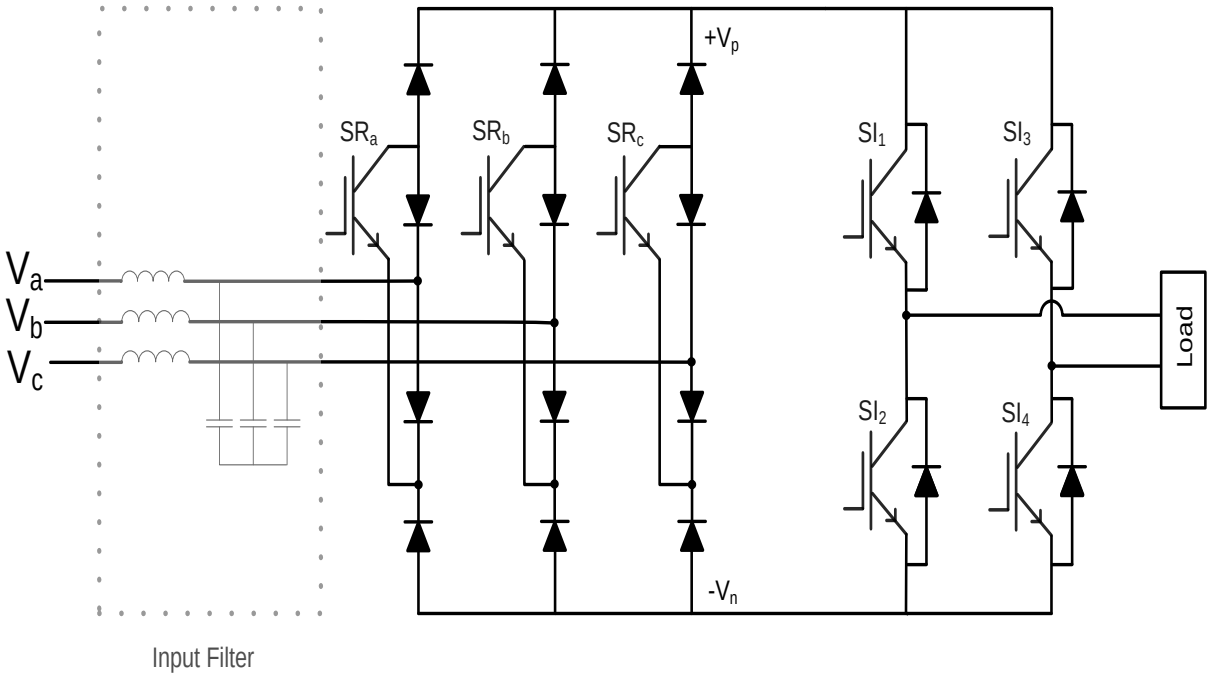

Fig. 5.1 Three-phase to single-phase super-sparse matrix converter.

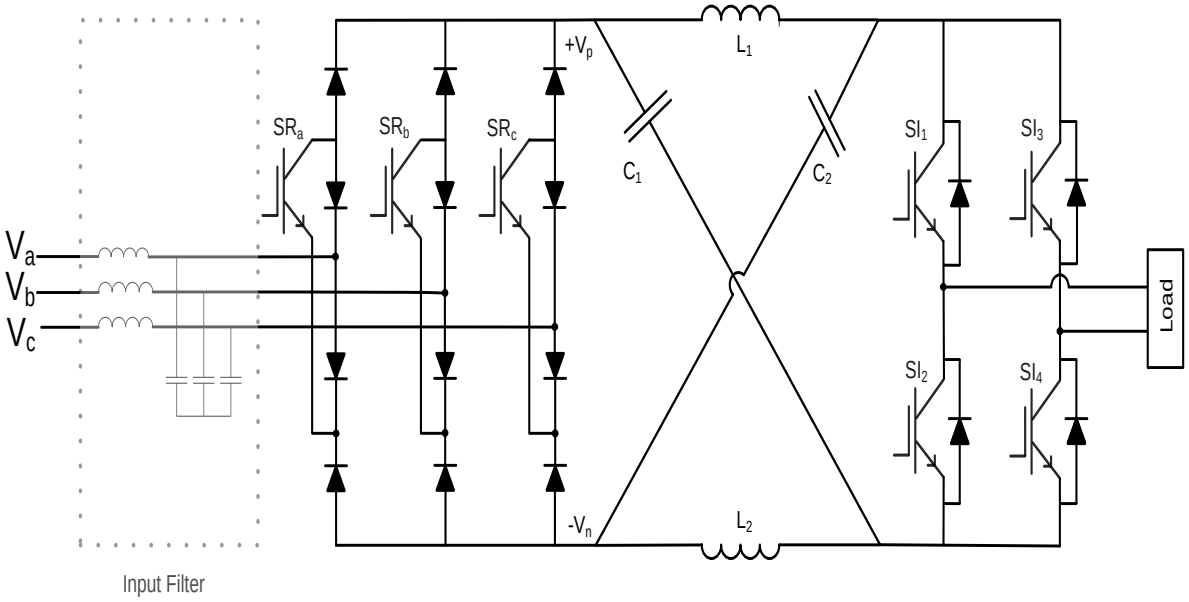

Fig. 5.2 Three-phase to single-phase super-sparse Z-source matrix converter.

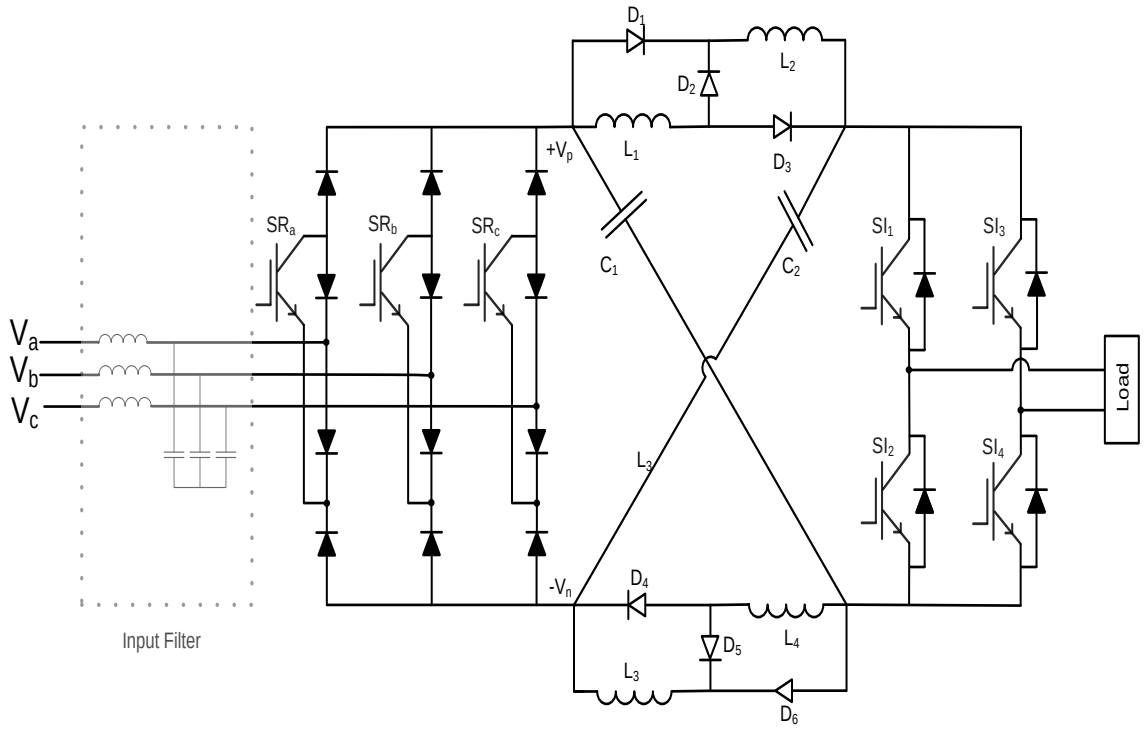

Fig. 5.3 Three-phase to single-phase super-sparse switched-inductor Z-source matrix converter.

5.3 Control Strategy

Control of the developed converters is based on a combination of the space-vector rectification and inversion PWM techniques. The front-end rectifier, whose one leg is depicted in Fig. 5.4, draws sinusoidal input currents and controls the input displacement angle. For a unity input power factor, the reference input phase current vector is aligned with that of the input phase voltage.

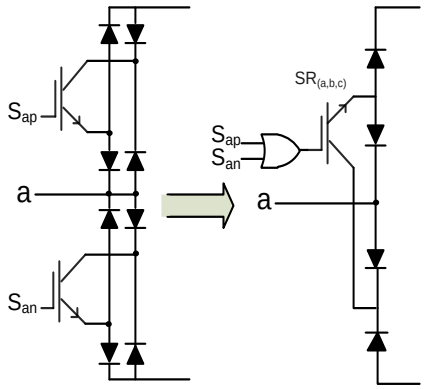

Fig. 5.4 Legs of the front-end rectifier. Left: sparse matrix converter, right: ultra-sparse matrix converter.

Input current vectors are shown in Fig. 5.5 For example, (S_{ap}, S_{cn}) indicates that the input phase "a" is connected to the positive (top) rail "p" and phase "c" is connected to the negative (bottom) rail "n". In the ultra-sparse topology, switching signals of the same leg, e.g., S_{ap} and S_{an}, must be merged using the "OR" operator. The new switching signals ($S_{ap} \| S_{an}$) turn switch SR_a on and off for rectification. The three-switch rectifier stage has three active vectors (011, 010, and 101) and four non-active vectors (000, 001, 010, and 100), where 0 and 1 denote turned-off and turned-on switches, respectively.

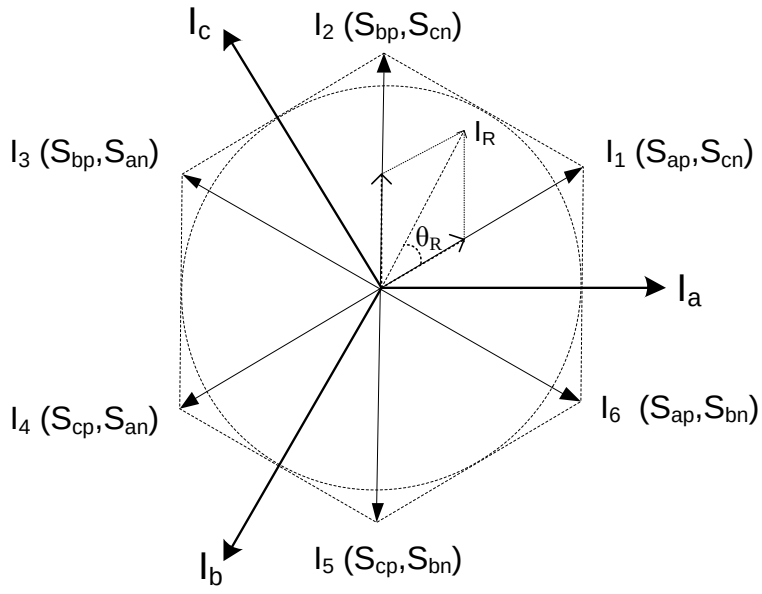

Fig. 5.5 Input current vectors.

The reference current vector is synthesized from the adjacent active vectors and a zero vector. Denoting the local angle of the reference current by θ_R, the duty ratios of the active, d_λ, d_δ, and zero, d_{0R}, vectors are calculated as

$$d_\lambda = m_c \sin\left(\frac{\pi}{3} - \theta_R\right) \tag{5.1}$$

$$d_\delta = m_c \sin(\theta_R) \tag{5.2}$$

$$d_{0R} = 1 - (d_\lambda + d_\delta) \tag{5.3}$$

where m_c is the current modulation index. The placement of the reference vector within one of the 60^o sectors is defined by switching vectors I_λ and I_δ. For example, as seen in Fig. 5, if $\lambda = 6$ then the adjacent vector $\delta = 1$. The input voltages are given by

$$V_a = V_m \sin(\omega_0 t) \tag{5.4}$$

$$V_b = V_m \sin\left(\omega_0 t - \frac{2\pi}{3}\right) \tag{5.5}$$

$$V_c = V_m \sin\left(\omega_0 t + \frac{2\pi}{3}\right) \tag{5.6}$$

In the end inverter, unipolar modulation has been employed. Although bipolar modulation is also feasible, the unipolar modulation is preferred since it allows a higher modulation index for the Z-source and switched-inductor Z-source topologies. It also produces fewer harmonics. The shoot-through state produces the voltage boost for both the converters mentioned, but is forbidden for the super-sparse matrix converter. Duty ratios of the inverter switches are

$$0 < \omega t < \pi: \begin{cases} SI_1: d_{an} = m_v \sin(\omega t) \\ \mathrm{SI}_2: d_{an\_zero} = 1 - m_v \sin(\omega t) \\ \mathrm{SI}_3: 0\ (off\ at\ all\ times) \\ \mathrm{SI}_4: 1\ (on\ at\ all\ times\ ) \end{cases} \tag{5.7}$$

$$\pi < \omega t < 2\pi: \begin{cases} SI_1: 0\ (off\ at\ all\ times) \\ \mathrm{SI}_2: 1\ (on\ at\ all\ times) \\ \mathrm{SI}_3: d_{bn} = m_v \sin(\omega t - \pi) \\ \mathrm{SI}_4: d_{bn\_zero} = 1 - m_v \sin(\omega t - \pi) \end{cases} \tag{5.8}$$

where m_v is the voltage modulation index and ω is the fundamental output radian frequency in rad/sec.

The time-averaged power outputs from the three-switch rectifying stage and the inverter stage are equal. This allows for the combination of the two modulation strategies. As illustrated in Fig. 5.6(a), assuming the input displacement angle of zero, the combined duty ratios are given by

$$d_{\lambda_{an}} = d_\lambda \times d_{an} = m_c m_v \sin(\omega t) \sin\left(\frac{\pi}{3} - \theta_R\right) \tag{5.9}$$

$$d_{\delta_{an}} = d_\delta \times d_{an} = m_c m_v \sin(\omega t) \sin(\theta_R) \tag{5.10}$$

$$d_0 = 1 - 2 \times \left(d_{\lambda_{an}} + d_{\delta_{an}}\right) \tag{5.11}$$

However, as seen in Fig. 5.6(b), for the Z-source and switched-inductor Z-source converters the shoot-through state must be included in the vector sequence as well. It should be noted that the duty ratios of the inverter switches for $0 < \omega t < \pi$ and $\pi < \omega t < 2\pi$ are different. Thus, the shoot-through and combined duty ratios for these converters are calculated using the following equations:

For the Z-source matrix converter:

$$d_{sh\_th} = \frac{1-B}{1-2B} \tag{5.12}$$

$$0 < \omega t < \pi \rightarrow \begin{cases} d_{\lambda_{an}} = d_{\lambda} \times d_{an} \\ d_{\delta_{an}} = d_{\delta} \times d_{an} \\ d_{0\_th} = 1 - \left(d_{\lambda_{an}} + d_{\delta_{an}} + d_{sh\_th}\right) \end{cases} \tag{5.13}$$

$$\pi < \omega t < 2\pi \rightarrow \begin{cases} d_{\lambda_{bn}} = d_{\lambda} \times d_{bn} \\ d_{\delta_{bn}} = d_{\delta} \times d_{bn} \\ d_{0\_th} = 1 - \left(d_{\lambda_{bn}} + d_{\delta_{bn}} + d_{sh\_th}\right) \end{cases} \tag{5.14}$$

where *B* is the boost factor.

The only difference for switched-inductor Z-source matrix converter is the shoot-through duty ratio which is given by

$$d_{sh\_th} = \frac{B-1}{3B+1} \tag{5.15}$$

The corresponding switching times can be then calculated as

$$T_{\lambda_{an}} = T_s \times \frac{d_{\lambda_{an}}}{2}, \quad T_{\delta_{an}} = T_s \times \frac{d_{\delta_{an}}}{2}, \quad T_{\lambda_{bn}} = T_s \times \frac{d_{\lambda_{bn}}}{2} \tag{5.16}$$

$$T_{\delta_{bn}} = T_s \times \frac{d_{\delta_{bn}}}{2}, \quad T_0 = T_s \times d_0, \quad T_{sh\_th} = T_s \times d_{sh\_th} \tag{5.17}$$

$$T_{0\_th} = T_s \times \frac{d_{0\_th}}{2} \tag{5.18}$$

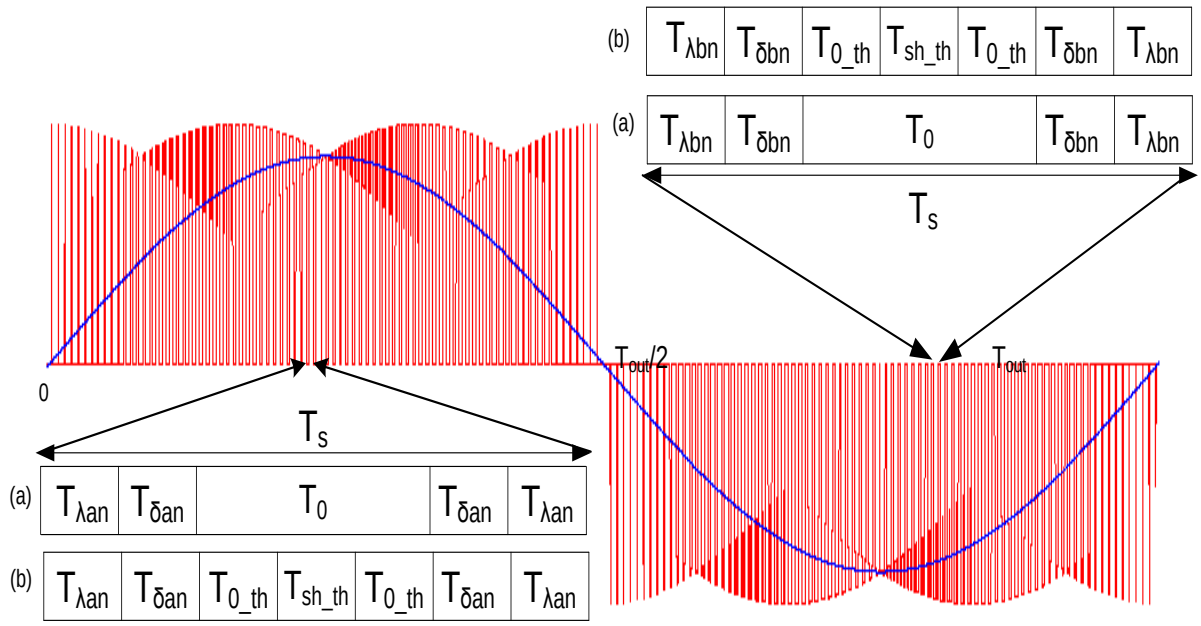

Fig. 5.6 State sequences within one switching cycle: (a) super-sparse matrix converter, (b) Z-source and switched-inductor Z-source matrix converters.

It can be seen in the already presented Fig. 5.6 that in the super-sparse matrix converter two combinations of input current and output voltage vectors are imposed in the first half of the switching period and followed by a zero vector state. Then active vectors are applied in a reverse order. The duty ratio of each vector state is the duty ratio of the current vector multiplied by the duty ratio of the inverter switches. For the Z-source and switched inductor Z-source matrix converts, the shoot-through state is introduced to boost the voltage.

Zero-vector modulation is important for double sided modulation. As a general rule for the super-sparse matrix converter, in the first half cycle, the λ-δ-0-δ-λ sequence should be followed, while in the second half of the cycle, it should be the δ-λ-0-λ-δ sequence. For both the Z-source and switched switched-inductance matrix converters the same principle should be

observed, however the “0” should be replaced by the 0_th–shoot-through–0_th sequence in both the first and second cycles.

The general idea of the indirect modulation strategy is to decouple the controls of input current and output voltage. The output voltage duty ratios depend on the input current phase angle. This may affect the modulation quality of output voltage, but keeping the input power factor close to unity minimizes this negative effect.

5.4 Circuit Analysis

5.4.1 Z-source Circuit

An equivalent circuit of the Z-source, placed between the rectifier and inverter stages, is shown in Fig. 5.7(a) for the non-shoot-through states and in Fig. 5.7(b) for the shoot-through states. In the non-shoot-through states, the rectifier stage produces $V_{an}, V_{bn}, V_{cn},$ or zero, depending on the position of the input current vector. Capacitors C_1 and C_2 are charged by any of the rectified input voltages. In Fig. 5.7(b), the inverter is operating under the shoot-through condition to provide the voltage boost. The duration of the shoot-through state depends on the desired voltage boost factor. Due to the reverse-biased rectifier diodes, the coupling between the rectifier and inverter stages is broken. Inductor L_1 is charged by C_1 and inductor L_2 is charged by C_2. Analysis of the equivalent circuits in Fig.5.7 yields the following relations: $V_c = (1-D)V_{pn}/(1-2D)$, boost factor, $B = 1/(1-D)$, the capacitor currents, $I_c = (1-D)V_{dc}/R_L$, and the inductor currents, $I_L = (1-D)^2 V_{dc}/(1-2D)R_L$.

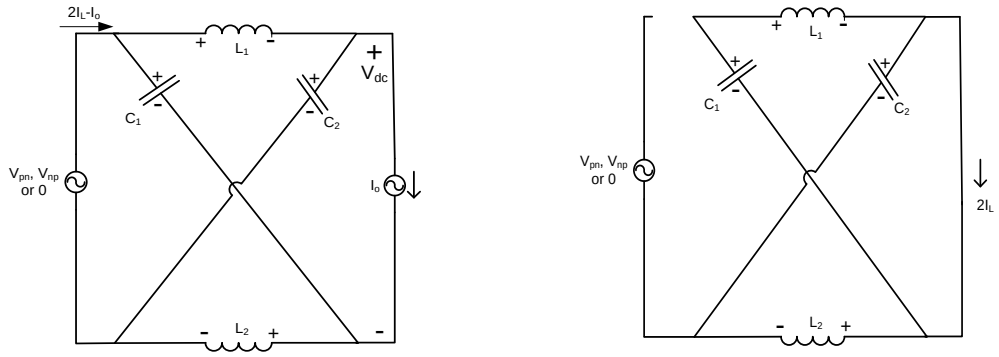

Fig. 5.7 Equivalent-circuits of the Z-source: left to right: non-shoot-through states, shoot-through states.

5.4.2 Switched Inductor Z-source Circuit

Fig. 5.8, analogous to Fig. 5.7, shows equivalent circuits of the switched-inductor Z-source under the non-shoot-through and shoot-through conditions. The rectifier stage output voltages are V_{an}, V_{bn}, V_{cn}, or zero, depending on the position of the input current vector. Fig. 5.8(a) illustrates a situation when diodes D_2 and D_5 are on and the other ones are off. Inductors L_1 and L_2 are in series, as are inductors L_3 and L_4. Capacitors C_1 and C_2 are simultaneously charged by the rectified input voltages. In Fig. 5.8(b), the inverter is operating under the shoot-through condition to boost the output voltage. Now, diodes D_1, D_3, D_4, and D_6 are on while D_2 and D_5 are off. The parallel inductors L_1 and L_2 are charged by C_1 and L_3 and L_4 by C_2. The following relations apply to the switched-inductor Z-source: capacitor voltage, $V_c = (1-D)V_{pn}/(1-3D)$, the capacitor currents, $I_c = (1-D)V_{dc}/R_L$, boost factor, $B = (1+D)/(1-3D)$, and the inductor currents, $I_L = (1-D)^2 V_{dc}/(1-2D)R_L$.

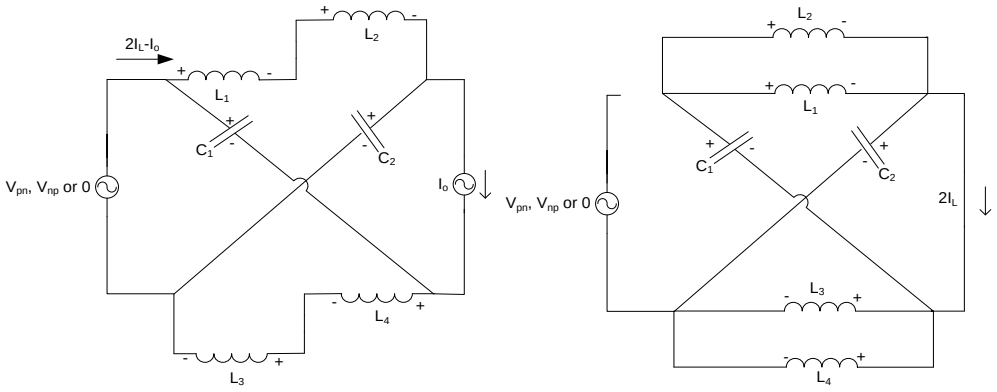

Fig. 5.8 Equivalent circuits of the switched-inductor Z-source, left to right: non-shoot-through states, shoot-through states.

5.5 Simulation Results

Computer simulations of the super-sparse, Z-source, and switched-inductor Z-source matrix converters were performed to verify the presented analysis. Using of the PSIM software from Powersim Inc. was employed. A dynamic link library, DLL, block was created in the PSIM environment, and written in the C programming language to define the switching signals of the IGBTs assumed as the power switches. Input filters were placed at the input of the converters to reduce the ripple of the input currents. The system parameters are listed in Table 5.1. Waveforms of the output voltages, output currents, and the filtered and unfiltered input current in phase "a" are shown in Figs. 5.9 to 5.11 for each of the three converters.

As seen from the waveforms, the quality of the output current is directly related to the line inductance and switching frequency. In the simulations, the switching frequency was 10 kHz and line inductance was 10 mH. To obtain lower ripple at the output, higher switching frequencies can be used. However, using higher switching frequencies causes larger switching loss. Wide bandgap semiconductors provide higher switching frequencies with less switching losses, and can be an option to increase the quality of the output currents.

Input AC Source	30 V / 60Hz
Load, R/L	10 mH / 64 Ω
Input Filter, L/C	4.6 mH / 18 μF
Switching Frequency	10 kHz

Input AC Source	30 V / 60Hz
Load, R/L	10 mH / 64 Ω
Input Filter, L/C	4.6 mH / 18 μF
Z-source, L/C	1mH / 1000uF
Switching Frequency	10 kHz

Input AC Source	30 V / 60Hz
Load, R/L	10 mH / 64 Ω
Input Filter, L/C	4.6 mH / 18 μF
Z-source, L/C	1 mH / 1000μF
Switching Frequency	10 kHz

Table 5.1 System parameters. Top to bottom: super-sparse, Z-source, and switched-inductor Z-source matrix converters.

All converters were fed from a 30-V three-phase source and supplied same RL loads. Fig. 5.9 applies to the super-sparse matrix converter. The modulation index was set to 0.7. The dc-link voltage was modulated between two line-to-line voltages in order to produce a positive voltage. It can be seen that the input voltage and current of phase “a” are in phase, resulting in a unity power factor. The Z-source matrix converter illustrated in Fig. 5.10 boosts the voltage and current about 4 times with the modulation index of 0.5 and the boost factor of 2. As seen in Fig. 5.11, the voltage in the switched inductor Z-source matrix converter is stepped up about 6 times with the same shoot-through times and modulation index, and a unity input power factor is maintained. Performance of the converters fully matches the theoretical analysis.

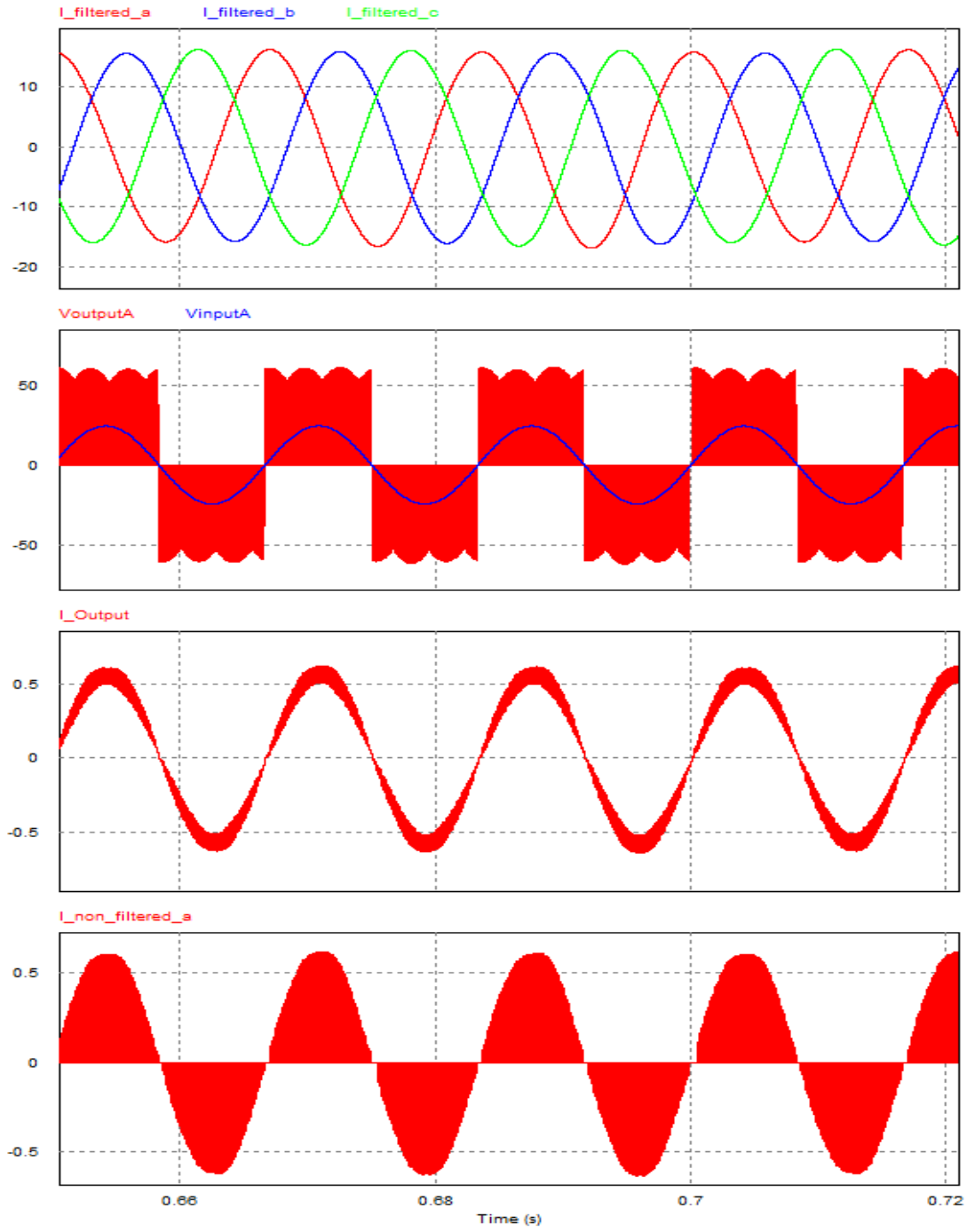

Fig. 5.9 Super-sparse matrix converter. Top to bottom: filtered input phase currents, output and input voltages, output current, unfiltered input currents.

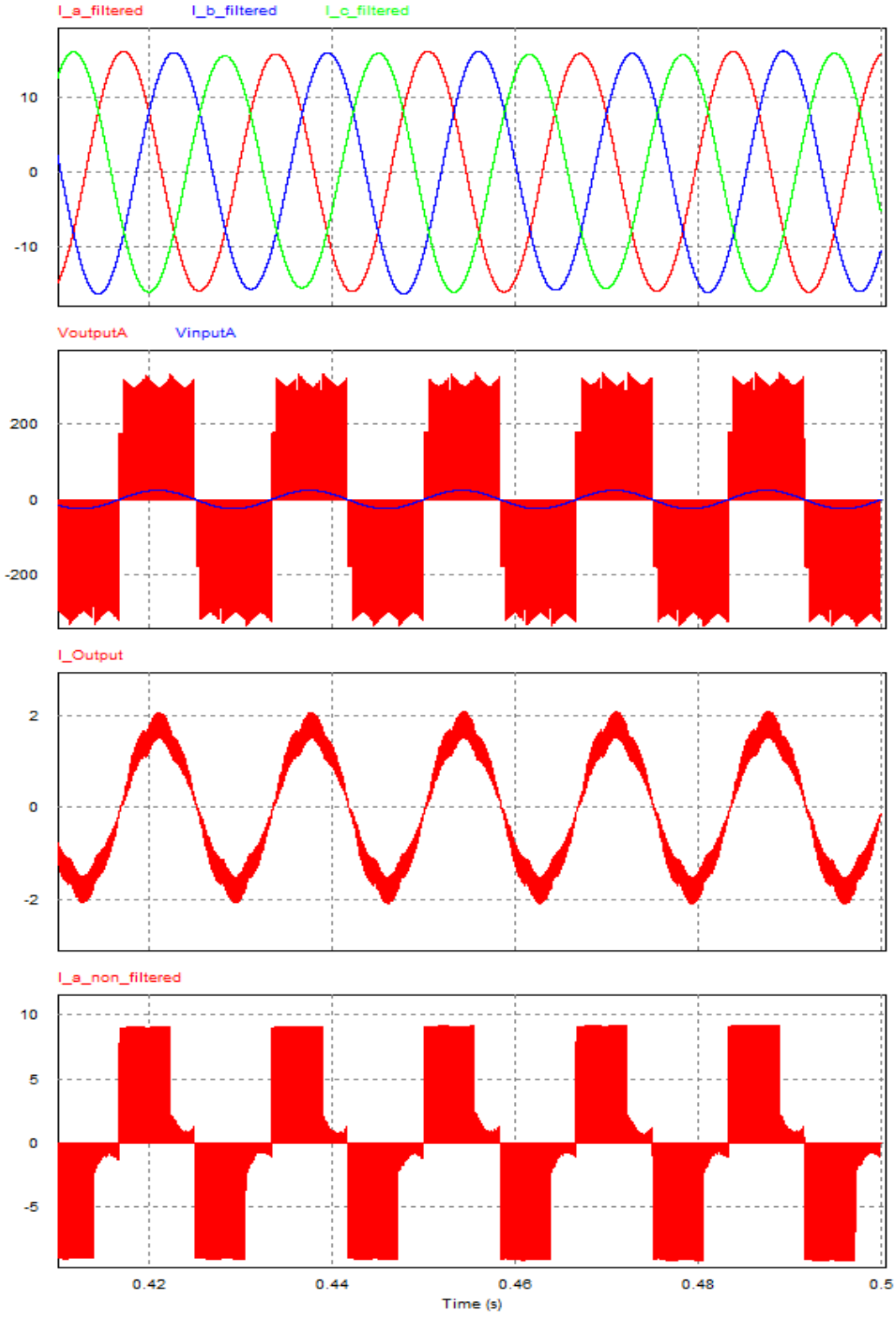

Fig. 5.10 Z-source matrix converter. Top to bottom: filtered input phase currents, output and input voltages, output current, unfiltered input currents.

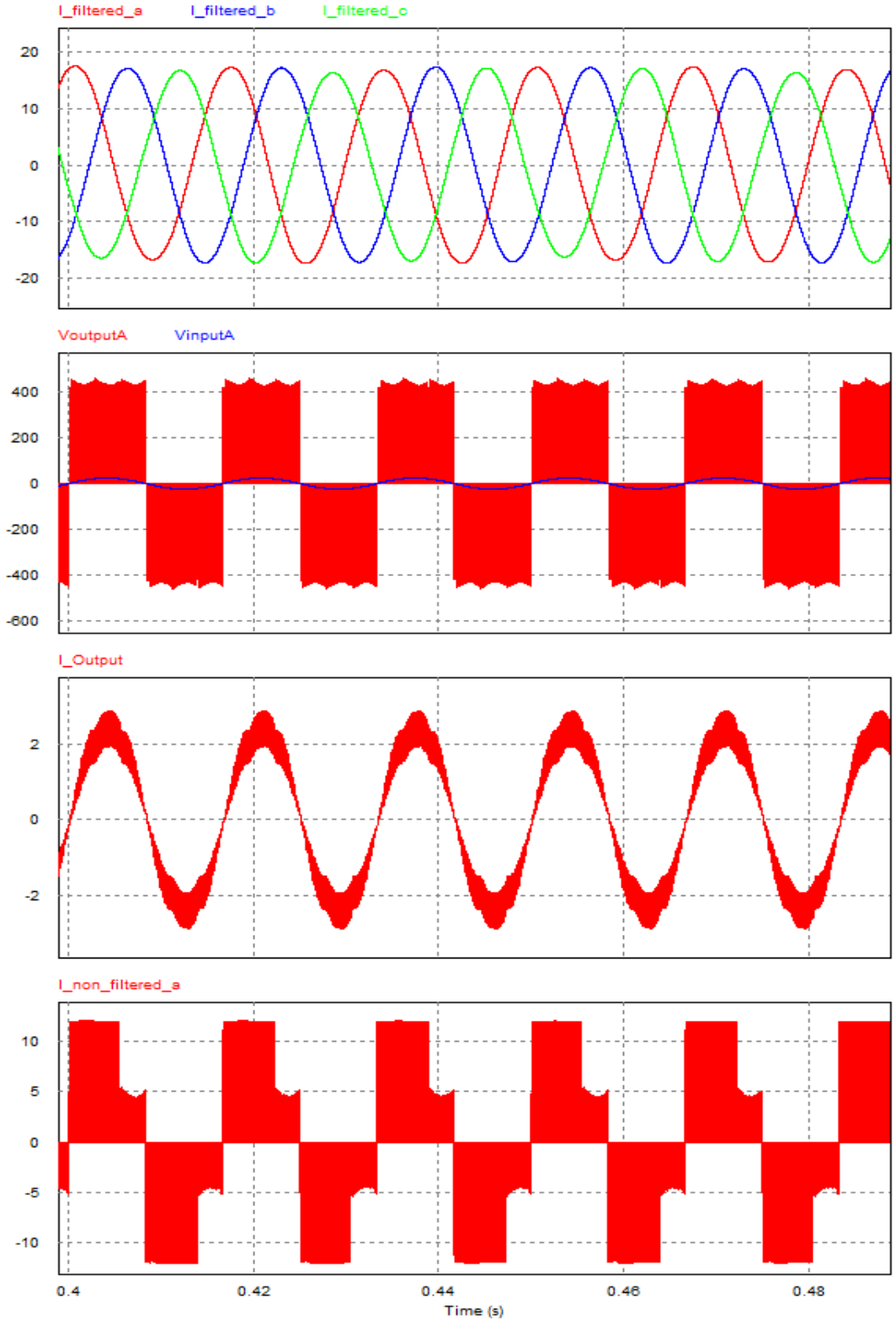

Fig. 5.11 Switched inductor Z-source matrix converter. Top to bottom: filtered input phase currents, output and input voltages, output current, unfiltered input currents.

5.6 Conclusion

The Z-source and switched-inductor Z-source circuits have been combined with the super-sparse matrix converter topology to create novel three-phase to single-phase matrix converters with voltage boosting capability and a unity power factor. The converters are suitable for all applications with unidirectional power flow. The three-phase to single-phase super-sparse matrix converter was obtained by removing one leg from the corresponding three-phase to three-phase converter. Except for the voltage boosting, the buck-type super-sparse matrix converter is suitable for similar applications as those of the other two converters. Computer simulations have verified the operating features of the developed converters.

Chapter 6

Implementation of Boost Matrix Converters

6.1 Introduction

After evaluating the performance of boost matrix converters, it is essential to experimentally validate the results using a prototype converter at realistic power levels. This chapter presents the hardware implementation as well as the firmware from the boost matrix converter topologies. To begin with, the overall structures of the converter prototypes are described. Then, the design of each circuit is explained in detail. Finally, the firmware along with the circuit is analyzed.

6.2 Hardware Implementation

6.2.1 Structure of the Prototype Converters

To validate the results, prototypes of the boost matrix were built. As shown in Fig. 6.1, the overall structure of the prototypes consists of five parts: the control platform, the measurement circuits, the gate drives, the power circuits, and the filters. The control platform in comprise of a digital signal processor (DSP) board. The DSP is the central processing unit for:

- all modulation calculations and control functions
- collecting data from the measurement circuits and performing analogue to digital (A/D) conversion
- providing the switching signals to the gate drives, according to the modulation demands

- protecting the power circuit by turning off all switching devices when the protection circuit signals an over-voltage, over-current, or high temperature conditions.

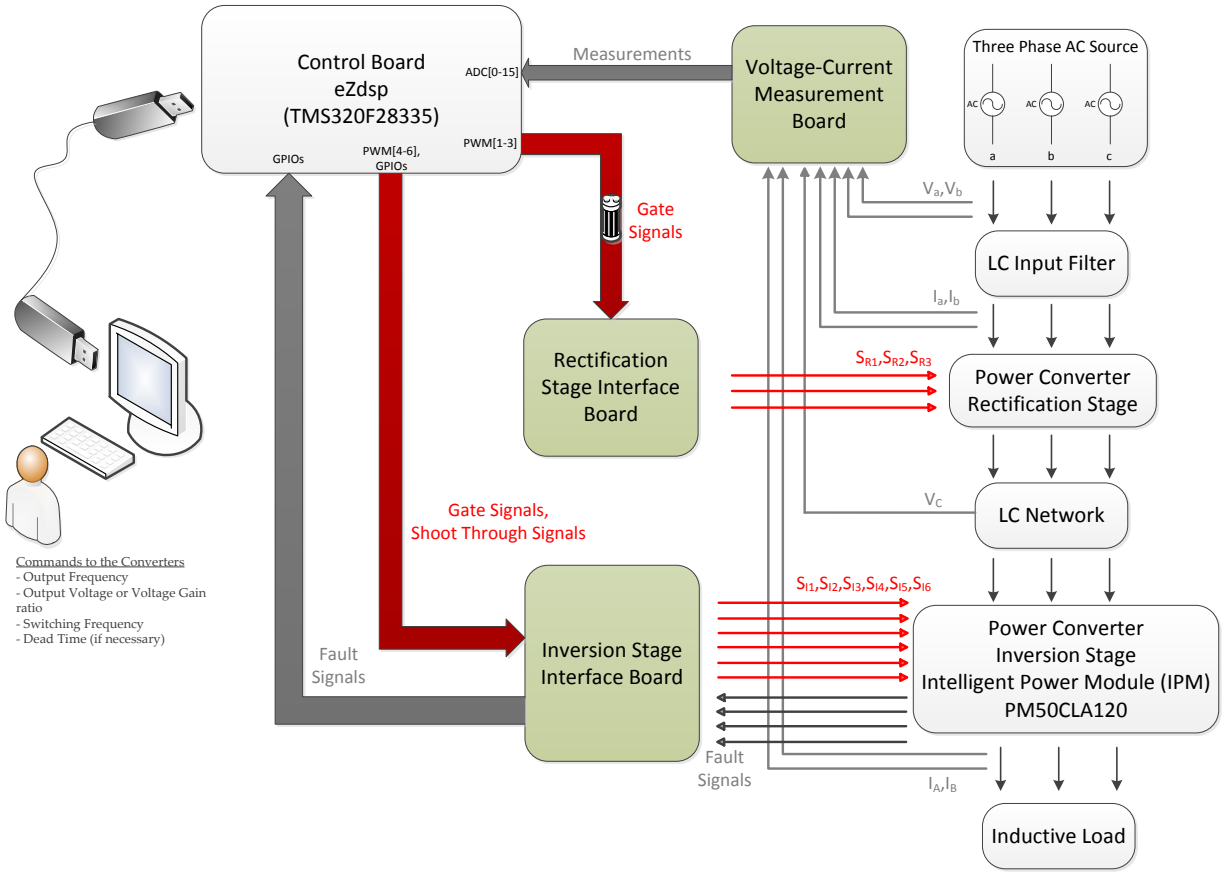

Fig. 6.1 Structure of the implemented boost matrix converter.

The measurement circuits provide the input data that is required by the control board to perform the modulation. The magnitudes of the line phase voltages are needed to discern a possible phase loss, as well as matching the input voltage angles and input current angles to obtain a unity power factor. The magnitudes of the input phase currents are needed in the modulation strategy to determine the duty cycles for the switching devices, and are measured using current transducers.

To commutate the current between switches in the rectification stage, the input current space vector is applied. LC network voltage transducer is designed to monitor to overvoltage in the dc-link. Based on the measured input voltages and currents, the control board performs

necessary calculations and then sends out the switching signals to the gate drives. The gate drives provide electrical isolation between the control platform and the power circuit. Using the gate drives, the control board can drive the high voltage switching devices using low voltage control signals. The prototype power circuits have been built for the boost matrix converter topologies discussed in Chapters 5. The input filters and load are connected to the input and output terminals of the power circuit, respectively. The protection circuit provides overvoltage protection to the power circuit. To ensure that the power circuit does not operate over the maximum current level, the control board monitors the load currents by using current transducers, providing additional protection for the prototype.

6.2.2 Voltage – Current Measurement Board

As shown in Fig. 6.1, the measurement circuits comprise voltage transducers, current transducers, and level shifters. According to the modulation strategy, the input currents generated by the boost matrix converter topologies are synchronized with the input voltages. As a result, the magnitude of the line voltages are required to determine the reference angle of the input current vector as well as the duty cycles for the switching devices. To measure the input phase voltages, LEM LV20-P transducers , were used.

The schematic diagram of the voltage measurement circuit for this prototype is shown in Fig. 6.2. The nominal primary voltage of the voltage transducer is set to 100 V_{rms}. A resistor, R_p, is used for measurement of the primary current of the transducer. In order to achieve a 10 A_{rms} primary nominal current for the voltage transducer, a 10 kΩ resistance was selected. Based on the primary current, the voltage transducer uses the Hall effect to generate a secondary current, I_s, with the conversion ratio of 2500:1000. A measurement resistor, R_m, is then employed to generate an isolated output voltage signal, proportional to I_s.

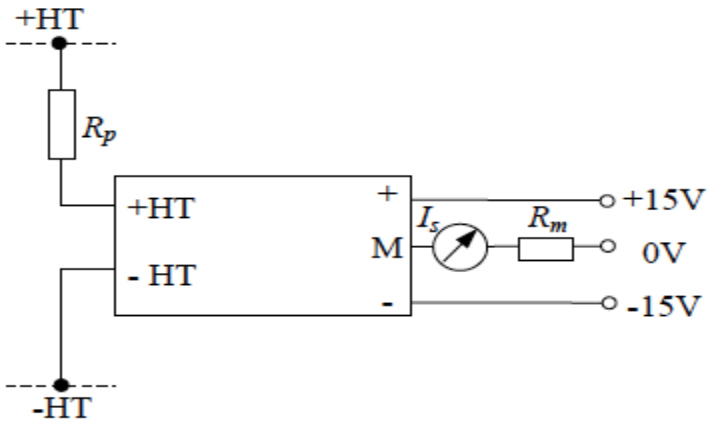

Fig. 6.2 Schematic diagram of a voltage transducer.

Knowing that the secondary nominal current is 25 mA_{rms} at the rated voltage, a 300 Ω was selected for the best resolution and an output of 7.5 V_{rms}. Each A/D conversion channel expects an input signal within the range of 0-3 V. Because the TMS320F28335 DSP controller from Texas Instruments handles only positive cycle of the ac voltages, firstly 10.6 V_{pk} (7.5 V_{rms}) is stepped down to -1.5 V_{pk} to 1.5 V_{pk} voltage level and then a voltage offset of 1.5 V is summed to result in 0-3V_{pk} range with the cascaded summing amplifier and non-inverting amplifier as shown in Fig.6.3 and Fig.6.4.

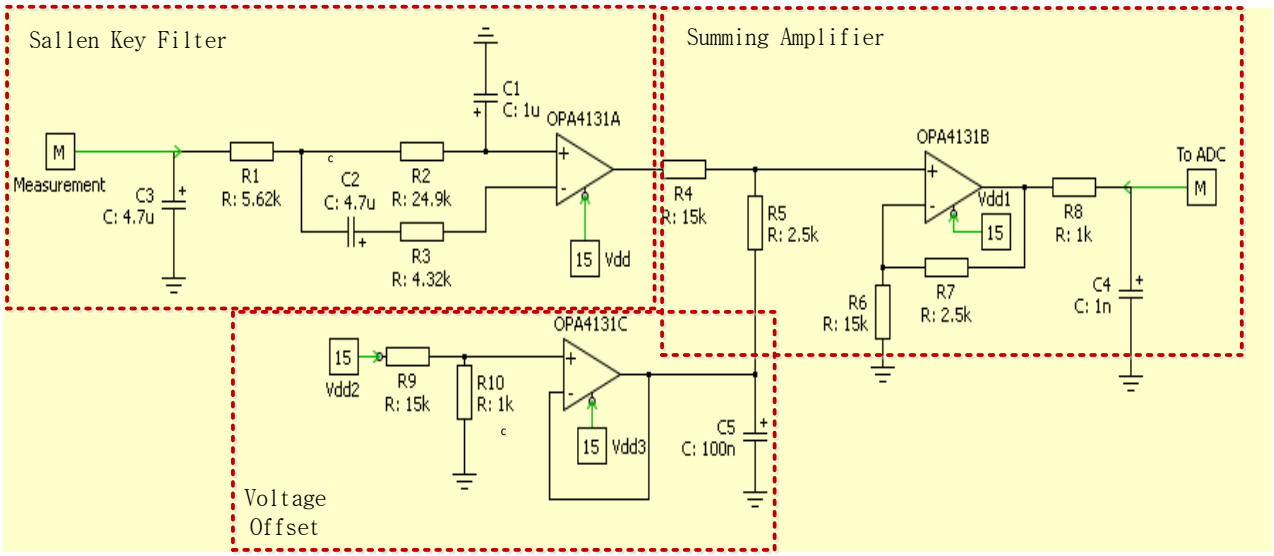

Fig. 6.3 Schematic diagram of an interface to the ac voltage transducers.

A Sallen-Key filter is employed at the front end of the measurements as a voltage follower to prevent high voltage spikes through the transducers. Fig. 6.4 shows a photograph of the voltage and current measurement board that was built for this prototype.

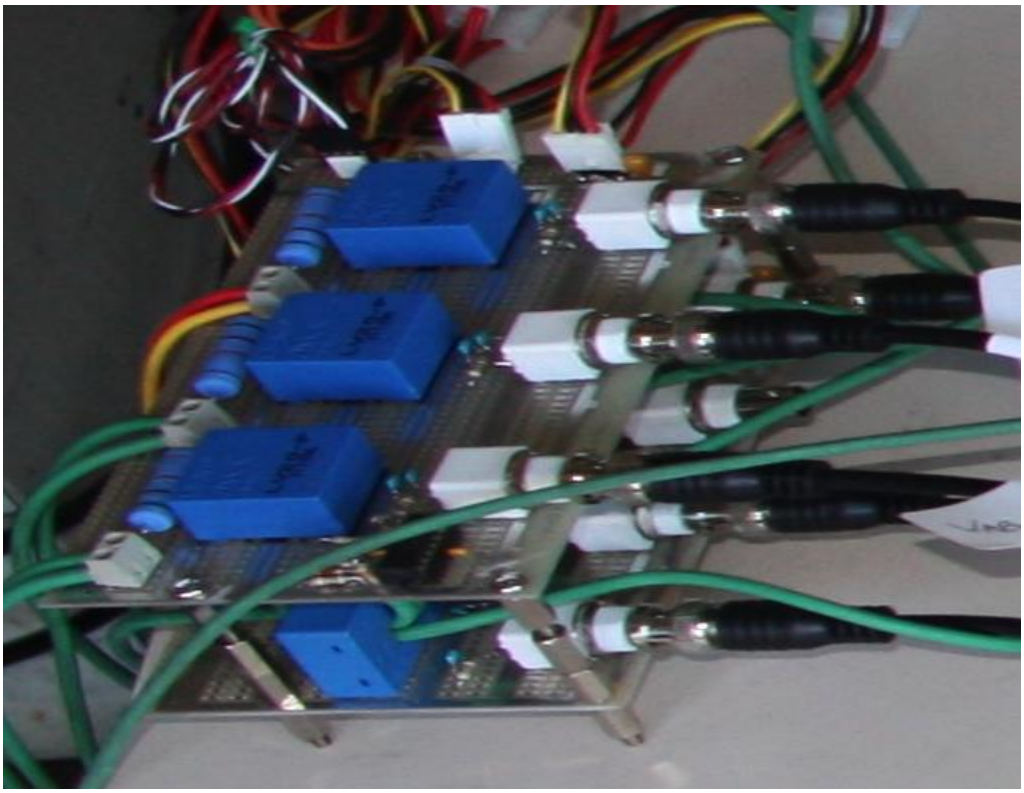

Fig. 6.4 The voltage and current measurement board

To ensure that the rectifier stage converter does not operate over the maximum voltage level, the control board continuously monitors one of the LC network capacitor voltages using the same voltage transducers used to measure ac voltages. LEM LV20-P can be operated both in the ac and dc modes, the latter shown in Fig 6.5. A voltage divider is used to obtain 0-3 V input range to the A/D channels. Sallen-Key topology filter includes the voltage divider.

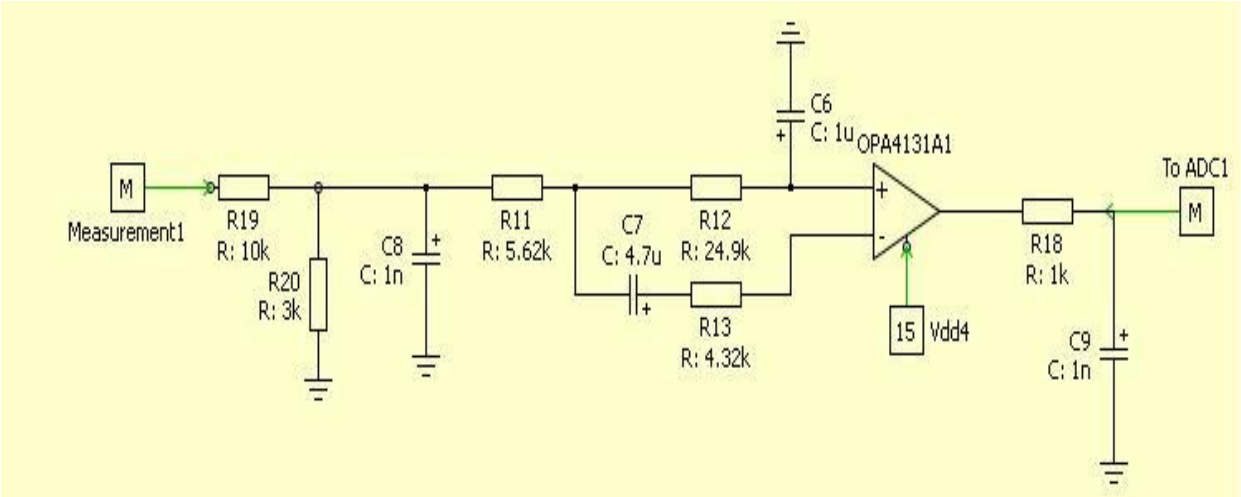

Fig. 6.5 Schematic diagram of interface to the dc voltage transducers.

To ensure that the prototype converter does not exceed the maximum current levels, the control board monitors both the input currents and load currents using four current transducers, LEM LAH-25NPs. The connection of the current transducer for this prototype is shown in Fig. 6.6.

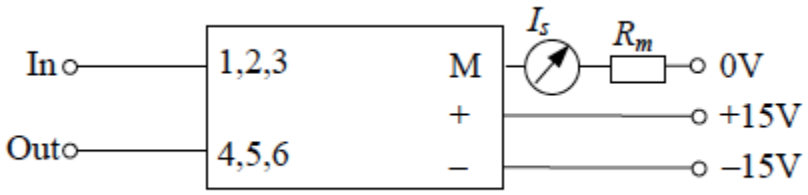

Fig. 6.6 Schematic diagram of a current transducer.

The current transducer uses the Hall effect to generate a secondary current, I_s, with the conversion ratio 1:1000 to the primary current. Knowing that the secondary nominal current for the current transducer is 25 mA_{rms}, a 200 Ω resistor is used to generate a voltage signal, which is within the range of +3 V, for the A/D conversion channel on the DSP. An operational amplifier bases circuit including a low-pass filter, Sallen-Key filter, and voltage offset is shown in Fig. 6.7 for the current transducers interface.

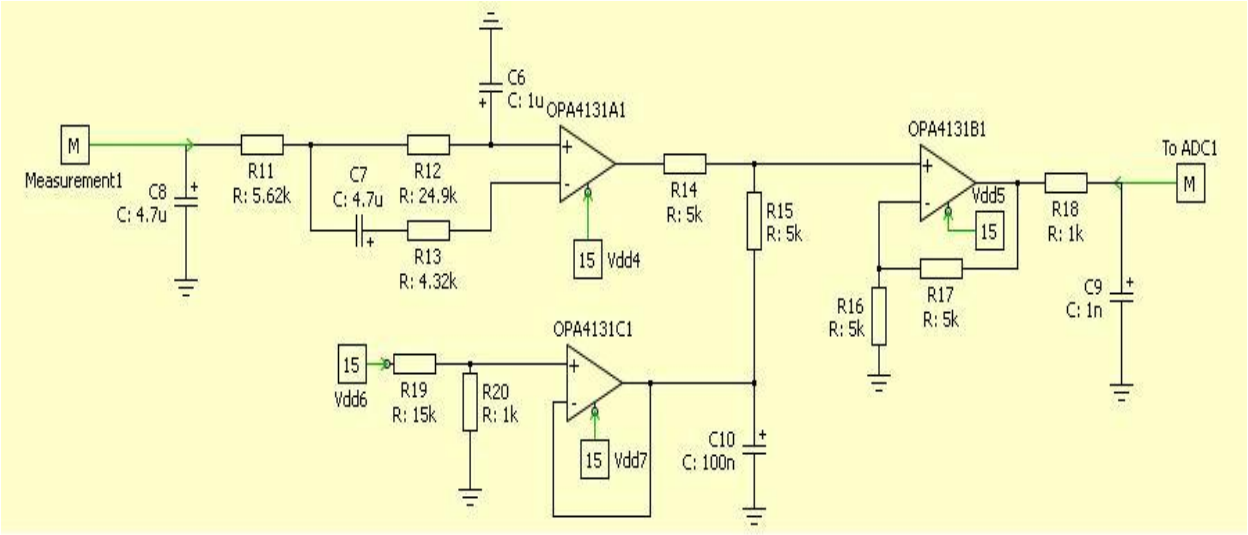

Fig. 6.7 Schematic diagram of an interface to the ac current transducers.

6.2.3 Control Board – eZDSP controller (TMS320F28335)

The F28335 eZDSP controller starter kit is a complete software development platform for the TMS320F2833x series of floating-point DSP controllers. The eZDSP controller kit includes an F28335 target board that features integrated JTAG emulation, 128Kx16 asynchronous SRAM, CAN 2.0 and RS-232 interfaces, and expansion headers that provide access to all F28335 I/O signals. Also included in the kit is the Code Composer Studio™ Integrated Development Environment, USB interface to the host PC, and a universal power supply.

All the corresponding modulation calculations are done in the DSP controller, which also transfers gate signals from the PWM blocks and receives fault signals from the general purpose input-output pins (GPIO).

The main hardware features are:

- TMS320F28335 Floating-Point Digital Signal Controller
- 150 MHz operation
- 512 KB on-chip flash memory
- 68 KB on-chip RAM

- 12-bit ADC with 16 input channels
- 128k x 16 off-chip SRAM
- Clamshell socket for the F28335 DSC
- RS-232 interface with on-board transceiver and 9-pin DSUB connector
- CAN interface with on-board transceiver and 9-pin DSUB connector
- Multiple expansion connectors provide access to all F28335 I/O signals
- Embedded USB JTAG Controller
- Operates from a single 5V supply with provided AC adapter

6.2.4 Inversion Stage Power Converter – Powerex Intelligent Power Module (IPM)

The Powerex Intelligent Power Modules are advanced hybrid power devices that combine high speed, low loss IGBTs with optimized gate drive and protection circuitry. Highly effective short-circuit protection is realized through the use of advanced current sense IGBT chips that allow continuous monitoring of power device current. System reliability is further enhanced by the IPM's integrated over-temperature and under-voltage lock out protection. Intelligent Power Modules (IPM) are designed to reduce system size, cost, and time to market.

PM50CLA120 IPM is used for the implementation and is rated up to 50 A phase currents and 1200 V line voltages. Such IPMs are constructed using ceramic isolation material. A direct bond copper process in which copper patterns are bonded directly to the ceramic substrate without the use of solder is used in these modules. This substrate provides the improved thermal characteristics and greater current carrying capabilities that are needed in these higher power devices. Gate drive and control circuits are contained on a separate printed circuit board (PCB) mounted directly above the power devices. The PCB has a multilayer construction with special shield layers for EMI noise immunity. The IGBT power switches in the Powerex IPM modules

are controlled by a low level input signal. The active low control input will keep the power devices off when it is held high. Typically the input pin of the IPM is pulled high with a resistor connected to the positive side of the control power supply [80]. An on signal is then generated by pulling the control input low. For the interface to the gate signals an inverting buffer SN74LS241 is used, so that all the control signals are inverted.

The fault output is an open collector with its maximum sink current internally limited. When a fault condition occurs the open collector device turns on allowing the fault output to sink current from the positive side of the control supply. Fault and on/off control signals are usually transferred to and from the system controller using isolating interface circuits. Isolating interfaces allow high and low side control signals to be referenced to a common logic level. The isolation is provided by opto-couplers.

6.2.5 Inversion Stage Interface Circuit

The gate signals generated in the DSP controller are transferred to the interface board through ribbon cables and interfaced with a line driver to accommodate the voltage level up to 5 V from 3.3 V. The interface circuit consists of opto-couplers to transfer control signals and isolated power supplies to power the IPM's internal circuits.

The inversion stage needs four separate isolated power supplies for the gate signals, because the top three power switches are floating and require three separate isolated power supplies. The bottom switches have a common emitter and need only one power supply. For that purpose Powerex's VLA106-24151 and VLA106-24154 isolated DC-DC converters are used. Both DC to DC converters are designed to operate from a 24 V DC supply and produce an isolated 15 V DC output. The VLA106-24151 provides up to 100 mA and the VLA106-24154 provides up to 300 mA for control power. Both DC to DC converters use transformers to ensure

2500 Vrms isolation between the primary and secondary side. The interface board uses three VLA106-24151 DC to DC converters to provide power supply for the upper switches. For the low side control power can be supplied by a VLA106-24151. The IPM interface is shown in Fig. 6.8.

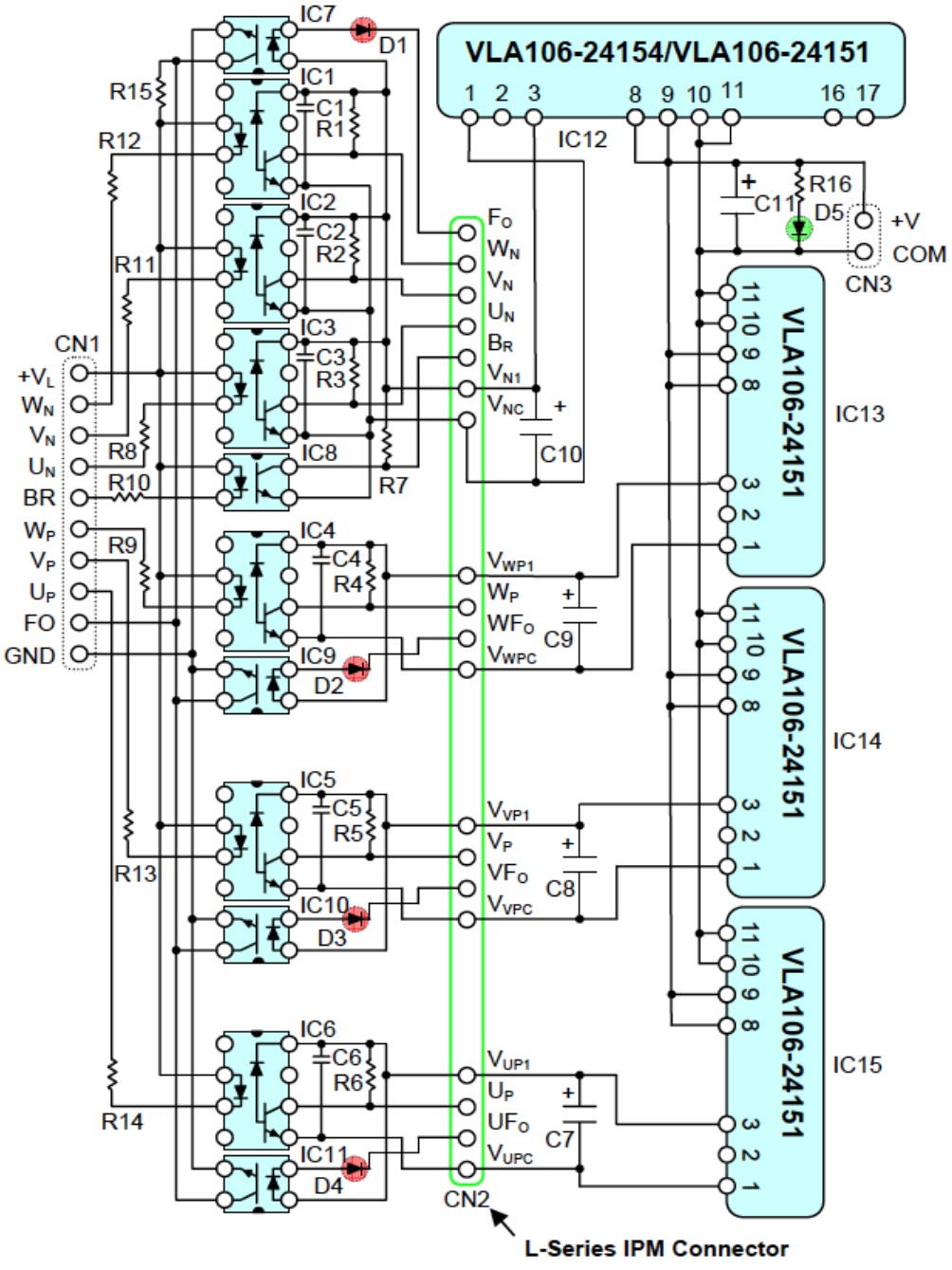

Fig. 6.8 Schematic diagram of the IPM interface circuit [81].

This circuit uses two types of opto-coupled transistors to transfer logic level control signals between the system controller and the IPM. The opto-couplers ensure galvanic isolation to completely separate the controller from the high voltage in the power circuit. The IPM also provides isolated control power supplies to power the IPMs built-in gate drive and protection circuits.

There are two types of PWM signals applied within the switching cycle. The first type of signals are formed without the shoot-through state. The second type of signals is the shoot-through states. These two sets of signals are combined with an OR gate to form the calculated gate signals.

The six main IGBT control signals (UP ,VP ,WP ,UN ,VN ,WN) that are now included with the shoot-through signals are transferred from the DSP controller to the IPM using high speed opto-coupled transistors, IC1-IC6. To maintain noise immunity, high speed opto-couplers generally require a film or ceramic decoupling capacitor connected near their VCC and GND pins (C1-C6) [81]. The IPM's active low control inputs are pulled high (off state) by resistors R1-R6. An "on" signal is generated by turning on the opto-coupler to pull the IPM's control input pin low. The resistance of the control input pull up resistors is selected low enough to avoid noise pick up by the IPM's high impedance input and high enough so that the high speed opto-transistor pulls the IPM's input low enough to assure turn on. The high speed opto-couplers have very high common mode transient noise immunity. Agilent HCPL4504 opto-coupler which has a minimum common mode transient noise immunity of 15,000V/μs are used for the prototype.

The IPM's fault output signals are transferred back to the control board using low speed opto-coupled transistors IC7, IC9, IC10, and IC11. During normal operation the fault feedback line (pin 2 of CN1) is pulled high to the +VL supply by the 4.7 k Ω resistor R15. When a fault condition is detected by the IPM it will immediately turn off the involved IGBT and pull its fault

output pin low. The IPM's fault output has an open collector characteristic with an internal 1.5 k Ω limiting resistor. Current flows from the +15V local isolated supply through the low speed opto-coupler's LED to the IPM's fault pin. The opto-coupler's transistor turns on and its collector pulls the fault feedback line low to indicate a fault. If any of the IPM's four fault output signals become active its fault isolation opto-coupler will pull the fault feedback line low [80]. Fig. 6.9 shows the implementation of the inversion stage interface

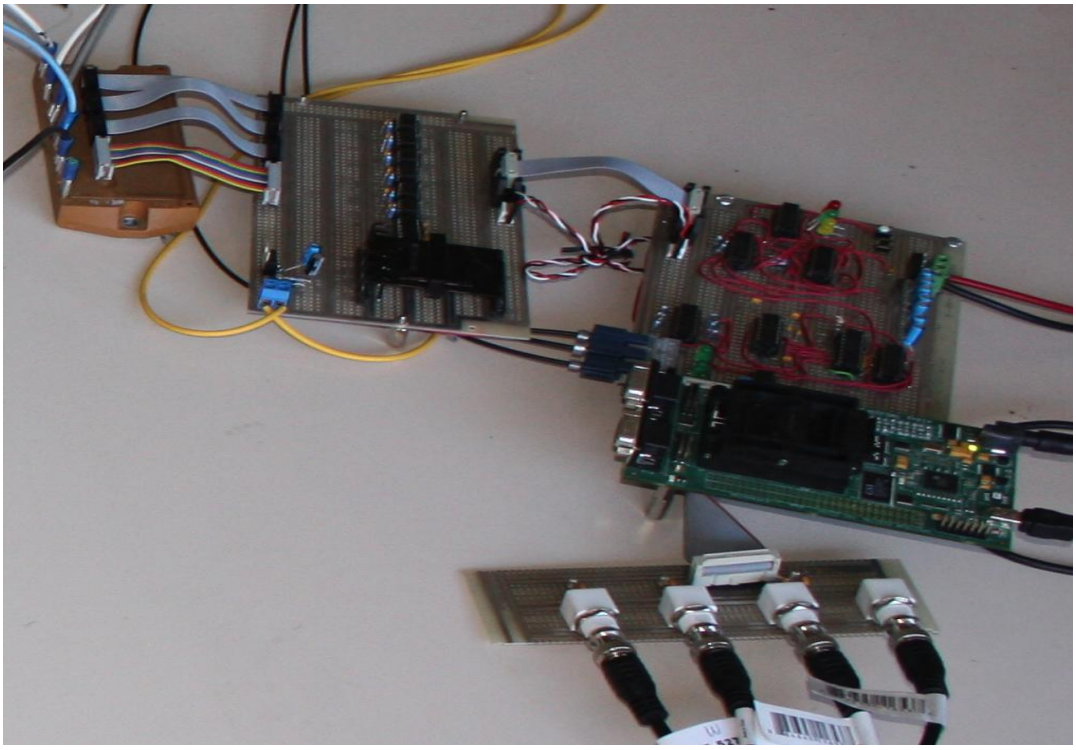

Fig. 6.9 Inversion stage interface.

The interface board includes an LED in series with each fault output (D1-D4) to provide a quick visual indication when the IPM's fault signal is active. Also; a flip flop with on board buttons are included to control the gate signals flowing through the IPM at the time of the fault. Buttons are controlling the start/stop of the gate signals. The circuit automatically trips itself, turns the LEDs on and shuts down the gate signals in any of the four faults. After clearing the

fault conditions, pushing the reset button resumes the whole operation come back to normal. Isolated control power for the IPM is supplied by Powerex isolated DC to DC converters (IC12, IC13, IC14, IC15) described above. Each power supply is decoupled at the IPM's pins with a low impedance electrolytic capacitor (C7-C10) for decoupling.

6.2.6 Rectification Stage Interface Circuit

To construct a boost matrix converter as the rectification stage three IGBT modules (60 A/1200 V), manufactured by SEMIKRON, are used. The IGBT modules were soldered on a custom-designed board where the input and output terminals are placed on either side of the board. The top layer is the signal plane that consists of the gate drive circuits, the gate signal tracks and the DC voltage supply tracks. Each gate drive circuit is built close to its respective IGBT module to ensure smooth commutation process and reduce any parasitic effects. The input filter capacitors are connected close to the input terminals on the board in order to reduce the stray inductance in the device conductive loops. Twelve fast recovery diodes 8EWF12S were used in the board and were placed in parallel with each IGBT leg. Each diode had a rating of 1200 V and 40 A.

The rectifier module was placed in a black box to minimize the EMI noise. The IGBT drivers were supplied from 3 separate DC to DC voltage sources. The gate signals were further from the DSP controller that's why fiber optical cables are used to reduce the cable noises. The implementation of the rectification circuit is shown in Fig. 6.10. The prototypes were tested at realistic power levels in the laboratory to prove the abilities of the boost matrix converters to generate the required output voltages and frequencies as well as maintain a set of sinusoidal and balanced input currents. By removing the LC network and disabling the shoot-through the gating signals the prototype can be operated as an indirect matrix converter.

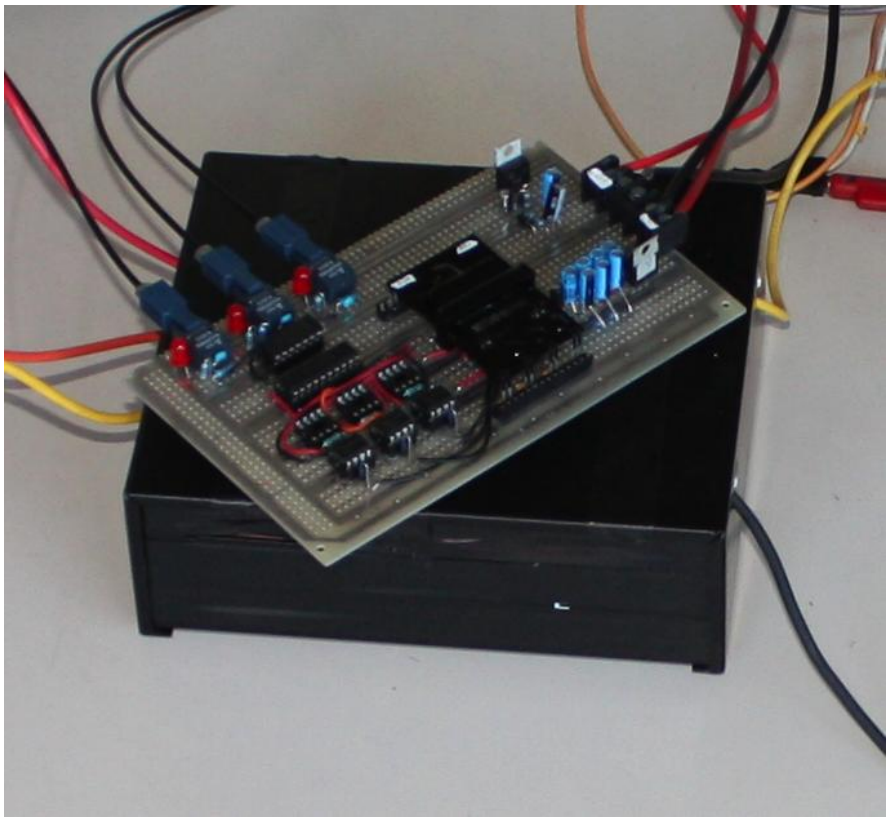

Fig. 6.10 Rectification stage interface and converter.

6.3 Software Implementation

The TMS320F28335 is designed for industrial applications and has several peripheral circuits. The 16-channel, 12-bit ADC module and the PWM modules are the main controllers to generate the gate signals with the proposed modulation techniques. Ninety-six combined software and hardware interrupts are supported by F28335. These interrupts are governed by the peripheral interrupt expansion (PIE) block, which has control on enabling or disabling the interrupts. The FTDI FH2232H based JTAG interface supports the real-time debugging. JTAG provides the user to monitor and modify the contents of the RAM memory and the registers without halting the processor.

6.3.1 ADC Module

The ADC module has 16 analog input channels. A channel to be sampled can be selected by sending its corresponding 4-bit address to the MUX. There are two sequencer blocks, Sequencer1 and Sequencer2, where the addresses of the channels to be sampled are placed in an appropriate order. For each sequencer of most eight channels are selected. To obtain sixteen channels in the software code Sequencer1 and Sequencer2 are merged into a cascaded sequencer. To start an ADC sequence, a start-of-conversion (SOC) signal is needed. Cascaded sequencer, the SOC signals were aligned with the PWM module or to get simultaneous sampling while applying the right PWM signals [82].

To get noise-free measurements, the high ADC clock frequency is set to 12.5 MHz. While the DSP controller allows higher clock frequencies, nonlinearity prevent from increasing such frequency limits. Seven measurements are sensed with the transducers. Within those seven measurements, four are crucial for the space vector modulations (input line voltages and input phase currents) and three are protection and future work based measurements.

The phase angle of the input voltage is a critical piece of information for the input rectifier space vector modulation. A phase-locked loop (PLL) is a closed loop system, in which an internal oscillator is controlled to keep the time and phase of an external periodical signal using a feedback loop. The PLL is simply a servo system that controls the phase of its output signal such that the phase error between the output phase and the reference phase is minimized. The quality of the lock directly affects the performance of the control loop in grid tied applications. As line notching, voltage unbalance, line dips, phase loss and frequency variations are common conditions faced by equipment interfacing with electric utility, the PLL needs to be able to reject these sources of error and maintain a clean phase lock to the grid voltage. To this purposes input voltages are converted to synchronous domain with the clark transformation

followed by the Park transformation to get rotating frame. The PLL applied to the “q” axis voltage and in return the required grid angle for the space vector modulation is received.

6.3.2 PWM Module

The TMS320F28335 has six independent enhanced PWM (ePWM) modules included. Each of the ePWM modules has two output channels: ePWMxA and ePWMxB belongs to the particular module. submodule in each ePWM module. The time-base submodule takes charge of the event timing for its own ePWM module.

One of the main tasks for the time-base sub module is to determine the PWM time-base clock relative to the system clock. The PWM time-base clock is used to regulate the timing of all the events in the PWM module. The period of the time-base clock (T_{TBCLK}) for the PWM module can be scaled to several times of the system clock period $T_{SYSCLKOUT}$ as:

$$T_{TBCLK} = T_{SYSCLKOUT} * CLKDIV * HSPCLKDIV \tag{6.1}$$

where CLKDIV and HSPCLKDIV are bits in the time-base control register (TBCTL) serving for the time base clock pre-scale. The time-base sub-module can also be used to specify the period of the time-base counter (TBCTR) depending on its different operation modes. There are three types of operation modes for the time-base submodule, which can be selected in time-base control register (TBCTL); namely up-count mode, down count mode and up-down-count mode. During a complete PWM period, for the first two modes, the time-base counter (TBCTR) increment or decrement in a given a saw tooth carrier wave. For up-down mode the, the TBCTR increments in the first half the PWM period and then turns to decrement in the second part of the period giving a triangular carrier wave. This mode allows to have two up and downs that are necessary for the proposed modulation techniques. For this mode switching period (TMPRD) can be established as the following equation:

$$TBPRD = \frac{T_{PWM}}{2*T_{SYSCLKOUT}*CLKDIV*HSPCLKDIV} \quad (6.2)$$

where T_{PWM} is the PWM period. For the software codes switching frequency is set to 10kHz and TBPRD is found to be 1250 while HSPCLK is set to 25 MHz.

Action qualifier output control registers AQCTLA and AQCTLB are programmed to obtain the low or high attitudes of the each counter compare (CMPA and CMPB) registers. In Fig. 6.9 the mode is set to up-down mode. The opposite mode, down-up mode, is also possible. In this example TBPRD is set to 4 and in case 1 CMPA is set to 4 which indicates no PWM. This ratio can be increased by lowering the CMPA value. The CMPA value of 0 gives a full PWM signal. The same way CMPB values of the same register results the PWMB output displays the same or opposite behavior.

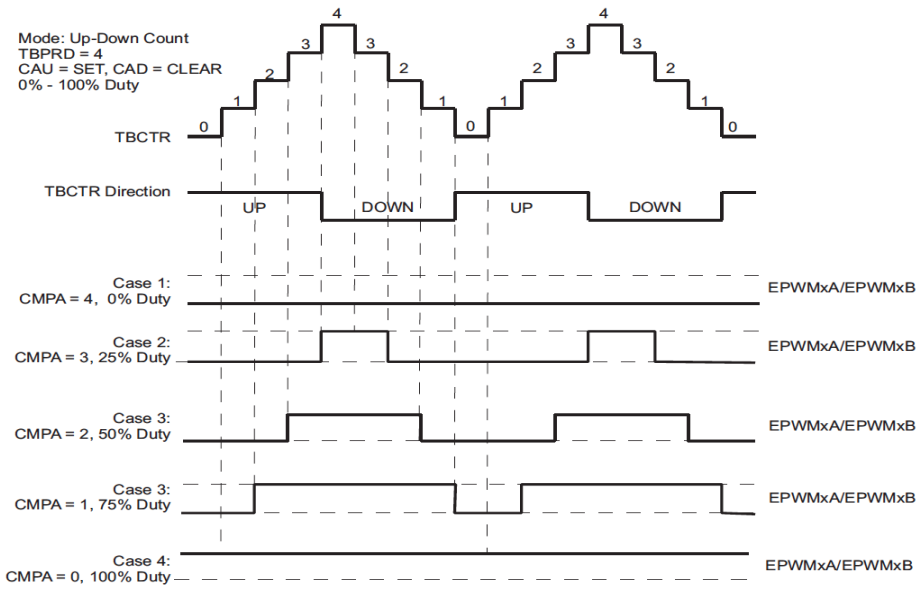

Fig. 6.11 An example up-down mode (courtesy of Texas Instruments [83]).

In the firmware switching tables are created to generate the rectification and inversion stage space vectors. It can be seen that the up-down mode is sufficient to generate such PWM

signals without any additional hardware realization. The four types of AQCTLA signals were coded, Table 6.1 represents these four types and their behavior.

Register	Hex	Mode	PWM Behaviour
AQCTLA	0x0060	up-down	___-------___
AQCTLA	0x0090	down-up	----_____----
AQCTLA	0x0690	down-up-down-up	--__------__--
AQCTLA	0x0960	up-down-up-down	__--_____--__

Table 6.1 AQCTLA register coding.

Depending on the rotating input current angle, the gate signals for the rectifier stage AQCTLA registers are formed referring to Table 6.2. This register only defines the mode and particular duty ratios have to be calculated to decide the up or down points. Table 6.3 shows how inversion stage PWM registers need to be formed to perform the required proposed combined space vector modulation.

Sector #	pwm04.AQCTLA	pwm05.AQCTLA	pwm06.AQCTLA
0	0x0060	0x0090	0x0060
1	0x0090	0x0060	0x0060
2	0x0060	0x0060	0x0090
3	0x0060	0x0090	0x0060
4	0x0090	0x0060	0x0060
5	0x0060	0x0060	0x0090

Table 6.2 AQCTLA register coding for the rectification space vector.

Sector #	pwm01. AQCTLA	pwm01. AQCTLB	pwm02. AQCTLA	pwm02. AQCTLB	pwm03. AQCTLA	pwm03. AQCTLB
0	0x0090	0x0600	0x0960	0x0690	0x0060	0x0600
1	0x0690	0x0960	0x0060	0x0600	0x0060	0x0900
2	0x0060	0x0600	0x0090	0x0600	0x0960	0x0690
3	0x0060	0x0900	0x0690	0x0960	0x0060	0x0600
4	0x0960	0x0690	0x0060	0x0600	0x0090	0x0600
5	0x0060	0x0600	0x0060	0x0900	0x0690	0x0960

Table 6.3 AQCTLA register coding for the inversion space vector.

The task of the DSP controller is to calculate the instants for each switching in the boost matrix converter. First, the DSP initializes the direct memory access to the RAM. Hereafter the interrupt system is setup and controlled by PIE controllers. The PWM signals has the priority and starts the conversion for the ADCs. At the beginning of the interrupt service routine the reference values for output frequency and voltage levels are read from the command file that is controlled from the computer via USB. The processor will get the digital readings of the A/D conversion and the angle of the voltage vector is calculated by the software PLL. Both the input current vectors and output voltage vectors are calculated. Knowing these vectors, the modulation index and the boost factor are calculated. The next task is to multiply the duty cycles and determine whether the sum of the hexagon sectors is even or odd. The switching instants are then calculated and scaled for the CMPA and CMPB registers. Even if the proposed control method is simple to implement, it still requires long clock cycles. To reduce this burden switching tables were created for the CMPA and CMPB values for both inversion and rectification stage. The calculated duty cycles are assigned in additions so up or down points are specified for the

AQCTLA values. Such calculations are shown in Table 6.4 for the rectification stage and in Table 6.5 for the inversion stage:

Sectors #	pwm04.CMPA	pwm05.CMPA	pwm06.CMPA
0	0	aPWM	aPWM
1	aPWM	aPWM	0
2	aPWM	0	aPWM
3	0	aPWM	aPWM
4	aPWM	aPWM	0
5	aPWM	0	aPWM

Table 6.4 CMPA registers values for the rectification stage.

Sector #	pwm01. CMPA	pwm01. CMPB	pwm02. CMPA	pwm02. CMPB	pwm03. CMPA	pwm03. CMPB
0	$bPWM$	$bPWM$	$cPWM$	$dPWM$	sPWM	0
1	$cPWM$	$dPWM$	0	sPWM	bPWM	bPWM
2	sPWM	0	$bPWM$	$bPWM$	$cPWM$	$dPWM$
3	$bPWM$	$bPWM$	$cPWM$	$dPWM$	0	sPWM
4	$cPWM$	$dPWM$	$sPWM$	0	$bPWM$	$bPWM$
5	0	$sPWM$	$dPWM$	$dPWM$	$cPWM$	$bPWM$

Table 6.5 CMPA and CMPB registers values for the rectification stage.

For the simplicity, following abbreviations are used for the corresponding gate signals:

$aPWM =$ Dgammaalfa + Dgammabeta

bPWM = Dgammaalfa + Dgammabeta + Ddeltaalfa + Ddeltabeta

$cPWM =$ Ddeltaalfa

$dPWM =$ Dgammabeta + Ddeltabeta + Ddeltaalfa

$$sPWM = Dgammaalfa + Dgammabeta + Ddeltaalfa + Ddeltabeta + Dzero$$

6.4 Conclusion

A 5 kW prototype three-phase boost matrix converter was constructed. The system can be divided into three groups: power circuits, control circuits, and measurement circuits. The power circuits are the IPM and a custom made ultra-sparse rectifier, as well as the input filter and LC network. The interface circuits are employing the gate signals, protection and the modulation control. The control system is based on the Texas Instruments TMS320F28335 microprocessor. The modulator equations are implemented in the processor in C language. The processor serves as a pulse pattern generator, handles all timing issues, PWM control, and ADCs. At a switching frequency of 10 kHz, the control system is loaded approximately 60%.

The matrix converter was implemented using IGBT modules for the rectification stage and IPM for the inversion stage. Thanks for the existence of IPMs the critical protection is applied without any further hardware. The overvoltage, overcurrent, high temperature, and undervoltage of the supply voltages for the gate signals are monitored within the IPM.

Chapter 7

Summary and Conclusion

Conventional ac to ac conversion consists of a PWM rectifier, a dc link, and a PWM inverter. This configuration allows the source-side converter completely regulate the source generator in terms of the speed, power factor, and electromagnetic torque. Compared to the proposed system, this architecture requires a higher number of fully-controlled switches, making the system more expensive, particularly for megawatt-level applications. In addition, the reliability is reduced due to the potential existence of shoot-through states arising from gate-drive failures.

Matrix converters have been proposed as an alternative solution. Direct matrix converters do not need the dc-link capacitor and are topologically simpler. Note that a three-phase to three-phase back-to back converter employs twelve unidirectional switches and twelve freewheeling diodes, while an equivalent direct matrix converter has nine bidirectional switches. Matrix converters can provide a unity input power factor and sinusoidal input and output currents, but the less-than-unity voltage gain constitutes their well-known weakness.

The proposed converter system integrates a source-side three-switch buck-type rectifier and a grid or load side LC network source inverter. The Z-source network allows boosting the voltage two to three times. In practice of wind-energy systems, , the Z-source converter would have to operate under extreme conditions of long shoot-through zero states to provide a higher boost factor needed for a gearless low-voltage generator. The constraints of a low modulation index and a long shoot-through state cause a conflict between the output power quality and the

system's boost ability. Furthermore, the voltage across Z-source capacitors is larger than the input voltage. This compels the use of larger capacitors, which increases the overall cost and volume. Also, the inrush current and resonances at the startup are not suppressed. The switched-inductor, quasi, and series Z-source circuits, subsequently referred to as LCD (inductor-capacitor-diode) networks offer possible solutions to those problems.

7.1 Summary of the Dissertation

The boost matrix converter is an indirect ac to ac converter, In contrast to traditional indirect matrix converters, the boost matrix converters performs voltage boosting retaining the all other aspects of matrix converters. The traditional matrix converters output is limited to 87% of the input voltage. However, with the integration of the LCD networks and properly controlled power switches, low voltage transfer ratio is no longer a concern.

Various modulation techniques are researched for the three-phase and single-phase converters. Huber and Borojevic proposed the indirect space vector modulation scheme in late 80s [55]. That modulation technology offered a theoretical voltage transfer ratio of 87%. Sinusoidal input currents with adjustable phase were obtained. However the quality of the input current and output voltage was directly related to the input displacement angle and with variations over 30^{o} caused reduced quality operating conditions.

The space vector is operated in a vector plane and new switching rules were developed to accommodate the minimum number of switching with minimum number of switches. The optimization in the number of switching is reduced by approximately 10%. The single-phase matrix converter is presented with its combined space vector with unipolar inverter modulation

techniques. It provides the least number of switches in matrix converters named super-sparse converters, with boosting ability.

The PSIM and PLECS proved to be powerful tools for simulation of power electronics converters. A C-script based code is implemented in both simulation tools that give very fast access to simulations at various levels and fast response. The simulations are used in the design of the matrix converter. The power switches alone are not adequate to form matrix converters; some reactive elements are needed as well. An input filter is required to attenuate the switching harmonics of the input current. Furthermore, the LC network between the rectification and inversion stages provides boosting ability. A design example of 5 kW boost matrix converters are carried out. Their resulting values are compared in terms of number of boosting, voltage/current ratings of the components, boost/THD ratios. All measurements show good correspondence to the analytical derivations as well as the simulation results throughout the dissertation.

7.2 Conclusion

The aim of the dissertation was to investigate an alternative to conventional matrix converters, which suffer from a low voltage transfer ratio. Theoretical analyses were carried out, supported by simulations, and verified by experiments. For that purpose a prototype boost matrix converter was built. The contributions to the field of matrix converters achieved in this dissertation can be listed as:

- Novel three three-phase boost matrix converters are designed and described.
- An optimized space vector modulation algorithm has been proposed. The new algorithm minimizes the number of switchings in the boost matrix converter. The

modulation employs the concept of vector plane, and the algorithm is suitable for microprocessor based applications. The algorithm has been implemented in the real-time control system for the converter.

- Novel two single-phase boost matrix converters have been designed and described.
- An optimized single-phase space vector modulation algorithm has been developed and tested by simulations.

7.3 Future Work

Even though good experimental results were obtained, there is still some work to be considered. Certain practical and theoretical difficulties need to be addressed. A further integration of the matrix converter and its auxiliary circuits such as gate drive circuits, input current filter, transducers on a single PCB needs to be attained. A stand-alone control PCB should be designed with TMS320F28335 for real-time applications. Casing and heat sink requirements should be calculated and designed properly for the enclosure.

The quality of the input currents of the all converters need to be improved. A further study of relations between the LC circuits and the input filter circuits is desired, as well as that of the relations between the current quality and the boost factor.

The converter msut be tested under various load conditions. The protection strategy needs to be worked out with or without the clamping circuits. A phase loss is a common problem for the converters. Therefore, a strategy needs to be developed to protect the converter in such cases.

Surface mount based PCB circuit needs to be designed and built for the interface and the measurement circuits. Implementation of generator control and grid tied converters can improve performance of the proposed converters.

Using a matrix converter leads to a considerable reduction in the amount of reactive components. However, the integration of the LC network increases the number of reactive parts. A cost analysis should be done between the conventional matrix converters, back-to-back VSI converters, and the proposed converters.

Matrix converters are very sensitive to distorted input voltages. In the proposed converters, sinusoidal voltage waveforms were assumed but in practice this is not always true. Control algorithms can be improved to compensate for the distorted input voltages to generate balanced sinusoidal input currents and output voltages. The theoretical analysis of the boost matrix converters under unbalanced or distorted input voltage conditions should be expanded.

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