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Thermal Characterization of Silicon Carbide MOSFET Module Suitable for High-Temperature Computationally-Efficient Thermal-Profile Prediction

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***Abstract*—This paper characterizes the thermal behavior of a commercialized silicon carbide (SiC) power MOSFET module with special concerns on high-temperature operating conditions as well as particular focuses on SiC MOSFET dies. A temperature-dependent Cauer-type thermal model of the SiC MOSFET is proposed and extracted based on offline finite-element simulations. This Cauer model is able to reveal the temperature-dependent thermal property of each packaging layer and it is suitable for the high-temperature thermal-profile prediction with sufficient computational efficiency. Due to the temperature-dependent thermal properties of the SiC die and ceramic material, the junction-heatsink thermal resistance can be raised by more than 10% under high-temperature conditions (up to 200 °C), which can considerably worsen thermal estimations of the SiC die and its packaging materials. Furthermore, the experimental measurement of transient thermal impedance was conducted under operating temperature variations (with virtual junction temperature ranging from 60.5 °C to 199.6 °C), and the effectiveness of the proposed temperature-dependent Cauer model was fully validated.**

***Index Terms*—Finite-element method (FEM), high operating temperature, computational efficiency, SiC power MOSFET module, temperature-dependent Cauer model.**

I. Introduction

The power electronic system based on wide bandgap (WBG) devices is by far one of the most promising technologies in order to achieve a large energy efficiency improvement and a potential power-loss reduction by more than 50% [1], [2]. As one of the most popular WBG devices, the silicon carbide (SiC) MOSFET features several superiorities in comparison with the conventional silicon (Si) IGBT [2], e.g., the enhanced electric field, the enhanced thermal conductivity, the high-temperature operation capability, and etc.

Over recent years, the high-temperature capability of SiC MOSFET has always been an active research topic, as it enables new application areas such as automotive, aircraft, and deep-space exploration [3], [4]. It has been demonstrated that the SiC die is capable of operating with junction temperatures being above 200 °C [5]–[8]. Although the rated junction temperatures of commercialized SiC modules are still constrained by conventional die-attach and encapsulation technologies (as lower than 150 °C) [9]–[11], novel materials for die-attach and encapsulation are promising to enable a practical virtual-junction-temperature up to 250 °C [12]–[15].

Nevertheless, the wide utilization of SiC MOSFETs for high-temperature applications is still dramatically prohibited. One of the most significant limiting factors is its reliability uncertainty under such high-temperature conditions, as the lifetime of the power semiconductor is closely related to its thermal profile [16], [17]. Compared to the Si IGBT, the SiC MOSFET is more fragile to transient-overloading or short-circuit events, as it features a more compact die area and thinner gate oxide [18]. On the other hand, if suffered from a long-term high-temperature profile, the SiC MOSFET can be deteriorated by issues such as the inter-layer dielectric erosion, electrode delamination, and time-dependent gate-oxide breakdown [19]. Besides, the long-term thermal cycling with escalated temperature magnitude can easily accelerate the wear-out processes, such as the bond-wire lift-off and solder crack [16], [17]. In order to ensure a reliable operation of the SiC MOSFET throughout its targeted lifespan, a computationally-efficient thermal model suitable for the high-temperature thermal-profile prediction is highly demanded. Then, a mission-profile based reliability assessment methodology can be applied to translate the thermal-profile to a series of quantified reliability metrics [20], [21].

For the present-day thermal-profile prediction of power semiconductors, one of the most prevailing methodologies with a high computational efficiency is to perform thermal simulations using compact resistor-capacitor (RC) lumped thermal models [22], [23], i.e., the Foster-type and the Cauer-type. Specifically, the Foster-type RC-lumped thermal model (the Foster model) can be extracted from experimental measurements of the transient thermal impedance, which is usually accessible from the device datasheet. It has been utilized for the evaluation of long-term thermal profiles of SiC MOSFETs in [24]–[26]. The other Cauer-type RC-lumped thermal model (the Cauer model) is attainable based on the knowledge of device geometry and material property. A conventional yet straightforward method to extracted the RC parameters in the

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Cauer model is based on two analytical equations, as it is discussed in [27]. The applications of Cauer model for the thermal-profile prediction of SiC MOSFET can be found in several works. In [28], a Cauer network of a multi-chip SiC MOSFET module was studied with a special concern on the heat path. Moreover, a measurement method of the Cauer-type thermal model of SiC MOSFETs was proposed in [29].

However, the Foster-type and Cauer-type thermal models discussed above are generally obtained for a specific temperature condition with fixed thermal resistance and capacitance, while their accuracy for the high-temperature thermal prediction is still unknown. Especially, the thermal properties of the SiC die as well as its packaging materials can shift considerably due to effects of free electrons and lattice vibrations [30]. In consideration of this issue, [31] characterized the temperature-dependent thermal performance of a Si IGBT module. It was validated that omitting the temperature effect can lead to unrealistic thermal-profile predictions. Moreover, an electro-thermal model with a special focus on the SiC die was proposed in [32], and the temperature effect of SiC thermal properties was taken into account, which made the proposed model suitable for short-circuit thermal predictions.

Concerning the above mentioned issues, this paper characterizes the high-temperature thermal performance of the SiC power MOSFET module with special focus on SiC MOSFET dies, and a temperature-dependent Cauer model is proposed accordingly. Without losing the generality, a commercialized SiC MOSFET module is utilized as the study case and the high-temperature thermal behavior of SiC MOSFET is fully revealed. The thermal properties of packaging materials (including SiC) are investigated in Section II to demonstrate the physical reason of the temperature effect on thermal performance. In order to be compatible for the long-term thermal-profile prediction, a temperature-dependent Cauer model is extracted based on offline FEM simulations in Section III. The proposed Cauer model fully characterizes the temperature effect on each packaging layer and is suitable for high-temperature thermal profile predictions with sufficient computational efficiency. Furthermore, multiple experimental measurements of the transient thermal impedance were conducted under virtual junction temperature variations from 60.5 °C to 199.6 °C, and the results are given in Section IV. It is concluded that neglecting the temperature-dependency of thermal properties may cause 10% error on the magnitude of thermal resistance. Although experimental validations were conducted up to 199.6 °C on the commercialized SiC MOSFET module, the Cauer model as well as its modeling methodology can also be applied to SiC MOSFET modules with higher operating temperatures. In Section V, the FEM extracted Cauer model is benchmarked with the conventional analytical Cauer model obtained by [27], and it is found that the FEM extracted Cauer model can provide the higher prediction accuracy.

Compared to [31], which studied the temperature effect on thermal models of the Si IGBT, this work characterizes the SiC MOSFET module for a higher junction temperature range as it is driven by the high-temperature capability of SiC. Furthermore, the temperature-dependent thermal property of the ceramic layer is modeled to give a more comprehensive understanding of the temperature effect on SiC thermal modeling. Compared to [32], which focused only on the thermal modeling of SiC die, the whole SiC MOSFET module (from the die to the heatsink) is studied in this work.

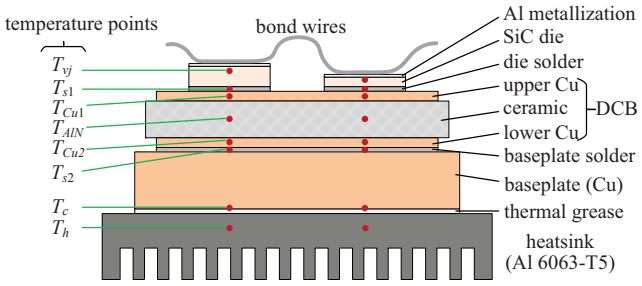


Fig. 1. Vertical view of the studied SiC MOSFET module interfacing with an Al-extrude heatsink.

II. Review of Structure and Thermal Properties of Commercialized SiC MOSFET Module

A. Structure of SiC MOSFET Module

The vertical structure of a commercialized SiC MOSFET module is typically made of multiple layer stacks with various packaging materials, which resembles its Si counterparts. The vertical view of a commercialized SiC MOSFET module is depicted in Fig. 1. The SiC dies are soldered on a direct copper bonded (DCB) substrate, which consists of double copper layers and a ceramic layer sandwiched in between. Likewise, the DCB substrate is fixed on the copper baseplate via the baseplate solder, and the baseplate is mounted on the cooling system via the thermal interface material. Moreover, several temperature measurement points are depicted in Fig. 1, which will be discussed in the following section.

It is noted that the ceramic layer is typically made of from aluminum oxide (Al_2O_3), aluminum nitride (AlN), or silicon nitride (Si_3N_4). Compared with Al_2O_3, the AlN and Si_3N_4 feature higher thermal conductivity, but reduced coefficient of thermal expansion, which are more preferable in high-performance power semiconductor modules.

In this work, a commercialized half-bridge SiC MOSFET module rated at 1200 V and 55 A (APTMC120AM55CT1AG by Microsemi) is adopted as the study case. The top view as well as the circuit diagram of the module are detailed in Fig. 2(a) and Fig. 2(b), respectively. Each SiC switch consists of dual MOSFET dies connected in parallel. In addition, one pair of SiC Schottky-barrier diode (SBD) dies is applied in anti-parallel with each pair of MOSFET dies to mitigate the reverse-recovery current during the switching transient. The geometry dimensions of the SiC MOSFET module under study are listed in Table I. The AlN is utilized in this module as the ceramic material, which features the lowest thermal conductivity among the aforementioned ceramic materials.

B. Temperature-Dependent Thermal Properties of Packaging Materials

For the thermal-profile prediction of power semiconductors, it is generally assumed that the power module is adiabatic from

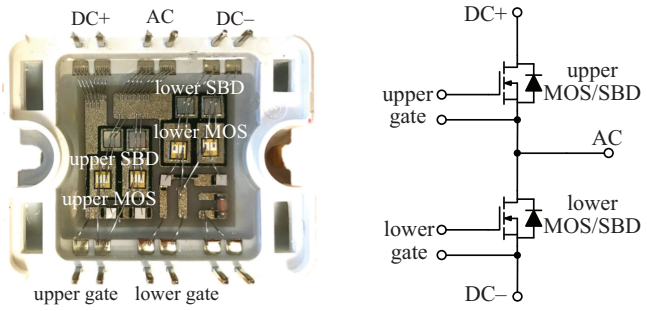


Fig. 2. Half-bridge SiC MOSFET module from Microsemi. (a) Top view. (b) Circuit diagram.

TABLE I
DIMENSIONS OF DIFFERENT LAYERS INSIDE THE STUDIED SIC MODULE (MICROSEMI APTMC120AM55CT1AG).

Layers	Size (mm^2)	Thickness (mm)
MOSFET die	2.80×3.00 (per die)	0.18
SBD die	3.08×3.08 (per die)	0.377
MOSFET solder	2.80×3.00 (per die)	0.09
SBD solder	3.08×3.08 (per die)	0.09
Upper copper	28.2×25.54	0.3
Ceramic (AlN)	28.2×25.54	0.63
Lower copper	28.2×25.54	0.3
Baseplate solder	28.2×25.54	0.2
Baseplate	49.46×40.8	2.5
TIM (silicone grease)	49.46×40.8	0.1

the top and lateral sides. The heat generated from the SiC die propagates through the solder layers, the DCB substrate, and the baseplate and eventually reaches the cooling system, where it is dissipated to the ambient. Therefore, the thermal properties of packaging materials, i.e., the thermal conductivity and specific heat capacity, will significantly affect the heat propagation process and the thermal performance of the SiC MOSFET module.

Specifically, the thermal conductivity measures the ability to conduct heat, which correlates to the thermal resistance in the RC lumped thermal model. The specific heat capacity, on the other hand, defines the quantity of heat required to raise the temperature per unit mass, as it can be characterized as the thermal capacitance in the RC lumped thermal model. Predicting the material temperature based on fixed thermal conductivity and specific heat capacity is regularly straightforward and easily accessible. However, the thermal properties of packaging layers can be considerably affected by material local temperatures due to effects of free electrons and lattice vibrations, which may lead to a significant discrepancy on thermal-profile estimation.

According to [31], [33]–[35], the thermal conductivities and specific heat capacities of various packaging materials (i.e., SiC, AlN, Si_3N_4, Cu, and Al) in correspondence with temperature are exhibited in Fig. 3(a) and Fig. 3(b), respectively. It can be obtained that the thermal conductivities of SiC and AlN feature an intensive temperature dependency, which

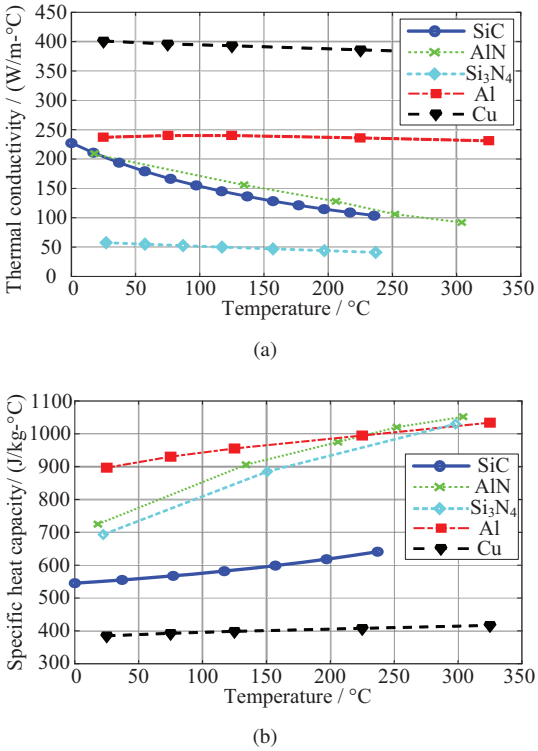


Fig. 3. Temperature-dependent thermal properties of packaging materials of the SiC MOSFET module. (a) Thermal conductivity. (b) Specific heat capacity.

decline with the increase of temperature. Moreover, the Cu and Si_3N_4 also exhibit a non-neglectable temperature dependency, though not comparable with that of the SiC and AlN. In Fig. 3(b), the specific heat capacities of SiC, AlN, Si_3N_4, and Al can be characterized as positively related with the material temperature. Especially, the ceramic materials of AlN and Si_3N_4 exhibit similar and more significant temperature dependencies, whereas other materials of the SiC, Cu, and Al are characterized by less temperature dependencies.

Consequently, neglecting the temperature-dependency of thermal properties of packaging materials may lead to unrealistic temperature estimations. Especially for the case of high-temperature operation, the actual junction temperature of the SiC die can be critically higher than the theoretical estimation without considering the temperature effect, as the thermal conductivities of SiC, AlN, Si_3N_4, and Cu are all negatively related with temperature.

III. EXTRACTION OF TEMPERATURE-DEPENDENT CAUER MODEL BASED ON FEM SIMULATION

For the high-temperature thermal modeling of the SiC MOSFET module, the Cauer-type thermal model is applied in this work, as it is illustrated in Fig. 4. Each packaging layer of the SiC MOSFET module is represented by a thermal capacitance in connection with a thermal resistance. Accordingly, the temperature-dependent thermal properties of each packaging layer can be characterized in this Cauer model.

In order to extract the RC parameters in the Cauer model, FEM based simulations were performed on a three-dimensional (3D) CAD model including geometry and mate-

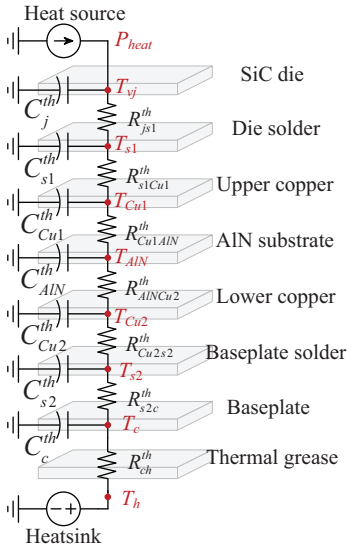


Fig. 4. Equivalent Cauer model of the SiC MOSFET module including structural information.

rial details (especially temperature-dependent thermal properties) of the SiC MOSFET module.

A. Implementation of FEM Simulation

The basic concept of FEM can be considered as subdividing the entire computational domain into separated small-scale parts and calculating local solutions of the diffusion-convection-reaction problem. For the analysis of heat-transfer process, multiple FEM based softwares are available, and the ANSYS/ICEPAK was utilized in this work.

As a study case, a 3D CAD model of the SiC MOSFET module under study was constructed in SOLIDWORKS, and was simulated in ANSYS/ICEPAK (as depicted in Fig. 5). The stacked multi-layer structure of the SiC module (as illustrated in Fig. 1 and Table I) was replicated in the model. The aforementioned thermal conductivities and specific heat capacities with temperature dependency were also programmed in ANSYS/ICEPAK. Then, multiple transient FEM simulations were conducted under different heatsink temperatures (i.e., 20 °C, 50 °C, 80 °C, 110 °C, and 140 °C). The upper-third volume of each MOSFET die was assumed as the heat source, since the generated heat is not uniformly distributed among the die volume but becomes more concentrated towards the upper-third volume of the die [32], [36]. Letting the upper-third die volume to be the heat source helps to better mimic the thermal behaviors inside the die and obtain the more realistic thermal impedance. Basic parameter settings of the FEM simulation are listed in Table II. A minimum time step of 10 μs is selected to fully reveal the transient thermal response, and the maximum value of iterations-per-step is established to be 100 to ensure that the convergence criteria is fulfilled for each time step. The procedures for performing each simulation trial are demonstrated as follows:

1) The external conditions (i.e., the heatsink temperature and the heating power) and material thermal properties are defined prior to the simulation trial.

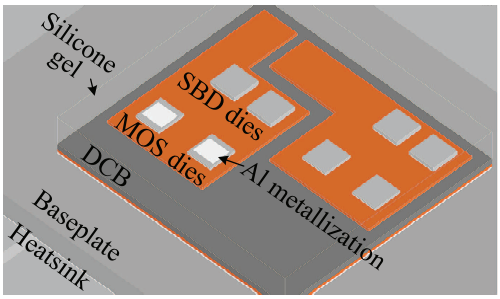


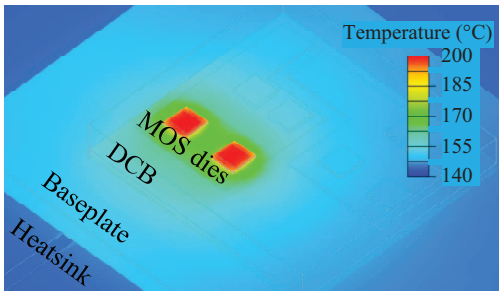
Fig. 5. Geometry overview of the 3D CAD model of the SiC MOSFET module in ANSYS/ICEPAK.

TABLE II
PARAMETER SETTINGS USED FOR THE FEM SIMULATION

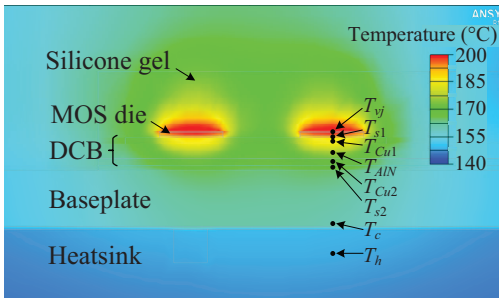
Parameters	Values
Minimum time step	10 μs
Simulation duration	190 s
Maximum iterations/step	100
Convergence criteria (energy)	$\leq 10^{-10}$ J
Minimum mesh size	30 μm
Heating power per die	30 W
Heatsink temperature	20–140 °C

2) During the starting stage of the simulation, a constant heating power P_{heat} = 30 W is applied to each MOSFET die until a thermal equilibrium is reached. The temperature distribution of the thermal equilibrium with heatsink temperature of 140 °C is depicted in Fig. 6. The steady-state temperatures at points of measurements [as indicated in Fig. 6(b)] under the thermal equilibrium are recorded. As the module is filled with silicone gel for insulation purpose (with thermal conductivity of 0.2 W/mK), a small portion of the generated heat can expand towards the top and lateral sides of the power stack at a pretty slow velocity [as can be seen from Fig. 6(b)]. Nevertheless, this effect will not degrade the modeling accuracy, given that the thermal conductivities of power-stack materials are in the range of 100–400 W/mK.
3) After the thermal equilibrium is reached, the heating power is removed and the cooling stage starts. Simultaneously, the transient temperature responses at the points of measurement are then monitored.

Given that the thermal distribution is significantly dependent on geometry and material, the temperature measurement points should be defined in individual layers, and aligned with the center point of the MOSFET die (i.e., T_{s1} on die solder, T_{Cu1} on upper copper, T_{AlN} on AlN ceramic, T_{Cu2} on lower copper, T_{s2} on baseplate solder, T_c on baseplate case, and T_h on heatsink). Specifically, the virtual junction temperature of T_{vj} is recognized as the mean temperature of heated die volume, as the temperature values also become much higher towards the upper-third part of the die [36]. Otherwise, an optimistic thermal expectation shall be obtained if T_{vj} is assumed as the average temperature of the whole die-volume. It is noted that the thermal response of lower MOSFET should be identical with that of the upper MOSFET, since uniform packaging



(a)



(b)

Fig. 6. FEM-simulated steady-state temperature distribution of the SiC MOSFET module under the case of heatsink temperature of 140 °C. (a) Top view. (b) Vertical view.

structures and materials are involved. Moreover, the thermal profile of the SiC MOSFET in FEM simulation shall not be affected by conditions of other power devices.

B. Extraction of Thermal Resistance and Capacitance

Knowing both the steady-state and transient temperature responses at the defined measurement points, the parameters of thermal resistance and capacitance components in the Cauer model can be extracted accordingly.

The aforementioned multi-layer Cauer model is generalized in Fig. 7 for the ease of illustration. First, the thermal resistances of the Cauer model can be obtained according to the steady-state temperature measurements:

$$\begin{cases} R^{th}_{k-1,k} = (T_{k-1,steady} - T_{k,steady})/P_{heat} \\ R^{th}_{k,k+1} = (T_{k,steady} - T_{k+1,steady})/P_{heat} \end{cases} \quad (1)$$

where $T_{k-1,steady}$, $T_{k,steady}$, and $T_{k+1,steady}$ designate the steady-state temperatures of the $(k-1)^{th}$, k^{th}, and $(k+1)^{th}$ measurement points under the thermal equilibrium, respectively. Then, the thermal capacitance of the k^{th} layer, C^{th}_k, can be extracted by:

$$C^{th}_k = P_k(t) \Big/ \frac{dT_k(t)}{dt} \quad (2)$$

$$\begin{cases} P_k(t) = \frac{T_{k-1}(t)-T_k(t)}{R^{th}_{k-1,k}} - \frac{T_k(t)-T_{k+1}(t)}{R^{th}_{k,k+1}}, k \neq 1 \\ P_k(t) = -\frac{T_k(t)-T_{k+1}(t)}{R^{th}_{k,k+1}}, k = 1 \end{cases} \quad (3)$$

where $T_{k-1}(t)$, $T_k(t)$, and $T_{k+1}(t)$ denote the transient temperature responses of the $(k-1)^{th}$, k^{th}, and $(k+1)^{th}$ measurement points obtained from the FEM simulation. Additionally,

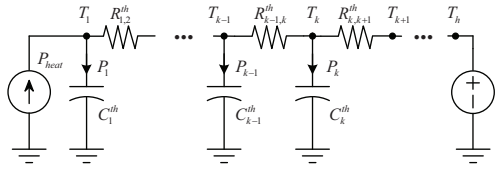


Fig. 7. The generalized multi-layer Cauer model for the extraction of thermal resistance and capacitance parameters.

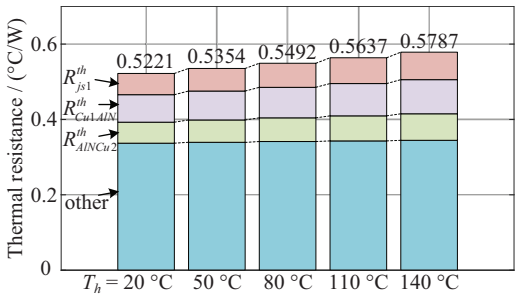


Fig. 8. Bar graph of FEM-extracted thermal resistance values with special emphasises on R^{th}_{js1}, R^{th}_{Cu1AlN}, and R^{th}_{AlNCu2}.

$P_k(t)$ denotes the transient power flowing through the k^{th} thermal capacitor branch.

C. Temperature-Dependent Cauer Model

Using the aforementioned methodology, the thermal resistance and capacitance under heatsink-temperature variations can be obtained accordingly, as listed in Table III. As the heatsink temperature increases from 20 °C to 140 °C, the thermal resistance values related to the SiC die (R^{th}_{js1}) and AlN ceramic (R^{th}_{Cu1AlN} and R^{th}_{AlNCu2}) are increased by 26%, 24%, and 29%, respectively. In contrast, the values of R^{th}_{s1Cu1}, R^{th}_{Cu2s2}, R^{th}_{s2c}, and R^{th}_{ch} are increased by 0.9%, 2.0%, 3.3%, and 2.2%, respectively. Therefore, the temperature-dependency of R^{th}_{s1Cu1}, R^{th}_{Cu2s2}, R^{th}_{s2c}, and R^{th}_{ch} can be omitted as they will not cause significant error to the thermal prediction. The bar-graph demonstrating the thermal resistance values is depicted in Fig. 8. The overall junction-heatsink thermal resistance R^{th}_{jh} is raised by more than 10%, from 0.5221 °C/W to 0.5787 °C/W.

As the heatsink temperature increases from 20 °C to 140 °C, the thermal capacitance values of C^{th}_{s1}, C^{th}_{Cu1}, C^{th}_{AlN}, C^{th}_{Cu2}, C^{th}_{s2} are increased by 15%, 11%, 29%, 16%, and 0.6% respectively, which is caused by the positive temperature dependency of specific heat capacities [illustrated in Fig. 3(b)]. On the other hand, the values of C^{th}_j and C^{th}_c feature a negative temperature-dependency, as they are decreased by 0.9% and 1.5% respectively. Because, for thermal capacitance with greater layer-thickness but less temperature dependency, i.e., C^{th}_j and C^{th}_c, the effect of heat-flux concentration may dominate under a high-temperature-gradient condition [23].

In order to reveal this thermal-resistance-temperature relationship in the Cauer model, curve fittings were performed using linear polynomials. In consideration of easy implementation, only the thermal components with parametric variance higher than 20% throughout the testing range are characterized

TABLE III
PARAMETERS OF THERMAL RESISTANCE AND CAPACITANCE OF THE MULTI-LAYER CAUER MODEL OBTAINED BY FEM SIMULATION.
(UNIT: R^{th} – °C/W, C^{th} – J/°C)

	Heatsink Temperature				
	20 °C	50 °C	80 °C	110 °C	140 °C
R^{th}_{js1}	0.0557	0.0592	0.0629	0.0665	0.0704
C^{th}_{j}	8.20×10^{-3}	8.18×10^{-3}	8.16×10^{-3}	8.16×10^{-3}	8.13×10^{-3}
R^{th}_{s1Cu1}	0.0628	0.0630	0.0632	0.0633	0.0634
C^{th}_{s1}	3.63×10^{-3}	3.76×10^{-3}	3.90×10^{-3}	4.04×10^{-3}	4.19×10^{-3}
R^{th}_{Cu1AlN}	0.0730	0.0767	0.0809	0.0857	0.0905
C^{th}_{Cu1}	1.50×10^{-2}	1.54×10^{-2}	1.58×10^{-2}	1.62×10^{-2}	1.67×10^{-2}
R^{th}_{AlNCu2}	0.0564	0.0599	0.0639	0.0684	0.0730
C^{th}_{AlN}	2.14×10^{-2}	2.30×10^{-2}	2.46×10^{-2}	2.62×10^{-2}	2.75×10^{-2}
R^{th}_{Cu2s2}	0.0390	0.0393	0.0395	0.0397	0.0398
C^{th}_{Cu2}	5.26×10^{-2}	5.44×10^{-2}	5.65×10^{-2}	5.89×10^{-2}	6.12×10^{-2}
R^{th}_{s2c}	0.0811	0.0820	0.0827	0.0832	0.0838
C^{th}_{s2}	8.46×10^{-2}	8.49×10^{-2}	8.51×10^{-2}	8.50×10^{-2}	8.51×10^{-2}
R^{th}_{ch}	0.1542	0.1552	0.1561	0.1569	0.1577
C^{th}_{c}	3.34	3.33	3.32	3.31	3.29
R^{th}_{jh}	0.5221	0.5354	0.5492	0.5637	0.5787

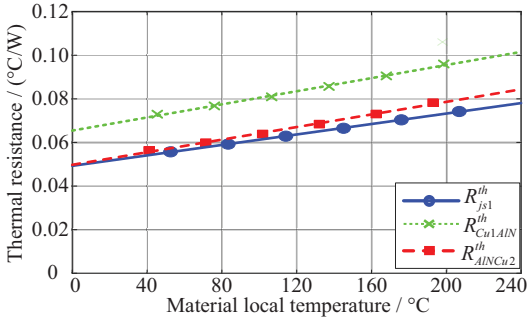


Fig. 9. Temperature-dependent thermal resistances and curve fitting results of R^{th}_{js1}, R^{th}_{Cu1AlN}, and R^{th}_{AlNCu2}.

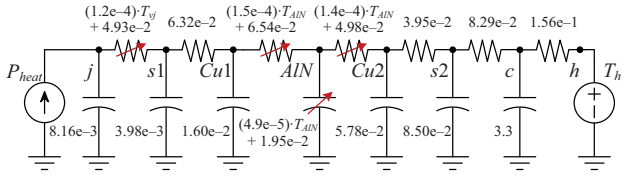


Fig. 10. The FEM-extracted Cauer model with temperature-dependent RC components.

by linear polynomials (i.e., R^{th}_{js1}, R^{th}_{Cu1AlN}, and R^{th}_{AlNCu2}). This selecting criteria also applies for the characterization of thermal capacitances, and only C^{th}_{AlN} with a parametric variance of 29% is modeled using the linear polynomial. As depicted in Fig. 9, the curve fitting results match well with discrete data points and reflect a rising tendency of R^{th}_{js1}, R^{th}_{Cu1AlN}, and R^{th}_{AlNCu2}. Then, the temperature-dependent Cauer model can be concluded accordingly. As illustrated in Fig. 10, the thermal resistance and capacitance components of R^{th}_{js1}, R^{th}_{Cu1AlN}, R^{th}_{AlNCu2}, and C^{th}_{AlN} are characterized as temperature dependent by linear polynomial equations, whereas other components can be regarded as temperature-constant as discussed above.

It is noted that the SiC SBD dies may also operate in applications and generate considerable amount of heat, which may also affect the thermal profiles of MOSFET dies [37]. In this situation, a module-level thermal characterization integrating thermal models of both the MOSFET and SBD shall be required. For that module-level thermal modeling, it is generally assumed that thermal models of the MOSFET and SBD are coupled through either the heatsink or baseplate [36]. Hence, the junction-heatsink (or junction-baseplate) thermal impedances of SiC MOSFET and SBD can be studied independently and integrated together via the heatsink or baseplate node as the module-level thermal model. Moreover, the FEM based modeling method discussed above can also be utilized for the thermal modeling of SiC SBD.

D. Application for Transient Thermal Simulation

As R^{th}_{js1}, R^{th}_{Cu1AlN}, R^{th}_{AlNCu2}, and C^{th}_{AlN} are dependent on material local temperatures, the values of these thermal components should be calibrated prior to the transient thermal simulation. An implementation flowchart of the Cauer-model simulation with a calibration process is depicted in Fig. 11. An iteration process with steady-state thermal calculations (iteration of mean T_{vj} and T_{AlN} and update of R^{th}_{js1}, R^{th}_{Cu1AlN}, R^{th}_{AlNCu2}, and C^{th}_{AlN}) is utilized to calibrate these temperature-dependent components until the convergence condition of $|T_{vj,n} - T_{vj,n}| \leq 1$°C is satisfied. In normal cases, it takes three times of iteration in maximum to reach the convergence condition. Thereafter, the transient thermal simulation can be conducted using the calibrated thermal resistance and capacitance values. A specific application example is demonstrated as follows.

One of the typical heating conditions of SiC power MOSFETs can be considered as a periodic power in a dc/ac inverter

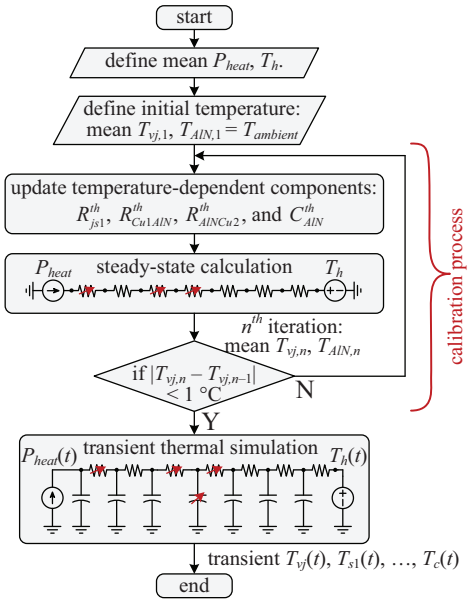


Fig. 11. Implementation flowchart of the Cauer-model simulation with a calibration process.

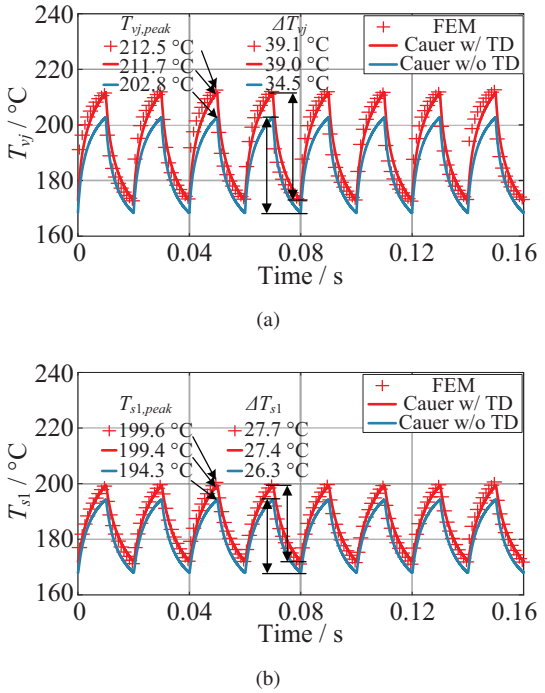


Fig. 12. Temperature profile of the SiC MOSFET module. (a) Cauer-simulated virtual junction temperature of T_{vj} with (w/) and without (w/o) the temperature dependency (TD), as well as the T_{vj} recorded from the FEM simulation. (b) Cauer-simulated die-solder temperature of T_{s1} w/ and w/o the TD, as well as the T_{s1} recorded from the FEM simulation.

application, which comes from switching and conduction losses per half ac-cycle. By simulating the Cauer model in a circuit simulator (MATLAB/Simulink), the virtual junction temperature of T_{vj} under a periodic heating power (square wave with 180 W magnitude, 50% duty cycle, and 50 Hz frequency) is obtained as depicted in Fig. 12(a), and the heatsink temperature is set to be 140 °C. For comparison, the T_{vj} simulated by the FEM simulation (ANSYS/ICEPAK) as well as by the Cauer model without temperature dependency are plotted in Fig. 12(a).

It can be seen that the T_{vj} obtained from the temperature-dependent Cauer model matches satisfactorily with that simulated by ANSYS/ICEPAK in Fig. 12(a). The temperature peaks $T_{vj,peak}$ obtained by the FEM simulation and temperature-dependent Cauer model are observed as 212.5 °C and 211.7 °C respectively (with 0.3% error). Additionally, the amplitudes of temperature swing ΔT_{vj} calculated by the two methods are exhibited as 39.1 °C and 39.0 °C (with 0.2% error). Nevertheless, a significant discrepancy is witnessed if the temperature-dependency of the thermal model is neglected. The maximum disparity of T_{vj} between Cauer-model calculations with and without the temperature dependency counts to be 8.9 °C (with 4.4% error), which occurs at peak points $T_{vj,peak}$ in Fig. 12(a). Moreover, a considerable discrepancy on ΔT_{vj} (with error up to 4.5 °C, 13%) can be observed from Fig. 12(a). Additionally, another reliability-critical variable, the die-solder temperature of T_{s1}, can also be obtained from the temperature-dependent Cauer model, as it is depicted in Fig. 12(b). Similar conclusions can also be drawn.

IV. Experimental Characterization of Transient Thermal Impedance

A. Introduction to Experimental Setup

In order to validate the temperature-dependent Cauer model, an experimental setup was built in laboratory and the junction-heatsink transient thermal impedance of the SiC MOSFET was measured. As demonstrated in Fig. 13, the main circuit of the experimental setup consists of a DC power source, an auxiliary IGBT, and a SiC module APTMC120AM55CT1AG with its peripheral circuits. It is noted that the circuit diagram illustrated above is only valid for the thermal characterization of the SiC MOSFET, not for that of the external SBD. A photograph of the experimental setup is exhibited in Fig. 14. The SiC module was mounted on a Al-extrude heatsink with temperature-control functionality, and a layer of silicone grease (*Dow Corning 340*) was applied in between.

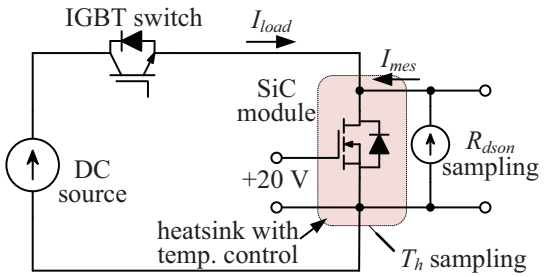


Fig. 13. Main circuit diagram of the experimental setup for the transient-thermal-impedance measurement of SiC MOSFET.

Doing so, the experimental measurement of transient thermal impedance was able to be conducted under temperature variations. The heatsink temperature T_h was sampled via an optic fiber temperature sensor, which was inserted into the heatsink plate. Meanwhile, the on-state resistance of R_{dson} was acquired by external voltage and current probes.

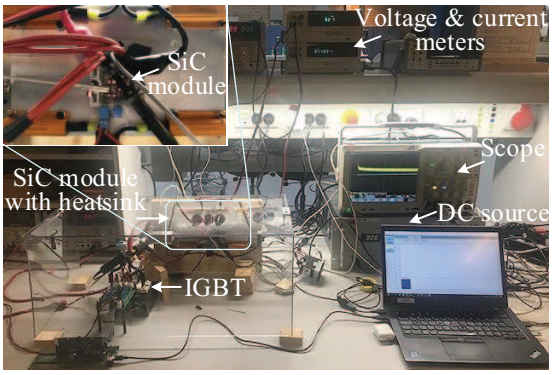


Fig. 14. Photograph of the experimental setup for the transient-thermal-impedance measurement of SiC MOSFET.

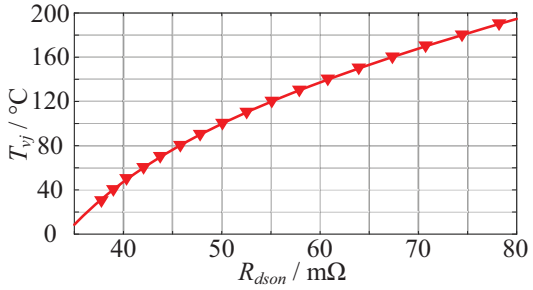


Fig. 15. Virtual junction temperature of T_{vj} in correspondence with the on-state resistance of R_{dson} of the SiC MOSFET module APTMC120AM55CT1AG.

B. Experimental Measurement of Transient Thermal Impedance

As the R_{dson} of the SiC MOSFET features an intensive sensitivity to the temperature, the virtual junction temperature of T_{vj} in time domain can be indirectly obtained by the measured R_{dson} profile [38]. This is also noted as the temperature-sensitive electrical parameter based methodology for junction temperature monitoring.

Without generating heating power from the MOSFET die, the T_{vj} can be assumed identical to the heatsink temperature of T_h once a thermal equilibrium is reached. Then, multiple sets of T_{vj} - R_{dson} data was able to be experimentally measured with the temperature-controlled heatsink. Then, the T_{vj} - R_{dson} function can be acquired as a fractional equation by means of curve fitting:

$$T_{vj}\left(R_{dson}\right) = \frac{n_1 \cdot {R_{dson}}^2 + n_2 \cdot R_{dson} + n_3}{R_{dson} + d_1} \tag{4}$$

where n_1 = 1.842, n_2 = 66.95, n_3 = −4427, and d_1 = −14.67, which can be obtained by the curve-fitting tool of MATLAB. The calibrated T_{vj} - R_{dson} function with the data points are depicted in Fig. 15.

The implementation procedure as well as the temperature responses of the transient thermal impedance measurement are illustrated in Fig. 16. During the initial stage of the experiment, both the auxiliary IGBT and the SiC MOSFET maintained conducted with load current of I_{load} = 30 A supplied by a programmable DC source. The SiC MOSFET works in its ohmic region and its junction temperature was

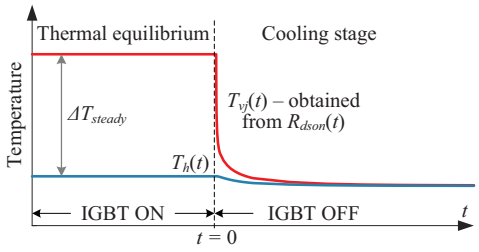


Fig. 16. Implemented test procedure and temperature response of the transient thermal impedance measurement.

heated up by the on-state resistance of R_{dson}. After the thermal equilibrium was reached and the junction temperature was in steady state, the gate voltage of the auxiliary IGBT was removed and the load current was switched-off. Then, the cooling stage starts and a measurement current of I_{mes} = 1 A was injected into the SiC MOSFET die by an external current source in parallel with the device. Meantime, the SiC MOSFET maintained conduction and still worked in the ohmic region. The transient R_{dson} indicating T_{vj} can be sampled by external voltage and current probes. It is noted that the resistive heating power generated by I_{mes} is in the range of tens of miliwatt ($I_{mes}^2 R_{dson}$), therefore the I_{mes} will not affect the accuracy of the measurement.

Multiple experimental measurements were conducted with different heatsink temperatures, i.e., T_h = 37 °C, 70.2 °C, 113.3 °C, and 145.8 °C. The load current of I_{load} = 30 A was applied and a broad range of junction temperature was reached during the experiment (see Table IV). It is noted that the transient thermal impedance under the T_{vj} of 199.6 °C was successfully tested, which is 50 °C higher than its rated junction temperature.

Once the transient virtual junction temperature of $T_{vj}(t)$ and the heatsink temperature of $T_h(t)$ were obtained from the cooling stage of the experiment, the transient thermal impedance from junction to heatsink can be calculated by:

$$Z_{jh}^{th}(t) = \frac{-\left[T_{vj}(t) - T_h(t)\right] + \Delta T_{steady}}{P_{heat}} \tag{5}$$

where ΔT_{steady} and P_{heat} denote the steady-state junction-heatsink temperature difference and the die loss, respectively.

C. Experiment Results and Comparison

The measured junction-heatsink transient thermal impedance of $Z_{jh}^{th}(t)$ under heatsink conditions of T_h = 37 °C, 70.2 °C, 113.3 °C, and 145.8 °C are depicted in Fig. 17(a)–(d), respectively. The thickness variations of $Z_{jh}^{th}(t)$ curves in Fig. 17(a)–(d) are induced by the noise-level differences under various P_{heat} conditions, as a higher P_{heat} value also helps to attenuate the measurement noises of $T_{vj}(t)$ according to (5). In order to do validation, the $Z_{jh}^{th}(t)$ simulated by the temperature-dependent Cauer model are also studied as exhibited in dashed curves, and identical external conditions (P_{heat} and T_h) are assumed in Cauer-model simulations. A steady-state error of lower than 0.9% between the Cauer-model simulation and experimental

TABLE IV
EXTERNAL CONDITION AND STEADY-STATE RESULTS OF MULTIPLE EXPERIMENTS UNDER THERMAL EQUILIBRIUM.

	Experiment No.			
	Expt 1	Expt 2	Expt 3	Expt 4
Heatsink temperature T_h	35.7 °C	70.2 °C	113.3 °C	145.8 °C
Load current I_{load}	30 A	30 A	30 A	30 A
Junction loss P_{heat}	46.3 W	55.4 W	73.2 W	91.9 W
Virtual junction temperature T_{vj}	60.5 °C	100.2 °C	154.9 °C	199.6 °C

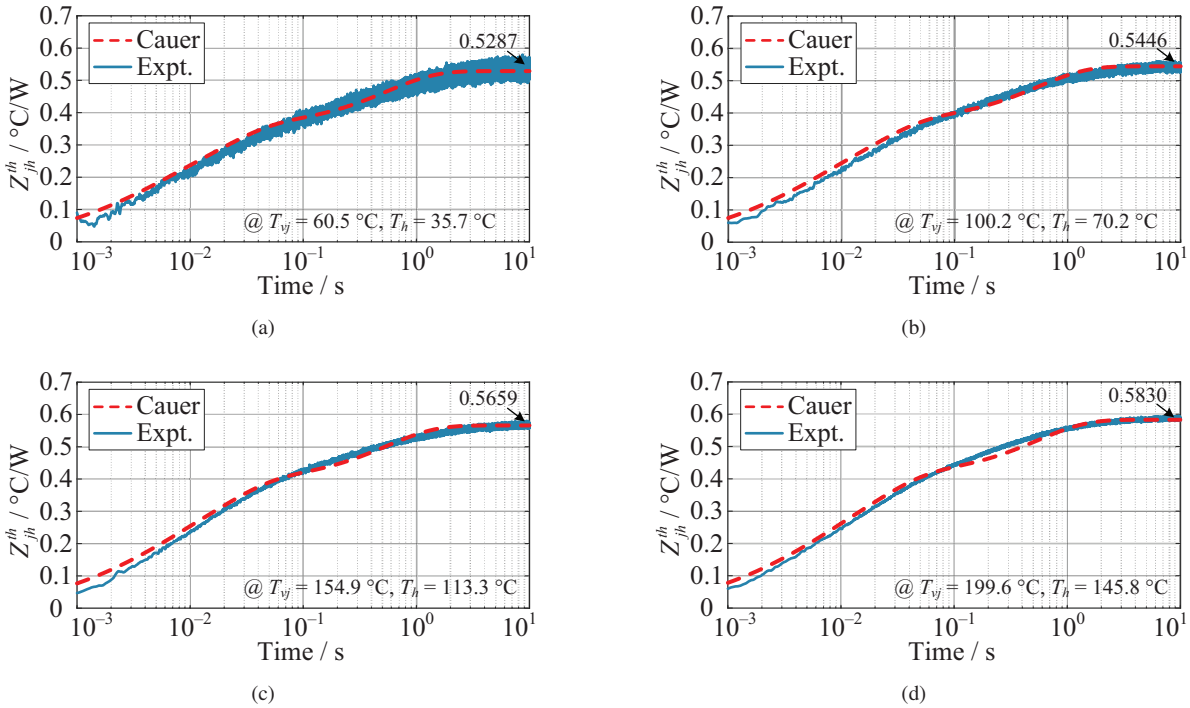


Fig. 17. Junction-heatsink transient thermal impedance obtained by both experimental measurements and the temperature-dependent Cauer model with different temperature conditions. (a) T_h = 35.7 °C, I_{load} = 30 A. (b) T_h = 70.2 °C, I_{load} = 30 A. (c) T_h = 113.3 °C, I_{load} = 30 A. (d) T_h = 145.8 °C, I_{load} = 30 A.

measurement applies for all of the conditions studied. It can be concluded that the proposed temperature-dependent Cauer model can characterize transient thermal behaviors of a real SiC MOSFET with limited error-band under both the normal and high-temperature conditions. Furthermore, the amplitude of the measured thermal impedance, i.e., the R^{th}_{jh}, is raised by more than 10% (from 0.5287 °C/W to 0.5830 °C/W) as T_{vj} increases from 60.5 °C to 199.6 °C, as indicated in Fig. 17.

V. BENCHMARKING OF MODELING METHODOLOGIES OF CAUER-TYPE THERMAL MODELS

As validated in Section IV, the FEM-extracted Cauer model is able to predict the high-temperature thermal performance of the SiC MOSFET module under both the transient- and steady-state. Other than conducting parameter extractions by FEM simulations, the conventional method studied in [27] can also be a promising solution for the establishment of the Cauer model, by which the temperature dependencies of thermal behaviors can be modeled using two analytical equations. This section will give an introduction to this method and provide a performance benchmarking of these two approaches.

A. Introduction to the Analytical Methodology

According to the Fourier's Law for heat conduction, the thermal resistance of each packaging layer can be calculated from the thermal conductivity of its forming material:

$$R^{th} = \frac{1}{k} \cdot \frac{d}{A} \tag{6}$$

where k is the material thermal conductivity, d is the heat-dissipation distance, and A is the effective cross-sectional area for heat spreading. An example for d_{AlN} and A_{AlN} identifications is demonstrated in Fig. 18. More analysis on the calculation of effective heat-spreading area can be found in [39].

Additionally, the thermal capacitance of single layer is able to be attained from its specific heat capacity:

$$C^{th} = c_h \cdot \rho \cdot d \cdot A \tag{7}$$

where ρ is the mass density of material, and c_h is the specific heat capacity. By applying (6) and (7), it is noted that the heat flux and temperature distribution of each physical layer are

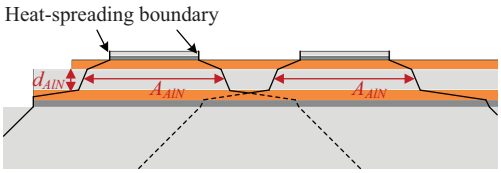


Fig. 18. Vertical view of the heat-spreading boundary and identifications of heat-dissipation distance d and effective cross-sectional area A of the AlN layer.

TABLE V
PARAMETER VALUES UTILIZED FOR ANALYTICAL CALCULATION OF THERMAL RESISTANCE AND CAPACITANCE

Component	Related layer	ρ (g/cm^3)	d (mm)	A (mm^2)
R^{th}_{js1}	j	—	0.12	16.8
R^{th}_{Cu1AlN} + R^{th}_{AlNCu2}	$Cu1$	—	0.15	20.5
	AlN	—	0.63	34.1
	$Cu2$	—	0.15	51.2
C^{th}_{j}	j	3.10	0.18	16.8
C^{th}_{AlN}	AlN	3.26	0.63	34.1

simplified as uniformly distributed within the defined cross-sectional area of A.

As the temperature dependencies of thermal conductivities and specific heat capacities can be obtained from Fig. 3, the temperature-dependent thermal resistance and capacitance are also able to be modeled according to (6) and (7).

B. Performance Benchmarking of Modeling Methodologies

In order to benchmark their ability to model the temperature-dependent thermal resistance, the values of R^{th}_{js1} and $R^{th}_{Cu1AlN} + R^{th}_{AlNCu2}$ obtained from both the FEM extraction and what is derived by (6) are detailed in Fig. 19(a). The values of heat-dissipation distance d and effective cross-sectional area A utilized for analytical derivations are listed in Table V for reference. It is observed in Fig. 19(a) that the temperature dependency is able to be characterized by (6), as comparable resistance-temperature slew rates are exhibited from both methods. Nonetheless, the analytical method shows relatively lower thermal resistance values, since (6) assumes an equalized distribution of the heat flux among the effective cross-sectional area. In contrast, the heat flux can be more concentrated beneath the center of the SiC die in FEM simulations, which better imitates the real heat-spreading scenario.

Moreover, the parameters of C^{th}_{j} and C^{th}_{AlN} calculated by (7) are compared with FEM extractions in Fig. 19(b), where an analogous explanation also applies. The values of ρ, d, and A used in (7) are also given in Table V for reference. As the temperature-field assumed in (7) is regarded as homogeneous among the effective heat-spreading area, more Joules of energy are to be calculated in (7) to heat up the whole area per Celsius degree, i.e., more thermal capacitance compared to FEM extractions. Consequently, a significant discrepancy on C^{th}_{AlN} can be observed in Fig. 19(b). In spite of this, the

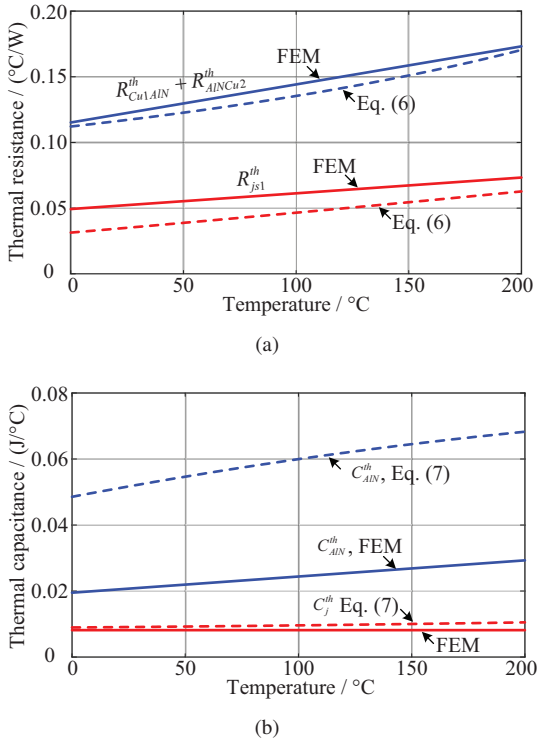


Fig. 19. Benchmarking of temperature-dependent thermal resistances and capacitances obtained from both the FEM extraction and the analytical equations. (a) R^{th}_{js1} and $(R^{th}_{Cu1AlN} + R^{th}_{AlNCu2})$. (b) C^{th}_{j} and C^{th}_{AlN}.

calculation on C^{th}_{j} exhibits a satisfactory match with its FEM extraction since the heat-spreading area of the SiC die is not comparable with that of the AlN ceramic layer and less computational error shall be incurred.

Overall, as featured by lower thermal resistances and higher thermal capacitances, the conventional method [by analytical equations (6) and (7)] will expect a relatively more optimistic thermal-profile estimation when compared with the FEM based method studied in this work. Nevertheless, it should also be pointed out that these two methods summarized in this work are currently unable to characterize the thermal degradation induced by the aging process of power device.

VI. CONCLUSION

This paper characterizes the thermal performance of a commercialized SiC MOSFET module with special concerns on high-temperature operating conditions as well as a particular focus on SiC MOSFET dies. It is found that the temperature-dependent thermal properties of the SiC die and AlN ceramic can considerably worsen the thermal performance under high operating temperature. Then, a temperature-dependent Cauer-type thermal model of the SiC MOSFET is extracted in this work based on FEM simulations, which is able to reveal the temperature-dependent thermal properties of packaging layers and it is suitable for high-temperature thermal-profile prediction with sufficient computational efficiency.

It is concluded from the proposed Cauer model that the overall thermal resistance can be raised by more than 10% under high-temperature conditions (up to 200 °C). An application case with periodic heating power has demonstrated

that the predicted virtual junction temperature of T_{vj} can be raised by 8.9 °C with the consideration of temperature dependency. Additionally, the junction temperature swing of ΔT_{vj} is elevated by 4.5 °C using the extracted Cauer model.

Furthermore, the accuracy of the extracted temperature-dependent Cauer model was validated through experiments. Multiple experimental measurements of thermal impedances were conducted under both normal- and high-temperature conditions (60.5–199.6 °C), and their transient thermal impedance curves match satisfactorily for a broad temperature range. A steady-state error of lower than 0.9% between the Cauer-model simulation and experimental measurement applies for all of the conditions studied. Additionally, the accuracy of the FEM-extracted Cauer model is proven to be more superior through the benchmarking with an analytical Cauer model.

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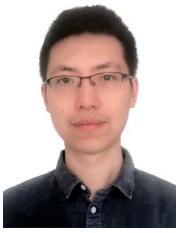

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