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Common-Mode Resonance Damping and DC Voltage Balancing Strategy for LCCL-Filtered Three-Level Photovoltaic Grid-Tied Inverters

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ABSTRACT The leakage current caused by common-mode (CM) voltage is a critical issue in transformerless three-level photovoltaic (PV) inverters, which can increase the output current distortion, bring extra power losses, aggravate the electromagnetic interference, and even cause degradation of the panels and safety issues. The LCCL filter was proven to be effective to mitigate the leakage current, whose capacitor is split into two parts, and the common point of the smaller one is connected to the neutral-point (NP) of the DC-link. However, the LCCL-filtered three-level inverter suffers from the CM resonance of the neutral current and the NP voltage imbalance. Therefore, this paper proposes a CM resonance damping and NP voltage balancing strategy for the transformerless LCCL-filtered three-level PV inverter. A novel dual-cascade-loop with a dc voltage-difference outer-loop and a neutral-current inner-loop is proposed to control the CM voltage with a $\alpha\beta\gamma$-frame space vector pulse width modulation (SVPWM) for damping the CM resonance and balancing the NP voltage. At last, the effectiveness of the proposed strategy is experimentally validated through a 10 kW transformerless LCCL-filtered T-type three-level PV inverter.

INDEX TERMS Common-mode (CM) resonance, LCCL filter, leakage current, neutral-point (NP) voltage, three-level inverter.

I. INTRODUCTION

Transformerless three-level inverters have been widely used in photovoltaic (PV) systems due to its high integration, high efficiency, low cost, and small total harmonic distortion of output voltage and current. However, the leakage current caused by common-mode (CM) voltage is a critical issue in transformerless three-level PV inverters, which can increase the output current distortion, bring extra power losses, aggravate the electromagnetic interference, and even cause safety issues [1]–[3].

Besides improving the modulation schemes [4]–[6] and blocking the flowing path of the leakage current [7], [8], bypassing the leakage current is also widely adopted to minimize the leakage current. The modified LCL (MLCL) filter is firstly used to bypass the leakage current by connecting the common point of the capacitors of LCL filter to the neutral point (NP) of the DC-link [1], [2], [9]–[12], as shown in Fig. 1(a). The topology can provide a low-impedance path and force the leakage current to circulate within the inverter rather than through the ground. Nevertheless, its filter capacitors are involved in both CM and differential-mode (DM) circuits [13], which means that the design of the capacitors need simultaneously satisfy the CM and DM requirements. It is thus hard to choose an appropriate capacitance value. As an optimization, a LCCL filter shown in Fig. 1 (b) was proposed in [13], whose capacitors are split into two parts, and the common point of the smaller one is connected to the NP of the DC-link. With the LCCL filter, the CM and DM circuit parameters can be decoupled by introducing decoupling factor λ, which will favor the design of filter capacitors [13]. Meanwhile, the resistance of the CM filter capacitor is enlarged ($1/\lambda\omega C_f > 1/\omega C_f$), which can restrict the neutral current to some extent and further reduce power loss. However, no matter the MLCL or LCCL filter is still confronted with the risk of the CM resonance.

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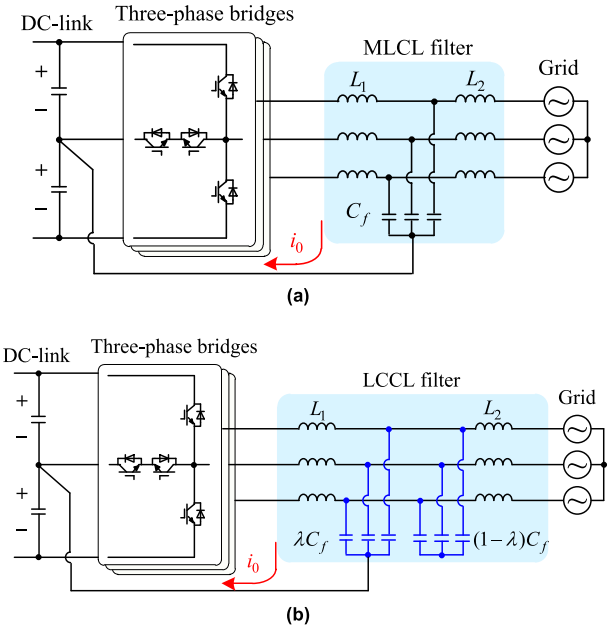

FIGURE 1. Topologies with (a) MLCL-filtered three-level inverter and (b) LCCL-filtered three-level inverter.

Passive damping methods such as inserting physical resistors in the capacitor branch of the LCCL filter can effectively damp the CM resonance, but will cause extra power loss [2], [14]. The active damping method is obviously a better choice. Although comprehensive active damping methods have been proposed for the DM resonance in the LCL filter [15]–[17], there are few methods focusing on the CM resonance damping in the LCCL filter of the three-level inverter. Only two types of active damping schemes have been reported recently to damp the CM resonance in the PV inverter with MLCL filter [1], [2]. Reference [1] proposed a zero-sequence voltage close-loop control strategy based on full state feedback to damp the CM resonance. And in [2], a CM current control with disturbance feed-forward was proposed to suppress the CM resonance.

However, both the CM resonance active damping methods changed the dwell time of redundant vectors to modulate the zero-sequence voltage [1], [2], which might result in the NP voltage imbalance [18], [19]. Therefore, [1] and [2] took extra measures to balance the NP voltage. In [1], a typical signal was superimposed onto the zero-sequence voltage reference to extend the inverter modulation index and to balance the NP voltage. However, the mechanism of NP voltage balancing was not discussed. In [2], besides a CM current control loop with a zero reference, an extra NP voltage balancing loop was added to equalize positive and negative dc voltages. However, because the outputs of the two independent loops were both zero-sequence voltages, they might interfere with each other and even cause conflicts. Therefore, it is necessary to integrate the two independent loops together and avoid the conflicts.

In this paper, the main contributions are as follows

- The relationship between the dc voltage-difference and the neutral current is established. Based on that, a novel dual-cascade-loop with a dc voltage-difference outer-loop and a neutral-current inner-loop is proposed. The integrated dual-loop structure can simultaneously damp the CM resonance and balance the NP voltage without any conflicts.
- Both the inner- and outer-loop controllers are carefully designed to ensure system ability and zero steady-error.

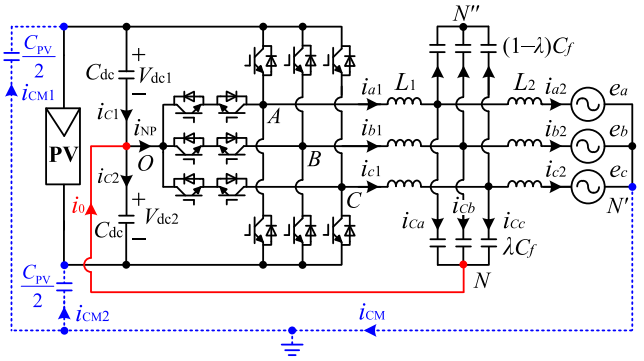

FIGURE 2. LCCL-filtered transformerless three-level PV inverter.

The remaining part of this paper is structured as follows. In Section II, the CM model of the LCCL-filtered three-level inverter is derived to demonstrate the CM resonance and the NP voltage imbalance issues. The dual-loop control strategy for damping CM resonance and balancing NP voltage is then proposed in Section III. And the design of the controllers is fully discussed. Finally, in Section IV, the experimental results on a 10 kW transformerless LCCL-filtered three-level T-type PV inverter are presented to verify the effectiveness of the proposed strategy.

II. CM MODEL OF THE LCCL-FILTERED INVERTER

Fig. 2 shows the LCCL-filtered transformerless T-type three-level PV inverter [13]. C_{PV} is the stray capacitance between PV panels and the ground, which can cause the leakage currents i_{CM1} and i_{CM2}. The resistances of L_1 and L_2 are neglected for emulating a worst-case scenario. The LCCL filter consists of two groups of star-connected capacitors. The common point N of the smaller capacitors $\lambda C_f (0 < \lambda < 0.5)$ is connected to the NP of the DC-link for mitigating the leakage current, and the smaller and the larger capacitors are both used for filtering high-frequency harmonics in the output differential mode (DM) currents. The value of λ can be chosen according to [13].

The CM model of the LCCL-filtered three-level inverter is derived as follows. In Fig. 2, the voltages across the output terminals A, B, C and the NP of the DC-link can be expressed as

$$\begin{cases} v_{AO} = L_1 \dfrac{di_{a1}}{dt} + L_2 \dfrac{di_{a2}}{dt} + e_a + v_{N'O} \\ v_{BO} = L_1 \dfrac{di_{b1}}{dt} + L_2 \dfrac{di_{b2}}{dt} + e_b + v_{N'O} \\ v_{CO} = L_1 \dfrac{di_{c1}}{dt} + L_2 \dfrac{di_{c2}}{dt} + e_c + v_{N'O} \end{cases} \tag{1}$$

where $v_{N'O}$ can be derived from the grounded path in Fig. 2

$$\begin{cases} v_{N'O} = \dfrac{2}{C_{\mathrm{PV}}} \displaystyle\int i_{\mathrm{CM1}} dt + V_{\mathrm{dc1}} \\ v_{N'O} = \dfrac{2}{C_{\mathrm{PV}}} \displaystyle\int i_{\mathrm{CM2}} dt - V_{\mathrm{dc2}}. \end{cases} \tag{2}$$

Through the neutral line in Fig. 2, the output voltages of the inverter can also be expressed as

$$\begin{cases} v_{AO} = L_1 \dfrac{di_{a1}}{dt} + \dfrac{1}{\lambda C_f} \int i_{Ca} dt \\ v_{BO} = L_1 \dfrac{di_{b1}}{dt} + \dfrac{1}{\lambda C_f} \int i_{Cb} dt \\ v_{CO} = L_1 \dfrac{di_{c1}}{dt} + \dfrac{1}{\lambda C_f} \int i_{Cc} dt. \end{cases} \tag{3}$$

According to [4]–[6], the CM voltage v_{CM} can be defined as

$$v_{\mathrm{CM}} = \frac{1}{3}(v_{AO} + v_{BO} + v_{CO}). \tag{4}$$

In addition, the leakage current i_{CM} and the neutral current i_0 can be expressed as

$$\begin{cases} i_{\mathrm{CM}} = i_{\mathrm{CM1}} + i_{\mathrm{CM2}} = i_{a2} + i_{b2} + i_{c2} \\ i_0 = i_{Ca} + i_{Cb} + i_{Cc} \\ i_{\mathrm{CM}} + i_0 = i_{a1} + i_{b1} + i_{c1}. \end{cases} \tag{5}$$

By summing the three equations in (1) and (3), the CM voltage can be respectively expressed as

$$v_{\mathrm{CM}} = \frac{1}{3} L_1 \frac{d(i_{CM} + i_0)}{dt} + \frac{1}{3} L_2 \frac{di_{CM}}{dt} + v_{N'O} \tag{6}$$

$$v_{\mathrm{CM}} = \frac{1}{3} L_1 \frac{d(i_{\mathrm{CM}} + i_0)}{dt} + \frac{1}{3} \frac{1}{\lambda C_f} \int i_0 dt. \tag{7}$$

And the dc voltage-difference ΔV_{dc}, which reflects the NP voltage fluctuation, can be derived from (2) as

$$\Delta V_{\mathrm{dc}} = V_{\mathrm{dc1}} - V_{\mathrm{dc2}} = 2v_{N'O} - \frac{2}{C_{\mathrm{PV}}} \int i_{\mathrm{CM}} dt \tag{8}$$

With v_{CM} in (7) substituted into (6) and $v_{N'O}$ in (6) substituted into (8), the following equation can be deduced

$$\Delta V_{\mathrm{dc}} = 2\left(\frac{1}{3} \frac{1}{\lambda C_f} \int i_0 dt - \frac{1}{3} L_2 \frac{di_{\mathrm{CM}}}{dt} - \frac{1}{C_{\mathrm{PV}}} \int i_{\mathrm{CM}} dt \right). \tag{9}$$

Based on (7) and (9), the CM model of the LCCL-filtered three-level inverter can be obtained as shown in Fig. 3. The CM voltage v_{CM} generates the leakage current i_{CM} through the $L_1 \sim L_2 \sim C_{\mathrm{PV}}/3$ branch. With the connection between the common point N of λC_f and the NP of the DC-link, the extra neutral current i_0 is generated in the $L_1 \sim \lambda C_f$ branch. Considering $\lambda C_f \gg C_{\mathrm{PV}}/3$, the impedance of the $L_1 \sim \lambda C_f$ branch for the high-frequency i_{CM} is much smaller than that of the $L_1 \sim L_2 \sim C_{\mathrm{PV}}/3$ branch. Thus, i_{CM} in the $L_1 \sim L_2 \sim C_{\mathrm{PV}}/3$ branch can be significantly mitigated.

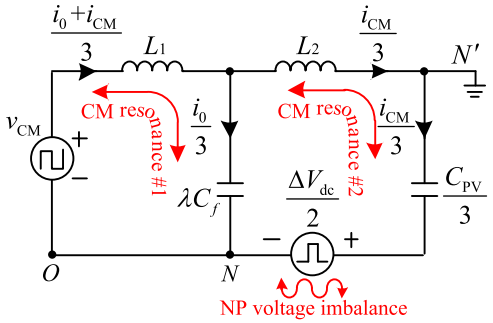

FIGURE 3. CM model of the LCCL filtered transformerless three-level PV inverter.

According to Fig. 3, the transfer function from CM voltage v_{CM} to leakage current i_{CM} can be derived as

$$G_{CM}(s) = \frac{i_{\mathrm{CM}}(s)}{v_{\mathrm{CM}}(s)} = \frac{3C_{\mathrm{PV}} s}{L_1 L_2 C_{\mathrm{PV}} \lambda C_f s^4 + \left(3L_1 \lambda C_f + L_1 C_{\mathrm{PV}} + L_2 C_{\mathrm{PV}}\right) s^2 + 3} \tag{10}$$

There are two resonance frequencies in the transfer function [1], [2], which can be expressed respectively as

$$\begin{cases} f_{r1} \approx \dfrac{1}{2\pi \sqrt{L_1 \lambda C_f}} \\ f_{r2} \approx \dfrac{\sqrt{3}}{2\pi \sqrt{L_2 C_{\mathrm{PV}}}} \end{cases} \tag{11}$$

It can be inferred that, although the leakage current can be effectively mitigated in the LCCL-filtered three-level inverter, there still are two concomitant issues to be solved.

One issue is the CM resonances in the $L_1 \sim \lambda C_f$ and $L_2 \sim C_{\mathrm{PV}}/3$ branches caused by the CM voltage v_{CM}. Note that, the parasitic capacitance C_{PV} of the photovoltaic array in f_{r2} is usually uncertain and varies with humidity, temperature, etc. In addition, as indicated in [1] and [2], the possible resonance frequency f_{r2} is usually much higher than the switching frequency, which makes it uncontrollable. Therefore, only the active damping for the first resonance frequency f_{r1} is implemented, while that for the second resonance frequency f_{r2} is not considered in this paper.

The other issue is the imbalanced NP voltage in Fig. 3. Therefore, auxiliary current and voltage loops are proposed in this paper to actively damp the CM resonances and balance the NP voltage, which will be presented in detail in next section.

III. CM RESONANCE DAMPING AND NP VOLTAGE BALANCING DUAL-LOOP CONTROL STRATEGY

A. NEUTRAL-CURRENT INNER-LOOP FOR CM RESONANCE DAMPING

Considering $\lambda C_f \gg C_{\mathrm{PV}}/3$ and $i_{\mathrm{CM}} \ll i_0$, the leakage current i_{CM} in (6) can approximately be neglected [2]. The transfer

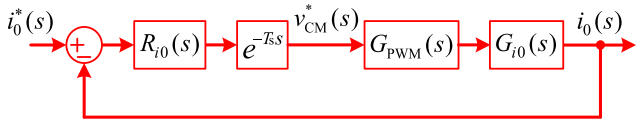

FIGURE 4. Block diagram of the neutral-current loop.

function from v_{CM} to i_0 can then be given by

$$G_{i0}(s) = \frac{i_0(s)}{v_{CM}(s)} = \frac{3\lambda C_f \omega_r^2 s}{s^2 + \omega_r^2} \tag{12}$$

where the CM resonance angle frequency $\omega_r = 2\pi f_{r1}$.

According to (12), there is no pole located in the left-half complex plane. If the neutral-current is operated in open-loop and v_{CM} contains a component near the resonance frequency, a current resonance will be generated by the CM voltage in the $L_1 \sim \lambda C_f$ branch, which may further trigger the overcurrent protection of the inverter. Therefore, an effective damping method is necessary in the LCCL-filtered three-level inverter to suppress the CM resonance.

Being similar to the conventional DM resonance suppression of the LCL filter, passive and active damping methods can be applied to damp the CM resonance. The passive damping will sacrifice the attenuation performance in high-frequency range and cause more loss [14]. The active damping method is thus preferred. A simple active damping method is to construct the closed-loop control of the neutral-current and to ensure that the resonance frequency and time delay meet the stability requirement [6]. The block diagrams of neural-current loop are depicted in Fig. 4.

In Fig. 4, $e^{-T_s s}$ represents the delay caused by sampling and control, where T_s is the control period. $G_{PWM}(s)$ is the transfer function of PWM, and it is usually considered as a delay of $e^{-0.5\,T_s s}$. $R_{i0}(s)$ is the current controller. The neutral-current feedback is calculated by adding three-phase inverter-side currents.

B. DC-VOLTAGE DIFFERENCE OUTER-LOOP FOR NP VOLTAGE BALANCING

To attach a cascaded outer-loop for the NP voltage balancing, the relationship between the neutral current i_0 and the dc-voltage-difference ΔV_{dc} need be established. Referring to Fig. 2, the positive and negative capacitors should meet

$$\begin{cases} C_{dc}\dfrac{d\,(V_{dc1})}{dt} = i_{C1} \\ C_{dc}\dfrac{d\,(V_{dc2})}{dt} = i_{C2} \end{cases} \tag{13}$$

Though the upper and lower capacitors are not absolutely identical [26], their difference is quite small and is neglected in this paper. Meanwhile, according to the Kirchhoff's current law, their currents should satisfy

$$i_{C2} = i_{C1} + i_0 - i_{NP} \tag{14}$$

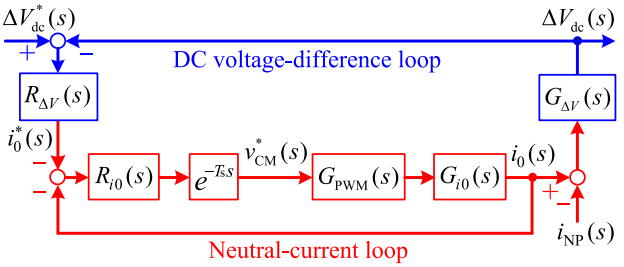

FIGURE 5. Proposed CM resonance damping and NP voltage balancing strategy.

Therefore, the relationship between i_0 and ΔV_{dc} can be derived as

$$C_{dc}\frac{d\,(\Delta V_{dc})}{dt} = -i_0 + i_{NP}. \tag{15}$$

According to (15), if the integral of i_0 is equal to that of i_{NP} in a period, ΔV_{dc} will not change. But if the reference $i_0^*(s)$ of the neutral-current loop shown in Fig. 4 is set to be zero or other constant value, the above conditions cannot be met because i_{NP} is not zero or constant. Then ΔV_{dc} will change and the imbalance of NP voltage will occur. Therefore, it is essential to set an appropriate reference $i_0^*(s)$ for the inner-loop through the dc-voltage difference outer-loop.

Regarding i_{NP} as a disturbance term in (15), the transfer function from i_0 to ΔV_{dc} can be obtained as

$$G_{\Delta V}(s) = \frac{\Delta V_{dc}(s)}{i_0(s)} = -\frac{1}{C_{dc}s}. \tag{16}$$

Based on (16), a voltage-difference outer-loop is thus proposed to balance the NP voltage as shown in Fig. 5, where $R_{\Delta V}(s)$ represents the outer voltage-difference regulator, and the superscript '$*$' denotes the reference variables. It can be inferred that, with the cascaded dual-loop control structure, the control commands of the inner- and outer-loop are harmonically integrated rather than interfere with each other.

C. DESIGN DETAILS FOR THE INNER- AND OUTER-LOOP CONTROLLER

1) DESIGN DETAILS FOR INNER-LOOP CONTROLLER

Since the primary objective of the inner-loop is to damp the resonance and ensure the stability of CM circuit, the proportional (P) controller is quite enough to achieve an adequate stability margin. And the open-loop transfer function of the neutral-current inner-loop shown in Fig. 4 can be expressed as

$$H_{i0}(s) = R_{i0}(s)e^{-T_s s}G_{PWM}(s)G_{i0}(s) = k_{ip}\frac{3\lambda C_f \omega_r^2 s}{s^2 + \omega_r^2}e^{-1.5T_s s} \tag{17}$$

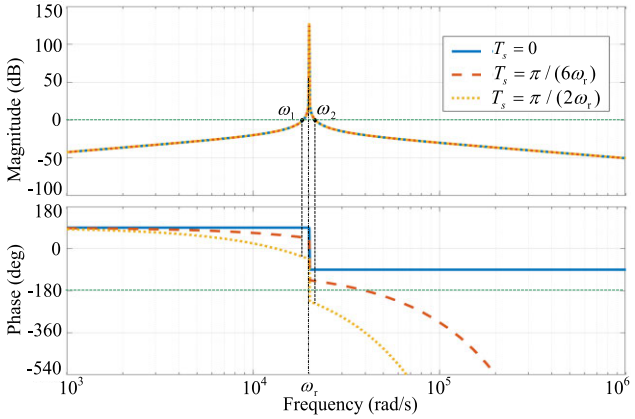

FIGURE 6. Bode diagrams of the inner-loop with different time delays.

TABLE 1. System parameters.

	Description	Parameters	Value
General Parameters	DC voltage	V_{dc}	750 V
	Stray capacitance	C_{PV}	150 nF
	AC grid voltage	e_{RMS}	380 V
	Fundamental frequency	f_1	50 Hz
	Switching frequency	f_{sw}	15 kHz
	Sampling frequency	f_s	30 kHz
	DC-link capacitance	C_{dc}	1670 μF
Filter Parameters	Inverter-side inductance	L_1	1.65 mH
	Grid-side inductance	L_2	1 mH
	LCCL capacitance	λC_f	3.3 μF
	LCCL capacitance	$(1-\lambda)C_f$	10 μF
	CM resonance frequency	f_{r1}	2.19 kHz

with magnitude (in decibels) and phase of $H_{i0}(s)$ given in (18) and (19) respectively.

$$20\lg\left|H_{i0}(s)\right|_{s=j\omega}\Big| = \begin{cases} 20\lg\left[k_{ip}\dfrac{3\lambda C_f\omega_r^2\omega}{\omega_r^2-\omega^2}\right], & (\omega<\omega_r) \\ \infty, & (\omega=\omega_r) \\ 20\lg\left[k_{ip}\dfrac{3\lambda C_f\omega_r^2\omega}{\omega^2-\omega_r^2}\right], & (\omega>\omega_r) \end{cases} \tag{18}$$

$$\angle H_{i0}(s)\big|_{s=j\omega} = \begin{cases} \dfrac{\pi}{2}-1.5\omega T_s, & (\omega<\omega_r) \\ -\dfrac{\pi}{2}-1.5\omega T_s, & (\omega>\omega_r) \end{cases} \tag{19}$$

The Bode diagrams of $H_{i0}(s)$ with different time delays are shown in Fig. 6 using the parameters listed in Table 1. According to the Nyquist stability criterion, only the frequency ranges with magnitudes above 0 dB are considered. According to (17), the number of the open-loop unstable poles P = 0. The numbers of the positive and negative crossings between ω_1 and ω_2 in Fig. 6 must be equal, to ensure the system stability. Fig. 6 shows that there is neither positive nor negative crossing between ω_1 and ω_2 when $T_s = 0$ or $T_s = \pi/(6\omega_r)$. In this case, the system is stable. However, when $T_s = \pi/(2\omega_r)$, there is one negative crossing and no positive crossing, showing an unstable system.

It can be derived from (19) that, the control period T_s should satisfy (20) for ensuring the system stability

$$-\frac{\pi}{2}-1.5\omega_2 T_s > -\pi \tag{20}$$

where ω_2 should satisfy a zero gain according to (18) ($\omega_2 > \omega_r$).

$$20\lg\left[k_{ip}\frac{3\lambda C_f\omega_r^2\omega_2}{\omega_2^2-\omega_r^2}\right] = 0 \tag{21}$$

Regarding the controller design, the proportional gain k_{ip} of inner loop can be designed as follows to guarantee the neutral-current inner-loop has enough phase margin ϕ_m [20]. According to (19), the right cut-off frequency ω_2 should guarantee an enough phase margin ϕ_m

$$-\frac{\pi}{2}-1.5\omega_2 T_s = \phi_m - \pi. \tag{22}$$

Then, substituting the ω_2 of (22) into (21), k_{ip} can thus be obtained as

$$k_{ip} = \frac{\left(\frac{\pi-2\phi_m}{3T_s}\right)^2-\omega_r^2}{3\lambda C_f\omega_r^2\frac{\pi-2\phi_m}{3T_s}}. \tag{23}$$

To further demonstrate the damping effect of the inner-loop, its closed-loop transfer function can be derived as

$$\Phi_{i0}(s) = \frac{i_0(s)}{i_0^*(s)} = \frac{H_{i0}(s)}{1+H_{i0}(s)} \tag{24}$$

Its magnitude response can be plotted together with the magnitude response without the active damping using the parameters listed in Table 1, as shown in Fig. 7. It should be noted that, without the active damping, a serious resonance peak exists at the resonance frequency f_{r1}. In contrast, an obvious suppression to resonance peak can be observed with the proposed neutral-current inner-loop, validating the damping effect.

2) DESIGN DETAILS FOR OUTER-LOOP CONTROLLER

The target of the outer-loop is to eliminate the voltage difference. On the one hand, the controller parameters should be reasonably designed to guarantee the system stability. On the other hand, the steady-state error of the outer-loop should be suppressed to zero with the selected controller. Therefore, the proportional-integral (PI) controller is preferred in the outer-loop.

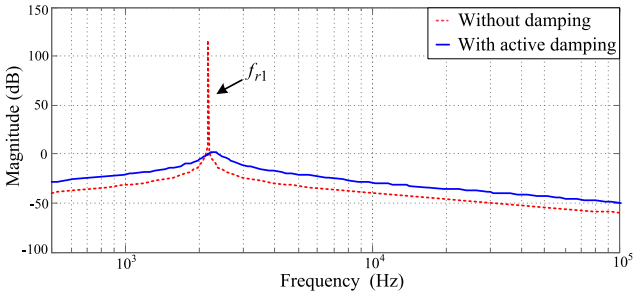

FIGURE 7. Magnitude responses with and without active damping.

According to Fig. 5, the open-loop transfer function of the outer-loop can be derived as (25) by multiplying the transfer functions of PI controller, inner-loop, and plant.

$$\begin{aligned} &H_{\Delta v}(s) \\ &= -R_{\Delta v}(s)\Phi_{i0}(s)G_{\Delta v}(s) \\ &= k_{vp}\frac{\tau_v s+1}{\tau_v s}\frac{K_I s}{1.5T_s s^3+s^2+\left(K_I+1.5T_s\omega_r^2\right)s+\omega_r^2}\frac{1}{C_{dc}s} \\ &= \frac{K_V\left(\tau_v s+1\right)}{s[1.5T_s s^3+s^2+\left(K_I+1.5T_s\omega_r^2\right)s+\omega_r^2]} \end{aligned} \tag{25}$$

where k_{vp} and τ_v are parameters of PI controller; time delay $e^{-1.5\,Tss}$ has been approximated to a one-order inertia element for a convenient calculation; K_I and K_V can be respectively expressed as

$$K_I = 3k_{ip}\lambda C_f\omega_r^2 \tag{26}$$

$$K_V = \frac{k_{vp}K_I}{\tau_v C_{dc}} \tag{27}$$

Its magnitude response and phase response can be deduced as (28) and (29) respectively.

$$\begin{aligned} &\left|H_{\Delta v}(s)\right|_{s=j\omega}\left| \right. \\ &= \frac{K_V\sqrt{1+\omega^2\tau_v^2}}{\omega\sqrt{\left(\omega_r^2-\omega^2\right)^2+\left(K_I\omega+1.5T_s\omega_r^2\omega-1.5T_s\omega^3\right)^2}} \end{aligned} \tag{28}$$

$$\begin{aligned} &\angle H_{\Delta v}(s)\left|_{s=j\omega}\right. \\ &= \tan^{-1}(\tau_v\omega)-\frac{\pi}{2}-\tan^{-1}(\frac{K_I\omega+1.5T_s\omega_r^2\omega-1.5T_s\omega^3}{\omega_r^2-\omega^2}) \end{aligned} \tag{29}$$

The Bode diagrams of $H_{\Delta v}(s)$ with different proportional gain k_{vp} are shown in Fig. 8 using the parameters listed in Table 1. It can be inferred that the magnitude response curve will shift upwards with the increase of k_{vp}, which will weaken the phase margin and even cause system instability. And the controller parameters k_{vp} and τ_v can also be tuned according to the given phase margin, which is similar to the foregoing design process in the neutral-current inner-loop and not repeated.

The zero steady-state errors of the outer-loop should also be theoretically verified. The transfer function between the error signal and the reference signal of the outer-loop can be

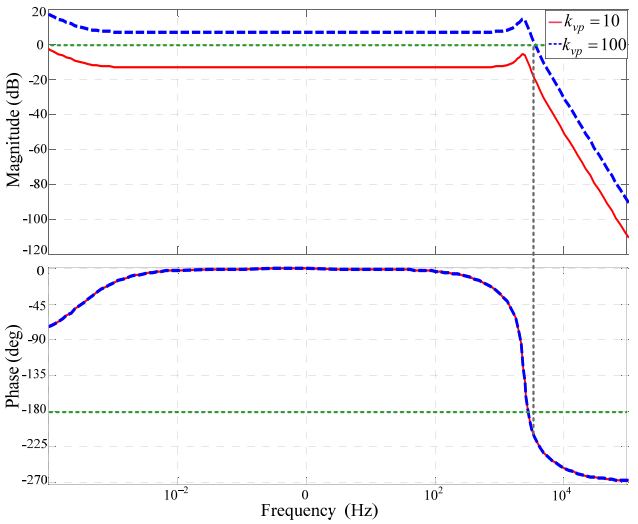

FIGURE 8. BODE diagrams of the outer-loop with two proportional gains.

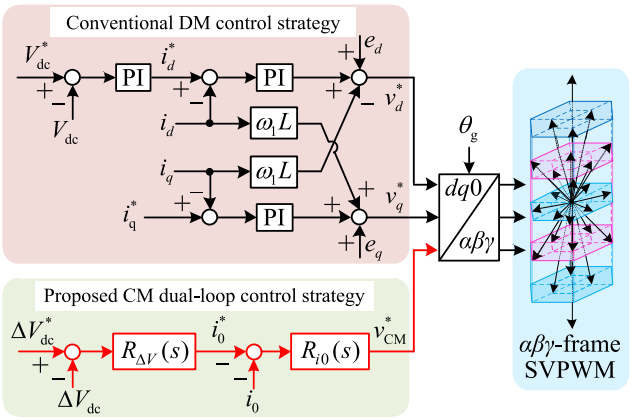

FIGURE 9. Overall control scheme with the proposed strategy.

expressed as

$$\begin{aligned} &\frac{E(s)}{\Delta V_{dc}^*(s)} \\ &= \frac{1}{1+H_{\Delta v}(s)} \\ &= \frac{1.5T_s s^3+s^2+\left(K_I+1.5T_s\omega_r^2\right)s+\omega_r^2}{1.5T_s s^3+s^2+\left(K_I+1.5T_s\omega_r^2\right)s+\omega_r^2+\frac{K_V(\tau_v s+1)}{s}} \end{aligned} \tag{30}$$

With the unit-step reference signal, the steady-state error of the outer-loop can thus be calculated as (31), which is the expected zero value.

$$\begin{aligned} &e_{ss} \\ &= \lim_{t\to\infty}e(t)=\lim_{s\to 0}sE_s(s) \\ &= \frac{1.5T_s s^3+s^2+\left(K_I+1.5T_s\omega_r^2\right)s+\omega_r^2}{1.5T_s s^3+s^2+\left(K_I+1.5T_s\omega_r^2\right)s+\omega_r^2+\frac{K_V(\tau_v s+1)}{s}}\Delta V_{dc}^* \\ &= 0 \end{aligned} \tag{31}$$

D. CONTROL SCHEME OF OVERALL SYSTEM

The proposed cascaded dual-loop CM control strategy are then combined with the commonly-used DM control

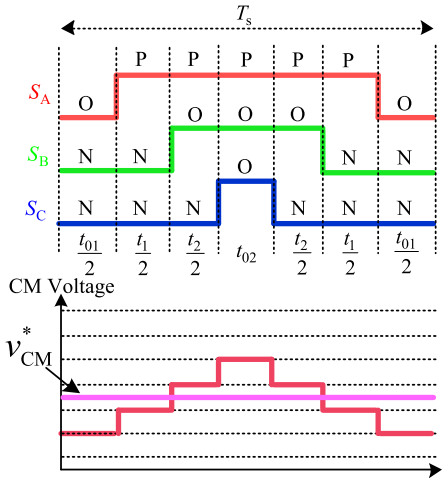

FIGURE 10. Switching states, dwell time and CM voltage in a switching period.

TABLE 2. Three experimental cases.

Number	Control Strategy Description	Filter
Case 1	Only using conventional DM control strategy	LCL
Case 2	Only using conventional DM control strategy	LCCL
Case 3	Conventional DM control strategy with proposed CM dual-loop control strategy (Fig. 9)	LCCL

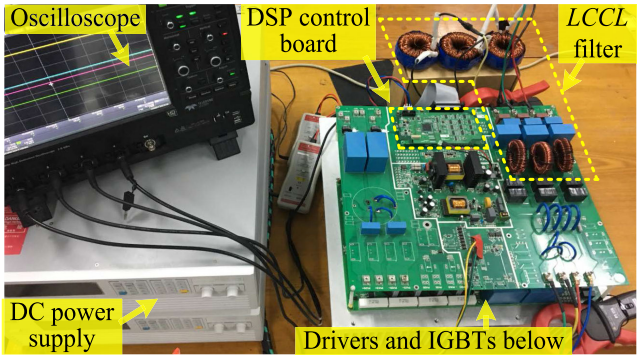

FIGURE 11. 10 kW transfromerless LCCL-filtered T-type three-level PV inverter.

strategy [21], [22] to form the overall system control scheme, as shown in Fig. 9, where $L = L_1 + L_2$; i_d and i_q are dq components of the inverter-side currents in the grid-voltage-oriented synchronous frame; ω_1 is the fundamental angle frequency; θ_g is the angle of the grid voltage. It should be noted that, the DM active damping need not be added in the control scheme since the DM parameters of the paper lie in the stable range [15].

In order to output an arbitrary CM voltage, the $\alpha\beta\gamma$-frame SVPWM is adopted, where the γ-axis is set to modulate the reference CM voltage v^*_{CM}. Different from the conventional $\alpha\beta$-frame SVPWM, the $\alpha\beta\gamma$-frame SVPWM can regulate the CM voltage by reallocating the dwell time of redundant vectors [23], [24]. With the example in Fig. 10, the dwell time

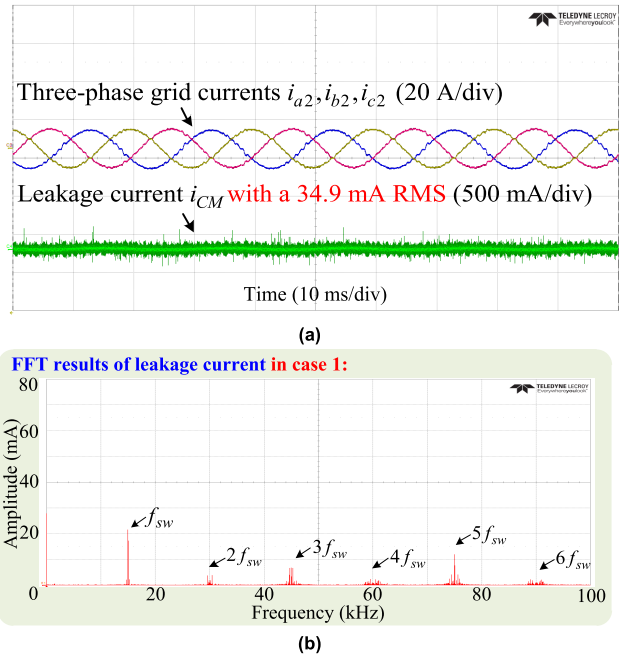

FIGURE 12. (a) Three-phase grid-currents and leakage current, (b) FFT results of leakage current in case 1.

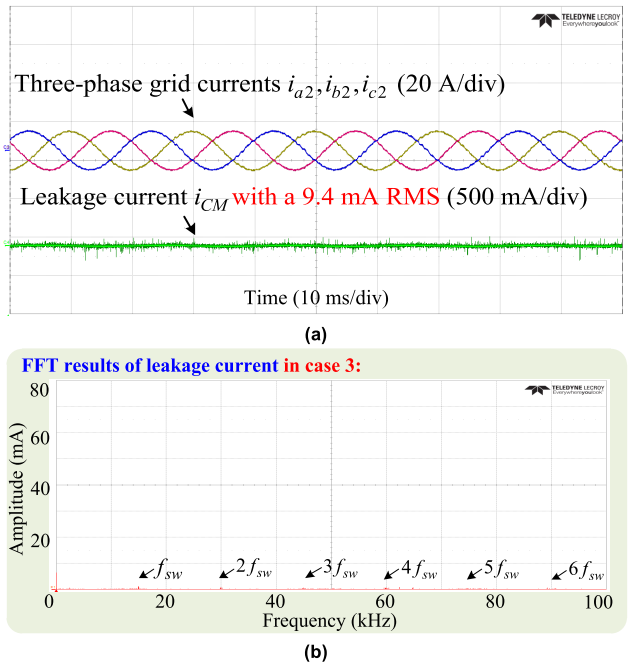

FIGURE 13. (a) Three-phase grid-currents and leakage current, (b) FFT results of leakage current in case 3.

of redundant vectors can be expressed as t_{01} and t_{02}, whose values can be calculated according to (32)

$$\begin{cases} V^*_{CM} = (-\frac{1}{3}V_{dc}t_{01} - \frac{1}{6}V_{dc}t_1 + 0 + \frac{1}{6}V_{dc}t_{02})/T_s \\ t_{01} + t_{02} = t_0 \end{cases} \quad (32)$$

where T_s is the switching period and t_0 is the total dwell time of the two redundant vectors.

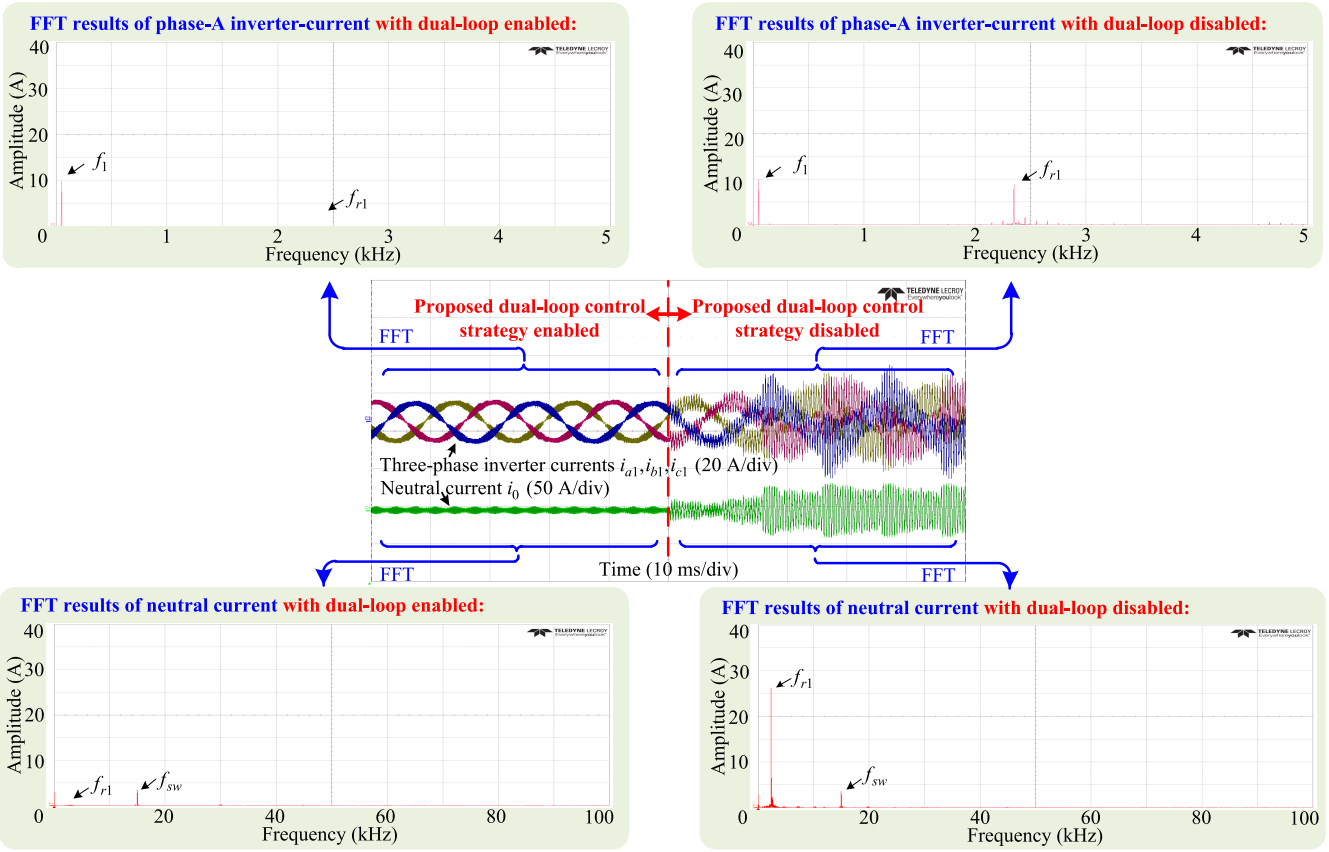

FIGURE 14. Three-phase inverter-currents, neutral current and corresponding FFT results with the proposed dual-loop control enabled and disabled.

IV. EXPERIMENTAL VERIFICATION

In this paper, a 10 kW LCCL-filtered three-level inverter has been built as shown in Fig. 11. The T-type integrated power module 10-FZ12NMA040SH from Vincotech is employed. The DSP TMS320F28377D from Texas Instruments (TI) is used to implement the control and modulation scheme. The Chroma programmable dc power supply 62050H-600S is used to support the dc voltage. Parameters of the experimental system are given in Table 1. And total three cases are organized in the prototype, as tabulated in Table 2.

A. VALIDATION OF LEAKAGE CURRENT REDUCTION

First of all, leakage current in the case 1 can be compared with that in the case 3. As shown in Fig. 12, when the prototype is implemented in the case 1, the leakage current has a RMS value of 34.9 mA and obviously includes massive high-frequency components around the switching frequency (f_{sw}) and its multiples.

But when the prototype operates in the case 3, the RMS of the leakage current can be reduced to 9.4 mA and high-frequency components in the leakage current can also be effectively eliminated, as shown in Fig. 13. The leakage current reduction with proposed CM dual-loop control strategy and LCCL filter is thus verified.

B. VALIDATION OF CM RESONANCE SUPPRESSION

In order to verify the CM resonance suppression of proposed dual-loop control strategy, the experiments with proposed dual-loop strategy enabled (case 3) and disabled (case 2) are carried out in the LCCL-filtered inverter. The waveforms at the switching moment are captured as shown in Fig. 14 and 15. As seen from Fig. 14, when the proposed dual-loop strategy is employed, there are no resonance components in the inverter-currents and neutral current. However, when the proposed strategy is disabled, significant resonance components immediately appear in inverter-currents and neutral current. Similarly, no resonance emerges in the grid-currents and leakage current with the proposed dual-loop strategy enabled, as shown in Fig. 15. But the grid-currents and leakage current immediately suffer from the CM resonance with the proposed dual-loop strategy disabled.

C. VALIDATION OF DC VOLTAGE-DIFFERENCE OUTER-LOOP

In order to verify the necessity and effectiveness of the dc voltage-difference outer-loop, this paper carries out two experiments. The first experiment alters the strategy from the dual-loop control to the inner-loop control, as shown in Fig. 16. When the outer-loop is enabled, i.e., i_0^* equals the output of the outer-loop regulator, $\Delta V_{\rm dc}$ steadily fluctuates

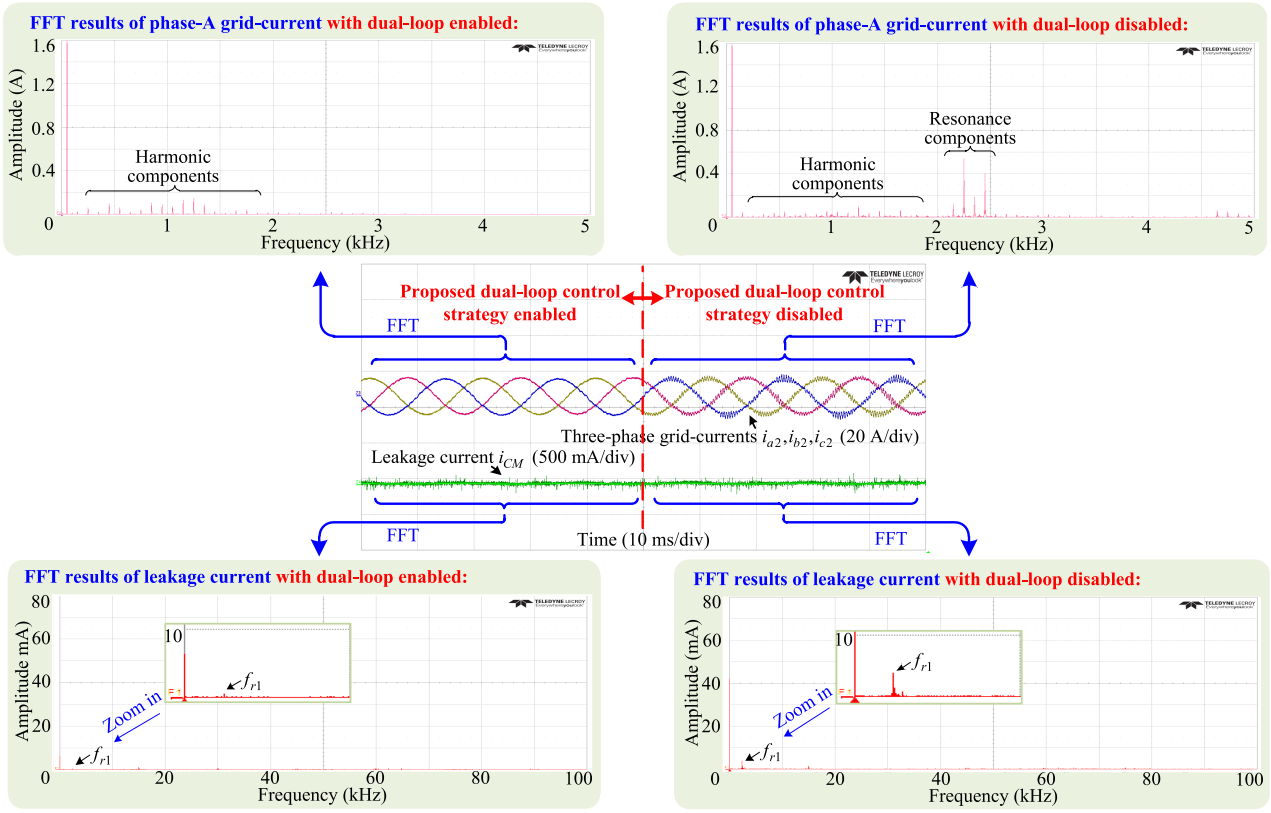

FIGURE 15. Three-phase grid-currents, leakage current and corresponding FFT results with the proposed dual-loop control enabled and disabled.

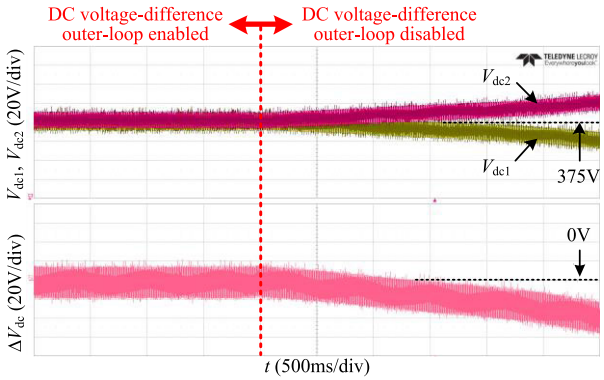

FIGURE 16. Positive and negative dc voltage, and dc voltage-difference with the outer-loop disabled and enabled.

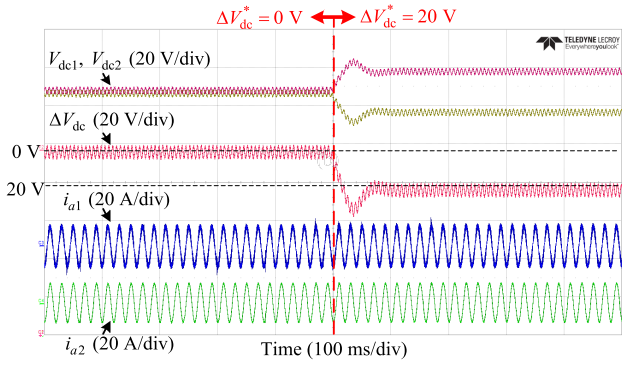

FIGURE 17. Positive and negative dc voltage, dc voltage-difference, phase-A inverter-current, phase-A grid-current with the reference of the outer-loop changed.

around 0V and only contains high frequency components caused by the switching of power devices [25]. Opposite, when the outer-loop is disabled, i.e., i_0^* is set to be zero, the positive and negative dc voltages gradually deviate from each other and their difference ΔV_{dc} begins to increase. The results indicate that the CM active damping control (i.e., the inner-loop) with a zero reference may interfere with the NP voltage control.

The second experiment alters the reference of the dc voltage-difference outer-loop from 0 V to 20V, as shown in Fig. 17. When the reference of outer-loop changes from 0 V to 20 V, the dc voltage-difference undoubtedly reaches 20 V after a dynamic process. Simultaneously, the inverter-currents and grid-currents can keep operating normally. The second experiment thus verifies the effectiveness of the dc voltage-difference outer-loop.

D. VALIDATION OF DISTURBANCE REJECTION

In order to verify the disturbance rejection of the proposed dual-loop control strategy, some disturbances including changing the active and reactive current references are added in the LCCL-filtered inverter with the proposed dual-loop control strategy (case 3).

The first experiment changes the reference of active current i_d* from 10 A to 5 A, and then to 10 A again, as shown in

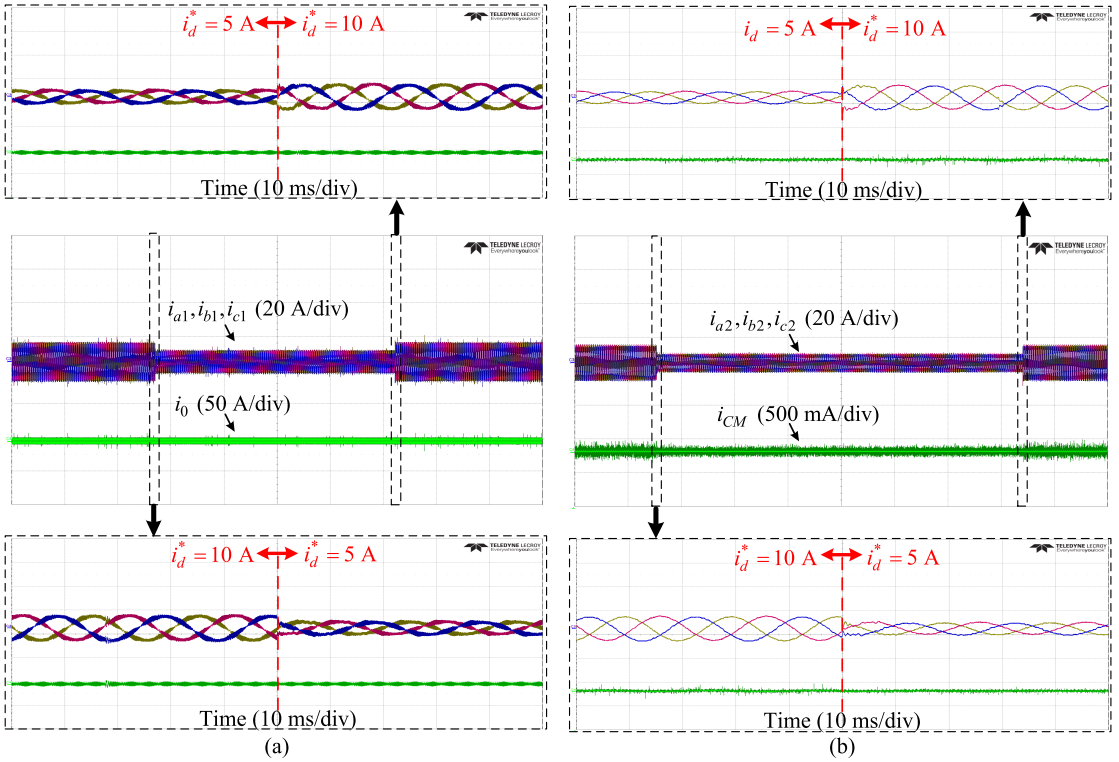

FIGURE 18. (a) Three-phase inverter-currents and neutral current, (b) three-phase grid-currents and leakage current when the active current reference i_d^* changes from 10 A to 5 A, then to 10 A again.

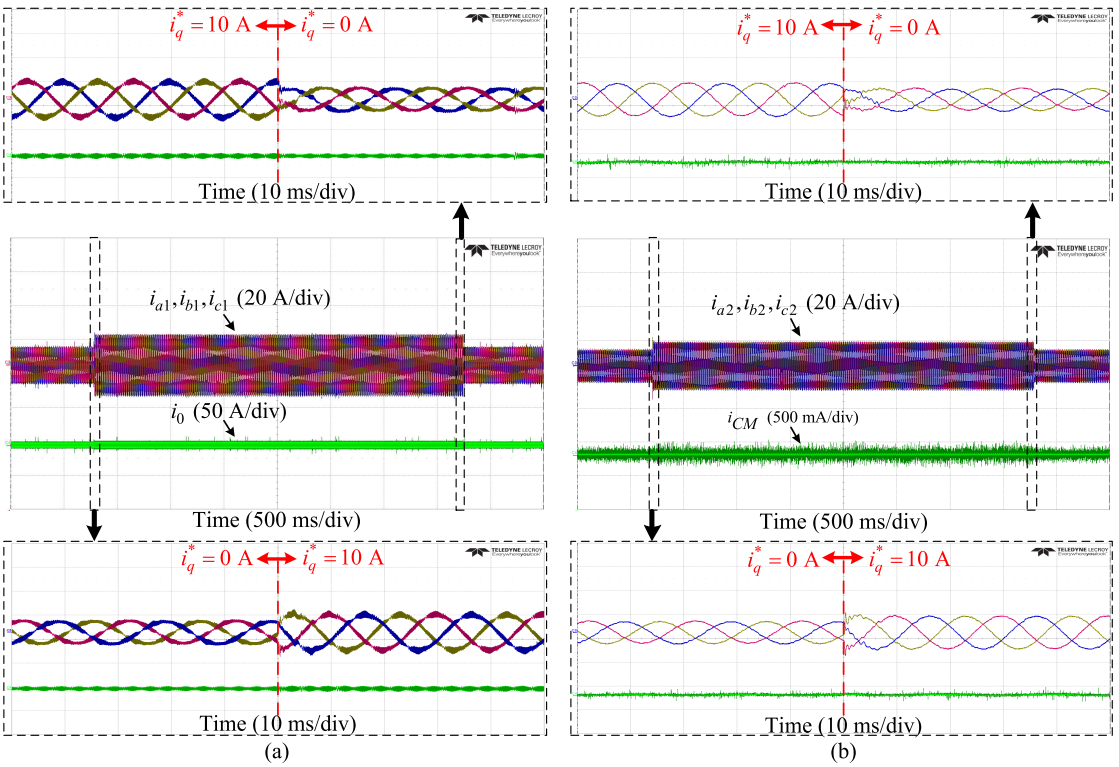

FIGURE 19. (a) Three-phase inverter-currents and neutral current, (b) three-phase grid-currents and leakage current when the reactive current reference i_q^* changes from 0 A to 10 A, then to 0 A again.

Fig. 18. And the second experiments changes the reference of reactive current i_q* from 0 A to 10 A, and then to 0 A again, as shown in Fig. 19.

It can be seen from Fig. 18 (a) and 19 (a) that there is no resonance problem emerging in the three-phase inverter-currents and the neutral current when the active or

reactive current references change. Similarly, the three-phase grid-currents and the leakage current can continue normal operation when the active or reactive current references change, as shown in Fig. 18 (b) and 19 (b).

V. CONCLUSION

The CM resonance and the NP voltage imbalance in the LCCL-filtered three-level inverter were investigated in the paper based on a derived CM model of the inverter. A CM resonance damping strategy based on a neutral-current loop was proposed. However, if the reference of the neutral current loop was set to be zero, the difference of the positive and negative dc voltages would increase gradually, leading to the NP voltage imbalance. In order to balance the NP voltage, the commonly-used method is to add an independent voltage-difference loop. However, the independent loop may be interfered by the neutral-current loop. Therefore, this paper proposed a cascaded dual-loop control strategy to avoid the interference, where the reference of the neutral-current loop was given by the output of the outer-loop regulator. The proposed strategy was proven experimentally to be effective for both damping the CM resonance and balancing the NP voltage.

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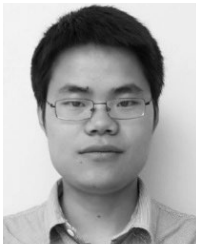

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