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A Bridgeless Buck-flyback PFC Converter with High PF and Dead Angles Eliminated

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***Abstract*-- The inherent dead angles of the input line current in buck power factor correction (PFC) converter deteriorate the power factor (PF) and commonly extra switches with high control complexity are required to eliminate these dead angles. Alternatively, this paper proposed a topological solution using a simple single voltage loop control. The proposed switch integrated bridgeless buck-flyback PFC converter operates in buck-flyback mode and can automatically change to flyback mode when the dead angles occur. Bridgeless operation modes of the proposed converter are achieved by dual converter cells and the corresponding PF expression is derived. Besides, the inductors and transformers ratio is analyzed to ensure the high PF (>0.99) and the satisfactory input current harmonics (meet the IEC 61000-3-2 Class D limits) in the 100~240 Vac input voltage range. The 100 W prototypes of the conventional buck and the proposed converters are built for experimental tests, which confirm the effectiveness of the proposed topology.**

***Index Terms*—dead angles eliminated, switches integrated, bridgeless Buck-flyback, high PF.**

I. INTRODUCTION

Compared to commonly employed boost power factor correction (PFC) converter, buck PFC converter has advantages of lower voltage stress across switch and higher efficiency at low line voltage, which is suitable for low power applications, such as laptop adaptors and low power AC power supply units [1], [2]. However, the inherent dead angles of the input line current have limited its applications, as there is no input line current flowing through the converter during these dead angles. Inevitably, this phenomenon deteriorates the power factor (PF) and increases the total harmonic distortions of the input line current (THD*i*). Consequently, to meet the IEC61000-3-2 requirement, the buck PFC converter with careful design has to limit its output voltage (e.g., set 80 Vdc output in the 100~240 Vac input voltage range) to minimize these dead angles [2]. Nonetheless, even though the buck PFC converter with limited output voltage can satisfy required PF and THD*i* to some extent, higher current conduction losses for a given power load and larger capacitors for a given hold-up time requirement are still problems to handle with in the design process [3], [4].

To tackle these dead angle issues, a variable on-time control is proposed to maximize the output voltage, but the dead angles still exist [3]. Others integrate buck-boost (or flyback, an isolated version of buck-boost) and buck topologies to obtain double switches-based buck PFC converter, which will switch to buck-boost or flyback mode before the dead angles occurrence. Although the dead angles are eliminated, these solutions impose an additional required switch and the control circuit complexity [4]-[7]. For example, input-parallel-output-parallel buck-flyback converters are proposed in [6], as shown in Fig. 1(a), which mainly operate in buck mode and switched into flyback mode once control circuit detects the upcoming dead angles. Notably, besides the additional circuits required, a boundary output voltage should be set to guarantee the smooth mode change [6].

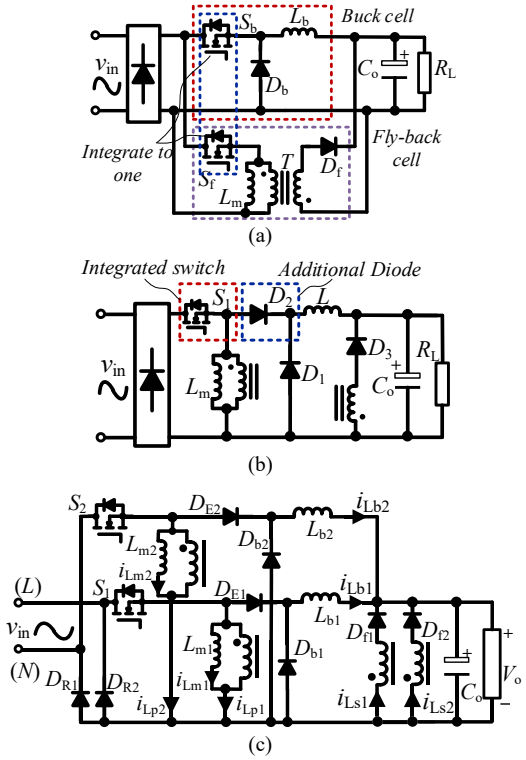


Fig. 1. The topology deriving process: (a) input-parallel-output-parallel buck-flyback PFC topology [6]; (b) switches integrated buck-flyback PFC topology; (c) the proposed switches integrated bridgeless buck-flyback PFC topology using dual buck and flyback cells.

In order to simplify the control circuit and eliminate the use of additional sensor, using switch integration method in [8], a switch integrated buck-flyback PFC converter is shown in Fig. 1(b). However, for this topology, although dead angles can be eliminated without extra control complexity, there is an additional diode in the current path and part of energy transferred to the load is through the flyback transformer, which will degrade the converter efficiency. On the other hand, bridgeless PFC converters

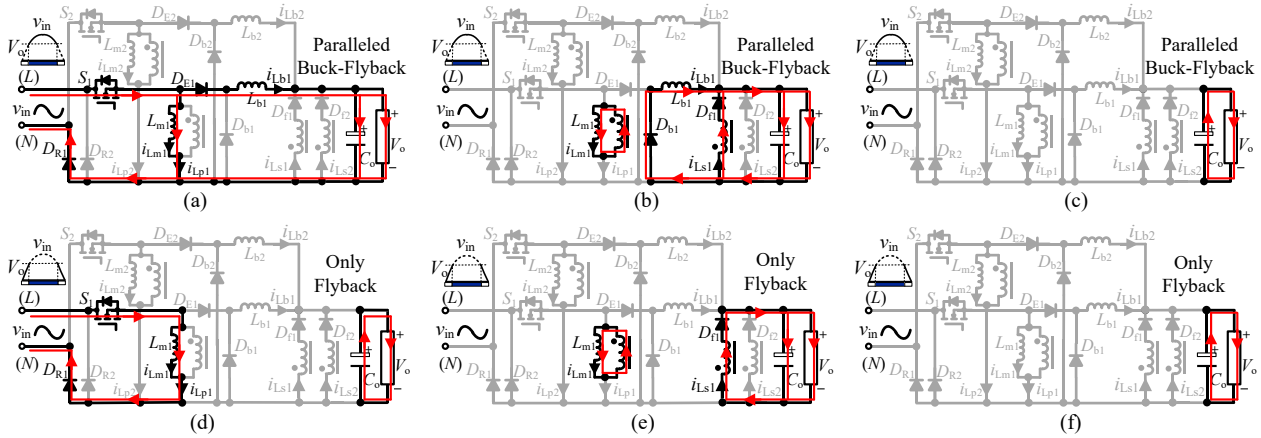


Fig. 2. Operation modes of the proposed converter in the positive input voltage. Buck and Flyback combination operation mode: when v_{in} > Vo, as shown in (a), (b), and (c). Flyback only operation mode: when v_{in} < Vo, as shown in (d), (e), and (f).

are becoming attractive due to their minimized conduction losses by eliminating the diode rectifier bridge [9], [10]. Among them, using the dual converter cells to obtain the bridgeless configurations is a popular solution and usually the obtained topologies possesses the merits of original PFC converters, e.g., dual buck, buck-boost, Cuk and Sepic [1], [9], [10].

Thus, to obtain a reasonable efficiency, the topology in Fig. 1(b) is further modified to the bridgeless buck-flyback converter, as shown in Fig. 1(c). Although the component count is doubled, the proposed bridgeless buck-flyback topology still inherits the merits of the topology in Fig. 1(b). It can adopt conventional simple control without sensing the line voltage and can eliminate dead angles by an automatic change from buck-flyback to flyback mode. Besides, theoretically the proposed converter does not have to limit its output voltage below 80V to meet the IEC 61000-3-2 requirement, which is an advantage when there is a hold-up time requirement. Moreover, the minimized conduction losses can maintain the efficiency of the proposed converter at a reasonable level compared with the conventional buck PFC converter.

This paper is organized as follows. Section II will introduce operation modes, derive the PF expression, and provides the inductor and transformer sizing to ensure that PF > 0.99 and the input current harmonics meet the IEC 61000-3-2 Class D limits in the 100~240 Vac input voltage range. Furthermore, discontinuous conduction mode (DCM) operation of the converter in order to nullify the reverse recovery losses of diodes while employ a single voltage loop control including guidelines on components selection are explained. Section III will demonstrate the experimental results of the proposed and the conventional buck PFC converters to verify the merits of the proposed converter. Finally, Section IV summarizes this study.

II. Analysis of The Proposed Converter

Fig. 1(c) has shown the proposed switch-integrated bridgeless buck-flyback PFC converter. Note that buck inductors L_{b1}, L_{b2}, and diodes D_{b1}, D_{b2} are from buck cells; magnetizing inductors L_{m1}, L_{m2}, and diodes D_{f1}, D_{f2}, are from flyback cells; switches S_1, S_2, are the commonly used components; D_{E1} and D_{E2} are the required extra diodes. In the positive half line cycle, L_{b1}, D_{b1}, L_{m1}, D_{f1}, D_{E1}, and S_1 operate to transfer the energy and in the negative half line cycle, L_{b2}, D_{b2}, L_{m2}, D_{f2}, D_{E2}, and S_2 operate. In this way, the traditional rectifier bridge can be cancelled and the conduction losses are spared.

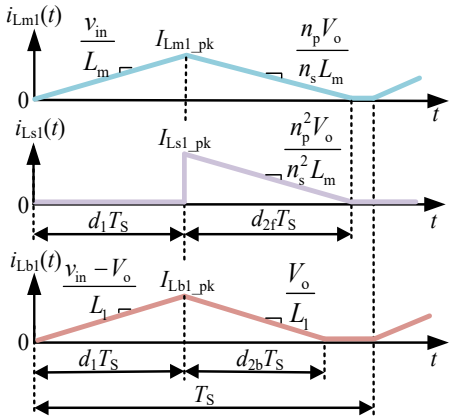
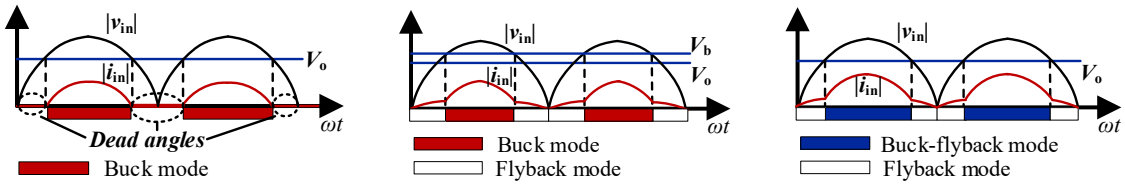


Fig. 3. Waveforms of the magnetizing inductor current i_{Lm1}, secondary winding current i_{Ls1}, and the buck cell inductor current i_{Lb1}. n_p and n_s the primary and secondary winding turns of transformer.

Assumptions are given as: (i) All the components are ideal. (ii) Switching frequency f_{SW} is much higher than the line frequency f_L and the input line voltage v_{in} can be seen as constant within one switching cycle T_S. (iii) Capacitor C_o is large enough so that output voltage V_o can be seen as constant in one switching cycle. (iv) v_{in} is ideal input line voltage with V_M as its peak value and V_{in} as the RMS value.

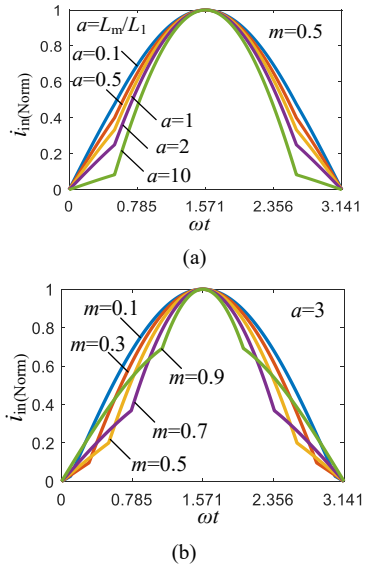
A. Operation modes

Due to the similar operation modes in the positive and negative half line cycle, this paper only gives analysis in the positive half line cycle. Fig. 2 gives the operation modes of the proposed converter and Fig. 3 shows the magnetizing inductor current i_{Lm1}, the secondary winding current i_{Ls1}, and the buck cell inductor current i_{Lb1} waveforms. There are two types of operation modes, buck-flyback combination operation mode and flyback only operation mode.



(a) (b) (c)

Fig. 4. Input voltage and current waveforms of converters: (a) conventional buck PFC converter with dead angles [2], (b) double switches-based buck PFC converter with requirement of detecting the boundary voltage V_b to switch between buck and flyback modes [4], [5], [7], (c) the proposed converter with two operation modes.



(a)

(b)

Fig. 5. Based on (3), the normalized input line current with (a) a as variable, and (b) m as variable.

For buck-flyback combination operation mode, as shown in Fig. 2(a), (b), (c), when $v_{in} > V_o$, both buck and flyback cells are in operation to transfer power.

In Fig. 2(a), when switch S_1 is turned on, for buck cell, the input line current i_{in} flows through the switch S_1, diode D_{E1}, and rectifier diode D_{R1} to charge L_{b1} and feed the load. For flyback cell, i_{in} flow through S_1 and D_{R1} to charge the magnetizing inductor L_{m1} of the transformer. During this on-time switching period, both the buck inductor current i_{Lb1} and magnetizing current i_{Lm1} increase linearly.

In Fig. 2(b), when S_1 is turned off, i_{Lb1} flow through D_{b1} to charge load, and the stored energy in the magnetizing inductor L_m is discharged to the load through the ideal transformer and diode D_{f1}. During this period, both i_{Lb1} and i_{Lm1} decrease linearly.

In Fig. 2(c), both current i_{Lb1} and i_{Lm1} have become zero, and only the output capacitor C_o feeds the load.

For flyback only operation mode, as shown in Fig. 2(d), (e), (f), when $v_{in} < V_o$, no current flows through the buck cell, same as in the conventional buck PFC converter. However, the flyback cell continues to work so that the dead angles of the input line current can be eliminated, as there is still current flowing through the flyback cell.

In Fig. 2(d), when S_1 is turned on, i_{in} flows through L_{m1} and D_{R1}, meanwhile, C_o feeds the load. During the on time switching period, the magnetizing current i_{Lm1} increases linearly.

In Fig. 2(e), the energy stored in L_{m1} is discharged to load through transformer and diode D_{f1}. During this period, i_{Lm1} reduces linearly.

In Fig. 2(f), i_{Lm1} has become zero and only the output capacitor C_o feeds the load.

B. PF and input current harmonics

Fig. 4 shows the different type converters' input line current waveforms. Seen from Fig. 4, the proposed converter has the paralleled buck and flyback cells both working in the whole line cycle and when the dead angles come, the buck cell itself stops the operation. Then there is still flyback cell maintaining the input current. Hence, the input line current i_{in} is the sum of the input currents i_{in_b} and i_{in_fly} from buck and flyback cells, expressed as:

$$i_{in}(t) = i_{S1\_ave}(t) = i_{in\_b}(t) + i_{in\_fly}(t) \tag{1}$$

For buck and flyback cells, i_{in_b} and i_{in_fly} have been given in [11] and [12]. Thus, (1) can be re-written as

$$i_{in}(t) = \begin{cases} \dfrac{V_M d_1^2}{2L_{m1} f_{SW}} \left(\dfrac{L_{m1}}{L_{b1}} |\sin \omega t| - \dfrac{V_o L_{m1}}{V_M L_{b1}} + |\sin \omega t| \right) & t \in [\dfrac{\theta}{\omega}, \dfrac{\pi - \theta}{\omega}] \\ \dfrac{V_M d_1^2 |\sin \omega t|}{2L_{m1} f_{SW}} & t \in [0, \dfrac{\theta}{\omega}) \cup (\dfrac{\pi}{\omega}, \dfrac{\pi}{\omega}] \end{cases} \tag{2}$$

where ω is the line angular frequency, d_1 is the duty cycle of switch S_1, and θ is equal to $\sin^{-1}(V_o/V_M)$.

Seen from (2), i_{in} relates to the ratio of L_{m1}/L_{b1} and V_o/V_M. Hence, let $L_{m1}/L_{b1} = a$ and $V_o/V_M = m$. (2) can be normalized as①:

$$i_{in(Norm)}(t) = \begin{cases} \dfrac{\alpha |\sin \omega t| - \alpha m + |\sin \omega t|}{a - \alpha m + 1} & t \in [\dfrac{\theta}{\omega}, \dfrac{\pi - \theta}{\omega}] \\ \dfrac{|\sin \omega t|}{a - \alpha m + 1} & t \in [0, \dfrac{\theta}{\omega}) \cup (\dfrac{\pi}{\omega}, \dfrac{\pi}{\omega}] \end{cases} \tag{3}$$

Based on (3), Fig. 5 is obtained. Seen from Fig. 5(a), when m is constant, by setting smaller a, the line current becomes more close to sinusoidal. On the other hand, when a is constant, the smaller m leads to more sinusoidal line current. In a half line cycle, the duty cycle d_1 can be considered as a time-invariant value if the converter uses a single voltage loop control, also referred as constant duty cycle control in [13]. Then the average input power P_{in_b} of buck and P_{in_f} of flyback cells can be derived as:

①-The normalized equation can be obtained by:

$$f(t)_{Norm} = \frac{f(t) - f(t)_{min}}{f(t)_{max} - f(t)_{min}}$$

Note that 'am' is added in (3) in both numerator and denominator on the purpose of finding out the impact of 'm' on $i_{in(norm)}$.

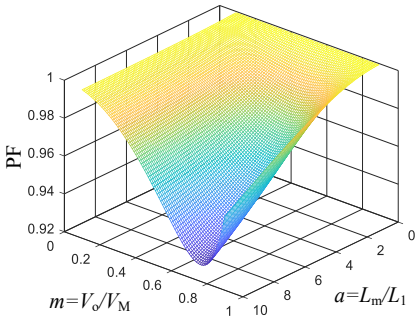


Fig. 6. Based on (6), PF surface with m and a as variables. When $a \in (0, 1.5]$, then PF>0.99 in a wide input voltage range is guaranteed.

$$P_{\text{in\_b}} = \frac{V_{\text{M}}^2 d_1^2}{4L_{\text{b1}} f_{\text{SW}}}[1 - \frac{2}{\pi}\sin^{-1}(\frac{V_{\text{o}}}{V_{\text{M}}}) - \frac{2V_{\text{o}}\sqrt{V_{\text{M}}^2 - V_{\text{o}}^2}}{\pi V_{\text{M}}^2}] \quad (4)$$

$$P_{\text{in\_f}} = \frac{V_{\text{M}}^2 d_1^2}{4L_{\text{m}} f_{\text{SW}}} \quad (5)$$

The average input power P_{in} is the sum of $P_{\text{in\_b}}$ and $P_{\text{in\_f}}$. Then, PF is derived as:

$$\text{PF} = \frac{\sqrt{\frac{\pi}{2}}[1 + a - \frac{2}{\pi}a\theta - \frac{2}{\pi}am\sqrt{1-m^2}]}{\sqrt{\theta - m\sqrt{1-m^2} + \int_{\theta}^{\pi-\theta}[a\,|\sin\omega t| - am + |\sin\omega t|]^2 d(\omega t)}} \quad (6)$$

Based on (6), Fig. 6 gives the PF surface with m and a as variables. Seen from Fig. 6, to ensure a high PF (> 0.99) in a wide input voltage range, which means that m changes widely, a should be in the range of (0, 1.5]. Furthermore, generally buck cell has better efficiency than flyback cell as there is no transformer in the buck cell. Hence, the ratio a should be chosen to ensure that buck cell processes more power than flyback cell. Assume β is the ratio between $P_{\text{in\_b}}$ and $P_{\text{in\_f}}$. Then, based on (4) and (5), it results in

$$\beta = \frac{P_{\text{in\_b}}}{P_{\text{in\_f}}} = a(1 - \frac{2}{\pi}\theta - \frac{2}{\pi}m\sqrt{1-m^2}). \quad (7)$$

Based on (7), Fig. 7 shows the power relationship between buck and flyback cells with a and m as variables. Seen from Fig. 7, when m is in a wide range, a should be as large as possible to allow buck cell process more power (β should be as large as possible). So in the range of (0, 1.5], a is determined to be 1.5.

In order to conduct the FFT analysis of the input current, firstly, i_{in} given in (2) needs to be simplified. Based on (4) and (5), assuming that the converter in this paper are all lossless systems (eff. η=1), then the constant duty cycle d_1 can be obtained from (4) and (5) as:

$$d_1 = \sqrt{\frac{4L_{\text{b1}} f_{\text{sw}} \pi P_{\text{in\_b}}}{\eta V_{\text{M}}^2(\pi - 2\sin^{-1} m - 2m\sqrt{1-m^2})}} \quad (8)$$

$$d_1 = \sqrt{\frac{4L_{\text{m1}} f_{\text{sw}} P_{\text{in\_f}}}{\eta V_{\text{M}}^2}} \quad (9)$$

where $P_{\text{in\_b}} = P_{\text{o}} \cdot \beta/(\beta+1)$ and $P_{\text{in\_f}} = P_{\text{o}}/(\beta+1)$. Substitute d_1 in (2) with (8) and (9), then it results in:

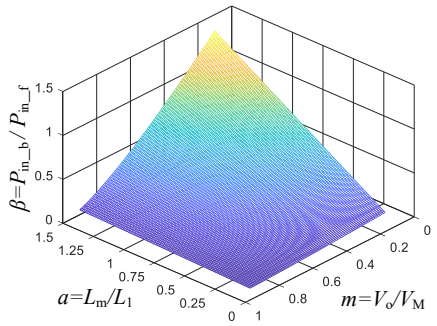


Fig. 7. Based on (7), power relationship between buck and flyback cells with a and m as variables. Seen from the curve, to get higher converter efficiency, a should be as large as possible.

$$i_{\text{in}}(t) = \begin{cases} \frac{2\pi P_{\text{in\_b}}(|\sin\omega t| - m)}{V_{\text{M}}(\pi - 2\sin^{-1} m - 2m\sqrt{1-m^2})} + \frac{2P_{\text{in\_f}}|\sin\omega t|}{V_{\text{M}}} & t \in [\frac{\theta}{\omega}, \frac{\pi-\theta}{\omega}] \\ \frac{2P_{\text{in\_f}}|\sin\omega t|}{V_{\text{M}}} & t \in [0, \frac{\theta}{\omega}) \cup (\frac{\pi}{\omega}] \end{cases} \quad (10)$$

Seen from (10) and (7), the input line current i_{in} of the proposed converter actually relates to V_{M}, m, P_{o}, and a (determined as 1.5). Similarly, the input current $i_{\text{in\_b}}$ of the conventional buck PFC converter can be obtained as:

$$i_{\text{in\_b}}(t) = \begin{cases} \frac{2\pi P_{\text{in\_b}}(|\sin\omega t| - m)}{V_{\text{M}}(\pi - 2\sin^{-1} m - 2m\sqrt{1-m^2})} & t \in [\frac{\theta}{\omega}, \frac{\pi-\theta}{\omega}] \\ 0 & t \in [0, \frac{\theta}{\omega}) \cup (\frac{\pi}{\omega}] \end{cases} \quad (11)$$

which involves to only V_{M}, m, and P_{o}.

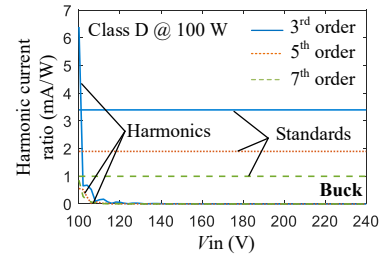
Therefore, based on (10) and (11), set P_{o} = 100 W, V_{o} = 80 V, and V_{M} = $\sqrt{2}$×(100~240) Vac, the input current harmonic spectrums of the proposed and the conventional converter can be obtained in Fig. 8 with the RMS input voltage V_{in} as variable.

Seen from Figs. 8(a) and 8(b), when V_{in} = 100 Vac, the 3rd order input current harmonics of the conventional buck PFC converter exceeds the corresponding 3rd order standard in the IEC 61000-3-2 Class D limits. In fact, the conventional buck PFC converter with a simple voltage loop control needs to further limit its input line current to pass the limit. Thus, according to (11), its P_{o} (= $P_{\text{in\_b}}$) or V_{o} (involves to m) need to be reduced. On the other hand, as shown in Figs. 8(c) and 8(d), the input current harmonics of the proposed converter has satisfied the limits with margins. Hence, compared to the conventional buck PFC converter, the proposed converter has better performances in terms of PF and the input current harmonics.

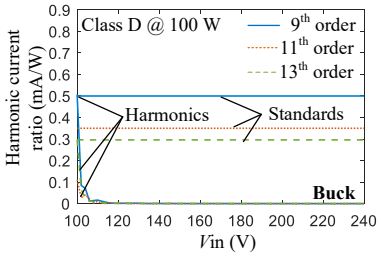
C. Component parameter determined

For the proposed converter operating in DCM, a simple voltage loop control is applied to regulate the output voltage and achieve the high PF. However, to ensure the DCM operation, the inductor limitation should be determined.

Referring to Fig. 3, the turning-off duty cycle $d_{2\text{b}}$ and $d_{2\text{f}}$ of buck and flyback cells can be expressed as:



(a)



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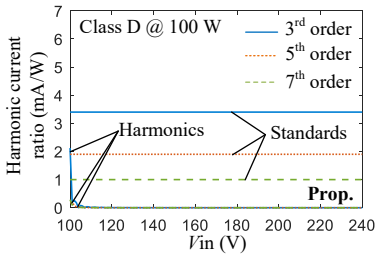
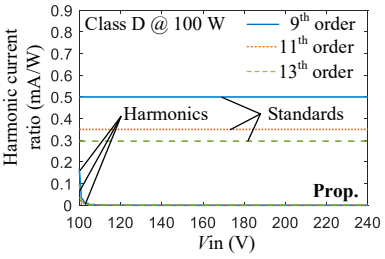


(c)



(d)

Fig. 8. Based on (10) and (11), the input current harmonic spectrums of the conventional buck and the proposed converters with V_o = 80 V, P_o = 100 W, and V_{in} as variable. (a) and (b) show the 3rd ~ 13th order input current harmonics of the buck converter; (c) and (d) show corresponding current harmonics of the proposed converter.

$$d_{2b} = \frac{d_1(V_M|\sin\omega t| - V_o)}{V_o} \tag{12}$$

$$d_{2f} = \frac{V_M|\sin\omega t| n_s d_1}{V_o n_p} \tag{13}$$

As converters operate in the DCM, $d_1+d_{2b} \le 1$ and $d_1+d_{2f} \le 1$, then there are:

$$\frac{V_o^2\eta(\pi - 2\sin^{-1}m - 2m\sqrt{1-m^2})}{4f_{sw}P_{in\_b}} \ge L_{b1} \tag{14}$$

$$\frac{V_M^2\eta}{4f_{sw}P_{in\_f}}\left(\frac{V_o n_p/n_s}{V_M + V_o n_p/n_s}\right)^2 \ge L_{m1} \tag{15}$$

Eq. (14) and (15) consider the limited inductance of each converter cell operating in DCM only, it should be further revised by considering $a = L_{M1}/L_{b1} = 1.5$ to ensure high PF. Moreover, the transformer turns ratio n_p/n_s in (15) can be determined by referring to [14], which has given the specific flyback design procedure. Basically, it uses the pre-set peak current limit and the maximum allowed turning-on duty cycle to derive the required parameters.

For the output capacitors, the capacitance is mainly determined by output ripple voltage and hold-up time requirements. In a steady operation, the output ripple voltage of a PFC converter is dominated by the second-order line frequency component, caused by the corresponding output ripple current. Thus, by assuming the second-order line frequency output current I_{o_rip} as:

$$I_{o\_rip} = I_o \sin(2\omega t + \varphi) \tag{16}$$

where φ is the angle difference between the grid. Then, the output ripple voltage ΔV_{o_rip} can be expressed as:

$$\begin{aligned}\Delta V_{o\_rip} &= \frac{1}{C_{o\_r}}\int_0^t I_o \sin(2\omega t + \varphi)d(t) \\ &= \frac{I_o\cos(\varphi) - I_o\cos(2\omega t + \varphi)}{2\omega C_{o\_r}}\end{aligned} \tag{17}$$

Based on (17), considering the worst case of ΔV_{o_rip}, then the required capacitance C_{o_r} is:

$$C_{o\_r} = \frac{P_o}{2\cdot\pi\cdot f_L\cdot V_o\cdot\Delta V_{o\_rip}} \tag{18}$$

where $P_o/V_o = I_o$ and $2\cdot\pi\cdot f_L = \omega$. Note that (18) is applicable to most PFC converters [14], [15]. However, for the PFC converters with high output voltage ripple requirement, (18) considers the worst scenario of output ripple may cause too much over design of capacitance selection. Specially, for the buck cell, P_o in (18) should be further revised as $P_o[1\text{-}2\sin^{-1}(m)/\pi]$, due to the dead angles.

The hold-up time t_{hold_up} actually involves the energy storage of the output capacitors. Accordingly, the minimum required capacitance C_{o_t} is:

$$C_{o\_t} = \frac{2P_o t_{hold\_up}}{V_o^2 - V_{o\_min}^2} \tag{19}$$

where V_{o_min} is the minimum output voltage. The final capacitance C_o should be the maximum value of C_{o_r} and C_{o_t}. In this paper, the hold-up time is not considered as the V_{o_min}, mainly depending on the lowest input voltage of the post DC-DC converter, is not specified here.

For semiconductors, empirically, the maximum peak or the average conduction currents determine the selection. Furthermore, a de-rated factor, e.g. 0.8 or 0.85, is used to guarantee the selected devices are capable to handle the conduction current. More delicately, others have used the power loss models of each devices in different topologies to find out the best cost-effective or the lowest power losses devices by design iterations [17]. However, it needs to build the components' database and the corresponding precise models to ensure the accurate results.

This paper only adopts the empirical way to determine the semiconductors, as the purpose of this paper is to offer a new topology solution for solving dead angles not yet to optimize it. The peak current expressions of main components switch S_1, rectifier diode D_{R1}, and diodes D_{b1}, D_{E1}, D_{f1} can be expressed as:

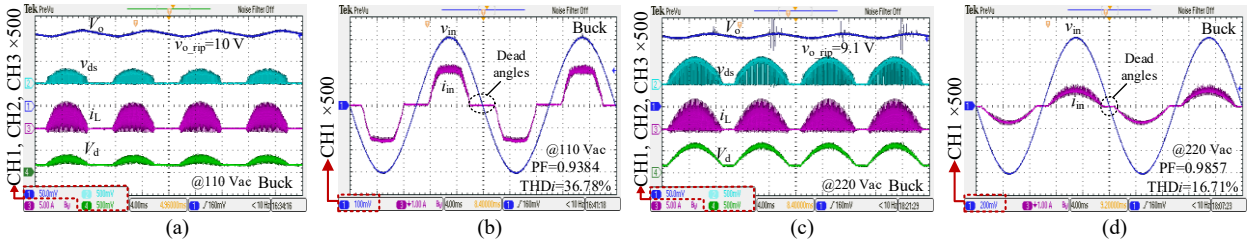


Fig. 9. The conventional buck PFC converter experimental waveforms with (a), (b) in 110 Vac and (c), (d) in 220 Vac input voltage. In (a) and (c), output voltage V_o [25 V/div], reversed voltage across switch v_{ds} [250 V/div], inductor current i_L [5 A/div], voltage across diode rectifier bridge V_d [250 V/div], and time [4 ms/div]. In (b) and (d), input voltage v_{in} [50 V/div], input current i_{in} [1 A/div] and time [4 ms/div].

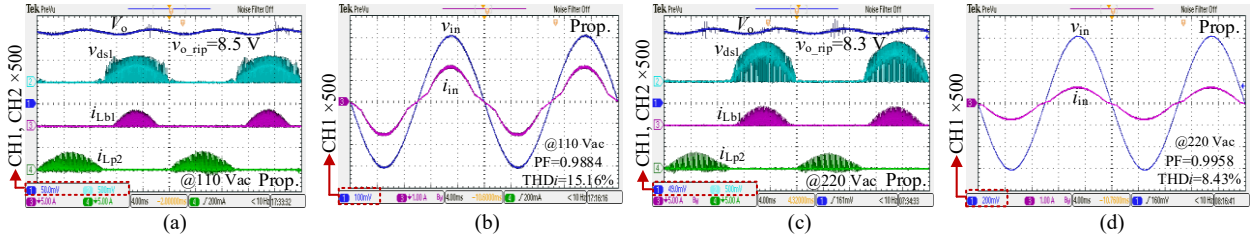


Fig. 10. The proposed bridgeless buck-flyback PFC converter experimental waveforms with (a), (b) in 110 Vac and (c), (d) in 220 Vac input voltage. In (a) and (c), output voltage V_o [25 V/div], reversed voltage across switch v_{ds1} [250 V/div], the buck cell inductor current i_{Lb1} [5 A/div], the flyback cell primary winding current in the transformer i_{Lp2} [5 A/div], and time [4 ms/div]. In (b) and (d), input voltage v_{in} [50 V/div], input current i_{in} [1 A/div] and time [4 ms/div].

$$I_{S1\_pk} = I_{DR1\_pk} = \left(\frac{V_M\left|\sin\omega t\right| - V_o}{L_{b1}} + \frac{V_M\left|\sin\omega t\right|}{L_{m1}}\right) d_1 T_S \quad (20)$$

$$I_{Db1\_pk} = I_{DE1\_pk} = I_{Lb1\_pk} = \frac{V_M\left|\sin\omega t\right| - V_o}{L_{b1}} d_1 T_S \quad (21)$$

$$I_{Df1\_pk} = I_{Ls1\_pk} = \frac{n_p^2 V_o}{n_s^2 L_{m1}} d_{2f} T_S \quad (22)$$

d_1 in (20) and (21) can be referred to (8) and d_{2f} referred to (13). Note that (20), (21), and (22) are only the peak current expressions in each switching cycle. The peak values in a half line cycle can be obtained when $|\sin\omega t|$=1.

III. Experimental Validations

For the proposed converter, using (14) and (15) with the specifications given in Table I, the limited L_m and L_b are obtained for DCM operation. Similarly, the DCM limited L is obtained for the conventional buck PFC converter. Considering margins, the final used L_m, L_b, and L are 0.9× calculated limited values to guarantee the DCM operations. Output capacitors and semiconductors are selected based on (18) and (20)~(22), respectively. Final devices are shown in the Table II. The conventional buck and the proposed buck-flyback prototypes with single voltage loop control are built for experimental validations. The control is implemented by DSP28335 and the switch driving IC chip is ADUM3223. Fig. 9 and Fig. 10 show the experimental waveforms of the conventional buck and the proposed bridgeless buck-flyback converters.

Seen from Figs. 10(a) and 10(c), in one line cycle, S_1, L_{m1}, and L_{b1} only operate in the half line cycle and in the complementary half line cycle, S_2, L_{m2}, and L_2 operate. These waveforms have proved that the proposed converter is operating under the 'dual bridgeless' configuration, as each converter cell operates in only positive or negative line cycle to avoid the use of diode rectifier bridge.

TABLE I
Key Parameters of Converters

Specifications	The proposed	Conv. buck
f_{SW}	50 kHz	50 kHz
f_L	50 Hz	50 Hz
V_{in}	100~240 Vac	100~240 Vac
V_o	80 Vdc	80 Vdc
P_o	100 W	100 W
d_{1max}	30%	30%
ΔV_{o_rip}	≤10 V	≤10 V
η	≈91%	≈93%
DCM Limited L	-	≤153 μH, cal.
DCM Limited Lm	≤390 μH, cal. by (15)	-
DCM Limited L_b	≤260 μH, cal. by (14)	-
a = Lm/L	1.5	-

TABLE II
Component Selections of Converters

Comp.	The proposed	*Comp.*	Conv. buck
L_{b1}, L_{b2} (0.9×limited L_b)	240 μH (Toroidal: CH571060)	L (0.9 × limited L)	138 μH (Toroidal: CH571060)
L_{m1}, L_{m2} (0.9×limited L_m)	360 μH (E core: B66366)	-	-
Turns ratio	41:31	-	-
D_{R1}, D_{R2}, D_{f1}, D_{62}	STTH12R06D	*Rectifier*	GBU8J
D_{E1}, D_{E2}, D_{b1}, D_{b2}	STTH5R06D	D	STTH5R06D
S_1, S_2	IXFH12N65X2	S	IXFH12N65X2
C_o	330 μF/100 V ×3	C_o	330 μF/100 V ×3

In Figs. 9(b) and 9(d), it is clear that the dead angles exist in the input line current of the conventional buck PFC converter. Consequently, the corresponding PF and THDi are 0.94 and 37% with 110 Vac input voltage, 0.99 and 17% with 220 Vac input voltage. By contrast, in Figs. 7(b) and 7(d), the proposed converter eliminates the dead angles and the corresponding PF and THDi are 0.99 and 15% with 110 Vac input voltage, 0.99 and 8% with 220 Vac input voltage. The performance improvements are obvious in terms of PF and THDi, especially in the low input line voltage. Besides, by comparing V_{o_rip} in Figs. 9 and 10, it can be seen that the proposed converter has relatively smaller output voltage ripple than the conventional buck PFC converter.

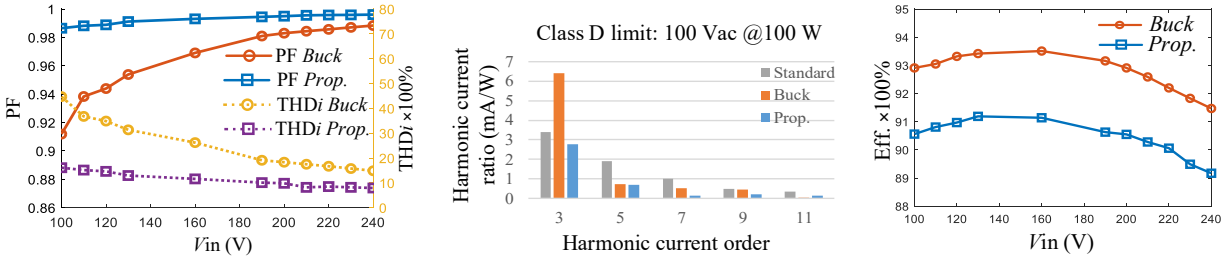


Fig. 11. Measured experimental data in the 100~240 Vac input voltage range, (a) PF and THD*i*, (b) harmonic current ratio, (c) efficiency (full load).

Furthermore, in the 100~240 Vac input voltage range, the measured experimental data are shown in the Fig. 11. Seen from Fig. 11(a), the PF of the proposed converter is near unity and the measured THD*i* is below 15%, better than the performances of the conventional buck PFC converter. Moreover, as shown in Fig. 11(b), the proposed converter can satisfy the IEC61000-3-2 Class D limits. By contrast, the conventional buck converter cannot meet the limits. These experimental results are in agreement with the corresponding input current harmonics analysis presented in Fig. 8.

Nevertheless, seen from Fig. 11(c), the efficiency of the proposed converter is worse than that of the conventional buck PFC converter, almost 2% less in average. This is due to the more component count and the used transformers in the proposed converter.

IV. Conclusions

To eliminate the dead angles of the input line current in the conventional buck PFC converter, many literatures use additional switch and control circuit to switch between the buck and flyback modes, which are effective but at cost of high control complexity.

Alternatively, in order to maintain the simple control meanwhile eliminate the dead angles, this paper integrates switches to allow the proposed converter automatically changing between the buck-flyback mode and the buck mode. Although the proposed converter decreases the efficiency due to the more component count, however, the dual bridgeless configuration can maintain the efficiency at an acceptable level. Consequently, in the 100~240 Vac input voltage range, compared to the conventional buck PFC converter, the proposed converter, in compliance with IEC 61000-3-2 Class D limits, has better PF, THD*i*, and smaller output voltage ripple, but at cost of around 2% decreased efficiency in the 100 W prototype.

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