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Published in:
IEEE Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2019.2954555

Publication date:
2020

Document Version
Accepted author manuscript, peer reviewed version

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2954555, IEEE Journal of Emerging and Selected Topics in Power Electronics

Resynchronization Analysis and Improvement of Grid-Connected VSCs During Grid Faults

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***Abstract*—Grid codes stipulate that grid-connected voltage source converter (VSC) interfaced generation units should possess fault ride-through capability during grid faults. Resynchronization with the post-fault grid is crucial for this purpose. However, it is not always easy for VSCs connected to a high-impedance weak grid to achieve the resynchronization during severe grid faults. This paper studies loss of synchronism (LOS) of VSCs during grid faults. A nonlinear model describing the dynamics of phase-locked loop (PLL) is developed and a modified equal area criterion is utilized to identify the crucial factor affecting the resynchronization. The findings show that PLL's integral regulator is unfavorable for the resynchronization, since it probably causes the system operating point to enter negative damping zones and even reverse regulation zones, consequently resulting in LOS. A variable structure PLL method with great simplicity is proposed to improve the resynchronization capability. The method removes PLL's integral regulator during grid faults to eliminate its unfavorable effect. Experimental and simulation comparisons with existing methods verify the performance of the method.**

***Index Terms*—Converter, phase locked loop, synchronization stability, transient stability, equal area criterion, LVRT.**

I. Introduction

VOLTAGE source converters (VSCs) are currently widely used as interfaces connecting photovoltaic systems or wind turbines to the power grid. Grid-connected VSC interfaced generation units present different operating characteristics from synchronous generator during grid faults [1], [2]. To standardize fault operating characteristics of grid-connected VSC units, mandatory grid codes have been formulated [3], [4]. To meet requirements from grid codes, it is desirable to enable VSC units to remain connected with the grid within a certain time period after grid faults and perform reactive current injection. For this purpose, it is important for VSC units to resynchronize with the remaining grid voltage during grid faults. Nonetheless, achieving the resynchronization is not always easy for VSCs connected to a high-impedance weak grid.

While connected to a weak grid, the output current of VSCs produces a significant voltage drop on the grid impedance, which makes the VSC terminal voltage easily changeable with the output current. Taking such a voltage signal as the input of phase-locked loop (PLL) could make it difficult to synchronize with the weak grid (especially during grid faults) [5], [6], and consequently grid synchronization instability (GSI) may occur. GSI in large disturbance cases such as grid faults is also called loss of synchronism (LOS) [5]. The phenomenon of GSI features the gradual divergence or deviation of the frequency of PLL from the fundamental frequency [5], [6], which likely results in the protective action and tripping of VSCs. Several LOS associated photovoltaic converter tripping accidents have been reported in the past few years [7], [8].

Previous interests on grid synchronization techniques were mostly directed to PLLs [9] and frequency-locked loops (FLLs) algorithms [10] themselves. Such research often takes it for granted that grid synchronization unit is an independent system and the voltage being detected is an independent input. However, such consideration is not realistic for weak grid scenarios. The research regarding GSI in weak grid scenarios should at least takes into account PLL, current control, grid impedance and so on. Previous research efforts in this respect can be classified into two categories: small-signal stability studies [11]–[21] and large-signal stability studies [5], [6], [22]–[34].

Previously, numerous small-signal stability studies [11]–[21] have affirmed that high bandwidth of PLL and low short-circuit ratio of the grid deteriorate the small-signal stability of grid-tied VSC systems and probably cause GSI, especially during low voltage ride through (LVRT). Wen *et al.* [11] presented impedance modeling and analyzed the effect of PLL on the impedance of VSCs. Wen *et al.* [12] and Rosso *et al.* [13] further investigated the impact of the interaction between parallel converters on GSI. Huang *et al.* [14] revealed the influence of reactive power control on GSI. Besides impedance analysis, modal analysis is also a popular choice in small-signal stability studies [15], [16]. Wang *et al.* [15] and Liu *et al.* [16] utilized modal analysis to investigate the influence of various factors on the dominated oscillation mode associated with PLL. Complex torque coefficient method is another powerful tool. By employing the method, Hu *et al.* [17], [18] provided insight into the fundamental mechanism of small-signal instability caused by the interaction between PLL and current controller. Additionally, various methods to improve small-signal stability have also been developed, e.g., introducing impedance compensation into PLL [19], adding feedforward compensation into current controller [20], and tuning the bandwidth of PLL [21]. Although small-signal stability studies of GSI have been extensively documented, it must be noted that they disregarded nonlinear characteristics of VSC systems and therefore could not address the case where initial state is far away from steady state equilibrium point or even there is no equilibrium point. In this respect, large-signal studies are indispensable.

To our knowledge, there have been not many large-signal studies on GSI (namely LOS). Göksu *et al*. [5] and Dong *et al*. [6] made groundbreaking research and analyzed the existence

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of post-fault equilibrium point. Yuan *et al.* [22] also contended that the absence of equilibrium point is a key inducement to LOS. Pei *et al.* [23] made a comprehensive analysis on equilibrium point considering different grid parameters and current references. In fact, from the viewpoint of stability requirements of nonlinear system, the resynchronization of grid-tied VSCs after grid faults depends on initial state and dynamic characteristics, in addition to the presence of equilibrium point.

Based on the findings in [5] and [6], the authors made further research [24]–[27] in this respect. It was found that the resynchronization was related to not only the existence of post-fault equilibrium point but also stochastic initial state and dynamic behavior of PLL. To analyze the dynamic behavior of PLL, Zhang *et al.* [28] and Han *et al.* [29] drew lessons from the transient stability mechanism of synchronous generator and attempted to apply the equal area criterion (EAC). The results showed that fault clearing angle matters to LOS. Actually, in contrast to slow power response of synchronous generator with rotating mass, fast PLL response of VSCs makes it possible to decide whether LOS occurs within grid fault period [14]–[17]. Hence, it might be inappropriate to directly apply the conventional EAC method into VSC units. Except for the EAC method, phase portrait method [30], [31] was also used to analyze the resynchronization of VSC systems. Nevertheless, the method has difficulty in identifying factors causing LOS and yielding a general stability criterion to assess whether LOS occurs.

For VSC systems with another control mode, i.e., voltage-controlled mode, their GSI issues are also of great concern. Huang *et al.* [32], Wu *et al.* [33], and Shuai *et al.* [34] investigated the GSI issue of droop controlled VSCs, power synchronization controlled VSCs, and virtual synchronization generator, respectively. Since the dynamic characteristics of VSCs is primarily shaped by control algorithm, the GSI characteristics under different control algorithms should be somewhat different. The GSI under current controlled mode is the focus of this study.

This paper reports new results of continuous research based on [24]–[27]. In this paper, a modified EAC is developed to clearly identify factors causing LOS and a general stability criterion is derived. The findings reveal two crucial factors resulting in LOS. One is the voltage drop on grid-side impedance and the other is PLL's second-order integral loop. In the prior work [24], an adaptive current injecting method was developed to address the first factor for improving the resynchronization capability. However, the method needs fast grid impedance detection. To explore other practicable methods, the attention of this study is turned to address the second factor. It is found that this factor can be eliminated by a simple method called as variable structure PLL (VSPLL). During grid faults, the method removes PLL's integral regulator while retaining proportional regulator. Consequently, the LOS risk due to the lag effect of integral regulator is avoided and the resynchronization capability is improved. Both experimental and simulation results show that the method has high performance such as zero overshoot and globally asymptotic stability.

The remainder of this paper is organized as follows. Section II develops a reduced-order nonlinear model to describe the dynamics of PLL. Section III uses a modified EAC to analyze the resynchronization and derives a quantitative stability criterion. Section IV proposes the VSPLL method. Sections V and VI conduct experimental and simulation verifications, respectively. Section VII concludes this paper.

II. System Modelling

A. Reduced-Order Nonlinear Model

Fig. 1 displays the circuit and control diagram of a single-converter infinite-bus (SCIB) system, in which R_g and L_g represent the Thévenin equivalent grid impedance; R_l and L_l represent the transmission line impedance. When a symmetrical grid fault, e.g., a three-phase grounding fault (grounding resistance is R_f) occurs, the fault-point voltage dips, triggering transient process of the system [1], [2]. VSC is often configured with a chopper protective circuit, which is activated during transient process to suppress DC-link overvoltage and accordingly maintain the DC-link voltage. Hence, the DC-link voltage during grid fault period was often seen as a constant voltage source in previous research [5], [6], [22]–[31]. After switching to fault control mode once the grid fault is detected, the reactive current reference in Fig. 1 is directly designated by grid code specification [3], whereas the active current reference is often set to zero considering the capability limit of converter.

The ac current control (ACC) in Fig. 1 is oriented by a PLL. Currently, synchronous reference frame-based PLL (SRF-PLL) is widely used. Fig. 2 shows the SRF-PLL diagram and also two reference frames of concern. The grid voltage reference frame (*XY* reference frame) that indicates the phase angle of grid voltage vector rotates with grid frequency $\omega_b\omega_g$ (ω_g is a per-unit value, the base value of which is ω_b). The PLL reference frame rotates with PLL frequency $\omega_b\omega_{pll}$. The included angle between the two reference frames is denoted as δ,

$$d\delta/dt = \omega_b\left(\omega_{pll} - \omega_g\right) \triangleq \omega_b\Delta\omega. \tag{1}$$

The frequency dynamics of PLL is described as

$$d\left(\omega_b\Delta\omega\right)/dt = d\left(\omega_b\omega_{pll}\right)/dt = k_p\, du_q/dt + k_i u_q \tag{2}$$

where k_p and k_i are PLL parameters. u_q is q-axis voltage of $\boldsymbol{u}_{abc}$, which converges to zero only when PLL reaches steady state. Note that the grid frequency dynamics in (2) is neglected considering the fact that the grid has slower frequency dynamics than the frequency dynamics of PLL.

Fig. 3(a) shows the equivalent circuit of the system, in which the ACC loop is represented by an impedance model [35].

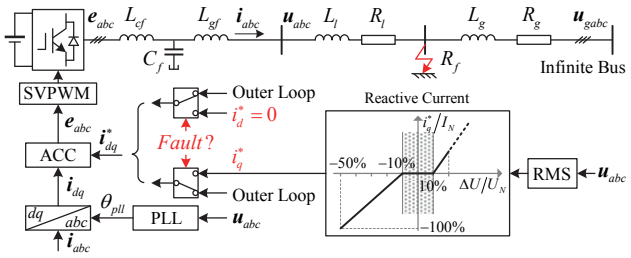

Fig. 1. Circuit and control diagram of a SCIB system. Once the grid fault is detected, the control algorithm is switched from normal control mode to fault control mode.

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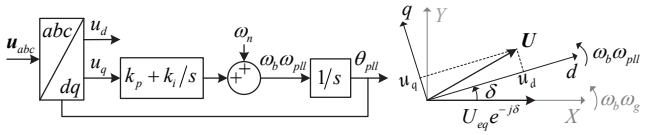

Fig. 2. SRF-PLL diagram and the relation between *XY* reference frame and PLL (*dq*) reference frame.

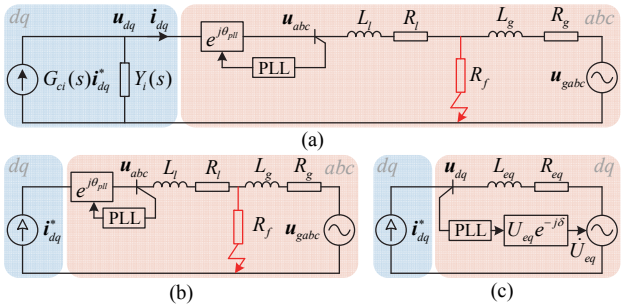

Fig. 3. Equivalent circuit of the system. (a) The ac current control (ACC) loop is represented by a controlled current source in parallel with input admittance [35, eq. (11)]. (b) The ACC loop is simplified to a quasi-steady-state current source. It is approximated to sinusoidal steady state at *abc* reference frame and direct-current steady state at *dq* reference frame, and therefore inductor plays a part only in the form of inductive reactance, e.g., $j\omega_{pll}L_l$, $j\omega_{pll}L_g$. (c) Equivalent circuit at *dq* reference frame.

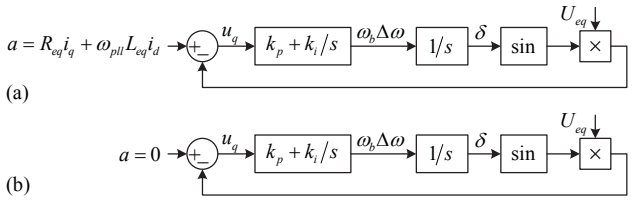

Fig. 4. Reduced-order nonlinear system model. (a) Non-ideal model comprising of PLL and equivalent grid impedance. (b) Ideal model (zero impedance or zero current).

Since the bandwidth of ACC is much higher than that of PLL, the ACC loop can be simplified to a quasi-steady-state current source in the time scale of PLL dynamics [24]–[31], as shown in Fig. 3(b). While neglecting the electromagnetic transient of current, the current source is approximated to dc steady state at *dq* reference frame, i.e., $d\boldsymbol{i}_{dq}/dt = 0$, and therefore it is allowed to be connected in series with inductance such as $j\omega_{pll}L_l$. In this context, the circuit is analytically solvable. However, it cannot pass the solvability examination of software tools because such a connection is improper in general practice. To this end, Fig. 3(a) is suggested for numerical calculation, if necessary.

Seeing from the terminal of the current source in Fig. 3(b) towards the grid side yields the Thévenin equivalent circuit. Further, the grid-side circuit can be transformed into *dq* reference frame, as shown in Fig. 3(c). Neglecting transient current and only considering steady-state current component yields the mathematical expression of the circuit in a form of phasor [24]–[31]. The mathematical expression before grid fault is

$$\begin{aligned} \dot{U}_{eq} &= U_g e^{-j\delta_0} \\ R_{eq} + j\omega_{pll}L_{eq} &= R_l + j\omega_{pll}L_l + R_g + j\omega_{pll}L_g \end{aligned} \tag{3}$$

where U_g is the infinite-bus voltage amplitude and δ_0 is the included angle in Fig. 2 before grid fault. The mathematical expression after grid fault is

$$\begin{aligned} \dot{U}_{eq} &= U_g e^{-j\delta_0}\frac{R_f}{R_f + R_g + j\omega_{pll}L_g} \triangleq U_{eq}e^{-j\delta} \\ R_{eq} + j\omega_{pll}L_{eq} &= R_l + j\omega_{pll}L_l + R_f \,/\!/\, \left(R_g + j\omega_{pll}L_g\right). \end{aligned} \tag{4}$$

By comparing (3) and (4), it is found that there is a phase jump appearing in the equivalent grid voltage $\dot{U}_{eq}$ when grid faults occur. Accordingly, there is also a change of orientation of *XY* reference frame, which means that the included angle in Fig. 2 instantaneously changes with the phase jump. The phase jump makes the initial state of the system far away from the steady state point (if there is a steady state) [24]. According to Fig. 3(c), the voltage equation of the equivalent circuit is,

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} \cos\delta & \sin\delta \\ -\sin\delta & \cos\delta \end{bmatrix}\begin{bmatrix} U_{eq} \\ 0 \end{bmatrix} + \begin{bmatrix} R_{eq} & -\omega_{pll}L_{eq} \\ \omega_{pll}L_{eq} & R_{eq} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{5}$$

where $\boldsymbol{u}_{dq}$ and $\boldsymbol{i}_{dq}$ correspond to $\boldsymbol{u}_{abc}$ and $\boldsymbol{i}_{abc}$, respectively. Besides, it can be deemed that $\boldsymbol{i}_{dq}$ has converged to $\boldsymbol{i}_{dq}^*$, because the ACC loop works very fast.

From (5), it can be further derived that

$$u_q = R_{eq}i_q + \omega_{pll}L_{eq}i_d - U_{eq}\sin\delta \triangleq a - U_{eq}\sin\delta \tag{6}$$

where a is an offset term introduced by the voltage drop on grid-side impedance. Under normal condition $a > 0$ since $i_q = 0$ and $i_d > 0$, whereas $a < 0$ under fault condition since $i_q < 0$ and $i_d = 0$ (see Fig. 1).

Equations (1), (2), and (6) constitute the nonlinear model of the system, as shown in Fig. 4(a). The parameters of grid-side impedance in the model could be considered variables and thus the model has generality with respect to any grid strength. The primary concern of this study is to analyze the fundamental mechanism of LOS and identify instability factors. Hence, it is reasonable to assume the grid-side impedance parameters are invariant during grid faults for simplifying the analysis.

If the grid-side impedance or the output current is zero, the offset term will be removed, as shown in Fig. 4(b). Most previous PLL investigations were based on the ideal model in Fig. 4(b) rather than the non-ideal model in Fig. 4(a). Therefore, the synchronization performance of VSC systems was not completely assessed. Especially, the LOS issue during grid faults was not discovered and addressed in previous PLL research.

Although the model in Fig. 4(a) has been widely recognized by previous research [24]–[31], it should be noted that it is only valid with the following assumptions:

1) The bandwidth of ACC is much higher than that of PLL so that ACC works much faster than PLL and accordingly the ACC loop together with the terminal filter can be simplified to a quasi-steady-state current source.
2) Transient current component is disregarded and steady state current component is the primary concern. Thus, inductor plays a part only in the form of inductive reactance so that the current source is allowed to be connected in series with grid-side inductance.

With proper parameters tuned for both ACC and PLL, the ACC bandwidth is larger than 200 Hz whereas the PLL bandwidth is about 10~30 Hz [18]. The latter frequency range is the concern of this study, which is fully separated with the former

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in frequency domain. Besides this, the dynamics of PLL is also much slower than the electromagnetic transient of current. Therefore, current transient component can be disregarded, as indicated in (5). On the above conditions, the validity of the model is well established [24]–[31]. If the ACC bandwidth is too low or the PLL bandwidth is too high, e.g., their ratio is about less than 7 [17], there will inevitably be interaction between the two loops and it will bring inaccuracy to the model. In this connection, the model should be modified to fit into the dynamics of the ACC loop. This issue still remains unresolved currently at least for large-signal stability analysis [31].

B. Swing-Equation Model

The model can be transformed into a form of swing equation,

$$J_{eq}\, d\omega_{pll}/dt = u_q - D_{eq}\left(\omega_{pll} - \omega_g\right) \tag{7}$$

$$J_{eq} = \frac{\omega_b}{k_i}\left(1 - \frac{k_p L_{eq} i_d^*}{\omega_b}\right) \approx \frac{\omega_b}{k_i},\ D_{eq} = \frac{k_p U_{eq}\omega_b}{k_i}\cos\delta \tag{8}$$

where J_{eq} and D_{eq} are equivalent inertia and damping coefficients. Note that J_{eq} is about tens to hundreds of milliseconds, which makes sense because the response of PLL is often tuned to be fast enough, e.g., ~30 Hz bandwidth [36].

From (8), it if found that the inertia effect originates from the integral regulator of PLL whereas the damping effect originates from the proportional regulator of PLL ($k_p = 0$ makes $D_{eq} = 0$). Note that although various "swing equations" were developed previously [37] to investigate the capability of VSCs to mimic inertia emulation and frequency support characteristics of synchronous generator, the "swing equation" concept was rarely used to investigate the synchronization characteristics of VSCs.

Equation (7) implies the comparability with the swing equation of classical synchronous generator,

$$J_{sg}\, d\omega_{sg}/dt = \Delta P - D_{sg}\left(\omega_{sg} - \omega_n\right). \tag{9}$$

The term u_q in (7) is comparable to imbalanced power term ΔP in (9) and thus u_q can be regarded as imbalanced component to drive PLL frequency to change. By referring to the transient stability mechanism of synchronous generator, it is believed that the resynchronization of VSC systems is characterized by the function relation $u_q(\delta)$ between u_q and δ.

III. Resynchronization Analysis

No matter how large the offset term a is, the phase-angle of the terminal voltage $\boldsymbol{U}$ is certainly detectable. However, it cannot be inferred that the VSC is always able to synchronize with the grid while using the detected phase-angle to conduct the desired current control. For the latter, the voltage equation (5) must also be considered. The impact of the offset term a on the resynchronization of VSCs depends on the size of a relative to U_{eq}. If $|a|$ is larger than U_{eq}, the VSC is unable to synchronize with the grid due to the absence of equilibrium point. If $|a|$ is smaller than U_{eq}, the VSC may still be unable to synchronize with the grid during dynamic regulation process of PLL.

C. Equilibrium Point Analysis

For the developed nonlinear model, its equilibrium point is indicated by

$$u_q = 0 \Leftrightarrow a = U_{eq}\sin\delta. \tag{10}$$

where $u_q = 0$ is not only the equilibrium point of PLL but also a basic requirement of voltage-oriented vector control. Equation (10) implies that the existence of equilibrium point is related to the offset term a, i.e., the voltage drop on the equivalent grid impedance. Hence, the voltage drop is considered one crucial factor affecting the resynchronization.

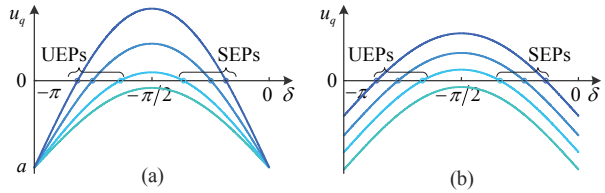

Fig. 5. Illustration of equilibrium point. Equilibrium point may disappear with (a) the decrease of post-fault equivalent grid voltage, or (b) the increase of voltage drop on grid-side impedance.

The zero-crossing point of the curve $a - U_{eq}\sin\delta$ is depicted in Fig. 5. If $|a| > U_{eq}$, caused by a severe grid voltage sag or a large offset term, there will be no longer equilibrium point. In this case, it is impossible to ensure the resynchronization during grid fault period, using either PLL or algebraic calculation [e.g., $\arctan(u_\beta/u_\alpha)$]. The critical point corresponds to $|a| = U_{eq}$. The right equilibrium points in Fig. 5 are stable equilibrium points (SEPs) whereas the left ones are unstable equilibrium points (UEPs), according to the small-signal stability condition [24]

$$du_q/d\delta < 0. \tag{11}$$

D. Dynamic Resynchronization Process Analysis

Even though there is a SEP, the resynchronization may still not be achieved during dynamic regulation process of PLL in the context that the offset term makes the function relation $u_q(\delta)$ no longer unbiased.

For synchronous generator, the damping term in (9) is able to weaken frequency oscillations during swing processes of rotor. A positive damping coefficient can improve the transient stability whereas a negative one does harm to that. The damping coefficient of synchronous generator generally keeps positive because of mechanical friction and damper windings. Neglecting the damping term, it is relatively conservative but credible using the equal area criterion (EAC) to quantitatively assess the transient stability.

Prior to adopting the concept of EAC to analyze the resynchronization of VSC systems, it is supposed to firstly evaluate the sign of damping coefficient D_{eq} in (8). When δ is within the zone $(-\pi/2, \pi/2)$, D_{eq} is positive. When δ is within the zone $(\pi/2, 3\pi/2)$, D_{eq} becomes negative. To ensure a positive damping effect, δ has to locate within the zone as follows,

$$\delta \in \left(\delta_{D1}, \delta_{D2}\right) = \left(-\pi/2 + 2k\pi,\ \pi/2 + 2k\pi\right). \tag{12}$$

Actually, (11) is equivalent to (12). In other words, the positive damping zone is the same as the small-signal stability zone. Equation (12) lays the foundation of using the concept of EAC. Further, as indicated in (8), when U_{eq} becomes quite small after a severe grid fault, D_{eq} becomes small as well. Hence, provided

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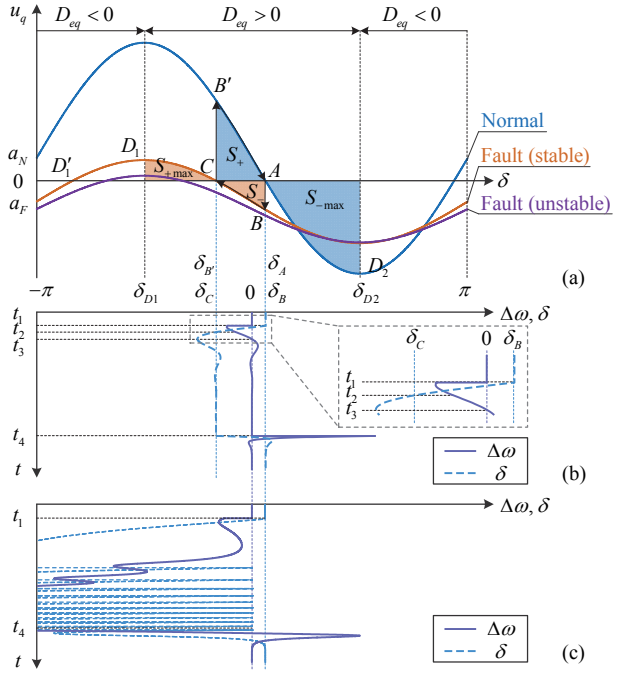

Fig. 6. Dynamic resynchronization process. (a) Accelerating and decelerating areas. (b) The operating point doesn't exceed the critical point D_1, and the system is stable. (c) The system becomes unstable during a more severe grid voltage sag.

that (12) is satisfied during grid fault period, the damping term in (7) will be removed, which yields that

$$J_{eq}\, d\omega_{pll}/dt = u_q. \tag{13}$$

Considering the difference in terms of the order of magnitude between J_{eq} in (7) and J_{sg} in (9), fast PLL response makes it possible to determine whether LOS occurs within the period of grid fault. Hence, the conventional EAC cannot be directly used to analyze the dynamic resynchronization process of VSCs during grid fault. A modified EAC is proposed here for this purpose.

1) Offset Term a < 0: The blue and orange curves in Fig. 6(a) represent normal and fault operating conditions, respectively. The points A and C are two corresponding SEPs. When a grid voltage sag occurs at t_1 (the phase keeps unchanged), the operating point steps from A to B. Then, the operating point moves towards C since B is not an equilibrium point. Without considering the effect of damping term, there is a decelerating process of $\Delta\omega$ and a decrease of δ. The decelerating area is

$$S_- = \int_{\delta_B}^{\delta_C} u_q d\delta = \int_{\delta_B}^{\delta_C} J_{eq}\frac{d\Delta\omega}{dt}d\delta = \frac{1}{2}J_{eq}\Delta\omega^2\Big|_{\delta_B}^{\delta_C} \tag{14}$$

where δ_B is PLL angle at the moment of the grid voltage sag; δ_C corresponds to the SEP C.

The operating point crosses the point C at t_2 and $\Delta\omega$ begins increasing due to u_q becomes positive (In fact, $\Delta\omega$ begins increasing before t_2 due to the effect of damping term). Then, δ reaches the minimum when $\Delta\omega$ returns to zero at t_3. It is expected that δ would not exceed the positive damping zone in the accelerating process, otherwise the negative damping effect would appear. The conservative maximum accelerating area is

$$S_{+\max} = \int_{\delta_{D1}}^{\delta_C} u_q d\delta = \frac{1}{2}J_{eq}\Delta\omega^2\Big|_{\delta_{D1}}^{\delta_C} \tag{15}$$

where δ_{D1} is given by (12). Hence, a sufficient condition for ensuring the resynchronization during the grid voltage sag is

$$S_- \le S_{+\max}. \tag{16}$$

If $S_- = S_{+\max}$, $\Delta\omega$ will increase to zero when the operating point reaches the critical point D_1, which seems to be the critical stability condition. In fact, the resynchronization can be ensured as long as $\Delta\omega$ increases to zero before the operating point reaches the UEP D_1'. In other words, the UEP D_1' defines the critical stability boundary [24]. The distance between the operating point and the boundary characterizes how far the system is from instability. However, once the operating point crosses the positive damping boundary, D_{eq} becomes negative. Under such circumstances, the sufficient condition (16) cannot be derived strictly because it is difficult to quantitatively evaluate the effect of negative damping.

2) Offset Term a > 0: When the grid voltage sag is cleared at t_4, the operating point steps from C to B'. Then, the operating point moves towards A, accompanied by an accelerating process of $\Delta\omega$ and an increase of δ. The accelerating area is

$$S_+ = \int_{\delta_{B'}}^{\delta_A} u_q d\delta = \frac{1}{2}J_{eq}\Delta\omega^2\Big|_{\delta_{B'}}^{\delta_A}. \tag{17}$$

Similarly, the conservative maximum decelerating area is

$$S_{-\max} = \int_{\delta_{D2}}^{\delta_A} u_q d\delta = \frac{1}{2}J_{eq}\Delta\omega^2\Big|_{\delta_{D2}}^{\delta_A}. \tag{18}$$

Similar to (16), a sufficient condition for the resynchronization after the grid voltage recovery is derived as follows,

$$S_+ \le S_{-\max}. \tag{19}$$

3) Offset Term a = 0: If a is zero or insignificant compared with U_{eq}, the function $u_q(\delta)$ will be unbiased or nearly unbiased. The resynchronization is guaranteed in this case owing to the dissipative effect of damping term [24].

The above analysis suggests that the dynamic performance in resynchronization processes is decided by the inherent property of PLL. PLLs contain a second-order integral loop and accordingly possesses universal properties of second-order systems, such as damping, overshoot, and oscillation. The angle overshoot in Fig. 6 is due to lag effect of the second-order integral loop. More precisely, δ lags behind $\Delta\omega$. For instance, when δ reaches its steady-state value δ_C at t_2, $\Delta\omega$ is unfortunately smaller than zero. Thus, δ has to continue decreasing, leading to the unfavorable angle overshoot. If the angle overshoot exceeds the UEP D_1', the resynchronization would not be guaranteed any longer.

Fig. 6(c) indicates that the system really becomes unstable when a more severe voltage sag than that in Fig. 6(b) happens. Since the accelerating area is insufficient, the angle overshoot exceeds the UEP D_1' and $\Delta\omega$ fails to return to zero after the first swing. The negative damping effect as well as the subsequent reverse regulating effect directly leads to LOS.

Therefore, from the viewpoint of dynamic resynchronization process, PLL's second-order integral loop could be considered another crucial factor affecting the resynchronization.

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E. Stability Criterion

Summarizing the foregoing results yields the stability criterion in Table I. It should be noted that Fig. 6 just illustrates a basic resynchronization process during a grid voltage sag and recovery. The grid voltage amplitude in Fig. 6 changes while the grid phase remains unchanged. In reality, both of them changes when a grid fault occurs. As a result, the initial value of δ, corresponding to the location of point B, is stochastic [24]. Therefore, there is difficulty in online use of the stability criterion. However, offline use is feasible. It is also noted that the stability criterion in Table I is derived from a single-converter infinite-bus system. For a more complex system configuration, it is necessary to perform system simplifications, make additional assumptions, or develop advanced stability criteria.

TABLE I
STABILITY CRITERION OF RESYNCHRONIZATION

Conditions	Results	Remarks
$\lvert a\rvert > U_{eq}$	Unstable	No equilibrium point
$\lvert a\rvert \le U_{eq}$, $a < 0$, $S_- \le S_{+\max}$	Stable	Sufficient condition
$\lvert a\rvert \le U_{eq}$, $a > 0$, $S_+ \le S_{-\max}$	Stable	Sufficient condition
$\lvert a\rvert \le U_{eq}$, $a = 0$	Stable	Sufficient condition
Other conditions	Unstable	Unstable to a large extent

IV. RESYNCHRONIZATION CAPABILITY IMPROVEMENT

A. Proposed VSPLL Method

The factors affecting the resynchronization have been clarified, including the voltage drop on grid-side impedance and the second-order integral loop of PLL. Eliminating any of them can improve the resynchronization capability. In the previous work [24], an adaptive current injecting (ACI) method was proposed to eliminate the first factor. However, the method needs to fast estimate post-fault grid impedance. It is not easy to accomplish the estimation during several cycles after grid faults.

This study is devoted to addressing the second factor. The simplest way is removing the integral regulator during grid fault period so as to yield a first-order integral loop. The unfavorable angle overshoot can be avoided with the first-order integral loop, since there is no overshoot in any first-order system.

The proposed VSPLL method is shown in Fig. 7. Once a grid fault is detected, the integral regulator of PLL is removed until fault clearance. The method is highly simple and therefore it is easy to use in practice. The VSPLL during grid fault period becomes a type-1 PLL [38]. The highlight of this method is to indicate that type-1 PLL is a more appropriate choice for fault-ride through applications than type-2 PLL, although type-1 PLL itself has been investigated by prior research [38].

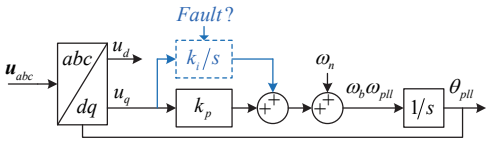

Fig. 7. Proposed VSPLL method.

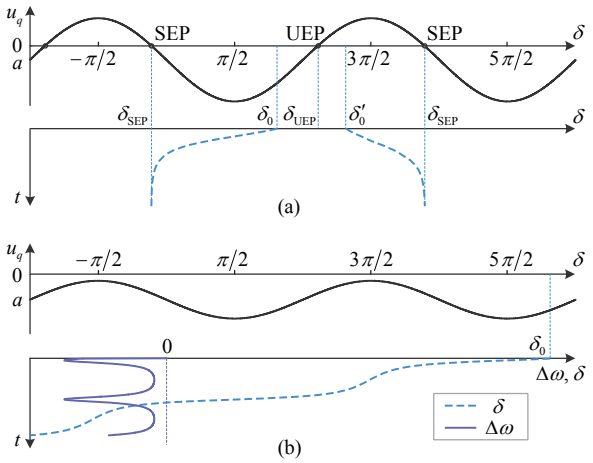

Fig. 8. Convergence process of the VSPLL. (a) With equilibrium point, δ_0 converges to the left-side δ_{SEP} and δ_0' converges to the right-side δ_{SEP}. (b) Without equilibrium point, $\Delta\omega$ continuously oscillates.

B. Globally Asymptotic Stability Analysis

Note that the presence of SEP is still a prerequisite of asymptotic stability. Hence, it is assumed that $|a| \le U_{eq}$ in order to mathematically demonstrate the asymptotic stability. Removing the integral regulator during grid faults yields that

$$d\delta/dt = \omega_b \Delta\omega = k_p u_q = k_p\left(a - U_{eq}\sin\delta\right). \tag{20}$$

Several SEPs and UEPs of the resulting first-order system are shown in Fig. 8(a). A positive definite Lyapunov function is defined as,

$$V = \left(\delta - \delta_{SEP}\right)^2/2. \tag{21}$$

The time derivative of V is

$$\dot{V} = k_p\left(\delta - \delta_{SEP}\right)\left(a - U_{eq}\sin\delta\right). \tag{22}$$

If a stochastic initial value δ_0 is located between the interval (δ_{SEP}, δ_{UEP}) [see Fig. 8(a)], then $\delta > \delta_{SEP}$ and $a - U_{eq}\sin\delta < 0$ in the whole convergence process. Hence,

$$\dot{V} < 0. \tag{23}$$

A similar stability proof can be made for another stochastic initial value δ_0' located inside (δ_{UEP}, δ_{SEP}). Also, Fig. 8(a) indicates that there is no overshoot in the convergence process.

If there is no equilibrium point resulting from $|a| > U_{eq}$, then δ will decrease continuously, as shown in Fig. 8(b). In this case, $\Delta\omega$ undergoes a continuous oscillation rather than converges to zero. By comparing Fig. 8(b) with Fig. 6(c), it is found that the resynchronization capability is somewhat improved. To reduce PLL frequency deviation $\Delta\omega$ in Fig. 8(b), (20) suggests that decreasing k_p seems to be an available way. To create equilibrium point in this case, one of the simplest ways is to adjust active current reference [23], [24].

C. Comparisons with Existing Methods

Fig. 9 displays the schematic diagrams of three existing methods addressing the LOS issue. Table II summarizes their pros and cons. The simplest method is called as PLL freezing [39], which freezes PLL's PI regulator and then output angle according to the frequency and angle at the moment of freezing. Since the frozen PLL becomes open-loop, the method has static error issue and accordingly cannot cope with grid phase jumps

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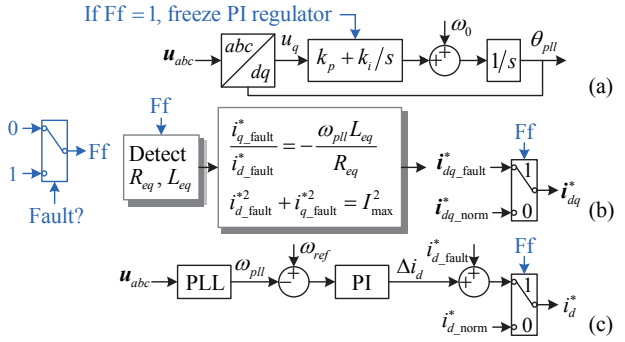

Fig. 9. Three existing typical methods addressing LOS. (a) PLL freezing method [39]. (b) Adaptive current injecting (ACI) method [24]. (c) PLL frequency based active current regulating method [5].

TABLE II
PROS AND CONS OF SEVERAL METHODS

Methods	Pros	Cons
PLL freezing [39]	Simple	Static error
ACI [24]	Stable even zero voltage	Need to detect grid impedance
PLL frequency-based regulating method [5]	Simple	Stability without theoretical proof
Proposed VSPLL	Simple, stable, and no overshoot	Cannot address the non-existence of SEPs

often occurring along with grid faults. Additionally, the current control oriented by this wrong angle is not in line with what grid code requires, since it is impossible to guarantee how much active or reactive component the output current contains. Particularly, it may even cause reactive power absorption.

The adaptive current injecting (ACI) method [24] specifies the ratio of active and reactive currents according to the post-fault equivalent grid impedance angle, consequently making the offset term become zero. However, the ACI method requires fast impedance estimation. It is not an easy task within a short period of several cycles after grid faults. Besides, there are often plenty of VSCs interconnected to the point of common coupling, and hence the offset term of one VSC is affected by the output current from others besides itself. In this regard, the ACI method is still in doubt for its practicability.

The PLL frequency-based active current regulating method [5] regulates the active current reference to enhance the re-synchronization capability. However, Reference [5] fails to analyze the equilibrium point and stability of the method, which makes the method unreliable for applications.

Actually, the proposed VSPLL could be seen as a tradeoff between the original PLL and the frozen PLL. Specifically, the PLL freezing method is equivalent to setting PI parameters to zero. To remain regulating capability, the VSPLL retains the proportional regulator while removing the integral regulator, accordingly addressing both static error and angle overshoot. The comparisons with three existing methods indicates the merit of the VSPLL method, as summarized in Table II.

It should be noted that asymmetrical grid faults are more common than symmetrical faults. The first method [39] disregards which type of faults and the latter three methods [5], [24] were without yet considerations for asymmetrical faults. How to address the LOS issue during asymmetrical grid faults needs further research, especially from the standpoint of large-signal stability.

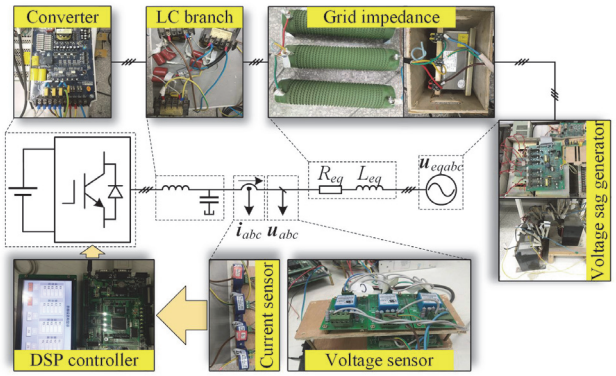

Fig. 10. Simulation system (diagram) and experimental setup (pictures) [41].

TABLE III
PARAMETERS OF THE TEST SYSTEM

Capacity	1 [kW]	DC-link voltage	400 [V]
Normal line voltage	170 [V]	Current loop	2 + 10/*s* [p.u.]
Fault line voltage	~24.3 or ~12.2 [V]	PLL	60.5 + 605/*s* [rad/p.u.] [1]
Grid resistance	0.121 [p.u.]	Switch frequency	3 [kHz]
Grid inductance	0.217 [p.u.]	Sample time	5 [μs]

[1] Equivalent to (25+250/*s*) [deg/V]. Note that (25+250/*s*) is PLL parameter adopted in the experiment [41]).

TABLE IV
TEST CASE SETUP

	Case I	Case II	Case III	Case IV
Normal line voltage (V)	170	170	170	170
Fault-point line voltage (V)	~24.3	~12.2	~12.2	~12.2
Reactive current peak (A)	4.74	5.10	5.10	5.10
Active current peak (A)	0.0	0.0	1.0	1.6
Is equilibrium point existent?	Yes	No	No	Yes
Experimental result (Fig. No)	11	12	12	13

V. EXPERIMENTS VERSUS SIMULATIONS

The VSPLL method have been implemented in an actual DSP digital controlled VSC platform and MATLAB/ Simulink platform for verifying its performance as well as one-to-one experimental *vs.* simulation comparisons. The setup of the experimental and simulation platform is depicted in Fig. 10. The two systems have the same parameters, as shown in Table III. The difference between them lies in the representation of the power grid. Grid faults in simulation are generated by a programmable voltage source. In contrast, grid faults in experiments are generated by a voltage sag generator, which works based on a transformer with multiple user-side tapping points. It can simulate different levels of voltage sags by switching the user-side tapping points.

A total of four test cases are designed in the following verification, in which normal grid voltage, post-fault grid voltage, reactive and active current references designated during grid fault period are summarized in Table IV. The fault in Case I is slighter than that in Case II, and it could be calculated that there is equilibrium point in Case I but there is not in Case II. A nonzero active current reference is designated in Case III to decrease the offset term, but it is not enough so there is still no

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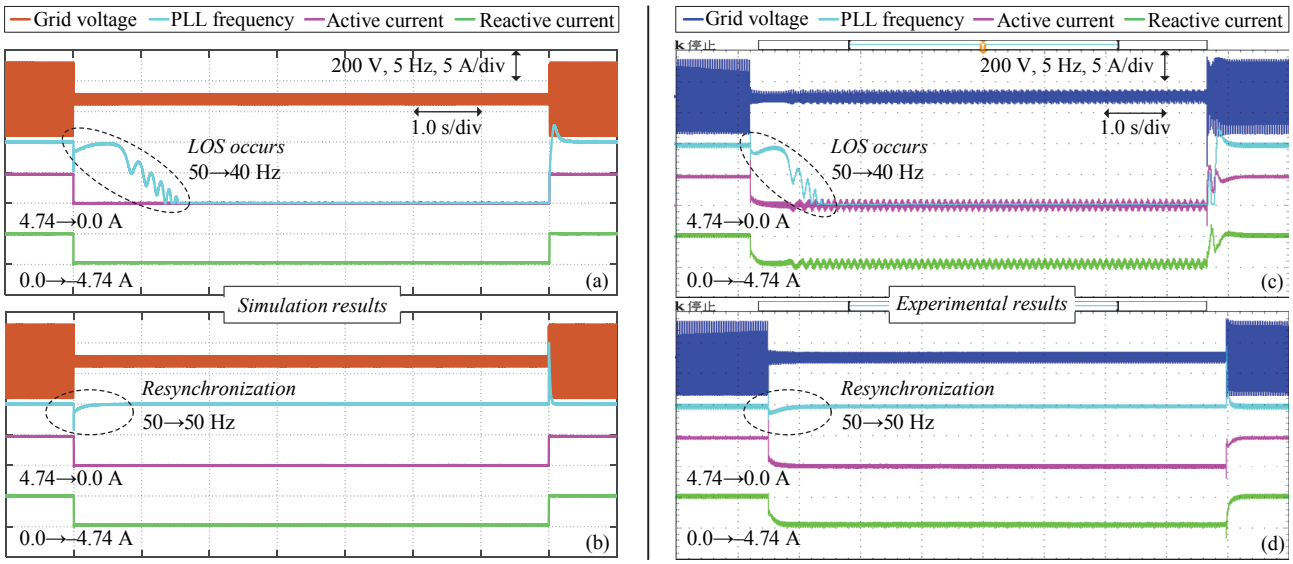

Fig. 11. Case I results indicate that the VSPLL is able to achieve the resynchronization whereas the original PLL cannot. (a) Simulation result with the original PLL. (b) Simulation result with the VSPLL. (c) Experimental result [41] with the original PLL. (d) Experimental result [41] with the VSPLL. Figs. 11–13 (c), (d) have been presented in our prior conference paper [41], the aim of which was to compare stability performance with different integral parameters or active currents.

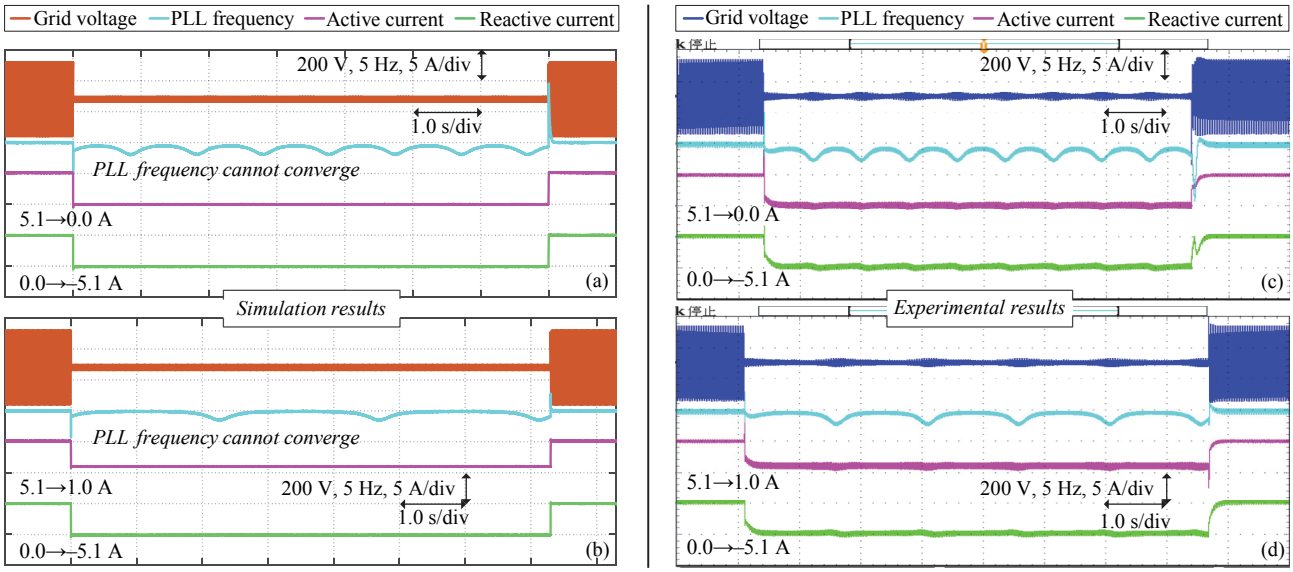

Fig. 12. Cases II and III results indicate that resynchronization cannot be achieved because of without equilibrium point, even though the VSPLL is used. (a) and (b) are simulation results, in which active current during grid fault are 0.0 A and 1.0 A, respectively. (c) and (d) are experimental results [41]. Note that the voltage sag generator is a transformer instead of a constant voltage source and hence the post-fault voltage keeps varying, resulting in slight difference from simulation results.

equilibrium point. In Case IV, a larger active current output is designated, which creates equilibrium point.

Note that the fault duration lasts for a long enough time (e.g., 8 s) in the experiment in order to show the whole process of losing synchronism comprehensively and clearly. Under practical fault duration of power systems, such as ~100 ms [40], it is possible that grid faults have been cleared before the VSPLL converges, but the method itself is valid in terms of asymptotic stability.

A. Case I

There is equilibrium point in Case I. Nonetheless, the system may become unstable during grid fault period owing to $S_{-} > S_{+\max}$, according to the stability criterion in Table I. Fig. 11(a) and (c) show that LOS really occurs with the original PLL. By contrast, if the VSPLL method is utilized, it can be seen from Fig. 11(b) and (d) that the first-order PLL can fast achieve resynchronization without any overshoot. Also, Fig. 11 shows that the simulation and experimental results are highly similar, slight difference of which is because the voltage sag generator is not a constant voltage source. Hence, the post-fault grid voltage in Fig. 11(c) remains varying.

B. Cases II and III

In Cases II and III, the active currents designated during grid fault period are 0.0 A and 1.0 A, respectively, as shown in Fig.

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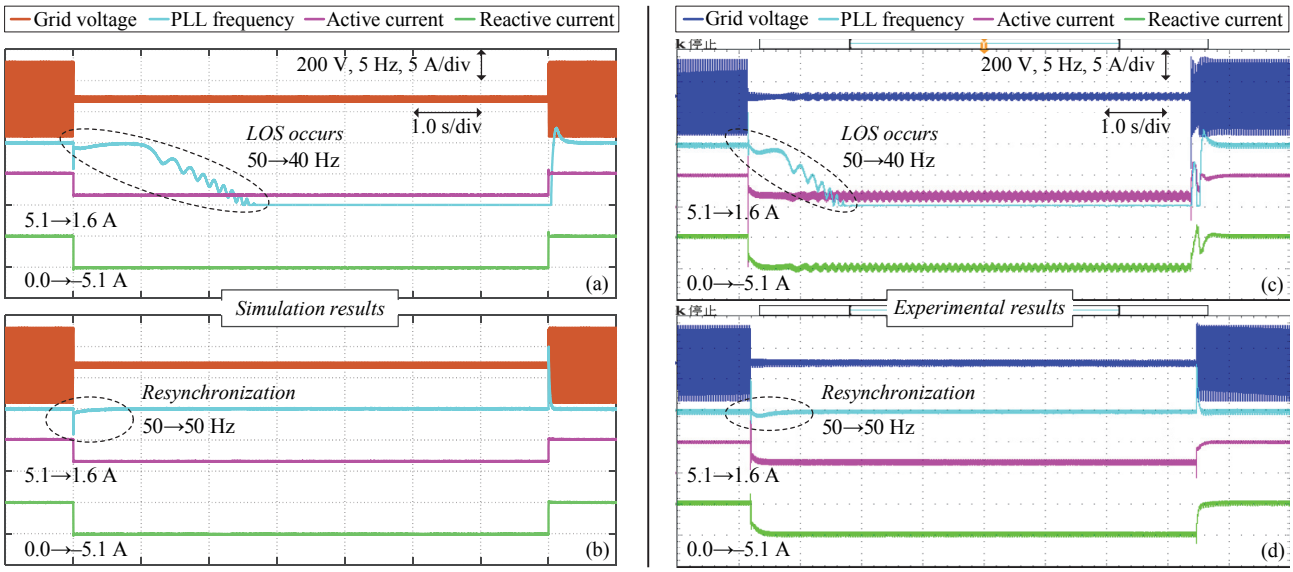

Fig. 13. Case IV results indicate that the VSPLL is able to achieve the resynchronization when equilibrium point is created by outputting a larger active current during grid fault, whereas the use of the original PLL results in LOS. (a) Simulation result with the original PLL. (b) Simulation result with the VSPLL. (c) Experimental result [41] with the original PLL. (d) Experimental result [41] with the VSPLL.

12. Although the positive active current output in Case III can help reduce the offset term, there is still no equilibrium point. Therefore, even if the VSPLL method is adopted, the system without equilibrium point fails to converge during grid faults. Instead, PLL frequency undergoes a continuous oscillation. The results in Fig. 12 coincide with the theoretical analysis in Fig. 8(b). By comparison between Cases II and III, it is found that the smaller the offset term, the weaker PLL frequency oscillation, and the closer it is to the fundamental frequency.

C. Case IV

The active current reference in Case IV is set to a larger value 1.6 A than 1.0 A in Case III. Thus, equilibrium point is created because the offset term is further reduced. Consequently, the resynchronization can be easily achieved using the VSPLL method, as shown in Fig. 13(b) and (d). In contrast, the use of the original PLL results in LOS, as shown in Fig. 13(a) and (c). It has been clarified that the LOS event is because of the effect of PLL's second-order integral loop. Again, it is verified that the proposed VSPLL method is able to address the LOS issue provided that there is post-fault equilibrium point.

Even if there is no equilibrium point after grid faults, it is suggested by (20) that PLL frequency deviation $\Delta\omega$ can be reduced by properly lowering k_p. A small enough PLL frequency deviation during grid faults would not cause grid-tied VSCs to trip.

VI. Simulation Verifications on Wind Turbines

Considering wide application of VSCs in wind turbine equipment, simulation verifications are further conducted on wind turbines. Type-3 and type-4 wind turbine detailed modeling is made on PSCAD/EMTDC platform. In order to simulate actual systems as far as possible, both the models are electromagnetic transient models with switch-level accuracy. The simulated SCIB system is shown in Fig. 14 and wind turbine parameters are given in Table V. When the three-phase grid fault shown in Fig. 14 occurs, both the grid voltage amplitude and phase change. The current reference at the PLL reference frame during grid fault period is set to $0.0 - j1.0$ p.u.

Two different cases are set to verify the performance of the VSPLL method in two scenarios, i.e., with SEP and without SEP. Case A: grounding resistance R_f is 2.0 Ω; Case B: grounding resistance R_f is 0.5 Ω. It can be verified that there is post-fault equilibrium point in Case A whereas there is not in Case B. Furthermore, the stability judgment result in Case A is probably unstable whereas it is definitely unstable in Case B.

A. Case A: 2.0 Ω Grounding-Resistance Fault

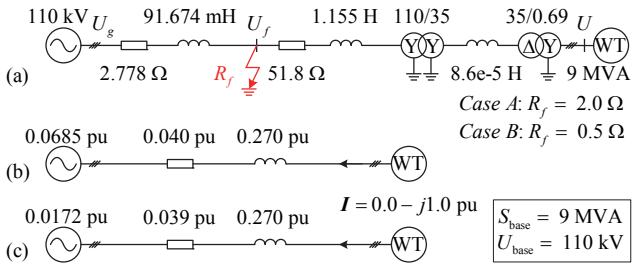

Fig. 14. Simulated SCIB system. (a) Original system. (b) Post-fault equivalent system in Case A. (c) Post-fault equivalent system in Case B.

TABLE V
6 × 1.5 MVA 690 V Wind Turbine Parameters (Per-Unit Value)

Type-3 wind turbine parameters (part)			
Stator leakage inductance	0.171	Stator resistance	0.008
Rotor leakage inductance	0.156	Rotor resistance	0.006
Turbine inertia constant	5.0	DC voltage loop	5+100/s
Grid coupling inductance	0.3	Rotor current loop	1.2+50/s
Mutual inductance	2.9	PLL	100+1500/s
Type-4 wind turbine parameters (part)			
Grid coupling inductance	0.15	DC voltage loop	1.5+100/s
GSC current loop	0.8+8/s	PLL	100+1500/s

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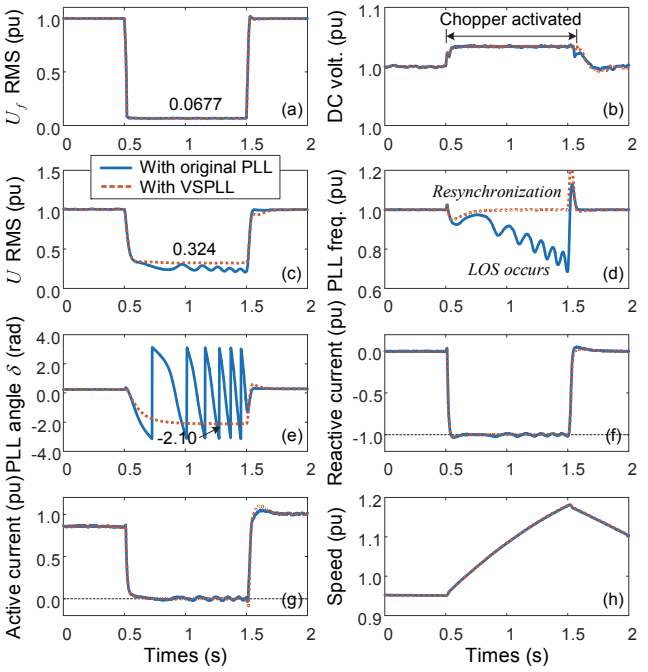

Fig. 15. Simulation result on type-4 wind turbine (2 Ω grounding resistance).

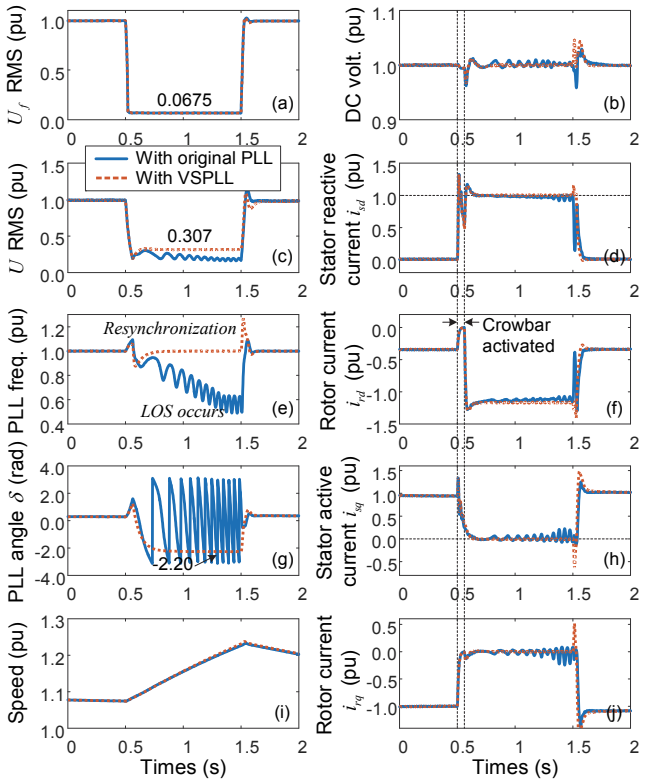

Fig. 16. Simulation result on type-3 wind turbine (2 Ω grounding resistance).

Figs. 15 and 16 display the simulation results on type-4 and type-3 wind turbines, respectively. The grid fault occurs at 0.5 s. The fault-point voltage U_f dips to about 0.0677 p.u., as shown in Fig. 15(a). The active power absorbed by machine-side converter cannot be outputted completely through grid-side converter (GSC) and hence DC-link voltage increases, as shown in Fig. 15(b). Chopper circuit is then activated to maintain the DC-link voltage within its limitation. Because of fast regulation of GSC current loop, the output currents arrive at their references rapidly, as shown in Fig. 15(f) and (g). Fig. 15(d) and (e) show PLL frequency and PLL angle, respectively, which cannot converge to their equilibrium points when the original PLL is utilized. PLL frequency fails to return to the fundamental frequency after the first swing due to insufficient accelerating area. Accordingly, the operating point enters the reverse regulation zone. The reverse regulating effect ultimately brings about the LOS event.

In contrast to the result with the original PLL, Fig. 15 displays that the resynchronization is achieved with the VSPLL method. Moreover, there is no overshoot in PLL angle, which coincides with the theoretical analysis. The grid fault is cleared at 1.5 s. Since the offset term in the normal grid condition is insignificant compared to the grid voltage, the system is able to resynchronize with the grid after grid fault clearance.

The simulation result in Fig. 16 is similar to that in Fig. 15. When the grid fault occurs, rotor current increase significantly. Rotor-side converter is rapidly blocked to protect the converter against damage. Meantime, crowbar circuit is activated to absorb the superfluous power generated by rotor winding, followed by a fierce transient process. After several cycles, rotor-side converter regains control function. During the subsequent fault-ride through process, both stator current and rotor current are regulated to track their references rapidly. From Fig. 16(e), it can be seen that the resynchronization can be achieved rapidly with the VSPLL but cannot with the original PLL.

TABLE VI
COMPARISONS BETWEEN SIMULATION AND THEORETICAL RESULTS

	Theoretical values (p.u.)	Simulation values (p.u.) and relative errors (%)			
		type-4 wind turbine		type-3 wind turbine	
U_f	0.0685	0.0677	1.2	0.0675	1.5
U	0.326	0.324	0.6	0.307	5.8
δ	–2.03	–2.10	3.45	–2.20	8.4

A steady-state comparison is made between the simulations and theoretical calculations, as shown in Table VI. The simulation on type-4 wind turbine is closer to the theoretical result than that on type-3 wind turbine. Actually, for doubly-fed induction generator, its stator active current i_{sq} is regulated by rotor-side converter to zero during riding through fault, but the current injected into grid-side converter is determined by power loss of converter. The total active current output to the grid during grid fault is not strictly zero but a small negative value. Therefore, it can be verified actual values of U_f, U, δ are smaller than their theoretical values.

B. Case B: 0.5 Ω Grounding-Resistance Fault

The grid fault in Case B is more severe than that in Case A. As predicted by the stability criterion, the resynchronization cannot be achieved in Case B since there is no stable equilibrium point (SEP). Taking type-3 wind turbine as an example, Fig. 17 shows the simulation result. Without a SEP, PLL frequency fails to converge to the fundamental frequency, even if the VSPLL method is utilized. As displayed in Fig. 17(e), PLL

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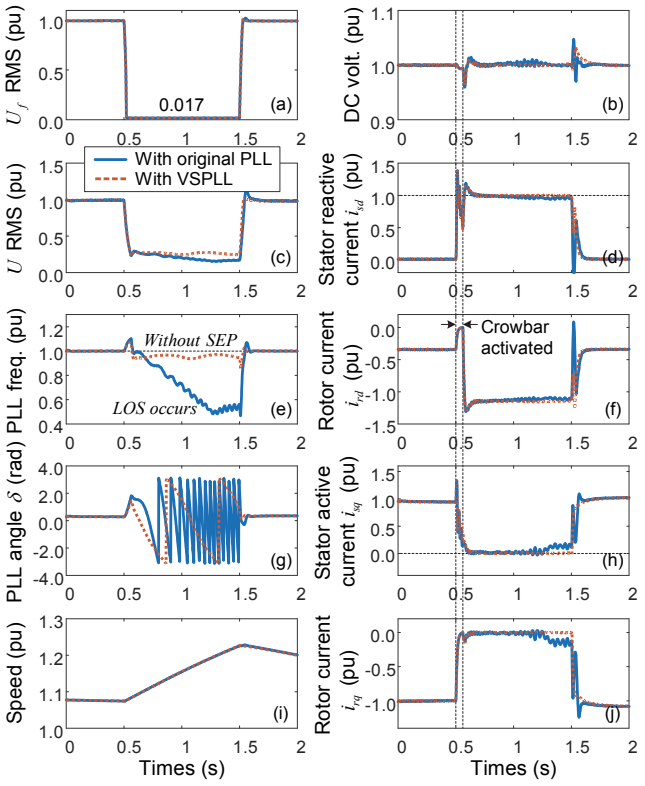

Fig. 17. Simulation result on type-3 wind turbine (0.5 Ω grounding resistance).

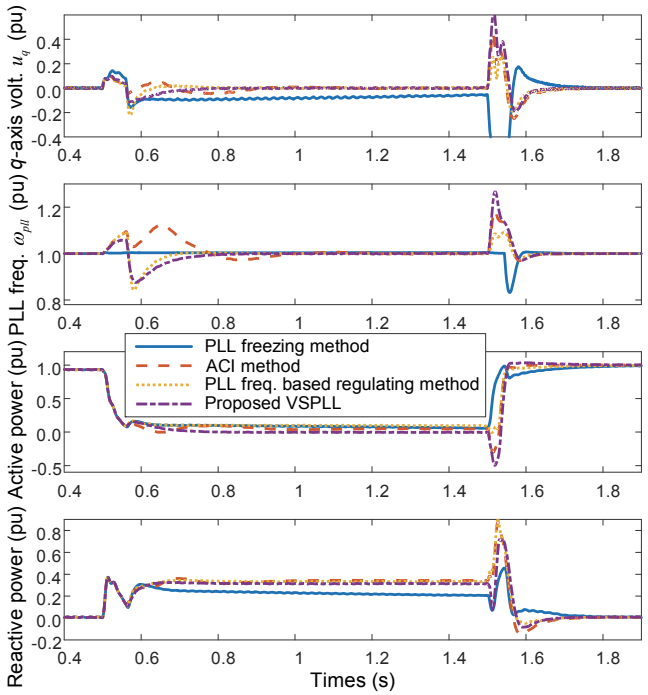

Fig. 18. Taking type-3 wind turbine as an example to compare various methods. The proposed method has the highest simplicity while showing similar performance with the second and third methods.

frequency remains oscillating and has a minor deviation to the fundamental frequency. Nonetheless, the resynchronization capability has been improved a lot compared to the original PLL. The frequency deviation could become small enough while setting a proper proportional parameter. Thus, wind turbine could successfully ride through grid faults without needing protective action to trip [7].

C. *Comparisons with Existing Methods*

In addition to the comparison made in Section IV.C in terms of principle of the existing and proposed methods, simulation comparisons are also conducted, as shown in Fig. 18. Overall, the proposed method shows similar performance compared to the ACI method and the PLL frequency based active current regulating method. All of these three methods can achieve the resynchronization. However, the proposed VSPLL is the simplest in terms of complexity.

It should be noted that the PLL freezing method has a fatal flow in terms of static error. Since PLL's regulator is frozen during grid fault period, it cannot detect the terminal voltage angle any longer. Thus, the output frequency remains unchanged and the output angle depends on the angle at the beginning time of freezing. The reactive current oriented by this wrong angle is not in line with the expected reactive current, and it may accordingly cause reactive power absorption rather than injection in some cases. Hence, the PLL freezing method has difficult in complying with existing grid codes.

In view of high simplicity and practicability, this study recommends using the VSPLL method to avoid potential LOS risks of grid-tied VSCs. Although NERC report [7] previously recommended the PLL freezing method for addressing the LOS issue, the comparison with the VSPLL indicates that the latter seems to be a better choice.

VII. Conclusions

It is important yet challenging for VSCs connected to a high-impedance weak grid to resynchronize with the grid during severe grid faults. The resynchronization analysis and improvement of VSCs were studied in this paper. A swing equation model describing the dynamics of PLL was developed and a modified equal area criterion was utilized to identify factors affecting the resynchronization. Two factors were revealed, one of which was grid-side impedance's voltage drop in the input of PLL. The other was PLL's second-order integral loop whose lag effect causes the risk of losing synchronism during dynamic process. This paper highlighted the second factor and developed a VSPLL aiming at eliminating the factor to improve the resynchronization capability. The method has been verified by experiments and simulations, and it was recommended for industrial applications due to its great simplicity and high performance.

The modeling and analysis in this paper could also be extended to multi-converter systems. This work is ongoing. Besides, the resynchronization issue of interest in this study is directed to symmetrical faults. The resynchronization issue during asymmetrical grid faults, which involves separate synchronization with positive- and negative-sequence components simultaneously, needs further research in the future.

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