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Overload and Short Circuit Protection Strategy for Voltage Source Inverter Based UPS

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***Abstract*—In this paper, an overload and short circuit protection method is proposed for voltage source inverter based Uninterruptible Power Supply (UPS) system. In order to achieve high reliability and availability of the UPS, short circuit and overload protection scheme are necessary. When overload or short circuit happens, using the proposed control method, the amplitude of the output current can be limited to a constant value, which can be set by the customer to avoid the destruction of the power converter, and to obtain a faster recovery performance as well. The detailed principle of the proposed protection method is discussed in this paper. It mainly contains three parts in the control diagram for current limit, first is the anti-windup in the voltage and current controllers, then the feedforward of the capacitor voltage to the current control loop, the last is the fast reset of the resonant part of the current controller when overcurrent happens. The procedure of developing the control method is also presented in the paper. Experimental results on a commercial UPS system are presented to verify the effectiveness of the control method.**

***Index Terms*—Uninterruptible Power Supply (UPS), short circuit, overload, overcurrent protection, voltage source inverter.**

I. INTRODUCTION

Voltage source inverters (VSIs) are widely used in a large variety of applications, such as the Uninterruptible Power Supply (UPS) system, Distributed Generation (DG) system [1], and even in the electric vehicles (EVs) [1]-[9]. A VSI usually consists several semiconductor switches, such as IGBTs. It is estimated that about 38% of the faults in a power system is due to failures of switching devices [1]. High operation reliability is always required for the power inverter based applications, especially in a high power system [1].

Therefore, the fault detection and protection system occupies an important position in the UPS. Switching devices can be broken under overcurrent condition [2]. The typical reason of the destruction of the power switches is the

overheat of the chip. This kind of failure will happen if the inverter is working under overload condition or a short circuit fault. In order to improve the reliability of a power system, the short circuit is one of the most critical situation to be considered [1], [10]-[12]. This paper will focus on the overload and short circuit protection of the voltage source inverter based UPS system. Sometimes the inverter should remain connected even under overload or short circuit condition, so a control strategy is required to limit the output current [4] - [8]. With an effective overcurrent control method, the system can return back to normal operation as soon as the fault is cleared [9], [13], [14].

There are mainly two kinds of overcurrent protections methods: hardware based methods and software based methods. [7]. Overcurrent will happen under two different faults: fault-under-load (FUL) (at output phases) or hard switching fault (HSF) [2], [4], [15], [16]. When HSF happens, the load is short-circuited before running the converter. Under this kind of short circuit fault, the increasing rate of the current is as same as the normal turn-on condition. Differ from the HSF, the FUL usually happens when the converter is already running, and typically, the FUL will cause a higher peak current than the HSF [4]. More details of detecting FUL can be found in [15], [16]. The detailed possible cases for overcurrent in a three-phase inverter is listed as below [7].

i) FUL: Inverter is working under strong overload.

ii) FUL: Single phase (asymmetrical fault) or three-phase (symmetrical) ground short circuit fault.

iii) FUL: Phase to phase short circuit between two phases (asymmetrical fault).

iv) HSF: Shoot through of any phase of the inverter.

The HSF happens mainly because of the failure of the dead time, the problem of the PWM modulation or the problem of the driver circuit. This paper will focus on the protection under the condition of the FUL.

Fast detection of overcurrent or short circuit fault is necessary to avoid the switching devices suffering from overheating and destruction [4]. Many kinds of short circuit protection methods for IGBTs have been proposed [1], [2]. It is difficult to deal with the short circuit fault since normally the switching devices will be broken in a very short time when it happens. Therefore, most of the existing IGBT short circuit detection and protection methods are hardware circuit based. Some are algorithm based. A brief review of the existing protection methods is given below.

A. Primary hardware protection

Overcurrent fuses [5], relays [17]-[20], or breakers are normally adopted for the primary hardware protection in the power systems and are considered as a backup protection method to isolate the converter from the power transmission line when overcurrent happens [5], [9], [21].

B. Driver circuit based hardware protection

Another kind of hardware protection strategy is based on the characteristic of the switching devices under different working mode [3], [22]-[26]. Typically, there will be a detection and protection logic circuit integrated into the driver circuit to turn-off the switching devices under fault condition. The common used detection or protection methods are shown below. 1) V_{CE} or V_{DS} voltage monitoring [6], [22]. 2) V_{GE} or V_{CE} voltage monitoring [26]-[29]. 3) Gate-charge monitoring [30], [31]. 4) Collector current monitoring[32]-[34].

C. Main power circuit based hardware protection or combined with modified algorithm control method

In some other literatures, the protection methods are based on modifying the main power circuit by adding auxiliary protection circuit or using different control method in the software under fault condition. The concept of the protection in [5] is using an auxiliary switch, connected along with driving circuit, between the positive rail of the DC bus capacitors and the collector/drain terminal of the upper switching transistor. The disadvantage is that the complexity of the circuit is increased given that auxiliary drive circuit need to be incorporated for switching the protecting transistor [5]. Also in [5], it proposed another protection method called linear current protection method, which contains more auxiliary switches and resistors for the protection circuit. This method will increase the cost and the volume of the system; also will increase the power loss because of the auxiliary components. In [35], it proposed a protection method based on a 12-pulse thyristor rectifier bridge to cut off the DC bus when overcurrent happens. It presented a protection method based on fuse on the DC bus in [36]. In [37], it proposed a hardware based method, which is called hardware hysteresis circuit that used to detect the fault and then limit the current; additionally, it will transfer from voltage control mode (VCM) to current control mode (CCM) once the fault happens.

D. Algorithm based overload or short circuit protection method

The overcurrent control strategy in [7] is based on generating new current reference according to a current limit function, an auxiliary control loop, and a look up table is used to store the original current reference. In [8], a current

limiting method was proposed based on a hysteresis comparator circuit and switched to current controlled mode after overcurrent happens. The main disadvantage of this control method is complexity of the auxiliary current control mode, and it has a longer response time as the authors mentioned in [8], and it need to design a hysteresis comparator circuit for each phase. In [38], it proposed a protection method called triple-loop short circuit limiter. However, from the simulation and experimental result, the limited output current value was not accurate and the recover after fault clearance was slow. In [39], it proposed a protection method based on virtual impedance, it has the same problem as [38], and it is not effectiveness for short circuit fault since it is not discussed in [39]. Similar to [7], a current limiting method based on a lookup table was proposed in [40] for a single phase inverter. The difference is that it will generate new voltage reference other than current reference when overload happens to decrease the output voltage, thus to limit the output current. The drawback is that it does not provide a fixed limited current when different level of overload happens, then it cannot guarantee the safety of the system. Moreover, it does not provide short circuit protection capability. In [41], two kinds of interesting short circuit protection methods were proposed, which are only algorithm based. However, there are problems with both of the two methods. More details about it are described in Section II.B when compare to the proposed method in this paper.

Some other short circuit protection methods are presented in [42]-[43]. The inverter will change to CCM from VCM when short circuit happens. This kind of methods are highly rely on the fault detection algorithm. The switch of the two modes cannot be instantaneous if there is delay in the detection or after the fault is cleared. In addition, it will occupy more resources in the controller since it must provide two kinds of operation modes, VCM and CCM, which will increase the cost of a system when choosing a higher-level controller.

In this paper, an algorithm based overcurrent protection method for power inverters is proposed, which is suitable for both overload and short circuit conditions at output phases. The control strategy contains some basic technologies, such as the anti-windup loop in the PR controller and the voltage feedforward control, but it is not enough to have a fast and accurate overcurrent protection. The reset of the resonant regulator has been added in the control when overcurrent happens. The key point is that we found that all of these three parts are necessary to obtain a satisfying overcurrent protection performance. It is easy to implement into the existing inverter control scheme by just adding some lines in the code. Compared with the abovementioned protection methods, it does not need auxiliary circuit, sensors or changing of control logic with only VCM. Therefore, it is suitable for high power application design to

decrease the cost and increase the power density as well. In addition, the protection logic is not to shut down the system immediately when overload or short circuit happens. It intends to limit the output current to a preset constant value inside the SOA of the switching devices during a period of time, which is an important point to evaluate the reliability and availability of a UPS system, especially when a critical load is supplied. More details of the proposed method is presented in Section II.

The rest of this paper is organized as below: in Section II, the proposed protection method is discussed in detail, and the analysis is presented; in Section III, the experimental results are provided; then the conclusion is given in IV.

II. The Proposed Protection Method

The proposed overload and short circuit protection method is algorithm based. In the control scheme, an output voltage feedforward loop is added, and when overcurrent happens, no matter it is because of overload or short circuit at the output phases, the output of the resonant part of the current controller will be reset to zero, which will prevent the output currents exceed the limited value. The using of the output voltage feedforward will give a fast response of the protection progress by suppressing the effect of the capacitor voltage. In addition, anti-windup loop is also added in the resonant controller, which is also needed for a fast and accurate current limit when overload or short circuit happens. Analysis and more details about the protection control scheme will be discussed below.

A. The control scheme

For a three-phase UPS system, the output is typically organized to be able to work with single phase or three phases to make it suitable for different kinds of loads, at the same time to have a more flexible system. So in this paper the control is under *abc* stationary coordinates frame, which is more convenient to test the effectiveness of the control strategy phase by phase or three-phase together.

Fig. 1 shows the topology of the NPC three-phase three-level inverter with an LC filter at the output side. Fig. 2 shows the control scheme used in this paper. Conventionally, the anti-windup loops are added in the voltage and current PR controllers to avoid the windup possibility of the resonate controller. However, based on this kind of control, it is not enough to have a great performance of overload and short circuit protection. In the proposed control scheme, in order to have a fast and accurate current limit under overload or short circuit conditions, if the output current exceeds the limited value, the resonant part of the PR controller in current control loop will be reset to zero. Additionally, compared with the conventional voltage and current control loops, the filter capacitor voltage V_c is feedforward to the

output of the current control loop. With the coordination of the three parts in the control scheme, which are the anti-windup loops in the voltage and current controllers, the capacitor voltage feedforward control and the reset of the resonant part of the current controller when overcurrent happens, a fast and accurate current limit performance can be obtained. By the feedforward of the capacitor voltage, when overcurrent happens, especially under short circuit condition, one can suppress the influence of the capacitor voltage to the output current. The reset of the resonator of the current controller can reduce the modulation waveform quickly to the limited value to avoid the inverter going into uncontrollable condition or the overshoot of the current. Each of the three parts plays an important role for the current limit under overload or short circuit condition.

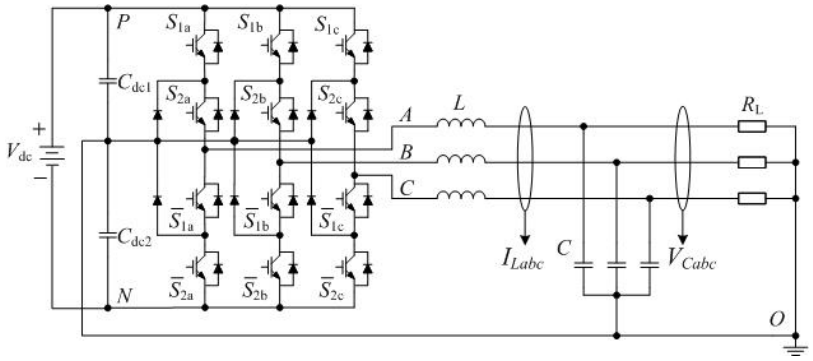


Fig. 1. Topology of the NPC inverter.

Fig. 3 shows the simplified linear control model for the voltage inverter in the UPS. In which, $G_V(s)$ represents the transfer function of the voltage controller; $G_I(s)$ represents the transfer function of the current controller, and $G_{PWM}(s)$ represents the transfer function of the inverter. Defining that:

$$G_V(s) = K_{PV} + \frac{K_{RV}s}{s^2+\omega^2},\ G_I(s) = K_{PI} + \frac{K_{RI}s}{s^2+\omega^2},\ G_{PWM}(s) = K_{PWM}\frac{1}{1+1.5T_s} \tag{1}$$

where K_{PV} and K_{RV} are the proportional and resonate coefficients of the voltage PR controller, respectively; K_{PI} and K_{RI} are the proportional and resonate coefficients of the current PR controller, respectively; and for the three-level voltage source inverter, the gain K_{PWM} equals to $V_{dc}/2$. Moreover, in order to suppress the influence of the fluctuation of the DC bus voltage, the DC bus voltage will always be considered in the control, the PWM signal will be divided by $V_{dc}/2$ before sending to the driver circuit. So that the gain of the path from the output of the current controller to the inverter output, from the point PWM^* to the point $V_{XO}(s)$ (X=A, B, C) in Fig.2, will be one. Accordingly, a unit feedforward control is applied in this paper, $F(s)$=1.

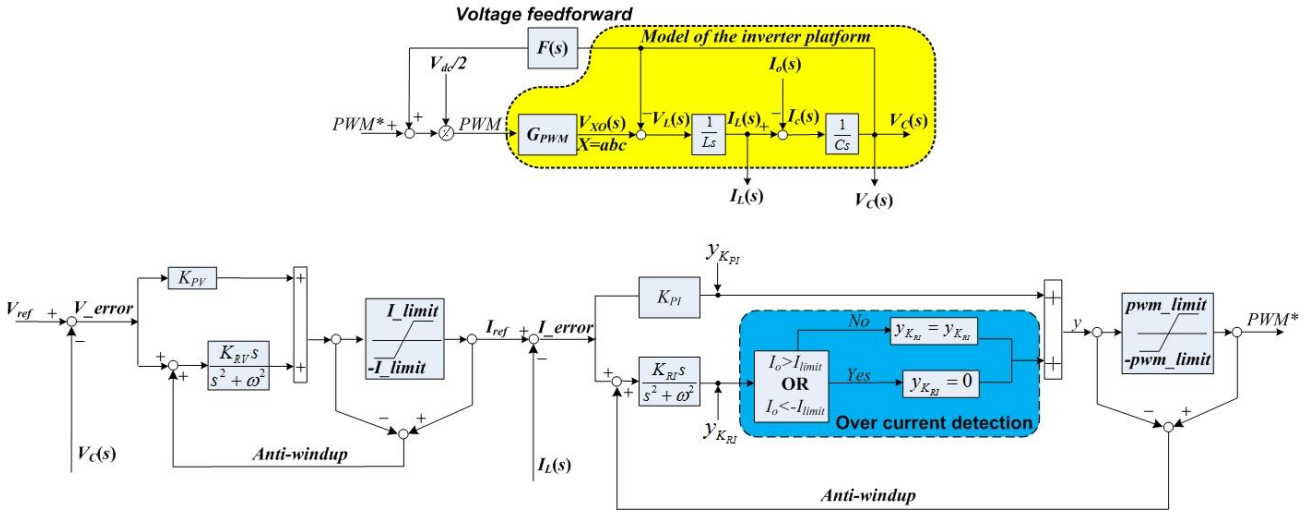


Fig. 2. The control diagram considering overload and short circuit protection.

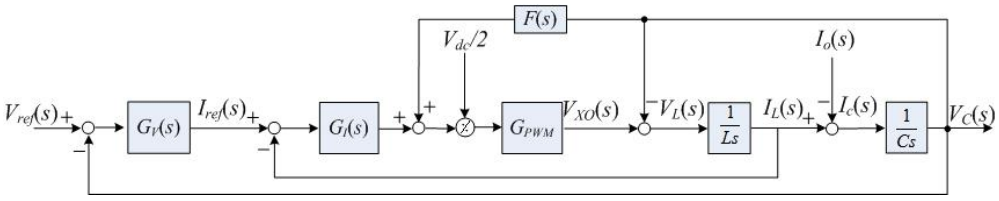


Fig. 3. A simplified linear model of the control.

B. The analysis of the overload and short circuit protection method

It is necessary to analyze the PR controller for explaining the proposed control method since it plays an important part in the control. The diagram of the general PR controller is shown in Fig.4. The transfer function of the PR controller is shown below.

$$G_{PR}(s) = K_P + \frac{K_R s}{s^2 + \omega^2} \tag{2}$$

Considering an input error signal of same frequency with the PR like $u_{error}(t) = M\sin(\omega t + \varphi)$, the Laplace transform of $U_{error}(t)$ is:

$$u_{error}(s) = \mathscr{L}[M\sin(\omega t + \varphi)] = \mathscr{L}[M\sin(\omega t)\cos\varphi + M\cos(\omega t)\sin\varphi] = M(\cos\varphi)\frac{\omega}{s^2+\omega^2} + M(\sin\varphi)\frac{s}{s^2+\omega^2} \tag{3}$$

After the resonant part of the PR controller, see $y_{KR}(s)$ in Fig.4 and applying (3), it yields to:

$$y_{K_R}(s) = K_R M\left\{\cos\varphi\frac{\omega s}{(s^2+\omega^2)^2} + \frac{\sin\varphi}{2}\left[\frac{s^2-\omega^2}{(s^2+\omega^2)^2} + \frac{1}{(s^2+\omega^2)}\right]\right\} \tag{4}.$$

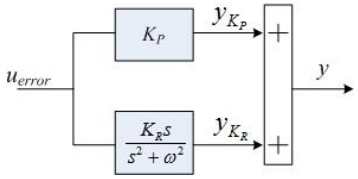


Fig. 4. Control diagram of the PR controller.

By using reverse Laplace transform of (4), it gives as following:

$$y_{K_R}(t) = [M(\cos\varphi)\frac{\omega}{s^2+\omega^2} + M(\sin\varphi)\frac{s}{s^2+\omega^2}]\frac{K_R s}{s^2+\omega_0^2} = K_R M\left\{\frac{\cos\varphi}{2}t\sin(\omega t) + \frac{\sin\varphi}{2}[t\cos(\omega t) + \frac{1}{\omega}\sin(\omega t)]\right\} \quad (5).$$

Take two different values of φ as examples to analyze the output of resonant controller. When $\varphi = 0^o$, the output signal would be:

$$y_{K_R}(t) = K_R M\left\{\frac{\cos\varphi}{2}t\sin(\omega t) + \frac{\sin\varphi}{2}[t\cos(\omega t) + \frac{1}{\omega}\sin(\omega t)]\right\} = \frac{K_R M}{2}t\sin(\omega t) \quad (6)$$

when $\varphi = 90^o$, the output signal would be:

$$y_{K_R}(t) = K_R M\left\{\frac{\cos\varphi}{2}t\sin(\omega t) + \frac{\sin\varphi}{2}[t\cos(\omega t) + \frac{1}{\omega}\sin(\omega t)]\right\} = \frac{K_R M}{2}[t\cos(\omega t) + \frac{1}{\omega}\sin(\omega t)] \quad (7)$$

It can be noticed that the output increases with time until the input signal is zero, when adopted in a control architecture, the final value of the resonant controller will be a constant with a zero steady state error if the controller is well tuned. The resonant controller operates when an error signal is present. In addition, it can be noticed that the resonant controller only work with a non-zero input signal. It means that the output of the resonant controller will continue accumulate with the error signal over time. Therefore, a small error can become a large correction if given enough time. As the error is accumulated, the system will be forced to correct the error until the steady state error is zero. However, overshoot on the controlled signal always happens with an integral or resonant controller. To evaluate the effectiveness of a controller in a control diagram, some tools can be applied.

Step response is often implemented to verify the effectiveness and stability of a control scheme [44]-[49]. Fast dynamic response is necessary for a power system, and it can reduce the deviation of output voltage or current during the transient event with effective control [44]. The unit step response is widely implemented in the power electrical system, it is the time behavior of the output of the system when the input changes from 0 p.u. to 1 p.u. in a short time but within the rated power of a system [50].

From a practical standpoint, knowing how the system responds to a sudden input is important because large and possibly fast deviations from the long-term steady state may have extreme effects on the controller and on other portions of the overall system dependent on this controller. In addition, the overall system cannot act until the controller's output settles down to some vicinity of its final state, delaying the overall system response. Formally, knowing the step response of a dynamical system gives information on the stability of such a system, and on its ability to reach one stationary state when starting from another operation point [50].

Normally, three useful information we can get from the step response of a system: overshoot value, settling time and

status at steady state. When overload or short-circuit happens, the system will go into a new operation point, from the load side point of view, it is like a serious load step change, more current need to be provided from the converter side. To protect the hardware, we need to focus on these three aspects as well: to lower the overshoot, to decrease the settling time from overshoot to steady state, to have an accurate current limit value at steady state. Thus, from step response analysis of the control strategy, it guides us a way to improve the control.

Three different control configurations are considered to analyze the behavior of the step response of the control architecture:

Case1: using only proportional controller K_{PI} in the current control loop with the V_C feedforward control, the close loop transfer function of the current control loop is:

$$I_L(s) = \frac{G_I(s)\dfrac{1}{Ls+rL}}{1+G_I(s)\dfrac{1}{Ls+rL}} I_{ref}(s) = \frac{K_{PI}}{Ls+rL+K_{PI}} I_{ref}(s) \tag{8}$$

Case 2: using PR controller in the current control loop without the V_C feedforward control, the close loop transfer function of the current control loop is:

$$\begin{aligned} I_L(s) &= \frac{G_I(s)\dfrac{1}{Ls+rL}}{1+G_I(s)\dfrac{1}{Ls+rL}} I_{ref}(s) - \frac{\dfrac{1}{Ls+rL}}{1+G_I(s)\dfrac{1}{Ls+rL}} V_C(s) \\ &= \frac{K_{PI}s^2 + K_{RI}s + K_{PI}{\omega_o}^2}{Ls^3 + (K_{PI}+rL)s^2 + ({\omega_o}^2 L + K_{RI})s + (K_{PI}+rL){\omega_o}^2} I_{ref}(s) - \frac{s^2+\omega^2}{Ls^3 + (K_{PI}+rL)s^2 + ({\omega_o}^2 L + K_{RI})s + (K_{PI}+rL){\omega_o}^2} V_C(s) \end{aligned} \tag{9}$$

where $V_C(s) = \dfrac{I_L(s) - I_o(s)}{Cs}$, accordingly, one can obtain:

$$\begin{aligned} I_L(s) = &\frac{K_{PI}Cs^3 + K_{RI}Cs^2 + K_{PI}{\omega_o}^2 Cs}{LCs^4 + K_{PI}Cs^3 + [({\omega_o}^2 L + K_{RI})C + 1]s^2 + K_{PI}{\omega_o}^2 Cs + {\omega_o}^2} I_{ref}(s) \\ &+ \frac{s^2 + {\omega_o}^2}{LCs^4 + (K_{PI}+rL)Cs^3 + [({\omega_o}^2 L + K_{RI})C + 1]s^2 + (K_{PI}+rL){\omega_o}^2 Cs + {\omega_o}^2} I_o(s) \end{aligned} \tag{10}$$

In (9), it is clearly showing that, without V_C feedforward control, the influence of the capacitor voltage to the inductor current cannot be eliminated. In (10), the term $I_o(s)$ can be seen as an external interrupt.

Case 3: in order to decoupling the capacitor voltage $V_C(s)$ and the inductor current $I_L(s)$, V_C feedforward control is added into the current control loop, then the close loop transfer function of the current control loop will be:

$$I_L(s) = \frac{G_I(s)\dfrac{1}{Ls+rL}}{1+G_I(s)\dfrac{1}{Ls+rL}} I_{ref}(s) = \frac{K_{PI}s^2 + K_{RI}s + K_{PI}{\omega_o}^2}{Ls^3 + (K_{PI}+rL)s^2 + ({\omega_o}^2 L + K_{RI})s + (K_{PI}+rL){\omega_o}^2} I_{ref}(s) \tag{11}$$

In (11), it can be noticed that the influence from the capacitor voltage to the inductor current is eliminated.

The unit step response analysis using Matlab for the abovementioned three cases, the result is shown in Fig.5 using the parameters shown in Table I. It can be noticed that without the V_C feedforward control in case 2, there is a big overshoot at the very beginning, and the waveform oscillated with time at steady state. It could be foreseen that without V_C feedforward control, when serious overload or short circuit happens, there would be a giant overshoot in the output current, and it will oscillate at steady state. However, with V_C feedforward in case 3, the performance of both overshoot suppression and settling time can be improved. In addition, one important discovery is that if V_C feedforward is applied with only P controller as shown in Case 1, there is no overshoot in the output, which makes clear that the behavior of the resonant controller causes the overshoot.

Thus from Case 1, a very positive hint to additional improve the performance of overcurrent protection, resetting the output of the resonator of current controller to zero when overcurrent happens, which can prevent the current going into uncontrollable state.

TABLE I
Parameters of the controllers and hardware circuits in the experiments

Coefficient	Parameters	Value
Fundamental frequency	ω_o	314 rad/s
Filter capacitor	C_f	60μF
Filter inductor	L_f	200μH
Equivalent series resistance (ESR) of filter inductor	rL	0.06Ω
Proportional part of the voltage controller	K_{PV}	0.8 A/V
Resonant part of the voltage controller	K_{RV}	1000 As/V
Proportional part of the current controller	K_{PI}	1.25 V/A
Resonant part of the current controller	K_{RI}	600 Vs/A
Preset current amplitude limit value	I_{limit}	20A
Nominal output voltage	V_{ref}	230Vrms
Switching frequency	f_s	20kHz
Digital signal processer (DSP)	--	TMS320F28377D

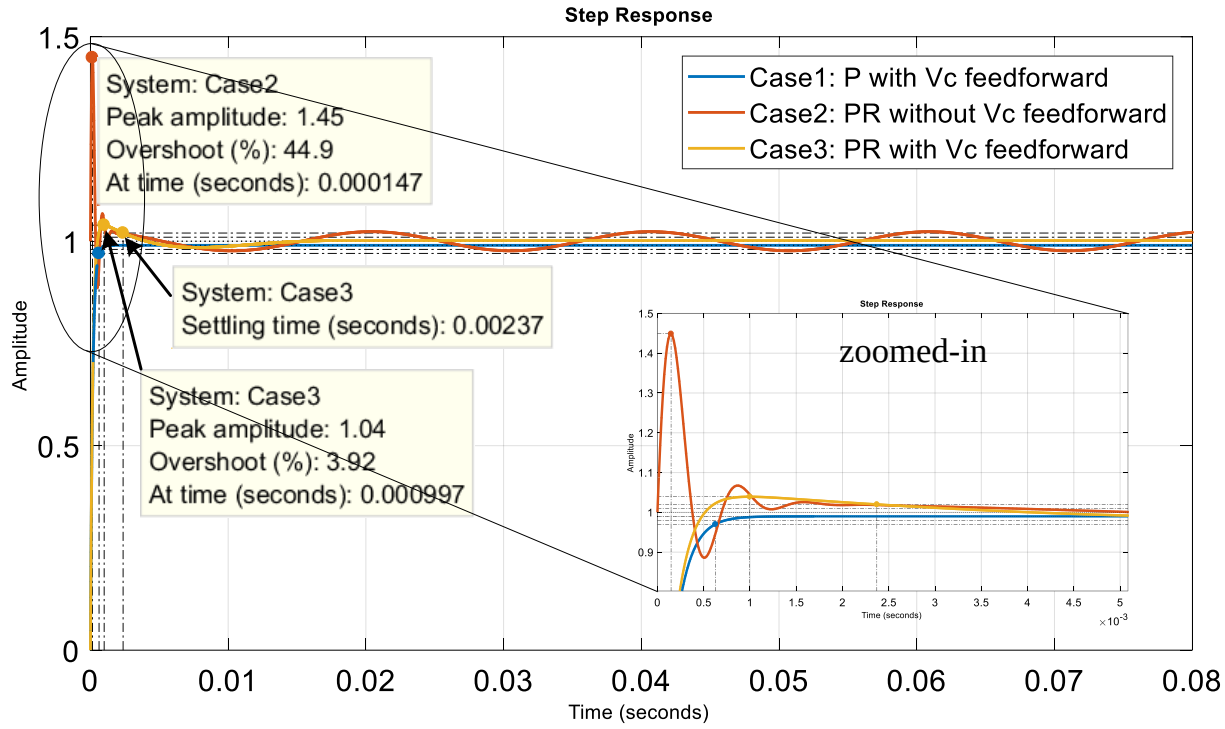


Fig. 5. Step response of different control configurations.

The overshoot is caused by the rapid accumulation of error. This large error is accumulated by the general integrator. This is called “integral wind-up”. So anti-windup loop is often adopted with the PI or PR controller to suppress the influence of the windup. Assume that an error exists, the resonator will accumulate this error over time. Therefore, the output of the accumulator slowly rises. The overshoot is exacerbated by high resonant gain. Unfortunately, the effect is also observed with low gains. The system may or may not settle at the set point. The operation of the resonator may be improved by disabling the accumulation action if the output voltage is above a particular point. Therefore, a fast reset the output of the resonant controller is essential when overload or short circuit happens.

As a conclusion of the proposed control scheme for a fast overload and short circuit protection, it mainly contains three parts: the anti-windup loop in the PR controller, the output voltage feedforward control, and the fast reset of resonant controller of current control loop. Each part plays an important role for a quick dynamic response when overload or short circuit happens.

Compares to the methods in [40]-[43], when applying the method in this paper, the healthy phase will not be influenced by the fault phase, and the phase angle of both voltage and current will not be changed, only the current amplitude is limited to a preset value. In addition, the proposed method in this paper is capable for both overload, phase to ground short circuit and phase to phase short circuit faults, while it only discussed one of them in other papers.

Among the algorithm based methods, the methods that proposed in [41] can provide overload protection, and phase to ground short circuit protection but without phase to phase short circuit protection, which is used to compare with the method in this paper. A table is provided in [41] to show the performance of the two methods, which is extended to compare with the presented method in this paper that is shown in Table II. From the table, it can be noticed that even the healthy phase will be influenced when fault happens, and the current limited value is not accurate, it varies under different cases. Simulation and experimental results that provided in [41] show the phenomenon as well. When applying the method in this paper, the healthy phase will not be influenced by the fault phase. In addition, the phase angle of both voltage and current will not be changed, only the current amplitude is limited to a preset value, which is fixed and accurate. It is only depend on different preset values for different rated power of UPS systems. The healthy phase will not be influence by the fault phase as well when asymmetric overload or phase to phase short circuit happens, which is not shown in the table. In addition, the method in this paper is valid for the three kinds of over current fault, while the methods in [41] are only valid for two of them.

Table II Comparison with the methods in [41]

Items \ Methods		Method I in [41]	Method II in [41]	Method in this paper
Output current	Healthy phase	zero	pre-fault current	pre-fault current, will not be influenced by fault phase
	Fault phase	The current limiting references with reverse phase angle and required current limiting magnitude, varies current limit value under different cases, $\sqrt{3}$ I_{limit}, $2I_{limit}$ or between the range [I_{limit}, $\sqrt{3}$ I_{limit}]	The current limiting references with regulated phase angle and required current limiting magnitude, varies current limit value under different cases, $\sqrt{3}$ I_{limit}, $2I_{limit}$ or between the range [I_{limit}, $\sqrt{3}$ I_{limit}]	Limited amplitude without changing the phase angle. Limited to the preset value according to the customers' application.
Output voltage	Healthy phase	zero	86.6% of rated voltage (phase angle changed as shown in [41]	Rated voltage without changing the phase angle
	Fault phase	zero	zero	zero
Valid for fault types		Overload, phase to ground short cirvuit	Overload, phase to ground short cirvuit	Overload, phase to ground short circuit, phase to phase short circuit

III. Experimental Results

In order to verify the effectiveness of the proposed overload and short circuit protection method for three phase voltage source inverters, experiments have been developed by the real UPS system in Salicru S.A. Three cases of FUL

that cause overcurrent conditions mentioned in the introduction were considered: i) overload, ii) phase to ground short circuit, and iii) phase to phase short circuit. The configuration of the control and platform is shown in Table I. Fig. 6 shows the NPC three-phase three-level inverter based UPS platform. Parameters of the filters and controllers are shown in Table I.

Fig. 6. The prototype of the NPC three-phase three-level topology based UPS platform.

Fig. 7 shows the waveform of normal working condition. Sinusoidal waveform of output voltage is obtained, which is the basic requirement of a UPS system. Fig. 8 shows the waveform when overload happens. It can be seen that when a strong load, which is beyond the limit, was suddenly connected to the inverter, the output current will be limited to the preset constant value. Under unknown overload condition, the output current is still controllable to avoid damage of the load and the UPS itself. The other phenomenon that should be mentioned is that the UPS system will not be shut down when overload happens, it is necessary for some of critical loads, such as telecommunication systems, network servers, database system, and medical equipment.

Fig. 9 and Fig. 10 depict the waveforms when the UPS transfer from normal working condition to overload condition. It is clearly showing the reset operation of the resonant regulator of the current controller in the DSP when overload happens, which shows the same phenomenon of the simulation results. In addition, it shows an accurate current limit performance since the current is limited to the preset value of 20A. The waveform looks good during the transient time

that demonstrate a good performance of the presented current limit control scheme.

Fig. 11 and Fig. 12 give the experimental results when phase to ground short circuit fault happens. It shows the dynamic performance of the cases from normal to short circuit and the reverse. The output current can be limited to the preset value quickly and went back to normal operation when the fault was cleared as expected.

Fig. 13 shows the results when the UPS operated under normal working condition with three-phase load. Fig. 14 and Fig. 15 depict the waveforms when symmetric overload happens in three phases. It is a serious case from no load to overload condition directly; however the current can still be limited to the preset value quickly and accurately by using the proposed method. It shows the effectiveness of the presented control method. It should be noticed that the results of Phase C was not shown in the experimental results since there are no more channels on one oscilloscope. Fig. 16 to Fig. 18 are the experimental results when phase to phase short circuit fault happens. It can be noticed that the fault happened on the two phases will not influence the normal operation of the other healthy phase, and it can go back to normal operation quickly when the fault was cleared, very similar results are obtained as shown in the simulation. The consistency of the simulation and experimental results further shows the effectiveness and the availability of the proposed method.

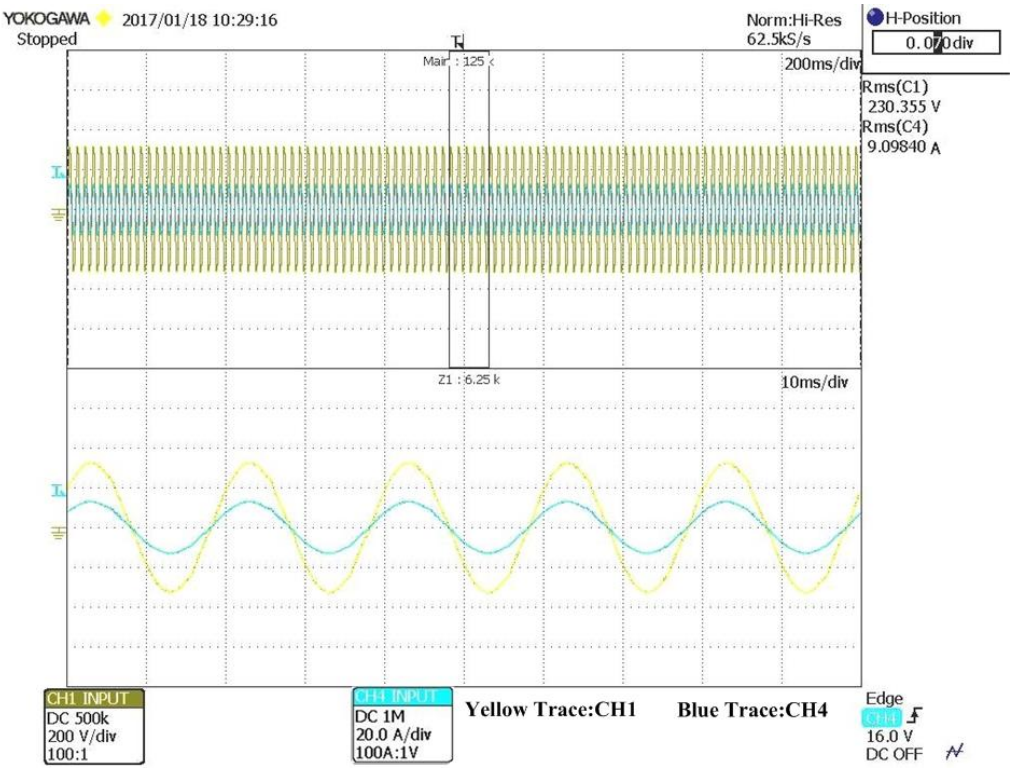


Fig. 7. Normal operation with single-phase load, CH1: Output voltage; CH4: Output current.

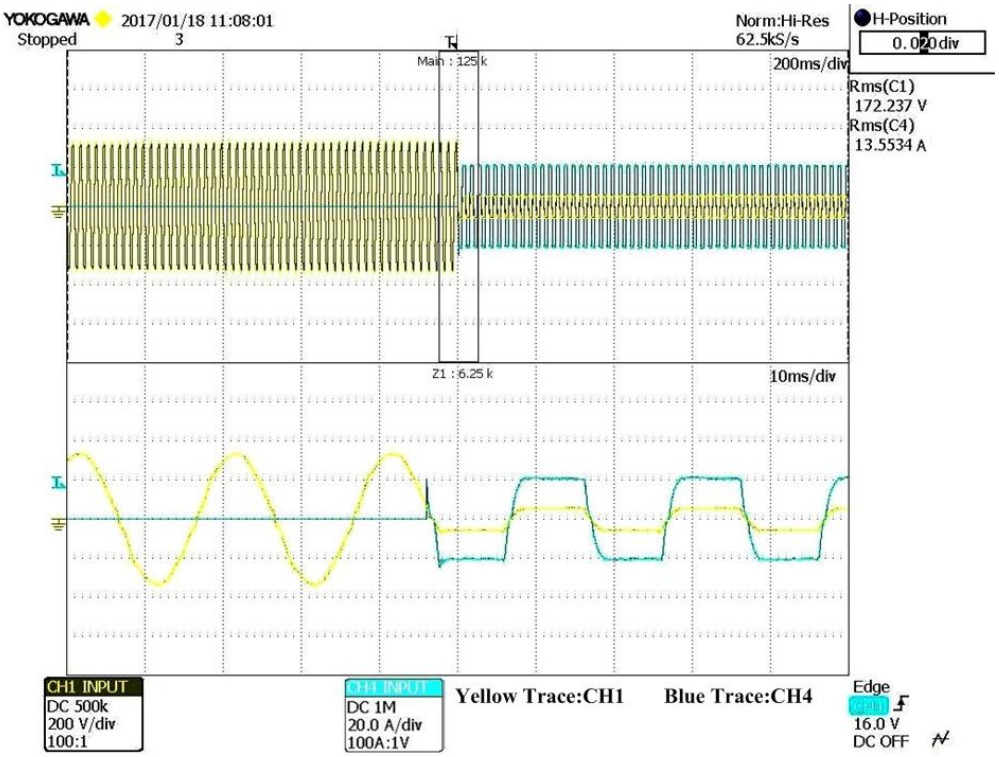


Fig. 8. Overload happens with single-phase load, CH1: Output voltage; CH4: Output current.

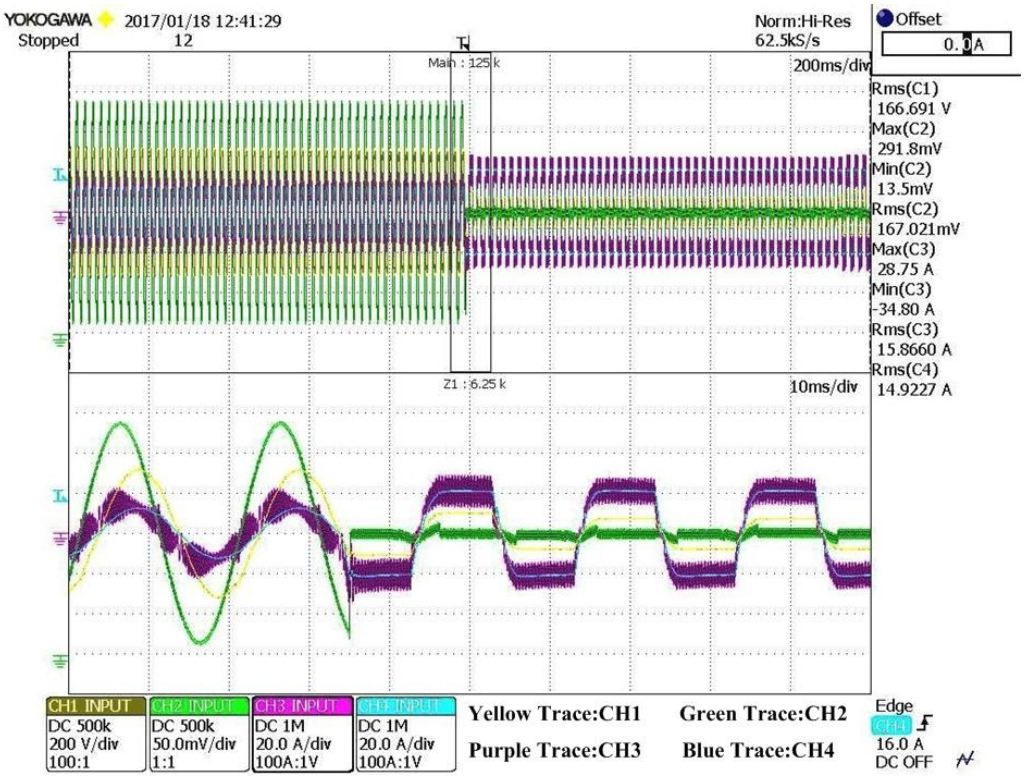


Fig. 9. Single phase from normal to overload condition, CH1: Output voltage; CH2: Resonant output of current controller in DSP; CH3: Inductor current; CH4: Output current.

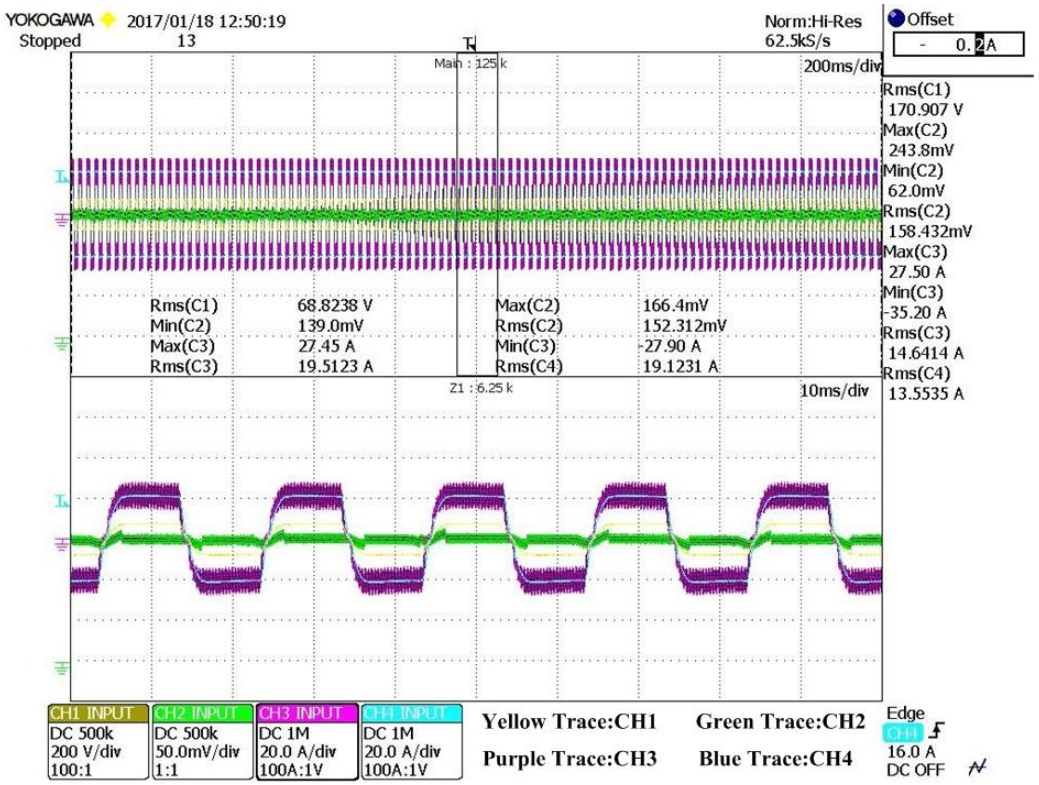


Fig. 10. Overload happens with single-phase load, CH1: Output voltage; CH2: Resonant output of current controller in DSP; CH3: Inductor current; CH4: Output current.

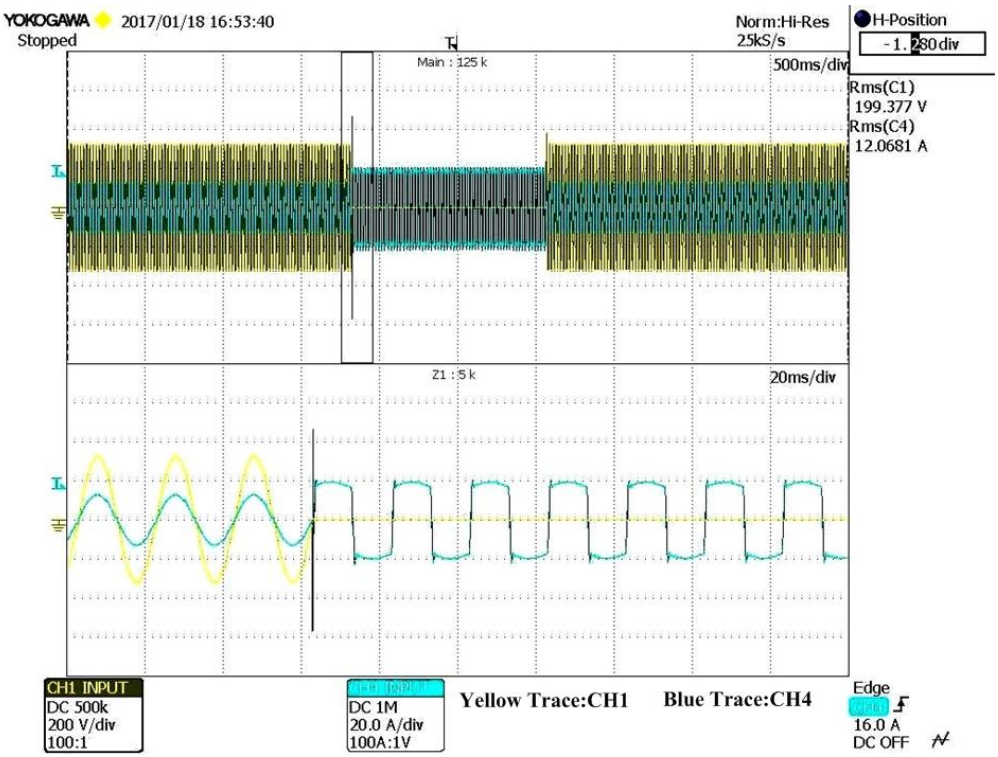


Fig. 11. Single phase from normal to phase to ground short circuit, CH1: Output voltage; CH4: Output current.

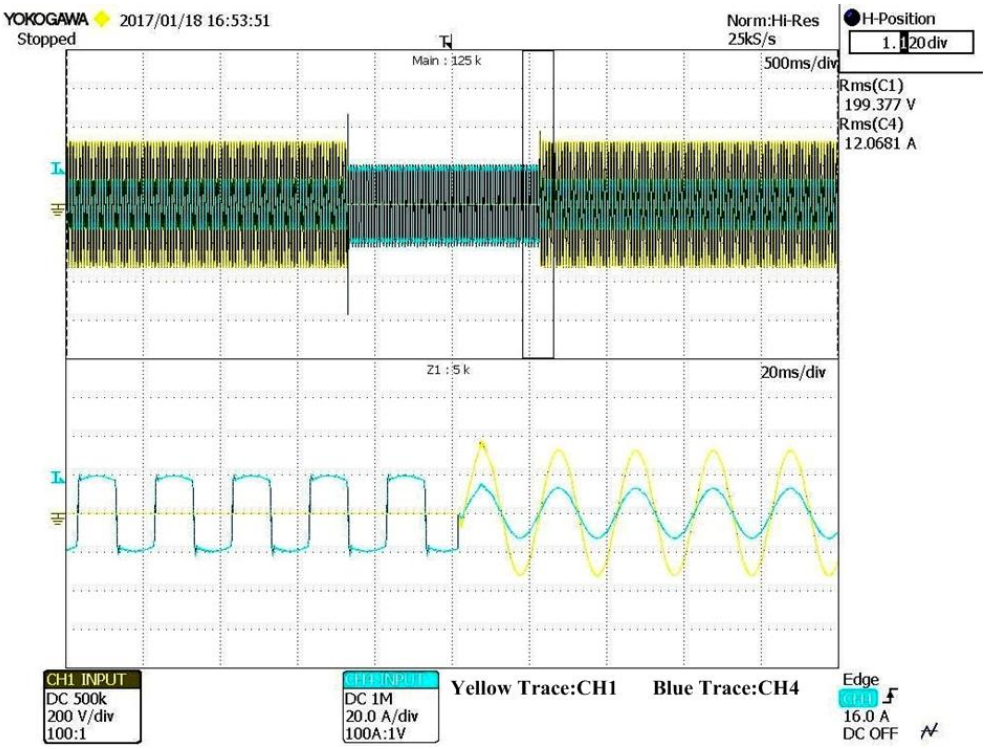


Fig. 12. Phase to ground short circuit condition switch to normal working condition on single-phase, CH1: Output voltage; CH4: Output current.

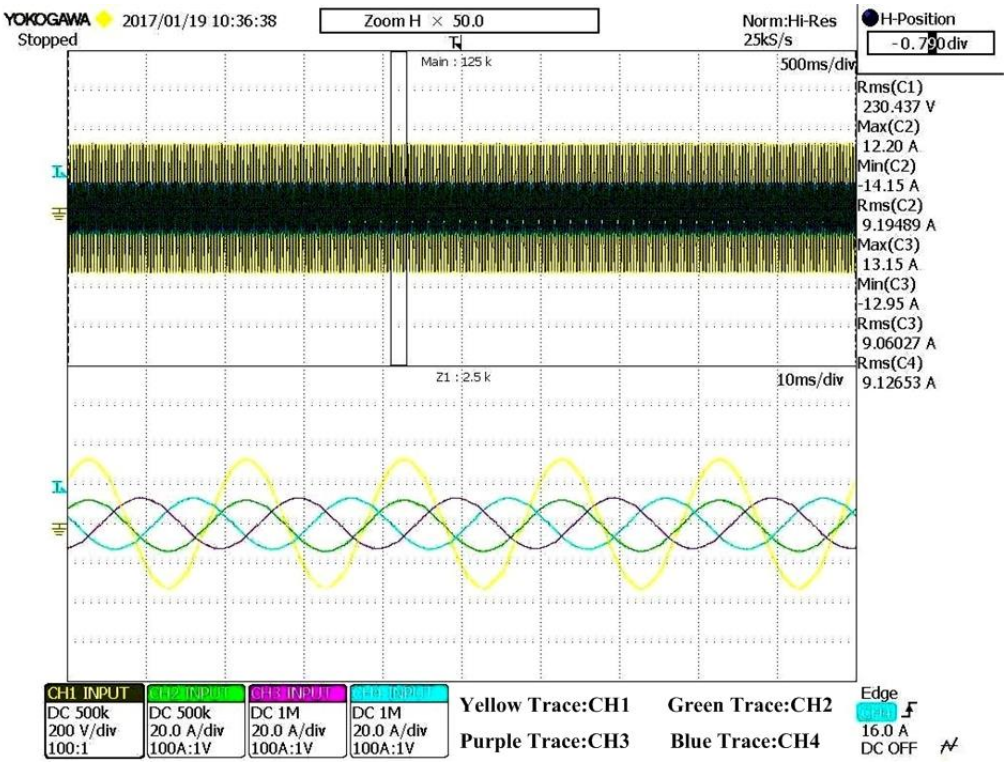


Fig. 13. Three-phase load normal working condition, CH1: Phase A output voltage; CH2: Phase A output current; CH3: Phase B output current; CH4: Phase C output current.

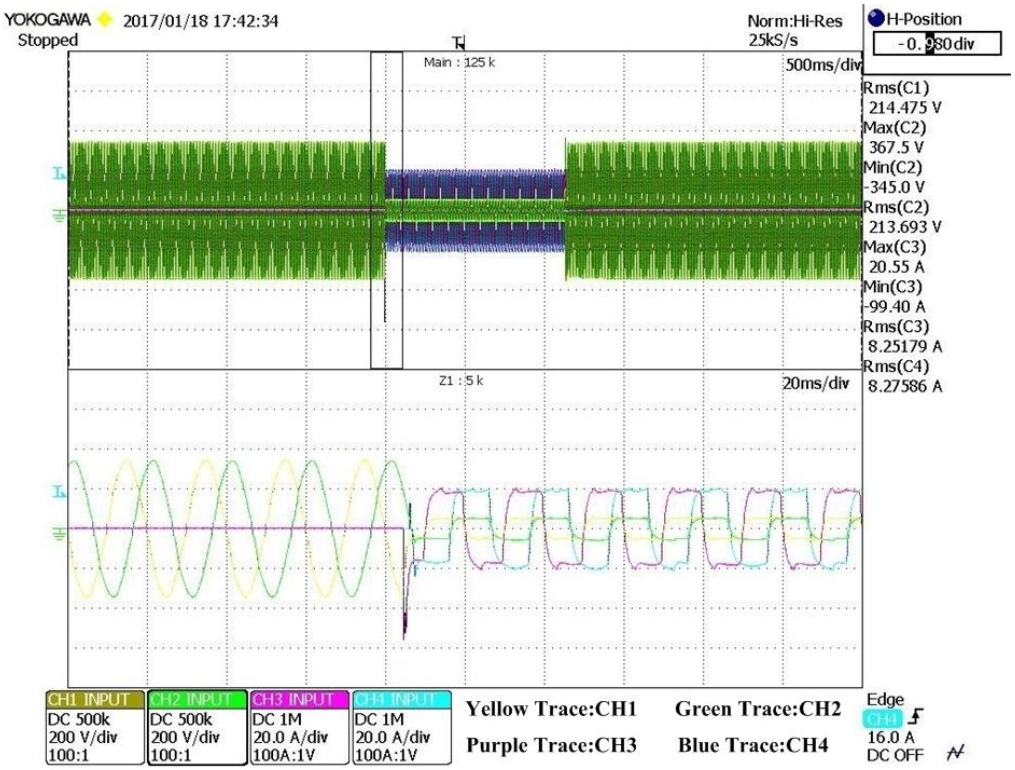


Fig. 14. Overload happens with three-phase load, CH1: Phase A output voltage; CH2: Phase B output voltage; CH3: Phase A output current; CH4: Phase B output current.

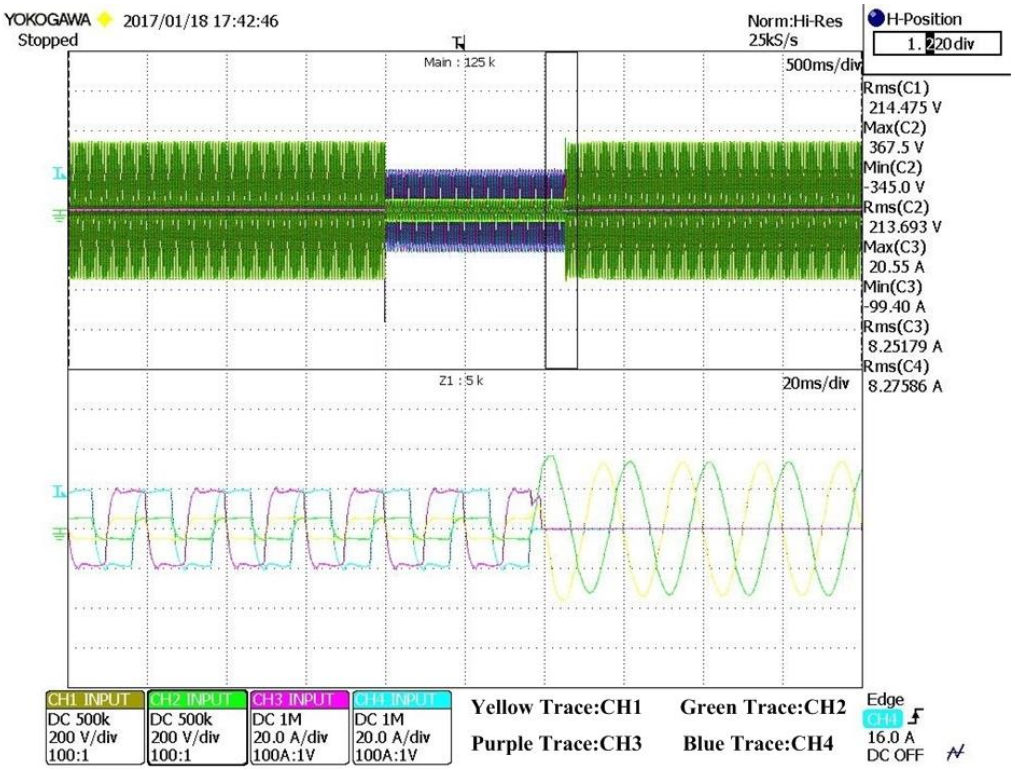


Fig. 15. Three-phase overload switch to no load condition, CH1: Phase A output voltage; CH2: Phase B output voltage; CH3: Phase A output current; CH4: Phase B output current.

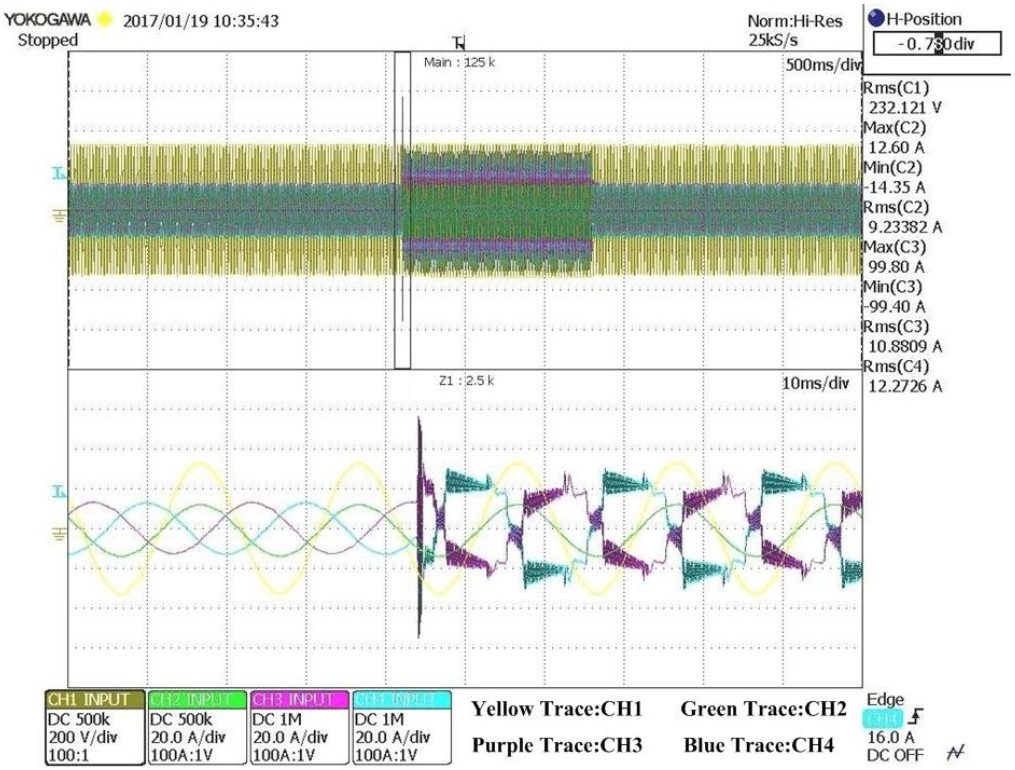


Fig. 16. Normal operation to phase to phase short circuit, CH1: Phase A output voltage; CH2: Phase A output current; CH3: Phase B output current; CH4: Phase C output current.

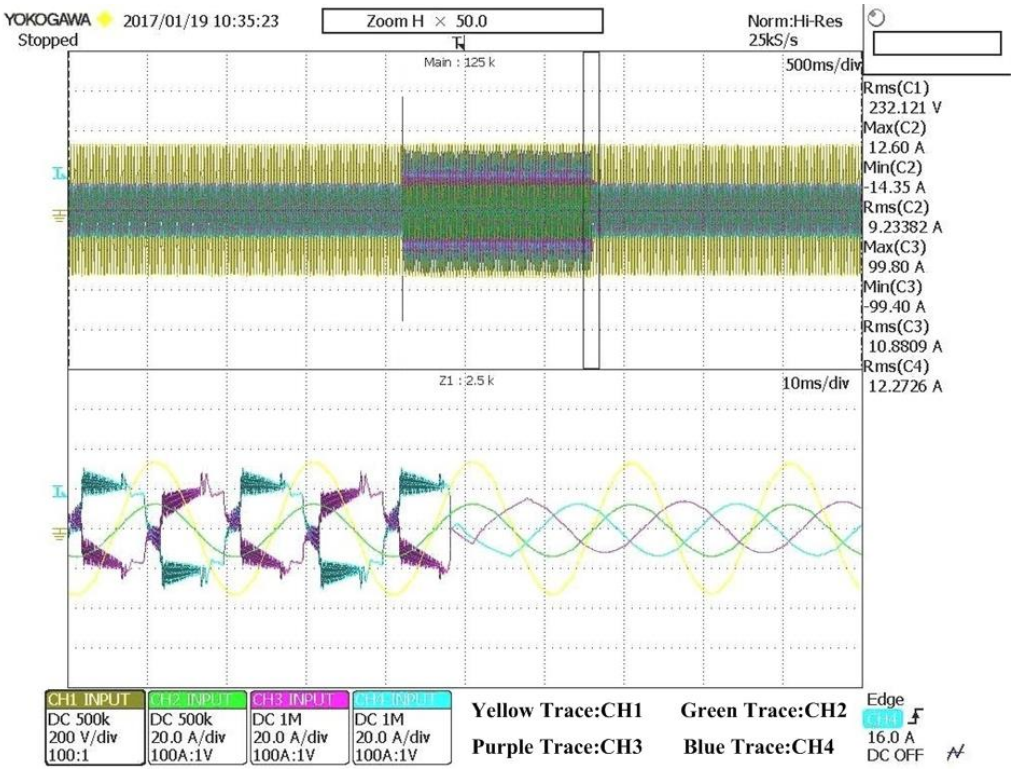


Fig. 17. Phase to phase short circuit to normal operation, CH1: Phase A output voltage; CH2: Phase A output current; CH3: Phase B output current; CH4: Phase C output current.

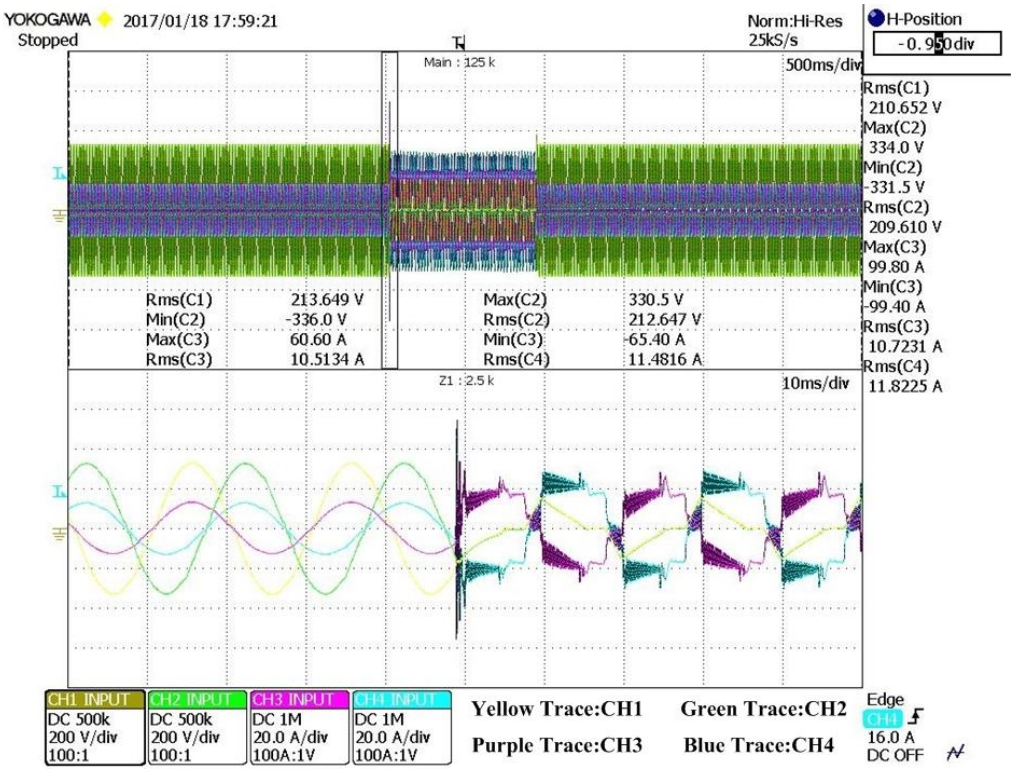
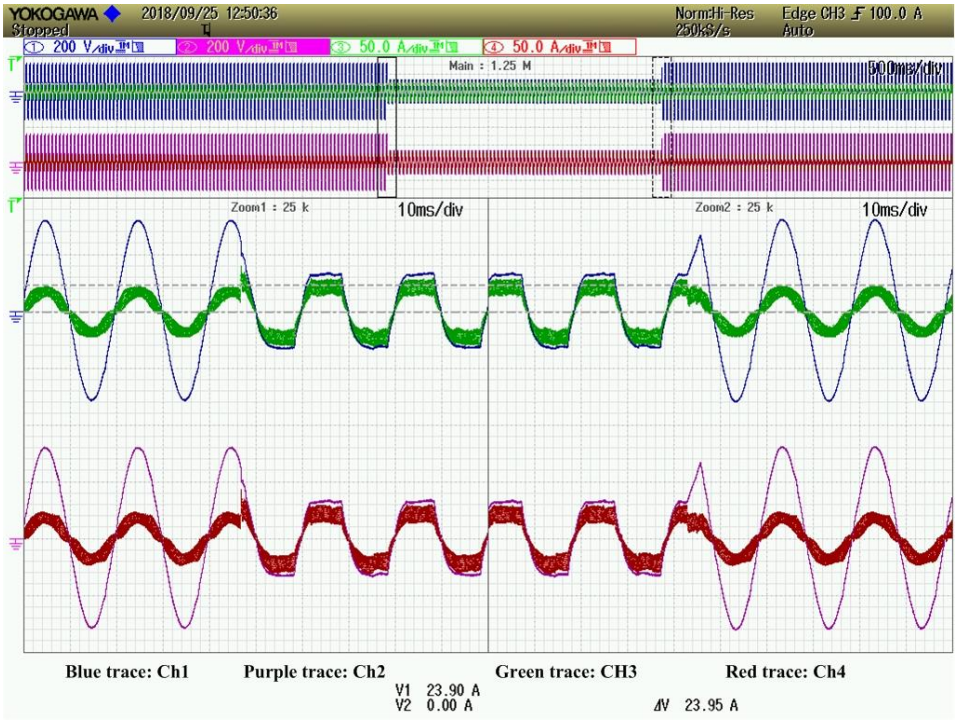
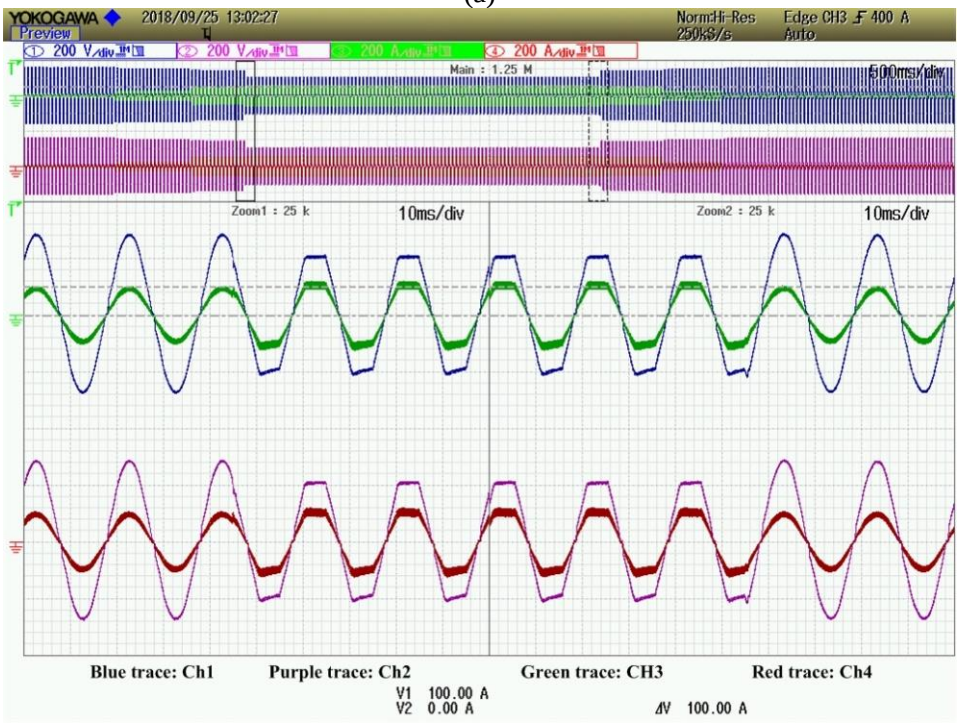


Fig. 18. Normal operation to phase to phase short circuit, CH1: Phase A output voltage; CH2: Phase B output voltage; CH3: Phase A output current; CH4: Phase B output current.

Finally, current limit tests when UPS inverters operate in parallel have been developed. Two different current limit values have been selected to verify the effectiveness. Fig. 19(a) shows the results when the current limit value is 24A, Fig. 19(b) depicts the results when the current is limited to 100A when stronger load is connected. From the results, we can notice that an accurate current limit performance can be obtained even when inverters operate in parallel.



(a)



(b)

Fig. 19. Current limit results when UPS inverters operate in parallel, CH1: Phase A voltage of inverter 1; CH2: Phase A voltage of inverter 2; CH3: Phase A current of inverter 1; CH4: Phase A current of inverter 2. (a) 24A current limit, (b) 100A current limit.

IV. CONCLUSION

This paper presents a control method to ensure overload and short circuit protection in voltage source inverters based

UPS systems. With the proposed control method, UPS output current can be limited to a reference value within the safe operation area, so that when overload or short circuit happens instantaneous voltage drop occurs. The proposed solution compared with the state-of-the-art ones is superior in terms of accuracy and validity under more kinds of overcurrent issues, while being compatible with advanced current/voltage tracker regulators based on resonant controllers. Furthermore, as a sharp contrast with the existing techniques, the proposed approach is not only robust to symmetric three-phase faults but also the asymmetric single-phase overload/short-circuit conditions in a three-phase system, and the healthy phase will not be disturbed by the fault phase. Another brilliant feature is that as opposite to conventional techniques in which the control has to switch between voltage to current mode once overload/short-circuit occurs, and back to voltage mode once the fault is cleared, is that the proposed controller does not have to switch between operation modes, which may lead to instabilities or oscillatory transients. In this approach, once the fault is cleared, the UPS system can go quickly back to normal operation conditions without changing the control mode, operating all the time as a voltage controlled source. Experimental results on a commercial UPS platform have been implemented to verify the effectiveness of the proposed control method.

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