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An Optimized Hybrid Modulation Scheme for Reducing Conduction Losses in Dual Active Bridge Converters

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***Abstract*—A linearized hybrid modulation scheme for the DAB converter is proposed in this paper. For the purpose of minimizing the conduction losses dissipated on the transformer and the power transistors, an optimal relationship function between the two control variables employed in extended phase shift (EPS) modulation can be derived. However, the obtained relationship function is a complex expression, which is not good for simple online control. Hence, a linearized modulation scheme is proposed in this paper. This modulation scheme can achieve a quasi-minimum RMS value of the leakage inductance current for the same output power. Meanwhile, the zero voltage switching (ZVS) of the power transistors can be achieved over the whole power range. The power transfer capability is also kept same as the optimal EPS scheme. Finally, experiments are conducted on a laboratory prototype to validate the effect of the linearized modulation scheme on the reduction of conduction losses. The experimental results present an improved converter efficiency and the realization of ZVS.**

I. Introduction

Firstly proposed in 1988 [1], the dual active bridge (DAB) converter is now widely used in many applications such as distributed power systems and energy storage [2], [3]. Due to its advantages of galvanic isolation and bidirectional power flow, DAB converters are applied among multiple dc energy sources such as battery packs, ultra-capacitors and photovoltaic submodules to match various voltage levels [4]–[7]. Moreover, since the DAB converter can naturally achieve zero voltage switching (ZVS) without any auxiliary components and has a simple and symmetrical structure, it is also a potential candidate for high efficiency and high power density applications such as electric vehicles and aerospace [8]–[11]. For the same reason, the DAB is also an ideal dc-dc conversion choice for applications where modular design is often needed such as energy storage systems and power electronic transformers.

A conventional way to control the DAB converter is using single phase shift (SPS) modulation to fulfill the power/voltage/current requirements. SPS is simple and easy for real time control. However, utilizing this simple modulation scheme can not guarantee ZVS if the voltage ratio deviates far from one, which results in poor efficiency at partial load conditions. Notably, under this situation, even the switches might be broken with excessive dv/dt caused by ZVS failure [12]–[14]. In order to overcome this drawback, many improved modulation methods are introduced to extend the DAB soft-switching operating range, such as extended phase-shift (EPS) modulation [15], dual phase-shift (DPS) modulation [16], [17] and triple phase-shift (TPS) modulation [18]–[21]. Other than only one phase shift in SPS, these improved modulation schemes try to introduce more control variables.

In the simple SPS modulation, only the outer phase shift between the primary and the secondary full bridge is regulated, leading to a two-level primary and secondary winding voltage. If varying inner phase shift (as defined in Section II-B) is considered, the winding voltages turn to three-level because the diagonal switches in each full bridge are not turned on or off synchronously any more. Taking [21] as an example, a comprehensive searching of operation modes with TPS is implemented, and the corresponding soft-switching boundaries for each operation mode are derived. However, the analysis of power transfer range is absent, which is important for selecting proper operation mode due to the varying given powers.

Alternatively, applying multiple control variables makes it possible to realize a more ambitious target, such as current stress optimization [22]–[26], backflow power reduction [27] and non-active power loss minimization [28]. Actually, these optimization targets are based on optimizing different parts of the leakage inductance current, e.g. current stress optimization usually refers to reducing the peak value of the leakage inductance current, backflow power is often related to the intervals when the current direction is reversed into the power source.

Besides, many optimized control schemes are focusing on reducing the root mean square (RMS) value of the leakage inductance current [29]–[32], which is closely related to the conduction losses of the power semiconductors and high-frequency transformer. Notably, hybrid modulation methods could be adopted in order to extend the converter performance over a wide operation range [33], [34]. Furthermore, the switching frequency can also be varied aiming at specific optimization objects. In [35], the switching frequency is varied to modulate the DAB in a specific single-stage ac-dc converter. In [36], the circulating current is minimized over a wide power range using variable frequency modulation.

Among the aforementioned modulation methods, some of them are complicated and not easy to implement. One usual situation is that in order to make the DAB converter work at the optimal operation point, massive calculations are often conducted to handle those complex relationships among the

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control variables. The reason is that at least three limitations should be taken into account during the operation, i.e. the ZVS range, the power transfer capability and the optimization targets. Of course, there exist other factors depending on different requirements, such as the voltage variation range, the transient response or the effect of the passive components. One way to solve the complexity is to adopt a look-up table in the control process, where the optimal operation points are calculated in advance and input into a table prior to the converter operation. But the performance of this method is adversely affected by the components mismatched parameters due to their tolerances, temperature dependency and lifetime. Moreover, a large memory is needed to guarantee the accuracy if the converter has to work in a wide operation range. In terms of the variable switching frequency modulation, one large challenge is the design of passive components and the electromagnetic interference filter.

In order to make the DAB converter more adaptive and applicable, this paper proposes an optimized hybrid modulation scheme to simplify the control process based on EPS modulation. The main contributions of this paper are:

- The comprehensive analysis of the power transfer range for each operation mode, which is derived based on the ZVS conditions rather than operation mode boundary conditions as in some literature.
- The analytical optimization expressions for each operation mode are derived in order to minimize the RMS value of the leakage inductance current.
- Several simplified optimization methods are proposed based on different voltage ratio requirements and preferred working conditions in various applications.
- Independent of the voltage ratio limitation and being simpler than other methods, the linearized optimization method is applied to the available DAB setup in this paper and validated by the experimental results.

This paper is organized as follows. Firstly, the EPS based operation modes for boost and buck scenarios under ZVS conditions are presented in Section II. Next, according to the derived operation modes in Section II and selected components for the DAB setup, the losses distribution are calculated in Section III. In Section IV, an optimal modulation scheme (called 'OMS1' in the following) is firstly derived. In order to simplify this scheme and considering different voltage ratio requirements, three approximated modulation schemes are developed. With the aim of selecting the most suitable modulation method, a through comparison is presented among these four schemes at the end of Section IV. Therefore, in Section V, the selected linear scheme is applied into a laboratory prototype to validate the feasibility on conduction losses reduction and ZVS realization. Finally, conclusions are given in Section VI.

II. Basic Modulation Methods for Dual Active Bridge Converters

A. DAB Model

The topology of the DAB converter is shown in Fig. 1. It consists mainly of two full bridges HB_1 and HB_2, the middle terminals of which are linked by a high-frequency transformer and the side ends are paralleled with the input and output dc voltage ports. In order to flexibly adjust the leakage inductance, an auxiliary inductor is cascaded with the high-voltage primary winding so that a lower additional power loss is induced compared to the secondary low-voltage high-current winding.

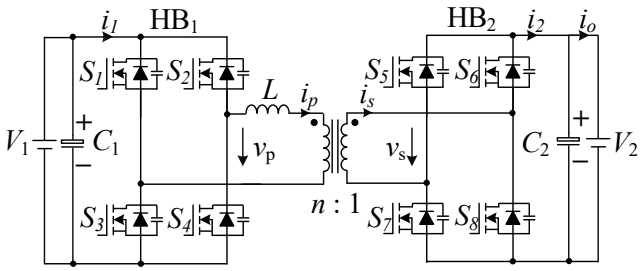


Fig. 1. Topology of the dual active bridge (DAB) converter.

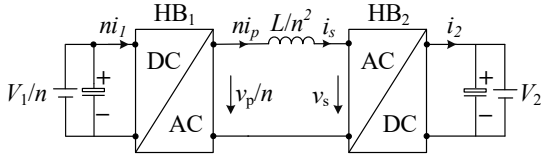


Fig. 2. Simplified DAB model by referring the converter to the secondary side of the transformer.

The magnetizing inductance is considered much larger than the leakage inductance, leading to negligible magnetizing current compared with the load current. Therefore in the T-type transformer equivalent circuit, the branch with magnetizing inductor can be seen as an open circuit. On this basis, the DAB model is obtained as shown in Fig. 2 after referring the circuit parameters to the secondary side.

B. Operation Modes

Due to the bidirectional power transfer ability and the symmetrical topology, the DAB converter has four operating scenarios: forward/backward, buck/boost. Assuming the power flow is from the primary side to the secondary side, a factor k is introduced as

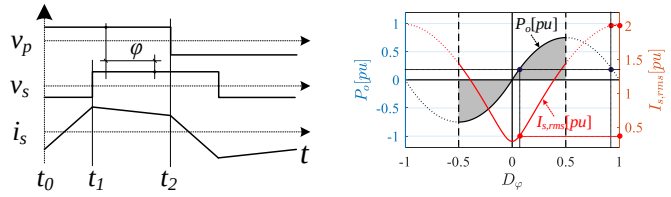
$$k = \frac{V_1}{nV_2} \tag{1}$$

to signify the voltage ratio. $k < 1$ and $k > 1$ denote boost and buck scenarios, respectively.

In order to simplify the calculations, the base power P_b and base current I_b defined in (2) are used to normalize the real values. Therein, V_1, V_2 and f_{sw} denote the input, output dc voltage and the switching frequency, respectively. L is the total inductance consisting of the transformer leakage inductance and the auxiliary inductance.

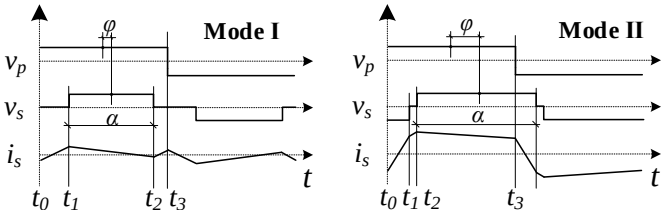
$$P_b = \frac{(nV_2)^2}{8Lf_{sw}}, \quad I_b = \frac{n^2V_2}{8Lf_{sw}} \tag{2}$$

The power is mainly controlled by the outer phase shift φ, which is the displacement angle between the fundamental components of v_p and v_s. If $D_\varphi = \varphi/\pi$ is defined for



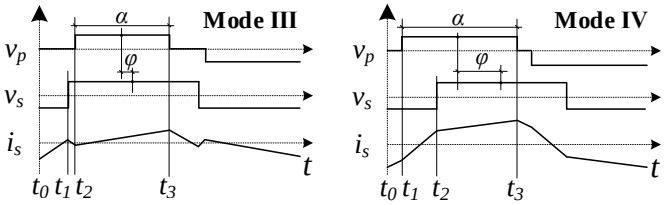
(a) (b)

Fig. 3. (a) typical SPS working waveforms over one switching period, which is a special case of EPS by setting $D_\alpha = 1$ in Mode II (b) the output power $P_{\rm o}$ and the RMS leakage inductance current $I_{\rm L,rms}$ of the DAB converter with repect to D_φ, $k = 0.75$ in this case.



(a) (b)

Fig. 4. In boost scenario, typical EPS working waveforms in one switching period (a) Mode I, $D_\varphi < (1 - D_\alpha)/2$ (b) Mode II, $D_\varphi > (1 - D_\alpha)/2$.



(a) (b)

Fig. 5. In buck scenario, typical EPS working waveforms in one switching period (a) Mode III, $D_\varphi < (1 - D_\alpha)/2$ (b) Mode IV, $D_\varphi > (1 - D_\alpha)/2$.

simplification, $D_\varphi \in [0, 1]$ stands for forward power flow from V_1 to V_2 and $D_\varphi \in [-1, 0]$ for the reverse direction. In fact, D_φ is often limited in $[-0.5, 0.5]$ to lower the RMS value of the leakage inductance current while maintaining the same power transfer capability, which can be explained by Fig. 3.

Given the SPS working waveforms in Fig. 3(a) and with $T_{sw} = 1/f_{sw}$, the normalized average output power $P_o[pu] = 1/P_b \cdot 1/T_{sw} \cdot \int_0^{T_{sw}} [v_s(t) \cdot i_s(t)]dt$ and the normalized RMS leakage inductance current $I_{s,rms}[pu] = 1/I_b \cdot \sqrt{1/T_{sw} \cdot \int_0^{T_{sw}} i_s^2(t)dt}$ are derived as

$$P_o[pu] = 4kD_\varphi(1 - D_\varphi) \tag{3}$$

$$I_{s,rms}[pu] = \frac{2\sqrt{3}}{3} \cdot \sqrt{(12D_\varphi^2 - 8D_\varphi^3 - 2)k + k^2 + 1} \tag{4}$$

which can be represented by the black curve and red curve in Fig. 3(b), respectively. It can be seen that there are always two points in the ranges of $[0, 0.5]$ and $[0.5, 1]$ for the same power, but the leakage inductance current is smaller in $[0, 0.5]$. This conclusion is also applicable to other phase-shift modulation schemes including EPS.

In EPS, considering the voltage-second balance of the leakage inductor, two operation modes can be found for boost or buck scenario, as shown in Fig. 4 and Fig. 5, respectively. If the inner phase shift is denoted by $D_\alpha = \alpha/\pi$, then $\alpha \in [0, \pi]$ corresponds to $D_\alpha \in [0, 1]$. Clearly, if $D_\alpha = 1$, EPS is fallen into SPS. In this regard, SPS can be seen as a special case of EPS.

The current waveform is shaped by the voltage drop on the leakage inductor.

$$\frac{L}{n^2}\frac{di_s(t)}{dt} = \frac{v_p(t)}{n} - v_s(t) \tag{5}$$

Considering $i_s(t_0) = i_s(t_3)$ in half switching period ($t_3 = T_{sw}/2$), the segmented current can be calculated, as listed in Table I.

In order to achieve zero-voltage switching for all switches, the parasitic capacitor of each off-state transistor should be fully discharged at first, which happens through the resonance of the parasitic capacitor C_{oss} and the leakage inductance

TABLE I
EXPRESSIONS OF THE NORMALIZED LEAKAGE INDUCTANCE CURRENT DURING DIFFERENT INTERVALS FOR EACH EPS OPERATION MODE

Mode I ⇢ Fig. 4(a)	
$[t_0, t_1]$	$i_s(t)[pu] = \frac{8k}{T_{sw}}t - 2k + 2D_\alpha$
$[t_1, t_2]$	$i_s(t)[pu] = \frac{8(k-1)}{T_{sw}}t + 2 - 2k + 4D_\varphi$
$[t_2, t_3]$	$i_s(t)[pu] = \frac{8k}{T_{sw}}t - 2k - 2D_\alpha$
Mode II ⇢ Fig. 4(b)	
$[t_0, t_1]$	$i_s(t)[pu] = \frac{8(k+1)}{T_{sw}}t - 2k - 4D_\varphi + 2$
$[t_1, t_2]$	$i_s(t)[pu] = \frac{8k}{T_{sw}}t - 2k + 2D_\alpha$
$[t_2, t_3]$	$i_s(t)[pu] = \frac{8(k-1)}{T_{sw}}t - 2k + 2 + 4D_\varphi$
Mode III ⇢ Fig. 5(a)	
$[t_0, t_1]$	$i_s(t)[pu] = \frac{8}{T_{sw}}t - (2k-2)D_\alpha - 4D_\varphi$
$[t_1, t_2]$	$i_s(t)[pu] = -\frac{8}{T_{sw}}t - (2k+2)D_\alpha + 4D_\varphi + 4$
$[t_2, t_3]$	$i_s(t)[pu] = \frac{8(k-1)}{T_{sw}}t + (2k-2)D_\alpha + 4D_\varphi + 4 - 4k$
Mode IV ⇢ Fig. 5(b)	
$[t_0, t_1]$	$i_s(t)[pu] = \frac{8}{T_{sw}}t - (2k-2)D_\alpha - 4D_\varphi$
$[t_1, t_2]$	$i_s(t)[pu] = \frac{8(k+1)}{T_{sw}}t + (2k+2)D_\alpha - 4D_\varphi - 4k$
$[t_2, t_3]$	$i_s(t)[pu] = \frac{8(k-1)}{T_{sw}}t + (2k-2)D_\alpha + 4D_\varphi + 4 - 4k$

TABLE II
COMBINED LIMITATIONS BY ZVS AND OPERATIONAL CONSTRAINTS

Mode I	$2k/(1-k)D_\varphi < D_\alpha < k, \quad 0 < D_\varphi < (1-k)/2$
Mode II	$D_\alpha > 2k(1-D_\varphi)/(1+k), \quad (1-k)/2 < D_\varphi < 1/2$
Mode III	$2D_\varphi/(k-1) < D_\alpha < 1/k, \quad 0 < D_\varphi < (k-1)/(2k)$
Mode IV	$D_\alpha > 2(1-D_\varphi)/(1+k), \quad (k-1)/(2k) < D_\varphi < 1/2$

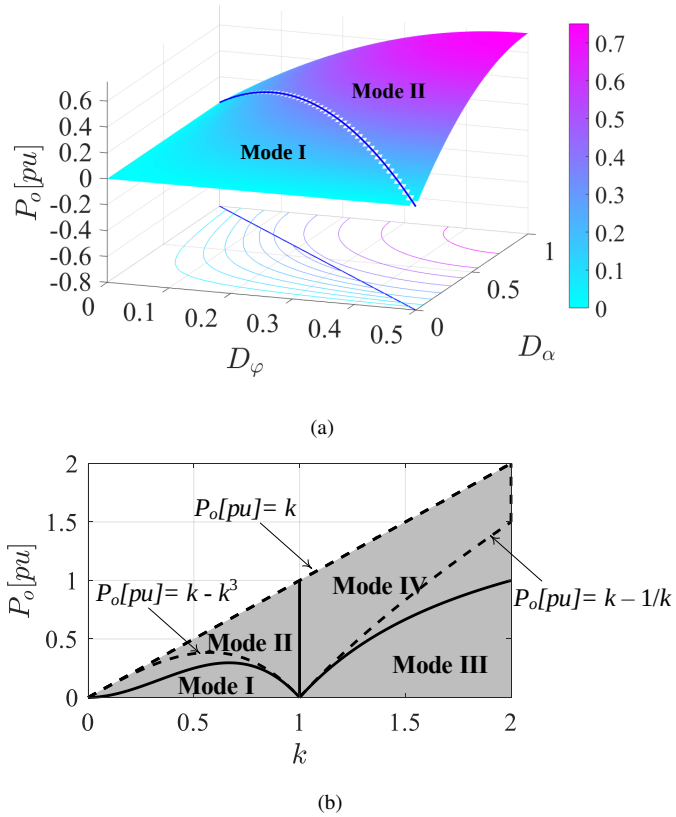


Fig. 6. (a) Output power in terms of D_α and D_φ with the blue curve as the operational constraint. (b) ZVS-limited power transfer range in terms of k: gray area is the ZVS range for EPS and it is divided into 4 parts (i.e. 4 modes) by solid curves. The area encircled by dashed lines is ZVS range for SPS.

L. Afterwards, the body diode will be naturally conducted, resulting in a near-zero source-to-drain voltage V_{DS} (the actual value is equal to the voltage drop on the body diode). Thus zero-voltage switching can be achieved if the transistor is turned on at this moment, indicating that the direction of the current flow is from source to drain at the switching-on instants for $S_1 \sim S_8$. According to this constraint, the polarity of the leakage current at switching instants can be confirmed and the ZVS conditions can be further derived with the current expressions in Table I. Then associating with the operational constraints for each mode, the combined limitations on the control variables are attained in Table II.

C. ZVS-limited Power Transfer Range

Using the current expressions in Table I, the average output power in one switching period can be calculated with

$$P_o[pu] = \begin{cases} 4kD_\alpha D_\varphi & \text{Mode I,III} \\ -k[4D_\varphi^2 - 4D_\varphi + (1-D_\alpha)^2] & \text{Mode II,IV} \end{cases} \tag{6}$$

Since D_φ in I, III is smaller, the power transmission ability is weaker compared to II, IV, as shown in Fig. 6(a). In other words, Mode I and Mode III are suitable for lower power transmission while Mode II and Mode IV for higher. On this basis, the limited power transfer range by considering the ZVS constraints in Table II can be derived as

$$P_o[pu] \in \begin{cases} \left.\begin{matrix} (0, \quad 2k^2(1-k)] \rightarrow \text{Mode I} \\ (2k^2(1-k), \quad k] \rightarrow \text{Mode II} \end{matrix}\right\} k<1 \\ \left.\begin{matrix} (0, \quad 2(k-1)/k] \rightarrow \text{Mode III} \\ (2(k-1)/k, \quad k] \rightarrow \text{Mode IV} \end{matrix}\right\} k>1 \end{cases} \tag{7}$$

and shown by the gray area in Fig. 6(b). For comparison, in SPS, due to the ZVS conditions $D_\varphi > (1-k)/2$ and $D_\varphi > (k-1)/(2k)$, the power range limited by

$$P_o[pu] \in \begin{cases} [k-k^3, \quad k] \rightarrow k<1 \\ [k-1/k, \quad k] \rightarrow k>1 \end{cases} \tag{8}$$

is also plotted in Fig. 6(b). The boundary conditions in (8) are denoted by the dashed lines in Fig. 6(b) . Varying with the voltage ratio k, the ZVS can be theoretically achieved from zero to the maximum power in EPS, while this is applicable to SPS only when $k = 1$. In other words, the ZVS range is considerably extended in EPS because of the introduced control variable D_α.

III. Losses Distribution

A. Transformer and Auxiliary Inductor

The losses of the magnetical components include copper losses and core losses. For the given transformer and inductor in Table III, the copper losses can be calculated with

$$P_{cond,Tr} = \left(\frac{R_L + R_{Trp}}{n^2} + R_{Trs}\right) \cdot I_{s,rms}^2 \tag{9}$$

where R_L is the auxiliary inductor resistance, and R_{Trp}, R_{Trs} are the primary and secondary winding resistances of the transformer, respectively.

For simplification, assuming the transformer and inductor are fed by the fundamental sinusoidal components, this allows for calculating core losses with the Steinmetz equation [39]

$$p_v = C_m f_{sw}^\alpha \hat{B}^\beta \tag{10}$$

and the core volume V_{Tr} and V_L, respectively. The peak magnetic flux density $\hat{B}$ is estimated with $\hat{B}_{Tr} \approx 2V_1/(\pi^2 f_{sw} N_{Trp} A_{Tr})$ (N_{trp}: primary winding turns, A_{Tr}: effective magnetic cross section) and $\hat{B}_L \approx \mu_{eff}\mu_0 N_L \hat{I}_L / l_L$ (μ_{eff}: equivalent relative permeability of a gapped core, N_L: winding turns, $\hat{I}_L$: peak inductor current, l_L: effective magnetic path length) for the transformer and auxiliary inductor, respectively. Detailed information is listed in Table IV.

B. Power Switches

The losses caused by the power semiconductors mainly consist of conduction and switching losses. For the calculation of the conduction losses, the RMS switch currents can be easily derived from the RMS transformer current $I_{s,rms}$ due to that every switch conducts current during half of the switching period. Therefore, given the switch parameters in Table III, he conduction losses of the power switches can be calculated with

$$P_{cond,sw} = 4 \cdot \frac{R_{DSonp}}{N_{swp}} \cdot \left(\frac{I_{s,rms}}{\sqrt{2}n}\right)^2 + 4 \cdot \frac{R_{DSons}}{N_{sws}} \cdot \left(\frac{I_{s,rms}}{\sqrt{2}}\right)^2 \tag{11}$$

TABLE III
COMPONENTS PARAMETERS OF THE IMPLEMENTED PROTOTYPE

Components	Parameters
Primary winding of the DAB HF transformer: 35 turns copper foil	R_{Trp}=607.9 mΩ @T_a=25 ^oC
Secondary winding of the DAB HF transformer: 10 turns copper foil	R_{Trs}=16.5 mΩ @T_a=25 ^oC
Auxiliary inductor: 10 turns Litz wire, 20 strands, 0.355 mm	R_L=27.9 mΩ @T_a=25 ^oC
MOSFETs $S_1 \sim S_4$: IPW65R080CFD	R_{DSonp}=72 mΩ @T_j=25 ^oC
MOSFETs $S_5 \sim S_8$: 2 x IPP110N20N3 in parallel	R_{DSons}=9.6 mΩ @T_j=25 ^oC

TABLE IV
MAGNETIC CORE PARAMETERS

Transformer (core type: ETD59/31/22 material: N97)					
V_{Tr}	A_{Tr}	N_{Trp}	C_m	α	β
51.2 cm^2	368 mm^2	35	8.21	1.28	2.2
Auxiliary Inductor (core type: ETD44/22/15 material: N87)					
V_L	l_L	μ_{eff}	C_m	α	β
17.8 cm^2	10.3 cm	120	10	1.26	2.15

R_{DSonp}/N_{swp} and R_{DSons}/N_{sws} are the equivalent switch on-state resistance if each switch consists of N_{swp} and N_{sws} paralleled semiconductors in the primary and secondary full-bridges, respectively.

On the basis of ZVS turn-on, only turn-off losses are considered for calculating switching losses for each transistor, which can be estimated by [40]

$$p_{sw} = U_{DS} \cdot I_{off} \cdot \frac{t_{ru} + t_{fi}}{2} \cdot f_{sw} \tag{12}$$

where U_{DS} denotes the turn-off voltage and I_{off} is the current at switching-off instants. t_{ru} and t_{fi} are the voltage rise time and current fall time during switching-off transients.

C. Capacitors

The losses dissipated on the input and output capacitors are calculated with the equivalent series resistance (ESR), which can be obtained from the datasheet, leading to

$$p_{cap} = \frac{R_{ESR}}{N_{cap}} I_c^2 \tag{13}$$

where N_{cap} is the number of parallel capacitors. The selected capacitors are one B43544A6397M000 (C_1=0.39 mF) on the input side and five EETEE2D301HJ in parallel (C_2=1.5 mF) on the output side.

D. Losses Distribution

The total losses are the sum of all discussed power losses and can be categorized as switching losses P_{sw}, conduction losses P_{cond}, core losses P_{core} and capacitor losses P_{cap}, namely

$$P_{total} = P_{sw} + P_{cond} + P_{core} + P_{cap} \tag{14}$$

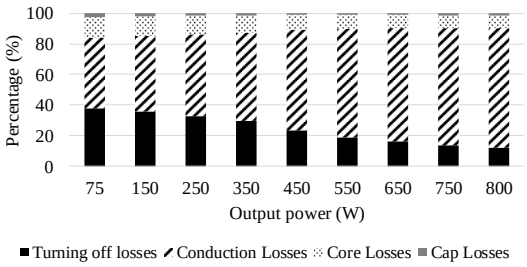


Fig. 7. Calculated losses distribution percentages.

with further specifications:

$$\begin{aligned} P_{sw} &= P_{sw,S_1\sim S_4} + P_{sw,S_5\sim S_8} \\ P_{cond} &= P_{cond,Tr} + P_{cond,sw} \\ P_{core} &= P_{core,Tr} + P_{core,L} \\ P_{cap} &= P_{cap,in} + P_{cap,out} \end{aligned} \tag{15}$$

Operating the converter under ZVS conditions, the calculated losses percentages of different dissipation parts are shown in Fig. 7. It can be seen that for the given setup, the conduction losses are the dominating part over the whole power range, although the switching losses are almost equal to the conduction losses in light load. Besides, the conduction losses portion increases a lot in the heavy load. therefore, reducing conduction losses is of high importance to improve the system performance.

IV. OPTIMIZED MODULATION SCHEMES FOR REDUCING CONDUCTION LOSSES

As shown in Fig. 7, conduction losses are the major loss source for the given converter setup, which are determined by the RMS value of the leakage inductance current $I_{s,rms}$ seen from (9) and (11). It is also shown in (6) that there are infinite combinations of D_α and D_φ for the same average output power, which provides the possibility to reduce the conduction losses without sacrificing other performances. Fig. 8 illustrates an example of operating waveforms with different values of D_α and D_φ but with the same output power. Clearly, the RMS current in Fig. 8(b) is smaller than Fig. 8(a).

As proved in the following, for different output power levels, there exist an optimal operating point at which the leakage inductance current is minimized and simultaneously the ZVS can be guaranteed. But the derived analytical solutions are too complex for practical control. Therefore, a linearized modulation scheme is proposed to simplify the control process.

A. Conventional Current Minimization (OMS1)

The normalized RMS currents $I_{s,rms}[pu]$ for each operation mode are firstly derived based on the working waveforms in Fig. 4 $\sim$ 5, and the results are listed in Table V. In order to minimize the leakage inductance current and satisfy the output power requirements at the same time, the power expression of Mode I in (6) is rewritten as $D_\varphi = P_o[pu]/(4kD_\alpha)$ and then

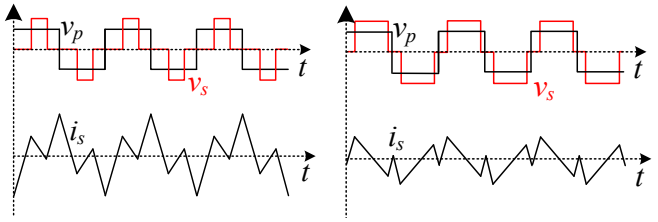


Fig. 8. Simulated working waveforms with different combinations of D_α and D_φ (a) D_α=0.35, D_φ=0.053 (b) D_α=0.73, D_φ=0.026 for the same output power.

TABLE V
EXPRESSIONS OF THE NORMALIZED LEAKAGE INDUCTANCE CURRENT FOR EACH OPERATION MODE

Operation Mode	RMS leakage inductance current $I_{s,\mathrm{rms}}[pu]$
Mode I	$\frac{2}{3}\cdot sqrt\Big[3(k-2)D_\alpha^3+9D_\alpha^2 + (36D_\varphi^2-9)kD_\alpha+3k^2\Big]$
Mode II	$\frac{2}{3}\cdot sqrt\Big[-6D_\alpha^3+(-18kD_\varphi+9k+9)D_\alpha^2 + (36D_\varphi-18)kD_\alpha+3k^2+3k(1-2D_\varphi)^3\Big]$
Mode III	$\frac{2}{3}\cdot sqrt\Big[3-(6k^2-3k)D_\alpha^3+9k^2D_\alpha^2 - 3kD_\alpha(3-12D_\varphi^2)\Big]$
Mode IV	$\frac{2}{3}\cdot sqrt\Big[-6k^2D_\alpha^3+(9k^2-18kD_\varphi+9k)D_\alpha^2 - (18-36D_\varphi)kD_\alpha+3-3(1-2D_\varphi)^3k\Big]$

it is substituted into the expression of $I_{s,rms}[pu]$ in Table V, resulting in

$$I_{s,rms}[pu]= \frac{2}{3}\cdot\sqrt{3(k-2)D_\alpha^3+9D_\alpha^2+\Big(\frac{9P_o[pu]^2}{4k^2D_\alpha^2}-9\Big)kD_\alpha+3k^2} \tag{16}$$

For achieving the extreme value of $I_{s,rms}[pu]$ for a certain output power $P_o[pu]$, the differential of (16) with respect to D_α is set to be 0, namely $\partial I_{s,rms}[pu]/\partial D_\alpha = 0$, solving which will lead to

$$(12k^2-24k)D_\alpha^4+24kD_\alpha^3-12k^2D_\alpha^2-3P_o[pu]^2=0 \tag{17}$$

It is difficult to directly solve for the analytical solution of (17) due to the high order of D_α. So $P_o[pu]$ in (17) is replaced by $4kD_\alpha D_\varphi$, and the simplified result is

$$(k-2)D_\alpha^2+2D_\alpha-k(4D_\varphi^2+1)=0 \tag{18}$$

Then it becomes easy to obtain the solutions of (18), which are

$$D_{\alpha1}=\frac{1-\sqrt{(1-k)^2-4k(2-k)D_\varphi^2}}{2-k} \tag{19}$$

TABLE VI
OPTIMAL VARIABLES RELATIONSHIP WITH MINIMIZED LEAKAGE INDUCTANCE CURRENT IN EACH OPERATION MODE (OMS1)

Mode I --→ Fig. 4(a)
$D_{\alpha,opt1}=\frac{1-\sqrt{(1-k)^2-4k(2-k)D_\varphi^2}}{2-k}, \quad 0<D_\varphi\le\frac{1-k}{2}$
Mode II --→ Fig. 4(b)
$D_{\alpha,opt1}=\frac{2D_\varphi+k-1+\sqrt{(1-k-2D_\varphi)^2+[k(1-2D_\varphi)]^2}}{k}, \quad for \quad \frac{1-k}{2}<D_\varphi<\frac{k-1+\sqrt{1-k^2}}{2k}$
$D_{\alpha,opt1}=1, \quad for \quad \frac{k-1+\sqrt{1-k^2}}{2k}\le D_\varphi<\frac{1}{2}$
Mode III --→ Fig. 5(a)
$D_{\alpha,opt1}=\frac{k-\sqrt{(k-1)^2-4(2k-1)D_\varphi^2}}{2k-1}, \quad 0<D_\varphi\le\frac{k-1}{2k}$
Mode IV --→ Fig. 5(b)
$D_{\alpha,opt1}=kD_\varphi-k+1+\sqrt{[(1-2D_\varphi)k-1]^2+(1-2D_\varphi)^2}, \quad for \quad \frac{k-1}{2k}<D_\varphi<\frac{1-k+\sqrt{k^2-1}}{2}$
$D_{\alpha,opt1}=1, \quad for \quad \frac{1-k+\sqrt{k^2-1}}{2}\le D_\varphi<\frac{1}{2}$

$$D_{\alpha2}=\frac{1+\sqrt{(1-k)^2-4k(2-k)D_\varphi^2}}{2-k} \tag{20}$$

In order to select the correct solution from (19) and (20), the derived ZVS conditions for Mode I (in Table II) are considered. Substituting $D_\varphi<(1-k)/2$ into (19) and (20), the resulted

$$D_{\alpha1}<k \tag{21}$$

$$D_{\alpha2}>(2-2k+k^2)/(2-k)\ge k \tag{22}$$

indicate that $D_{\alpha1}$ satisfies the ZVS condition $D_\alpha<k$ while $D_{\alpha2}$ does not. Therefore, the correct analytical solution of (18) should be $D_{\alpha1}$. In other words, if (19) is satisfied, the leakage inductance current in Mode I for a certain output power will be located at the extreme value point. However, extreme values do not always mean the minimum values.

In order to verify whether $D_{\alpha1}$ is a proper solution of minimal $I_{s,rms}$, the relationships among $I_{s,rms}$-D_α-D_φ (ref. Table V) are depicted in Fig. 9. As shown in Fig. 9(a), only the red-colored area is related to Mode I, limited by the operational condition $D_\alpha<1-2D_\varphi$. It can be seen that for a certain output power, the black intersection points are the minimum $I_{s,rms}[pu]$ at different power levels. Thus it can be concluded that $D_{\alpha1}$ is the correct solution for achieving the minimum $I_{s,rms}$, which is exactly the $D_{\alpha,opt1}$ in Table VI.

Applying similar deriving process to Mode II, the resulting $I_{s,rms}[pu]$ surface with respect to D_α and D_φ is shown in Fig. 9(b). As for Mode III and Mode IV, the optimized results are directly given in Table VI, from which it can be seen that the analytical solution of D_α is segmented depending on the operation range of D_φ in Mode II and Mode IV. Especially,

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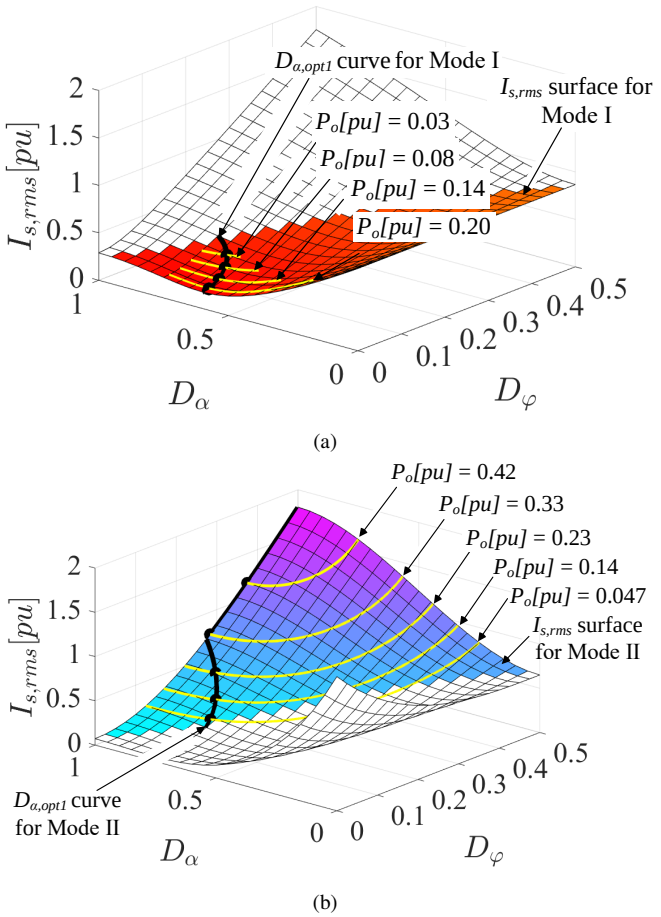

Fig. 9. 3D plot of the RMS leakage inductance current as the function of D_α and D_φ in boost scenario ($k = 0.75$ in this case) for (a) Mode I (b) Mode II. The expressions of $D_{\alpha,opt1}$ for achieving minimum $I_{s,rms}$ at different power levels can be found in Table VI.

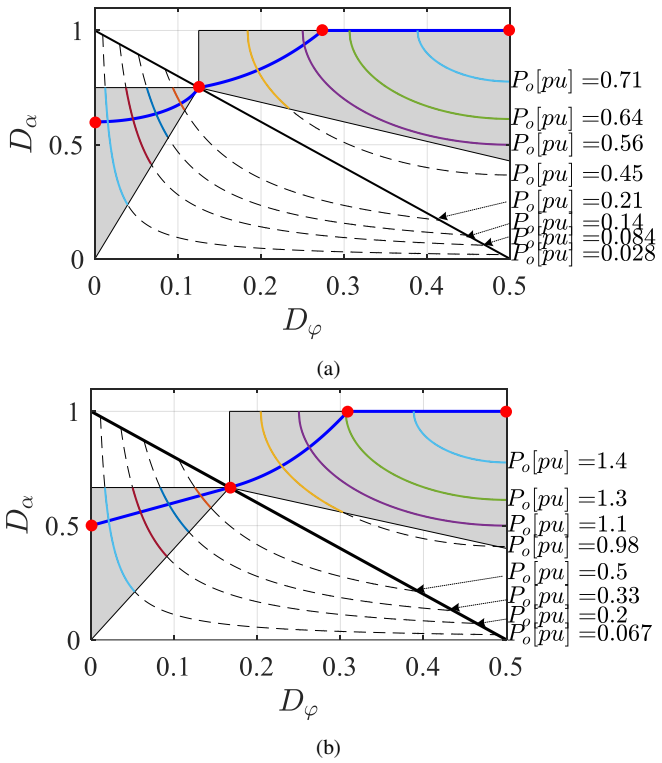

Fig. 10. The relationship function $D_\alpha = f(D_\varphi)$ in OMS1 (denoted by the blue curve) including the gray ZVS range and colored power curves in: (a) Boost scenarios ($k = 0.75$ in this case). (b) Buck scenarios ($k = 1.5$ in this case).

if D_φ is close to 0.5, the optimal D_α is equal to 1, meaning that the DAB converter transfers to the SPS modulation.

The modulation scheme for achieving minimum $I_{s,rms}$ is termed as Optimized Modulation Scheme 1 (OMS1). Although the RMS leakage inductance current can be theoretically minimized by adopting $D_{\alpha,opt1}$, it is difficult to realize OMS1 in practical control due to the complex relationship between D_α and D_φ, as shown in Table VI.

Thus it is important to simplify the relationship expression between D_α and D_φ. Besides D_α and D_φ, the RMS leakage inductance current is also determined by the voltage ratio k (ref. Table V). For different applications, the input and output voltage may change broadly, implying various voltage ratio requirements. On this basis, the following simplifying schemes are optimized considering both conduction losses reduction and different voltage ratio ranges.

B. Simplified Optimal Modulation Schemes

Due to the fact that the OMS1 is hard to realize, it is necessary to simplify the modulation scheme and meanwhile keep $I_{s,rms}$ as close to the minimum value as possible for reducing the conduction losses. As shown in Fig. 10, the gray areas are limited by ZVS conditions and the colored curves denote different output powers. The derived optimal relationship $D_\alpha = f(D_\varphi)$ for minimum $I_{s,rms}$ is represented by the blue curve. Either in buck scenario (Fig. 10(a)) or boost scenario (Fig. 10(b)), there are four key intersections induced by the segmented optimal function, which are shown by the red points. From left to right, the coordinates of these four cross points are derived as $[0, k/(2-k)]$, $[(1-k)/2, k]$, $[(k-1+\sqrt{1-k^2})/(2k), 1]$, $[0.5, 1]$in Fig. 10(a), and $[0, 1/(2k-1)]$, $[(k-1)/(2k), 1/k]$, $[(1-k+\sqrt{k^2-1})/2, 1]$, $[0.5, 1]$ in Fig. 10(b). Since the power is increased with D_φ and D_α, three different load situations are divided by the four intersections, i.e. light load, medium load and heavy load. Based on different voltage ratio requirements and load situations, the $D_{\alpha,opt1}$ expression can be simplified in various ways.

1) Unified Modulation Scheme (OMS2): A unified modulation scheme can be derived by applying curve fitting technique among the three points $[0, 1/(2k-1)]$, $[(k-1)/(2k), 1/k]$ and $[0.5, 1]$, resulting in

$$D_{\alpha.opt2} = \frac{4\,(3k-2)}{k\,(k-2)} D_\varphi^2 + \frac{2\,(2k-1)}{k} D_\varphi + \frac{k}{2-k} \quad (23)$$

which is as proposed in [41]. In this scheme, only one expression is needed over the three load conditions.

Similarly, the unified modulation expression in buck scenarios also can be derived as follows.

$$D_{\alpha,opt2} = \frac{4k(2k-3)}{2k-1} D_\varphi^2 + (4-2k) D_\varphi + \frac{1}{2k-1} \quad (24)$$

The relation expressions denoted by (23) and (24) are plotted as the red curves in Fig. 11. Nevertheless, depending

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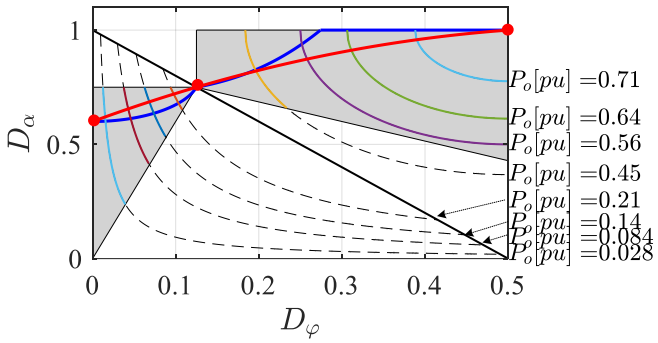
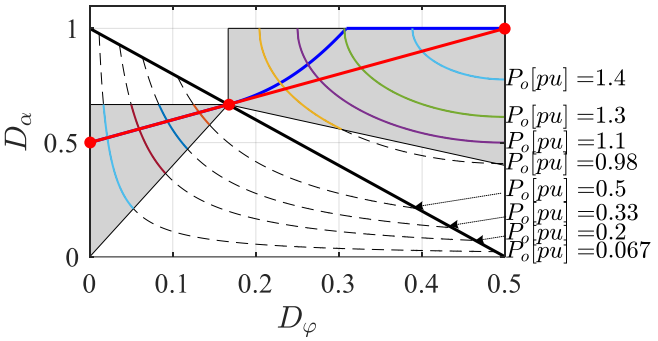
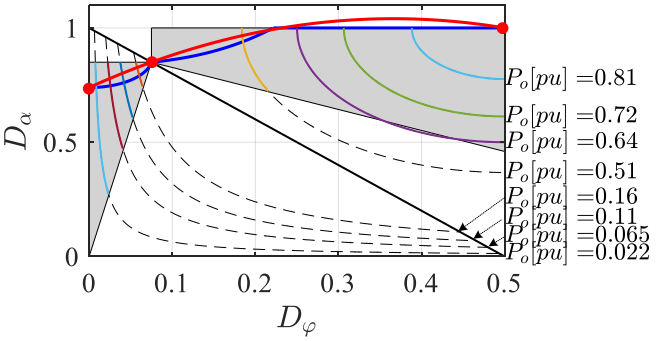


(a)

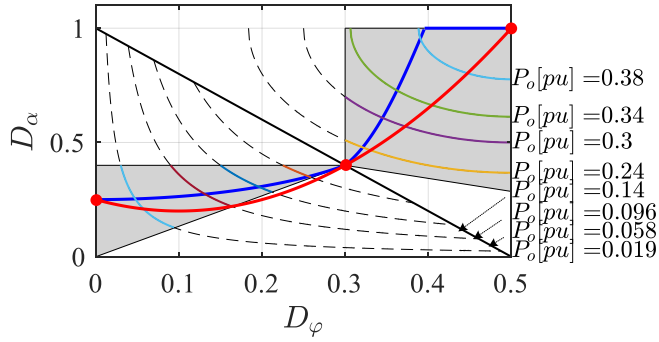


(b)

Fig. 11. The relationship function of (a) (23) for Boost scenarios ($k = 0.75$ in this case). (b) (24) for Buck scenarios ($k = 1.5$ in this case) in unified modulation scheme (OMS2), denoted by the red curves.



(a)



(b)

Fig. 12. Two ZVS failure cases for $D_{\alpha,opt2}$ in boost scenarios (a) $k = 0.85$ (b) $k = 0.4$ in unified modulation scheme (OMS2)

on the varying voltage ratio k, the red curve could exceed the gray ZVS range. For example, two failed cases caused by too large or too small k in boost scenarios are shown in Fig. 12, where part of the red curve is beyond the ZVS region. Therefore, there is a limited range of k for unified modulation.

In order to satisfy $D_{\alpha,opt2} \leq 1$ for any value of D_φ in $[0, 0.5]$, the symmetry axis of (23) should be larger than 0.5, then the maximum value of k can be solved, which is

$$\frac{(2k-1)(2-k)}{4(3k-2)} \geq \frac{1}{2} \quad \longrightarrow \quad k_{max} = 0.78 \tag{25}$$

On the other hand, in order to avoid the situation shown in Fig. 12(b), $D_{\alpha,opt2}$ in (23) should be larger than the ZVS border $2kD_\varphi/(1-k)$ for any $D_\varphi \in [0, (1-k)/2]$, leading to

$$\frac{k^2}{2(3k^2-5k+2)} \geq \frac{1-k}{2} \quad \longrightarrow \quad k_{min} = 0.45 \tag{26}$$

Similarly, the k range for (24) can be obtained in the same way, which is within $[1.28, 2.23]$ in buck scenarios for unified modulation scheme.

2) Partially Unified Modulation Scheme (OMS3): Seen from Table VI, EPS transfers into SPS ($D_{\alpha,opt1} = 1$) in heavy load. If the SPS is kept for easy control, the complex optimal expressions in light and medium load can be unified with one expression. In this regard, another group of three points $[0, k/(2-k)]$, $[(1-k)/2, k]$ and $[(k-1+\sqrt{1-k^2})/(2k), 1]$ in boost scenarios are used for curve fitting, and the D_α is kept at 1 in the range of $D_\varphi \in [(k-1+\sqrt{1-k^2})/(2k), 0.5]$. The simplified result will be

$$D_{\alpha,opt3} = \begin{cases} A_k \cdot D_\varphi^2 + B_k \cdot D_\varphi + C_k, \\ \qquad 0 < D_\varphi < \dfrac{k+\sqrt{1-k^2}-1}{2k} \\ 1, \qquad \dfrac{k+\sqrt{1-k^2}-1}{2k} \leq D_\varphi \leq \dfrac{1}{2} \end{cases} \tag{27}$$

with

$$\begin{cases} A_k = \dfrac{\left(8-8k-4k^2\right)\sqrt{1-k^2}+8k^3-8k^2-8k+8}{k\,(2-k)\,(1-k^2)} \\ B_k = \dfrac{\left(4-4k-2k^2\right)\sqrt{1-k^2}+2k^3-6k^2-4k+4}{k\,(k+1)\,(k-2)} \\ C_k = \dfrac{k}{2-k} \end{cases} \tag{28}$$

Applying a similar change into the buck scenarios, the curve fitting results are as follows.

$$D_{\alpha,opt3} = \begin{cases} A_k \cdot D_\varphi^2 + B_k \cdot D_\varphi + C_k, \\ \qquad 0 < D_\varphi < \dfrac{1-k+\sqrt{k^2-1}}{2} \\ 1, \qquad \dfrac{1-k+\sqrt{k^2-1}}{2} \leq D_\varphi \leq \dfrac{1}{2} \end{cases} \tag{29}$$

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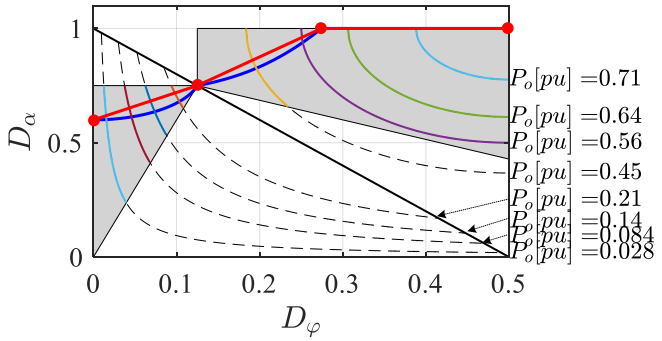
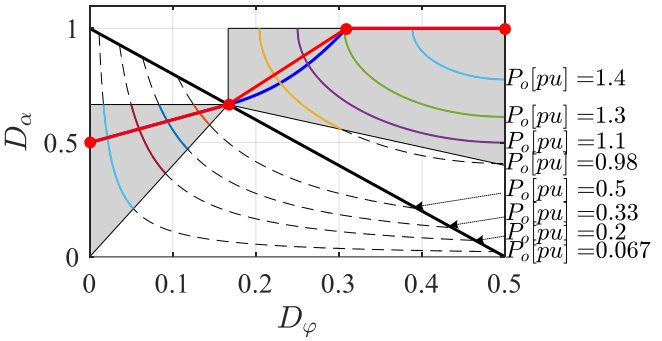


(a)



(b)

Fig. 13. The linearized relationship function of (a) (31) for Boost scenarios ($k = 0.75$ in this case). (b) (32) for Buck scenarios ($k = 1.5$ in this case) in linear modulation scheme (OMS4), denoted by the red curves.

with

$$\begin{cases} A_k = \dfrac{4k[(2k^2-2k-1)\sqrt{k^2-1}+2(k+1)(k-1)^2]}{2k^3-k^2-2k+1} \\ B_k = \dfrac{(4k+2-4k^2)\sqrt{k^2-1}-4k^3+4k^2+6k-2}{2k^2+k-1} \\ C_k = \dfrac{1}{2k-1} \end{cases} \tag{30}$$

Similar to the unified modulation scheme (OMS1), the voltage ratio in (27) and (29) needs to be limited within $[0.56, 0.91]$ and $[1.10, 1.80]$, respectively.

3) Linearized Modulation Scheme (OMS4): One common drawback of OMS2 and OMS3 is the limited range of voltage ratio k. In order to overcome this, a piecewise linear approximation scheme can be derived by considering the three load situations individually. Therefore, the four key points are all taken into account to linearize the complex exressions in Table VI, resulting in

$$D_{\alpha,opt4} = \begin{cases} \frac{2k}{2-k}D_\varphi + \frac{k}{2-k}, & D_\varphi \in [0, \frac{1-k}{2}] \\ \frac{\left(2-2k^2+2\sqrt{1-k^2}\right)}{k(1+k)}D_\varphi - \frac{(1-k)\sqrt{1-k^2}+1-k-2k^2}{k(1+k)}, & D_\varphi \in [\frac{1-k}{2}, \frac{k-1+\sqrt{1-k^2}}{2k}] \\ 1, & D_\varphi \in [\frac{k-1+\sqrt{1-k^2}}{2k}, 0.5] \end{cases} \tag{31}$$

in boost scenarios and

$$D_{\alpha,opt4} = \begin{cases} \frac{2}{2k-1}D_\varphi + \frac{1}{2k-1}, & D_\varphi \in [0, \frac{k-1}{2k}] \\ \frac{2k\sqrt{k^2-1}+2k^2-2}{k+1}D_\varphi - \frac{(k-1)\sqrt{k^2-1}+k^2-k-2}{k+1}, & D_\varphi \in [\frac{k-1}{2k}, \frac{1-k+\sqrt{k^2-1}}{2}] \\ 1, & D_\varphi \in [\frac{1-k+\sqrt{k^2-1}}{2}, 0.5] \end{cases} \tag{32}$$

in buck scenarios.

Fig. 13 gives two cases derived from (31) and (32), respectively. It can be clearly seen that no matter how the voltage ratio changes, the linearized red curves will always locate within the gray ZVS area. Accordingly, the linerized modulation scheme (OMS4) is set free from the voltage ratio limitation.

C. Comparison of Different Optimized Schemes

Based on different voltage ratio requirements and the preferred working conditions of the converter, the approximation principles of OMS2 $\sim$ OMS4 have been explained in Section IV-B. Compared to the original OMS1 in Section IV, the three simplified schemes have their own pros and cons. In the following, a detailed comparison will be performed from different perspectives.

Firstly, with regard to the unification (depending on D_φ), it can be evaluated by the number of segments in the relationship functions between D_α and D_φ, which is represented by the stars number in the second column of Table VII. More segments means poorer unification performance. Although both OMS1 and OMS4 have the same three segments, the OMS4 is easier to implement due to the linear approximation.

Then the voltage ratio limitations (i.e. k range) are compared for different schemes. As shown in last section, OMS1 and OMS4 can theoretically guarantee ZVS for any value of k, whereas a limited range should be considered for OMS2 and OMS3 to avoid ZVS failure over the whole power transfer range. In this regard, OMS1, OMS4 are better than OMS2, OMS3.

From the point of calculation burden, two conditions of the voltage ratio are considered, i.e. a fixed or a varying k. If V_1 and V_2 are fixed, the voltage ratio can be seen as a constant and thereby the $k-$depending coefficients (e.g. A_k, B_k, C_k) of $D_{\alpha,opti}(i = 1, 2, 3, 4)$ expressions are also constants. On this basis, $D_{\alpha,opt4}$ has the simplest form due to the lower number of mathematical multiplications and square roots, which also means faster processing speed for the digital processor. This advantage will become further clear when multiple DAB modules are working at the same time. On the other hand, if V_1 and V_2 are varying, the sampling speed of V_1, V_2 and the calculation burden of the $k-$depending coefficients should be taken into account. Regarding this, it can be found that OMS2 surpasses the other schemes, represented by four stars in Table VII.

At last, assuming the converter works in steady sate, the input and output voltages are stabilized with a fixed k. In respect of this, the complexity of different schemes are evaluated by adding the star numbers from the second to fourth column in

TABLE VII
COMPARISON OF OMS1, OMS2, OMS3 AND OMS4

	Unification	Voltage limitation	Calculation burden		Complexity
			fixed k	varying k	
OMS1	★	★★	★	★	4 · ★
OMS2	★★★	★	★★	★★★★	6 · ★
OMS3	★★	★	★★★	★★	6 · ★
OMS4	★	★★	★★★★	★★★	7 · ★

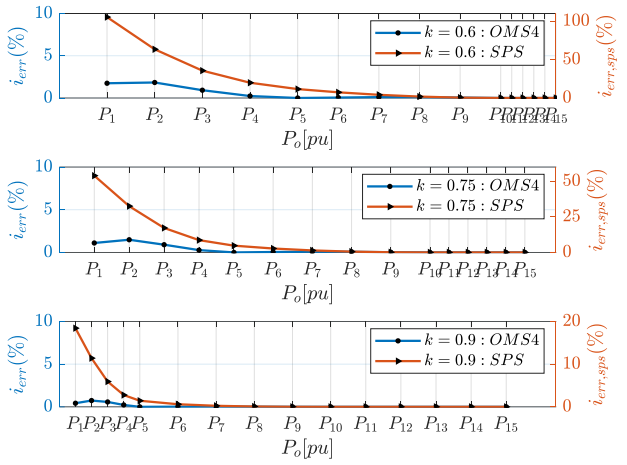


Fig. 14. Relative errors defined by (33) varying with voltage ratios and output powers

Table VII, and the summations are shown in the last column. It can be seen that OMS has the highest 7 stars, and thus will be selected as the focus to further evaluate the effectiveness on reducing conduction losses.

V. RESULTS AND DISCUSSION

As illustrated in IV-C, the linearized modulation scheme (OMS4) overtakes other schemes with a simpler form of modulation expression. However, OMS4 is essentially an approximating method, and this means that the effectiveness on conduction losses reduction is not as good as OMS1 which can achieve minimum leakage inductance current $I_{s,rms}$. Hence the relative error calculated by (33) is used to measure the deviation from the minimum $I_{s,rms}$.

$$i_{err} = \frac{|I_{s,rms,OMS4} - I_{s,rms,OMS1}|}{I_{s,rms,OMS1}} \cdot 100\% \qquad (33)$$

For comparison, the values of $I_{s,rms}$ under SPS modulation is also calculated, and the following relative error between $I_{s,rms,sps}$ and the minimum $I_{s,rms,OMS1}$ is used to compare with (33).

$$i_{err,sps} = \frac{|I_{s,rms,sps} - I_{s,rms,OMS1}|}{I_{s,rms,OMS1}} \cdot 100\% \qquad (34)$$

The calculated results varying with different voltage ratios and normalized output powers are shown in Fig. 14. Therein,

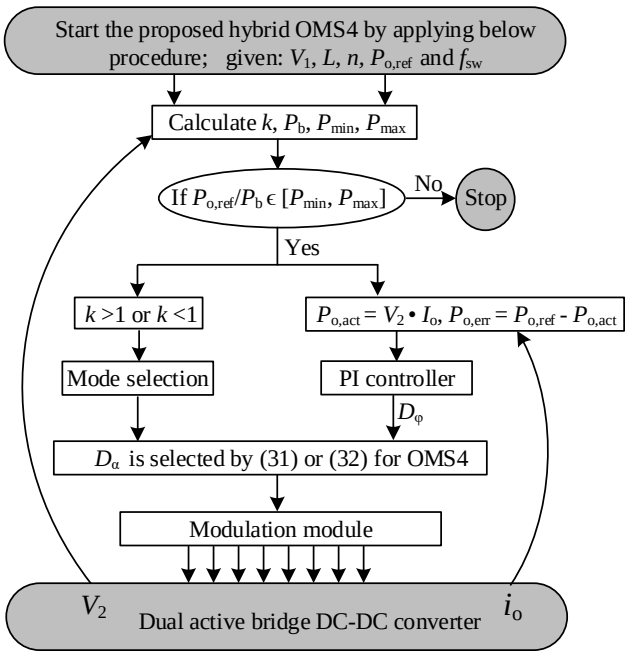


Fig. 15. Procedure of applying linearized modulation scheme (OMS4) to the DAB converter

P_5, P_{10} and P_{15} are the $k-$related output powers at the three boundary points (i.e. $[(1-k)/2, k]$, $[(k-1+\sqrt{1-k^2})/(2k), 1]$, $[0.5, 1]$ that define the three segments in OMS4 in boost scenarios). Then the various other power levels $P_i (i = 1..15)$ can be expressed by

$$P_i = \begin{cases} 0.2 \cdot i \cdot P_5, & i = 1..5 \\ P_5 + 0.2 \cdot (i-5) \cdot (P_{10} - P_5), & i = 6..10 \\ P_{10} + 0.2 \cdot (i-10) \cdot (P_{15} - P_{10}), & i = 11..15 \end{cases} \qquad (35)$$

with

$$P_5 = 2k^2(1-k), P_{10} = \frac{2(k^2 - 1 + \sqrt{1-k^2})}{k}, P_{15} = k \qquad (36)$$

From Fig. 14, it can be seen that $i_{err,sps}$ is larger than $i_{err,OMS4}$, especially in light load and medium load. When the voltage ratio k is 0.6, the maximum $i_{err,sps}$ even exceeds 100%. Consequently, it can be obtained that OMS4 is more applicable to the DAB converter, especially when the converter works in light load and the voltage ratio deviates far from unity. On the other hand, comparing $I_{s,rms,OMS4}$ with the optimal $I_{s,rms,OMS1}$, the relatives errors i_{err} are very small (less than 2%) for various voltage ratios and output power levels, especially in medium and high power load ($P_5 \sim P_{15}$, less than 0.5%), which proves the effectiveness of linearized modulation scheme on reducing the conduction losses. The process of applying OMS4 to the DAB converter is illustrated in Fig. 15.

An experimental platform for the DAB converter is built to validate the linearized modulation scheme OMS4, as shown in Fig. 16. The main circuit parameters are listed in Table VIII.

In order to fully evaluate the performance improvement caused by linearized modulation scheme, two groups of com-

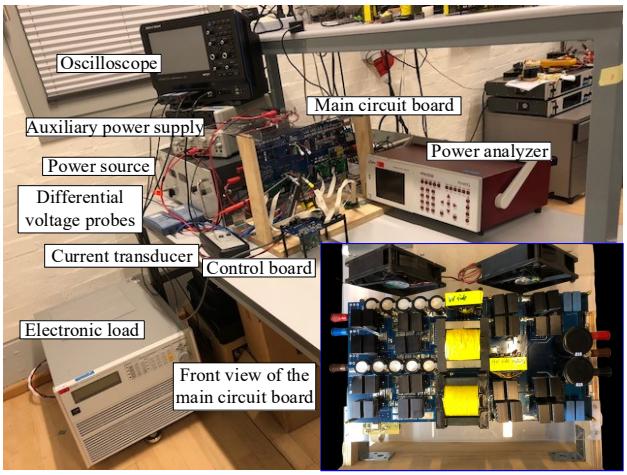


Fig. 16. Test platform for the DAB converter

TABLE VIII
SYSTEM SPECIFICATIONS

Parameters	Description	Value
P	Rating power	1.5 kW
$n:1$	Turns ratio of the transformer	3.5 : 1
f_{sw}	Switching frequency	60 kHz
T_{dead}	Dead time	400 ns
L_s	Series inductor	36.2 μH
L_{trp}	Primary-side leakage inductance	4.5 μH
L_{trs}	Secondary-side leakage inductance	372.5 nH
C_1	Primary DC capacitor	0.78 mF
C_2	Secondary DC capacitor	1.5 mF

parative experiments are conducted for each mode: group one (G1) adopts the optimized linear modulation (OMS4) and the other group (G2) does not use any optimized scheme (but still modulated by EPS). Moreover, for the purpose of highlighting the effect of the conduction losses, the operating points of two groups are both located within the ZVS range. As shown in IV-B3, the piecewise linear scheme has three segments. Therefore, for either boost or buck scenarios, the measured working waveforms with three different output power levels are shown in the following.

In Mode I, the steady state waveforms of the DAB converter are illustrated in Fig. 17, where v_p and v_s are voltage waveforms generated by HB_1 and HB_2, and i_p, i_s are the primary and secondary transformer current, respectively. Fig. 17(a) shows the measured waveforms when the DAB converter works without adopting any optimized modulation (belongs to G2). Fig. 17(b) shows the working waveforms when the converter is modulated by linearized scheme (belongs to G1). The output power for both situations is given at 190 W. As marked in the figure, the value of $I_{s.rms}$ in Fig. 17(b) is lower than that in Fig. 17(a), indicating the effectiveness of OMS4 in reducing the conduction losses of the DAB converter. As a result, the overall system efficiency is improved from 92.5% to 95 %. Besides, in order to directly see if the ZVS is achieved, the drain-source voltage and the gate signal of S_7 (turned on at the rising edge of v_s) are illustrated in Fig. 17(c) and Fig.

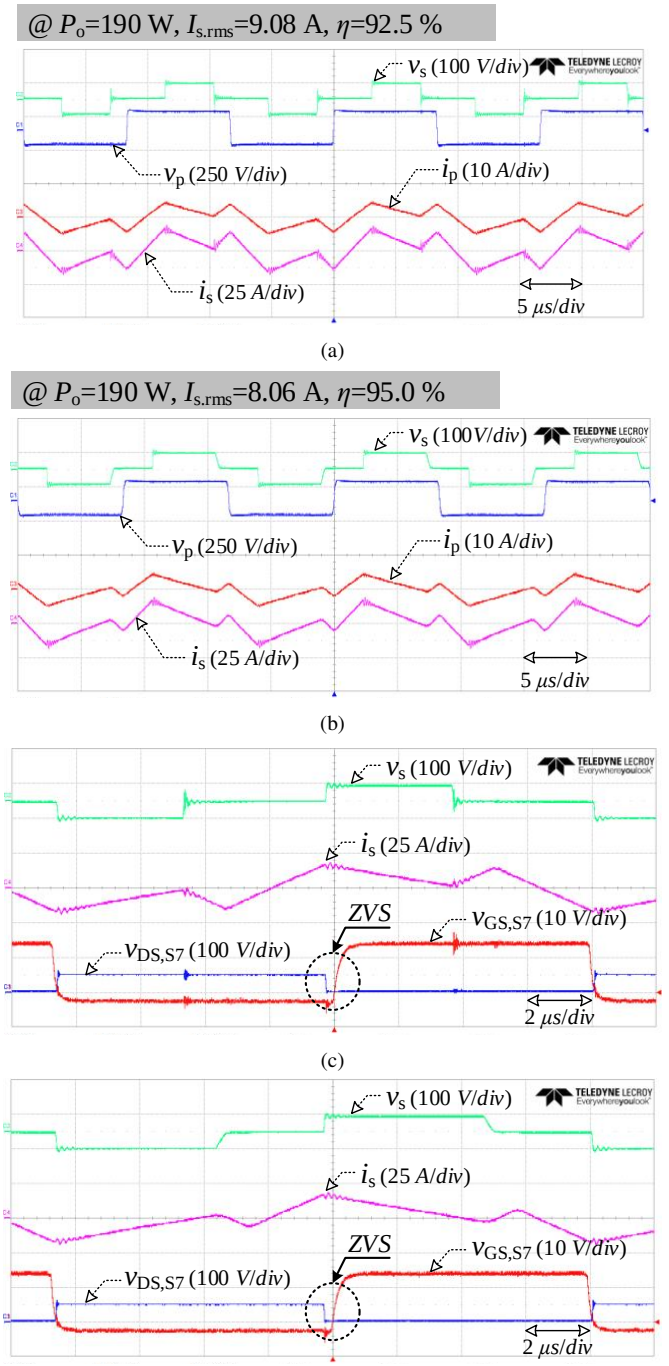


Fig. 17. Experimental waveforms of DAB converter in Mode I where V_1=120 V, V_2=46 V ($k = 0.75$) (a) working waveforms without optimized modulation (b) working waveforms with linearized modulation scheme (c) ZVS realization without optimized modulation (d) ZVS realization with linearized modulation scheme.

17(d), corresponding to the working conditions in Fig. 17(a) and Fig. 17(b), respectively. It can be seen that the switching-on signal (i.e. rising edge) of $v_{GS,S7}$ comes after the drain-source voltage $v_{DS,S7}$ becoming zero, which implies that the transistor S_7 has achieved zero-voltage turn-on.

In Mode II, the converter is operated at two power levels (i.e. 430 W and 700 W) and the working waveforms are shown in Fig. 18 and Fig. 19, respectively. Although there

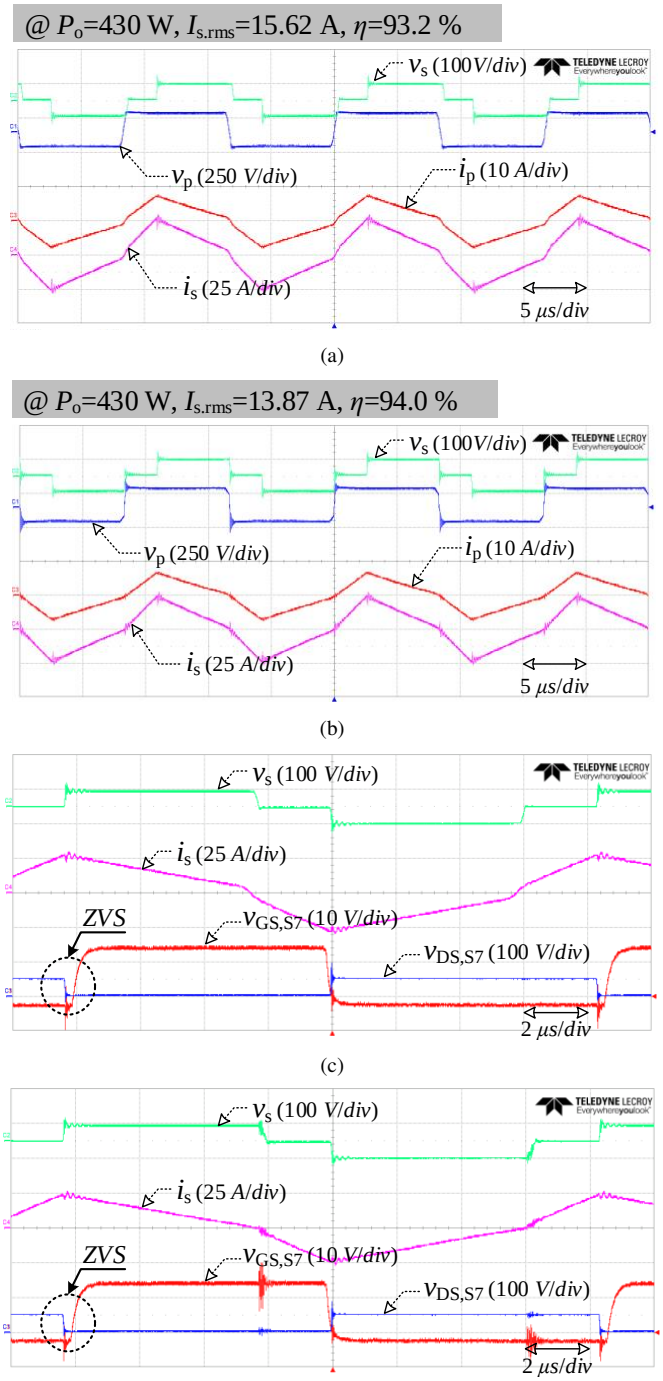


Fig. 18. Experimental waveforms of DAB converter in Mode II where V_1=120 V, V_2=46 V ($k = 0.75$) (a) working waveforms without optimized modulation (b) working waveforms with linearized modulation scheme (c) ZVS realization without optimized modulation (d) ZVS realization with linearized modulation scheme.

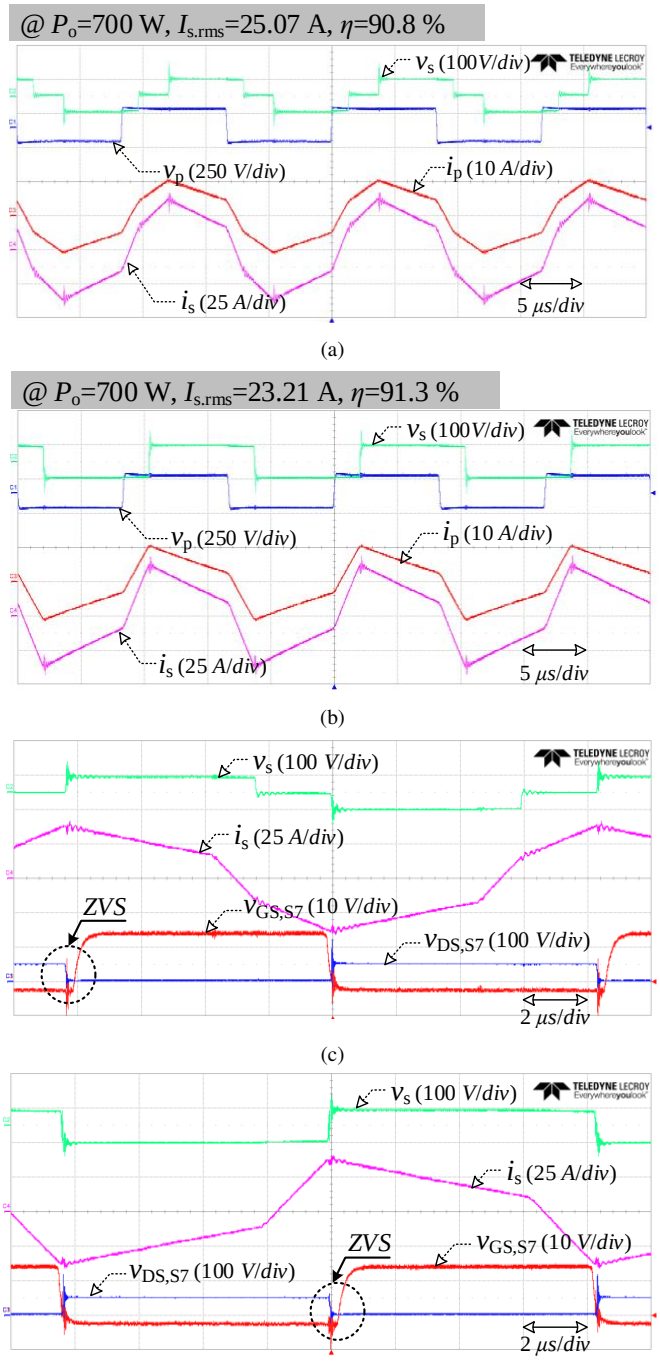


Fig. 19. Experimental waveforms of DAB converter in Mode II where V_1=120 V, V_2=46 V ($k = 0.75$) (a) working waveforms without optimized modulation (b) working waveforms with linearized modulation scheme (c) ZVS realization without optimized modulation (d) ZVS realization with linearized modulation scheme.

are some oscillations at the switching-on instants of S_7, the voltage across S_7 is kept at zero when the gate signal reaches high level, thus ZVS is still guaranteed in these two higher power situations. On the other hand, compared to Fig. 18(a) and Fig. 19(a), the converter efficiency is improved when the optimized linear modulation scheme is utilized in Fig. 18(b) and Fig. 19(b), respectively.

In terms of buck scenarios, Fig. 20 $\sim$ Fig. 22 present the corresponding waveforms for Mode III and Mode IV, respectively. Similar conclusions can be achieved with reduced conduction losses and improved efficiency. Also, the ZVS is realized at different output power levels.

Besides, the linear OMS4 is essentially a hybrid modulation scheme, consisting of EPS in light, medium load and SPS in heavy load. This can be seen from the expressions (31) and (32) and the working waveforms in Fig. 19 and Fig. 22. By switching the converter between light load and heavy load with

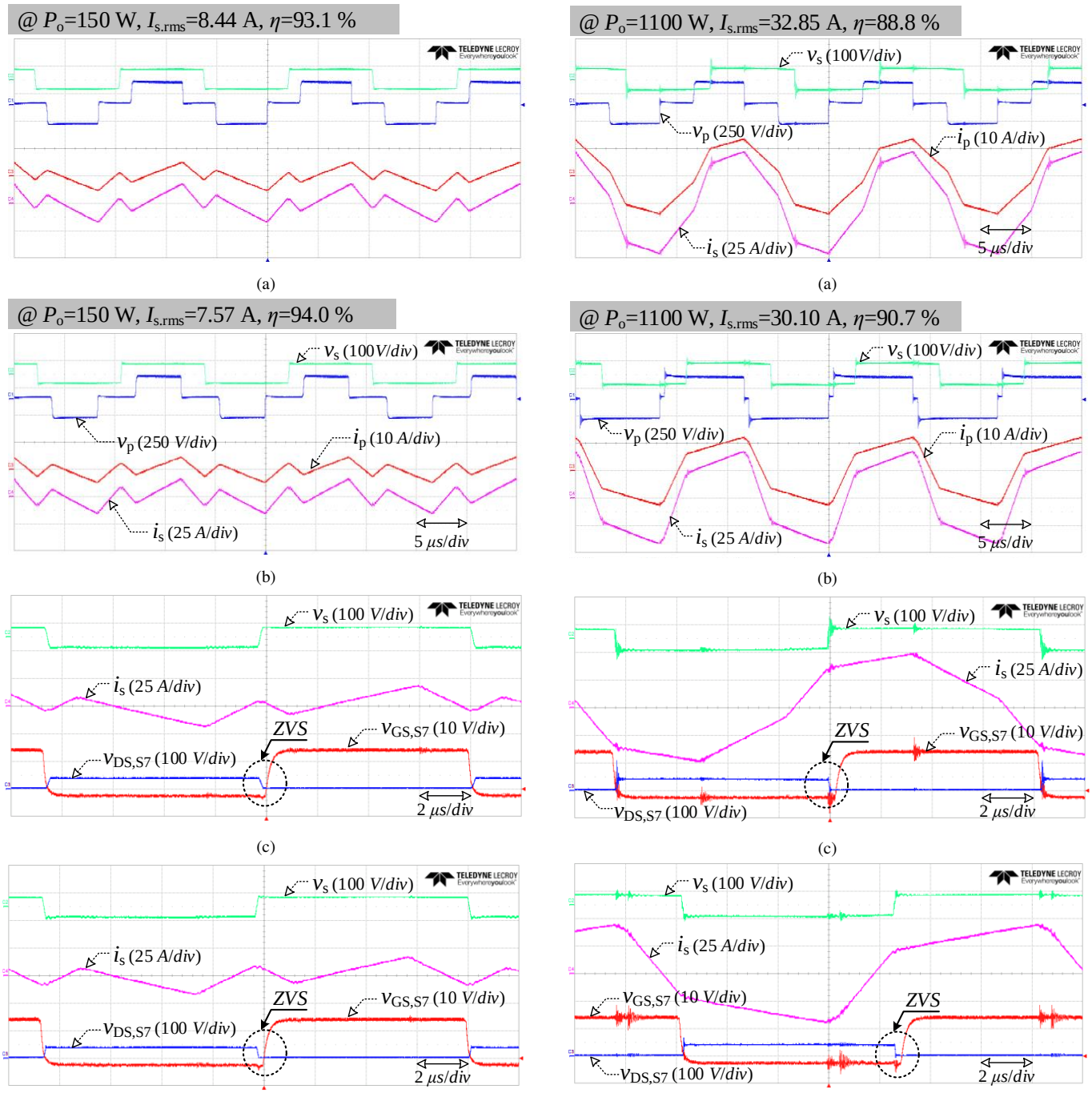


Fig. 20. Experimental waveforms of DAB converter in Mode III where V_1=190 V, V_2=36 V ($k = 1.5$) (a) working waveforms without optimized modulation (b) working waveforms with linearized modulation scheme (c) ZVS realization without optimized modulation (d) ZVS realization with linearized modulation scheme.

Fig. 21. Experimental waveforms of DAB converter in Mode IV where V_1=190 V, V_2=36 V ($k = 1.5$) (a) working waveforms without optimized modulation (b) working waveforms with linearized modulation scheme (c) ZVS realization without optimized modulation (d) ZVS realization with linearized modulation scheme.

OMS4, the dynamic response is shown in Fig. 23, where V_2 is the output dc voltage, i_o is the output current and i_s is the leakage inductance current referred to the secondary side. The power is increased from 150 W to 700 W in Fig. 23(a) and then decreased in Fig. 23(b). Part of i_s is amplified in green frames for having a clear view on the current shape of i_s. It can be seen that the converter can smoothly changes from EPS to SPS or reverse depending on the power condition.

Furthermore, the input and output voltage are changed to operate the converter with different voltage ratios, and the measured efficiency curves are shown in Fig. 24. Corresponding to boost and buck scenarios, Fig. 24(a) ($k = 0.9$) and Fig. 24(b) ($k = 1.2$) plot the converter efficiency at different output powers. In the figure, three situations are illustrated: the red curve denotes the linearized modulation scheme (belongs to G1), the blue curve represents the normal EPS modulation without any optimization (belongs to G2) and the black curve

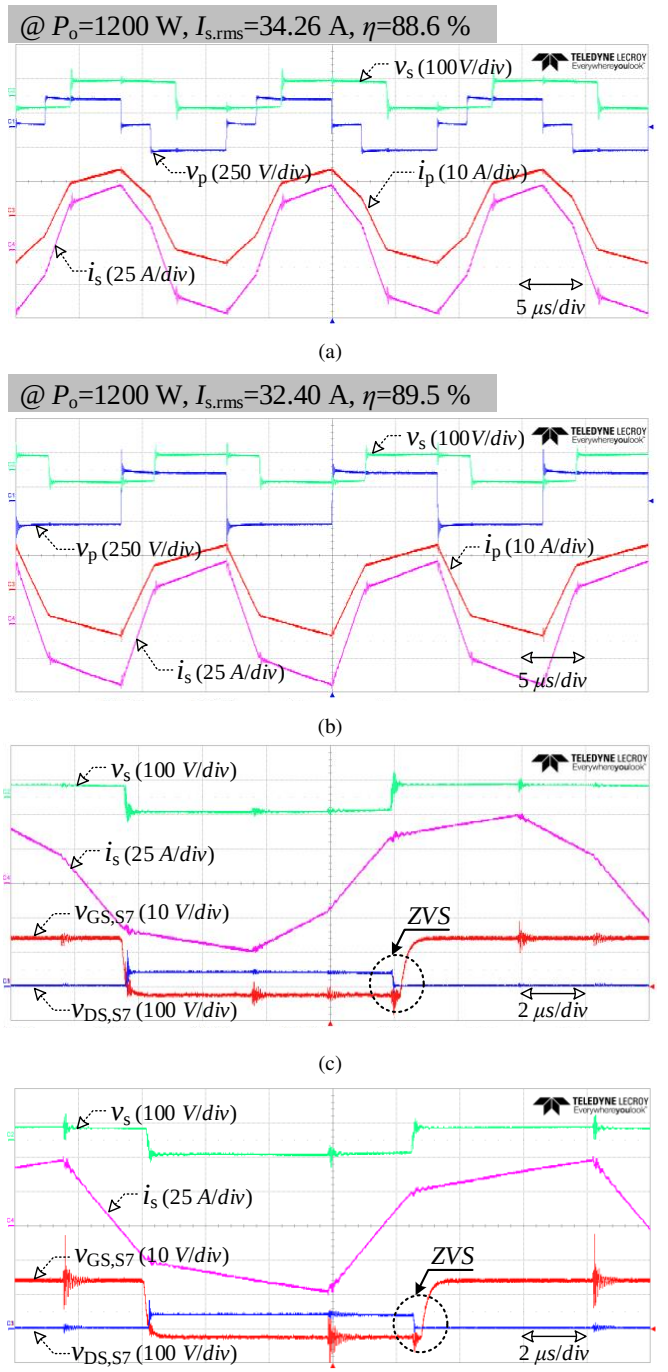


Fig. 22. Experimental waveforms of DAB converter in Mode III where V_1=190 V, V_2=36 V ($k = 1.5$) (a) working waveforms without optimized modulation (b) working waveforms with linearized modulation scheme (c) ZVS realization without optimized modulation (d) ZVS realization with linearized modulation scheme.

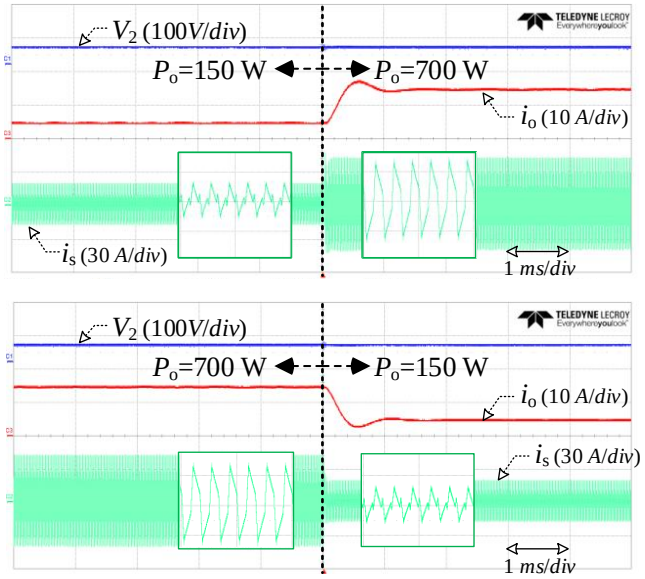


Fig. 23. Dynamic response with the output power (a) increased from 150 W to 700 W (b) decreased from 700 W to 150 W in boost scenario (V_1=120 V, V_2=46 V).

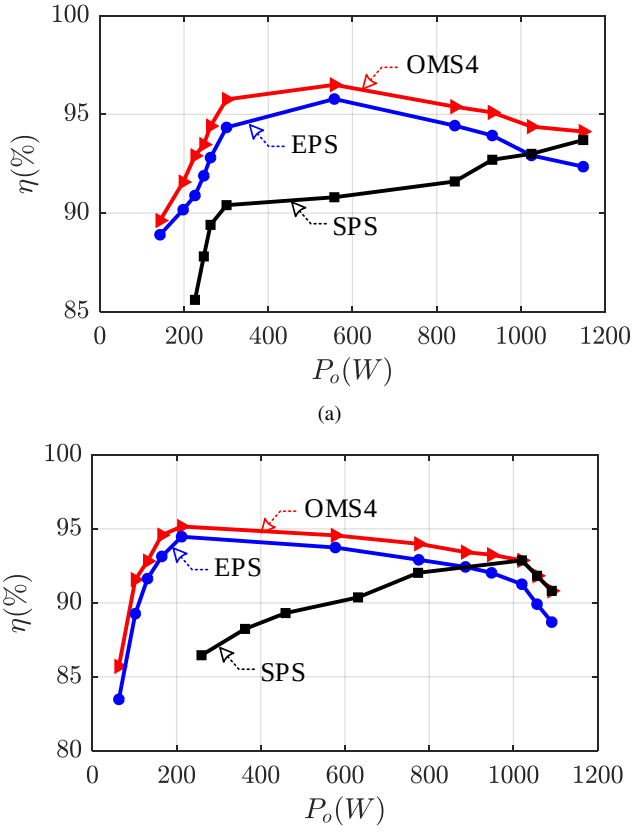


Fig. 24. Measured efficiency curves of the DAB converter for different output power levels, where the red curve, blue curve and black curve denote the converter efficiencies with linear modulation scheme (G1), without any optimization (G2) and with SPS, respectively. (a) Boost operation, V_1=190 V, V_2=60 V ($k = 0.9$) (b) Buck operation, V_1=190 V, V_2=45 V ($k = 1.2$).

is the resulted efficiency by applying SPS over the whole power range. Among the three situations, the linearized modulation scheme has a better efficiency performance in either boost or buck scenarios. In light load, due to the ZVS failure in SPS (black curve), the induced switching losses result in lower efficiency compared to the other two situations (G1 and G2). When the converter works with higher output power, the linearized modulation transfer into SPS scheme and thus the red curve and the black curve are overlapped in heavy load

conditions. In terms of G2 (blue curve), since it can also achieve ZVS, the efficiency is higher than SPS in light and medium load, but lower than G1 because of the larger leakage inductance current.

VI. Conclusions

In order to reduce the conduction losses of the DAB converter and still keep other performance parameters unchanged, an optimized hybrid modulation scheme is proposed in this paper. On the basis of achieving ZVS over the whole operation range and maintaining the same power transfer ability as the single phase shift modulation, an optimal modulation scheme is firstly derived with minimum leakage inductance current. By exploring the possibility to further simplify the relationship functions between the control variables, three other modulation schemes are presented considering various voltage ratio requirements and working conditions for the DAB converter. Therein, the linearized modulation scheme is prominent with less complexity after a through comparative analysis and thus is selected as the focus of this paper. By operating the converter with linear modulation scheme, the conduction losses can be effectively reduced and the system efficiency is improved. Comparative experiments are implemented to highlight the conduction losses reduction and in addition, the experimental results also validate the ZVS realization with linear modulation.

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