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New High Voltage Gain DC-DC Converter based on modified Quasi Z-Source Network

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***Abstract*—In this paper, a new non-isolated high voltage gain DC-DC converter using a combination of the modified quasi Z-Source and switched-capacitor networks is proposed. The proposed DC-DC converter has an acceptable number of elements and shows the low voltage stresses for its semiconductors and capacitors. Moreover, the voltage gain of the proposed converter is significantly high, where it can achieve high voltage gains with lower duty cycles compared to the other similar converters. In addition, the steady-state analysis is given along with the passive elements design. Then, the proposed converter is compared with similar converters to highlight its advantages and drawbacks. Finally, the simulation results in PSCAD/EMTDC software are given to validate the theoretical analysis.**

Keywords—Quasi Z-Source; non-isolated DC-DC converter; high voltage gain; switched-capacitor

I. INTRODUCTION

Renewable energy sources like fuel cells, wind and solar are becoming more popular considering the disadvantages of fossil fuels. However, renewable energy sources can only provide an output voltage of 12 to 80 V_{DC}, which is not desirable in industrial applications with the desired voltage of 200, 400 or 600 V_{DC} [1,2]. As a result, high voltage gain DC-DC converters are essential in the mentioned applications. Isolated and non-isolated converters are two major categories of the DC-DC converters. A high-frequency transformer is used in the topology of the isolated DC-DC converters, which provides the galvanic isolation between the input source and the load. Moreover, turns ratio of the transformer enhances the boosting capability of the isolated converters [3].

However, the high number of components leads to a high cost, large volume and low efficiency for the isolated DC-DC converters. In addition, the saturation possibility for the transformer is another disadvantage of the isolated converters. Conventional non-isolated DC-DC converters represent lower voltage gains compared to the isolated ones. However, non-isolated converters, usually, employ a lower number of the components and have a simpler structure compared to the isolated ones. The major problem of the non-isolated DC-DC converters is their low voltage gain, which restricts their applications in industry [4].

Various techniques and topologies have been presented to increase the voltage gain of the non-isolated DC-DC converters. Cascaded [5] and voltage-lift techniques [6], using switched-capacitor (SC) [7], switched-inductor (SL) [8] and multiplier cells [9] are the major methods for increasing the voltage gain of the converters. Z-source converters [10] can provide higher voltage gain compared to the conventional voltage/current-fed converters. In addition, Z-source based converters like quasi Z-source (qZS) [11], switched boost (SB) [12] and quasi switched-boost (qSB) [13] converters have been introduced to achieve higher voltage gain and power density compared to the conventional converters. Combination of the mentioned techniques can further enhance the boosting capability of the non-isolated DC-DC converters.

Combination of the qZS converter and a voltage-lift cell has resulted in a high voltage gain DC-DC converter in [14]. However, this converter suffers from the high voltage stresses on the switches and diodes and, also, a high number of the inductors. The proposed converter in [15] is introduced by the combination of the qZS converter and the cascading technique. The presented converter in [16] uses a qZS network and voltage multiplier cell to improve the voltage gain.

In [17], the SL network has been combined with the qZS network to improve the boosting capability. The voltage gain of this converter has been improved at the cost of high voltage stress on the semiconductors. Likewise, the SC network has been combined with the qZS network in [18] to improve the voltage gain, however, this improvement is not significant.

In [19], both of the SC and SL networks are employed to improve the voltage gain of the SB network. The improvement of the voltage gain in this converter is not remarkable, while it uses a high number of inductors and diodes. The voltage gain of the presented DC-DC converter in [20] is double of the conventional qZS DC-DC converter. On the other hand, this topology demands a high number of the diodes and capacitors. The high voltage gain qZS converter in [21] represents low voltage stress on its capacitors and a high voltage gain. However, this topology uses a high number of capacitors and inductors, which will increase its size, cost, weight and losses. A hybrid Z-source boost DC-DC converter is presented in [22] with high step-up capability using qZS networks in its topology. However, this converter this converter has a high number of passive elements.

In this paper, a new non-isolated high voltage gain DC-DC converter using combination of modified quasi Z-Source network and switched-capacitor cells is proposed. The proposed converter can achieve high voltage gains in lower duty cycles compared to some selected converters. In addition, the voltage stresses on the semiconductors and capacitors are low. In this paper, the proposed converter is introduced in section II, then the steady-state analysis is done in section III. Passive components design based on the steady-state analysis is done in section IV. The proposed converter is compared

with the similar converters in section V. Finally, the simulation results are represented in sections VI.

II. The Proposed Topology

The proposed topology is shown in Fig. 1. The proposed converter consists of two main parts: The modified qZS network and the switched capacitor network. The modified qZS network is comprised of inductors L_1 and L_2, capacitors C_1, C_2 and C_3, diodes D_1, D_2 and D_3 and switch S_1. In addition, switch S_2, diode D_4 and capacitor C_4 consist the switched-capacitor network. Diode D_5 connects the positive terminal of the input voltage to the positive terminal of the output voltage and C_o is the output capacitor.

III. Steady-State Analysis

The proposed converter has two operating modes, which the equivalent circuit of each operating mode is depicted in Fig. 2.

Mode 1 [$t_0 \le t < t_1$]

The first mode starts by turning off the switches S_1 and S_2 and reverses bias of the diode D_5. This condition results in forward bias of diodes D_1, D_2, D_3 and D_4. In this mode, L_1, L_2 and C_2 are discharging, while, C_1, C_3 and C_4 are charging. Thus, the following equations are given:

$$\begin{cases} v_{L1} = V_{in} + V_{C2} - V_{C3}, \; v_{L2} = -V_{C2} \\ V_{C1} = V_{C2} \\ V_{C3} = V_{C4} \end{cases} \tag{1}$$

$$\begin{cases} I_{in} = I_{L1}, \; i_{C1} + i_{C2} = I_{L2} - I_{L1}, \\ i_{C3} + i_{C4} = I_{L1} \end{cases} \tag{2}$$

$$\begin{cases} v_{S1} = -V_{C3}, \; v_{S2} = -V_{C4} \\ V_{D5} = V_{in} - V_o \end{cases} \tag{3}$$

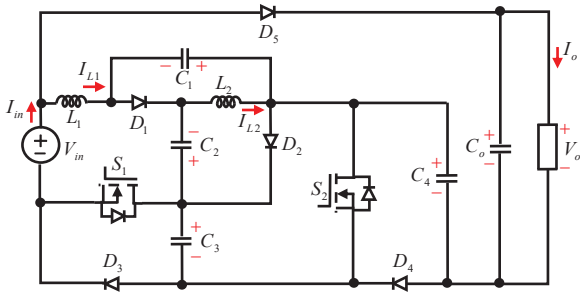
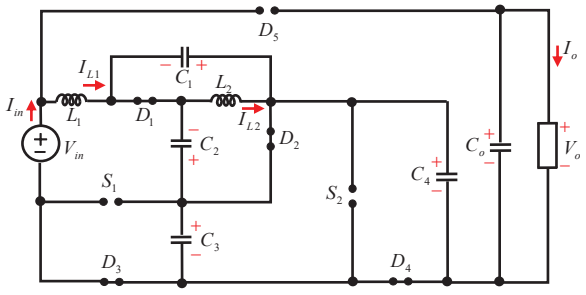
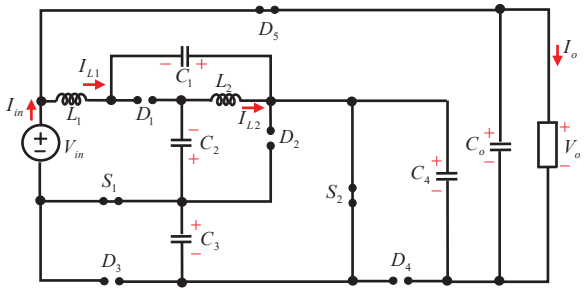


Fig. 1. Proposed high step-up DC-DC converter



(a)



(b)

Fig. 2. Equivalent circuits of the proposed converter. (a) Mode 1. (b) Mode 2.

In the above equations, V_{C1}, V_{C2}, V_{C3} and V_{C4} are the average voltages across C_1, C_2, C_3 and C_4, respectively. V_{in} is the input voltage and V_o is the output voltage. v_{L1} and v_{L2} are the voltages across L_1 and L_2, respectively. Moreover, I_{L1} and I_{L2} are the average current flowing through L_1 and L_2, respectively. i_{C1}, i_{C2}, i_{C3} and i_{C4} are the currents flowing through the capacitors C_1, C_2, C_3 and C_4, respectively. I_{in} is the input current. v_{S1} and v_{S2} present the voltages across S_1 and S_2. Also, v_{D5} is the voltage across D_5.

Mode 2 [$t_1 \le t < t_2$]

In the second operating mode, S_1, S_2 and D_5 are conducting, while other semiconductors are off. This condition leads to charging of L_1, L_2 and C_2, besides discharging of C_1, C_3 and C_4. The following equations are valid for the second operating mode.

$$\begin{cases} v_{L1} = V_{in} + V_{C3} + V_{C1}, \; v_{L2} = V_{C3} - V_{C2}, \\ V_o = V_{in} + V_{C3} + V_{C4} \end{cases} \tag{4}$$

$$\begin{cases} i_{C1} = -I_{L1}, \; i_{C2} = I_{L2}, \; i_{C3} = -I_{in} - I_{L2}, \\ i_{C4} = I_{L1} - I_{in}, \; I_{L1} = I_{in} - I_o \end{cases} \tag{5}$$

Voltages across the non-conducting elements are as follows:

$$\begin{cases} v_{D1} = V_{C2} - V_{C1} - V_{C3} \\ v_{D2} = v_{D3} = -V_{C3} \\ v_{D4} = -V_{C4} \end{cases} \tag{6}$$

where, v_{D1}, v_{D2}, v_{D3} and v_{D4} represent the voltages across D_1, D_2, D_3 and D_4, respectively. The switching period ends with turning off the switches. Fig. 3 shows the steady-state operating waveforms of the components consist the proposed DC-DC converter. The switching algorithm of the switches is based on PWM algorithm and both of the switches S_1 and S_2 has the same gating pulses. Considering the voltage balance law of the inductors during one switching cycle and Fig. 3, the average voltages across the capacitors

and the voltage gain of the proposed converter can be asserted as follows:

$$\begin{cases} V_{C1} = V_{C2} = \dfrac{D}{1-3D} V_{in} \\ V_{C3} = V_{C4} = \dfrac{1}{1-3D} V_{in} \\ G = \dfrac{V_o}{V_{in}} = \dfrac{3(1-D)}{1-3D} \end{cases} \quad (7)$$

Based on the proposed converter's voltage gain equation, it can achieve high voltage gains in low duty cycles and with low voltage stress on the capacitors.

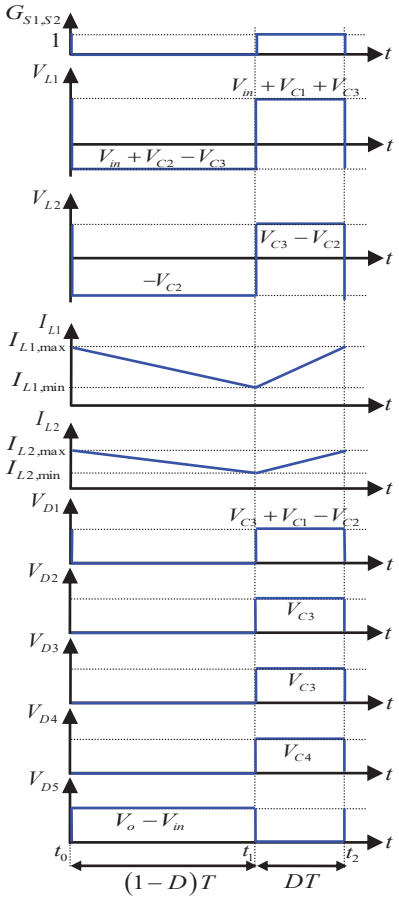


Fig. 3. Steady-state waveforms of the proposed converter.

IV. Passive Components Design

A. Inductor design

The current ripple of inductor L_1 can be obtained by substituting (1) and (7) in $V_L = L\dfrac{di}{dt}$ as follows:

$$\Delta I_{L1} = \frac{2D(1-D)}{L_1 f_s (1-3D)} V_{in} \quad (8)$$

f_s is the switching frequency in the above equation. Likewise, the current ripple of inductor L_2 is given as follows:

$$\Delta I_{L2} = \frac{D(1-D)}{L_2 f_s (1-3D)} V_{in} \quad (9)$$

Considering the current balance law during one switching period for C_1 and C_2, leads to the following equations for the average value of the currents flowing through the inductors.

$$I_{L1,ave} = I_{in} - I_o = \frac{G^2 V_{in}}{R} - \frac{G V_{in}}{R} = \frac{6(1-D)}{R(1-3D)^2} V_{in} \quad (10)$$

$$I_{L2,ave} = I_{L1,ave} \quad (11)$$

Inductors equations can be obtained by considering (8), (9), (10), (11) and the inductor current ripple factor ($x_L\% = \Delta I_L / I_{L,ave}$) as follows:

$$L_1 = 2L_2 = \frac{RD(1-3D)}{3x_{L1}\% f_S} \quad (12)$$

B. Capacitor Design

Substituting (5) in $I_C = C\dfrac{dV_C}{dt}$, besides considering (10) and (11) results the following equation for the voltage ripple of the capacitors.

$$\begin{cases} \Delta V_{C1} = \Delta V_{C2} = \dfrac{3D(1-D)(3D^2-4D+3)}{C_{1or2} f_s R (1-3D)^2} V_{in} \\ \Delta V_{C3} = \dfrac{3D(1-D)(3D^2-7D+6)}{C_3 f_s R (1-3D)^2} V_{in} \\ \Delta V_{C4} = \dfrac{3D^2(1-D)}{C_4 f_s R (1-3D)} V_{in} \end{cases} \quad (13)$$

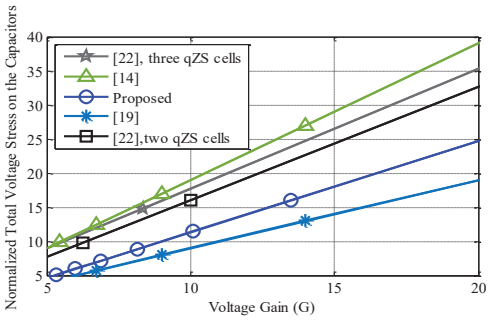
The capacitors values can be derived by considering (7), (13) and the capacitor voltage ripple factor ($x_C\% = \Delta v_C / V_C$) as follows:

$$\begin{cases} C_{1,2} = \dfrac{3(1-D)(3D^2-4D+3)}{x_{C1,2}\% f_s R (1-3D)} \\ C_3 = \dfrac{3D(1-D)(3D^2-7D+6)}{x_{C3}\% f_s R (1-3D)} \\ C_4 = \dfrac{3D^2(1-D)}{x_{C4}\% f_s R} \end{cases} \quad (14)$$

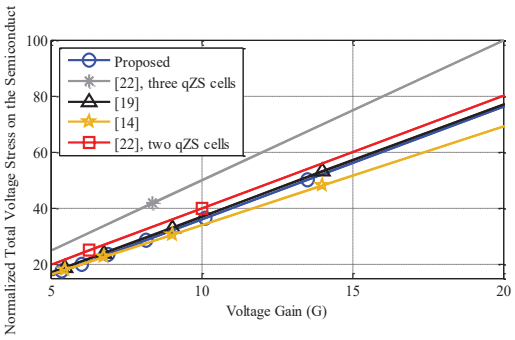
V. Comparison with Similar Converters

For better clarification of features and drawbacks of the proposed high step-up DC-DC converter, a comprehensive comparison is done among the similar structures with almost the same variation range of the duty cycle in Table I. Based on Table I, the presented converter in [14] has the lowest number of active elements, while the presented converter in [19] has the highest number of them. In addition, the

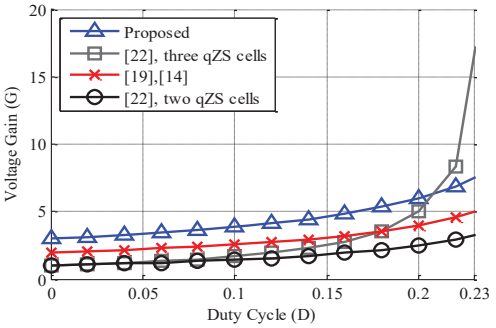
presented converters in [19] have the lowest number of passive elements. The proposed converter has the third lowest total number of elements in Table I. In addition, the presented converter in [22] with three qZS cells has the limited variation range for its duty cycle. Furthermore, the voltage stress of the capacitors, switches and diodes are compared in Table I. For better demonstration, the comparison of the voltage gain, the normalized total voltage stress on the capacitors and the normalized total voltage stress on the switches and diodes are shown in Fig. 4. Based on Fig. 4(a) and Table I, the presented converter in [19] has the lowest total voltage stress on its capacitors in the same voltage gain. The proposed DC-DC converter has the second lowest total voltage stress on the capacitors.



(a)



(b)



(c)

Fig. 4. Comparison of the parameters for presented converters in Table I. (a) The normalized total voltage stress on capacitors versus the voltage gain. (b) The voltage gain versus the duty cycle. (c) The voltage gain comparison.

Table I. Comparison of the similar high step-up DC-DC converters.

Parameters		Proposed converters	[22]		SL/SC-SBC[19]	[14]
			Two qZS cells	Three qZS cells		
Component number		$2S$, $5D$, $2L$, $5C$	$1S$, $3D$, $3L$, $5C$	$1S$, $4D$, $4L$, $7C$	$2S$, $7D$, $2L$, $3C$	$1S$, $3D$, $4L$, $4C$
Voltage stress	Switches	$\frac{GV_{in}}{3(1-D)}$	GV_{in}	GV_{in}	$\frac{DGV_{in}}{1-D}, \frac{GV_{in}}{2}$	GV_{in}
	Power diodes	$\frac{GV_{in}}{3(1-D)}$, $(G-1)V_{in}$	GV_{in}	GV_{in}	$\frac{DGV_{in}}{1-D}, \frac{GV_{in}}{2}$ $\frac{DGV_{in}}{2(1-D)}$	$\frac{GV_{in}}{1-D}, \frac{GV_{in}}{2}$
Capacitor voltage		$\frac{DGV_{in}}{3(1-D)}$, $\frac{GV_{in}}{3(1-D)}$	$DGV_{in}, 2DGV_{in}$ $(1-2D)GV_{in}$	$(1-2D)GV_{in}, DGV_{in}$ $(1-3D)GV_{in}, 2DGV_{in}$	$\frac{DGV_{in}}{1-D}, \frac{GV_{in}}{2}$	$\frac{GV_{in}}{2}, \frac{(1+D)GV_{in}}{2(1-D)}$
Duty cycle variation range		$0 < D \le 0.33$	$0 < D \le 0.33$	$0 < D < 0.25$	$0 < D \le 0.33$	$0 < D \le 0.33$
Voltage gain (G)		$\frac{3(1-D)}{1-3D}$	$\frac{1}{1-3D}$	$\frac{1}{1-4D}$	$\frac{2(1-D)}{1-3D}$	$\frac{2(1-D)}{1-3D}$

Based on Fig. 4(b) and Table I, the presented converter in [14] and the proposed converter have the lowest and second lowest total voltage stress on their semiconductors, respectively. Finally, according to Fig. 4(c) and Table I, the proposed converter has the highest voltage gain compared to the similar converters except for the duty cycles between 0.22 and 0.25. For the very limited range of duty cycles between 0.22 and 0.25, the presented converter in [22] with three qZS cells has the highest voltage gain.

VI. SIMULATION RESULTS

To verify the proper operation of the proposed converter, a simulation in PSCAD/EMTDC is performed using the values shown in Table II.

TABLE II. Values of the components used in the simulation.

Parameter	Value	Parameter	Value
V_{in}	$40V$	L_1 & L_2	$500\mu H$

$C_1,\ldots,C_5$	$470\mu F$	D	0.2
f_S	$50kHz$	R	400Ω
G	6	P_o	$144W$

The simulation results of the proposed converter are shown in Fig. 5. Based on Fig. 5(a), the proposed converter gives $V_o = 239V$, $V_{C1,2} = 20V$, $V_{C3,4} = 99V$, which are compatible with the theoretical values obtained from (7) with values of $V_o = 240V$, $V_{C1,2} = 20V$, $V_{C3,4} = 100V$. In addition, in Fig. 5(a), the maximum and minimum values of the voltages across the inductors are equal to $V_{L1,\max} = 158V$, $V_{L1,\min} = -39V$, $V_{L2,\max} = 79V$, $V_{L2,\min} = -19V$. These values are close to the values obtained from the steady state-analysis in (1) and (4). Moreover, Fig. 5(a) gives $I_{L1,ave} = I_{L2,ave} = 2.9A$ with current ripples equal to $\Delta I_{L1} = 2\Delta I_{L2} = 1.2A$. These simulation values for the currents flowing through the inductors are compatible with the theoretical values $I_{L1,ave} = I_{L2,ave} = 3A$, $\Delta I_{L1} = 2\Delta I_{L2} = 1.28A$ obtained from (8), (9), (10) and (11). Moreover, according to Fig. 5(b), the maximum voltage across the S_1 , S_2 , D_1 , D_2 , D_3 and D_4 is $99V$, while the voltage stress of D_5 is equal to $200V$. The mentioned voltage stresses across the semiconductors are compatible with the theoretical equations in (3) and (6) with the values of $v_{S1} = v_{S2} = v_{D1} = v_{D2} = v_{D3} = v_{D4} = 0.5v_{D5} = 100V$.

VII. Conclusion

In this paper, a new high step-up DC-DC converter using a modified quasi Z-Source network and SC network is proposed. The proposed converters could achieve high voltage gains using lower duty cycles compared to the similar converters. In addition, the proposed converter had an acceptable number of elements and lower voltage stresses on its elements. In this paper, the steady-state analysis with the design procedure is prepared. Then, a comparison with the similar literature, besides the simulation results verified the advantages and the proper operation of the proposed converter.

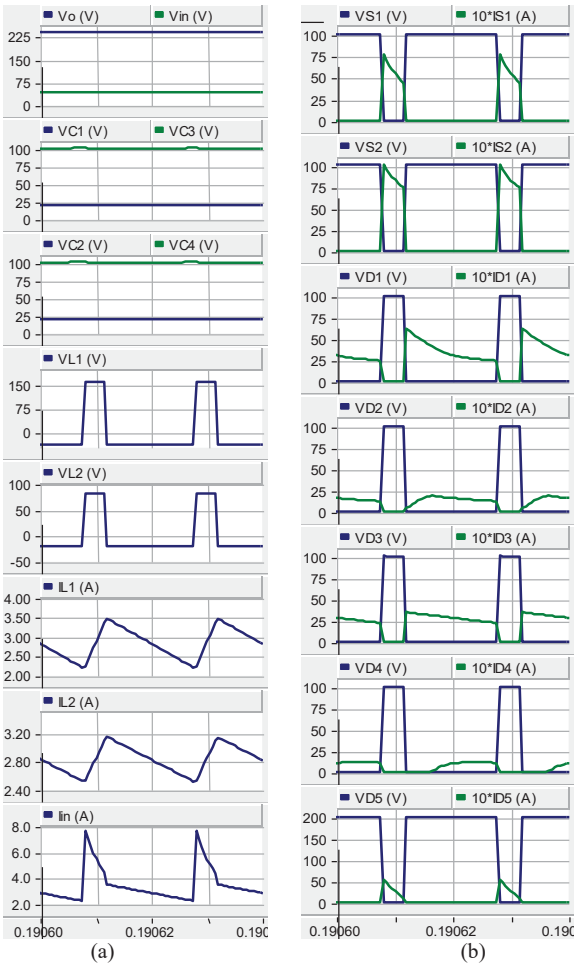


Fig. 5. Simulation results of the proposed converter. (a) Input and output voltages, voltages across and currents flowing through the inductors, voltages across the capacitors. (b) Input current and voltage stress of the semiconductors.

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