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Enhanced Zero-Voltage-Switching Conditions of Dual Active Bridge Converter Under Light Load Situations

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***Abstract*— Generally, power electronic converters are designed to obtain the highest efficiency at the rated power while they are partially loaded during most of their operation time. For dual active bridge (DAB) converters, the zero-voltage-switching (ZVS) is prone to failure in light load situations, where precise ZVS conditions are needed but the commonly used current-based and energy-based methods are not good enough to characterize the operating boundaries of the ZVS realization. In this paper, based on the practical turn-on procedure, an improved calculation method of the ZVS condition is introduced here. The method mainly focuses on analyzing the transient procedure during the dead time, by taking into account the non-linearity of the parasitic output capacitance of the transistors. Also, comparative experimental results are shown to validate the feasibility of the analysis.**

***Keywords*—zero voltage switching, dual active bridge, loss estimation**

I. Introduction

One advantage of the DAB converter [1] is the inherent capability of naturally achieving ZVS for all switches without any auxiliary circuits, and this advantage has facilitated a wide application of DAB converters, such as in distributed power systems and energy storage systems [2]–[10]. However, due to the lower leakage inductance current in light-load conditions, the energy stored in the transistor output capacitor may not be totally released during the dead time, and this may result in ZVS failure owing to the high voltage across the transistor at turn-on instant.

There are two commonly used methods to identify the limitations on the control variables for achieving ZVS, i.e. current-based method[11]–[14] and energy-based method [15]. Therein, the current-based method is developed from the body diode conduction when the power device is switched on and thus ZVS conditions can be attained by controlling a positive or negative leakage inductance current at switching instants. In other words, the leakage inductance current are controlled to be larger/smaller than zero at specific switching instants. However, the positive/negative current direction is the result of the ZVS achievement, which is not sufficient in order to guarantee soft-switching. In respect of the energy-based method, the ZVS is achieved under condition that the energy stored in the output capacitance is totally released before the transistor is switched on. Compared to the current-based method, this method is more accurate, which requires a minimum leakage inductance current at the switching instants, not just larger or smaller than zero. However, the non-linearity of the parasitic output capacitance is usually not taken into account, in spite of the fact that the output capacitance of a power device varies a lot during the turn-on/turn-off procedure. Owing to this missed consideration, the obtained ZVS range would contain some critical operating points that could lead to fully ZVS failure.

In this paper, a direct way to derive the zero 'voltage' switching condition is presented by practically analyzing the transient procedure during the dead time. Compared to the current and energy types of ZVS conditions, the proposed voltage-based ZVS conditions have a higher accuracy. Especially, the non-linearity of the parasitic output capacitance (C_{oss}) is also included in the derivation of the ZVS conditions. In the following, the current- and energy-based ZVS derivations are briefly introduced at first, followed by a detailed analysis of the proposed voltage-based method. Furthermore, experimental results are shown to validate the accuracy of obtained ZVS conditions based on the proposed method. In the end, the conclusions are summarized.

II. Conventional ZVS conditions

The DAB topology is shown in Fig. 1(a). Referring to the primary side of the transformer, during different sub-intervals, the leakage inductance current i_p is determined by the voltage drop on the leakage inductance L, which is

$$L \cdot \frac{di_p(t)}{dt} = v_p(t) - nv_s(t) \tag{1}$$

By operating the DAB converter with the generalized triple phase shift (TPS) modulation, the working waveforms of one typical light-load operation mode are as shown in Fig. 2, where D_p and D_s represent the duty cycles of the primary (v_p) and secondary (v_s) voltages of the transformer, respectively, and D_φ is the phase shift ratio between the fundamental components of v_p and v_s. By denoting T_{sw} as the switching period, $D_p \cdot T_{sw}/2$ is the high-level ($+V_1$) time of v_p, which is regulated by the inner phase shift between the transistor Q_1

and Q_4 in HB_1. The same meaning is used for $D_s \cdot T_{sw}/2$ in the secondary H-bridge HB_2.

In order to obtain the ZVS conditions for one transistor, the transient turn-on procedure is firstly introduced as follows. In the beginning, the parasitic output capacitance C_{oss} is discharged and the drain-source voltage v_{DS} of the transistor starts to decrease from the turn-off voltage (equal to V_1 for HB_1 transistors and V_2 for HB_2 transistors) to zero. Afterwards, the output capacitance is reversely charged until the voltage v_{Coss} ($v_{Coss} = v_{DS}$) is equal to the forward voltage ($-V_F$) of the anti-parallel body diode. Then the body diode is naturally conducting. During the diode-conducting interval, the drain-source voltage v_{DS} is almost zero and if the transistor is turned on at this moment, ZVS can be achieved. As a consequence, the current is always from the source terminal to the drain terminal when one transistor is softly turned on, and due to this, the direction of the leakage inductance current at switching instants can be confirmed. Together with (1) and the volt-second balance principle, the current-based ZVS imitations on the control variables D_p, D_s and D_φ can be solved. Besides, it can be derived that for the operation mode shown in Fig. 2, the voltage ratio $k = V_1/(nV_2)$ should be larger than 1 to guarantee ZVS for all switches in the converter.

Another type of energy-based ZVS condition is focusing on the energy balance between the transistor output capacitor and the leakage inductor. Through the soft-switching procedure, the key point is to ensure that the resonance between the output capacitors C_{oss} and the leakage inductor L can totally release the energy stored in C_{oss}. On this basis, the relation is $1/2LI_{sw}^2 > h/2C_{oss,eq}V^2$, where I_{sw} is the leakage inductance current at the switching instant, V is the off-state voltage of the transistor and h is the number of charging/discharging transistor output capacitors at the same switching instant. In this method, it requires a minimum value of I_{sw}, not simply larger or smaller than zero as in the current-based ZVS conditions.

Taking the soft turn-on of Q_4 as an example, which happens at the switching instant $t = t_3$ in Fig. 2, the current-based ZVS conditions of Q_4 can be solved as

$$i_p(t_3) = -I_3 = -\frac{nV_2}{4Lf_{sw}}\left[(k-1)D_p - 2D_\varphi\right] < 0 \longrightarrow \quad D_p > \frac{2}{k-1}D_\varphi \tag{2}$$

where I_3 is the absolute value of $i_p(t_3)$, as denoted in Fig. 2. f_{sw} is the switching frequency. At $t = t_3$, Q_1, Q_5, Q_8 are turned on, Q_3, Q_6, Q_7 are turned off, and the output capacitances of Q_2 and Q_4 start resonating with the leakage inductor, as shown in Fig. 1(b). Therefore, combined with (2), the energy-based ZVS conditions of Q_4 can be calculated with

$$\frac{1}{2}LI_3^2 > C_{oss,p}V_1^2 \quad \rightarrow \quad I_3 > V_1\sqrt{\frac{2C_{oss,p}}{L}} \xrightarrow{(2)} \quad D_p > \frac{2}{k-1}D_\varphi + \frac{4kf_{sw}}{k-1}\sqrt{2LC_{oss,p}} \tag{3}$$

by assuming $C_{oss,Q2} = C_{oss,Q4} = C_{oss,p}$.

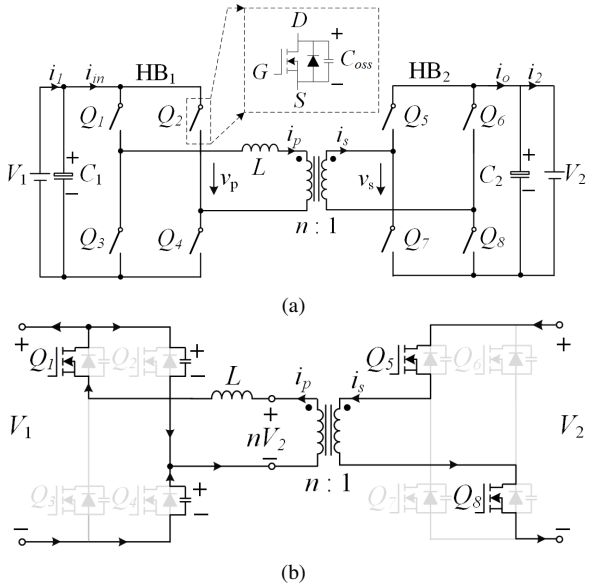


Fig. 1. Operation of the DAB converter (a) DAB topology. (b) Zero-voltage turn-on of Q_4.

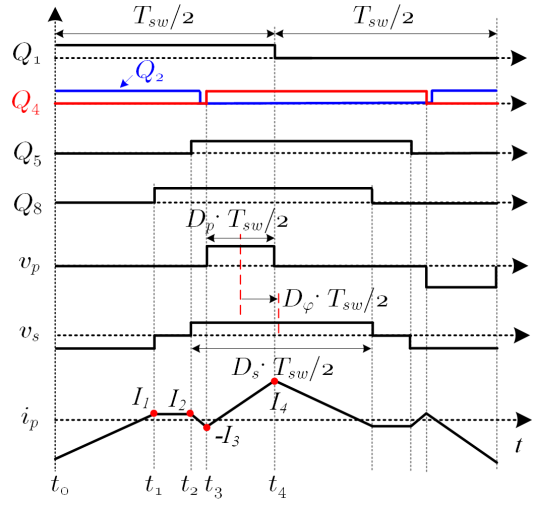


Fig. 2. Typical working waveforms at light load for the DAB converter in Fig. 1(a).

III. Improved ZVS Conditions

As explained in last section, the commonly used types of ZVS conditions are indirectly obtained from the perspective of current direction or energy balance. Both methods are developed based on the ideal switching on/off of the power semiconductor devices, leading to (partly) hard-switching operation within a large portion of the derived ZVS regions. In fact, due to the existence of the parasitic output capacitance, the drain-source voltage v_{DS} across the transistor changes softly from the off-state voltage to zero. This voltage changing process needs time to finish, which is within the generalized dead time in order to avoid short circuit. Furthermore, the non-linearity of the parasitic output capacitance (C_{oss}) is not correctly taken into account in both methods. The values of C_{oss} might change significantly depending on the varying drain-source voltage v_{DS} within the transient procedure. As given in the data sheet, Fig. 3 shows a typical characteristic

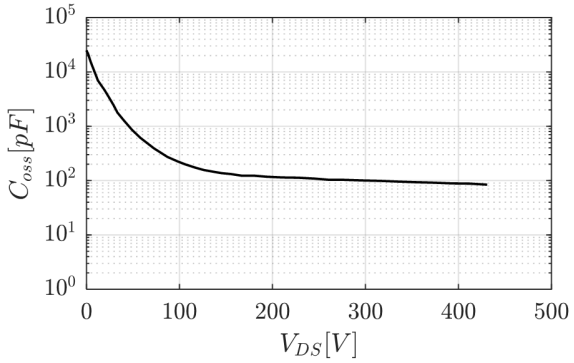


Fig. 3. Non-linear output capacitance $C_{oss}(v_{DS})$ of the used MOSFET IPW65R080CFD.

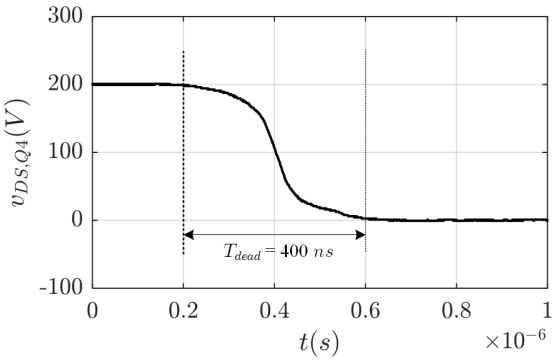


Fig. 4. Measured transient voltage of $v_{DS,Q4}$ during turn-on in a DAB prototype at $V_1 = 200\ V$.

of C_{oss} for the used power device IPW65R080CFD. If v_{DS} varies from 200 V to 0 V during the turn-on procedure, the actual output capacitance increases sharply from 118 pF to the highest 25000 pF, which is a large variation.

In order to further improve the accuracy of ZVS conditions, another type of voltage-based method considering the non-linear parasitic output capacitance is presented in this section.

Seen from Fig. 1(b), the following differential equations can be used to describe the transient voltages of Q_4 and Q_2.

$$\begin{cases} C_{oss,Q2}(v_{DS,Q2})\dfrac{dv_{Coss,Q2}(t)}{dt} = i_{Coss,Q2}(t) \\ C_{oss,Q4}(v_{DS,Q4})\dfrac{dv_{Coss,Q4}(t)}{dt} = i_{Coss,Q4}(t) \end{cases} \tag{4}$$

The items $C_{oss,Qi}(v_{DS,Qi})|_{i=2,4}$ indicates the non-linear output capacitance, and $v_{coss,Qi}$, $i_{Coss,Qi}$ are the voltage and charging/discharging current of $C_{oss,Qi}$. According to Kirchhoff laws, there are

$$\begin{cases} i_p(t) = i_{Coss,Q4}(t) - i_{Coss,Q2}(t) \\ v_{Coss,Q4}(t) = V_1 - v_{Coss,Q4}(t) \end{cases} \tag{5}$$

where V_1 is the off-stage voltage of the power device (equals to the input DC voltage) and $i_p(t)$ is the leakage inductance current, as depicted in Fig. 1(a). Solving (4) and (5) together will lead to

$$i_p(t) = \left[C_{oss,Q2}(v_{DS,Q2}) + C_{oss,Q4}(v_{DS,Q4})\right]\frac{dv_{Coss,Q4}(t)}{dt} \tag{6}$$

Seen from (6), the voltage gradients of $v_{Coss,Q4}$ ($v_{Coss,Q4}$ = $v_{DS,Q4}$) are determined by the current $i_p(t)$ and the summation of the non-linear parasitic capacitance of Q_2 and Q_4. Fig. 4 gives an example of the measured transient drain-source voltages of Q_4 at V_1 = 200 V with a dead time T_{dead} = 400 ns.

In order to simplify the analysis, an equivalent capacitance $C_{eq,Q4}$ is introduced as

$$C_{eq,Q4} = C_{oss,Q4}(v_{DS,Q4}) + C_{oss,Q2}(v_{DS,Q2}) \tag{7}$$

Note that $C_{eq,Q4}$ is also non-linear and changes with the voltage $v_{DS,Q4}$. The used power devices for Q_2 and Q_4 are the same MOSFET IPW65R080CFD, thus the non-linear $C_{oss}(v_{DS})$ curve as shown in Fig. 3 is applicable to both Q_2

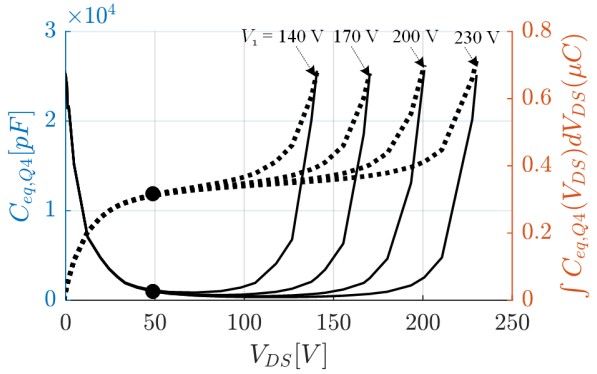


Fig. 5. Profiles of the equivalent capacitance $C_{eq,Q4}$ and charge with different off-state voltages (V_1).

and Q_4. Considering the fact that $v_{DS,Q2} + v_{DS,Q4}$ is always equal to V_1, (7) can be transferred into

$$C_{eq,Q4} = C_{oss,Q4}(v_{DS,Q4}) + C_{oss,Q4}(V_1 - v_{DS,Q4}) \tag{8}$$

Based on (8), the profiles of $C_{eq,Q4}$ can be described by the solid curves in Fig. 5, which have a "Bathtub-shape". During the turn-on procedure of Q_4, the voltage $v_{DS,Q4}$ decreases softly from the off-stage voltage V_1 to zero. In the meantime, the equivalent output capacitance $C_{eq,Q4}$ firstly decreases sharply and then keeps constant roughly for a while before increasing to the highest value, which aligns well with the changing gradients of the voltage $v_{DS,Q4}$ as shown in Fig. 4.

Moreover, it can be observed from Fig. 5 that the changing trends of $C_{eq,Q4}$ within the range of $V_{DS} \in$ [0 V, 50 V] are the same among different off-state voltages. For addressing this, the integrals of $C_{eq,Q4}$ along the V_{DS} axis are depicted by the dotted curves in Fig. 5. It can be seen that these dotted curves are overlapping in the range of $V_{DS} \in$ [0 V, 50 V]. Therefore, the average value of $C_{eq,Q4}$ within $V_{DS} \in$ [0 V, 50 V] can be used to estimate the drain-source voltage trajectory of Q_4 as $v_{DS,Q4}$ changes from 50 V to 0 V, regardless of the off-stage voltages. For the used MOSFET IPW65R080CFD, the average value is

$$C_{eq,Q4,avg} = \frac{1}{50}\int_0^{50} C_{eq,Q4}(V_{DS})dV_{DS} = 5757 \text{ pF} \tag{9}$$

In order to judge the practical ZVS conditions of Q_4, three experimental cases of ZVS, quasi-ZVS and non-ZVS are shown in Fig. 6. In the three cases, the index "ZVS" indicates ZVS success, "quasi-ZVS" means quasi ZVS success and "non-ZVS" denotes ZVS failure. α_p, α_s, φ equal to $D_p \cdot 180°$, $D_s \cdot 180°$, $D_\varphi \cdot 180°$, respectively, corresponding to the marked control variables in Fig. 2. Actually, the operating points in these three cases are the boundaries of the safe ZVS region, marginal ZVS region and non-VS dangerous region, which will be discussed subsequently.

In the "ZVS" case (blue), as shown in Fig. 6(a), when Q_4 begins to turn on ($v_{\text{GS,ZVS}}$ turns to zero), the drain-source voltage $v_{\text{DS,ZVS}}$ has decreased from the 200 V to 10 V. Then it continuously decreases to zero until $v_{\text{GS,ZVS}}$ rises to the threshold voltage ($v_{\text{GS(th)}}$ = 3.5 V for the used MOSFET IPW65R080CFD). Therefore, the "ZVS" case can achieve the full ZVS operation.

On the other hand, in the "quasi-ZVS" case with larger φ, the drain-source voltage $v_{\text{DS,quasi-ZVS}}$ is as high as 70 V when the driving signal $v_{\text{GS,quasi-ZVS}}$ becomes positive. But then it rapidly decreases to around 15 V by the time $v_{\text{DS,quasi-ZVS}}$ reaching the threshold voltage. Thus this case is termed as quasi-ZVS operation.

By keeping the same α_p and α_s, the value of φ is adjusted to higher 10° in the "non-ZVS" case. As seen from Fig. 6(b) and Fig. 6(d), the gate-source voltage and the leakage inductance current start to oscillate due to the ZVS failure. This voltage and current oscillations might damage the power devices and the gate driver, and hence the related operating points are named as dangerous region.

Comparing the transient waveforms of $v_{DS}(t)$ in Fig. 6(a), it can be found that $v_{DS,Q4}$ has a sharp plunge from the off-state voltage to zero in the ZVS failure case. In contrast, $v_{DS,Q4}(t)$ softly decreases to zero in the other two cases. Based on (6) and (7), the voltage shape of $v_{DS,Q4}$ (equals to $v_{Coss,Q4}$) is affected by the non-linear $C_{eq,Q4}$ and the leakage inductance current $i_p(t)$. But due to the variations of $C_{eq,Q4}$ and $i_p(t)$, it is difficult to directly solve the transient voltage $v_{DS,Q4}$. Thus (6) is transformed into the following integral form

$$\int_0^{v_{DS,ins}} C_{eq,Q4}(v_{DS,Q4}) dv_{DS,Q4} = \int_0^{t_{ins}} i_p(t) dt \quad (10)$$

where $v_{DS,ins}$ is the instantaneous drain-source voltage at any time instant $t = t_{ins}$ during the transient procedure. It can be seen that both sides of (10) mean the concept of charge Q. In order to fully charge/discharge the parasitic output capacitance $C_{oss,Q2}$ and $C_{oss,Q4}$, the right side of (10) should be larger than the left side. Otherwise, one of the two situations of quazi-ZVS or non-ZVS would happen, depending on the remaining time from $v_{DS,Q4}$ = 50 V to $v_{DS,Q4}$ = 0 V, which will be explained later.

Using the extracted waveform data of $v_{DS,Q4}(t)$ and $i_p(t)$, the integrals of the leakage inductance currents in eight experimental cases are shown in Fig. 7. To align with the integrals in (10) where the initial $v_{DS,Q4}$ is zero, the time sequence is reversed from the end to start of the dead time interval. Besides, the signs of the $i_p(t)$ integrals are also reversed to positive so as to compare with the integrals of

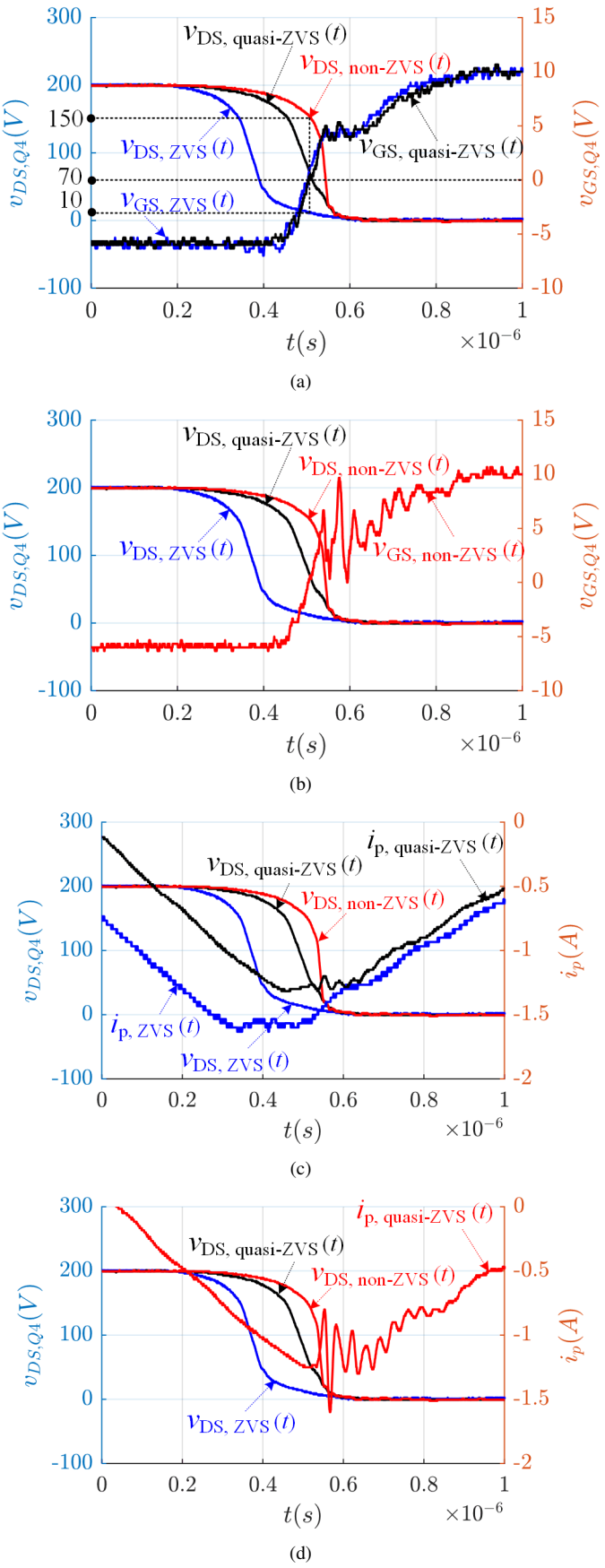


Fig. 6. Three experimental cases of the ZVS operation, quasi ZVS operation and ZVS failure of Q_4. blue: ZVS success (safe region), $\alpha_p = 60°$, $\alpha_s = 110°$, $\varphi = 6°$. black: quasi ZVS (marginal region), $\alpha_p = 60°$, $\alpha_s = 110°$, $\varphi = 9°$. red: ZVS failure (dangerous region), $\alpha_p = 60°$, $\alpha_s = 110°$, $\varphi = 10°$.

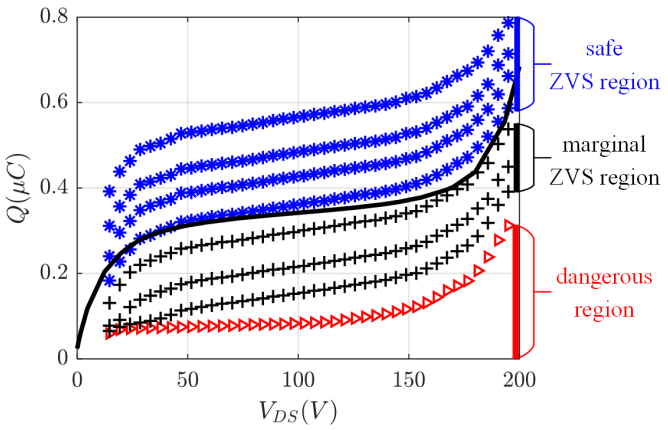


Fig. 7. The calculated integrals of $i_p(t)$ in eight experimental cases. blue "*": Case 1 to Case 4 from top to bottom (safe ZVS region). black "+": Case 5 to Case 7 from top to bottom (marginal ZVS region). red "▷": Case 8 (dangerous region). $\alpha_p = 60°$, $\alpha_s = 110°$ are applied to the eight cases, and $\varphi = 3°, 4°...10°$ in Case 1, 2..8, respectively. Therein, Case 4, Case 7 and Case 8 correspond to the "ZVS" case, the "quasi-ZVS" and the "non-ZVS" case in Fig. 6. Besides, the integral of $C_{eq,Q4}$ over various v_{DS} is depicted by the solid curve.

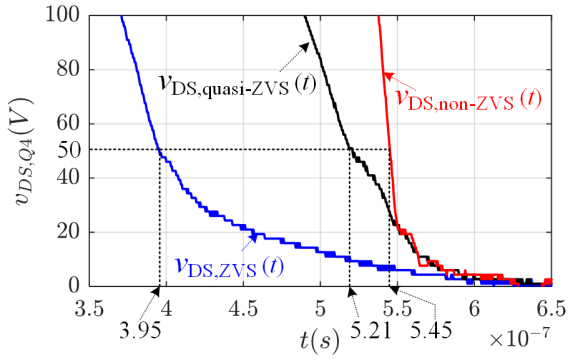


Fig. 8. Zoomed waveforms of $v_{DS,Q4}$ of the three cases in Fig. 6.

$C_{eq,Q4}$ in Fig. 7. According to the previous discussion, the Q-V_{DS} plane is divided into three regions: safe ZVS region (where ZVS is totally achieved), marginal ZVS region (where ZVS is quasi achieved without damaging the power devices or gate drivers) and dangerous region (where ZVS totally fails). As the phase shift φ increases from 3° to 10° in the eight cases, the operating points location gradually changes from the safe region to the dangerous region.

In order to judge the boundary conditions among the three regions, the waveforms of $v_{DS,Q4}$ are zoomed in Fig. 8. At the time instants $t = 0.395\ \mu s$ and $t = 0.521\ \mu s$, the drain-source voltages of the "ZVS" and "quasi-ZVS" cases (blue and black) are both equal to 50 V, so that there is enough time left for Q_4 to release the stored energy in the output capacitance. Whereas in the "non-ZVS" case (red), the $v_{DS,Q4}$ keeps a much higher voltage than 50 V until $t = 0.545\ \mu s$, resulting in little time left to totally discharge the output capacitance before the end of the dead time and thus leading to ZVS failure. Apart from the non-linear parasitic output capacitance, the transient drain-source voltage is also slightly influenced by the leakage inductance current. As it can be seen in Fig. 6(c), the current $i_p(t)$ is almost constant during $v_{DS,Q4} \in$ [0 V, 50 V], and it equals to $-I_3$, which is marked in Fig. 2. Similar as before, by setting $t = 0.611\ \mu s$ (when all $v_{DS,Q4}$ decrease to zero) in Fig. 8 as the origin $t = 0$, the original $t = 0.395\ \mu s$ is transformed into $\Delta t = 0.216\ \mu s$. The ZVS boundary conditions of the safe ZVS region and the marginal ZVS region can be derived by satisfying

$$\int_0^{\Delta t} I_{3,min} dt \geq \int_0^{50} C_{eq,Q4,avg} dv_{DS,Q4} \tag{11}$$

Equation (11) implies that in order to achieve total ZVS for Q_4, the parasitic output capacitance $C_{oss,Q2}$ and $C_{oss,Q4}$ should not only totally charge/discharge, but also be completed within a limited time interval.

Due to the fact that the operating points in marginal ZVS region do not need to fulfill (11), the minimum I_3 can only be obtained from the boundary "quasi-ZVS" case (i.e. the "quasi-ZVS" case in Fig. 6 or Case 7 in Fig. 7). Similarly, to simplify the calculations, the original $t = 0.611\ \mu s$ in Fig. 8 is set as the origin $t = 0$, then the original $t = 0.521\ \mu s$ is transformed into $\Delta t_m = 0.09\ \mu s$. As a result, the following equation should be met.

$$\int_0^{\Delta t_m} I_{3,min} dt \geq -\int_0^{\Delta t_m} i_p(t) dt \tag{12}$$

Using the calculated $I_{3,min}$ by (11) or (12), the ZVS limitations on the control variables can be derived by

$$\begin{aligned} I_3 = \frac{nV_2}{4Lf_{sw}}\left[(k-1)D_p - 2D_\varphi\right] \geq I_{3,min} \\ \longrightarrow D_p > \frac{2}{k-1}D_\varphi + \frac{4Lf_{sw}}{nV_2(k-1)}I_{3,min} \end{aligned} \tag{13}$$

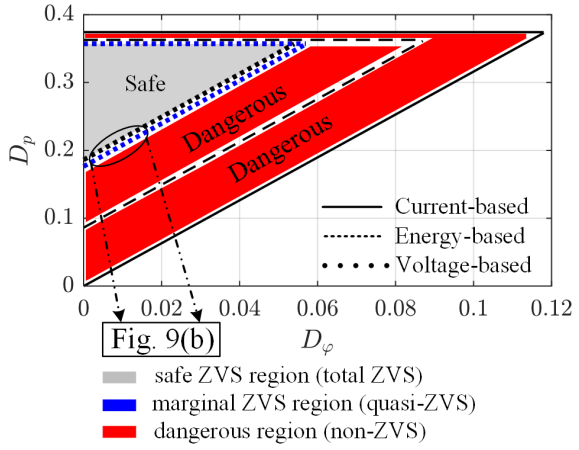
The same procedure can be applied to the other switching instants (e.g. t_1, t_2, t_4) in a half switching period and the calculated ZVS limitations are summarized in the last column of Table I. $I_{1,min}$, $I_{2,min}$ and $I_{4,min}$ are the minimum leakage inductance currents needed to achieve total ZVS or marginal ZVS of Q_8, Q_5, Q_3, respectively. Due to the mirror symmetry of the working waveforms in one switching period, the two power devices in one leg share the same ZVS conditions. Hence the ZVS conditions for Q_8, Q_5, Q_4, Q_3 are also applicable to Q_6, Q_7, Q_2, Q_1, respectively.

Besides, similar to (2) and (3), the derived voltage-based and energy-based ZVS limitations at different switching instants are also listed in Table I. For a clear comparison, an example of the ZVS range is calculated by the three methods and it is shown in Fig. 9.

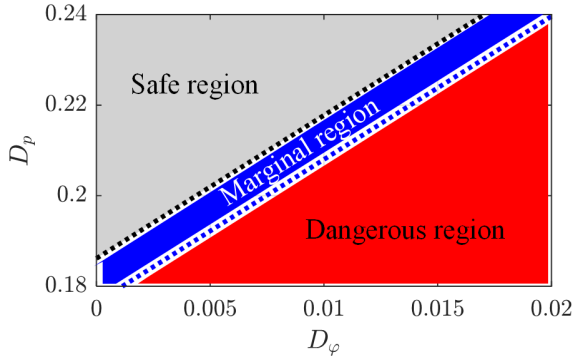
Seen from the top inset in Fig. 9, owing to the ignorance of the transient turn-on procedure in current-based method, a large portion of the induced ZVS range (wrapped by solid lines) is the dangerous region. The same issue exists in the energy-based ZVS region (wrapped by dashed lines) due to the disregard of the non-linearity of the parasitic output capacitance. In the voltage-based method, the three regions discussed above are depicted in Fig. 9 and partly amplified for a clear view in the bottom inset. These three regions are identified by the safe ZVS conditions (11) and the quasi-ZVS conditions (12). Detailed information can be found in the caption note of Fig. 9

TABLE I
THREE TYPES OF ZVS LIMITATIONS ON THE CONTROL VARIABLES FOR DAB CONVERTERS

t (ref. Fig. 2)	Current-based	Energy-based	Voltage-based (proposed)
t_1, Q_8	$D_s > kD_p$	$D_s > kD_p + \frac{4}{n} f_{sw}\sqrt{2LC_{oss,s}}$	$D_s > kD_p + \frac{4Lf_{sw}}{nV_2} I_{1,min}$
t_2, Q_5	$D_s > kD_p$	$D_s > kD_p + \frac{4}{n} f_{sw}\sqrt{2LC_{oss,s}}$	$D_s > kD_p + \frac{4Lf_{sw}}{nV_2} I_{2,min}$
t_3, Q_4	$D_p > \frac{2}{k-1} D_\varphi$	$D_p > \frac{2}{k-1} D_\varphi + \frac{4kf_{sw}}{k-1}\sqrt{2LC_{oss,p}}$	$D_p > \frac{2}{k-1} D_\varphi + \frac{4Lf_{sw}}{nV_2(k-1)} I_{3,min}$
t_4, Q_3	$D_p > -\frac{2}{k-1} D_\varphi$	$D_p > -\frac{2}{k-1} D_\varphi + \frac{4kf_{sw}}{k-1}\sqrt{2LC_{oss,p}}$	$D_p > -\frac{2}{k-1} D_\varphi + \frac{4Lf_{sw}}{nV_2(k-1)} I_{4,min}$



(a)



(b)

Fig. 9. (a) ZVS range comparison among the current-based, energy-based and voltage-based methods. (b) Zoomed view of Fig. 9(a). In the voltage-based method, the three regions discussed before are depicted, i.e. safe ZVS region (total ZVS achieves), marginal ZVS region (quasi-ZVS achieves), and dangerous region (ZVS fails). Following parameters are used: $D_s = 0.61$, $k = 1.63$ are applied in current-based method. $L = 45\ \mu H$, $n = 3.5$, $f_{sw} = 60\ kHz$, $C_{oss,p} = 215\ pF$, $C_{oss,s} = 401 \times 2\ pF$ are used in energy-based method. $V_2 = 35\ V$, $I_{1,min} = I_{2,min} = 1.5\ A$ are adopted in voltage-based method. Notably, in the energy-based method, $C_{oss,p}$ is the typical output capacitance of IPW65R080CFD, and $C_{oss,s}$ is double times the typical value of IPP110N20N3G because two MOSFETs are paralleled for each switch in HB_2. In the voltage-based method, $I_{3,min} = 1.34\ A$ (obtained from (11)) is used to specify the safe region boundary and $I_{3,min} = 0.32\ A$ (obtained from (12)) the marginal ZVS region boundary.

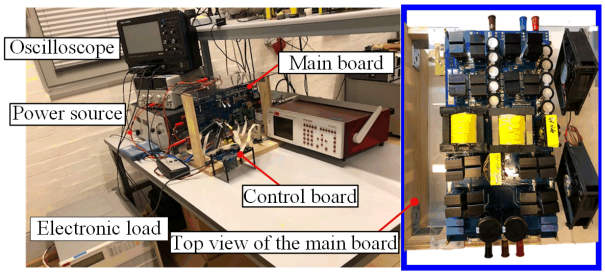


Fig. 10. Test platform for the DAB converter.

TABLE II
SYSTEM SPECIFICATIONS FOR DAB CONVERTER

Parameters	Description	Value
P	Rated power	1.5 kW
V_1	Input DC voltage	230 V
V_2	Output DC voltage	25 V
$n:1$	Turns ratio of the transformer	3.5 : 1
f_{sw}	Switching frequency	60 kHz
T_{dead}	Dead time	400 ns
L_s	Series inductor	36.2 μH
L_{trp}	Primary-side leakage inductance	4.5 μH
L_{trs}	Secondary-side leakage inductance	372.5 nH
C_1	Primary DC capacitor	0.78 mF
C_2	Secondary DC capacitor	1.5 mF

IV. EXPERIMENTAL VALIDATION

A test platform shown in Fig. 10 is built and the converter parameters are listed in Table II. The used transistor type is IPW65R080CFD in HB_1 and two IPP110N20N3 are in parallel for each switch in HB_2. In order to validate the universality of the proposed method, the DAB setup is operated with another group of input (V_1) and output (V_2) DC voltages, as listed in Table II.

Using the new group of V_1 and V_2 (different from $V_1 = 200\ V$, $V_2 = 35\ V$ in Fig. 9), the enhanced ZVS range can be calculated by the proposed voltage-based method, and a similar D_p-D_φ plane including different ZVS regions and dangerous region is as shown in Fig. 11. Due to the changed voltage ratio $k = V_1/(nV_2) = 2.63$ and the secondary duty ratio $D_s = 0.833$, the ZVS ranges in Fig. 11 are different from Fig. 9 (where $k = 1.63$, $D_s = 0.61$) with a wider range of D_φ and a narrower range of D_p. In order to verify the effectiveness of the obtained ZVS regions in Fig. 11,

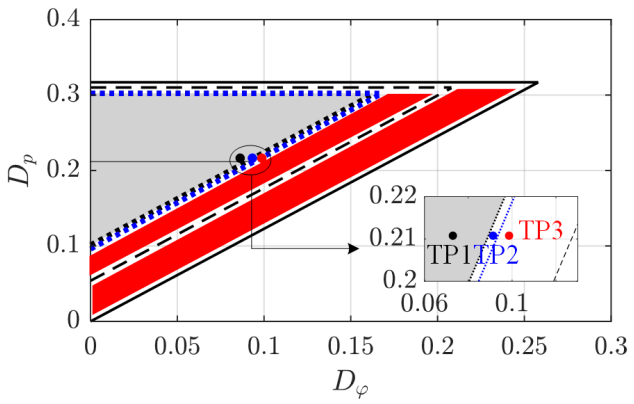


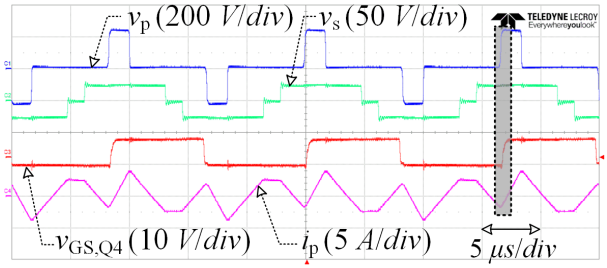
Fig. 11. ZVS limitations derived from the proposed method by setting different input and output DC voltages (V_1 = 230 V, V_2 = 25 V) and selecting three test points for the experimental validation. The meanings of the curve types and shaded areas are the same as Fig. 9. Test point 1 (TP1): safe ZVS region, D_p = 0.212, D_s = 0.833, D_φ = 0.067. Test point 2 (TP2): marginal ZVS region, D_p = 0.212, D_s = 0.833, D_φ = 0.094.. Test point 3 (TP3): dangerous region, D_p = 0.212, D_s = 0.833, D_φ = 0.1.

three test points from the safe ZVS region, the marginal ZVS region and the dangerous region are applied to the DAB prototype, as indicted by "TP1", "TP2" and "TP3" in the amplified inset. The matching operating waveforms are shown in Fig. 12(a), Fig. 13(a) and Fig. 14(a), respectively. v_p and v_s are the primary and secondary terminal voltages of the two H-bridges HB_1 and HB_2, respectively. i_p is the leakage inductance current, which is also the output terminal current of the primary HB_1 and thus denoted with the item "p".

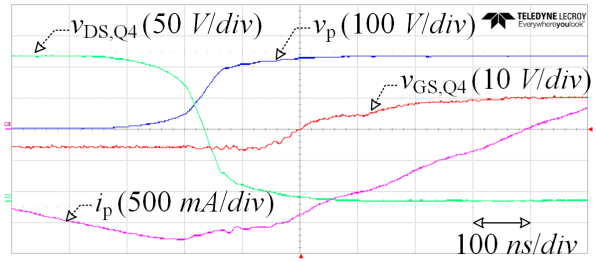
In order for a clear view of the transient turn-on procedure, the shaded gray areas in Fig. 12(a) to Fig. 14(a) are zoomed in Fig. 12(b) to Fig. 14(b), respectively. As the converter operates from TP1 (total ZVS) to TP3 (ZVS failure), the gradients of the drain-source voltage $v_{DS,Q4}$ gradually changes more and more sharply, and eventually results in a large $v_{DS,Q4}$ when the gate-source voltage $v_{GS,Q4}$ reaches the threshold voltage (= 3.5 V) in Fig. 14(b). This would lead to voltage spikes of v_p (as highlighted by the black ellipse in Fig. 14(a)), while the waveforms of v_p in Fig. 12(a) and Fig. 13(a) are clear and soft at the same switching instant. In the meantime, the leakage inductance current and the gate-source voltage oscillations are also induced by the ZVS failure as shown in Fig. 14(b).

V. Conclusions

By taking into account the non-linear parasitic output capacitance of the power semiconductor devices, a voltage-based ZVS condition is proposed in this paper. Compared to the commonly used current- and energy-based methods, the voltage-based method is developed according to the practical transient switching procedure and thus it has a higher accuracy. Depending on the C_{oss} profile, which changes a lot with the drain-source voltage, the minimum leakage inductance currents can be obtained to achieve ZVS. Based on the practical results, the converter operating points are divided into three regions, i.e. safe ZVS region (total ZVS), marginal ZVS region (quasi-ZVS) and dangerous region (ZVS failure). Besides, a comparative analysis of the three methods is implemented by

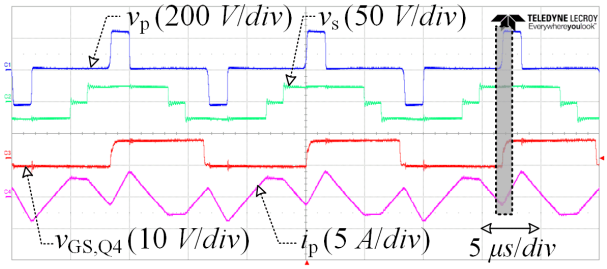


(a)

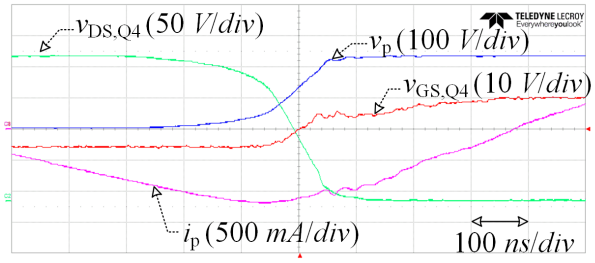


(b)

Fig. 12. Test point 1 (TP1, cf. black point in Fig. 11): steady state working waveforms within the safe ZVS region.



(a)



(b)

Fig. 13. Test point 2 (TP2, cf. blue point in Fig. 11): steady state working waveforms within the marginal ZVS region.

taking a triple-phase-shift operation mode as an example, and the same procedure can also be applied to other operation modes. In order for an effective validation, experimental results with different system specifications are conducted and the results can prove the effectiveness of the proposed voltage-based method by deriving a more accurate ZVS condition.

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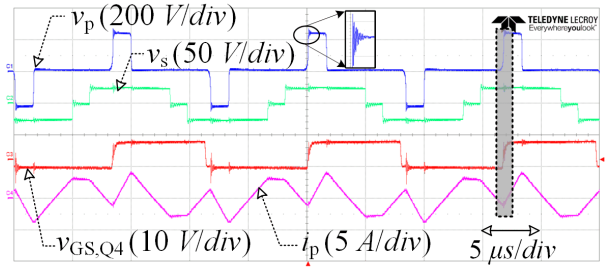
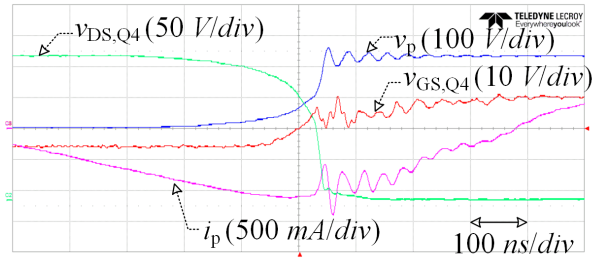


(a)



(b)

Fig. 14. Test point 3 (TP3, cf. red point in Fig. 11): Steady state working waveforms in the dangerous region.

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