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Accuracy Analysis of the Zero-Order Hold Model for Digital Pulsewidth Modulation

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***Abstract*—This paper analyzes the accuracy of the zero-order hold (ZOH) model for the digital pulsewidth modulator (DPWM) in the *s*-domain. The *s*-domain model and the exact *z*-domain model for the control loop of the single-phase inverter with L-type filter is elaborated for quantifying the deviation of the ZOH model for DPWM. The influence of the different computational delay and duty-cycle update modes on this deviation is analyzed in detail. The compensation method for this deviation of the ZOH model is proposed for accurately predicting the stability region of the control system in the *s*-domain. The simulations and experimental tests are executed to verify the effectiveness and correctness of the theoretical analysis.**

***Index Terms*—Compensation method, model accuracy, digital pulsewidth modulator, ZOH, stability analysis.**

I. INTRODUCTION

The stability analysis of pulsewidth modulated converters has attracted significant attentions recently [1]. The current control loop is the innermost, and fastest, loop of the cascaded control loops, which are typically used in a converter control system. The proportional gain of the current controller determines the bandwidth of the current control loop [2], i.e., a large gain gives a high bandwidth and consequently a fast transient response of the current. This is important, e.g., for fault ride through [3], [4]. Yet, the proportional gain cannot be made so high that the stability of the current control loop is jeopardized. The upper limit of the proportional gain is dependent on how the pulswidth modulator (PWM) is implemented and the resulting total computational delay of the current controller [5].

Digital PWM (DPWM) is widely used in power converters to generate switching drive pulses with a constant frequency. The duty-cycle is updated once or twice per switching period at the peak and/or the valley of the triangular carrier, which are known as single- and double-update-modes [6]. Meanwhile, the current and voltage are also sampled at the peak and/or the valley of the triangular carrier to avoid sampling harmonics due to the switching event [7]. In the case of this sampling and duty-cycle update mode, the grid-connected converter with the digital controller can be exactly modeled in the *z*-domain [8], and the digital controller can be designed accordingly. However, the analysis of the control system in the *z*-domain requires a uniform sampling/duty-cycle update frequency [9], which means that the *z*-domain model is not suitable for analyzing the network of multiple grid-connected converters with different sampling/switching frequencies. Moreover, for the future power-electronic-based power systems [6], the discrete *z*-domain model of converters is not readily compatible with the continuous dynamic behavior of electric power networks. Therefore, the continuous *s*-domain model of converters and, particularly the accurate model of the sampling process and DPWM is critical for the stability analysis and control of the future converter-based power systems.

In the process of DPWM, there is a time delay between the instant of updating the reference signal and the instant when the switching event occurs. However, this time delay, as well as the PWM delay, are, in some cases, neglected for simplification, i.e., the DPWM is modeled as a unity gain [10], [11], which may lead to the inaccurate/conservative design of the controller. In order to accurately predict the stability region of the control system, various models of DPWM have been proposed based on different methods. The DPWM can be taken into account by modeling it as a duty-cycle-dependent transfer function by using the small-signal analysis [12]. However, this model can only be adopted for DC/DC converters in the steady-state operating point and is not readily applicable for grid-connected converters. Consequently, a simplified and universal model that considers the DPWM as a half-switching-period delay is reported [6], which can be further simplified by using a Padé approximation if found convenient [13], [14]. Yet, there exists a difference between this approximated model and the actual process of DPWM, especially for power converters with a low pulse ratio, i.e. the ratio of switching to fundametnal frequency. A zero-order hold (ZOH) model further improves the accuracy compared to the time-delay and Padé-approximation models [15]. Although a better accuracy is obtained, this paper shows that the ZOH model is still an approximation of the DPWM, and the compensation of the ZOH model deviation is necessary for accurately analyzing and designing the controller in the *s*-domain.

In the process of the sampling in the digital control system,

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the voltage and current signal need to be sampled ahead of the duty-cycle updating instant for avoiding any duty-cycle limitation [16]. This sampling process consequently introduces an extra delay, named as computational delay, which also affects the phase margin [17], especially for converters with a low sampling frequency [18]. Shifting the sampling instant toward the duty-cycle update instant gives a way to increase the bandwidth of the closed-loop system [19], [20]. Yet, such a shift of the sampling instant tends to introduce low-order current harmonics [9] and the fractional delay, which complicates the dynamic analysis of the control system. These effects are less adverse when the interval between the sampling instant and the duty-cycle-updating instant is much smaller than the switching period [21]. Consequently, this method is usually used in high-power converters with a low switching frequency [22]. As the reduction of the computational delay, the model accuracy of the DPWM plays a dominant role in the analysis of the stability region of the control system.

This paper evaluates first the accuracy of the ZOH model for the DPWM with the different computational delay and duty-cycle update modes, and then the compensation method for this equivalent model is proposed to accurately predict the stability region of the control system in the *s*-domain. The rest of this paper is organized as follows: Section II describes a single-phase voltage source converter (VSC) with an inductance (*L*)-filter. The ZOH model of the DPWM and the *z*-domain representation for the control loop discretized by the forward difference is explicitly identified. In Section III, the deviation of the equivalent ZOH model for DPWM is analyzed and a compensation method for the ZOH model is proposed and discussed, considering the different duty-cycle update modes and the computational delay. In Section IV, an experimental verification is carried out to confirm the effectiveness of the theoretical analysis. Section V concludes this paper.

II. Control System Models

A. System Description

Fig. 1 illustrates a single-phase *L*-filtered VSC, where u_{ab} and i are the converter output voltage and current, respectively, and u represents the grid voltage. L and R are the filter inductance and resistance, respectively. For simplicity, a proportional current controller is considered to examine the stability region of the current loop.

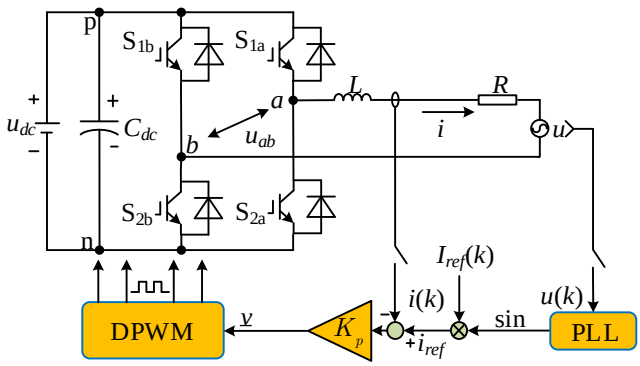

Fig. 1. Single-phase VSC with a proportional current controller.

The grid voltage u, the line current i in the static reference frame are defined as follows:

$$u = u_m \sin(\omega_0 t) \tag{1}$$

$$i = i_m \sin(\omega_0 t + \varphi_i). \tag{2}$$

Kirchhoff's voltage law (KVL) is used to analyze the voltage across the inductor L. The voltage equation is

$$L\frac{di}{dt} = u - u_{ab}. \tag{3}$$

Therefore, the block diagram of the control loop with the current regulator $R(s)$ can be drawn as Fig. 2.

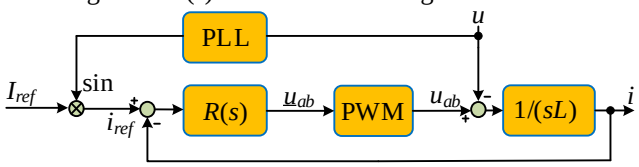

Fig. 2. Block diagram of the control loop with a proportional gain current controller.

In this paper, the proportional gain K_p is applied in the current regulator. Without considering the dynamics of the DPWM and computational delay effect, the open-loop transfer function of the current loop is given as

$$G_o(s) = \frac{K_p}{sL}. \tag{4}$$

The closed-loop transfer function can be expressed as

$$G_{c1}(s) = \frac{G_o(s)}{1 + G_o(s)} = \frac{K_p}{sL + K_p}. \tag{5}$$

It is clear that the control system remains stable provided that K_p is positive. However, K_p is practically limited by aforementioned DPWM dynamics and computational delay [23].

B. ZOH Model for DPWM

The DPWM with the different duty-cycle update modes and computational delay are illustrated in Fig. 3, where T_{cp} is the computational duration of the control algorithm, and the duty-cycle needs to be calculated before next duty-cycle update instant. Therefore, the sampling instant and duty-cycle computation should happen at least one computational duration in advance of the next duty-cycle update instant. Normally, the sampling instant occurs one sampling interval in advance of the duty-cycle update instant as shown in Fig. 3(a) and Fig. 3(b). Furthermore, the sampling instant can be shifted towards the next sampling instant to reduce the time delay. Due to the performance improvement of the microcontroller, the computational duration T_{cp} has been reduced dramatically, and the computational delay T_d between the sampling instant and the duty-cycle-updating instant can thus be set near to zero, as shown in Fig. 3(c) and Fig. 3(d). Meanwhile, to further reduce the time delay, the double-update-mode is usually applied in DPWM shown in Fig. 3(b) and Fig. 3(d).

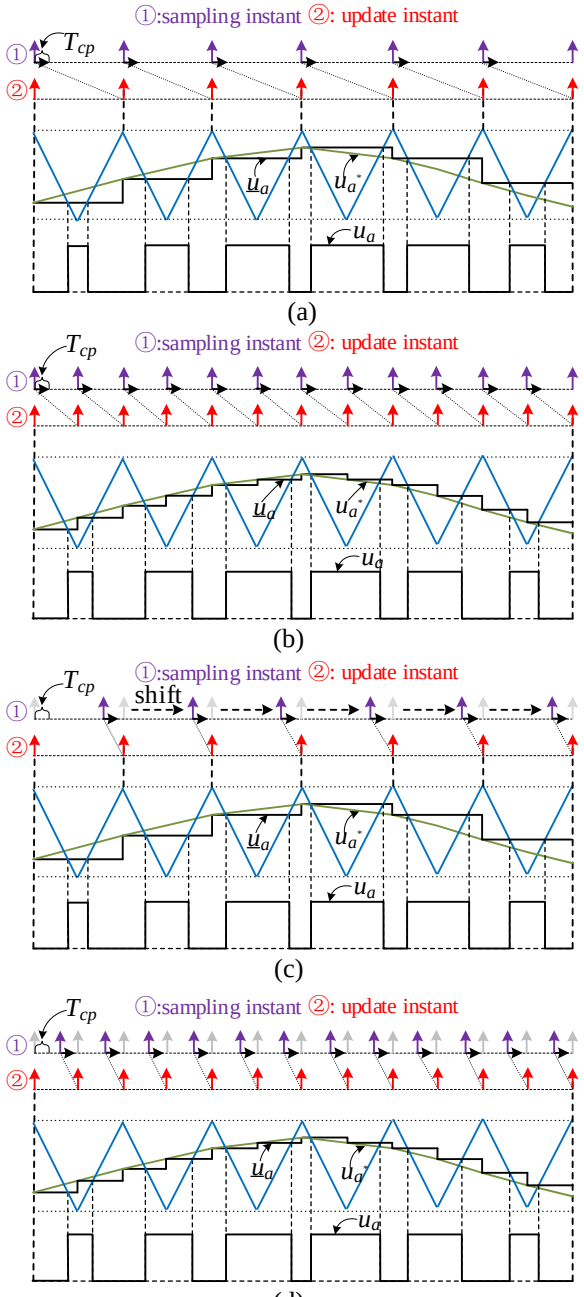

Fig. 3. DPWM with different update modes and computational delay. (a) the single update with one-step delay, (b) the double update with one-step delay, (c) the single update with a small computational delay, and (d) the double update with a small computational delay

In Fig. 3, u_a^* is the ideal output voltage for the phase a of the converter. $\underline{u}_a$ is formed from u_a^* by the ZOH. u_a^* and $\underline{u}_a$ can be expressed as

$$\begin{cases} u_a^* = -u_b^* = \dfrac{u_{ab}^*}{2} \\ \underline{u}_a^* = -\underline{u}_b^* = \dfrac{\underline{u}_{ab}^*}{2} \end{cases} \tag{6}$$

where u_{ab}^* is the ideal output voltage of the converter. $\underline{u}_{ab}$ formed from u_{ab}^* by the ZOH, which is calculated by the current regulator. u_b^* is the ideal output voltage for the phase b of the converter. $\underline{u}_b$ is formed from u_b^* by the ZOH.

In Fig. 3, $\underline{u}_a$ is compared to the triangular carrier to generate the actual output voltage u_a for the phase a of the converter, which guarantees area equivalence, that is

$$\underline{u}_a^*(k)T_h = \int_{kT_h}^{(k+1)T_h} u_a dt \tag{7}$$

where T_h is the duty-cycle update period, which is also the period of the ZOH.

The output voltage for the phase b also satisfies

$$\underline{u}_b^*(k)T_h = \int_{kT_h}^{(k+1)T_h} u_b dt \tag{8}$$

According to (3), (6)—(8), the sampled current satisfies

$$\begin{aligned} i(k+1) &= i(k) + \frac{1}{L}\int_{kT_h}^{(k+1)T_h} u_{ab} dt - \frac{1}{L}\int_{kT_h}^{(k+1)T_h} u dt \\ &= i(k) + \frac{1}{L}\int_{kT_h}^{(k+1)T_h} (u_a - u_b) dt - \frac{1}{L}\int_{kT_h}^{(k+1)T_h} u dt \\ &= i(k) + \frac{1}{L}\underline{u}_{ab}(k)T_h - \frac{1}{L}\int_{kT_h}^{(k+1)T_h} u dt. \end{aligned} \tag{9}$$

The current dynamics caused by the signal $\underline{u}_{ab}$ is different from the one caused by the actual output voltage u_{ab} within one switching interval. But at the duty-cycle update instant, the sampled current controlled by $\underline{u}_{ab}$ is equal to that controlled by u_{ab} according to (9). The ZOH hence can be applied to model the DPWM process. The transfer function of the ZOH is given as

$$G_{zoh}(s) = \frac{1 - e^{-T_h s}}{T_h s}. \tag{10}$$

The open-loop transfer function with the ZOH model for the DPWM and the computational delay can be expressed as

$$G_{os}(s) = R(s)G_{ds}(s)G_{zoh}(s)P_s(s) = K_p e^{-T_d s}\frac{1 - e^{-T_h s}}{T_h s}\frac{1}{sL} \tag{11}$$

where $G_d(s) = e^{-T_d s}$ represents the computational delay transfer function. $P_s(s)$ is the s-domain transfer function of the model for the single-phase inverter with L-filter. By using the model shown in (11), the control system can be easily analyzed in the s-domain.

C. Discrete Control System Model

According to (9), the discrete current at the duty-cycle update instant satisfies

$$\frac{i(k+1) - i(k)}{\underline{u}_{ab}(k)} = \frac{T_h}{L} - \frac{1}{L\underline{u}_{ab}(k)}\int_{kT_h}^{(k+1)T_h} u dt. \tag{12}$$

Based on (12), the z-domain open-loop transfer function with the one-step delay can be expressed as

$$G_{oz}'(z) = R(z)G_{dz}(z)P_z(z) = z^{-1}\frac{T_h K_p}{(z-1)L} \tag{13}$$

where $P_z(z)$ is the z-domain transfer function of the control system without the computational delay. A fractional order delay is introduced into the transfer function of the control system if the sampling instant is shifted towards the duty-cycle update instant shown in Fig. 3(c) and Fig. 3(d). The z-domain open-loop transfer function is in this case expressed as

$$G_{oz}(z) = R(z)G_{dz}(z)G_{inv}(z) = \left\{1 - \frac{T_d}{T_h} + \frac{T_d}{T_h}z^{-1}\right\}\frac{T_h K_p}{(z-1)L}. \tag{14}$$

It is clear that (14) is equal to (13) if $T_d = T_h$. if $T_d \ll T_h$, that is

$$\frac{T_d}{T_h} << 1 \tag{15}$$

which implies that computational delay can be neglected.

The *z*-domain model shown in (13) is directly derived from (9), which is an accurate discrete description of the converter with *L* filter modulated by DPWM [8]. Therefore, this *z*-domain model can accurately describe the dynamics of the control system.

III. Accuracy of the ZOH Model for DPWM

A. Deviation of the DPWM Model

The ZOH transfer function, see (10), can be expressed as an integrator subtracting a delayed integrator as

$$G_{zoh}(s) = \frac{1}{T_h}\{\frac{1}{s} - \frac{1}{s}e^{-T_h s}\}. \tag{16}$$

According to (16), the output of the ZOH with a sinusoidal input is a cosine and a cosine with delay, that is

$$\begin{aligned} Y_{zoh}(t) &= \mathcal{L}^{-1}\{G_{zoh}(s)\mathcal{L}[\sin(\omega t)]\} \\ &= \frac{1}{\omega T_h}[\cos(\omega t) - \cos(\omega t - \omega T_h)] \\ &= \frac{1}{T_h}\int_{t-T_h}^{t} \sin(\omega t)dt. \end{aligned} \tag{17}$$

It is clear from (17) that for any sinusoidal input, the output of the ZOH model is the average of the input signal within the time interval t-T_h to t. On the other hand, due to $\underline{u}_{ab}^*$ formed from u_{ab}^* by the ZOH as shown in Fig. 3, the average output of the DPWM is equal to $\underline{u}_{ab}^*$ expressed by (7), which is the average of the rectangular integral shown in Fig. 4. Therefore, there exists the deviation between the ZOH model for DPWM and actual modulating process, and this deviation is illustrated in Fig. 4. This deviation for a low-frequency modulating wave (high pulse-ratio) shown in Fig. 4(a) is smaller than that for a high-frequency modulating wave (low pulse-ratio), it means that this ZOH model for DPWM is not suitable for analyzing the control system in the high-frequency domain.

Therefore, the model of the control loop with the ZOH model will lead to an inaccurate stability criterion for the current controller. In contrast, the control system model given in (14) is directly discretized based on (9) and (12) using the forward difference, which accurately models the dynamic characteristic of the control system.

According to the *s*-domain transfer function shown in (11), the frequency response function of control loop with ZOH model below the Nyquist frequency is given as

$$\begin{aligned} G_{os}(j\omega) &= \frac{1-e^{-T_h j\omega}}{j\omega T_h}\frac{K_p}{j\omega L}e^{-j\omega T_d} \\ &= \frac{K_p}{\omega L}\left|\frac{\sin(\omega T_h/2)}{\omega T_h/2}\right| e^{j(-\frac{\pi}{2}-\frac{\omega T_h}{2}-j\omega T_d)}. \end{aligned} \tag{18}$$

Similarly, based on the *z*-domain transfer function shown in (14), the frequency response function of the discrete model is expressed as

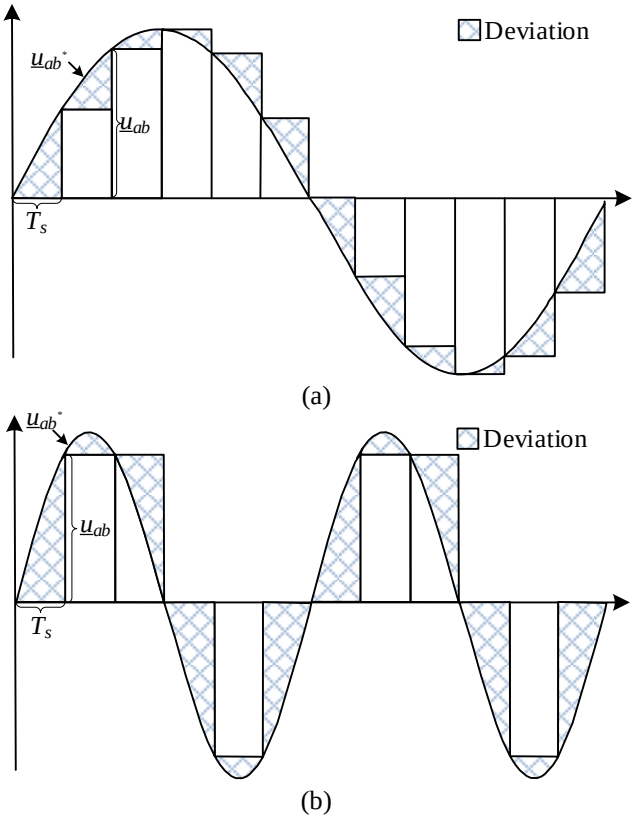

Fig. 4. Deviation of the ZOH model. (a) high carrier–fundamental frequency ratio, and (b) low carrier–fundamental frequency ratio.

$$\begin{aligned} G_{oz}(e^{jwT_h}) &= (1 - \frac{T_d}{T_h} + \frac{T_d}{T_h}e^{-j\omega T_h})\frac{T_h K_p}{(e^{j\omega T_h}-1)L} \\ &= \{(1-\frac{T_d}{T_h}) + \frac{T_d}{T_h}e^{-j\omega T_h}\}\frac{T_h}{2L}\frac{K_p}{\left|\sin(\omega T_h/2)\right|}e^{j(-\frac{\pi}{2}-\frac{\omega T_h}{2})}. \end{aligned} \tag{19}$$

The deviation of the *s*-domain transfer function with the ZOH equivalent model can be defined as

$$\begin{aligned} D(\omega) &= \frac{G_{oz}(e^{j\omega T_h})}{G_{os}(j\omega)} \\ &= \{\frac{\omega T_h/2}{\sin(\omega T_h/2)}\}^2\{(1-\frac{T_d}{T_h})e^{j\omega T_d} + \frac{T_d}{T_h}e^{j\omega(T_d-T_h)}\}. \end{aligned} \tag{20}$$

The same technology roadmap can be applied for analyzing the deviation of the *s*-domain transfer function with the ZOH equivalent model for different converter types and current controllers. The difference is the value of the deviation in (20).

B. Compensation for the DPWM Model

It can be seen from (20) that there is an obvious deviation of the frequency response between the accurate *z*-domain model in (19) and the *s*-domain transfer function with the ZOH model in (18), which needs to be compensated to obtain an accurate frequency response of the control loop in the *s*-domain. when $T_d \ll T_h$, the term of the last bracket in (20) can be simplified as

$$(1-\frac{T_d}{T_h})e^{j\omega T_d}+\frac{T_d}{T_h}e^{j\omega(T_d-T_h)} \approx 1+\frac{T_d}{T_h}[1-\cos(\omega T_h)]+j\frac{T_d}{T_h}[\omega T_h-\sin(\omega T_h)]\approx 1 \quad (21)$$

$D(j\omega)$ in (20) thereby can be simplified and the compensation coefficient is defined as

$$k_{comp}(\omega)=D(j\omega)\approx\{\frac{\omega T_h/2}{\sin(\omega T_h/2)}\}^2. \quad (22)$$

It is deduced from (21) and (22) that when $T_d \ll T_h$, there is no phase deviation between the *s*-domain model and *z*-domain model. But the gain deviation still exists. Therefore, the proportional gain K_p should be compensated by (22), and the compensated gain K_{pc} for the *s*-domain model can be expressed as

$$K_{pc}=K_p/k_{comp}. \quad (23)$$

According to frequency response function of the *s*-domain model shown in (18), the phase crossover frequency f_{cro} satisfies

$$-\pi/2-2\pi f_{cro}T_h/2-2\pi f_{cro}T_d=-\pi. \quad (24)$$

f_{cro} can be solved from (24) as

$$f_{cro}=\frac{1}{2(T_h+2T_d)}. \quad (25)$$

When $T_d = T_h$, f_{cro} satisfies

$$f_{cro}=\frac{1}{6T_h}=\begin{cases}\frac{1}{6}f_{sw} & \text{(single update)}\\ \frac{1}{3}f_{sw} & \text{(double update)}\end{cases} \quad (26)$$

where f_{sw} is the switching frequency. In the condition of the critical stability, according to (18), K_p should satisfy

$$\frac{1}{2\pi f_{cro}L}\left|\frac{K_p\sin(\pi/6)}{\pi/6}\right|=1. \quad (27)$$

The critical proportional gain K_{p_crit} can be solved from (27) as

$$K_{p\_crit}=\frac{\pi L}{3T_h}\frac{\pi/6}{\sin(\pi/6)}=\begin{cases}\frac{\pi^2}{9}Lf_{sw} & \text{(single update)}\\ \frac{2\pi^2}{9}Lf_{sw} & \text{(double update)}.\end{cases} \quad (28)$$

The compensation coefficient at the critical frequency is

$$k_{comp}(2\pi f_{cro})=\{\frac{\pi/6}{\sin(\pi/6)}\}^2=\frac{\pi^2}{9}. \quad (29)$$

which is constant even if the duty-cycle update mode is changed.

when $T_d \ll T_h$, and then T_d in (25) can be neglected and f_{cro} can be expressed as

$$f_{cro}=\frac{1}{2T_h}=\begin{cases}\frac{1}{2}f_{sw} & \text{(single update)}\\ f_{sw} & \text{(double update)}.\end{cases} \quad (30)$$

Similarly, in the critical stability condition, K_{p_crit} satisfies

$$K_{p\_crit}=\frac{\pi}{T_h}L\frac{\pi/2}{\sin(\pi/2)}=\begin{cases}\frac{\pi^2}{2}Lf_{sw} & \text{(single update)}\\ \pi^2Lf_{sw} & \text{(double update)}.\end{cases} \quad (31)$$

and the compensation coefficient at the phase crossover frequency is expressed as

$$k_{comp}(2\pi f_{cro})=\{\frac{\pi/2}{\sin(\pi/2)}\}^2=\frac{\pi^2}{4}. \quad (32)$$

It is deduced from (26) to (32) that there is an obvious difference in the case of between the one-step delay and the small computational delay. The gain deviation of the *s*-domain transfer function with the ZOH equivalent model dramatically increases with the decreasing of the computational delay but is not affected by the duty-cycle update mode.

IV. Simulation and Experimental Results

In order to verify the correctness of the theoretical analysis, the simulation and experimental test are performed and parameters for simulation and experiment are listed in Table I.

TABLE I
System Parameters

Parameters	Value
The grid voltage *u*/Vrms	220
The frequency of the grid voltage *f* /Hz	50
dc-link rated voltage	600
Sampling frequency f_{sw}/kHz	5
ac–side inductor *L*/mH	12

A. Simulation Results

Fig. 5 shows the line current in the case of the single-update-mode with one-step delay. The proportional gain K_p steps from 57 Ω to 63 Ω at the instant 20 ms. According to (28) and (26), in this case, the critical proportional gain K_{p_crit} calculated by using the ZOH model for DPWM is equal to 65.8 Ω and f_{cro} = 833 Hz. Yet, as shown in Fig. 5, the control system has become unstable when K_p rises to 63 Ω, which means that 65.8 Ω is not a correct critical proportional gain, and the compensated critical gain by using (23) is 60 Ω, which is located the range of 57 Ω to 63 Ω, verifying the correctness of the theoretical analysis.

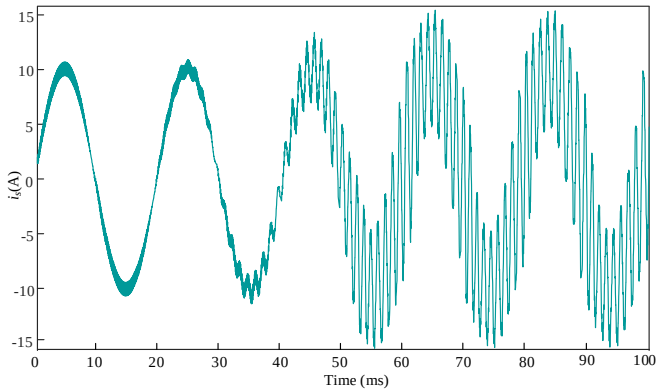

Fig. 5. The line current in the case of the single-update-mode with one-step delay.

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Fig. 6 shows the line current in the case of the double-update-mode with one-step delay. In this case, the critical proportional gain and phase crossover frequency calculated by using the *s*-domain model with the ZOH model for DPWM are equal to 131.59 Ω and 1666 Hz, respectively. As shown in Fig. 6, the control system becomes unstable when K_p is increased from 115 Ω to 125 Ω, which is lower than 131. 59 Ω but the compensated proportional critical gain is 120 Ω located in this range. And the compensation coefficient solved by (22) is still equal to $\pi^2/9$, which is not affected by different duty-cycle update modes.

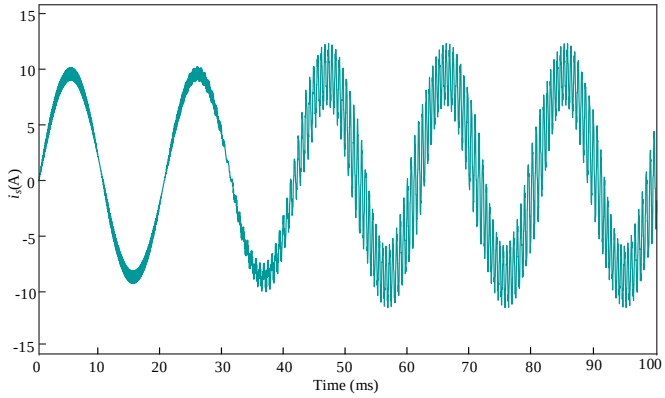

Fig. 6. The line current in the case of the double-update-mode with one-step delay.

Fig. 7 shows the line current in the case of the single-update-mode with a small computational delay (20 mirco-*s*). The critical proportional gain of the *s*-domain model with the ZOH model for DPWM and phase crossover frequency calculated by (30) and (31) are 296 Ω and 2500 Hz, respectively. However, the control system becomes unstable when the proportional gain is increased from 115 Ω to 125 Ω. This range just covers the compensated proportional gain 120 Ω, it can be known that the *s*-domain model with the ZOH model for DPWM has a large deviation when the small computational delay is small. This deviation can be effectively compensated by using the compensation coefficient.

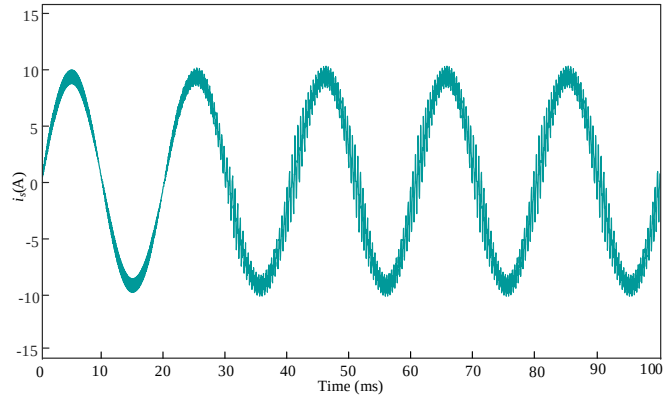

Fig. 7. The line current in the case of the single-update-mode with a small computational delay.

Fig. 8 shows the line current in the case of the double-update-mode with a small computational delay. The critical proportional gain by solving the *s*-domain model with the ZOH model is 592 Ω, and the phase crossover frequency is 5000 Hz. The control system becomes unstable when the proportional gain rises from 230 Ω to 250 Ω at the instant 20 ms. This instability of the line current is not obvious for the reason that the resonant frequency is the same as the switching frequency. The current ripple when the current is near to zero is increased dramatically, which implies that the control system has become unstable. The compensated proportional gain is 240 Ω, which is located in the range of 230 Ω to 250 Ω. The compensation coefficient still is $\pi^2/4$, which is coincident with the value solved by (32). Consequently, the proposed compensated method can effectively compensate the proportional gain solved by using the *s*-domain model with the ZOH model for DPWM.

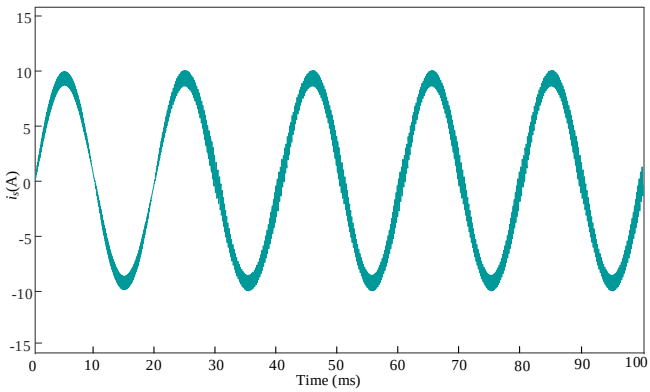

Fig. 8. The line current in the case of the double-update-mode with a small computational delay.

Moreover, in Fig. 9, the double-update-mode with a small computational delay is tested in the condition of L = 10 mH. In this case, the proportional gain can be solved as 493.5 Ω by using the *s*-domain model with the ZOH model for DPWM. The proportional gain of the controller steps from 195 Ω to 205 Ω at the instant 20 ms, and the control system becomes unstable at this instant. Therefore, the critical proportional gain is located in the range of 195 Ω to 205 Ω other than 493.48 Ω, and the compensated proportional gain calculated by (23) is equal to 200 Ω located in this range, which again proves the effectiveness of the compensated method.

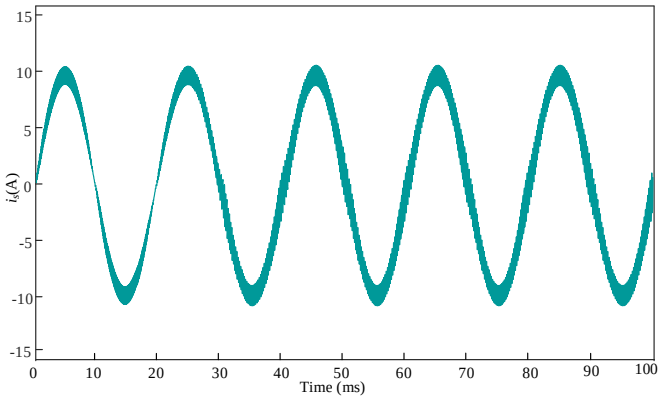

Fig. 9. The line current in the case of the double-update-mode with a small computational delay (L=10 mH).

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B. *Experimental Results*

The parameter of the experimental test is same with the that of the simulation. Fig. 10 shows the line current in the case of the single-update-mode with one-step delay. In this case, the proportional gain compensated by (23) is equal to 60 Ω. However, this critical value is varied from 57 Ω to 63 Ω in experiments, due to the inherent nonlinearities brought by the hysteresis of the filter inductor and the dead time of the converter. This slight variation correlates with the compensated value of 60 Ω. On the contrary, the stability region solved by (28) without the compensation is 65.797 Ω, out of the range.

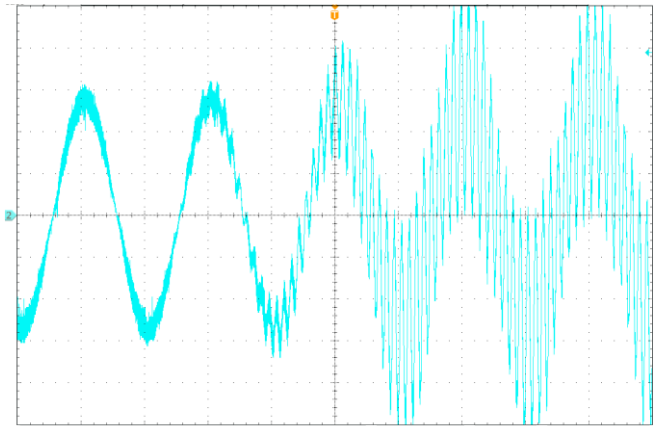

Fig. 10. The line current in the case of the single-update-mode with one-step delay (*i*:2A/div).

Fig. 11 shows the experimental results in the case of the double-update-mode with one-step delay. Similarly, the proportional gain and phase crossover frequency can be solved by (26) and (28), and the control system becomes unstable when the proportional gain is increased from 115 Ω to 125 Ω, which is lower than 131.59 Ω solved by (28). Yet, the compensated proportional gain is 120 Ω, which is correlated to the range of 115 Ω to 125 Ω. The experimental result is same to the simulation result and again verifies the correctness of the compensated method.

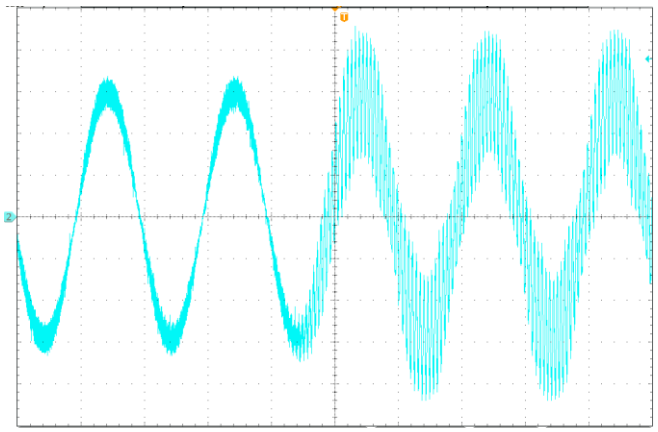

Fig. 11. The line current in the case of the double-update-mode with one-step delay (*i*:2A/div).

Similarly, the line current in the case of the single-update-mode with the small computational delay shown in Fig. 12, become unstable while the K_p is suddenly changed from 115 Ω to 125 Ω. The compensated K_{pc} = 120 Ω, which coincides with the experimental results. However, the proportional gain K_p solved by (31), which is not compensated by (23), is equal to 296 Ω, which is much far from the experimental results. Therefore, it is necessary to compensate the proportional gain in the case of the small computational delay.

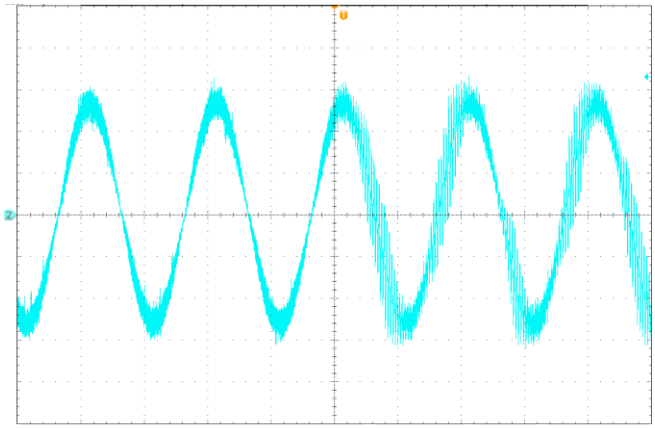

Fig. 12. The line current in the case of the single-update-mode with a small computational delay (*i*:2A/div).

Furthermore, the double-update-mode with a small computational delay is tested in Fig. 13, which shows that the control system becomes resonant with the increase of the proportional gain from 230 Ω to 250 Ω, which is much lower than 592 Ω solved by using the ZOH model for DPWM. The compensated value 240 Ω is located in the range of 230 Ω to 250 Ω, which coincides with the simulation result. Therefore, the experimental result verifies the correctness of the proposed method.

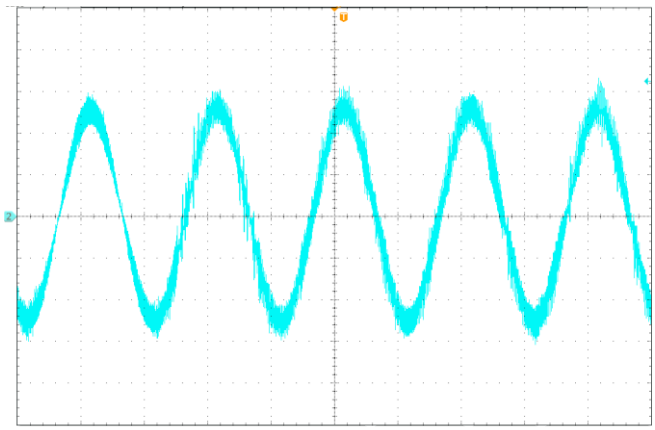

Fig. 13. The line current in the case of the double-update-mode with a small delay (*i*:2A/div).

V. CONCLUSION

This paper presents an accuracy analysis of the equivalent ZOH model for DPWM. A compensation method is derived to compensate the model deviation. The proposed analysis method and compensation method can be developed to different current controllers and converter types. From the theoretical analysis and the experimental verification, the following conclusions can be drawn:

1) The phase response of the ZOH model for DPWM is accurate.
2) The gain deviation of the ZOH model at the crossover frequency is small with the one-step delay but increases dramatically when the computational delay is reduced. Therefore, the model deviation should be compensated in the case of the small computational delay.
3) The gain deviation at the phase crossover frequency is not varied with the duty-cycle update modes, the compensation coefficient hereby is constant at the phase crossover frequency.

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