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Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2019.2937942

Publication date:
2020

Document Version
Publisher's PDF, also known as Version of record

Design-Oriented Transient Stability Analysis of PLL-Synchronized Voltage-Source Converters

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***Abstract*—Differing from synchronous generators, there are lack of physical laws governing the synchronization dynamics of voltage-source converters (VSCs). The widely used phase-locked loop (PLL) plays a critical role in maintaining the synchronism of current-controlled VSCs, whose dynamics are highly affected by the power exchange between VSCs and the grid. This article presents a design-oriented analysis on the transient stability of PLL-synchronized VSCs, i.e., the synchronization stability of VSCs under large disturbances, by employing the phase portrait approach. Insights into the stabilizing effects of the first- and second-order PLLs are provided with the quantitative analysis. It is revealed that simply increasing the damping ratio of the second-order PLL may fail to stabilize VSCs during severe grid faults, whereas the first-order PLL can always guarantee the transient stability of VSCs when equilibrium operation points exist. An adaptive PLL that switches between the second-order and the first-order PLL during the fault-occurring/-clearing transient is proposed for preserving both the transient stability and the phase-tracking accuracy. Time-domain simulations and experimental tests, considering both the grid fault and the fault recovery, are performed, and the obtained results validate the theoretical findings.**

***Index Terms*—Grid faults, phase-locked loop (PLL), transient stability, voltage-source converters (VSCs).**

I. Introduction

VOLTAGE-SOURCE CONVERTERS (VSCs) are commonly used with renewable energy resources, flexible power transmission systems, and electrified transportation systems. The ever-increasing penetration of VSCs is radically changing the dynamic operations of power grids. Differing from synchronous generators (SGs), the dynamic behavior of the VSC is highly affected by its control algorithms. The instability phenomena resulted from the control dynamics of VSCs under different grid conditions are increasingly reported, ranging from the harmonic stability to the loss of synchronization (LOS), which severely challenge the security of electricity supply in the power grid with high penetration of renewables [1].

Manuscript received April 22, 2019; revised July 11, 2019; accepted August 23, 2019. Date of publication August 28, 2019; date of current version January 10, 2020. This work was supported by Aalborg University Strategic Talent Management Programme. This article was presented in part at IEEE International Power Electronics Conference (IPEC-ECCE Asia), Niigata, Japan, May 2018, and IEEE Energy Conversion Congress and Exposition, Portland, OR, USA, Sep. 2018. Recommended for publication by Associate Editor M. GE Liserre. *(Corresponding author: Xiongfei Wang.)*

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Digital Object Identifier 10.1109/TPEL.2019.2937942

There have been increasing research efforts spent on tackling the stability challenges brought by VSC–grid interactions. The small-signal modeling and stability analysis of power-electronic-based power systems have been thoroughly discussed in the recent years [2]. It is found that the phase-locked loop (PLL) brings a negative damping within its bandwidth, which tends to destabilize the VSC under the weak (i.e., low short-circuit ratio) grid condition [3], [4], and the asymmetric *dq*-frame control dynamic of the synchronous reference frame (SRF)-PLL leads to frequency-coupled oscillations [5].

In contrast, only a few research works can be found on the transient stability (i.e., the synchronization stability) of VSCs under large grid disturbances. In a recent report from North American Electric Reliability Corporation (NERC), the LOS of the PLL under grid faults has been found as one cause of the trip of a 900-MW photovoltaic power plant in Southern California [6]. Hence, the analysis of the impact of the PLL on the transient stability of VSCs during large disturbances is urgently demanded. Although a wide variety of improved PLLs with adaptive parameter-tuning during transient disturbances have been developed [7]–[9], only the dynamic performance of the PLL itself is considered in those works. The VSC–grid interaction, i.e., the voltage at the point of common coupling (PCC) used for the grid synchronization will be affected by the VSC's injected current, due to the voltage drop across the grid impedance, was overlooked. This VSC–grid interaction is the key factor leading to the LOS of the PLL. As will be demonstrated in this article, the second-order adaptive PLLs proposed in [7]–[9] still have a risk of LOS under large grid disturbances.

Considering VSC–grid interactions, a large-signal nonlinear model of the SRF-PLL is reported in [10], which reveals that the LOS will be inevitable if the VSC does not have equilibrium points during grid faults. Moreover, when there are equilibrium points during grid faults, the transient stability of the VSC is also analyzed by using the equal-area criterion (EAC) presented in [11]. Although the EAC-based analysis is intuitive with a physical insight, the conclusion is only valid when the proportional gain (K_p) of the SRF-PLL is zero, which is not feasible in practice. A more accurate analysis characterizing the dynamics of the SRF-PLL during grid faults is provided in [12]–[15] by using the phase portrait approach.

A number of control methods have also been developed for avoiding the LOS of the PLL-synchronized VSCs. The simplest approach is to freeze the PLL during grid faults [16], which is also recommended in the NERC report [6]. Yet, an

obvious disadvantage of this method is that the VSC has no synchronization units during grid faults, and, thus, it fails to detect the right grid phase angle. Consequently, the injected active and reactive current is out of control during that period, which violates the grid code [17].

Besides freezing the PLL, the transient stability of VSCs can also be enhanced by directly modifying the injected active and reactive current to the grid, including the zero current injection [18], the adaptive current injection based on the *X*/*R* ratio of the grid impedance [19], and the adaptive current injection based on the detected frequency of the PLL [20], [21]. The zero current injection method cannot comply with the grid code, which requires the VSC to inject 1.p.u. reactive current during severe faults [17]. The adaptive current injection based on the *X*/*R* ratio requires the prior knowledge of the grid impedance, which is also impractical. In contrast, the adaptive current injection based on the output frequency of the PLL is more feasible, which, however, still may fail to inject 1 p.u. reactive current under the grid fault, when the grid impedance is not purely inductive [20]. To avoid modifying the injected current profile, the damping ratio of the SRF-PLL can be increased to enhance the transient stability of VSCs [12]–[15], [22]. Yet, those works have not quantified how large the damping ratio of the PLL is needed to stabilize VSCs, and, thus, the PLL design guideline is still missing.

This article presents a design-oriented analysis of the transient stability impact of the PLL on current-controlled VSCs. Since the LOS of VSCs is inevitable when there is no equilibrium point during large disturbances [10], only the transient stability of VSCs with equilibrium points is considered. As an extension of the analysis presented in [12] and [13], this article first quantifies the critical damping ratio of the PLL under different operating conditions, i.e., different depths of grid voltage sags and different voltage drops across the line impedance. It is revealed that when only one equilibrium point exists during the fault, the SRF-PLL cannot stabilize VSCs no matter how large the damping ratio is adopted. Yet, this transient instability can be avoided if the SRF-PLL is reduced as a first-order PLL by freezing the integral controller. On the other hand, since the first-order PLL suffers from the steady-state phase-tracking error when the grid frequency has a steady-state drift from its nominal value [23], an adaptive PLL, which switches between the SRF-PLL and the first-order PLL based on the grid condition, is then developed to avoid the LOS of current-controlled VSCs. Moreover, instead of freezing the whole PLL, the adaptive PLL operates as the second-order PLL when the postfault grid voltage comes to the steady state, which allows an accurate phase tracking during the grid fault and thus facilitates the fault recovery. Time-domain simulations and experimental tests validate the theoretical findings and the performance of the adaptive PLL.

II. Grid-Connected VSCs

A. System Description

Fig. 1 illustrates the simplified single-line diagram of a grid-connected three-phase VSC using the typical vector current control, where L_f is the output filter of the converter, $Z_{\rm line}$ represents the line impedance, $V_{\rm gcp}$ and $\theta_{\rm gcp}$ are the amplitude

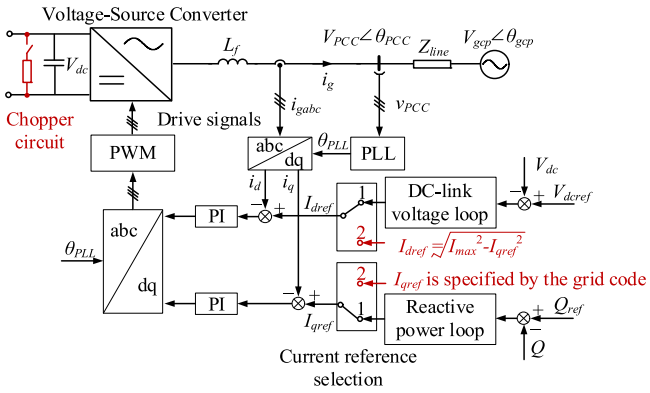

Fig. 1. Single-line diagram of a grid-connected VSC during the normal and fault ride-through operations. The current reference selection is switched to 1 during the normal operation and is switched to 2 during the fault ride through.

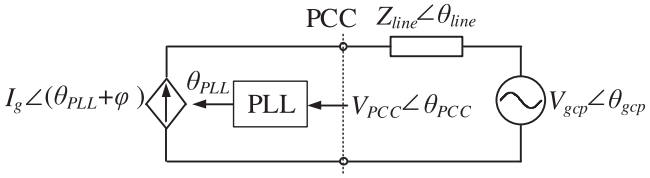

Fig. 2. Simplified converter-grid system for the transient stability analysis.

and the phase angle of the voltage at the grid connection point (GCP). The PCC voltage is measured for synchronizing the VSC with the grid by means of the PLL. $V_{\rm PCC}$ and $\theta_{\rm PCC}$ are the amplitude and the phase angle of the PCC voltage, respectively, and $\theta_{\rm PLL}$ is the phase angle detected by the PLL. $\theta_{\rm PLL}=\theta_{\rm PCC}$ is expected at the steady state. $I_{d\rm ref}$ and $I_{q\rm ref}$ are current references for the active current and the reactive current, respectively. The current reference selection is switched to 1 during the normal operation, where $I_{d\rm ref}$ and $I_{q\rm ref}$ are determined by the dc-link voltage loop and the reactive power loop, respectively. During the grid faults, the current reference selection is switched to 2, where $I_{q\rm ref}$ is directly specified based on the requirement of the grid code, and $I_{d\rm ref}$ is changed based on $I_{q\rm ref}$ in order to avoid the overcurrent of the VSC [22]. A proportional+ integral (PI) controller is used for the current regulation in the dq-frame to guarantee a zero steady-state tracking error [24]. The outputs of the PI controller are transformed to the *abc* frame and then fed into the pulsewidth modulation (PWM) block to generate drive signals of power switches.

Based on the principle of model order reduction, the fast dynamics of the system can be neglected when analyzing the impact of the slow dynamics [25]. The bandwidth of the PLL is designed much lower than that of the inner current loop [26]. Thus, the inner current loop can be approximated as a unity gain in the transient stability study. As the dc-link voltage loop and the reactive power loop are deactivated during the grid fault, the synchronization stability of the VSC during the grid fault is dominated by the dynamics of the PLL. Consequently, the system diagram shown in Fig. 1 can be simplified as a controlled current source with its phase angle regulated by the PLL, as shown in Fig. 2. φ denotes the phase difference between the PCC voltage $v_{\rm PCC}$ and the grid current i_g, which is also called

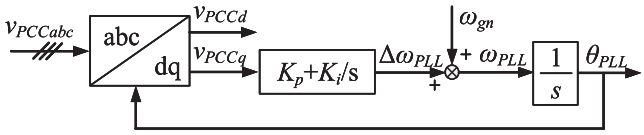

Fig. 3. Block diagram of the SRF-PLL.

the power factor angle. I_g is the amplitude of the grid current. θ_{line} represents the line impedance angle. It is worth mentioning that this simplified representation of grid-connected VSCs has been proven adequate in [10]–[16], [18]–[22] for analyzing the transient stability impact of the PLL.

B. Mathematical Model of the PLL Considering Line Impedance Effect

Fig. 3 illustrates the block diagram of the commonly used SRF-PLL [23]. The three-phase PCC voltages are sampled and transformed to the *dq* frame. The q-axis voltage is regulated by a PI controller for tracking the grid phase [23].

Based on Fig. 3, the dynamic equation of the PLL can be expressed as

$$\theta_{\text{PLL}} = \int \left[\omega_{\text{gn}} + \left(K_p + K_i \int\right) v_{\text{PCC}q}\right] \tag{1}$$

where ω_{gn} is the nominal grid frequency. K_p and K_i are the proportional and integral gain of the PI regulator, respectively. $v_{\text{PCC}q}$ represents the q-axis component of the PCC voltage.

Based on Fig. 2, $v_{\text{PCC}q}$ can be calculated as

$$v_{\text{PCC}q} = v_{zq} + v_{\text{gcp}q} \tag{2}$$

where v_{zq} and $v_{\text{gcp}q}$ denote the q-axis component of the voltage across the line impedance and the GCP voltage, respectively. The line impedance can be given by $Z_{\text{line}} = R_{\text{line}} + jX_{\text{line}}$, and v_{zq} and $v_{\text{gcp}q}$ can then be derived as

$$v_{zq} = I_d X_{\text{line}} + I_q R_{\text{line}} \tag{3}$$

$$v_{\text{gcp}q} = V_{\text{gcp}} \sin\left(\theta_{\text{gcp}} - \theta_{\text{PLL}}\right). \tag{4}$$

Defining the angle difference between θ_{PLL} and θ_{gcp} as δ, i.e.

$$\delta = \theta_{\text{PLL}} - \theta_{\text{gcp}}. \tag{5}$$

Substituting (2)–(5) into (1), and considering the integral relationship that $\theta_{\text{gcp}} = \int \omega_{\text{gn}} dt$, which yields

$$\delta = \int \left(K_p + K_i \int\right)\left(I_d X_{\text{line}} + I_q R_{\text{line}} - V_{\text{gcp}} \sin\delta\right). \tag{6}$$

Thus, the second-order phase-swing behavior of the PLL that considers the VSC–grid interaction can be characterized by (6). On the basis of this, the equivalent diagram of the SRF-PLL can be drawn, as shown in Fig. 4.

C. Equilibrium Points

The stable operation of the system requires the existence of equilibrium points, where $v_{\text{PCC}q} = 0$, leading to

$$I_d X_{\text{line}} + I_q R_{\text{line}} = V_{\text{gcp}} \sin\delta. \tag{7}$$

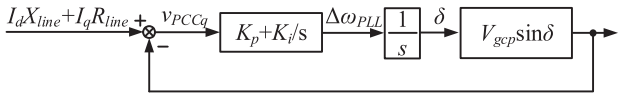

Fig. 4. Equivalent diagram of the SRF-PLL considering the effect of the line impedance.

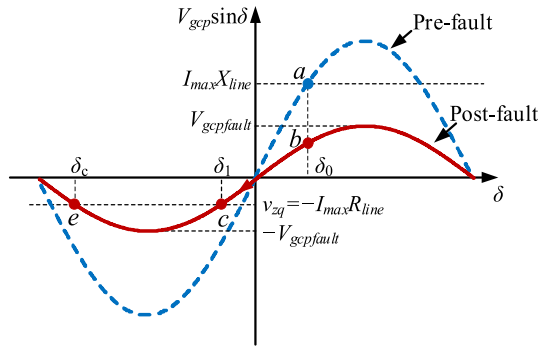

Fig. 5. Voltage–angle curves of the grid-connected VSC when $-I_{\max}R_{\text{line}} > -V_{\text{gcpfault}}$.

The existence of the solution of (7) requires

$$\left|I_d X_{\text{line}} + I_q R_{\text{line}}\right| \le V_{\text{gcp}}. \tag{8}$$

It is known from (8) that the existence of the equilibrium points is affected by the injected active current and reactive current, the grid impedance, and the grid voltage magnitude during the fault. Equation (8) is always satisfied if $I_d X_{\text{line}} + I_q R_{\text{line}} = 0$, which can be realized by choosing $I_d = I_q = 0$ [18] or $I_d/I_q = -R_{\text{line}}/X_{\text{line}}$ [19]. However, these solutions violate the grid code [17]. Considering the specific amount of the injected active current and reactive current required by the grid code, the loss of equilibrium points is more likely to happen during severe faults (small V_{gcp}) under the weak grid condition (large X_{line} and R_{line}). The LOS will be inevitable if there is no equilibrium point during grid faults [10], and it may also take place even if the equilibrium point exists [12], which will be detailed in the following section.

III. Design-Oriented Transient Stability Analysis

In this section, the LOS mechanism of VSCs during grid faults is elaborated. Depending on the number of equilibrium points, two operating scenarios of the VSC are considered, i.e., the VSC with two equilibrium points and the VSC with single equilibrium point during the grid fault.

Fig. 5 illustrates the voltage–angle curves of the VSC before and after the fault, which are drawn based on (6). The VSC is usually controlled with the unity power factor in the steady state, i.e., $I_d = I_{\max}$, $I_q = 0$, where $I_{\max}$ denotes the rated current of the VSC. Therefore, v_{zq} can be simplified as $I_d X_{\text{line}} + I_q R_{\text{line}} = I_{\max} X_{\text{line}}$. The dashed line in Fig. 5 illustrates the curve of $V_{\text{gcp}}\sin\delta$ before the grid fault, where the system is initially operated at the equilibrium point a, where $I_{\max} X_{\text{line}} = V_{\text{gcp}}\sin\delta_0$.

Once the fault occurs, the GCP voltage magnitude drops to $V_{\rm gcpfault}$, and the curve of $V_{\rm gcpfault}\sin\delta$ is shifted as shown by the solid line in Fig. 5. According to the grid code [17], the VSC needs to provide 2% reactive current per percent of the voltage drop, and a full reactive current is thus required when the GCP voltage is below half of the nominal value, i.e., $I_d = 0$, $I_q = -I_{\max}$. As a consequence, v_{zq} is changed as $I_d X_{\rm line} + I_q R_{\rm line} = -I_{\max} R_{\rm line}$. It is obvious that the VSC will lose the synchronism with the grid if $-I_{\max} R_{\rm line} < -(V_{\rm gcpfault}\sin\delta)_{\max} = -V_{\rm gcpfault}$, since there is lack of equilibrium points [10].

On the other hand, the LOS can also arise even if there are equilibrium points during the fault [12]. From the solid line in Fig. 5, it is clear that the system has two equilibrium points when $-I_{\max} R_{\rm line} > -V_{\rm gcpfault}$, which are, similar to the power–angle curve of the SG, denoted as the stable equilibrium point (SEP) *c* and the unstable equilibrium point (UEP) *e* [27]. Yet, when $-I_{\max} R_{\rm line} = -V_{\rm gcpfault}$, the system only has single equilibrium point.

A. LOS Mechanism of VSCs With Two Equilibrium Points During Faults

As shown by the solid line in Fig. 5, the operating point of the system moves from the point *a* to the point *b* at the fault-occurring instant. Since $-I_{\max} R_{\rm line} < V_{\rm gcpfault}\sin\delta_0$ (i.e., $v_{{\rm PCC}q} < 0$) at the point *b*, the output frequency of the PLL starts to decrease, which leads to a decrease in δ. The frequency continues to decrease until it reaches the SEP *c*, where $-I_{\max} R_{\rm line} = V_{\rm gcpfault}\sin\delta_1$, as shown in Fig. 5. Since the output frequency of the PLL is below the grid frequency at the point *c*, δ continues to decrease, yet the output frequency of the PLL begins to increase after the point *c* due to $-I_{\max} R_{\rm line} > V_{\rm gcpfault}\sin\delta$ (i.e., $v_{{\rm PCC}q} > 0$). Consequently, the following two possible operating scenarios can take place.

1) The output frequency of the PLL recovers to the grid frequency before the UEP *e*. As $-I_{\max} R_{\rm line} > V_{\rm gcpfault}\sin\delta$ (i.e., $v_{{\rm PCC}q} > 0$) still holds before the UEP *e*, the output frequency of the PLL further increases, which results in an increase in δ. Thus, the operating point of the PLL retraces the $V_{\rm gcpfault}\sin\delta$ curve and finally reaches the SEP *c* after several cycles of oscillation, and the system is stable.
2) The output frequency of the PLL is still below the grid frequency at the UEP *e*, Then, the output frequency turns to decrease again after the point *e*, due to $-I_{\max} R_{\rm line} < V_{\rm gcpfault}\sin\delta$ (i.e., $v_{{\rm PCC}q} < 0$), and δ keeps decreasing. The system eventually loses the synchronism with the grid.

B. Parametric Effect of the PLL on Transient Stability of VSCs With Two Equilibrium Points During Faults

Following the analysis of the LOS mechanism of VSCs with two equilibrium points during faults, the parametric effect of the PLL is analyzed in this section. As a second-order dynamic system, the PLL are generally characterized by two important parameters, i.e., the damping ratio (ζ) and the setting time (t_s) [23], which can be expressed by the controller parameters of the PLL as follows [24]:

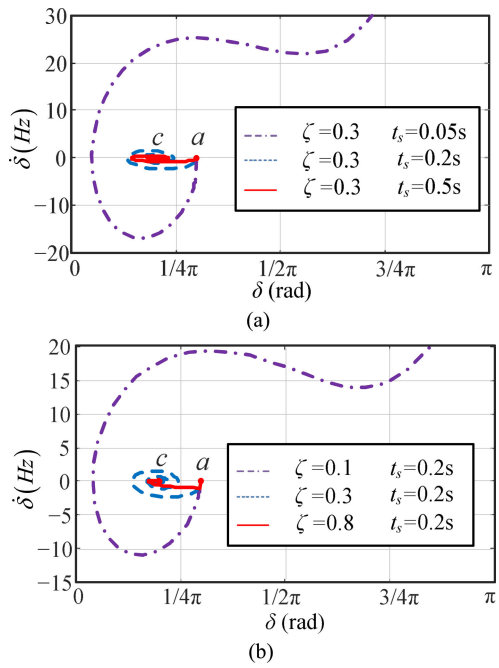

Fig. 6. Phase portraits of the PLL when $V_{\rm gcp}$ drops from 1 to 0.6 p.u. (a) $\zeta = 0.3$ and $t_s = 0.05$ s (unstable), 0.2 s (stable), and 0.5 s (stable). (b) $t_s = 0.2$ s and $\zeta = 0.1$ (unstable), 0.3 (stable), and 0.8 (stable).

$$\zeta = \frac{K_p}{2}\sqrt{\frac{V_{\rm gn}}{K_i}} \tag{9}$$

$$t_s = \frac{9.2}{V_{\rm gn} K_p} \tag{10}$$

where $V_{\rm gn}$ is the nominal grid voltage. Applying the derivation on both sides of (6), and considering the relationship $X_{\rm line} = (\omega_{\rm gn} + \dot{\delta})L_{\rm line}$ yields the following:

$$\ddot{\delta} = \frac{K_i}{1 - K_p I_d L_{\rm line}}\left[I_d\left(\omega_{\rm gn} + \dot{\delta}\right)L_{\rm line} + I_q R_{\rm line} - V_{\rm gcp}\sin\delta\right] - \frac{K_p V_{\rm gcp}\cos\delta}{1 - K_p I_d L_{\rm line}}\cdot\dot{\delta}. \tag{11}$$

Then, substituting (9) and (10) into (11), the parametric effect of the PLL on the transient stability of the VSC during the grid fault can be evaluated. As for the second-order nonlinear dynamic system, the phase portrait approach provides an intuitive and design-oriented analysis [28], [29].

1) Influences of the Settling Time and Damping Ratio of the PLL: For illustrations, three phase portraits based on (11) are plotted in Fig. 6. The impacts of different settling times with the same damping ratio are evaluated in Fig. 6(a), whereas the effects of different damping ratios with the same settling time are analyzed in Fig. 6(b). Points *a* and *c* represent the SEPs of the system before and after the fault, respectively. It is clear that the system is stable when the phase portrait converges to the SEP *c* after the fault, as shown by the solid and dashed lines in Fig. 6, and is unstable when the phase portrait is diverged, as

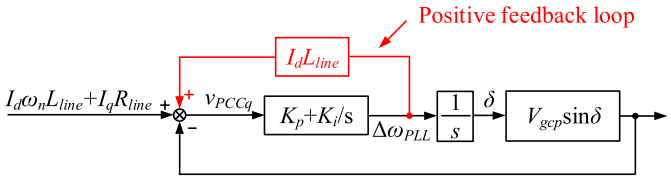

Fig. 7. Equivalent transformation of the block diagram of the SRF-PLL considering the effect of the frequency-dependent line reactance.

shown by dashed-dotted lines in Fig. 6. Therefore, two important conclusions can be drawn.

1) Reducing the settling time of the PLL jeopardizes the transient stability of the VSC, as shown in Fig. 6(a). This fact is resulted from the frequency-dependent nature of the line reactance, which inherently introduces a positive feedback loop. Considering the relationship $X_{\text{line}} = (\omega_n + \dot{\delta})L_{\text{line}}$, v_{zq} in (3) can be rewritten as $v_{zq} = I_d\omega_n L_{\text{line}} + I_q R_{\text{line}} + I_d\dot{\delta}L_{\text{line}}$, and, thus, Fig. 4 can be transformed as Fig. 7, where a positive feedback loop is formed with the term $I_d\dot{\delta}L_{\text{line}}$. Since the smaller settling time implies a larger K_p, the loop gain of the positive feedback loop is consequently increased, and the transient stability is further deteriorated. Yet, if the line impedance is pure resistive ($L_{\text{line}} = 0$) or there is no active current injection ($I_d = 0$), the positive feedback loop shown in Fig. 7 will not exist and the settling time has no influence on the transient stability of the VSC, which has also been pointed out in [12].
2) Increasing the damping ratio of the PLL enhances the transient stability of the VSC, as shown in Fig. 6(b). From the analysis based on Fig. 5, it is known that the LOS takes place when the PLL has a phase overshoot crossing the UEP *e*. This phase overshoot can be reduced by increasing the damping ratio of the PLL [23], and consequently the transient stability of the VSC is enhanced. This conclusion is similar to the system with SGs, where the large damping term of the SG is also proven to be beneficial for its transient stability [27].

2) Critical Damping Ratio of the PLL: It is worth mentioning that the damping ratio of 0.707 is commonly chosen for the parameter tuning of the PLL [23], [24], yet it is inappropriate when the transient stability of the VSC is concerned. Thus, the critical damping ratio that guarantees the transient stability of the system is quantified in the following.

Basically, the VSC will be stable after the large disturbance if δ is converged to the new equilibrium value and will be unstable if δ is diverged. The trajectory of δ can be obtained by solving (11). As (11) is the second-order nonlinear differential equation, only numerical solution is possible [29]. The critical damping ratio is identified by an iterative calculation procedure, as shown in Fig. 8. The damping ratio is initialized with a small positive value (e.g., 0.1), and then increased with a fixed step size during every iteration until the solution of (11) is converged. This procedure can be repeated to determine the critical damping ratios in different operating scenarios.

It is known from (3)–(6) that the dynamic of δ is affected not only by the postfault grid voltage V_{gcpfault}, but also by the

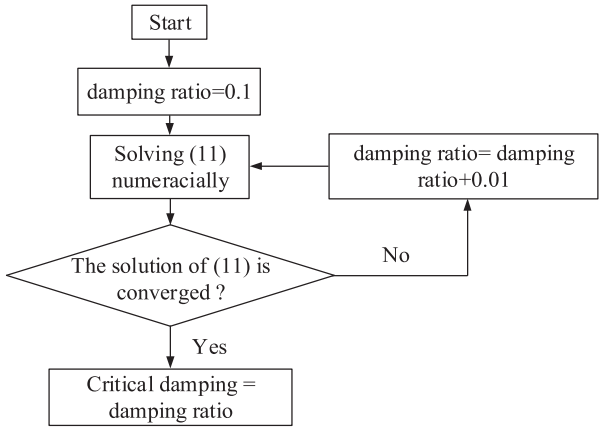

Fig. 8. Iterative calculation procedure for the critical damping ratio.

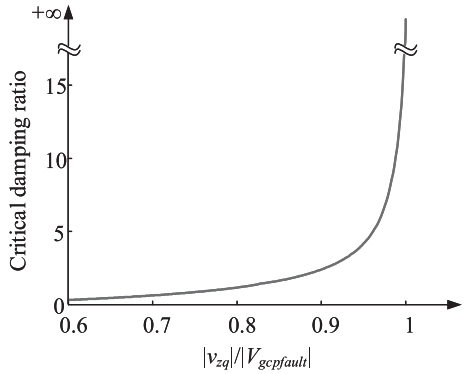

Fig. 9. Critical damping ratio with different $|v_{zq}|/|V_{\text{gcpfault}}|$ ratios.

q-axis voltage drop across the line impedance v_{zq}. Therefore, the critical damping ratios with different $|v_{zq}|/|V_{\text{gcpfault}}|$ ratios are plotted in Fig. 9. It is clear that the higher $|v_{zq}|/|V_{\text{gcpfault}}|$ ratio, the larger critical damping ratio is required. Moreover, when $|v_{zq}|/|V_{\text{gcpfault}}| = 1$, which corresponds to the case that the PLL has single equilibrium point, δ cannot be converged no matter how large the damping ratio is adopted. This phenomenon will be analytically explained in the following section.

C. Transient Stability of VSCs With Single Equilibrium Point During Faults

Fig. 10 illustrates the voltage–angle curve of the VSC under the condition of $v_{zq} = -I_{\max}R_{\text{line}} = -V_{\text{gcpfault}}$. In this case, the SEP *c* and the UEP *e* merge as a single point, and the output frequency of the PLL has to be recovered to the grid frequency at the point *c*(*e*) in order to remain the synchronism with the grid, i.e., $\dot{\delta} = 0$ at the point *c*(*e*). Consequently, the dynamic response of δ must be overdamped for a stable operation. Any small phase overshoots in the dynamic response can make the system cross over the point *c*(*e*), and eventually result in the LOS.

Applying the derivation on both sides of (6) yields

$$\begin{aligned}\ddot{\delta} &= (K_p + K_i\int)(I_dX_{\text{line}} + I_qR_{\text{line}} - V_{\text{gcp}}\sin\delta)\\ &= (K_p + K_i\int)(-I_{\max}R_{\text{line}} - V_{\text{gcpfault}}\sin\delta) = \dot{\delta}_1 + \dot{\delta}_2\end{aligned} \tag{12}$$

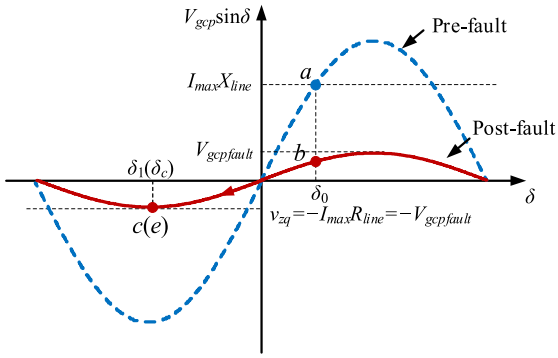

Fig. 10. Voltage–angle curves of grid-connected VSCs when $v_{zq} = -I_{\max}R_{\text{line}} = -V_{\text{gcpfault}}$.

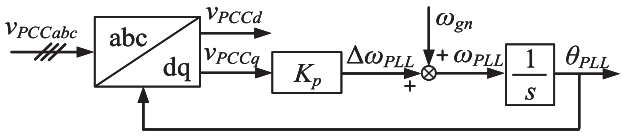

Fig. 11. Block diagram of the first-order PLL.

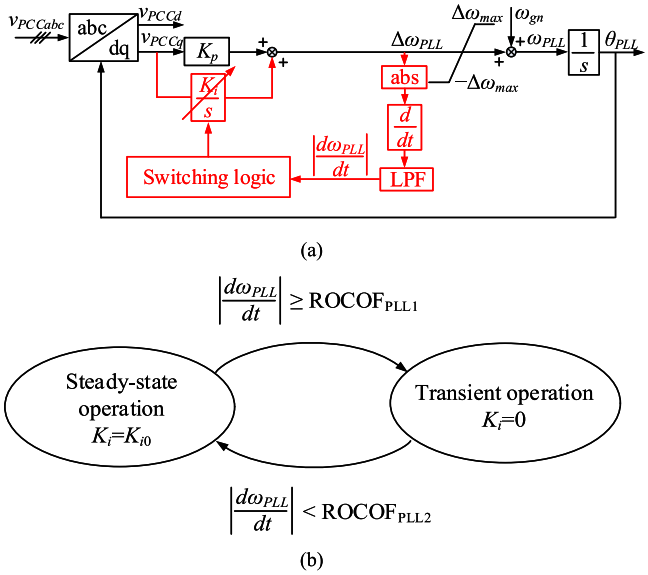

Fig. 12. Adaptive PLL for the transient stability enhancement. (a) Control block diagram. (b) Mode switching logic.

where

$$\dot{\delta}_1 = K_p\left(-I_{\max}R_{\text{line}} - V_{\text{gcpfault}}\sin\delta\right) \tag{13}$$

$$\dot{\delta}_2 = K_i\int\left(-I_{\max}R_{\text{line}} - V_{\text{gcpfault}}\sin\delta\right). \tag{14}$$

Since $-I_{\max}R_{\text{line}} = V_{\text{gcpfault}}\sin\delta$ holds at the equilibrium point $c(e)$, it is known from (13) that $\dot{\delta}_1 = 0$ at the point $c(e)$. Yet, $-I_{\max}R_{\text{line}} < V_{\text{gcpfault}}\sin\delta$ always holds during the dynamic process when the operating point moves from the point b to the point $c(e)$ under grid faults, as shown in Fig. 10. This makes the integration of $(-I_{\max}R_{\text{line}} - V_{\text{gcpfault}}\sin\delta)$, i.e., $\dot{\delta}_2$, smaller than zero at the point $c(e)$. Consequently, the condition $\dot{\delta} = \dot{\delta}_1 + \dot{\delta}_2 = \dot{\delta}_2 < 0$ always holds at the point $c(e)$ as long as $K_i > 0$. This fact implies that the SRF-PLL will cross over the point $c(e)$, and, thus, the LOS is inevitable for the VSC when there is only one equilibrium point during the fault, no matter how large the damping ratio is adopted.

IV. Adaptive PLL for the Transient Stability Enhancement

A. General Idea

From the analysis presented in Section III-C, the LOS of the VSC with single equilibrium point during the fault is inevitable as long as $K_i > 0$. However, by setting K_i equal to 0, (12) can be simplified as $\dot{\delta} = \dot{\delta}_1 = K_p(-I_{\max}R_{\text{line}} - V_{\text{gcpfault}}\sin\delta)$, and consequently $\dot{\delta} = 0$ will always hold at the SEP. The transient stability of the VSC can thus be guaranteed as long as the equilibrium point exists.

However, with $K_i = 0$, the SRF-PLL becomes a first-order PLL [30], as shown in Fig. 11. The first-order PLL does mitigate the LOS problem during grid faults as long as equilibrium points exist, yet it suffers from the steady-state phase-tracking error when the grid frequency deviates from its nominal value [23]. To tackle this challenge, an adaptive PLL is introduced for enhancing the transient stability of the VSC. The basic idea of this method is to make the VSC operating with the SRF-PLL during the steady-state operation to achieve the zero phase-tracking error, and the SRF-PLL is switched to the first-order PLL only during grid fault-occurring/clearing process, which thus guarantees the transient stability of the VSC.

Fig. 12(a) illustrates the control diagram of the adaptive PLL, and its switching logic is given in Fig. 12(b). Since $v_{\text{PCC}q}$ has an abrupt change during large grid disturbances, leading to an abrupt change of $\Delta\omega_{\text{PLL}}$ detected by the PLL, the integral gain K_i can thus be changed based on the rate of change of frequency (ROCOF) detected by the PLL, i.e.

$$\begin{aligned} K_i &= 0, \left|\frac{d\omega_{\text{PLL}}}{dt}\right| \geq \text{ROCOF}_{\text{PLL1}} \\ K_i &= K_{i0}, \left|\frac{d\omega_{\text{PLL}}}{dt}\right| < \text{ROCOF}_{\text{PLL2}} \end{aligned} \tag{15}$$

where K_{i0} is the designed integral gain of the PLL during the steady-state operation, $\Delta\omega_{\max}$ denotes the output frequency limit of the PLL. $\text{ROCOF}_{\text{PLL1}}$ and $\text{ROCOF}_{\text{PLL2}}$ represent the threshold values of ROCOF for switching the PLL between two different modes, respectively. $|d\omega_{\text{PLL}}/dt|$ is the ROCOF detected by the PLL, which is obtained by applying derivation to the absolute value of its output frequency, and a first-order low-pass filter (LPF) is added after the derivation in order to attenuate the high-frequency noise, i.e.,

$$G_{\text{LPF}}(s) = \frac{1}{T_{\text{filter}}s + 1} \tag{16}$$

where T_{filter} is the time constant of the LPF. $T_{\text{filter}} = 180$–240 ms is recommended in [31], and $T_{\text{filter}} = 200$ ms is selected in this article.

It should be noted that the frequency detected by the PLL can be deviated from the real grid frequency at the fault instant [32]. Hence, the adaptive PLL proposed in this article does not rely on the derivative of the real grid frequency for the fault detection. In contrast, the high $|d\omega_{\rm PLL}/dt|$ detected by the PLL essentially represents an abrupt change of $v_{{\rm PCC}q}$, which indicates the large grid disturbances and dictates the mode switching, as shown in Fig. 12.

B. Selection of $ROCOF_{PLL1}$ and $ROCOF_{PLL2}$

In order to adaptively switch the SRF-PLL to the first-order PLL during grid transients, it is known from (15) that $\text{ROCOF}_{\rm PLL1}$ should be selected smaller than $|d\omega_{\rm PLL}/dt|$ detected by the PLL at the fault instant. Therefore, the upper boundary of $\text{ROCOF}_{\rm PLL1}$ can be given by

$$\begin{aligned}\text{ROCOF}_{\rm PLL1} &\le \left|\frac{d\omega_{\rm PLL}}{dt}\right|_{\rm fault} \\ &\approx \left(1-e^{-\Delta t/T_{\rm filter}}\right)\left|\left(\frac{\dot{\delta}_{\rm fault}-\dot{\delta}_{\rm prefault}}{\Delta t}\right)\right| \\ &= \left(1-e^{-\Delta t/T_{\rm filter}}\right)\left|\frac{\dot{\delta}_{\rm fault}}{\Delta t}\right| \end{aligned} \tag{17}$$

where $\dot{\delta}_{\rm prefault}$ is the output frequency deviation of the PLL before the fault, which is zero. $\dot{\delta}_{\rm fault}$ is the output frequency deviation of the PLL at the fault instant, which can be calculated based on (12). Δt represents the time duration of the fault transient, which is usually less than half-cycle of the grid voltage, i.e., $\Delta t \le 10$ ms [33]. $1-e^{-\Delta t/T_{\rm filter}}$ represents the dynamic response of the LPF used in Fig. 12(a) [34].

Substituting (12) into (17) yields the following

$$\begin{aligned}\text{ROCOF}_{\rm PLL1} &\le \left|\frac{d\omega_{\rm PLL}}{dt}\right|_{\rm fault} \\ &\approx \left(1-e^{-\Delta t/T_{\rm filter}}\right) \\ &\quad\times\frac{(K_p+K_i\int)|(-I_{\max}R_{\rm line}-V_{\rm gcpfault}\sin\delta)|}{\Delta t} \\ &= \left(1-e^{-\Delta t/T_{\rm filter}}\right) \\ &\quad\times\frac{(K_p+K_i\int)(I_{\max}R_{\rm line}+V_{\rm gcpfault}\sin\delta)}{\Delta t}. \end{aligned} \tag{18}$$

Since $\delta > 0$ always holds at the fault instant, the sufficient condition of (18) is derived as

$$\text{ROCOF}_{\rm PLL1} \le \left(1-e^{-\Delta t/T_{\rm filter}}\right)\frac{K_pI_{\max}R_{\rm line}}{\Delta t}. \tag{19}$$

Substituting (10) into (19) yields the following:

$$\text{ROCOF}_{\rm PLL1} \le \frac{9.2I_{\max}R_{\rm line}}{V_{\rm gn}t_s\Delta t}\left(1-e^{-\Delta t/T_{\rm filter}}\right). \tag{20}$$

The typical value of $R_{\rm line}$ is 0.02 p.u. for the transmission grid [27], while this value is much larger in the distribution grid [27]. Nevertheless, the minimum value in the right-hand side of (20) is of concern to determine the upper boundary of $\text{ROCOF}_{\rm PLL1}$, and, thus, $R_{\rm line} = 0.02$ p.u. is selected in this article. The typical settling time of the PLL is 100 ms, i.e., $t_s = 100$ ms [24]. Substituting $V_{\rm gn} = 1$ p.u., $I_{\max} = 1$ p.u., $R_{\rm line} = 0.02$ p.u., $t_s = 100$ ms, and $\Delta t = 10$ ms into (20) yields $\text{ROCOF}_{\rm PLL1} \le 8.8$ Hz/s.

The lower boundary of $\text{ROCOF}_{\rm PLL1}$ is determined based on the criterion of avoiding the adaptive PLL to be wrongly switched to the first-order PLL during the steady-state operation. It is noted that the frequency fluctuation always exists in the real power grid [27]. The power system with a high penetration of renewable energy resources usually experiences a higher ROCOF [27], and the 2.5 Hz/s ROCOF withstand capability of the generation unit is specified in [35], which requires $\text{ROCOF}_{\rm PLL1} \ge 2.5$ Hz/s. Therefore, $\text{ROCOF}_{\rm PLL1}$ is selected in the range between 2.5 and 8.8 Hz/s. In this article, $\text{ROCOF}_{\rm PLL1} = 5$ Hz/s is selected in simulations and experimental tests.

When the adaptive PLL is switched to the first-order PLL at the fault instant, the system can always be stabilized at the new equilibrium point, after which the first-order PLL can be switched back to the SRF-PLL. The value of $|d\omega_{\rm PLL}/dt|$ converges to zero at the equilibrium point in theory, but noises always exist in practice. Therefore, a small positive value of $\text{ROCOF}_{\rm PLL2}$ is selected to enhance the robustness of the algorithm. In this article, $\text{ROCOF}_{\rm PLL2} = 0.5$ Hz/s is adopted in simulations and experimental tests.

It should be noted that if there is a grid frequency deviation during the fault, the steady-state phase-tracking error will be inevitable when the adaptive PLL switches to the first-order PLL. Consequently, the accuracy of the reactive current injection is also affected. However, this phase-tracking error can be compensated after the adaptive PLL switches back to the SRF-PLL (second-order PLL). The smaller time constant of the LPF can improve the dynamic of the switching between the first-order PLL and the SRF-PLL, but it also jeopardizes the robustness of the switching logic against noises. As will be shown in Section V, by using the LPF with the time constant of 200 ms, the adaptive PLL is kept as the SRF-PLL in most of the fault period, where the accurate reactive current injection can be guaranteed.

C. Comparative Analysis of Transient Stability of VSCs With Different PLLs

In this section, the transient stability of the VSC with different PLLs are compared with phase portraits. The main circuit parameters of the system are given in Table I. The lowest GCP voltage that theoretically guarantees the transient stability of the system can be calculated as $V_{\rm gcpfaultmin} = I_{\max}R_{\rm line} = 0.1$ p.u., i.e., when the GCP voltage drops below 0.1 p.u., the PLL does not have equilibrium points and the LOS is inevitable.

Three different cases with different PLL parameters, which are summarized in Table II, are compared. In cases I and II, the SRF-PLL is adopted during the normal operation and grid faults, and the difference between them is that the damping ratio is set as 0.5 in the case I and 1.5 in the case II. In case III, besides the parameters used in case II, the adaptive PLL shown in Fig. 12 is further employed to enhance the transient stability of the system.

TABLE I
MAIN CIRCUIT PARAMETERS USED IN SIMULATIONS

SYMBOL	DESCRIPTION	VALUE (P.U.)
V_{gcprms}	RMS value of the GCP voltage	33 kV (1 p.u.)
P	Power rating of the VSC	1 MW (1 p.u.)
f_g	Grid frequency	50 Hz (1 p.u.)
L_f	Inductance of the output filter	0.096 p.u.
L_{line}	Line inductance	0.28 p.u.
R_{line}	Line resistance	0.1 p.u.

TABLE II
CONTROL PARAMETERS OF THE PLL

SYMBOL	CASE I	CASE II	CASE III
PLL structure	SRF-PLL	SRF-PLL	Adaptive-PLL
ζ	0.5	1.5	1.5
t_s	0.1s	0.1s	0.1s

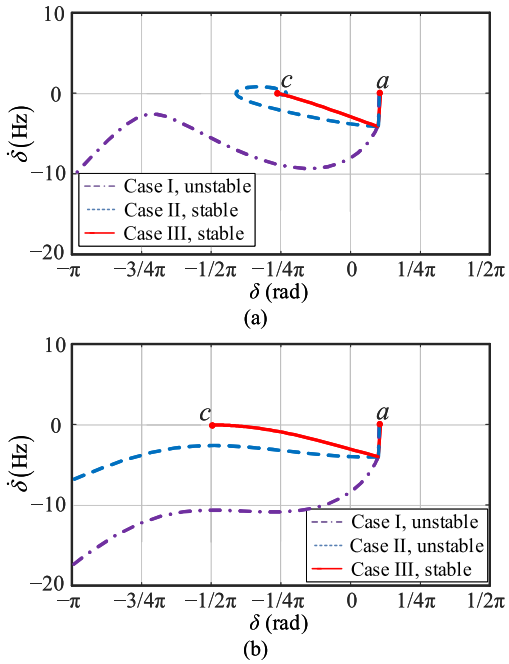

Fig. 13. Phase portraits of the PLL with different designs when the GCP voltage drops. (a) $V_{\rm gcp}$ drops to 0.14 p.u. (b) $V_{\rm gcp}$ drops to 0.10 p.u.

The large-signal nonlinear responses of different PLLs are analyzed by using phase portraits, which are plotted based on the dynamic equation given in (11). Different depths of voltage sags are evaluated, and two typical operating scenarios are considered, as shown in Fig. 13, where the points a and c represent the SEPs of the PLL before and after the fault, respectively. The system is stable if its phase portrait is converged to the new SEP c after the fault, and it becomes unstable if its phase portrait is diverged.

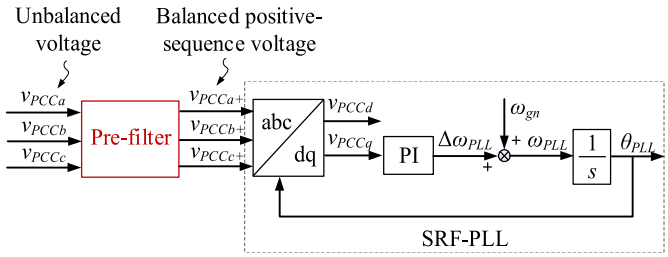

Fig. 14. Block diagram of the SRF-PLL with a prefilter used to extract the positive-sequence voltage.

Fig. 13(a) shows the phase portraits of different PLLs when the GCP voltage drops to 0.14 p.u. In this operating scenario, it can be calculated that $|v_{zq}|/|V_{\rm gcpfault}| = 0.1/0.14 = 0.71$, and it is known from Fig. 9 that the corresponding critical damping ratio is 0.695. Consequently, the LOS is inevitable in case I, due to $\zeta = 0.5 < 0.695$, as shown by the dashed-dotted line in Fig. 13(a). In contrast, the synchronization can still be remained in case II, where $\zeta = 1.5 > 0.695$, as shown by the dashed line in Fig. 13(a). Hence, it is clear that the transient stability of the system can be enhanced by the increased damping ratio of the PLL in this operating scenario. However, when the GCP voltage drops to the theoretically lowest voltage limit, i.e., 0.10 p.u., the system has only one equilibrium point and the system becomes unstable with the PLL parameters in both cases I and II. In contrast, the adaptive PLL can stabilize the system in both operating scenarios, as indicated by the solid lines in both Fig. 13(a) and (b).

D. Asymmetrical Faults

It is noted that only the symmetrical faults have been considered in the above-mentioned analysis. Yet, the asymmetrical faults, which introduce both positive- and negative-sequence voltages to the VSC, are more commonly seen in practice, and the zero-sequence voltage does not appear due to the use of the delta-wye transformers for VSCs [27].

During asymmetrical faults, a prefilter is generally used at the input of the SRF-PLL for extracting the positive-sequence voltage, as shown in Fig. 14 [36]–[38]. However, the prefilter is designed to have little effect on the synchronization stability of the SRF-PLL. This is because the prefilter needs to detect the positive-sequence voltage with a much faster speed than the synchronization dynamic of the SRF-PLL during the fault instant [24], such that there are no interactions between the sequence component detection and the grid synchronization [36].

Hence, the assumption that the input voltage of the SRF-PLL is three-phase balanced still holds during asymmetrical faults, thanks to the fast positive-sequence voltage detection of the prefilter. The performed analysis in this article is thus valid, and same conclusions, i.e., the transient stability of the VSC can be improved by increasing the damping ratio of the SRF-PLL, and it can be further enhanced by using the first-order PLL, can also be drawn for asymmetrical faults. This statement will be

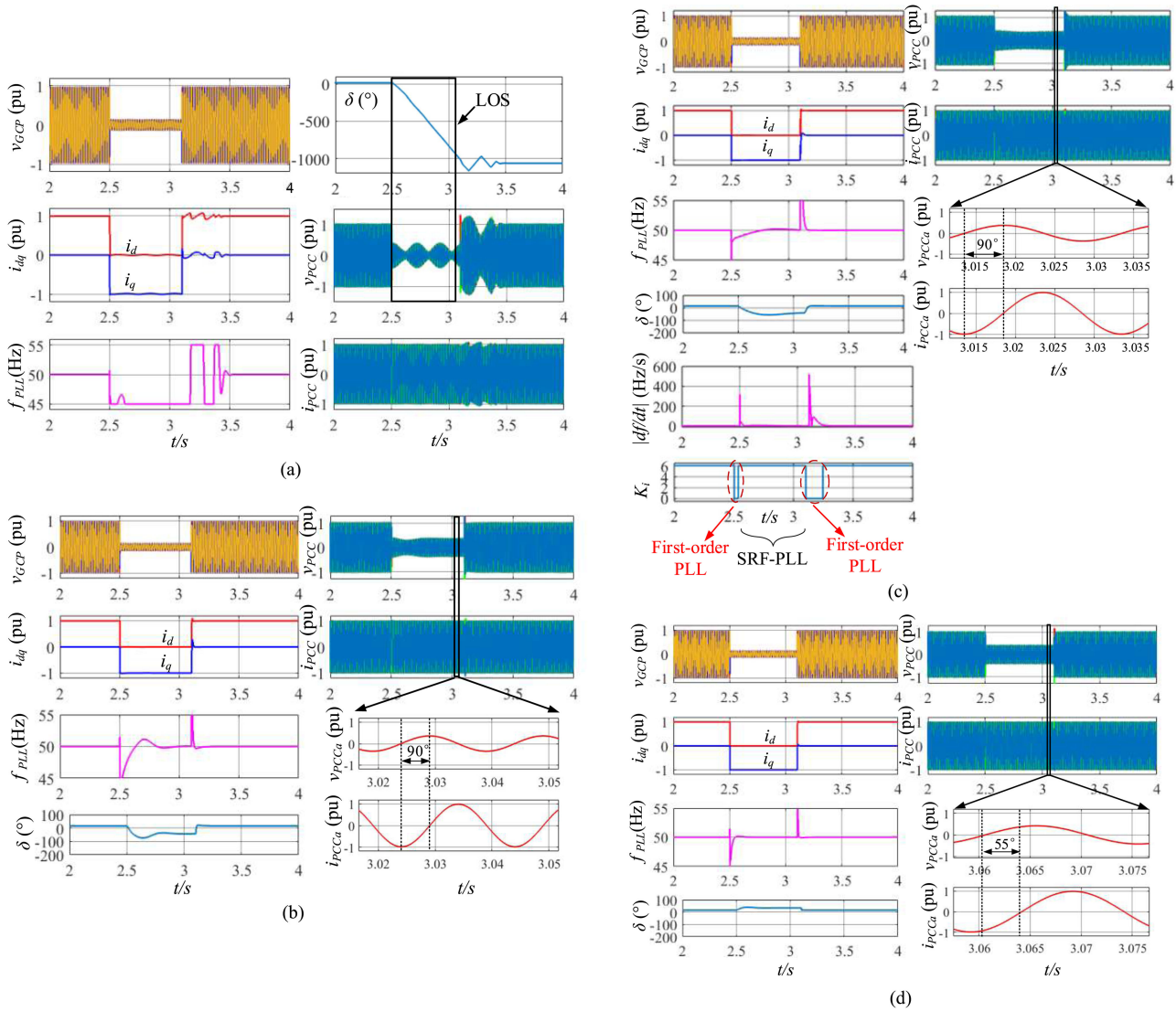

Fig. 15. Simulation results of the VSC during the symmetrical fault, where $V_{\rm gcp}$ drops to 0.14 p.u. (a) Case I: PLL with $\zeta = 0.5$, unstable. (b) Case II: PLL with $\zeta = 1.5$, stable and accurate phase angle detection. (c) Case III: adaptive PLL, stable and accurate phase angle detection. (d) Freezing the PLL: stable but inaccurate phase angle detection

further justified by the simulation and experiments performed in the following section.

V. Simulation and Experimental Results

A. Simulation Results

To validate the theoretical analysis, time-domain simulations are carried out in the MATLAB/Simulink and PLECS blockset with the nonlinear switching circuit model shown in Fig. 1. The parameters given in Tables I and II are adopted. The output frequency limits of the PLL are set as 45–55 Hz. In the normal operation, the VSC operates with $I_d = I_{\max}$, $I_q = 0$. During severe grid faults, the VSC injects the rated reactive current into the grid to support the grid voltage, i.e., $I_d = 0$, $I_q = -I_{\max}$.

Moreover, to further highlight the advantage of the proposed method, the method that freezes the PLL during the fault [16] is also simulated. In this method, the phase angle used with the VSC after freezing the PLL ($\theta_{\rm freeze}$) is determined by the measured phase angle and frequency of the PLL before it is frozen ($\theta_{\rm prefreeze}$ and $\omega_{\rm prefreeze}$), i.e., $\theta_{\rm freeze} = \theta_{\rm prefreeze} + \omega_{\rm prefreeze} \cdot t$.

Corresponding to the scenario considered in Fig. 13(a), Fig. 15 shows the simulation results of the VSC during the symmetrical fault, where three-phase voltages drop to 0.14 p.u. at $t = 2.5$ s, and the fault is cleared at $t = 3.1$ s. It is clear that the PLL with the parameter $\zeta = 0.5$ (case I) cannot remain synchronization with the grid during the fault, and the output frequency of the PLL is saturated at its lower limit (45 Hz), which cannot be recovered to the grid frequency, leading to a diverged δ, as shown in Fig. 15(a). However, the PLL with the parameter $\zeta = 1.5$ (case II) and the adaptive PLL (case III) can still be kept synchronized with the grid during the fault, as shown in Fig. 15(b) and (c). The simulation results agree well with the phase portrait analyses in Fig. 13(a).

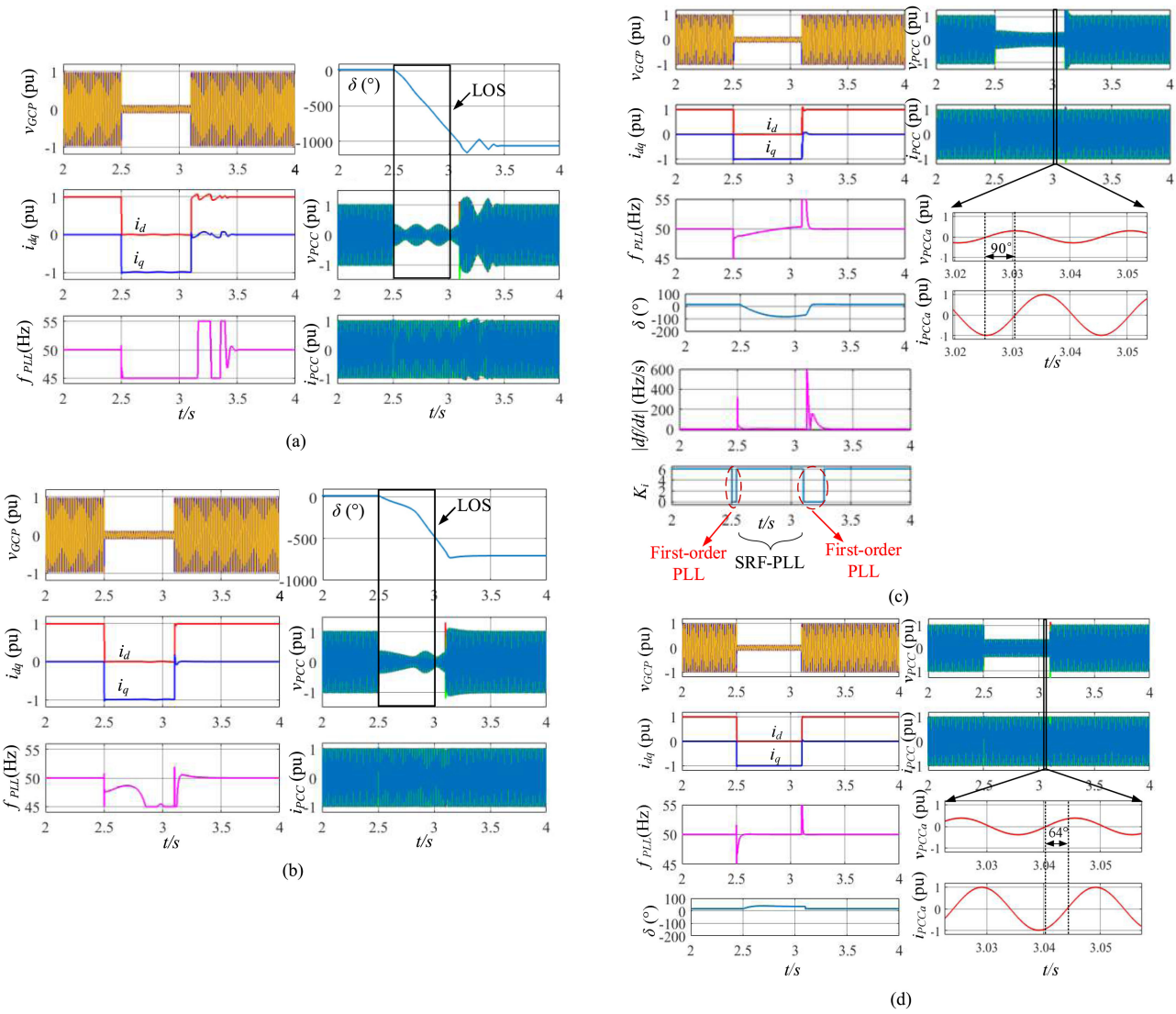

Fig. 16. Simulation results of the VSC during the symmetrical fault, where V_{gcp} drops to 0.10 p.u. (a) Case I: PLL with $\zeta = 0.5$, unstable. (b) Case II: PLL with $\zeta = 1.5$, unstable. (c) Case III: adaptive PLL, stable and accurate phase angle detection. (d) Freezing PLL: stable but inaccurate phase angle detection.

It is worth mentioning that K_i of the adaptive-PLL only switches to zero during the grid transients, i.e., the fault-occurring/-clearing instants, rather than the whole fault period. As shown in Fig. 15(c), K_i switches back to its designed value when the VSC reaches to a new steady state during the fault, which implies that the first-order PLL is switched back to the SRF-PLL. Thus, the accurate phase tracking of the PLL can be guaranteed even during the fault period. Moreover, the seamless transfer between the normal operation and the transient operation is also achieved with the adaptive PLL.

On the other hand, if the PLL is activated during the fault, the accurate phase angle detection can always be guaranteed if there is no LOS. As shown in Fig. 15(b) and (c), the phase difference between the PCC voltage and the injected current during the fault is 90°, indicating the pure reactive current injection. In contrast, by freezing the PLL, the phase angle is not affected by the grid voltage dip, and, thus, the stability can be remained. However, the VSC fails to detect the correct grid phase angle. As shown in Fig. 15(d), the phase difference between the PCC voltage and the injected current during the fault is 55°, indicating the VSC fails to inject the right amount of reactive current, which violates the grid code.

Fig. 16 shows the simulation results of the VSC during the symmetrical fault, where three-phase voltages drop to 0.10 p.u. at $t = 2.5$ s, which corresponds to the operating scenario in Fig. 13(b), and the fault is cleared at $t = 3.1$ s. Since there is only one equilibrium point during the fault, only the VSC with the adaptive PLL can be kept synchronized in this scenario, as shown in Fig. 16(a)–(c). The simulation results confirm the phase portrait analyses provided in Fig. 13(b). Moreover, by using the adaptive PLL, not only the transient stability, but also the accurate phase angle detection, can be guaranteed. As shown in Fig. 16(c), the phase difference between the PCC voltage and the injected current during the fault is 90°, indicating a purely reactive current injection. Similarly, by freezing the PLL, the stability can be guaranteed but the VSC fails to detect the right

grid phase angle, the phase difference between the PCC voltage and the injected current during the fault is 64°, as shown in Fig. 16(d). This indicates that the VSC fails to inject the rated reactive current if the PLL is frozen.

Figs. 17 and 18 further show the simulation results of the VSC during asymmetrical faults. The dual second-order generalized integrator based prefilter is adopted [38], and the parameters of the SRF-PLL given in Table II are used. The magnitudes of the positive-sequence voltages during asymmetrical faults are selected to be same as that used in the phase portrait analysis given by Fig. 13, which are 0.14 and 0.10 p.u., respectively.

Corresponding to the scenario considered in Fig. 13(a), Fig. 17 shows the simulation results of the VSC under the asymmetrical fault with $V_{\mathrm{gcp}a} = 0.42$ p.u. and $V_{\mathrm{gcp}b} = V_{\mathrm{gcp}c} = 0$ p.u., which corresponds to 0.14 p.u. positive-sequence voltage. It is clear that LOS occurs when the PLL with the parameter $\zeta = 0.5$ (case I) is adopted, as shown in Fig. 17(a). In contrast, the system can be kept stable by increasing the damping ratio of the PLL ($\zeta = 1.5$, case II) or using the adaptive PLL (case III), as shown in Fig. 17(b) and (c). The simulation results agree well with the phase portrait analysis shown in Fig. 13(a).

Corresponding to the scenario considered in Fig. 13(b), Fig. 18 shows the simulation result of the VSC under the asymmetrical fault with $V_{\mathrm{gcp}a} = 0.3$ p.u. and $V_{\mathrm{gcp}b} = V_{\mathrm{gcp}c} = 0$ p.u., which corresponds to 0.10 p.u. positive-sequence voltage. It is clear that the system can be kept stable only with the adaptive PLL, as shown in Fig. 18(c), which also agrees with the phase portrait analysis shown in Fig. 13(b).

Hence, the simulation results in Figs. 17 and 18 justify that the performed analysis also applies to asymmetrical faults where the prefiltered PLL is used, and the same findings can also be drawn, i.e., the transient stability of the VSC can be improved by increasing the damping ratio of the SRF-PLL, and it can be further enhanced by using the first-order PLL.

Fig. 19 shows the simulation result of the VSC with the adaptive PLL under the distorted grid voltage (including 5% of fifth-order harmonic and 8% of seventh-order harmonic). It is clear that neither the switching logic nor the grid phase angle detection accuracy is affected by the grid harmonics, indicating the strong robustness of the proposed adaptive-PLL against grid harmonics.

B. Experimental Results

To further verify the simulation results, the experimental tests are carried out with a three-phase grid-connected converter with the downscaled voltage and power ratings. However, the per unit values of parameters used in the experiment are the same as that used in the simulation, which are listed in Table III. The experimental setup is shown in Fig. 20. The circuit tested in the experiment is identical to that shown in Fig. 1. The control algorithm is implemented in the DS1007 dSPACE system, where the DS5101 digital waveform output board is used for generating the switching pulses, and the DS2004 high-speed A/D board is used for the voltage and current measurements. The active/reactive current, the output frequency, and the integral gain of the PLL are outputted through the DS2102 high-speed

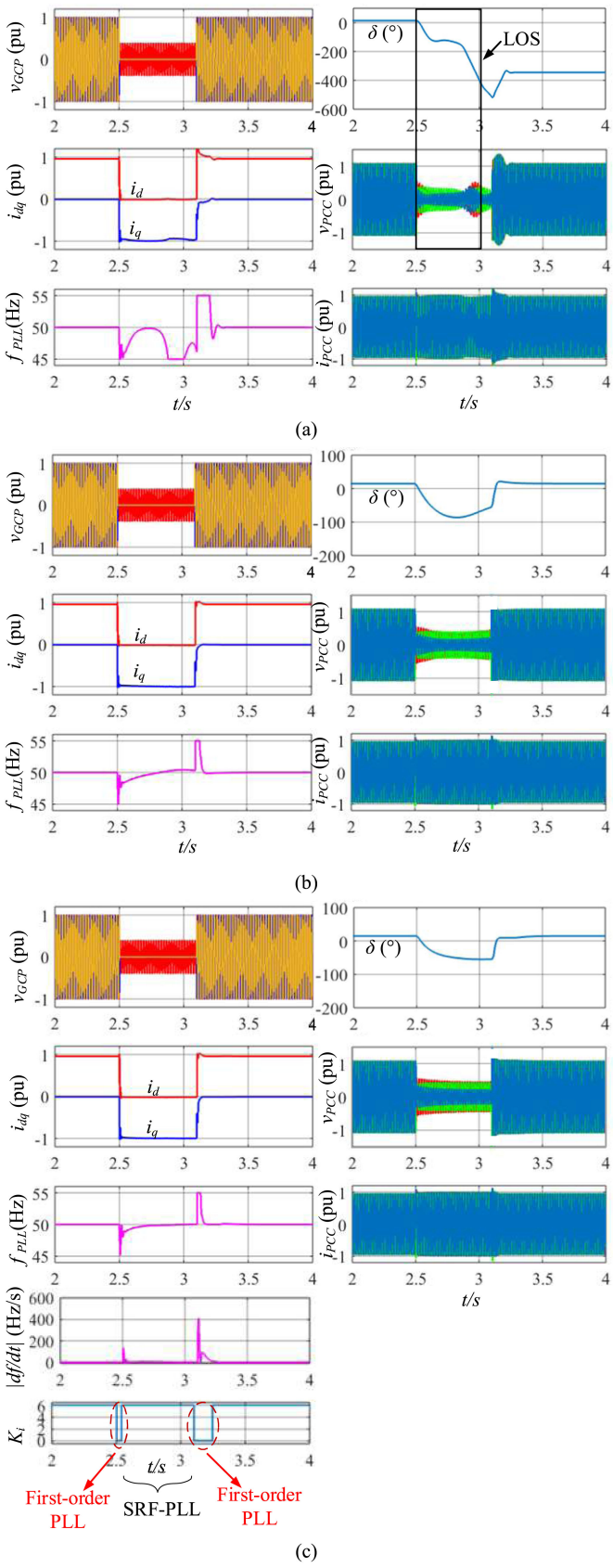

Fig. 17. Simulation results of the VSC during the asymmetrical fault, where $V_{\mathrm{gcp}a} = 0.42$ p.u. and $V_{\mathrm{gcp}b} = V_{\mathrm{gcp}c} = 0$ p.u. (a) Case I: PLL with the parameter $\zeta = 0.5$, unstable. (b) Case II: PLL with the parameter $\zeta = 1.5$, stable. (c) Case III: adaptive PLL, stable.

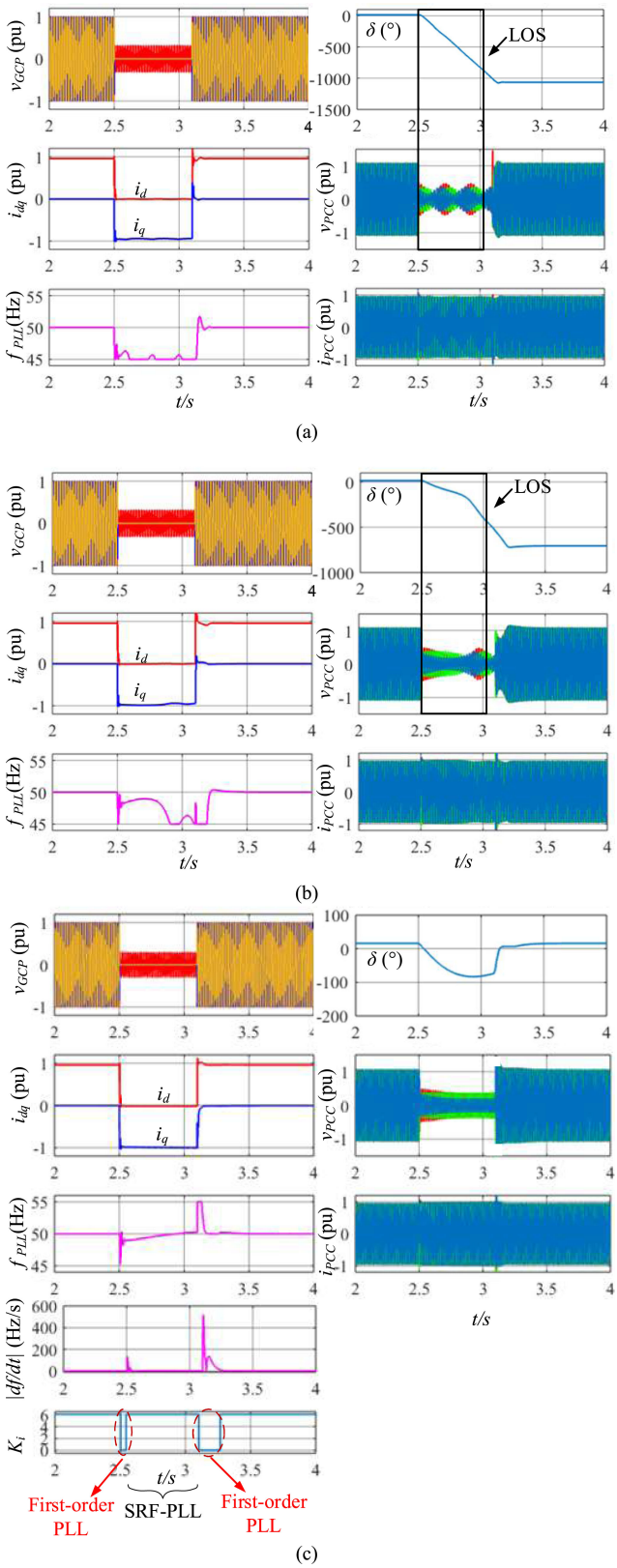

Fig. 18. Simulation results of the VSC during the asymmetrical fault, where $V_{\mathrm{gcp}a} = 0.3$ p.u. and $V_{\mathrm{gcp}b} = V_{\mathrm{gcp}c} = 0$ p.u. (a) Case I: PLL with the parameter $\zeta = 0.5$, unstable. (b) Case II: PLL with the parameter $\zeta = 1.5$, unstable. (c) Case III: adaptive PLL, stable.

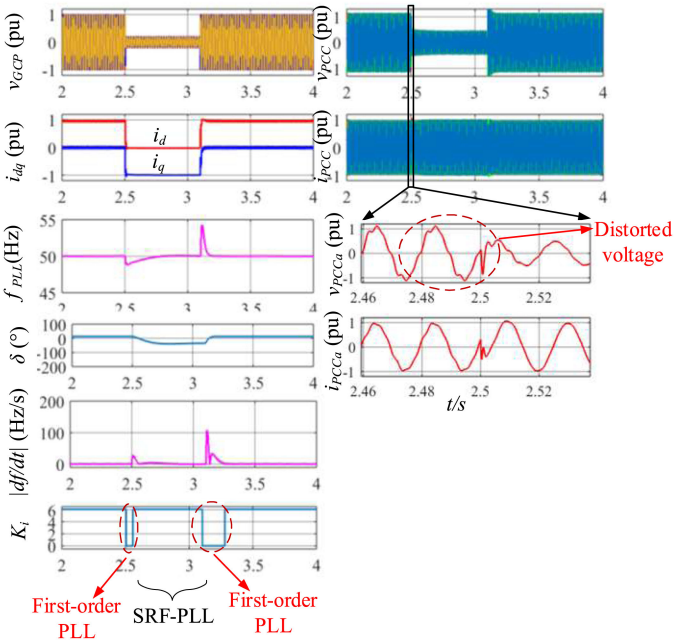

Fig. 19. Simulation results of the VSC with the adaptive PLL during the symmetrical fault. V_{gcp} drops to 0.2 p.u. and the grid voltage includes 5% of fifth-order harmonic and 8% of seventh-order harmonic.

TABLE III
MAIN CIRCUIT PARAMETERS USED IN EXPERIMENTS

SYMBOL	DESCRIPTION	VALUE (P.U.)
V_{gcprms}	RMS value of the GCP voltage	110 V (1 p.u.)
P	Power rating of the VSC	3.6 kW (1 p.u.)
f_g	Grid frequency	50 Hz (1 p.u.)
L_f	Inductance of the output filter	0.096 p.u.
L_{line}	Line inductance	0.28 p.u.
R_{line}	Line resistance	0.1 p.u.

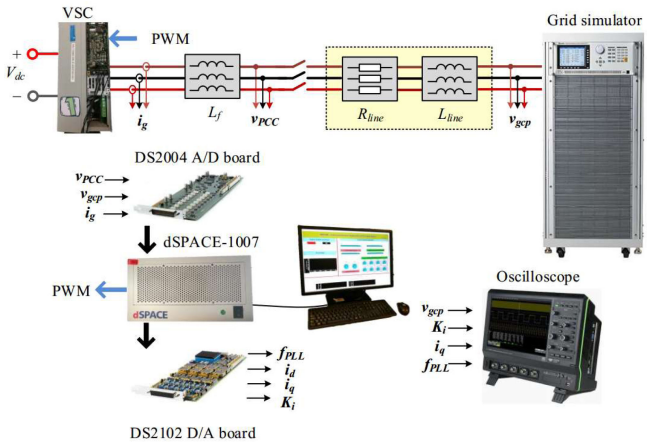

Fig. 20. Configuration of the experimental setup.

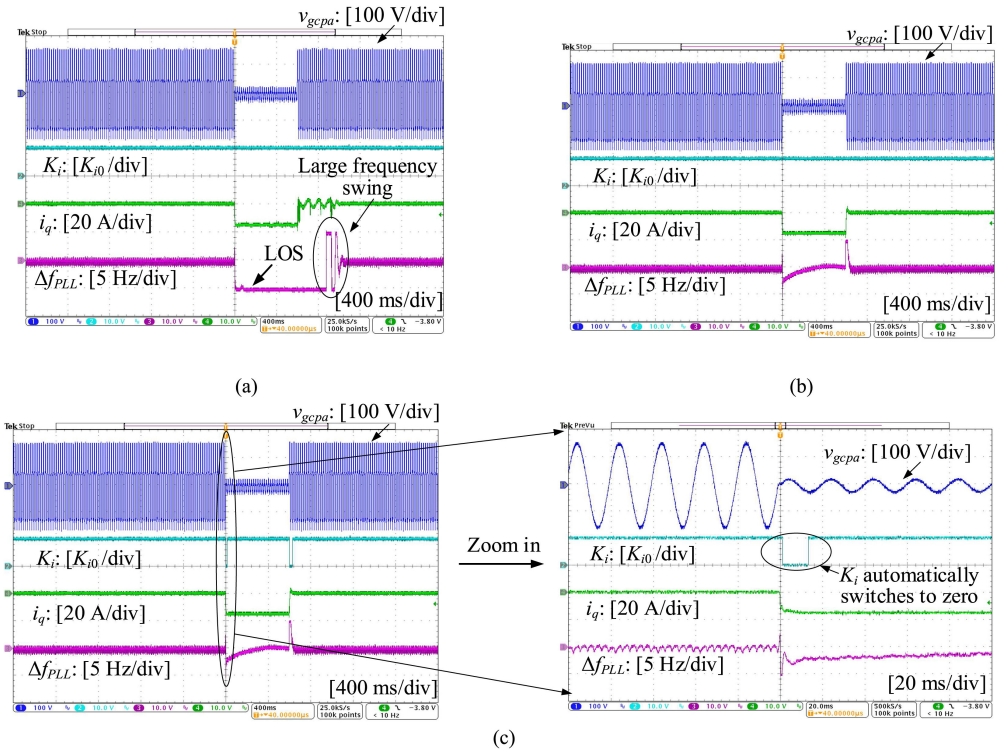

Fig. 21. Experimental results of the VSC with different designed PLLs during the symmetrical fault, where V_{gcp} drops to 0.14 p.u. (a) Case I: PLL with $\zeta = 0.5$, unstable. (b) Case II: PLL with $\zeta = 1.5$, stable. (c) Case III: adaptive PLL, stable.

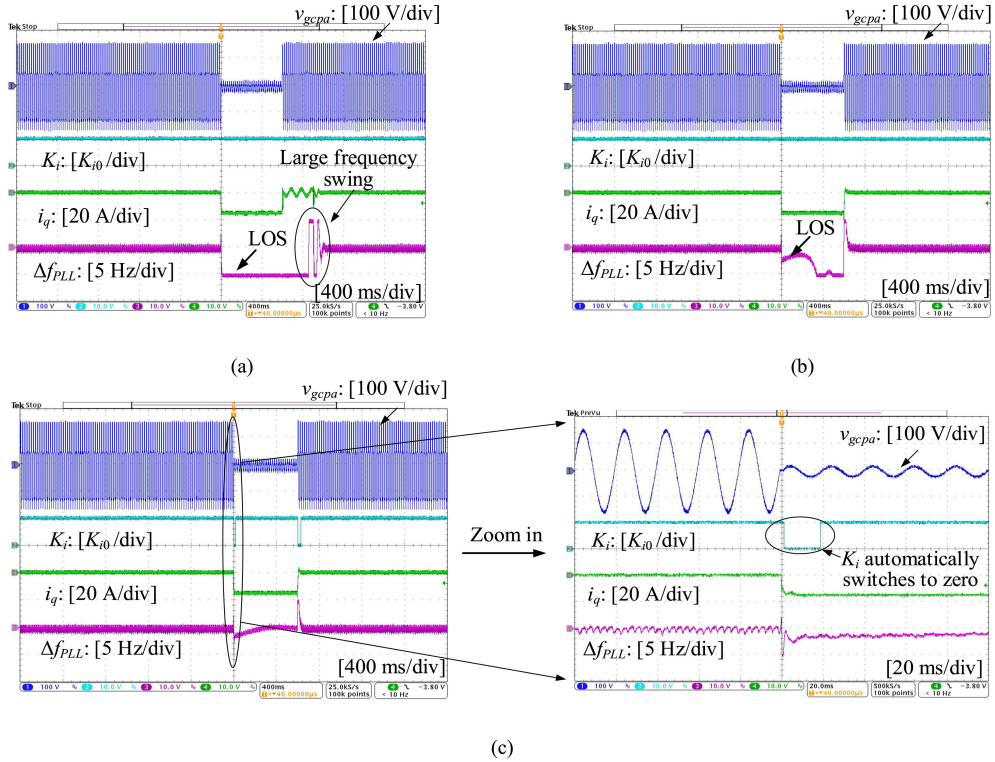

Fig. 22. Experimental results of the VSC with different designed PLLs during the symmetrical fault, where V_{gcp} drops to 0.10 p.u. (a) Case I: PLL with $\zeta = 0.5$, unstable. (b) Case II: PLL with $\zeta = 1.5$, unstable. (c) Case III: adaptive PLL, stable.

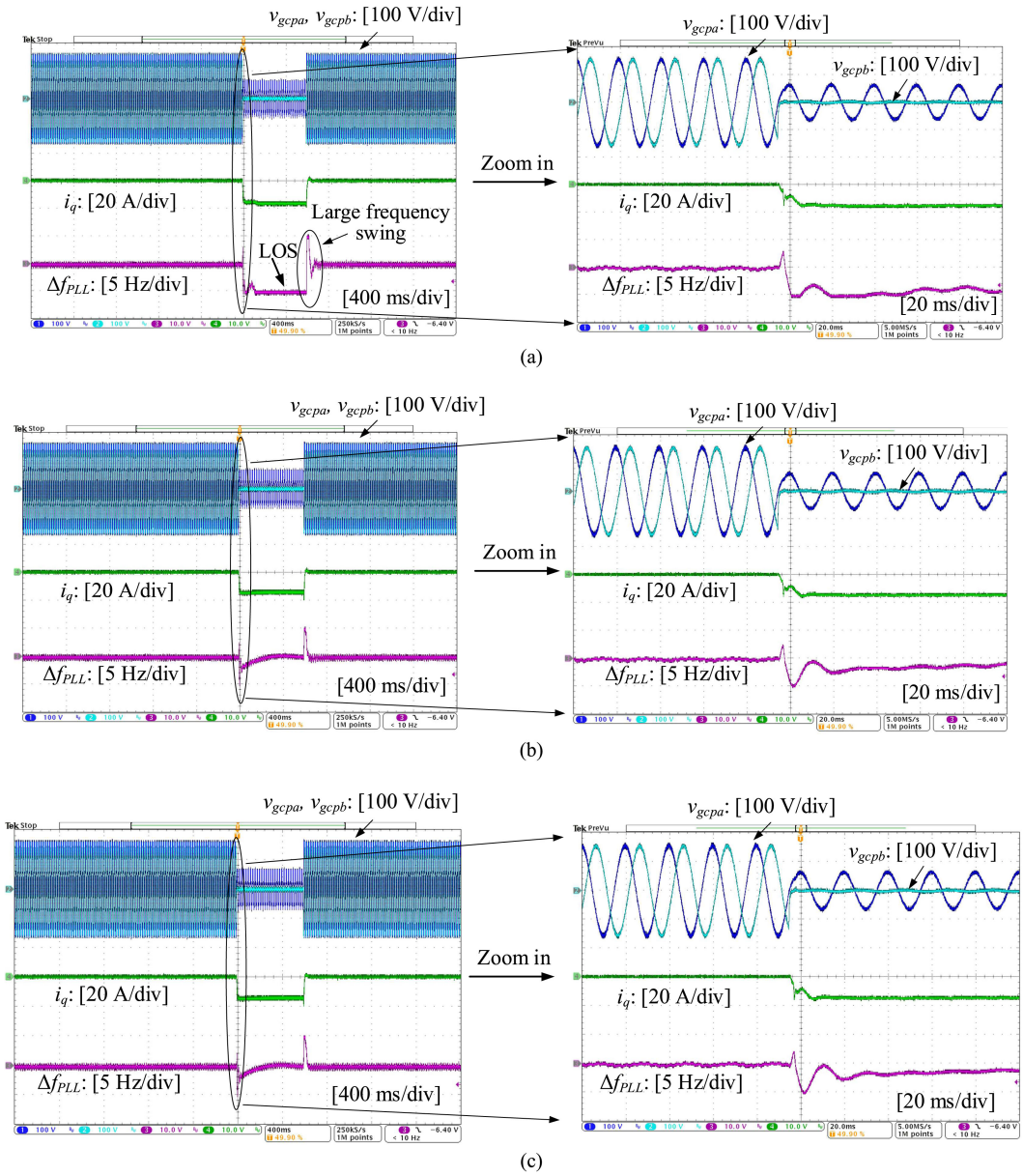

Fig. 23. Experimental results of the VSC during the asymmetrical fault, where $V_{\mathrm{gcp}a} = 0.42$ p.u. and $V_{\mathrm{gcp}b} = V_{\mathrm{gcp}c} = 0$ p.u. (a) Case I: PLL with the parameter $\zeta = 0.5$, unstable. (b) Case II: PLL with the parameter $\zeta = 1.5$, stable. (c) Case III: adaptive PLL, stable.

D/A board. A constant dc voltage supply is used at the dc side, and a 45-kVA Chroma 61850 grid simulator is used to generate the grid voltage.

Fig. 21 shows the measured results of the VSC during the symmetrical fault, where three-phase voltages drop to 0.14 p.u. Three different PLLs listed in Table II are compared. The VSC operates with $I_d = I_{\max}$ and $I_q = 0$ during the normal operation and $I_d = 0$ and $I_q = -I_{\max}$ when V_{gcp} drops more than 50% of the nominal voltage. It can be seen from Fig. 21(a) that the LOS of the system takes place when the PLL with parameter $\zeta = 0.5$ is used, where the output frequency of the PLL is saturated at the lower limit (45 Hz) and cannot be recovered to the nominal grid frequency during the fault. Moreover, a large frequency swing can be observed before the system is resynchronized with the grid during the grid voltage recovery. In contrast, both the PLL with $\zeta = 1.5$ and the adaptive PLL can be kept stable in this scenario, as shown in Fig. 21(b) and (c). These test results confirm the theoretical analysis and the simulation results in Figs. 13(a) and 15.

Fig. 22 shows the measured results of the VSC during the symmetrical fault, where three-phase voltages drop to 0.10 p.u. Three different PLLs listed in Table II are compared. It is clear that only the VSC with the adaptive PLL can be kept synchronized with the power grid, thanks to the fact that K_i of the adaptive PLL can be automatically switched to zero during the fault-occurring and fault-clearing transients, as shown in Fig. 22(c). The experimental tests match well with the theoretical predictions and the simulation case studies in Figs. 13(b) and 16.

Corresponding to the simulation studies carried out in Figs. 17 and 18, Figs. 23 and 24 show the measured results of the

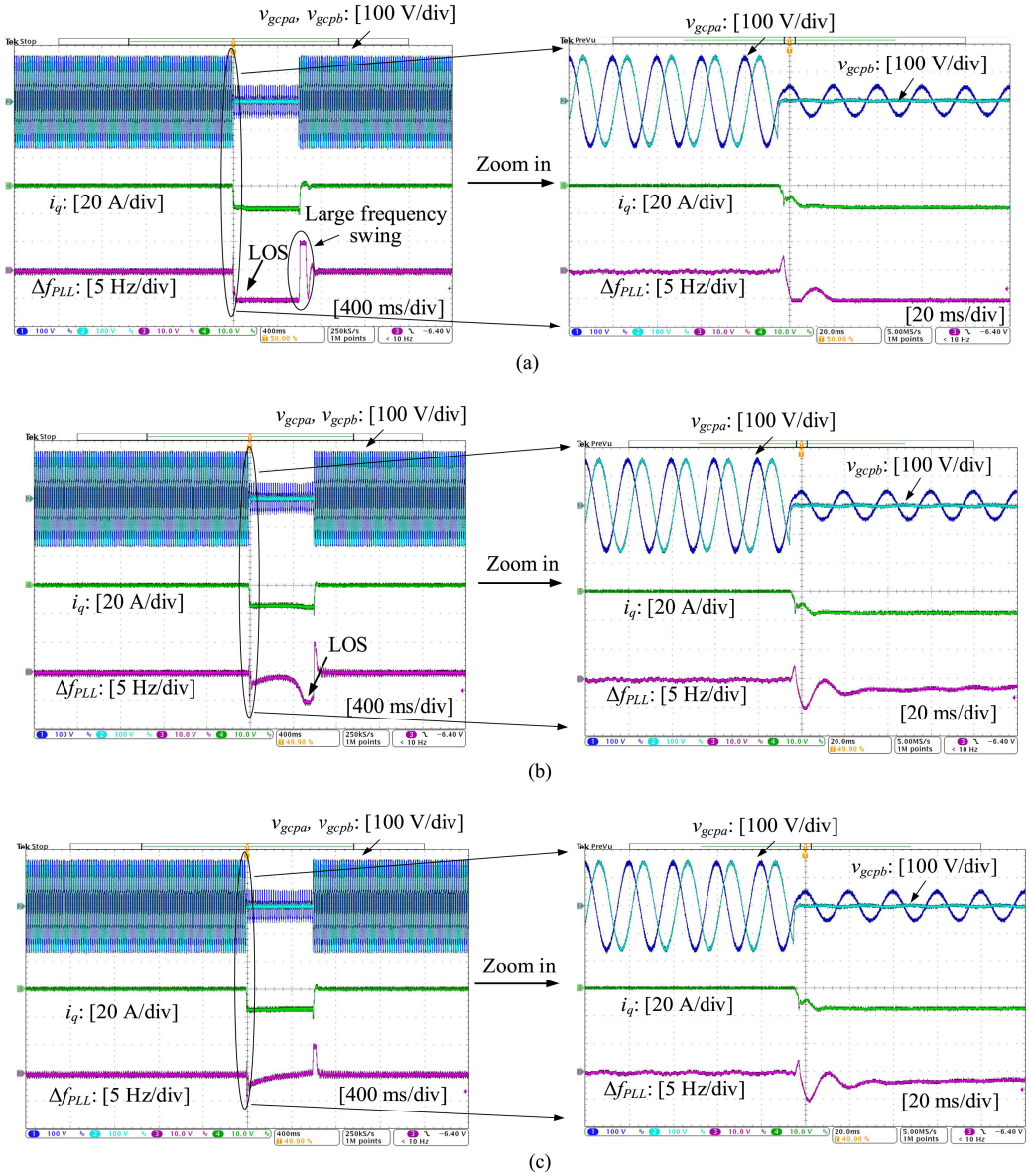

Fig. 24. Experimental results of the VSC during the asymmetrical fault, where $V_{\mathrm{gcp}a} = 0.3$ p.u. and $V_{\mathrm{gcp}b} = V_{\mathrm{gcp}c} = 0$ p.u. (a) Case I: PLL with the parameter $\zeta = 0.5$, unstable. (b) Case II: PLL with the parameter $\zeta = 1.5$, unstable. (c) Case III: adaptive PLL, stable.

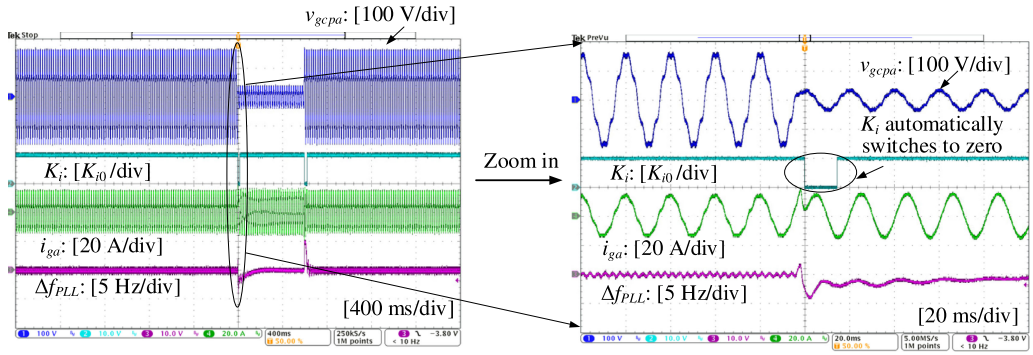

Fig. 25. Experimental results of the VSC with the adaptive PLL during the symmetrical fault. V_{gcp} drops to 0.2 p.u., and the grid voltage includes 5% of fifth-order harmonic and 8% of seventh-order harmonic.

VSC under asymmetrical faults. For the asymmetrical fault with $V_{\mathrm{gcp}a} = 0.42$ p.u. and $V_{\mathrm{gcp}b} = V_{\mathrm{gcp}c} = 0$ p.u., the LOS occurs when the PLL with the parameter $\zeta = 0.5$ (case I) is adopted, as shown in Fig. 23(a). Yet, the system can be kept stable by increasing the damping ratio of the PLL ($\zeta = 1.5$, case II) or using the adaptive PLL (case III), as shown in Fig. 23(b) and (c). Moreover, when $V_{\mathrm{gcp}a}$ is further dropped to 0.3 p.u., only the adaptive PLL can stabilize the system, as shown in Fig. 24(c). The experimental results match well with the simulation studies.

Fig. 25 shows the measured result of the VSC with the adaptive PLL under the distorted grid voltage (including 5% of fifth-order harmonic and 8% of seventh-order harmonic), and the satisfactory performance of the adaptive PLL can be observed, which further confirms the simulation results shown in Fig. 19.

VI. Conclusion

This article has analyzed the impact of the PLL on the transient stability of VSCs during grid faults. The large-signal nonlinear responses of the PLL with different parameters have been characterized by means of the phase portrait. The major findings of this article are summarized as follows.

1) The transient stability of the VSC can be enhanced by increasing the damping ratio of the SRF-PLL when the system has two equilibrium points during the fault. The value of the critical damping ratio to stabilize the system is identified based on the voltage ratio $|v_{zq}|/|V_{\mathrm{gcpfault}}|$. However, the LOS of the SRF-PLL is inevitable when only one equilibrium point exists during the fault.
2) In contrast to the SRF-PLL, the first-order PLL has no LOS problem whenever the system has equilibrium points, yet it suffers from the steady-state phase-tracking error when the grid frequency has a steady-state drift from its nominal value.
3) The proposed adaptive PLL enables the VSC to operate with the SRF-PLL in the steady-state operation and with the first-order PLL during the fault-occurring/-clearing transients, which not only guarantees the transient stability of the system, but also ensures the phase-tracking accuracy even during the grid fault.

All the findings have been elaborated theoretically and confirmed by time-domain simulations and experimental tests.

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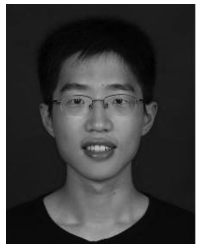

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