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Published in:
IEEE Transactions on Industry Applications

DOI (link to publication from Publisher):
10.1109/TIA.2019.2934024

Publication date:
2019

Document Version
Accepted author manuscript, peer reviewed version

Link to publication from Aalborg University

Citation for published version (APA):
Tanaka, T., Wang, H., & Blaabjerg, F. (2019). A DC-Link Capacitor Voltage Ripple Reduction Method for a Modular Multilevel Cascade Converter With Single Delta Bridge Cells. *IEEE Transactions on Industry Applications*, *55*(6), 6115 - 6126. [8792104]. https://doi.org/10.1109/TIA.2019.2934024

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A DC-link Capacitor Voltage Ripple Reduction Method for a Modular Multilevel Cascade Converter with Single Delta Bridge Cells (MMCC-SDBC)

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***Abstract*— This paper proposes a capacitor voltage ripple reduction method used for a Modular Multilevel Cascade Converter (MMCC) with Single Delta Bridge Cells (SDBC), by applying a third harmonic zero-sequence current. A practical case study on an 80 MVar/ 33 kV MMCC-SDBC based STATCOM is used to demonstrate the method. The impact of the third harmonic zero-sequence current level of the capacitor ripple reduction and the electro-thermal stresses on IGBT modules are analyzed. An optimal parameter of the current level is obtained by compromising the above performance factors. The obtained result shows that the required capacitance, as well as capacitor bank volume, are reduced by 20 % without increasing the total power semiconductor losses by using the proposed method.**

Keywords*— Modular Multilevel cascade Converter, STATCOM, Capacitor voltage ripple reduction, Zero-sequence current.

I. INTRODUCTION

The Modular Multilevel Cascade Converter (MMCC) family based on cascade connection of multiple single-phase converters has significant advantages for high power and high voltage applications compared with the conventional voltage source converters: such as easily scaling-up power and voltage ratings, lower harmonic distortion by multi-level voltage waveform and also modular/redundant operation. Therefore, the MMCC family has used for high voltage direct current (HVDC) transmission systems, High power Static Var Compensators (STATCOMs) and so on [1] [2].

A common disadvantage of the MMCC family is the low-frequency voltage ripple in each of the dc-link capacitors of the galvanic isolated single-phase converter. This increases size and cost and decreases the lifetime of the dc-link capacitors. In addition, the switching frequency of the single-phase converters of the MMCC family is set to be a very low value such as lower than several hundred Hz because of its multiple cascade connection structure. Although this can reduce the switching loss of each power module, this increases the capacitor voltage ripple. Therefore, the dc-link capacitor design should take the impact of the Pulse Width Modulation (PWM) into account [3], [4].

Research works published so far have proposed the dc-link capacitor voltage ripple reduction methods for one type of MMCC family with Double Star Chopper Cells (DSCC) based on cascade connection in a double star of multiple cascade chopper converters. The MMCC-DSCC solution is used in HVDC systems and Back-to-Back converter applications because of the function of converting AC/DC or DC/AC. The dc-link capacitor voltage ripple reduction methods can be classified into three principals. The first group is the second harmonic circulating current injection method [5-10]. The second group uses the circulating current with a combination of 2nd and 4th harmonic components. This enhances the reduction effect of the capacitor voltage ripple [11]. The third group uses both the circulating currents and the common-mode voltage of the DSCC, which enhances the reduction effect of the capacitor voltage ripple more [12], [13].

However, no studies have proposed dc-link capacitor voltage ripple reduction methods for another type of the MMCC family with Single Delta Bridge Cells (SDBC), which is based on cascade connection of single delta of H-bridge single-phase converter. The MMCC-SDBC solution is typically used for STATCOM applications. Unfortunately, the above-mentioned dc-link capacitor voltage ripple reduction methods for the MMCC-DSCC cannot directly be applied to the MMCC-SDBC because of the different circuit architecture. The development of the capacitor voltage ripple reduction method for the MMCC-SDBC is useful to reduce the cost and size of the converter for the STATCOM [14].

This paper proposes a method for dc-link capacitor voltage ripple reduction used only for one type of MMCC family with Single Delta Bridge Cells (SDBC) under STATCOM operation, which way injects the third harmonic zero-sequence current. Firstly, a case study model of the STATCOM based on MMCC-SDBC having a rating of 80 MVar/ 33 kV is presented [15]. Secondly, the principle of the capacitor voltage ripple reduction by

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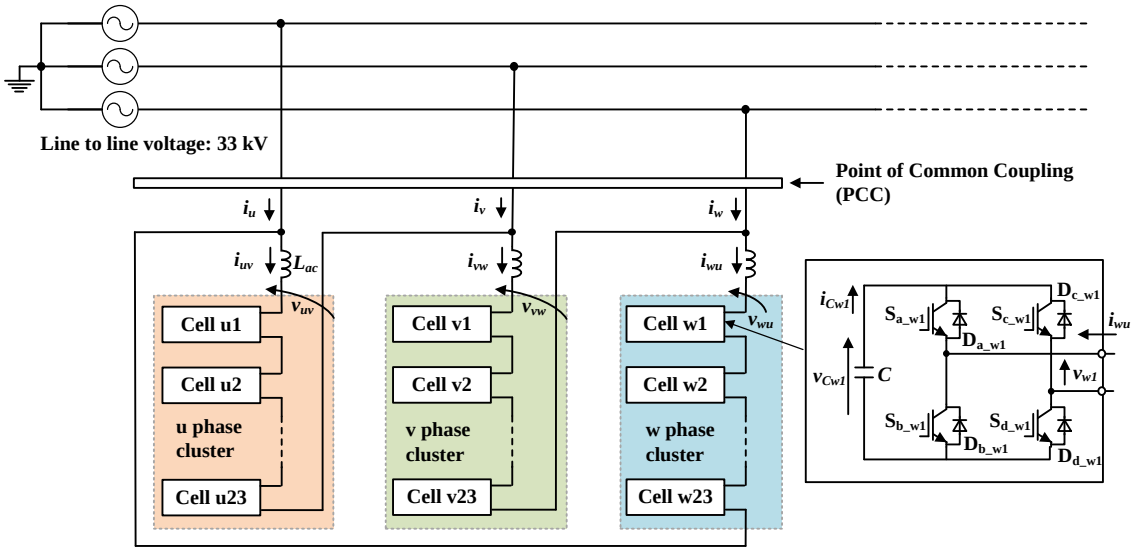

Fig. 1. The circuit configuration of the MMCC-SDBC.

using the proposed third harmonic zero-sequence current injection is presented. The mathematical formula of the dc-link capacitor voltage considering the Pulse Width Modulation (PWM) is also derived. Thirdly, the impact of the third harmonic zero-sequence current to the capacitor voltage ripple is analyzed based on the analytic model taking into account different reactive currents and grid voltages. Next, the electrical and thermal stress of each power module regarding the injected third harmonic zero-sequence current is analyzed based on the case study model. An optimum third-harmonic zero-sequence current to reduce the capacitor voltage ripple is also presented. Further, the capacitor bank of each case is designed considering the required capacitance and reliability. The capacitor bank volume reduction by applying the proposed method is finally discussed considering the obtained results.

II. The Theoretical Behavior of The DC-Link Capacitor Voltage

Fig. 1 shows the circuit configuration of the STATCOM based on an MMCC-SDBC having a rated 80 MVar power for the grid line of 33 kV, which is used as a case study model. Table I shows the detailed specifications of the MMCC-SDBC. Each phase-cluster of the MMCC-SDBC has an output maximum 59.8 kV (= 23 converter cells × 2600 Vdc) by using the series connection of galvanic isolated H-bridge converter cells using Insulated Gate Bipolar Transistor (IGBT) modules which have a 4500 V rated voltage. It is noted that the required isolation voltage to ground of each converter cell becomes more than 59.8 kV in this specification. The widely used Phase-Shift Pulse Width Modulation (PS-PWM) is selected due to the advantage that the voltage and current stress among the 69 single-phase converter cells are equally distributed. This makes the converter cell design simpler. Due to the large converter cell counts, the switching frequency of each power semiconductor device is reduced to a low value of 225 Hz in this specification. Although this suppresses the switching loss

TABLE I
The Detailed Specification of the MMCC-SDBC.

Rated power Q_r	±80 MVar
Nominal grid voltage V_S	33 kVrms (±20%)
Nominal cell DC-side voltage V_{Cref}	2600 Vdc
Nominal cell AC-side voltage v_x	1450 Vrms
Equivalent switching frequency f_{eq_sw}	10.35 kHz
Rated line current I_r	1400 Arms
Carrier frequency f_c	225 Hz
Grid frequency f_g	50 Hz
Interconnection inductor L_{ac}	7.8 mH (%L=6%)
Dc-link capacitance each cell C_x	7.0 mF
Total cell counts N_{cell}	23×3
IGBT module	MBN900D45A (HITACHI)

of each power module, the impact of the PWM operation appears significantly on the dc-link capacitor voltage. The following section derives the formula of the dc-link capacitor voltage of each converter-cell in the MMCC-SDBC considering the PS-PWM operation. The dc-link capacitor voltage with both the original operation and the proposed operation using the voltage ripple reduction method are compared.

A. The original capacitor voltage

Fig. 2 shows with a solid line the conventional operation waveforms of the u1-cell converter (see Fig. 1) as an example. When the MMCC-SDBC is in steady state and each dc-link capacitor voltage is balanced, the output voltage reference of each cell in the u-phase cluster e_{m_u} is given by

$$e_{m\_u} = M_a \sin \omega_m t + e_{m\_z} \quad (1)$$

$$M_a \equiv \frac{\sqrt{2}(V_S \pm \omega_m L_{ac} I/\sqrt{3})}{(N_{cell}/3)V_{Cref}} \quad (2)$$

with the modulation factor: M_a, the grid frequency: ω_m, each cell output voltage of the zero-sequence component: e_{m_z}, the nominal grid voltage: V_S, the inductance of each

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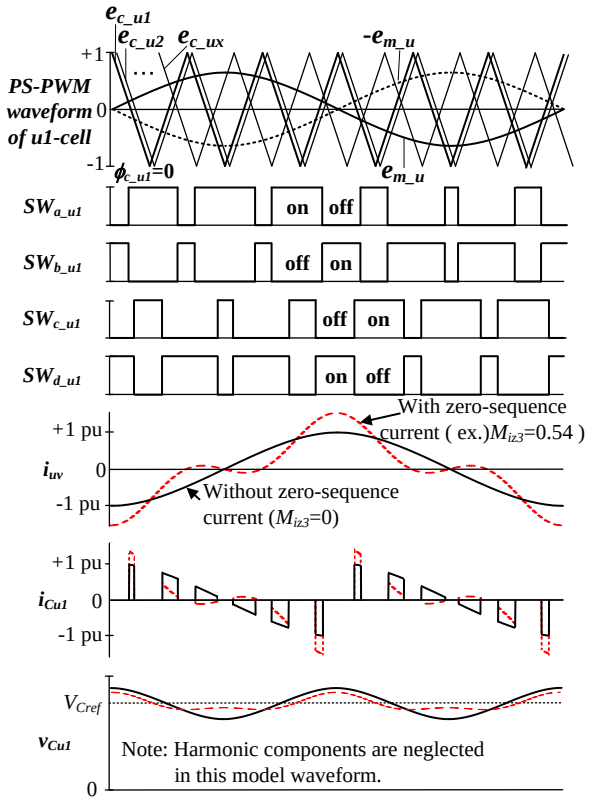


Fig. 2. PS-PWM waveforms and current in the u1-cell.

phase-cluster AC inductor: L_{ac}, the phase current at the PCC: I, the total cell number: N_{cell}, the dc-link voltage reference of each cell converter: V_{Cref}. The e_{m_z} has zero value in this condition. It is noted that the polarity of the voltage drop of the AC inductor depends on a leading/lagging of the STATCOM output current.

The e_{c_u1} is the carrier signal of the u1-cell converter. The phase delay of the e_{c_u1} from the e_{m_u}, which has a zero value in Fig. 2. Because of the PS-PWM, the phase delay ϕ_{c_ux} of the other cell converters in the u-phase cluster is given by

$$\phi_{c\_ux}\big|_{x=2,\ldots,N_{cell}/3} = \phi_{c\_u1} + \frac{x-1}{N_{cell}/3}\frac{1}{\omega_c} \qquad (3)$$

with the number of the optional cell in the u-phase cluster: x, the carrier frequency ω_c [rad/s] of the PS-PWM.

The switching functions SW_{a_ux}, SW_{b_ux}, SW_{c_ux}, and SW_{d_ux} show the on/off states of the power semiconductor switches S_{a_ux}, S_{b_ux}, S_{c_ux}, and S_{d_ux}, respectively, which is determined by the PS-PWM of the e_{m_u} and the e_{c_ux} by neglecting the dead time duration. SW_{a_ux}, SW_{b_ux}, SW_{c_ux}, and SW_{d_ux} are expressed as a Fourier series expansion in the following:

$$SW_{a\_ux} = \frac{1}{2}(1+e_{m\_u}) + \sum_{n=1}^{m}\left[\frac{2}{n\pi}\sin\left\{\frac{n\pi}{2}(e_{m\_u}-1)\right\}\cos(n\omega_c t - n\phi_{c\_ux})\right] \qquad (4)$$

$$SW_{b\_ux} = 1 - SW_{b\_ux} \qquad (5)$$

$$SW_{c\_ux} = \frac{1}{2}(1-e_{m\_u}) + \sum_{n=1}^{m}\left[\frac{2}{n\pi}\sin\left\{\frac{n\pi}{2}(-e_{m\_u}-1)\right\}\cos(n\omega_c t - n\phi_{c\_ux})\right] \qquad (6)$$

$$SW_{d\_ux} = 1 - SW_{c\_ux} \qquad (7)$$

The u1-cell output current, as well as the u-phase cluster current i_{uv}, is defined as

$$i_{uv} = \sqrt{\frac{2}{3}} I \sin(\omega_m t + \phi_{pf}) + i_{zero} \qquad (8)$$

where ϕ_{pf} is the power factor of the MMCC-SDBC, i_{zero} is the zero-sequence current. It is noted that the zero-sequence current i_{zero} is controlled to zero value where all capacitor voltages are balanced.

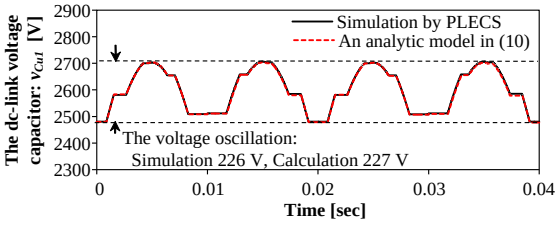
The dc-link capacitor current i_{Cux} of each u-phase converter cell is given by using the switching functions as follows:

$$i_{Cux} = -i_{uv}(SW_{a\_ux} - SW_{c\_ux}) \qquad (9)$$

By integrating (9), the dc-link capacitor voltage v_{cu1} of each u-phase converter cell is expressed by (10) with the initial value of v_{cu1}: V_{Cu1_ini}.

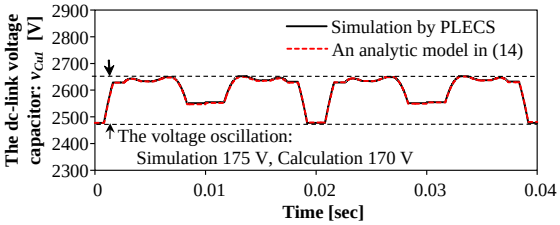
$$v_{Cux} = -\frac{1}{C}\int i_{Cux}dt + V_{Cux\_ini} \qquad (10)$$

Fig. 3(a) plots the dc-link capacitor voltage v_{Cu1} of the u1 cell converter based on the analytic model in (10) and the simulation under the rated operation given in Table I. The simulation waveform is obtained by using the PLECS software on the practical scale model based on the specification of Table I. The ϕ_{C_u1} and V_{Cu1_ini} in the analytic model is set at - 3.11 rad and 2480 V, respectively, which values are adjusted to the simulation values. The analytic model corresponds reasonably well with the simulation result.



Note: M_a = 0.827 p.u., M_{a3} = 0 p.u. ϕ_{C_u1} = -3.11 rad, V_{c_ini} = 2480 V

(a) Conventional operation as the M_{iz3} = 0 p.u.



Note: M_a = 0.827, M_{a3} = 0.0702 p.u. ϕ_{C_u1} = -3.11 rad, V_{c_ini} = 2477 V

(b) Proposed operation with M_{iz3} = 0.5 p.u and $\phi_{iz3} = \phi_{pf}$

Fig. 3. The u1-cell capacitor voltage waveforms.

B. *The proposed capacitor voltage ripple reduction method*

Fig. 2 shows with a dotted line the proposed operation waveforms of the u1-cell converter. The i_{zero} is normally controlled at zero value where all capacitor voltages are balanced. However, it is possible to output an optional value. A third harmonic zero-sequence current, which has the same angle and amplitude among the three-phase clusters is to reduce the dc-link capacitor voltage ripple and it is considered in the next part.

The i_{zero} is defined as

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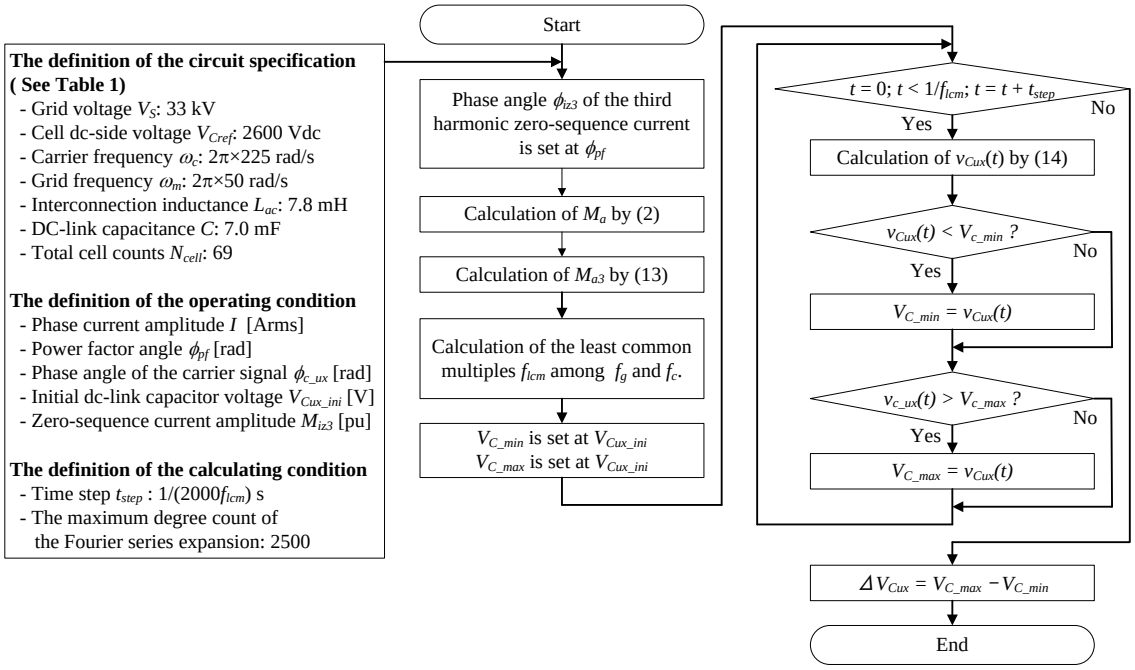

Fig. 4. The numerical calculation flow for the dc-link capacitor voltage ripple stage.

$$i_{zero} = \sqrt{\frac{2}{3}} M_{iz3} I \sin(3\omega_m t + \phi_{iz3}) \qquad (11)$$

where M_{iz3} is the amplitude ratio of i_{zero} at the I, ϕ_{iz3} is the phase difference from e_{m_u}.

In order to inject i_{zero}, each cell converter requires an additional output voltage. The additional output-voltage reference e_{m_z} is given by

$$e_{m\_z} = M_{a3} \sin\left(3\omega_m t + \frac{\pi}{2} + \phi_{iz3}\right) \qquad (12)$$

$$M_{a3} = \frac{\sqrt{6}\omega_m L_{ac} I M_{iz3}}{(N_{cell}/3) V_{Cref}} \qquad (13)$$

The switching functions SW_{a_ux}, SW_{b_ux}, SW_{c_ux} and SW_{c_ux} under the proposed dc-link capacitor voltage ripple reduction operation can be obtained by substituting (1), (2), (12) and (13) for (4), (5), (6) and (7).

The dc-link capacitor current i_{Cux} of each u-phase converter cell under the proposed dc-link capacitor voltage ripple reduction operation can be obtained by substituting the above-mentioned switching functions, (8) and (11) for (9).

The dc-link capacitor voltage v_{Cux} of each u-phase converter cell under the proposed dc-link capacitor voltage ripple reduction operation can be expressed by (14), by substituting the above-mentioned dc-link capacitor current i_{Cux} for (10).

Fig. 3(b) shows the dc-link capacitor voltage v_{Cu1} of the u1 converter cell based on the analytic model (14) and the simulations. In these results, 50% of the third harmonic zero-sequence current is injected with M_{iz3} = 0.5, ϕ_{iz3} = ϕ_{pf}, ϕ_{C_u1} = - 3.11 rad, V_{Cu1_ini} = 2477 V as an example. The simulation waveform is also obtained using PLECS software on the practical scale model based on the specifications in Table I. The analytic waveform corresponds well with the simulation waveforms. The proposed method reduces the capacitor voltage ripple by 23% compared with the original voltage ripple.

C. *The optimum phase angle ϕ_{iz3} of the third harmonic zero sequence current*

Equation (14) reveals that the dc-link capacitor voltage ripple consists of the following three components.

- ✓ The first component is some terms in (14), which are pulled out by the modulation factor M_a of the grid frequency. This becomes the main component of the dc-link capacitor voltage.
- ✓ The second component comes from some terms in (14), which are due to the modulation factor M_{a3} of the third harmonic voltage in order to inject the third harmonic zero-sequence current.

$$v_{Cux} = -\sqrt{\frac{2}{3}}\frac{M_a}{4\omega_m C}\left\{I\sin(2\omega_m t + \phi_{pf}) - M_{iz3} I \sin(2\omega_m t + \phi_{iz3}) + \frac{M_{iz3} I}{2}\sin(4\omega_m t + \phi_{iz3})\right\}$$
$$+\sqrt{\frac{2}{3}}\frac{M_{a3}}{4\omega_m C}\left\{I\sin\left(2\omega_m t - \phi_{iz3} + \frac{\pi}{2} - \phi_{pf}\right) - \frac{I}{2}\sin\left(4\omega_m t - \phi_{iz3} + \frac{\pi}{2} + \phi_{pf}\right) - \frac{M_{iz3} I}{3}\cos\left(6\omega_m t + \frac{\pi}{2}\right)\right\}$$
$$+\sqrt{\frac{2}{3}}\frac{I}{C}\int\left\{\sin(\omega_m t + \phi_{pf}) + M_{iz3}\sin(3\omega_m t + \phi_{iz3})\right\}\sum_{n=1}^{\infty}\frac{4}{n\pi}\cos\left(\frac{n\pi}{2}\right)\sin\left[\frac{n\pi}{2}\left\{M_a\sin\omega_m t + M_{a3}\sin\left(3\omega_m t - \phi_{iz3} + \frac{\pi}{2}\right)\right\}\right]$$
$$\cos(n\omega_c t - n\phi_{c\_ux})dt + V_{Cux\_ini} \qquad (14)$$

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- ✓ The third component is the remaining terms in (14). Those terms are due to the PS-PWM.

The first component dominates the dc-link capacitor voltage ripple. For the sake of simplicity, the first component is in focus. When the amplitude M_{iz3} of the third harmonic zero-sequence current is zero, only the double frequency voltage ripple is remaining, which is the original capacitor voltage ripple component. When the M_{iz3} and the phase angle ϕ_{iz3} of the third harmonic zero-sequence current are set to 1 p.u. and ϕ_{pf}, the original capacitor voltage ripple component can be eliminated perfectly. This is the effect of the proposed capacitor voltage ripple reduction method. It is obvious, due to the optimum ϕ_{iz3} to obtain the maximum voltage ripple reduction effect, the capacitor voltage ripple should be set to be the same as the power factor angle ϕ_{pf}.

III. The Numerical Analysis of the DC-Link Capacitor Voltage Ripple

Fig. 4 shows the numeric calculation flow of the dc-link capacitor voltage ripple ΔV_{Cux} of each u-phase converter cell based on (14). The first process of this numeric calculation is the definition of the circuit specifications, the operating conditions, and the numeric calculation parameters. Next step is the definition of the phase angle ϕ_{iz3} of the third harmonic zero-sequence current, which is set at ϕ_{pu}, and is the optimum value to minimize the capacitor voltage ripple as described in Section II-C. Then, the numeric calculation period of $v_{Cux}(t)$ is calculated, which becomes the least common multiples f_{lcm} among f_g and f_c because the v_{Cux} is the periodic function repeated over intervals of $1/f_{lcm}$. Finally, the capacitor voltage ripple ΔV_{Cux} during the period $1/f_{lcm}$ is calculated, which becomes the differential value between the maximum value V_{C_max} and the minimum value V_{C_min} of $v_{Cu1}(t)$ for the period $1/f_{lcm}$. The following section analyzes the capacitor voltage ripple with respect to the PS-PWM condition, reactive current and grid voltage by using the numeric calculation method shown in Fig. 4.

A. *The impact of the PS-PWM to the capacitor voltage ripple ΔV_{Cux} of a u-phase cluster cell converter*

Fig. 5 shows the dc-link capacitor voltage ripple ΔV_{Cux} of the u-phase converter cells regarding the amplitude M_{iz3} of the third harmonic zero-sequence current. The STATCOM operating condition is set to be leading with full load output (I = 1400 Arms, ϕ_{pf} = π/2 rad) and the rated grid voltage (V_S = 33 kVrms). The following describes each of the plots.

- ✓ The dotted line plots show of the capacitor voltage ripple ΔV_{Cu1} of u1-cell converter. The phase angle ϕ_{c_u1} of the carrier signal is set to be -3.11 rad as an example, which value is the same as the analytic condition of Fig. 3 (b).
- ✓ The shadow area shows a range of values on the capacitor voltage ripple ΔV_{Cux} of each of the u-phase converter cell can take in respect to the ϕ_{c_ux}. The ϕ_{c_ux} has the values in the range [-π, π] depending on the converter cell. It is obvious that the ΔV_{Cux} has a significantly different value with respect to the ϕ_{c_ux}, which should be taken account when doing the capacitor design.
- ✓ The lowest solid line plots show the capacitor voltage ripple, but this calculation is excluding the term related to the PS-PWM in the analytic model (14). Obviously, if the impact of the PS-PWM is excluded from the calculation, the capacitor voltage has a large difference. So, the impact of the harmonics coming from the PS-PWM should be considered, when the capacitor is designed.

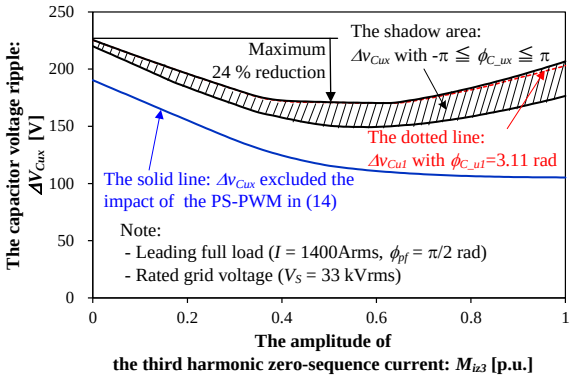

Fig. 5. The dc-link capacitor voltage ripple solved by the numeric calculation in Fig. 4.

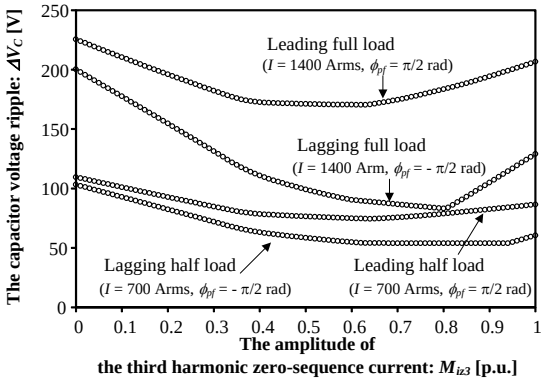

Fig. 6 The capacitor voltage ripple in respect to the amplitude ratio M_{iz3}, with different value of the reactive current.

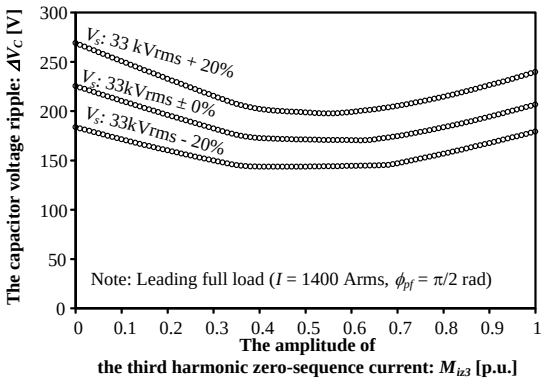

Fig. 7. The capacitor voltage ripple in respect to the amplitude ratio M_{iz3}, with different value of grid voltage.

In the following, the capacitor voltage ripple is defined as the maximum value ΔV_C with respect to the phase angle ϕ_{c_ux} of the carrier signal and modulation waveform

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between – π to + π.

B. *The capacitor voltage ripple ΔV_C with respect to the reactive current output*

Fig. 6 shows the plot of the capacitor voltage ripple ΔV_C regarding the M_{iz3} [pu], with different values of the reactive output current. It is obvious that the capacitor voltage ripple has a maximum at the leading full load point. The effective parameters of M_{iz3} to reduce the capacitor voltage ripple stay constant at around 0.5 regarding the different values of the reactive output current. When the M_{iz3} is larger than 0.5, the capacitor voltage ripple increases depending on the reactive current condition.

C. *The capacitor voltage ripple ΔV_C with respect to the grid voltage*

Fig.7 shows the plot of the capacitor voltage ripple in respect to the M_{iz3} [pu] with different amplitudes of the grid voltage V_S [pu] within the specification as shown in Table I, under leading full load condition. It is noted that the capacitor voltage ripple decreases relative to V_S. It is obvious that the effective parameters of M_{iz3} to reduce the voltage ripple stays constant at around 0.5 independent of the V_S.

IV. Electrical and Thermal Stress of the Power Modules

The proposed method can reduce the dc-link capacitor voltage ripple of the MMCC-SDBC by the injection of third harmonic zero-sequence current. However, it may increase the power semiconductor losses, peak junction temperature and peak current by using the third harmonic current. This paragraph analyzes the electrical and thermal stress of the power modules used in the practical 80 MVar / 33 kV scaled STATCOM based on the MMCC-SDBC using the proposed method.

A. *Electrical and thermal simulation model*

The electrical and thermal stress of the power modules in the MMCC-SDBC in respect to the M_{iz3} are simulated by using the simulation software PLECS. The specifications of the MMCC - SDBC are shown in Fig. 1 and Table I. The reactive current reference is set to be rated 1 p.u. The grid voltage is also set to be the rated 33 kV.

Fig. 8 depicts the overall control block diagram of the MMCC-SDBC with the proposed capacitor voltage ripple reduction method by using third harmonic zero-sequence current. The output current and the capacitor voltage control method are applied [16]. The third harmonic zero-sequence current given in (11) is added to the reference value of the zero-sequence current. The phase angle ϕ_{iz3} of the third harmonic zero-sequence current is set to be ϕ_{pf}. The amplitude M_{iz3} of the third harmonic zero-sequence current is normalized by the output current I and is set to have a value in the range between 0 and 1.

The power loss of each power module is simulated by the active component block function in the PLECS

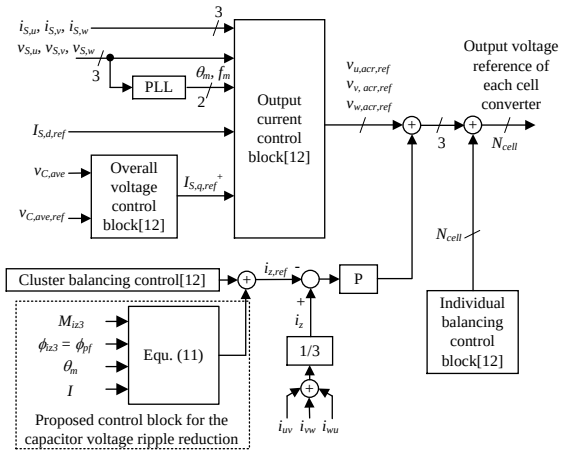

Fig. 8. The overall control block diagram for the MMCC-SDBC with the proposed capacitor voltage ripple reduction method.

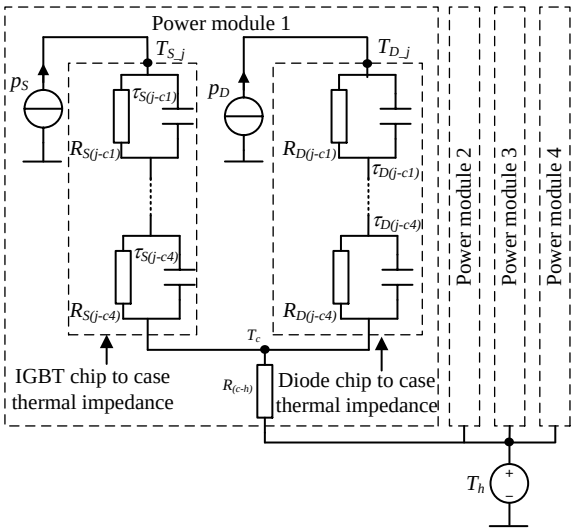

Fig. 9. The thermal network of each converter cell of the SDBC.

software. The on-state voltage $V_{ce}(I_c, T_{S\_j})$ of the IGBT side is set to be a line (15) in respect to the junction temperature T_{S_j} of the IGBT and the collector current I_C.

$$V_{ce}(I_c, T_{S\_j}) = V_{ce,25C^\circ}(I_c) + \frac{T_{S\_j}-25}{100}\{V_{ce,125C^\circ}(I_c) - V_{ce,25C^\circ}(I_c)\} \quad (15)$$

Here, $V_{ce,25°C}(I_c)$ and $V_{ce,125°C}(I_c)$ are the on state voltage at the junction temperature T_{S_j} = 25°C, 125°C, respectively, in response to the collector current I_c. This information is obtained from the datasheets of the manufacturers [17]. The on-state voltage $V_f(I_f, T_{D\_j})$ of the Free Wheeling Diode (FWD) side is set to be (16) in respect to the junction temperature T_{D_j} of the FWD and the forward current I_C of the FWD.

$$V_f(I_f, T_{D\_j}) = V_{f,25C^\circ}(I_f) + \frac{T_{D\_j}-25}{100}\{V_{f,125C^\circ}(I_f) - V_{f,25C^\circ}(I_f)\} \quad (16)$$

Here, $V_{f,25°C}(I_f)$ and $V_{f,125°C}(I_f)$ are the on state voltage at the junction temperature T_{D_j} = 25°C, 125°C, respectively, as a function of the I_c, which information is obtained from the datasheets of the manufacture [17]. The turn on energy loss $E_{on}(I_C, v_c)$, turn off loss $E_{off}(I_C, v_c)$ and reverse recovery loss $E_{rr}(I_f, v_c)$ of the power module at every

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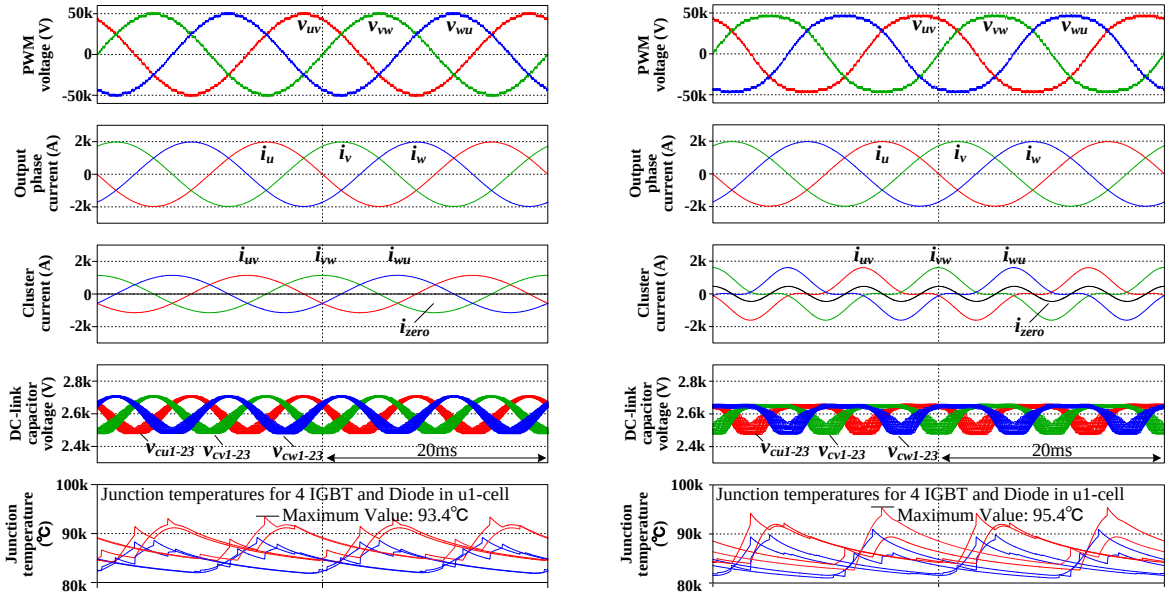

(a) The conventional operation (M_{iz3} = 0) (b) The proposed operation (M_{iz3} = 0.4)

Fig. 10. Key simulation waveforms of the MMCC-SDBC including thermal loading.

switching behavior are set to be calculated line in (17), (18) and (19), respectively, which are dependent on the current flow and the applied voltage v_c at the switching operation .

$$E_{on}(I_c, v_c) = \frac{v_c}{2600} E_{on,2600V}(I_c) \quad (17)$$

$$E_{off}(I_c, v_c) = \frac{v_c}{2600} E_{off,2600V}(I_c) \quad (18)$$

$$E_{rr}(I_f, v_c) = \frac{v_c}{2600} E_{rr,2600V}(I_f) \quad (19)$$

Here, $E_{on,2600V}(I_c,v_c)$, $E_{off,2600V}(I_c,v_c)$ and $E_{rr,2600V}(I_f,v_c)$ are the turn-on energy loss, turn off energy loss and reverse recovery energy loss at v_c = 2600V at every switching operation in response to the current flow, which information is obtained by the datasheet from the manufacturers [17].

The junction temperature of each power module is simulated by the thermal simulation function in the PLECS software. The thermal impedance between junction and heatsink is based on the Foster RC network which is shown in Fig. 9, and they are selected from the datasheets for the power modules [17]. Here, p_S is the power loss of the IGBT; p_D is the power loss of the FWD; T_{S_j} is the junction temperature of the IGBT; T_{D_j} is the junction temperature of the FWD; T_c is the case temperature in the power module; T_h is the heat sink temperature; $R_S(j\text{-}cn)$, $\tau_S(j\text{-}cn)$, $R_D(j\text{-}cn)$ and $\tau_D(j\text{-}cn)$ are thermal parameters for the Foster RC network of the power module (n:1-4). The limitation temperature is set to be 106°C determined by the absolute maximum value of 125°C provided by the manufacturer. A design margin of 0.85 is considered in this paper. As the temperature of the heatsink is normally much lower and more stable compared with the junction temperature in a properly designed converter system, the heat sink temperature is considered as a constant value of 60°C in this paper.

B. *Electrical and thermal waveforms*

Fig. 10 shows the electrical and thermal simulation waveforms with M_{iz3} = 0 (the conventional operation) and M_{iz3} = 0.4 as an example (the proposed operation). These waveforms show no evidence of abnormalities. The total harmonic distortion of the output phase current with M_{iz3} = 0 and M_{iz3} = 0.4 operations are almost the same, which

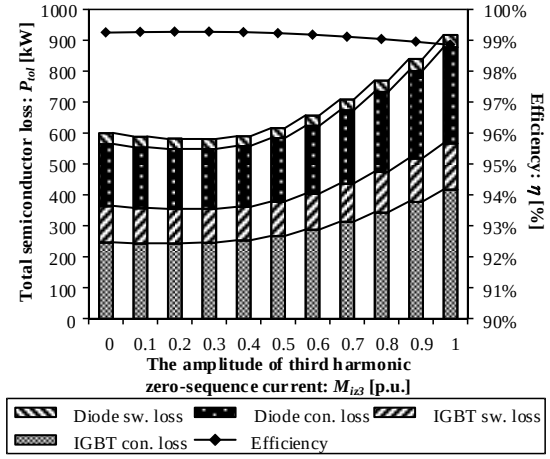

Fig. 11. The total semiconductor loss of the MMCC-SDBC.

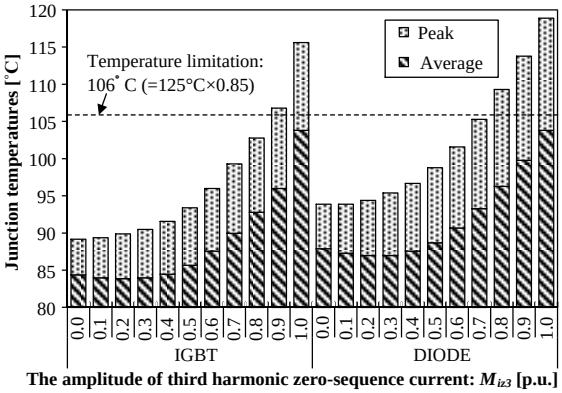

Fig. 12. The junction temperature of an IGBT and Diode switch selected as the maximum of switches of the MMCC-SDBC.

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are 0.35% and 0.4%, respectively. The peak modulation factors of each converter cell with M_{iz3} = 0 and 0.4 are 0.80 pu and 0.76 pu, respectively. The peak phase-cluster current for the proposed case increases by 40 % (1600 A) by the injection of the third harmonic zero-sequence current. This value is still lower than the allowable peak current value of 1800 A of the used power modules as mentioned in Table I. The peak junction temperature of the power module increases 2 Kelvin, which values are below the upper limit temperature of 106°C. The capacitor voltage ripple for the proposed case will decrease by 20 % in this operating condition.

C. *Power semiconductor losses and junction temperatures*

Fig. 11 shows the total semiconductor losses and electrical efficiency of the MMCC-SDBC with respect to the M_{iz3}. It is noted that the total semiconductor losses increase when M_{iz3} is above 0.3 p.u. because the r.m.s. value of each cluster current increases. However, the total semiconductor losses are slightly reduced when M_{iz3} is below 0.3 because of the V_{ce} - I_c characteristics of the used bipolar devices.

Fig. 12 shows the instant peak and average junction temperature of the IGBT and FWD having maximum thermal stress among the 276 modules with respect to M_{iz3}. It is noted that the average junction temperature exhibits similar trends as the total losses. On the other hand, the peak junction temperature increases as a function of the M_{iz3} because the peak value of the phase-cluster current increases due to the M_{iz3}. It is noted that the third harmonic zero-sequence current has not exceeded above 0.7 of M_{iz3}, because of the limitation of the peak junction temperature in this case.

D. *Peak current stress of the power modules*

Fig. 13 shows with solid line the peak phase-cluster current i_{peak} as a function of M_{iz3} under full load condition, which can be calculated by

$$i_{peak} = \sqrt{\frac{2}{3}} I_r (1 + M_{iz3}) \qquad (20)$$

where I_r is the rated phase current as mentioned in Table I. It should be noted that the amplitude M_{iz3} of the injection of the third harmonic zero-sequence current should not exceed above 0.55 p.u. due to the peak current limitation of the used power module.

E. *The optimum amplitude of the third harmonic zero-sequence current M_{iz3}*

Fig. 14 shows the total semiconductor losses and the capacitor voltage ripple regarding the M_{iz3}. The total semiconductor losses and the capacitor voltage ripple are normalized by each value at M_{iz3} = 0. The optimum value of M_{iz3} is selected to be 0.4 p.u. where the capacitor voltage ripple could be reduced to a minimum without any total power semiconductor loss increase compared with the conventional method (M_{iz3} = 0).

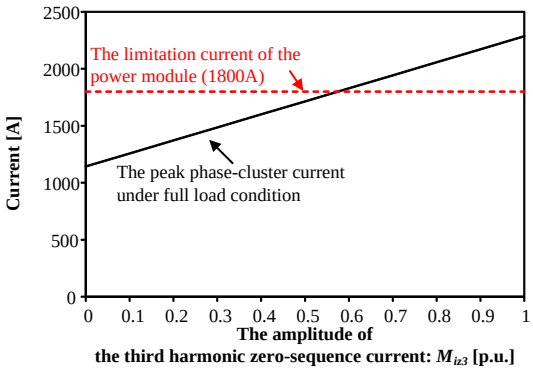

Fig. 13. The peak phase-cluster current as a function of M_{iz3}.

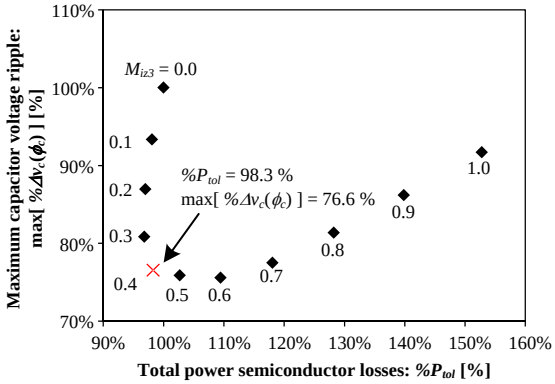

Fig. 14. The total semiconductor loss and the capacitor voltage ripple as a function of M_{iz3}.

V. CAPACITOR BANK DESIGN

The final purpose of the proposed capacitor voltage ripple reduction method is to reduce the entire capacitor bank size. Surely, the required capacitance is reduced by applying the proposed method, but the equivalent series resistance of the capacitor bank will be increased. Therefore, the core temperature of capacitor bank as well as the expected lifetime of the capacitor bank may get worse, which may influence the reduction of the capacitor bank volume [18], [19]. In order to clarify the capacitor bank size reduction effect of the proposed method, the capacitor bank is designed in this section.

A. *Capacitor bank structure*

Table II shows the target specification of the capacitor bank for the MMCC-SDBC having the specification given in Table I. The type of the dc-link capacitor is selected to be metalized polypropylene film capacitor (MPPF-Cap), which is commonly chosen for the medium and high voltage class MMCC solutions because of a high reliability [20], [21]. The capacitance of the dc-link capacitor bank with the conventional operation and the proposed method are set to be 7 mF and 5.4 mF, respectively, where the capacitor voltage ripples are suppressed to be less than 10%.

Fig. 15 shows the dc-link capacitor bank structure. In the actual STATCOM product case, the dc-link capacitor bank typically becomes one capacitor, which is custom made product provided by a capacitor manufacturer. In

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TABLE II
THE TARGET SPECIFICATION OF THE CAPACITOR BANK.

	Conventional method	Proposed method
Capacitor type	Metallized polypropylene film capacitor	
Rated dc voltage	2600 Vdc	
Capacitance	7 mF or more	5.4 mF or more
Expected life time	20 years or more	
Ambient temperature	60 ℃	

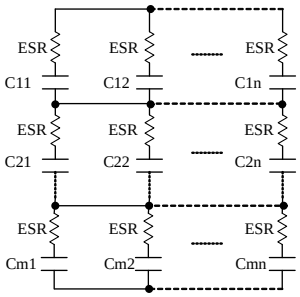


Fig. 15. Capacitor bank structure.

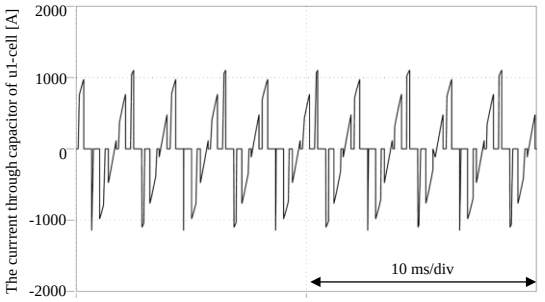
TABLE III
CAPACITOR BANK SPECIFICATION.

	Conventional case	Proposed case
Used capacitor	560 μF, 1300 Vdc, 85 ℃, Type 947C Polypropylene Film DC-Link Capacitors from Cornell Dubilier	
Series connection count: m	2	2
Parallel connection counts: n	25	20
Total count: $m \times n$	50	40
Total capacitance	7.00 mF	5.60 mF
Rated voltage	2600 Vdc	
Total capacitor volume	87.2 L	69.8 L

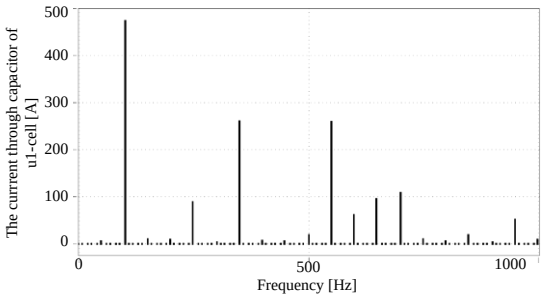
this paper, the capacitor bank is constructed by series and parallel connection of small capacitor elements. It should be noted that the total volume of the dc-link capacitor bank constructed by smaller capacitor elements becomes similar to the custom made product because of the same total energy stored in the capacitor. Table III shows the capacitor bank specification for both the conventional and the proposed case. The capacitor bank is selected to use 560 μF, 1300 Vdc, Type 947C MPPF-Cap. from Cornell Dubilier [22]. In order to overcome the applied dc voltage to the capacitor bank, the series connection number is designed to be 2 for both cases. In order to provide the capacitor bank with the required capacitance, the parallel counts of the conventional and the proposed case are designed to be 25 and 20, respectively. The total volumes of each dc-link capacitor bank for the conventional and proposed case are 87.2 L and 69.8 L, respectively. The capacitor bank volume is reduced by 20% by applying the proposed method.

B. The thermal stress of each MPPF-Cap

The hot spot temperatures of the dc-link capacitors under the conventional and proposed condition are calculated, which have to be kept below the rated temperature determined by the manufacturer. Fig. 16 and

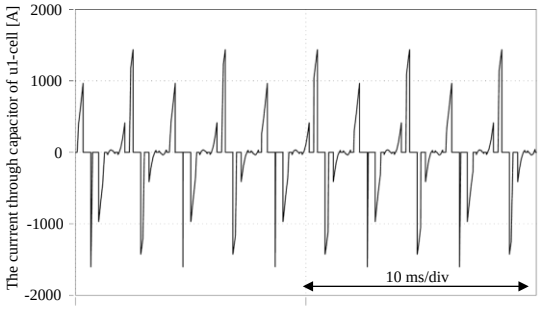


(a) Current waveform through the capacitor bank (473 Arms)

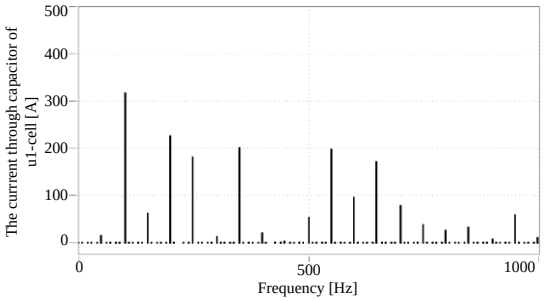


(b) FFT analysis

Fig. 16. The current through the capacitor bank under conventional condition.



(a) Current waveform through the capacitor bank (426 Arms)



(b) FFT analysis

Fig. 17.The current through the capacitor bank using the proposed method.

Fig. 17 show the current waveforms through the dc-link capacitor bank of the u-1 cell and an FFT analysis with or without the proposed method. The simulation conditions are the same as shown in Fig. 10. By applying the proposed method, the main current ripple component as

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the double fundamental frequency is reduced by 33% and distributed to higher frequency components. The r.m.s. values of the current through the capacitor bank in the conventional and proposed case are 473 Arms and 426 Arms, respectively.

In order to simplify the calculations, it is assumed that the current through each individual capacitor in the capacitor bank is balanced. The power loss of each capacitor is given by

$$P_{loss} = \sum_f ESR(f) \cdot I_C^2(f) \quad (21)$$

where $ESR(f)$ is the Equivalent Series Resistance of the capacitor according to the frequency f, I_C is the r.m.s. current through each capacitor in respect to f. The core temperature of the capacitor is given by

$$T_C = T_a + P_{Loss} \cdot R_{th} \quad (22)$$

where T_a is the ambient temperature around the capacitor, and R_{th} is the thermal resistance of the capacitor.

Table IV shows the P_{loss} and T_c of the individual capacitors for the conventional and proposed case. The power loss and hot spot temperature of the proposed capacitor case become slightly higher than in the conventional case in order to reduce a parallel number of capacitors. However, because the ESR of the film capacitors has enough small value, the core temperatures of the used capacitor for both cases become lower than its absolute temperature of 85 °C.

C. The expected lifetime of the capacitor bank

Generally, MPPF-Caps have very long lifetime under adequate operating conditions including the applied dc-voltage, the core temperature of the capacitor and the humidity when comparing with Aluminum Electrolytic Capacitors, which have wear out failure modes. For such kind of components, it is important to estimate the reliability by using its lifetime model. In this paper, the lifetime of the capacitor bank under the conventional and the proposed case is estimated by using the provided information from the capacitor manufacturer.

A widely used capacitor lifetime model applicable for film capacitor is as follows [23]:

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-n} \times 2^{\frac{T_0 - T}{k}} \quad (23)$$

where L is the lifetime under the thermal and electrical stress T and V, L_o is the lifetime under the reference temperature T_0 and the nominal voltage V_0. The coefficients k and n are a temperature dependent constant and voltage stress constant. The parameters L_0, T_0, n, and k for the used capacitor are obtained from a provided lifetime curve which are fitted to be 200000, 66 °C, 19.4, and 3.9, respectively.

Actually, there is a probability on a lifetime of individual capacitors, which also is considered [24]. It is assumed that a variation of the lifetime obeys the normal distribution. The cumulative distribution function (CDF) for the normal distribution can be calculated by

$$F(t) = \frac{1}{2}\left\{1 + \mathrm{erf}\left(\frac{t-\mu}{\sigma\sqrt{2}}\right)\right\} \quad (24)$$

where μ is the mean of the distribution, σ is the standard deviation, erf is the error function. The μ is determined by the expected lifetime calculated by (12). The σ is determined by considering±10% variation with a 95% confidence interval (CI).

TABLE IV
POWER LOSS AND HOT SPOT TEMPERATURE OF EACH CAPACITOR.

	Conventional case	Proposed case
Power loss	1.11 W	1.36 W
Hot spot temperature	63.3 °C	64.1 °C

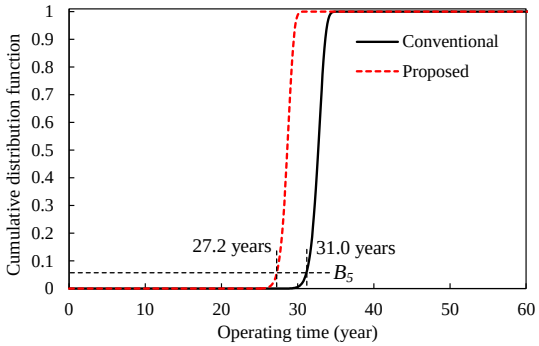

Fig. 18. Probability curves of wear-out failure for the capacitor banks.

It is assumed that all the considered devices are connected in series in the reliability model, i.e., any capacitor in the capacitor bank failure will lead to system failure. Then the capacitor bank wear-out failure $F_{CB}(t)$ can be calculated by

$$F_{CB}(t) = 1 - \prod(1 - F_i(t)) \quad (25)$$

where $F_i(t)$ is the CDF for each individual capacitor which is constructing the capacitor bank.

Fig. 18 shows the probability curves of wear-out failures of the capacitor bank for the conventional and the proposed case. It is noted that the lifetime B_5 means that 5% of the total amount of capacitor bank fails both for the conventional and for the proposed case, which are 31.0 years and 27.2 years, respectively. The proposed case is slightly worse than the conventional case, because of the slightly higher capacitor temperature due to reduced capacitor count. However, the B_5 lifetimes for both cases have enough high value for satisfying the target, which is expected to be longer than 20 years, as also specified in Table II.

VI. CONCLUSIONS

This paper proposes a method to reduce the dc-link capacitor voltage ripple for use in one power converter type of the MMCC family with Single Delta Bridge Cells (SDBC) under STATCOM operation by injecting the third harmonic zero-sequence current i_{zero}. The capacitor voltage formula is considering the injection of i_{zero} and applying the widely used Phase Shift PWM. The impact of the i_{zero} to the capacitor voltage ripple for different values of the output current and grid voltage condition is analyzed based on the method derived. The electrical and thermal stress of the power module is simulated on the practical-scaled MMCC-SDBC model having 80 MVar / 33 kV specifications. The proposed method can reduce

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the capacitor voltage ripple by maximally 23 % without increasing the total power semiconductor losses and the junction temperature limitation by the injection of the i_{zero} at a current amplitude M_{iz3} = 0.4 p.u. and a phase angle ϕ_{iz3} = power factor angle. The capacitor bank is designed considering the capacitor voltage ripple, electrical and thermal stress. The obtained results show that the proposed method can reduce the capacitor bank volume by 20 %.

It is noted that, the converter peak current increases proportionally to the M_{iz3}. Therefore, the allowable amplitude M_{iz3} may be reduced at the practical product design stage, considering each product design requirement, such as overcurrent level of gate block function and peak surge voltage at turn-off operation of power semiconductor devices.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIA.2019.2934024, IEEE Transactions on Industry Applications

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