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Current Limiting Control with Enhanced Dynamics of Grid-Forming Converters during Fault Conditions

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***Abstract*—With an increasing capacity in converter-based generation to the modern power system, a growing demand for such systems to be more grid-friendly has emerged. Consequently, grid-forming converters have been proposed as a promising solution as they are compatible with the conventional synchronous-machine-based power system. However, most research focuses on the grid-forming control during normal operating conditions without considering the fundamental distinction between a grid-forming converter and a synchronous machine when considering its short-circuit capability. Current limitation of grid-forming converters during fault conditions is not well described in the available literature and present solutions often aim to switch the control structure to a grid-following structure during the fault. Yet, for a future converter-based power system with no or little integration of synchronous machines, the converters need to preserve their voltage-mode characteristics and be robust towards weak-grid conditions. To address this issue, this paper discusses the fundamental issue of grid-forming converter control during grid fault conditions and proposes a fault-mode controller which keeps the voltage-mode characteristics of the grid-forming structure while simultaneously limiting the converter currents to an admissible value. The proposed method is evaluated in a detailed simulation model and verified through an experimental test setup.**

***Index Terms*—Grid-Connection, Voltage-Source Converter, Grid-Forming Control, Fault Ride-Through, Current limitation**

I. Introduction

A critical issue of the power system transitioning towards renewable energy sources is the gradual retirement of the bulk generation supplied by large synchronous machines. Conventional power systems dominated by synchronous machines both facilitate synchronizing torque, damping, and high system inertia which act as the primary ancillary support to the network during disturbances. To that end, during grid fault conditions, synchronous machines are capable of a large short-circuit current injection up to 6-8 pu [1, p. 319-345]. With a growing capacity of converter-based generation to the power system, concern is directed towards the overall stability of the system as power electronics-based generators neither provide inertia and synchronizing torque, nor are they capable of providing short-circuit currents much higher than their rated current. Usually, grid-tied converters are controlled as grid-following converters where a voltage-based synchronization unit, often a Synchronous-Reference Frame Phase-Locked Loop (SRF-PLL), is used to align the current reference of the vector current control [2].

However, as the scheme is largely dependent on the assumption of a stiff voltage at the point of connection, this synchronization unit is shown to cause low-frequency oscillations and loss of synchronization during weak-grid and grid fault conditions [3]–[5]. Furthermore, with a trend for connecting generation at all voltage levels and with a future possibility for islanded operation of different parts of the network as a result of a system split, this is not possible with grid-following converters as there do not exist a dedicated voltage to act in accordance with. This is a fundamental limitation for grid-following PLL-synchronized converters since they simply follow the external environment. As a result of this, a growing interest has emerged in the research of grid-forming converters to address this issue by emulating the dynamics and beneficial functionalities of synchronous machines including provision of synthetic inertia and a power-based synchronization mechanism.

Among the grid-forming converters, numerous control schemes exist: *droop control* [6], [7], *Virtual Synchronous Machine* (VISMA/VSM) [8], [9], synchronverter [10]–[12], *Power Synchronization Control* (PSC) [13], [14] and *Synchronous Power Controller* (SPC) [15], [16]. As the control schemes just mentioned do not necessarily specify a voltage magnitude and frequency set-point but modify these based on measurements from the local connection point, these converters may also be referred to as grid-supporting grid-forming converters [17]. It should be noted that grid-following converters may also be categorized as grid-supporting, but they still contain the fundamental issue of requiring to be connected to a stiff ac grid using the synchronization unit. As numerous researchers have identified the possible advantages of the grid-forming converter control during normal operating conditions, few efforts have been put to analyze and understand its transient characteristics and fault behavior, as replicating the short-circuit behavior of a synchronous machine is not feasible with current-sensitive semiconductor devices.

As described in [17], [18], there are mainly two methods which can provide current limitation and stability for grid-forming converter under large-signal disturbances: switching the control structure to the grid-following mode during the fault and limiting the converter currents using a virtual admittance structure. Along these lines, in [19], the converter control is switched to hysteresis control if the permissible allowed current is being exceeded. This method obviously looses all

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functionalities of the grid-forming control during this period, and how to deal with the saturation of outer control loops is not discussed. In a similar fashion, switching to grid-following control during the fault is proposed in [14], [20]–[22]. This solution needs a backup PLL for the synchronization, which then has its own stability issues for weak-grid conditions. As previously shown, the current limitation can be achieved simply by limiting the current references directly during the fault. However, this will cause wind-up in the outer power loops, which can lead to instability [17]. To circumvent this, several researchers propose the use of virtual resistors, either linear [23] or nonlinear [24] to reduce the converter voltage reference. Also, the influence of a virtual impedance structure on the current limitation is analyzed in [25]. As disclosed, the current limitation is largely depending on the fault location and the selected virtual impedance, which may limit its usefulness in practice as the maximum converter current is desired to be utilized during any fault condition. To that end, the virtual impedance concept may cause problems in parallel operation [24]. In [26], both limitations of the inner current reference and voltage reference reduction using the virtual impedance concept are conducted. In this way, the currents are limited and wind-up in the outer loops are avoided using the virtual impedance concept. Nevertheless, the virtual impedance still has the problem that its accuracy of limitation depends on several unknown factors as previously mentioned.

Conclusively, for the methods that switch to a grid-following structure during the fault, the robust grid-forming properties of the converter are lost. To that end, for the methods which directly limit the current references, either the outer power loops and droop controllers are not considered or wind-up and instability is encountered. To avoid wind-up in the outer power loops while limiting the currents, a virtual impedance may be used. However, the limiting performance of this is variable and depends on several unknown factors, which makes the utilization of it less attractive. Hence, how to deal with saturation in the outer loops alongside how to sustain the grid-forming structure while limiting the converter currents is not well described in the available literature. Thereby, this paper aims to describe the issues of current limitation of grid-forming converters considering the outer loops and their influence on the converter response. Besides this, an enhanced current limiting control method is proposed where the converter currents are precisely limited to the desired value and the converter remains as grid-forming during the fault. This is done by directly limiting the converter current references alongside adjusting the outer power references such to avoid wind-up in the outer loops and to keep their advantageous dynamics during the fault.

The remaining parts of the paper are structured as follows: Section II describes the structure of the considering grid-forming controller. The issues of grid-forming control during faults are identified and potential solutions for current limitation are tested in Section III. Section IV describes the proposed current limitation method alongside an enhanced fault recovery method using a dynamic damping controller. Subsequently, the proposed fault controller is experimentally verified in Section V. Finally, Section VI concludes the manuscript.

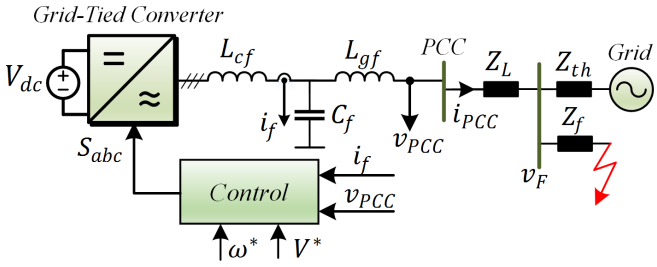

Fig. 1. The overall system of a grid-forming grid-tied Voltage-Source Converter (VSC) connected to an external Thevenin modeled grid with a symmetrical fault occurring close to the v_F bus.

TABLE I
MAIN PARAMETERS OF THE SYSTEM IN FIG. 1

Symbol	Description	Value
S_n	Rated power	7.35 kVA
V_b	Nominal l-l voltage	400 V (rms)
V_{dc}	dc-link voltage	730 V
f_0	Rated frequency	50 Hz
f_{sw}	Switching frequency	10 kHz
f_s	Sampling frequency	10 kHz
L_{cf}	Converter-side inductor	0.07 pu
L_{gf}	Grid-side inductor	0.04 pu
C_f	Filter capacitor	0.07 pu
Z_L	Thevenin/Line impedance	0.04j-0.5j pu
SCR	Short-Circuit Ratio	2-25

II. Structure of Grid-Forming Converter

The system under study is a grid-tied grid-forming converter as shown in Fig. 1 where the main parameters of the system can be seen in Table I. The detailed view of the grid-forming control structure, the Synchronous Power Controller (SPC), is depicted in Fig. 2 [27]. Here, the grid-forming converter is controlled to emulate a conventional synchronous generator with virtual mechanical and electrical characteristics. The mechanical part of the synchronous generator is emulated by virtual inertia and damping, which aims to support the network frequency, and the electrical part is emulated by a virtual stator impedance, which can be used to define the power sharing and power exchange with the grid [28]. The Power Loop Controller (PLC) provides the converter with the mechanical property of a synchronous machine and forms the relationship between power balance and the virtual angular frequency of the emulated machine. The Reactive Power Controller (RPC) provides the control with the voltage amplitude of the virtual machine by controlling the reactive power. The virtual angular frequency is integrated to obtain the phase angle, which together with the voltage magnitude forms the inner virtual electromotive force of the emulated machine. Droop control is contained in the outer two loops to determine the active and reactive power references based on the deviation of the network voltage and frequency. The droop controllers replicating the governor/turbine and Automatic Voltage Regulator (AVR)

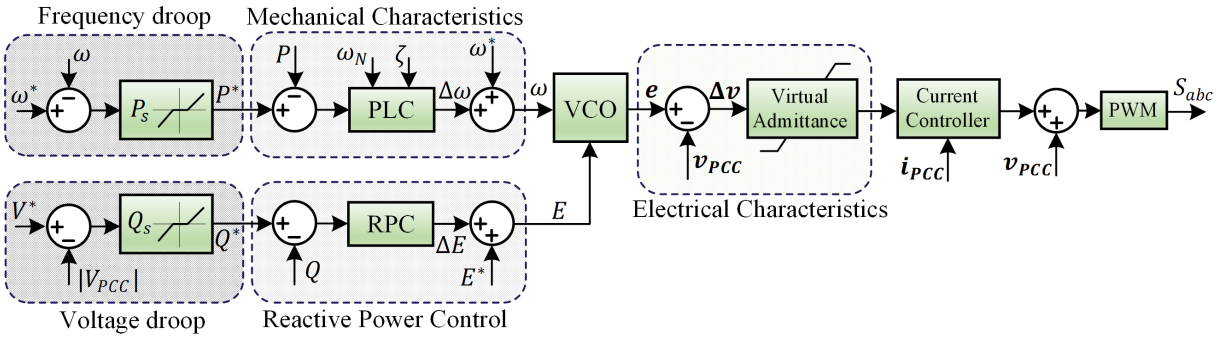

Fig. 2. Control block diagram of Synchronous Power Control (SPC). The Power Loop Controller (PLC) adjusts the frequency, dependent on the active power change from the droop controller with a defined natural oscillating frequency and damping coefficient.

of the synchronous machine are mathematically expressed as

$$P^* = P_s + (\omega^* - \omega)D_P \tag{1}$$

$$Q^* = Q_s + (V^* - |V_{PCC}|)D_Q \tag{2}$$

where P_s and Q_s are the external set points of the active and reactive power respectively, ω is the virtual oscillating frequency from the PLC, and D_P, D_Q are the droop gains for the active and reactive power, respectively. To achieve accurate and decoupled control of the active and reactive power, the virtual admittance block in Fig. 2, which specifies the virtual admittance of the stator windings, is included to guarantee an output impedance, which is dominantly inductive. The virtual admittance structure is implemented as

$$\mathbf{i}^*_{\alpha\beta} = \frac{\mathbf{e}_{\alpha\beta} - \mathbf{v}_{\alpha\beta}}{R_v + sL_v} \tag{3}$$

where R_v and L_v is the virtual resistance and inductance of the output stator impedance respectively, $\mathbf{e}$ is the virtual emf calculated from the two outer power loops, and $\mathbf{v}$ is the voltage measured at the Point of Common Coupling (PCC). Since the inner current control forms a cascaded loop with the virtual admittance, the bandwidth of the virtual admittance should be set significantly slower than that of the inner current loop. As described in [29], the virtual reactance should be fixed to 0.3 pu of the rated impedance of the converter, which corresponds to a typical reactance value for a grid-connected synchronous machine. Subsequently, the virtual resistance is selected to get a desired cut-off frequency of the virtual admittance low-pass filter. By choosing the cut-off frequency ten times slower than the inner current controller, a virtual resistance of 0.1 pu is selected.

With the virtual admittance selected such that the impedance seen from the converter terminals is highly inductive, the three-phase power transfer between the virtual machine and the grid at the sending-end can be determined as

$$P = \frac{3}{2}\frac{EV_g \sin(\delta)}{X} \approx \frac{3}{2}\frac{EV_g\delta}{X} = P_{max}\delta, \tag{4}$$

$$Q = \frac{3}{2}\left(\frac{E^2 - EV_g\cos(\delta)}{X}\right) \approx \frac{3}{2}\frac{E(E-V_g)}{X} \tag{5}$$

where δ is the phase angle difference between the two sources, X is the total output reactance between the two sources, P_{max} is the three-phase nominal active power, and E, V_g are the peak-values of the voltage at the sending-end and receiving-end, respectively. The SPC uses the internal synchronization mechanism in AC networks similar to a synchronous machine. This inherent power-based synchronization structure is obtained by using a regulator of the active power error, the Power Loop Controller (PLC), to generate the synchronization angle/frequency. Usually, to emulate the characteristic properties of a synchronous machine, but with a simple implementation, the swing equation is employed as

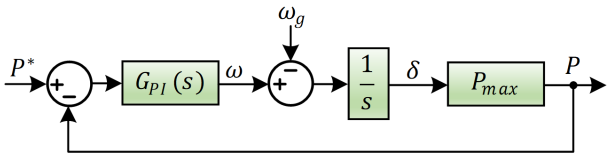

Fig. 3. Block diagram of PLC with a PI controller to form a relationship between active power error and virtual frequency of the machine.

$$\frac{2HS_n}{\omega_0}\frac{d^2\delta}{dt} = P_m - P_e - D\omega_0\frac{d\delta}{dt} \tag{6}$$

where H is the inertia constant, S_n is the rated power, D is the total damping coefficient, P_m is the mechanical power, P_e is the electrical power, ω_0 is the rated electrical angular frequency, and δ is the load angle of the machine relative to the grid. However, since the damping coefficient of the swing equation introduces a steady-state droop effect given a frequency deviation, a PI controller is used in the PLC instead. With this, the PLC dynamics of the block diagram in Fig. 3 can be expressed as

$$\frac{P(s)}{P^*(s)} = \frac{P_{max}K_{pp}s + K_{ip}P_{max}}{s^2 + K_{pp}P_{max}s + K_{ip}P_{max}} = \frac{2\zeta\omega_N s + \omega_N^2}{s^2 + 2\zeta\omega_N s + \omega_N^2} \tag{7}$$

To emulate the inertia constant and damping ratio of the second-order response, the controller gains should be selected as

$$K_{ip} = \frac{\omega_0}{2HS_n}, \quad K_{pp} = \zeta\sqrt{\frac{2\omega_0}{HS_nP_{max}}} \tag{8}$$

where the inertia constant is selected in the range $H \approx 2-5$ s.

Besides the PLC, the RPC is used to regulate the amplitude of the voltage reference to obtain a given desired reactive power similar as the AVR and exciter of a synchronous

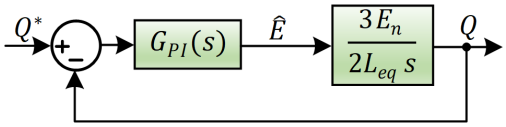

Fig. 4. Small-signal control block diagram of the reactive power controller (RPC).

machine. Using the three-phase reactive power from (5) and linearizing around $Q = 0$, i.e. $E_0 = V_{g0} = E_n$, one gets that

$$\hat{Q} = \frac{3}{2}\frac{2E_0 - V_{g0}}{L_{eq}s}\hat{E} = \frac{3E_n}{2L_{eq}s}\hat{E}. \tag{9}$$

where E_n is the nominal voltage of the virtual machine. Using a PI controller to regulate the reactive power as shown in Fig. 4, the closed-loop transfer function for the RPC becomes

$$\frac{Q(s)}{Q^*(s)} = \frac{\frac{3E_nK_{pq}}{2L_{eq}}s + \frac{3K_{iq}E_n}{2L_{eq}}}{s^2 + \frac{3E_nK_{pq}}{2L_{eq}}s + \frac{3K_{iq}E_n}{2L_{eq}}}. \tag{10}$$

The proportional and integral gains can be selected to achieve the desired damping and undamped natural frequency as

$$K_{pq} = \frac{4\zeta\omega_N L_{eq}}{3E_n}, \quad K_{iq} = \frac{2\omega_N^2 L_{eq}}{3E_n}. \tag{11}$$

The equivalent inductance L_{eq} is the total inductance between the inner machine emf and the grid voltage given as

$$L_{eq} = L_v + L_{cf} + L_{gf} + L_g + L_L \text{ where } L_v = \frac{X_v V_b^2}{\omega_0 S_n}. \tag{12}$$

The inner current controller is a PR controller implemented in the $\alpha\beta$-reference frame as in [30], [31].

III. Control Issues with Grid-Forming Converters during Grid Faults

This section explains the fundamental issues of grid-forming converter control during grid-fault conditions and initiates the development of the foundation for the proposed fault-mode controller to be described in section IV.

To highlight the control issue of the SPC, a symmetrical three-phase fault is tested as shown in Fig. 5 where its controller parameters for the grid-forming structure is displayed in Table II. To simulate the grid fault, the three-phase voltages of the Thevenin grid is directly controlled to instantaneously change its voltage magnitude when the fault is considered to occur. From Fig. 5, it can be observed that the PCC voltage is being highly supported inherently by the grid-forming structure without any control modification during the fault. Even though this is a particularly attractive feature, this voltage support is realized through a large injection of reactive current with a magnitude of 6.7 pu.

As the SPC is a voltage controlled structure, it simply requests a current reference to maintain the reference voltage in order to satisfy the demands from the outer PLC and RPC. Hence, compared to a grid-following converter, the SPC behaves as a voltage source with controlled amplitude and frequency. In case of short-circuit fault conditions, the controlled voltage source will naturally respond by injecting very high current values to sustain its voltage level. With

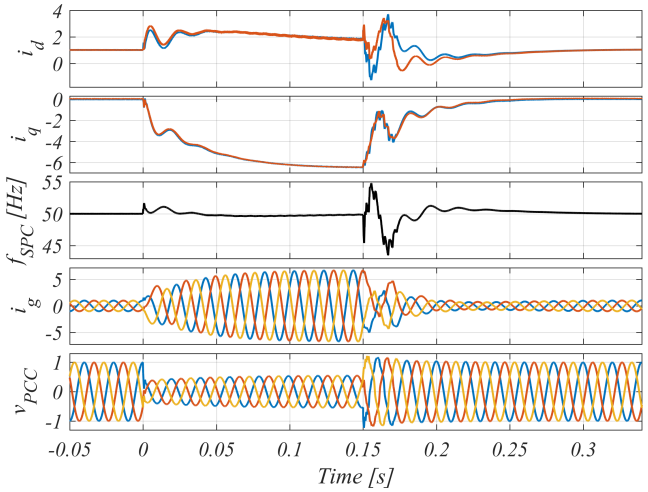

Fig. 5. Simulated fault response of SPC during a symmetrical fault with a voltage magnitude of 0.3 pu and a grid impedance of 0.04 pu. For the dq-axes currents, the actual (blue) and the reference values (red) are visualized.

that, since VSCs must be protected from overcurrent of the semiconductor devices, the current reference must be restricted given it is higher than permitted.

Even though the SPC can provide grid-supporting functionalities, provided that a power reserve is available, which enhances the transient stability of the network, the synchronization stability of the converter may be diminished in case of grid faults when including current limiters [32]. This may indicate that the outer loops have an impact on the response when the current magnitude is limited as their requested voltage reference may be met. Therefore, it is desired to test different limiting strategies to evaluate how a voltage-mode control structure can be employed during symmetrical grid faults. From this, current limitation is required but during grid faults where the converter may be saturated, synchronization instability may be at risk.

One solution is of course to oversize the converter such that it is able to handle larger currents. However, this comes with an increased converter cost, which is highly undesired. Another approach could be to decrease the virtual admittance to limit the current [23]. However, two issues have been encountered when doing this. At first, the value of admittance needed to achieve a given maximum current is dependent on the voltage sag and control, i.e. it changes for different fault conditions. One may decrease the admittance until the admissible current is achieved. However, the maximum allowable converter current is independent on any fault condition and control. Therefore, it is easier and more intuitive to implement a direct current limiter on the reference values. Secondly, if the inductance of the virtual admittance structure is increased for current limitation when a fault is detected, a dc-bias may be introduced to the current references as the inductor current cannot change its value instantaneously. Therefore an ac signal with a decaying dc component will occur in the current reference which is not desired. Accordingly, the current limitation will be based on directly limiting the converter current reference to avoid these issues. As the control structure operates with sinusoidal signals, an instantaneous hard limiter

TABLE II
CONTROL PARAMETERS OF THE SPC STRUCTURE IN FIG. 2

Grid-Forming Controller (SPC)	Parameters
Droop Control	$D_P = 0$, $D_Q = 178.7$ VAr/V
Virtual Admittance	$R_v = 0.1$ pu, $L_v = 0.3$ pu
Current Controller	$K_p = 12$, $K_r = 2000$
PLC	$H = 2$ s, $\zeta = 0.707$, $K_{pp} = 1.7$e-3, $K_{ip} = 10.7$e-3
RPC	$\zeta = 0.707$, $\omega_N = 20$ rad/s, $L_{eq} = 29.7$ mH, $E_n = 326.6$ V

will clip the peak of the signal, resulting in a deteriorated output current. To circumvent this, a circular limiter is implemented where the stationary frame current reference is determined as

$$\mathbf{i}^*_{\alpha\beta} = \begin{cases} \mathbf{i}_{\alpha\beta} \frac{I_{lim}}{\sqrt{i_\alpha^2 + i_\beta^2}} & \text{if} \quad \sqrt{i_\alpha^2 + i_\beta^2} > I_{lim}, \\ \mathbf{i}_{\alpha\beta} & \text{otherwise}, \end{cases} \tag{13}$$

where I_{lim} is selected as 1.2 pu of the nominal converter current. The result of the circular limiter can be examined in Fig. 6. As desired, the output current is limited to 1.2 pu during the fault, the outer control loops injects reactive power to boost the voltage, and the PLC reduces its active power output due to a jump in the virtual frequency. Only the peak-values of v_{PCC} is shown in Fig. 6 such that the sustained overvoltages after the fault recovery can be easily visualized. During the time $0 - 0.15$ s, the PCC voltage simply drops and is supported as shown in Fig. 5.

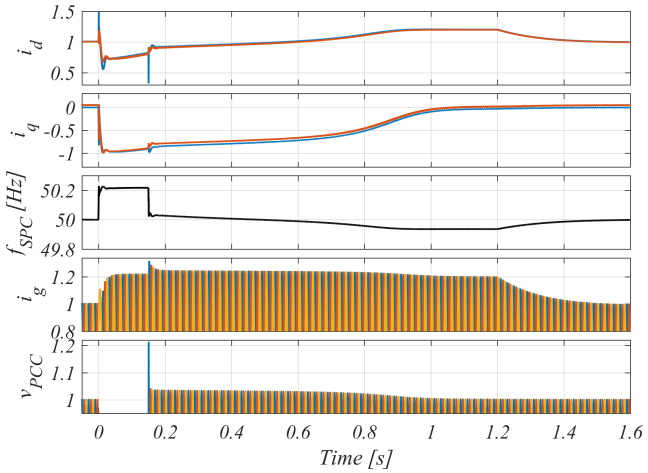

Fig. 6. Simulated fault response of SPC during a symmetrical fault with a voltage magnitude of 0.3 pu. The grid impedance is 0.04 pu and the current reference is limited to 1.2 pu. For the dq-axes currents the actual (blue) and the reference values (red) are visualized.

Withal, a few things should be perceived. Albeit capacitive reactive current is injected, the converter does not comply with the grid code since the voltage support is decreasing during the fault period (i_q increases during the fault). Furthermore, due to the high power references of the slow outer loops and the saturation of the current reference, an elongated unsatisfactory post-fault response is experienced caused by integrator windup in the outer loops. At this time, the active power is slowly increased to 1.2 pu till it matches the power references to the current limiter where after it returns the desired steady-state condition. Using this, it can be seen that the converter currents can be limited but the fault response and especially the post-fault response needs improvement. One problem of the method just discussed is that the outer power loops are not adjusted to take into account that the converter has very limited margins with respect to the injected currents and actually becomes saturated. To address this issue, it should be possible to limit the converter output current by changing the active and reactive power references in case of a fault [33]. With this, the admissible converter power is updated when the fault occurs as

$$S_{new} = \sqrt{\frac{3}{2}} \cdot \frac{V^+ - V^-}{V_b} S_n \tag{14}$$

where $V^+ = \sqrt{v_\alpha^{+2} + v_\beta^{+2}}$ and $V^- = \sqrt{v_\alpha^{-2} + v_\beta^{-2}}$, are the amplitudes of the positive and negative sequence voltages, respectively. In the case of a symmetrical fault where $V^- = 0$,

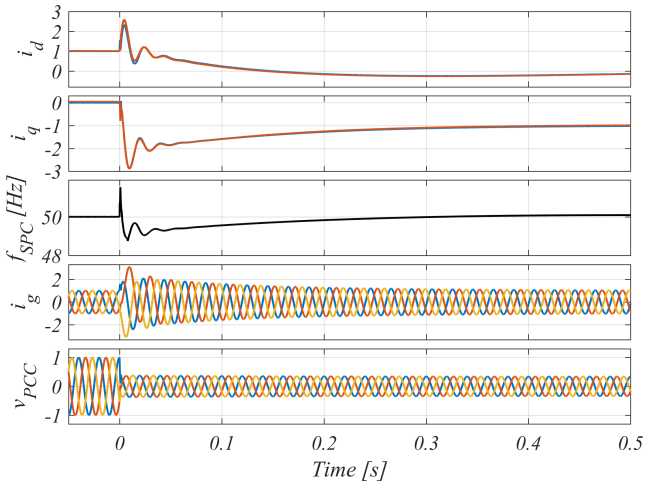

Fig. 7. Simulated fault response of SPC during a symmetrical fault with a voltage magnitude of 0.3 pu. The grid impedance is 0.04 pu and the power references are limited as shown in (16). For the dq-axes currents, the actual (blue) and the reference values (red) are visualized.

the expression reduces to

$$S_{new} = V_{pu} S_n. \tag{15}$$

The reactive power reference, which complies with the grid

codes, can then be computed as

$$Q^* = \begin{cases} \text{Voltage Droop} & \text{if } V_{pu} > 0.9, \\ 2S_{new}(1 - V_{pu}) & \text{if } 0.5 < V_{pu} < 0.9, \\ S_{new} & \text{otherwise.} \end{cases} \quad (16)$$

Using the updated apparent power and the reactive power reference, the active power reference which averts destructive overcurrents can be determined as

$$P^* = \sqrt{S_{new}^2 - Q^{*2}}. \quad (17)$$

In case the reactive power reference is greater than the new rated converter power, the active power reference is set to zero and the reactive power reference is set equal to S_{new}. The power limiting method presented in (16) is tested during a symmetrical fault as shown in Fig. 7. Using this, the maximum values of the injected current is reduced to around 3 pu and firmly decreases to 1 pu as the power reference dictate. Despite that, overcurrents are conspicuous for a duration of more than 10 fundamental cycles due to the slow transient response of the outer PLC and RPC.

IV. Enhanced Fault Ride-Through of Grid-Forming Converter

Based on the analysis and approaches just described for current limitation, a method is proposed which limits the converter current while keeping the fundamental structure of the grid-forming control during the fault. This is done by combining the two approaches from the previous section, i.e. inner current limitation and outer power reference adjustment. Additionally, a dynamic virtual damping controller is proposed to enhance the fault recovery process of the grid-forming converter when the fault is cleared.

A. Current Limitation and Reference Power Adjustment

Considering that it is just desired to limit the converter currents and not anything else during the fault, the current reference is still the most logical location to intervene. Therefore, a method where the reference power is adjusted based on the voltage dip during the fault (16) together with the circular current limitation (13) is proposed. As a result of these, the currents will be limited and the reference values set to the outer power controllers will be adjusted based on the grid code requirements. Accordingly, by using the circular limiter to provide precise current limitation alongside realizing that the power update approach from [33] can be reformulated and utilized for a grid-forming converter with outer power loops to avoid instability and wind-up, comprise the contribution and the proposed fault-mode controller. To that end, how to transition between the two power references and how to merge (16)-(17) with the droop operation of the SPC is as well addressed. The proposed structure is depicted in Fig. 8 where F_M is the fault-mode signal used to switch between the power references from the outer droop controllers and the power reference based on the grid code requirements. The fault signal, S_F, is set high when the magnitude of the stationary-reference frame voltage vector drops below 0.9 pu. When this occurs with a response time below 1 ms, F_M takes a logical high state and immediately switches to the fault-mode control. With the proposed method in Fig. 8, the fault-mode control is preserved after the fault recovery until the differences between the per-unit values of the active and reactive power references of the droop controllers and the fault-mode control defined in (16)-(17), fall below P_{diff}. Therefore, the time after fault recovery where the fault-mode control is activated is depending on P_{diff}, the droop coefficients, and the fault recovery response defined by the external network. However, considering the selected droop coefficients are general and selecting $P_{diff} = 5\%$ of the nominal power, then the fault-mode control is activated 150 ms after the fault has been cleared. As the difference between the two controllers is small when the fault-mode control is deactivated and since the bandwidths of the outer PLC and RPC are low, the reactivation of the droop controllers happens seamlessly without disturbances in the injected currents and does therefore not affect the performance of the system. Therefore, with this configuration the characteristics of the virtual machine is kept both during normal as well as fault conditions and the converter current is limited. The only difference between the modes is that the outer power references set by the droop controllers are bypassed during the fault.

The performance of the proposed method when exposed to a symmetrical fault is visualized in Fig. 9. Due to the imbalance between the measured and requested active power during the fault recovery, a frequency response dictated by the dynamics of the virtual mechanical characteristics of the emulated machine emerges. This temporary increase in the virtual oscillating frequency is necessary for the converter to once again pick up the load and keep synchronized with the external grid. By using this control approach, the current injection during the fault comply with the grid code and the post-fault response is significantly improved without exceeding the permitted current and without the inconvenience to adopt a PLL-based grid-following structure during the fault. As proposed in [14], [20], if a grid fault is detected, the power-synchronization control is switched to current-mode control in order to limit the converter currents. This can effectively be done but has the need for a backup PLL which is used in order for the converter to remain synchronized with the grid during the fault. As explained in [4], [5], [34], the PLL is a critical component for the converter stability, especially during low-voltage situations. Accordingly, it is highly advantageous that the method presented in Fig. 8 can limit the converter currents, comply with grid code requirements without switching the fundamentals of the control structure.

B. Enhanced Fault Recovery using Dynamic Damping

From Fig. 9, some amount of undesired weakly damped oscillations are experienced during the recovery process. These oscillations are becoming an increasing issue as the SCR is decreasing since an increased sensitivity between the injected currents from the converter and the PCC voltage will emerge. To enhance the fault recovery process, a dynamic damping method is proposed in addition to the fault control presented

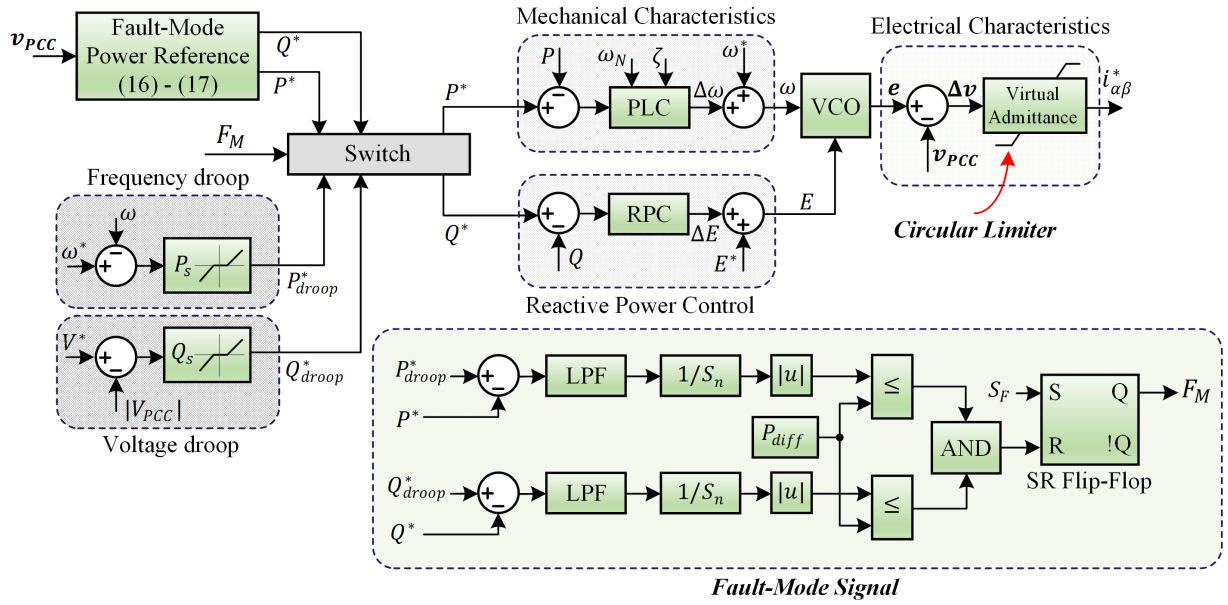

Fig. 8. Proposed fault-mode control structure of SPC where F_M selects between droop control and power reference control based on grid code requirements and a circular limiter is used to constrain the current reference.

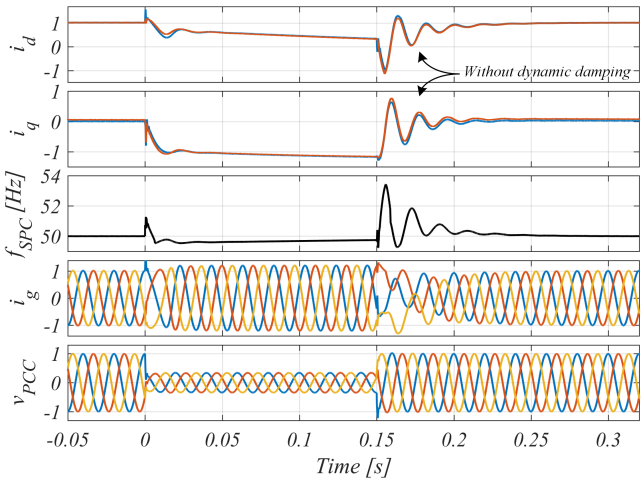

Fig. 9. Simulated fault response of SPC during a symmetrical fault with a voltage magnitude of 0.3 pu. The grid impedance is 0.04 pu and the control structure shown in Fig. 8 is used for the reference power calculation. For the dq-axes currents, the actual (blue) and the reference values (red) are visualized.

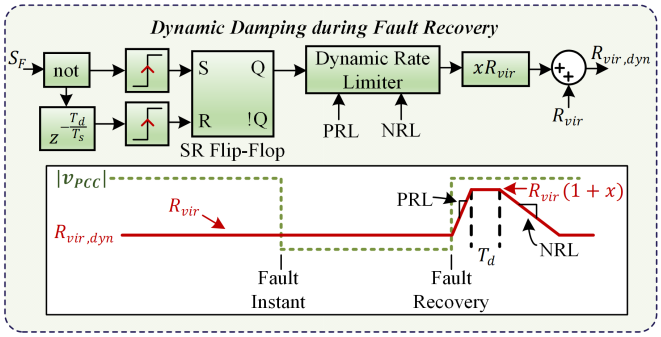

Fig. 10. Dynamic damping during fault recovery where the virtual resistance is increased momentarily during the fault recovery to provide additional system damping. The dynamic virtual resistance, $R_{vir,dyn}$, is increased to $R_{vir}(1+x)$ quickly based on the Postive Rate Limiter (PRL) when the voltage recovers. After a delay of T_d, the virtual resistance is again lowered to R_{vir} with the ramp rate defined by the Negative Rate Limiter (NRL).

in the previous section. The fundamental principle is to adaptively decrease the conductivity in the virtual admittance structure momentarily during the recovery period as shown in Fig. 10. The operation is that when the fault is cleared, the output of the SR flip-flop is set high, which increases the virtual resistance from R_{vir} to $R_{vir}(1+x)$ at a rate defined by the Positive Rate Limiter (PRL). This increased damping is sustained for a duration of T_d seconds where after the resistance is again decreased to its post-fault value with a rate defined by the Negative Rate Limiter (NRL). The slope defined by the PRL as depicted in Fig. 10 is intentionally drawn low for clear visibility. During the tests conducted, the PRL is set with a slope of 10000 making the increase in virtual resistance to happen in one sampling period. On the other hand, the NRL is set such that the virtual admittance will ramp down from $R_{vir}(1+x)$ to R_{vir} in 10 ms. The constant x showed in Fig. 10 can be set manually depending on which virtual damping is needed to provide an acceptable fault recovery response. Using the proposed dynamic damping during the fault recovery, it can be seen from Fig. 11 that the oscillations in the dq-axes currents have been highly decreased by the use of the dynamic damping controller in Fig. 10. A detailed view of the fault recovery response using different values for the dynamic damping is provided in Fig. 12. Here, the fault is cleared at 0 s and the actual dq-axes currents during the recovery are shown. As it can be clearly seen, the under- and overshoot in i_d and i_q, respectively, can be significantly reduced by increasing the virtual resistance in the dynamic damping control. The improvements in reducing the under- and overshoot during the fault recovery are specifically calculated and presented in Table. III where it can be observed that the overshoot in i_q can be fully eliminated. Such tight

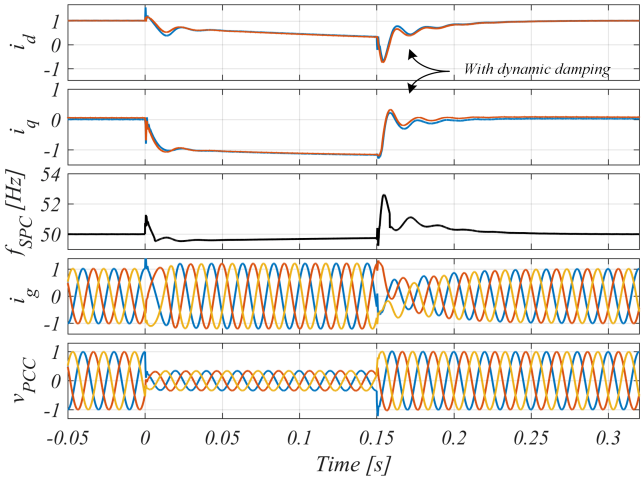

Fig. 11. Identical simulation case study as in Fig. 9 but with dynamic damping activated during the fault recovery as shown in Fig. 10 where $x = 1$. For the dq-axes currents, the actual (blue) and the reference values (red) are visualized.

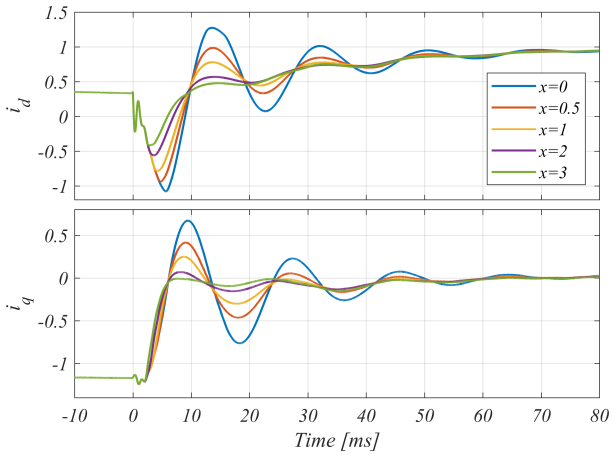

Fig. 12. Influence of dynamic damping on i_{dq} during fault recovery occurring at 0 s for the test conditions as in Fig. 9. The dynamic damping is changed using x from Fig. 10.

control of i_q has a positive impact on the PCC voltage recovery as injecting positive i_q will make the converter act as an inductor prolonging the voltage recovery process.

C. Method Comparison and Weak-grid Performance

With the fault-mode controller and dynamic damping structure being presented, the proposed SPC is compared to the solution proposed in [22], which represents a comprehensive and implementable fault-mode controller for a grid-forming converter during fault conditions. Here, the control structure is switched to a grid-following PLL-synchronized structure during the fault to limit the converter currents. When the fault has been cleared, the transitioning back to the grid-forming controller is performed using a feedback tracking controller, which after the fault, aligns the phase-angles of the two controllers and perform a seamless switching when aligned. For the comparison, two test cases are considered: a fault where the SCR is 5 and a fault where the SCR is 2, where the latter represents a more realistic case where the grid-forming technology may be utilized. The results of the two cases using the method based on [22] are shown in Fig. 13. In the top of each figure, one can identify the fault duration in addition to the time where the grid-following mode is activated. Besides a temporary overcurrent when entering the fault, it can be appreciated from Fig. 13(a) that the grid-following mode can limit the converter currents and provide a good fault ride-through response. The settling time of i_q when the fault occurs is 18 ms whereas during the voltage recovery, the active current settles in 23 ms and the reactive current has a slight overshoot of 0.4 pu before reaching steady-state. When decreasing the SCR to 2 as shown in Fig. 13(b), the disadvantage of the PLL-synchronized grid-following structure can be observed. A fully unstable response results where high uncontrolled converter over-currents arise. The stability is again obtained when the grid-following structure is switched back to the grid-forming controller.

TABLE III
INFLUENCE ON i_{dq} UNDER- AND OVERSHOOT DURING FAULT RECOVERY USING DIFFERENT DYNAMIC DAMPING VALUES OF x FROM FIG. 12.

x in Fig. 10	i_d undershoot	i_q overshoot
0	210 %	57 %
0.5	189 %	35 %
1	165 %	21 %
2	133 %	6 %
3	108 %	0 %

The same two tests are performed using the proposed structure as it can be perceived in Fig. 14. For the case where $SCR = 5$ (Fig. 14(a)), a similar response as observed with the grid-following structure is obtained. When comparing the transient time performance a slight difference exists. The settling time of i_q when the fault occurs is decreased to 10 ms whereas during the voltage recovery, the active current settles in 35 ms and the reactive current has an overshoot of 0.35 pu before reaching steady-state. To that end, compared to the small glitch happening in Fig. 13(a) when the grid-following mode is deactivated, the seamless transition of the proposed structure is unnoticeable from Fig. 14(a). For the last test where the $SCR = 2$, the results using the proposed structure can be seen in Fig. 14(b). Due to the high line impedance, a significant amount of reactive current needs to be provided in addition to the nominal active power injection. This results in a quite challenging operating condition as the injected current is a bit above nominal when the grid fault occurs. As it can be seen, the dq-axes currents quickly reach their reference values in a stable manner and the recovery process happens with a negligible overshoot in the q-axis current and in a low oscillatory manner. Due to the distorted and temporarily unbalanced voltage and currents around 20 ms into the fault, a jump can be observed in the dq-axes currents. Based on this, the proposed structure is able to limit the converter currents and transition to and from the proposed fault-mode controller in an appreciated manner, even during very weak-grid conditions.

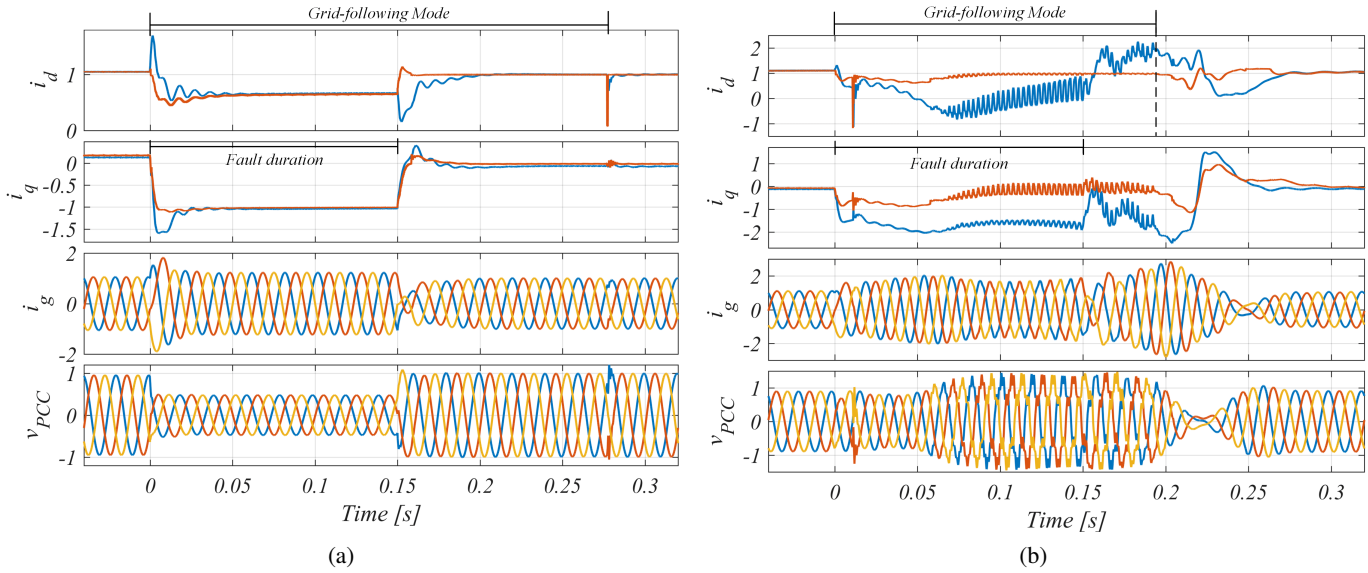

Fig. 13. Simulated fault response during a symmetrical fault with a voltage magnitude of 0.3 pu. The control structure is based on [22] where the grid-forming controller is switched to grid-following during the fault. For the dq-axes currents the actual (blue) and the reference values (red) are visualized. (a) $SCR = 5$, (b) $SRC = 2$.

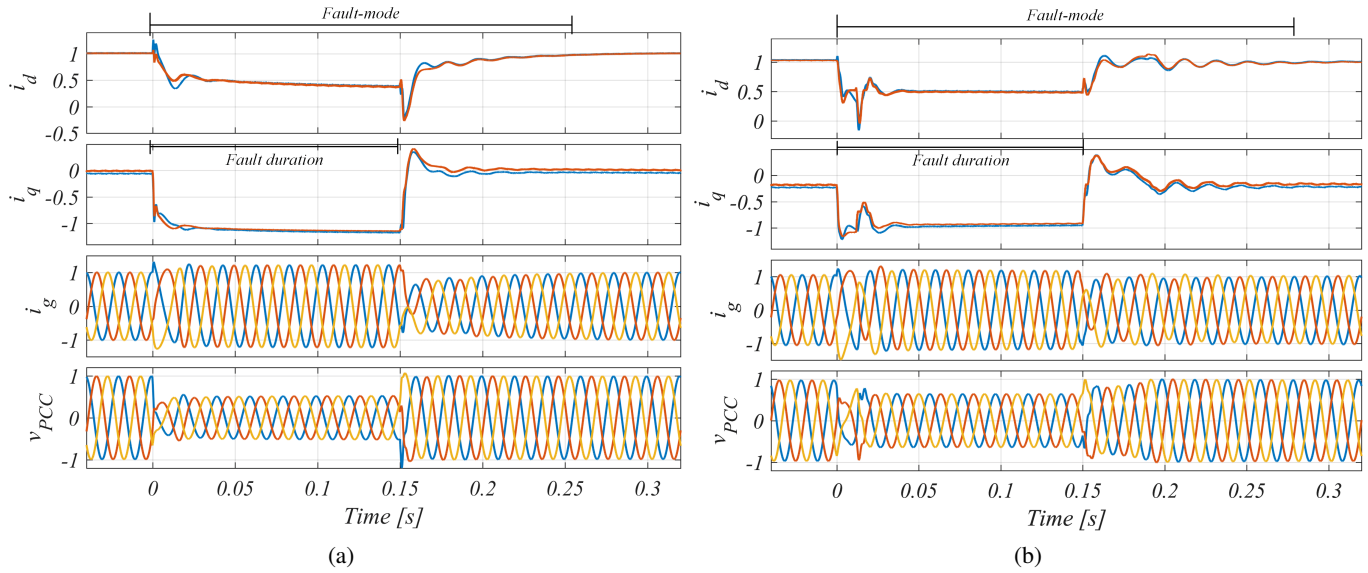

Fig. 14. Simulated fault response of proposed SPC using dynamic damping with $x = 2$ during a symmetrical fault with a voltage magnitude of 0.3 pu. The control structure shown in Fig. 8 is used for the reference power calculation. For the dq-axes currents, the actual (blue) and the reference values (red) are visualized. (a) $SCR = 5$, (b) $SRC = 2$.

V. Experimental Verification

To further verify the proposed fault-mode control and dynamic damping control, these are tested experimentally in the laboratory setup shown in Fig. 15. A Yaskawa D1000 active rectifier is used to control the dc-link voltage to the desired value of 730 V. The converter under test is the grid-tied converter, which is a Danfoss VLT FC-302 15 kVA frequency inverter. The converter currents, grid currents, and PCC voltages are being measured using two types of LEM sensors whereas only i_f and v_{PCC} are being used for control purposes. Between the LCL-filter and the grid simulator is the line impedance taking values in the range of 0.04-0.2 pu. The grid simulator is a Chroma Regenerative Grid Simulator Model 61845 which is specifically programmed to emulate the grid fault by directly controlling the three-phase voltages at its output. By this, at the fault instant of interest, the amplitudes of the three-phase voltages are reduced to 0.3 pu in 0.1 ms. Hereafter, they remain constant for the fault period of 0.15 s and then they increase to their nominal value with the same dynamic response. From the measurements, the actual programming, control, and data acquisition are processed in a dSPACE expansion box consisting of a DS1007 PPC processor board for code actuation, a DS5101 digital waveform output board for PWM pulse signal generation, and a DS2004 high-

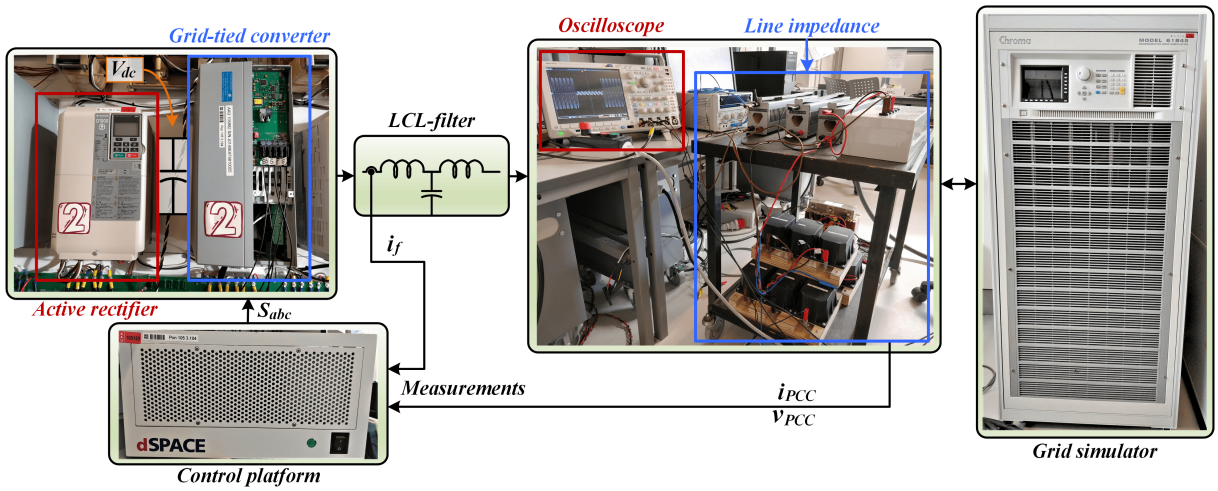

Fig. 15. Laboratory setup used for the experimental verification. The grid-tied converter is controlled using a dSPACE controller and is connected to an LCL-filter, a line impedance, and finally a grid simulator which emulates the voltage sag of the grid fault.

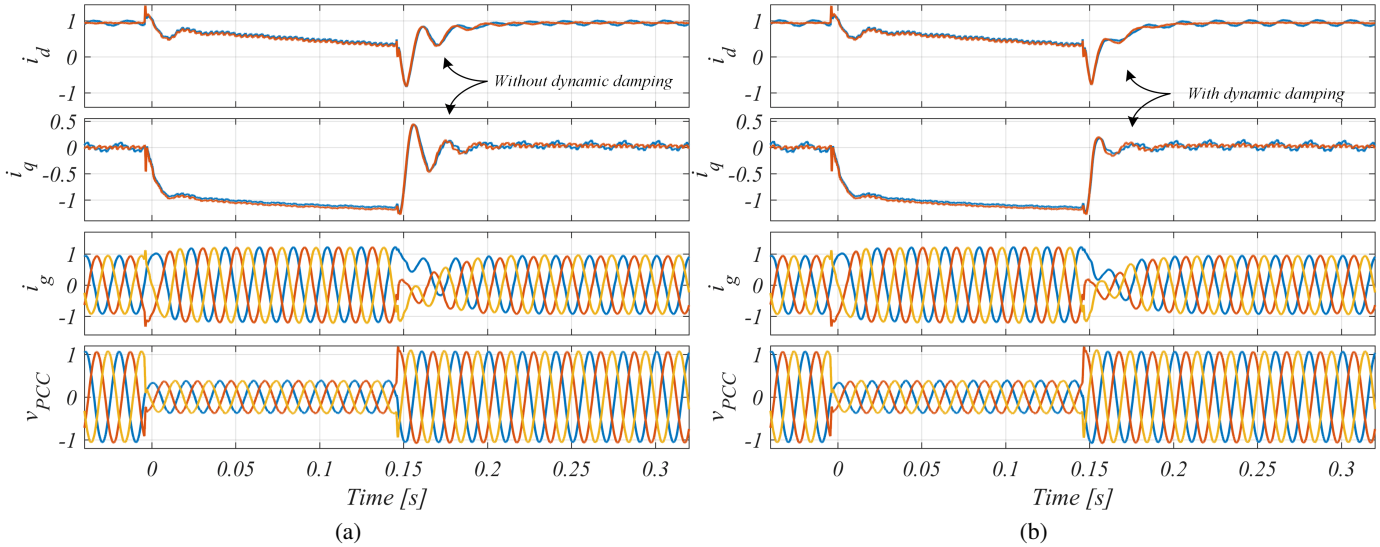

Fig. 16. Experimental validation of proposed fault mode controller for an SCR of 25. (a) Without dynamic damping during the fault recovery. (b) With dynamic damping during the fault recovery where $x = 1$ in Fig. 10. For the dq-axes currents, the actual (red) and the reference values (blue) are visualized.

speed A/D board for measuring of the currents and voltages. The parameter values for the setup and control can be seen in Table I and Table II, respectively. The response without and with the dynamic damping using the proposed fault-mode control is depicted in Fig. 16. The experimental results are in good agreement with the simulation study where it is evident that the dynamic virtual damping provides sufficient damping to achieve an acceptable fault recovery process. Finally, the proposed fault-mode controller is tested experimentally for an SCR of 5 as visualized in Fig. 17. Once again, the grid-forming structure is shown to be able to successfully ride through the fault without exceeding the maximum allowed converter current. Also, the weakly damped oscillations during the fault recovery are seen to be more adverse considering the lower SCR. However, the fault recovery is significantly enhanced with the use of dynamic damping control.

Notably, it can be seen from Fig. 17, that the PCC voltage contains higher distortions with a decreasing SCR. This originates as a result of the interaction between the larger line impedance and the voltage feed-forward in the controller. Accordingly, for lower SCRs, a trade-off between fast fault recovery response and low harmonic distortion in the PCC voltage must be made by adjusting the voltage feed-forward.

VI. Conclusion

Grid-forming converters are becoming increasingly attractive as potential candidates for converter control of future power electronics-based power systems due to their grid-friendly functionalities. As the converter include current-sensitive semiconductor devices, it cannot sustain the behavior of a voltage source during grid faults as its short-circuit capability is much lower than that of a synchronous generator. This paper discusses the issues of current limitation of grid-forming converters and introduce a proposed method, which

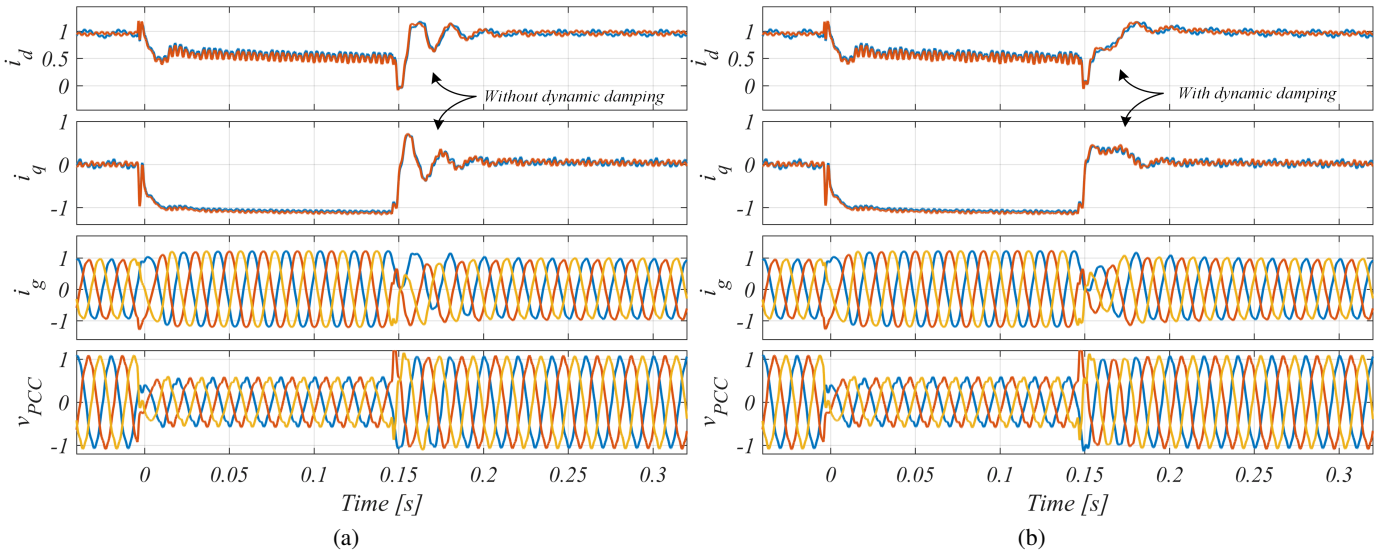

Fig. 17. Experimental validation of proposed fault mode controller for an SCR of 5. (a) Without dynamic damping during the fault recovery. (b) With dynamic damping during the fault recovery where $x = 3$ in Fig. 10. For the dq-axes currents, the actual (red) and the reference values (blue) are visualized.

includes several advantageous properties: instantaneous limitation of the converter currents, compliance with grid code requirements, and circumvention to switch the fundamentals of the control structure during the fault. To that end, enhanced fault recovery is attained by a proposed dynamic virtual damping controller. With this, it is shown that the grid-forming converter can provide grid-supporting functionalities during normal operating conditions and by only modifying the outer power reference generation instead of the inner structure, fault ride-through capability is achieved. The proposed fault-mode and dynamic virtual damping controller of the grid-forming converter are tested during very weak-grid conditions and its performance is verified experimentally.

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