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A Fault-Tolerant, Passivity-Based Controller Enhanced by the Equilibrium-to-Equilibrium Maneuver Capability for the DC-Voltage Power Port VSC in Multi-Infeed AC/DC Modernized Grids

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Abstract—Due to simplicity, practicality, and absence of communication needs, stabilizing the dc voltage via a dc-voltage power port voltage-sourced converter (VSC) connected to an ac grid (also known as the master VSC in some works of literature), is a favorable option in multi-infeed ac/dc modernized grids (MI-AC/DC-MGs). However, in MI-AC/DC-MGs, several devices may be connected/disconnected to/from the dc link. This affects the effective inductance and capacitance seen from the dc side of the dc-voltage power port VSC. Moreover, the use of dc-side LC-filter to improve the power quality aspects associated with the power feeding to the dc loads and with the power generated by dc generators is increasing. Such factors complicate the dynamics of the dc-voltage power port VSC and threaten its stability, as well as its transient performance. This article proposes an enhanced nonlinear control approach (compared to existing methodologies) for the dc-voltage power port VSC in MI-AC/DC-MGs considering the following very influential factors. First, it considers a nonlinear control approach considering the presence of the dc-side energy-storing components with uncertain parameters. The proposed controller accounts for complete nonlinear dynamics of the dc-voltage power port VSC with a dc-side inductance without any cascaded control structure. Thus, it “globally” stabilizes nonlinear dynamics by means of a passivity-based design approach with equilibrium-to-equilibrium maneuver capability. Second, it considers fault-tolerant control of the primary control of such systems in order to enhance the MI-AC/DC-MGs’ resiliency, which is highly required to improve the reliability of MI-AC/DC-MGs of the future. Making the primary control of the dc link “fault-tolerant” is a vital factor in order to have better-guaranteed power quality in the MI-AC/DC-MGs undergoing many types of events. This will cause MI-AC/DC-MGs to have fault ride-through (FRT) feature. Also, this feature, which is proposed and enhanced in this paper, generally strengthens the flexibility of MI-AC/DC-MGs by removing additional requirements for the controllers of other currently connected VSCs (e.g., those are working as constant P/Q active loads, etc., which are forming other entities of the multi-infeed ac/dc grid) in order to effectively benefit from them. Theoretical analyses, simulation results, and experimental tests are presented in order to show the effectiveness of the proposed controller in this article.

Index Terms—DC-side inductance, equilibrium-to-equilibrium maneuver, fault-tolerant controls, multi-infeed ac/dc modernized grids, passivity-based control, primary control, sigma-delta modulation/modulator based on sliding mode controls, variable-structure control, voltage-sourced converters.

I. INTRODUCTION

Electric power was initially generated in the late nineteenth century by means of dc systems using the dynamo. The distribution and utilization of electric power were also based on dc systems; there are a few distribution systems around the world that still use dc. However, ac power systems became developed and popular after series of events surrounding the introduction of competing electric power transmission systems in the late 1880s and early 1890s, called *The War of the Currents* [1]. Afterward, ac systems occasionally gave ground to dc systems because of various technical and economic reasons, so dc systems again became progressed. Nowadays, under the umbrella of smart grids, dc-energy-pool-based multi-infeed ac/dc modernized grids (MI-AC/DC-MGs) are gaining high momentum either in power distribution systems (e.g., in the shape of microgrids), or in transmission systems as discussed and detailed in [2]–[18]. MI-AC/DC-MGs are rapidly increasing under the smart grid vision to facilitate the effective integration of renewables, battery energy storage units, and modern ac/dc loads into existing grids.

One of the core parts of MI-AC/DC-MGs is a grid-connected voltage-sourced converter (VSC)—which is a dc-voltage power port [15] (also known as the master VSC in some literature e.g., [14]–[16], etc.)—whose dynamics are completely nonlinear and will dramatically be affecting ac-side dynamics and vice versa. Although the linear controller synthesis for the small signal linearized model of VSCs around one operating point is feasible and applicable [19], there still exists a possibility of a loss of some “unmodeled” dynamics associated with the linearization itself and of having poor transient performance in some circumstances [14]–[16]. Consequently, the enhancement of the nonlinear controller of VSCs should be considered, studied, and thoroughly investigated in some unseen aspects of their application in MI-AC/DC-MGs, feeding high-demand loads with different dynamics. To the best of authors’ knowledge, there are two major issues regarding the primary controls of the stiff-grid-connected VSC working as a dc-voltage power port in the sense of nonlinear dynamics (see [12]–[15] and [20]–[28] and references therein). The first one includes the dynamics of the dc-side inductors coming into the picture from many sources; the second one is having a fault ride-through (FRT) capability

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in the event of severe voltage sags (or voltage dips) with a guaranteed power quality for all of the entities. This paper addresses the two aforementioned MI-AC/DC-MG's issues. Tackling those and simultaneously combining them with each other in order to have one comprehensive control methodology—considering the global stability—are regarded as the main contributions of this article and elaborated as follows.

- 1) Regarding dc-side inductors, they may be created by current source converters (CSCs) connected to the dc-side grid with an inductive dc filter (choke) [29] and [30], by advanced dc-hub configurations to connect several renewables to the dc grid, or even by Z-source converters which are linked to the dc grid via LC networks [31] and [32]. Thus, we should consider any types of load interfaced with the dc side. Indeed, VSCs can be connected to different entities, such as dc sources and dc loads with their front-end filters and converters on the dc side. As a result, the development of different types of loads/generators is adding energy-storing components to the VSC's dc side in the shape of an uncertain inductor/capacitor, and from the control perspective, the dc-side current has to be considered as a state of the new dynamic system if global stability is required.
- 2) Regarding the enhanced FRT ability, one of the most important concerns of VSCs is their power quality and stability during faults and possible voltage dip situations either in the ac side of dc-voltage power port VSC, which is responsible for controlling the dc-side voltage [14], or in the ac side of other VSCs connected to the dc energy pool while they are absorbing/injecting power from/into their own ac grids. In fact, if other VSCs connected to the dc energy pool of a multi-infeed ac/dc (or hybrid ac/dc) configuration are controlled in the conventional dq -frame, any asymmetric faults or harsh unbalanced conditions in their own ac-side voltage results in the appearance of the second harmonic oscillation on the dc energy pool voltage; this happens provided that the dc-voltage power port VSC is also controlled in the dq -frame. This phenomenon also occurs when an asymmetric fault or a harsh unbalanced condition appears on the ac-side voltage of the dc-voltage power port VSC [14]–[16], [33], and [34].

For the first above-mentioned issue, in order to take into account the effect of the inductor on the dc-voltage dynamics, there are two key approaches. The first one is modeling the dynamics by employing the energy balance equation across the equivalent capacitor of VSC; the second one is modeling the dynamics by using Kirchhoff's current law (KCL) around the aforementioned capacitor. Both approaches result in nonlinear dynamics. However, the first one is suffering from cascaded/nested control structure, where the current controller is the most inner control loop as pointed out in [16]. Also, it is shown in [17] that the first approach results in the linearized model, which is unstable/non-minimum phase around some operating points as a result of changes in the operating point (or equivalently equilibrium point) of the closed-loop dynamics. This means that the closed-loop dynamics highly demands an equilibrium-to-equilibrium maneuver capability—a required feature for controlling nonlinear dynamic system [16] and [35]. Because of the need for having and inducing such a capability,

the second modeling approach is a better method to tackle instability and improper transient performance issues (e.g., poor power qualities) related to linearizing a nonlinear plant around one operating point; see pieces of literature in the control discipline and power electronic systems [14]–[18]. As a result, the dc-side current of the grid-connected VSC is flowing through an uncertain inductor. Consequently, the load current has to be considered as one of the states of the whole dynamics, as it will be shown in this paper, which is playing a vital role in the performance of the stabilization of the dc-link voltage. Multi-infeed ac/dc modernized grids' issues associated with the required “augmented” power quality and the interaction between ac-side and dc-side dynamics were not fully covered; for example, the enhanced primary controls of converters based on dc-voltage power ports can facilitate the integration of microgrids (either ac or dc types) into the main ac grid and form an MI-AC/DC-MG, which is a new trend recently discussed and proposed by the industry—e.g., Pacific Gas and Electric Company (PG&E), etc. [36].

For the second aforementioned issue, the phenomenon is regarded as an “enhancement” of the stiff-grid-connected VSC with an FRT capability. The FRT feature is added to multi-infeed ac/dc systems by proposing a new topology, which is discussed in [37]–[38] and improves the FRT by employing hybrid multilevel VSC with ac-side cascaded H-bridge cells. The stated structure is good in power transmission systems, which transfer a high amount of power. However, the mentioned structure complicates the multi-infeed ac/dc system in medium power applications while we can achieve FRT capability using the enhanced control strategy without any changes in the present VSC's topology. Accordingly, in the mentioned applications, dual-sequence controllers using a dual-phase-locked loop (dual-PLL) were offered by other researchers for renewables, such as photovoltaic plants, for VSC-based hybrid ac/dc (or equivalently multi-infeed ac/dc) distributed generation systems, or even for HVDC systems on the one hand [33]–[34]. On the other hand, the application of such controllers imposes a kind of requirements for and/or conditions of the connection to the dc side of grid-connected VSCs. In other words, if we want to connect a new PQ-controlled VSC to the dc side of a system of VSCs all connected to a shared dc link, the controller of the new VSC should be augmented with a dual-sequence structure. This necessity complicated MI-AC/DC-MG operation, control, and utilization and demands that a new customer should have and follow additional conditions to make it connectable to the dc side (and hence a better power quality under some circumstances). In fact, this prevents future smart grids from having more flexible MI-AC/DC-MGs. Besides, although it is possible to apply a dc-voltage power port VSC with a dual-sequence controller that utilizes the sequence component of the grid voltage to generate the appropriate positive/negative sequence components of reference currents needed to attenuate dc-voltage ripple and to satisfy the negative-sequence active/reactive power requirements, simultaneously, we are not able to “fully” remove the second harmonic oscillation on the dc voltage yet [14], [15], and [34]. The reason is that active power (and hence the d -component of the positive sequence of dc-voltage power port VSC's current) is not an independent control input (i.e., the control lever from the control system's perspective) in grid-

connected VSCs [14]. On top of all of above-mentioned issues, dual-sequence controllers with dual-PLLs put more computational burdens on the digital controller of the VSC because of calculating the inverse of matrices.

Passivity-based controls are able to simultaneously maneuver all states of grid-connected VSCs to the associated equilibrium points with a global stability [39]. Therefore, it is significantly necessary that dc-voltage power port VSCs are equipped with comprehensive nonlinear controllers based on passivity stability dealing with the dynamics of the dc-side inductor and enhanced with and the FRT capability. Firstly, this paper presents the modeling of the stiff-grid-connected dc-voltage power port VSC employed in multi-infeed ac/dc power architecture considering an uncertain inductance at the dc side of the VSC. It is noteworthy that, in this paper, only the integration into stiff grids is investigated in order to remove the impacts of the weak grids on the VSC dynamics—which is not the main focus of this paper [40]. In other words, the short-circuit ratio (SCR) of the system under test is selected to be that of stiff grids, whose X_{grid}/R_{grid} is equal to 1, testing the equilibrium-to-equilibrium maneuver here [40]–[43]. Secondly, this paper proposes major improvements, which are required to employ a nonlinear control strategy and structure having: (1) easy implementation in digital hardware devices along with satisfactory transient performance during different harsh scenarios; (2) simultaneous, global stabilization of all states of the dynamic system; (3) induced robust performance under parametric uncertainties due to the inherent robustness of the variable-structure-based controller; (4) excellent dynamic and transient performance in terms of tracking and disturbance rejection around all operating points; (5) induced equilibrium-to-equilibrium maneuver property by using flat outputs in the control algorithm; and (6) the total harmonic distortion (THD) reduction and, as a consequence, reduction in the size of the passive filter required—which were not addressed and tackled in other research works [7]–[28]. Thirdly, this paper covers faults, which are not collapsing the whole dynamic system, so it complements the analysis and design proposed in previous research works by considering all possible scenarios of the fault to maintain the stability of the dc system while an ac fault takes place in “any” grid exchanging power with the dc-voltage power port VSC under test. In fact, this paper contributes to the enhancement of the FRT and the prevention of power quality distortion, as well as its propagation from one ac grid to others when there exists any kind of faults or poor power quality in one of the ac grids engaged in forming the whole electrical energy transfer system; thus, mathematical analyses and alterations required have to be rounded out. To this end, the closed-loop dynamics of the system will be extracted in this paper. Then, the FRT controller is investigated by considering the ac-side faults in two different places; the former is placed on the ac side of the dc-voltage power port VSC, and the latter is placed on the ac side of other VSCs contributing to the MI-AC/DC-MG. Indeed, the latter faults are differently affecting the whole dynamics and closed-loop system; hence, a different analysis is required. To include the dc-side inductor dynamics, as well as the enhanced FRT property, different parts of the nonlinear controller should fundamentally be altered and resynthesized. Therefore, Sections II–III cover novel, mathematical, theoretical analyses of the proposed controller; necessary

changes in mathematical models, along with enhancements of the controller, are also covered. Simulation results and experimental outcomes are fully presented in Sections IV–V, respectively, in order to show the effectiveness of the proposed controller structure. Finally, the conclusion is provided.

II. MODELLING STIFF-GRID-CONNECTED VSC

Fig. 1 shows the configuration of a typical, stiff-grid-connected VSC, whose important parameters considered in the mathematical model are also illustrated. Following the method proposed in [17] and employing energy balance across the capacitor, i.e., C_{eq} , end up (1) for the dynamics of the dc voltage link.

$$\tilde{V}_{DC} = \frac{as^2 + bs + e}{As^2 + Bs + E} \tilde{I}_d - (R_s + r_{on}) \frac{Dist(\tilde{I}_q, s\tilde{I}_q, s^2\tilde{I}_q)}{As^2 + Bs + E}, \quad (1)$$

$$- \frac{\tilde{P}_{loss}}{As^2 + Bs + E} - \frac{\tilde{P}_{ext}}{As^2 + Bs + E},$$

with the definitions provided below,

$$a \triangleq -1.5L_{DC-eq}L_s \frac{P_{DC-0}I_{d-0}}{V_{DC-nominal}^2},$$

$$b \triangleq -3L_{DC-eq}(R_s + r_{on}) \frac{P_{DC-0}I_{d-0}}{V_{DC-nominal}^2} - 1.5L_{DC-eq}L_s \frac{P_{DC-0}I_{d-0}}{V_{DC-nominal}^2},$$

$$- 1.5L_{DC-eq}V_{sd} \frac{P_{DC-0}}{V_{DC-nominal}^2} - 1.5L_s I_{d-0},$$

$$e \triangleq -3(R_s + r_{on})I_{d-0} - 1.5V_{sd},$$

$$A \triangleq L_{DC-eq}C_{eq} \frac{P_{DC-0}}{V_{DC-nominal}},$$

$$B \triangleq (C_{eq}V_{DC-nominal} - L_{DC-eq} \frac{P_{DC-0}^2}{V_{DC-nominal}^3}),$$

$$E \triangleq (\frac{2}{R_{Load}}V_{DC-nominal}),$$

where “~” indicates the perturbed signal around the equilibrium point of each variable; the subscript “-0” denotes the value of the variable; V_{DC} is the dc-link voltage; C_{eq} is the equivalent dc-link capacitance seen from the grid-connected VSC’s dc side, which includes the main dc-link capacitance and filter capacitance; L_{DC-eq} is the equivalent inductance of the dc-inductor, which may vary from the nominal value due to uncertainties; V_{ds} is the d -component of the voltage space vector at the point of common coupling (PCC); (I_d, I_q) are the dq components of the VSC output current; R_s is the equivalent ac-side filter resistance; r_{on} is the equivalent average conduction resistance of the IGBTs and their related diodes (we can say $R \triangleq R_s + r_{on}$ as elaborated in [15]–[18]); P_{ext} is the external power injected to the dc side; P_{loss} is the power losses in the converter circuit; i_{Loss} deals with the VSC total power losses (we can also replace it with a parallel resistance, i.e., R_p , modeling the VSC’s total power losses as detailed in [15]–[18] and [44]); L_s is the inductor associated with the ac-side filter; P_{DC-0} is the operating point of the net power injected/absorbed into/from the dc port of VSC, which is equal to the VSC ac-side terminal power, i.e., P_i ; $V_{DC-nominal}$ is the operating point value of the dc-link voltage; “*Dist*” is a function of the $\tilde{I}_q, s\tilde{I}_q$, and $s^2\tilde{I}_q$ signals; and $P_{DC-0} \triangleq 1.5(RI_{d-0}^2 + RI_{q-0}^2 + V_{sd}I_{d-0})$ —all fully described in [17].

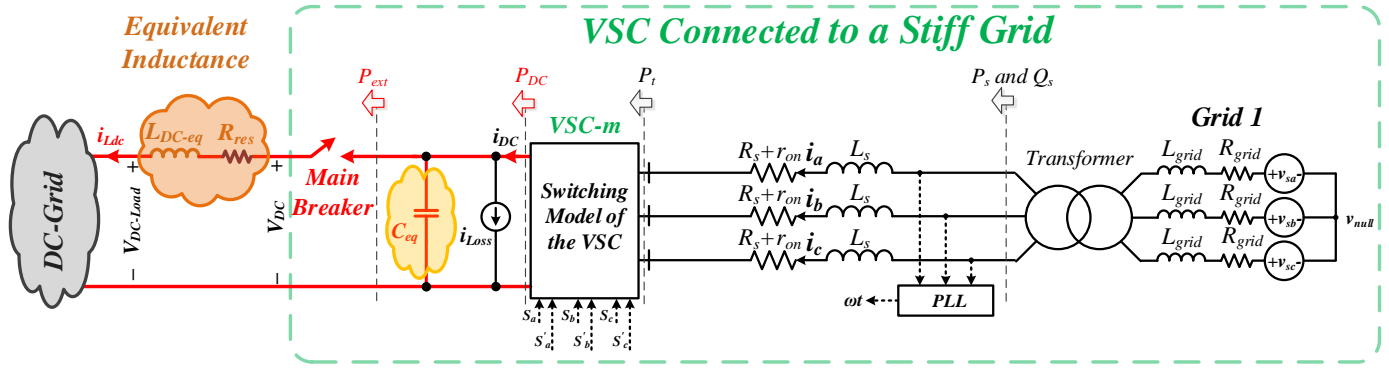


Fig. 1. The typical configuration of a stiff-grid-connected VSC as a dc-voltage power port with its important variables shown

Equation (1) reveals that considering L_{DC-eq} adds additional zeros and poles to the dynamics of the dc voltage compared to the dc-side dynamics extracted in [16] without including L_{DC-eq} . In this regard, [17] has mathematically proved and demonstrated that at different operating points and levels of the parametric uncertainties, the zero can lead to non-minimum phase dynamics, whereas the pole can be unstable; see Section III in [17]. Also, (1) is a cascaded structure in which the current controller is nested because of the fact that the structure is based on the commonly known current-controlled PWM-based VSC [19]. Consequently, it is not suitable to apply a nonlinear controller design to synthesize an enhanced controller on the one hand. On the other hand, the whole dynamics of the grid-connected VSC requires aggregating the load current flowing into an uncertain dc inductor L_{DC-eq} in the complete state-space representation of the total dynamic system. This demands that we apply Kirchhoff's current law (KCL) across the equivalent capacitor of a grid-connected VSC instead of employing an energy balance equation.

Applying a KCL across the equivalent capacitor C_{eq} results in (2), which contains all states of the whole dynamics in the abc -frame.

$$\begin{cases} L_s \frac{di_a}{dt} = -u_a V_{DC} - (R_s + r_{on})i_a + V_m \cos(\omega t), \\ L_s \frac{di_b}{dt} = -u_b V_{DC} - (R_s + r_{on})i_b + V_m \cos(\omega t - \frac{2\pi}{3}), \\ L_s \frac{di_c}{dt} = -u_c V_{DC} - (R_s + r_{on})i_c + V_m \cos(\omega t + \frac{2\pi}{3}), \\ \frac{dV_{DC}}{dt} = \frac{u_a}{C_{eq}} i_a + \frac{u_b}{C_{eq}} i_b + \frac{u_c}{C_{eq}} i_c - \frac{1}{C_{eq}} i_{Ldc} - \frac{V_{DC}}{R_{dc-Load}}, \\ L_{DC-eq} \frac{di_{Ldc}}{dt} = V_{DC} - R_{res} i_{Ldc} - V_{DC-Load}, \end{cases} \quad (2)$$

where—considering Fig. 1— i_a , i_b , and i_c are ac currents of the inductive output filter; from the standpoint of dynamics, $R_{dc-Load}$ is also able to model and includes the i_{Loss} (which is dealing with the VSC's total power losses associated with a given operating point) because of the fact i_{Loss} can be replaced with a passive resistance as elaborated in [15]–[18] and [44]; u_a , u_b and u_c are the general switching signals of the grid-connected VSC, i.e., switch position functions, which take value from the set $\{-1, +1\}$; V_m is the peak of the ac-side voltage; $i_{external}$ is the dc-current injected or absorbed from the dc-link; i_{Ldc} is the current flowing through L_{DC-eq} ; V_{dc} is the voltage across the capacitor;

$V_{dc-Load}$ is the voltage across the dc load; and the rest of the variables and parameters has been defined by (1). In (2), it is supposed that the reference phase angle and magnitude of three phase ac voltage are fed by a phase-locked loop (PLL) and grid-voltage measurements. Besides, by replacing $u_{a,b,c}$ with the average signal, $u_{ave_a,b,c}$, one can reach the average model of a grid-connected VSC using its switching model. In this case, u_{a_ave} , u_{b_ave} , and u_{c_ave} are bounded within the interval $[-1 +1]$. It should be pointed out that the dynamics of R_{res} , i.e., the filter damping resistor to suppress possible resonance in the dc-side LC -filter, has been neglected because of its infinitesimal value.

By making some convenient changes in (2) and using the chain rule for computing the derivative of state variables, we will then generate a “normalized” set of equations to make the problem independent of system parameters; this resulted in the normalized average model described by (3) and (4).

$$\begin{cases} \frac{di_{n_a}}{dt_n} = -u_{a_ave} V_{n_dc} - q i_{n_a} + \cos(\omega_n t_n), \\ \frac{di_{n_b}}{dt_n} = -u_{b_ave} V_{n_dc} - q i_{n_b} + \cos(\omega_n t_n - \frac{2\pi}{3}), \\ \frac{di_{n_c}}{dt_n} = -u_{c_ave} V_{n_dc} - q i_{n_c} + \cos(\omega_n t_n + \frac{2\pi}{3}), \\ \frac{dV_{n_dc}}{dt_n} = u_{a_ave} i_{n_a} + u_{b_ave} i_{n_b} + u_{c_ave} i_{n_c} - \frac{V_{n_dc}}{q_{dc-Load}} - i_{n_Ldc}, \\ \frac{L_{DC-eq}}{L_s} \frac{di_{n_Ldc}}{dt_n} = (V_{n_dc} - q_{res} i_{n_Ldc} - V_{n_dc_Load}), \end{cases} \quad (3)$$

with the definitions provided below,

$$\begin{cases} i_{n_a,b,c,Ldc} \triangleq (\frac{1}{V_m} \sqrt{\frac{L_s}{C_{eq}}}) i_{a,b,c,Ldc}, & q \triangleq (R_s + r_{on}) \sqrt{\frac{C_{eq}}{L_s}}, \\ V_{n_dc} \triangleq \frac{V_{DC}}{V_m}, & q_{dc-Load} \triangleq R_{dc-Load} \sqrt{\frac{C_{eq}}{L_s}}, \\ t_n \triangleq \frac{t}{\sqrt{L_s C_{eq}}}, & q_{res} \triangleq R_{res} \sqrt{\frac{C_{eq}}{L_s}}, \\ \omega_n \triangleq \omega \sqrt{L_s C_{eq}} \Rightarrow \omega t = \omega_n t_n, & \\ V_{n_dc_Load} \triangleq \frac{V_{DC-Load}}{V_m}, & \end{cases} \quad (4)$$

where subscript “ n ” indicates the normalized version of the variables expressed and defined in (2). It is noteworthy that the use of those changes makes all of the variables, including time, “unit less.” For example, it is noted that the voltages in the normalized system are being divided by the amplitude value of the ac-side source voltage, i.e., “ V_m .” Finally, the normalized voltages, currents, etc. are unit less. Using this state and input coordinate transformation on the average system (2), we easily obtain the normalized average model of (3) for all of the variables. Note that, in (3), there are four independent state variables of i_{n_a} , i_{n_b} , $V_{n_{dc}}$, and $i_{n_{Ldc}}$ as we have considered a three-wire system for the dc-voltage power port—and hence $i_{n_c} = -(i_{n_a} + i_{n_b})$ is employed thereafter once needed. The state-space model of the normalized nonlinear dynamic system can also be given by (5) and (6), which are using the formatting of the energy management expressions in [16] and the bilinear dynamic systems [45]. The general expression of the affine nonlinear dynamics of (5) and (6) using the matrices of “ f ,” “ g ,” and “ h ” is given in Subsection A in Appendix.

$$A \frac{dx_n}{dt_n} = (A_c + A_d)x_n + Bu_{ave} + v_n, \quad (5)$$

where, in (5), A is the diagonal matrix $\text{diag} [1, 1, 1, 1, \frac{L_{DC-eq}}{L_s}]$,

$$x_n = \begin{bmatrix} i_{n_a} \\ i_{n_b} \\ i_{n_c} \\ V_{n_{dc}} \\ i_{n_{Ldc}} \end{bmatrix}, \quad A_c(u_{ave}) = \begin{bmatrix} 0 & 0 & 0 & -u_{a_{ave}} & 0 \\ 0 & 0 & 0 & -u_{b_{ave}} & 0 \\ 0 & 0 & 0 & -u_{c_{ave}} & 0 \\ u_{a_{ave}} & u_{b_{ave}} & u_{c_{ave}} & 0 & -1 \\ 0 & 0 & 0 & +1 & 0 \end{bmatrix},$$

$$A_d(R) = \begin{bmatrix} -q & 0 & 0 & 0 & 0 \\ 0 & -q & 0 & 0 & 0 \\ 0 & 0 & -q & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{-q_{dc-Load}} & 0 \\ 0 & 0 & 0 & 0 & -q_{res} \end{bmatrix},$$

$$B = 0, \quad \text{and} \quad v_n = \begin{bmatrix} \cos(\omega_n t_n) \\ \cos(\omega_n t_n - \frac{2\pi}{3}) \\ \cos(\omega_n t_n + \frac{2\pi}{3}) \\ 0 \\ -V_{n_{dc-Load}} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - \frac{2\pi}{3}) \\ \cos(\omega t + \frac{2\pi}{3}) \\ 0 \\ -V_{n_{dc-Load}} \end{bmatrix}. \quad (6)$$

Referred to the energy management expressions, it should be mentioned that since matrix A_d is a function of R_s , r_{on} , and $R_{dc-Load}$ resistances—which are all “passive” circuit elements— A_d reflects and conveys the total losses of the dynamic system. However, since matrix A_c is a function of control inputs of $u_{a_{ave}}$, $u_{b_{ave}}$, and $u_{c_{ave}}$, A_c reflects a matrix associated with control inputs—which are all multiplied by states (and hence nonlinearity dynamics are accordingly generated). The aforementioned dynamics are also known as bilinear dynamic systems as they are, independently, linear in the control u and linear in the state variables x , but not in both. In other words, the dynamics only contain nonlinearities in the shape of the product of “ x_i ”s and “ u ”s, i.e., $x_i u$ [45]. Moreover, it should be

pointed out that although $B=0$ in (5) and (6), B has still been considered to preserve the generality of our problem formulations and to apply our methodology in other general cases. This can help the reader use the proposed approach in other application whose mathematical models include a non-zero “ B .”

The model given in (2) and (3) is a general model for the load, without any restriction. In this regard, we have considered a “general” Norton model (using Norton’s Theorem in circuit analysis with $-i_{Norton} = i_{external}$) of the dc grid connected to the dc side of the above-mentioned VSC, with added L_{DC-eq} and C_{eq} to cover all types of key, main loads including constant power loads, current source converters (CSCs) which create additional dynamics associated with their bulky dc inductors, fixed impedance loads, etc.

III. PROPOSED CONTROL STRATEGY FOR THE GRID-CONNECTED VSC

The structure employed for stabilizing the dc voltage of the stiff-grid-connected VSC discussed in this paper is shown in Fig. 2 to benefit from equilibrium-to-equilibrium maneuver feature of the control algorithm. For stabilizing the dc voltage considering the new model described through (6), the core block, i.e., flatness-based reference trajectory generation section, should be synthesized for the present problem and application. In addition, the section which is responsible for the generation of average control signals, i.e., passivity-based controller, should be altered for enhancing the FRT property in the mentioned structure to stabilize the dc voltage. The mentioned sections are dotted in red and blue color in Fig. 2, respectively, in order to show the parts that should be designed from the beginning.

A. Our Assumptions and Objectives for Synthesizing the Controller Proposed

In this paper, the term “global” stability does not refer to the entire MI-AC/DC-MGs’ states’ stability, and it means the “global” stability of the dc-voltage power port. Consequently, the proposed control design has aimed to make the primary control of *DC-Voltage Power Port VSC* as robust as possible, including the new dynamics of states and FRT capability. In addition, in this methodology, we are locally measuring all variables by high-bandwidth sensors with a reasonable frequency response—not through communications, etc. (i.e., communication-less algorithms)—for which we do not have to take into account the associated delay. Thus, it is noteworthy that there is “no” need to consider any communication-related delays in our proposed control design process as all variables are measured locally. As described by (2) and (3), the size of thin “bilinear” dynamic system in terms of the dimension of the state vector is four; in addition, we have disturbances affecting the dynamic system of the dc-voltage power port VSC in the shape of different loads and various types of faults. This control method is not based on a distributed control systems; power-wise, this control method has shown satisfactory transient performance for the medium-power, medium-voltage converters. Finally, from the standpoint of dynamics, i_{Loss} is replaced with a parallel passive resistance across the dc-voltage power port—modeling the existing losses discussed in [15]–[18] and [44]—so it is embedded in $R_{dc-Load}$.

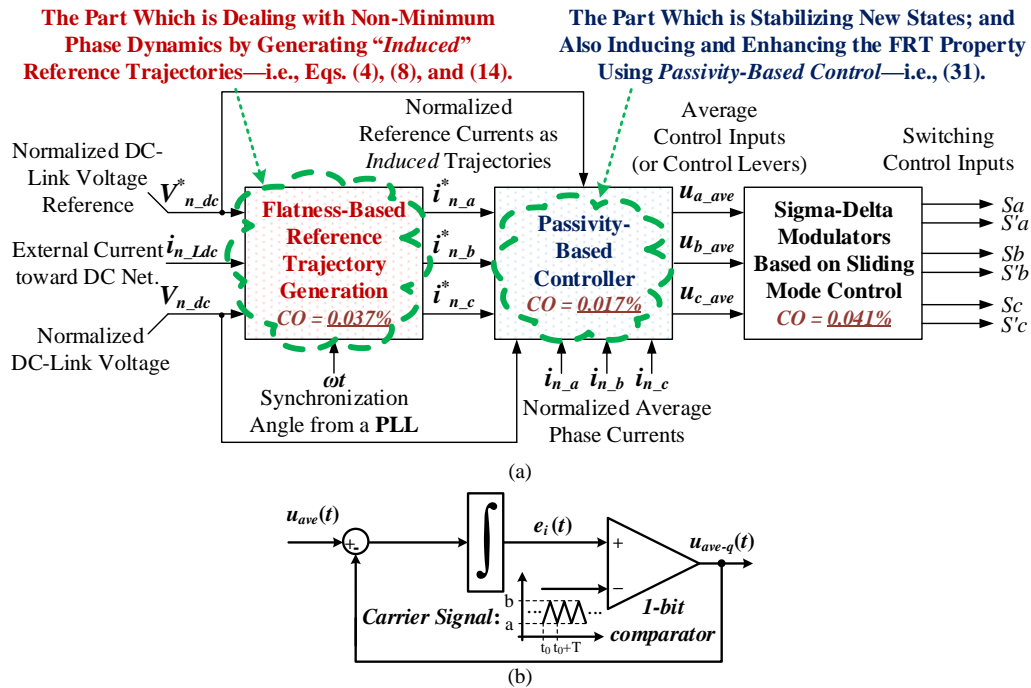


Fig. 2. The proposed primary control algorithm, which has been employed in the system shown in Fig. 1 including the computational overhead (CO) in percentage: (a) The enhanced nonlinear controller using (4), (8), (14), and (31); and (b) the Sigma-Delta Modulator based on the sliding mode control.

It is noteworthy that since our controller takes care of load changes by equilibrium-to-equilibrium maneuver capability, it simultaneously considers the i_{Loss} changes when VSC’s operating point changes.

Our control objectives are (1) an equilibrium-to-equilibrium maneuver capability, (2) global stability, and (3) robust transient performance while feeding high-demand loads with different dynamics for the dc voltage regulation using the dc-voltage power port in MI-AC/DC-MGs. The aforementioned tasks are very challenging when FRT feature is also taken into account, especially considering the non-minimum phase dynamics of the output of dc-voltage power ports. Having all of them in a single, comprehensive control methodology (or platform) is also considered in this article—which is also regarded as one of the integral contributions of this paper.

B. Our Proposed Controller—A Brief Review

Referred to Fig. 2, design efforts are primarily placed on synthesizing a feedback controller for the “indirect,” “induced” trajectory tracking problem—described now in terms of a corresponding desired trajectory for an alternative “minimum” phase output variable, such as the inductor current or the total stored energy. In other words, we resort to the “flatness” property in order to specify the required nominal state and input trajectories associated with our particular trajectory tracking problem. Thus, the proposed approach combines differential flatness, passivity-based controls, and sigma-delta modulation based on sliding mode controls, and it controls the minimum phase output variable. Finally, the passive output consideration of the exact tracking error dynamics allows for the state feedback which requires the nominal state trajectories and control inputs as data.

C. Flatness Property—A Brief Review

Briefly speaking, flatness in control system theories is a property of the system which is able to extend the notion of controllability from linear systems to nonlinear ones. A system is called “flat” system provided that the system has the flatness property. Flat systems have a flat output(s)—either physical or virtual (fictitious) ones. What is important is that they can be employed in explicitly expressing all states and inputs in terms of the flat output and a finite number of the flat output’s derivatives. To find the state trajectories, i.e., “ $x_{n\#}^*$ ”s, it is more convenient to use the flatness property of the nonlinear systems. Based on the flatness property, all parameters of the system can be completely and uniquely expressed by flat outputs, as well as a finite number of their derivatives; this facilitates finding the nominal inputs and states to have desired trajectories. This concept is very applicable to controlling non-minimum nonlinear systems since we can define the non-minimum dynamics with respect to minimum phase ones, which is employed in this paper (see [46]–[48] and references therein).

D. Passivity-Based Controls—A Brief Review

The essence of the passivity-based controllers is presented here. In passivity-based control design, the control input is synthesized such that the closed-loop system can be regarded as the negative interconnection of two dissipative subsystems and thus is an energy-based control. The controller should shape the energy of the system, and even change how energy flows inside the system. The key idea of passivity based controls is the use of the feedback so that the closed-loop system is a passive system. Thus, the energy function in the passivity-based controls can be regarded as an extension of the notion of Lyapunov function. Based on the Lyapunov stability

theory, we propose a desired time-varying trajectory for the linearized error dynamics state. This results in the need to inject damping into the desired system dynamics and to force the incremental energy (energy of the tracking error system) to be driven to zero by feedback. The methodology results in an output dynamic feedback controller which induces a “shaped” closed-loop energy and enhances the damping of the closed-loop system. For this reason, the method is better known as the “energy-shaping plus damping injection” methodology. The Lyapunov function of the total system is close to process the total energy, in the sense that it is the sum of a quadratic function. In classical control, it is quite well-known that passivity properties play a vital role in designing asymptotically stabilizing controllers for nonlinear systems [49]–[52].

E. System Integration for Implementing the Controller Proposed

In this part, we address how different parts are put together in order to implement the proposed primary controller. Referred to Fig. 2, this proposed primary control methodology is based on effectively changing the operating point of a VSC assigned to the dc-voltage power port. It works as the dc slack bus in a multi-infeed ac/dc grid when the power changes (also known as equilibrium-to-equilibrium maneuver), by means of the VSC primary controls. In this regard, considering making use of flat outputs—which are impactful because of existing non-minimum phase dynamics—the new operating points are calculated to feed the passivity-based controller—using (4), (14), and (8). The passivity-based controller’s task is making sure that the whole closed-system is stable in the average sense—using (31). Finally, as proved and shown by the first author in [16], sliding-mode-control-based sigma-delta modulations assigned to different phases are able to guarantee sliding regiments around the generated operating points for the phases “a,” “b,” and “c.” This means that the controller satisfies the “global” stability of the *DC-Voltage Power Port VSC* from control perspectives—as we have taken into account the large signal model of a VSC.

F. Synthesizing the States’ Reference Trajectories Generation for Including the Dynamics of L_{DC-eq}

The generation of signals u_{a_ave} , u_{b_ave} , and u_{c_ave} demands that new flatness-based trajectory equations are obtained in order to make new normalized reference state trajectories, i.e., $i_{n_a}^*$, $i_{n_b}^*$, and $i_{n_c}^*$. In the next stage, $i_{n_a}^*$, $i_{n_b}^*$, and $i_{n_c}^*$ are fed to the passivity-based controller to produce average control signals u_{a_ave} , u_{b_ave} , and u_{c_ave} (i.e., average switching signals/levers from control systems perspective). Then, they generate switching signals by feeding u_{a_ave} , u_{b_ave} , and u_{c_ave} through Sigma-Delta Modulators. The blocks associated with the flatness-based reference trajectory generation and the passivity-based control should accordingly be synthesized for the problem formulated here and the model employed in this paper (see [16] for the importance of each block); in this regard, the flat outputs are important to be updated in order to build u_{a_ave} , u_{b_ave} , and u_{c_ave} from $u_{a_ave}^*$, $u_{b_ave}^*$, $u_{c_ave}^*$, $i_{n_a}^*$, $i_{n_b}^*$, $i_{n_c}^*$, and $V_{n_dc}^*$. To this end, first, this subsection “reintroduces” the flat outputs and “regenerates” the reference state trajectories.

The counterpart of (15-a) in [16], i.e., (6) when satisfied with

nominal trajectories and nominal control inputs, is differentially flat with the following three flat outputs, i.e., $\{i_{n_a}^*$, $i_{n_b}^*$, $i_{n_Ldc}^*\}$. Thereby, (7) is obtained.

$$\begin{cases} \frac{di_{n_a}^*}{dt_n} = -u_{a_ave}^* V_{n_dc}^* - qi_{n_a}^* + \cos(\omega t), \\ \frac{di_{n_b}^*}{dt_n} = -u_{b_ave}^* V_{n_dc}^* - qi_{n_b}^* + \cos(\omega t - \frac{2\pi}{3}), \\ \frac{dV_{n_dc}^*}{dt_n} = u_{a_ave}^* i_{n_a}^* + u_{b_ave}^* i_{n_b}^* + u_{c_ave}^* i_{n_c}^* - i_{n_Ldc}^* - \frac{V_{n_dc}^*}{q_{dc-Load}}, \end{cases} \quad (7)$$

where variables with an asterisk are the normalized variables defined in (4) while they are all related to and associated with a specific given “equilibrium point.” In addition, it is noteworthy that the dc-side current i_{Ldc} in the steady state for different values of $R_{dc-Load}$ is modeled by $V_{DC} = R_{dc-Load} \times i_{Ldc}$ (or equivalently $V_{n_dc} = q_{dc-Load} \times i_{n_Ldc}$)—where $q_{dc-Load} = R_{dc-Load} \sqrt{\frac{C_{eq}}{L_S}}$ and $R_{dc-Load}$ models the equivalent resistance seen from the port with the V_{DC} voltage.

Equation (9) is obtained provided that flat outputs (8), i.e., $i_{n_a}^*$, $i_{n_b}^*$, and $V_{n_dc}^*$, are selected. It should be pointed out that (9) is taken into account in order to find a unique relationship between the reference trajectory of the output, i.e., $V_{n_dc}^*$, and the set of $\{i_{n_a}^*$, $i_{n_b}^*\}$ by considering the dynamics of the nominal average trajectories.

$$\begin{cases} i_{n_a}^* = I \cos(\omega t + \varphi), \\ i_{n_b}^* = I \cos(\omega t + \varphi - \frac{2\pi}{3}), \\ V_{n_dc}^* = \frac{V_{dc_energy_pool}}{V_m}, \end{cases} \quad (8)$$

where, as discussed, $i_{n_c}^* = -(i_{n_a}^* + i_{n_b}^*) = I \cos(\omega t + \varphi + \frac{2\pi}{3})$; ωt (which is equal to $\omega_n t_n$ based on (6)) is provided by a PLL—without having a cascaded, coupled dynamics with the whole dynamics— $I > 0$ is the amplitude value of the normalized reference state trajectories, i.e., $i_{n_a}^*$, $i_{n_b}^*$, and $i_{n_c}^*$; and $V_{dc_energy_pool}$ is the nominal voltage of the dc-voltage power port connected to the dc energy pool.

$$\begin{cases} \frac{di_{n_a}^*}{dt_n} = -u_{a_ave}^* V_{n_dc}^* - qi_{n_a}^* + v_{n_a}, \\ \frac{di_{n_b}^*}{dt_n} = -u_{b_ave}^* V_{n_dc}^* - qi_{n_b}^* + v_{n_b}, \\ \frac{di_{n_c}^*}{dt_n} = -u_{c_ave}^* V_{n_dc}^* - qi_{n_c}^* + v_{n_c}, \\ u_{a_ave}^* i_{n_a}^* + u_{b_ave}^* i_{n_b}^* + u_{c_ave}^* i_{n_c}^* = \frac{3I}{2V_{n_dc}^*} (1 - Iq). \end{cases} \quad (9)$$

Thereby, from (9) and (7), (10) is obtained.

$$\frac{dV_{n_dc}^*}{dt_n} = \frac{3I(1-Iq)}{2V_{n_dc}^*} - i_{n_Ldc}^* - \frac{V_{n_dc}^*}{q_{dc-Load}}. \quad (10)$$

As a consequence, one can obtain (11) due to the fact that $dV_{n_dc}^*/dt_n = 0$.

$$V_{n_dc}^* = -0.5i_{n_Ldc}^* + \sqrt{0.25i_{n_Ldc}^{*2} + 1.5I(1-Iq)q_{dc-Load}} \quad (11)$$

Furthermore, for the dc-side normalized current, one can obtain (12).

$$V_{n_dc}^* = q_{dc-Load} i_{n_Ldc}^* \quad (12)$$

where $i_{n_Ldc}^*$ is the normalized nominal value of i_{n_Ldc} associated with a specific given equilibrium point.

Afterward, (11) and (12) combine to conclude (13).

$$1.5I^2 q q_{dc-Load} - 1.5I q_{dc-Load} + (q_{dc-Load} + q_{dc-Load}^2) i_{n_Ldc}^{*2} = 0. \quad (13)$$

Finally, (14) is obtained, and it shows that using flat outputs (8), we will be able to generate the trajectories of minimum phase outputs (which are $i_{n_a,b,c}^*$) based on the non-minimum phase output of interest (i.e., V_{dc})—thus we are able to benefit from controlling “indirect,” “induced,” minimum phase outputs of $i_{n_a}^*$, $i_{n_b}^*$, and $i_{n_c}^*$ to control the non-minimum one.

$$I = \frac{1.5q_{dc-Load} - \sqrt{2.25q_{dc-Load}^2 - 6qq_{dc-Load}(q_{dc-Load} + q_{dc-Load}^2)\left(\frac{V_{n_dc}^*}{q_{dc-Load}}\right)^2}}{3qq_{dc-Load}} \quad (14)$$

Equation (14) takes care of generating the amplitude of the flatness-based reference trajectories (shown in Fig. 2), which is required to be synthesized for the problem formulation described in this article. In this article, Sigma-Delta modulators are exactly the same as the ones in [16], so they are not repeated here in order not to provide redundant information—see Fig. 4 and Subsections IV-D–IV-E in [16] for further information.

Now we need to “redesign” and “resynthesize” the passivity-based controller to induce and enhance the FRT property of the dc-voltage power port VSC as shown in Fig. 2. The next subsection has been allocated for this purpose.

G. Synthesizing the Controller for Enhancing Fault Ride-Through (FRT)

It should be pointed out that, in the context of control theories, FRT capability is generally called and defined as the fault-tolerant control to have a more reliable closed-loop dynamic system. Indeed, either the controller inherently induces the fault-tolerant property, which should be investigated, or the controller should be altered to have the same feature. Also, the fault-tolerant property supplements a robust feature of the controller due to the fact that the closed-loop dynamics withstand faulty situations and it is stable [54]. It is noteworthy that some types of faults may not be tolerable only by an FRT property added to the controller because of the nature of the fault itself. For example, the dc-side fault is not acceptable since it collapses the whole dc voltage. However, the system should be recoverable after dc fault removal, which is part of the FRT property here.

1) A Brief Discussion on the FRT Structure from the Control Perspective

For a given system, an input-output pair can be sketched for the fault-free and faulty system as the system behavior, whose exemplary, notional system input-output pair has been illustrated in Fig. 3 [54]. Also, different regions of performance have been demonstrated in Fig. 3. The structure of the general FRT control has been demonstrated in Fig. 4; the task of the FRT control is to recover the system behavior from degraded

performance to the required performance if possible.

The FRT can be regarded as a fault-tolerant property from control engineering perspective. From this point of view, there are two principal ways of fault-tolerant controller design, which are fault handling and control reconfiguration [54]. In this regard, Fig. 4 shows a typical, general structure of a system, which is controlled with FRT property. Referred to Fig. 4, we have to point out that the controller may also be able to induce the fault-tolerant property by itself. Consequently, “Fault Diagnosis” and “Controller Redesign” blocks are lumped into the “Controller” block in Fig. 4 since the controller is robust against fault, i.e., it is fault-tolerant.

2) Feedback Controller Design and Stability Analysis of the Closed-Loop System

This subsection presents the passivity-based control design strategy (shown in Fig. 2) for the stiff-grid-connected VSC system (shown in Fig. 1). Then, the globally asymptotic stability of the closed-loop system is rigorously ensured.

The open-loop dynamics of a general power electronic converter is described as follows.

$$A \frac{dx_n}{dt_n} = (A_c + A_d)x_n + Bu_{ave} + v_n, \quad (15)$$

where, as previously mentioned through (5) and (6), matrix A_d is associated with the total losses of the system, whereas A_c is associated with control inputs of the system—and hence A_c is a function of u_{ave} , i.e., $A_c = A_c(u_{ave})$.

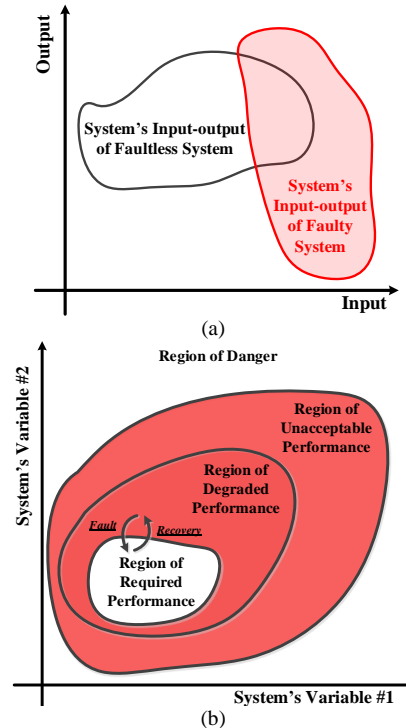


Fig. 3. The system input-output behavior for a general given system in (a) faulty and fault-free mode; and (b) fault-tolerant region with different levels of the danger.

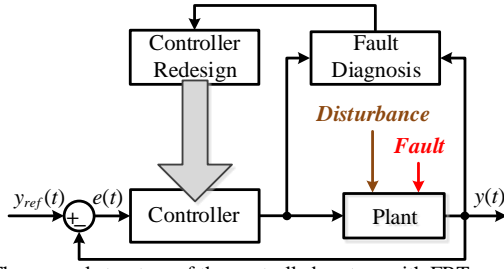


Fig. 4. The general structure of the controlled system with FRT property.

Now, it is supposed that $x_n^*(t_n)$ is the desired state trajectory, which can effectively be tracked using the nominal average control input $u_{ave}^*(t_n)$ in (15). Accordingly, (16) is obtained.

$$A \frac{dx_n^*}{dt_n} = (A_c + A_d)x_n^* + Bu_{ave}^* + v_n. \quad (16)$$

Defining the tracking error by equation $e = x_n - x_n^*$ results in (17) after straightforward mathematical manipulations—the derivation of (17) has been detailed in Subsection B in Appendix.

$$A \frac{de}{dt_n} = (A_c + A_d)e + B(u_{ave} - u_{ave}^*) + [A_c(u_{ave}) - A_c(u_{ave}^*)]x_n^*. \quad (17)$$

If one defines $e_{u_{ave}} = u_{ave} - u_{ave}^*$ and employs Taylor series expansion of A_c because of analytic, affine nature of A_c , (18) is reached for the error dynamics, whose matrix J is calculated based on the derivatives of A_c with respect to u_{ave} .

$$A \frac{de}{dt_n} = (A_c + A_d)e + Be_{u_{ave}} + Je_{u_{ave}}. \quad (18)$$

It is worth pointing out that the nonlinear part of the error dynamics is conservative and that the control input vector is now a time-varying vector depending upon the desired state trajectory. Consequently, if the Hamiltonian form is adopted using the Hamiltonian function $H(e) = 0.5e^T e$, (19) can be obtained. Equation (18) can be rewritten as

$$A \frac{de}{dt_n} = (A_c + A_d)e + B^*e_{u_{ave}}, \quad (19)$$

where $B^* = B + J$.

The following Theorem is provided to develop a feedback controller based on passivity-based control such that the system (19) in closed-loop with the developed controller is globally asymptotically stable.

Theorem 1. *Let the passive measurement output of system (19) be*

$$e_y = B^*e. \quad (20)$$

*Choose a control gain $K = \text{diag}[k, k, k]$ —with $k > 0$ —such that the matrix $[-A_d + B^*K(B^*)^T]$ is positive definite. Then, the origin of the system (19) in closed-loop with the control input*

$$u_{ave} - u_{ave}^* \triangleq e_{u_{ave}} = -Ke_y, \quad (21)$$

is asymptotically stable.

Proof. Define a Hamiltonian function $H(e) = 0.5e^T e$. The closed-loop system (19) with (21) can be described by

$$\frac{de}{dt_n} = A^{-1}A_c e + A^{-1}[A_d - B^*K(B^*)^T]e. \quad (22)$$

The derivative of H along the trajectory of (22) is as follows.

$$\begin{aligned} \frac{dH(e)}{dt_n} &= \frac{1}{2} \left(\frac{de^T}{dt_n} e + e^T \frac{de}{dt_n} \right) = \\ &= \frac{1}{2} e^T (A_c^T A^{-1} + A^{-1}A_c) e + e^T A^{-1} [A_d - B^*K(B^*)^T] e \\ &\quad - e^T A^{-1} [-A_d + B^*K(B^*)^T] e. \end{aligned}$$

Since matrix A is diagonal and positive definite, the derivative of H is negative definite if the matrix $[-A_d + B^*K(B^*)^T]$ becomes positive definite. Based on the Lyapunov stability theory, the origin of the system (19) with (21) is asymptotically stable if K is chosen such that (23) is guaranteed, i.e., $[-A_d + B^*K(B^*)^T]$ becomes positive definite.

$$[-A_d + B^*K(B^*)^T] > 0, \quad (23)$$

The proof is thus completed—note that after elaborating *Theorem 2* in the next subsection, we will prove that (23) is true and met for the dynamics of our system model in Subsection C in Appendix. \square

Remark 1. *The feedback controller design of (21) is essentially based on passivity-based control where the Hamiltonian function serves as a radially unbounded positive definite storage function. And the closed-loop system (19) with (21) is passive.*

Remark 2. *Note that $-A_d$ reflects and conveys the total losses of the dynamic system because of the fact that all arrays of $-A_d$ are related to $(R_s + r_{on})$ and $R_{dc-Load}$, etc., which are all positive definite values.*

The following technical result is to show the tracking ability of the system (15) with controller (21).

Corollary 1. *Under the control input (21), the state of system x_n (15) asymptotically converges to the desired state x_n^* in (16).*

Proof. From *Theorem 1*, one can that the closed-loop error system is asymptotically at the origin. This immediately implies that $\lim_{t \rightarrow \infty} e(t) = 0$, which is equivalently $\lim_{t \rightarrow \infty} x_n(t) = x_n^*$ for any initial conditions. The proof is thus completed. \square

3) Feedforward Controller Design for Tolerating Faults on AC Side of DC-Voltage Power Port

So far, it is supposed that there are no faults on the ac side of the VSC. If it is required that the system is fault tolerable against a fault on the ac side of dc-voltage power port VSC, the controller in (21) has to be able to stabilize the closed-loop dynamics in case of a faulty situation. To make the controller fault tolerable, and hence the whole dynamics, it is a must to derive the error dynamics in the case of fault scenarios when the controller in (21) is commanding control signals, and then, the required changes should be investigated to be added to (21).

In fact, in faulty situations on the ac side, (15) will be changed to (24), accordingly.

$$A \frac{dx_n}{dt_n} = (A_c + A_d)x_n + Bu_{ave} + v_{n_Fault}. \quad (24)$$

where v_{n_Fault} is the “new” voltage signals appearing on the ac side of VSC because of the presence of the fault on that point. However, all control signals, which also include (16), are generated based on the fault-free situation. As a result, based on the faulty situation, (19), and the controller previously synthesized for the fault-free scenarios, the error dynamics in (17) is altered to the following new error dynamics, i.e., (25).

$$A \frac{de}{dt_n} = (A_c + A_d)e + B^*e_{u_{ave}} + (v_{n_Fault} - v_n). \quad (25)$$

Consequently, all equations including $H(e)$ will depend on the $v_n - v_{n_Fault}$ vector, and it is “not” possible to have a negative definite function $dH(e)/dt_n$, because of the aforementioned vector, if (21) is purely employed in the closed-loop system.

To solve this problem and make the controller fault-tolerant, a feedforward-feedback controller is developed as follows.

$$e_{u_ave_Fault-Tolerant} = -K e_y + K_{Fault} (v_n - v_{n_Fault}). \quad (26)$$

The following Theorem shows the stability of the closed-loop system (25) with (26).

Theorem 2. Choose a feedback control gain K such that $[-A_d + B^* K (B^*)^T]$ is positive definite, and a feedforward control gain

$$K_{Fault} = \begin{bmatrix} \frac{1}{V_{n_dc}^*} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{V_{n_dc}^*} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{V_{n_dc}^*} & 0 & 0 \end{bmatrix}. \quad (27)$$

The origin of the system (25) in closed-loop with (26) is globally asymptotically stable.

Proof. The closed-loop error system (25) and (26) can be written by

$$\begin{aligned} A \frac{de_{Fault-Tolerant}}{dt_n} = & \\ A_c \frac{\partial H(e_{Fault-Tolerant})}{\partial e_{Fault-Tolerant}} + & \\ [A_d - B^* K (B^*)^T] \frac{\partial H(e_{Fault-Tolerant})}{\partial e_{Fault-Tolerant}} + & \\ B^* K_{Fault} (v_{n_Fault} - v_n) + (v_{n_Fault} - v_n), & \end{aligned} \quad (28)$$

where K_{Fault} , in general, is a matrix taking care of faulty situations once $v_n - v_{n_Fault}$ vector is not zero.

Based on (28), condition (29) has to be met and satisfied in order to have a fault-tolerant closed-loop dynamic system in case of the ac-side fault since the time derivative of new $H(e)$ is again negative definite (and hence Lyapunov stability criterion is satisfied).

$$B^* K_{Fault} (v_{n_Fault} - v_n) + (v_{n_Fault} - v_n) = 0. \quad (29)$$

Considering (19), for the stiff-grid-connected dc-voltage power port shown in Fig. 1 and expressed by (5) and (6), (30) reveals the matrix B^* associated with the aforementioned configuration.

$$B^* = \begin{bmatrix} -V_{n_dc}^* & 0 & 0 \\ 0 & -V_{n_dc}^* & 0 \\ 0 & 0 & -V_{n_dc}^* \\ i_{n_a}^* & i_{n_b}^* & i_{n_c}^* \\ 0 & 0 & 0 \end{bmatrix}. \quad (30)$$

Therefore, one possible K_{Fault} , which is able to satisfy condition (29) has been written in (27). Based on *Theorem 1*, one can check that the system (28) is globally asymptotically stable at the origin. The proof is thus completed. \square

Remark 3. It is noteworthy that K_{Fault} acts as a feedforward control gain to reject the disturbance while K is a feedback

control gain. The internal stability is guaranteed by the condition (23). Instead of requiring the system to be controllable, we require a relaxed condition, i.e., “stabilizability.” Therefore, we can always find a K such that (23) holds, which attests to the stabilizability of the system.

Finally, as shown in Fig. 2, the passivity-based controller (31) has been synthesized in order to make the control structure fault-tolerant. It should be pointed out that, according to previous discussions, (9) and (14) have been designed in order to include and stabilize the additional dc-side inductor’s dynamics, which have not been considered in the previous research works related to MI-AC/DC-MGs “with” global stability and “without” cascaded control structures (see [7]–[28] and references therein).

$$\begin{cases} u_{a_ave} = u_{a_ave}^* - k(-V_{n_dc}^* i_{n_a} + V_{n_dc}^* i_{n_a}^*) + \frac{1}{V_{n_dc}^*} (v_{n_a_Fault} - v_{n_a}), \\ u_{b_ave} = u_{b_ave}^* - k(-V_{n_dc}^* i_{n_b} + V_{n_dc}^* i_{n_b}^*) + \frac{1}{V_{n_dc}^*} (v_{n_b_Fault} - v_{n_b}), \\ u_{c_ave} = u_{c_ave}^* - k(-V_{n_dc}^* i_{n_c} + V_{n_dc}^* i_{n_c}^*) + \frac{1}{V_{n_dc}^*} (v_{n_c_Fault} - v_{n_c}). \end{cases} \quad (31)$$

Regarding fault-tolerant terminology, (15) describes the constraint and system structural equations of the system under test. Also, $v_{n_a,b,c_Fault} - v_{n_a,b,c}$ terms identify the ac-side fault of the dc-voltage power port VSC. Otherwise, it is zero, and (31) also adds a stabilizing control signal during the faulty situation by means of the last term expression written in (31). In other words, fault signals, i.e., $v_{n_a,b,c_Fault} - v_{n_a,b,c}$ terms, identify the presence of a fault, and it activates appropriate “stabilizing” signals, autonomously, which amount to the FRT property of the synthesized controller [54].

Remark 4. It is noteworthy that, as proved previously, any positive constant k (i.e., $k > 0$, regarded as the design parameter) satisfies the passivity-based condition (or equivalently Lyapunov stability criteria). The time response of the dynamic system from the standpoint of the transient performance is able to help the designer select the most appropriate k value. In other words, this paper has not focused on selecting the “optimal” value of k in a systematic fashion as it is out of the scope of this research. Also, this article has proved that the global stability of the closed-loop system with the proposed control is rigorously guaranteed—but this does not make any comments on the robust performance at all.

Based on *Remark 4*—by means of Fig. 10 in Section IV, which is simulating the whole dynamic system—it will be shown that we will be able to choose the value of k which is resulting in the best performance from the standpoint of number or oscillations, settling time, etc.

4) Closed-Loop Dynamics of DC-Voltage Power Port VSC in Case of Fault on the AC Side of Other VSCs Connected to DC-Voltage Power Port

So far, it is supposed that there is no fault on the ac side of other VSCs controlled in the dq -frame (e.g., see PQ-controlled VSCs discussed in [14], [15], and [19]) with augmented dual-sequence controllers as detailed in [33]–[34]. In case of the appearance of any faults on the ac side of those converters, the reflection of power on their dc side is the oscillating power with the second harmonic of the ac power frequency; see [14] and

[15]. Thus, based on the model we have provided by means of (3)–(11) in Section II, the second-harmonic oscillating power, which is seen from the dc side of a dc-voltage power port VSC, can be regarded as a variable resistance with the doubled frequency of their main grid’s frequency if it is modeled as passive elements considering the feeding dc-side current and stabilized dc voltage. As a result, it has to be investigated whether or not (22) is stable with the controller in (21) in the case of variable resistance with the double frequency of the ac-grid frequency of other PQ-controlled VSCs. It is only required that (23) is satisfied when the resistance is variable with the stated frequency. Since there is no condition on $q_{dc-Load}$ such that the condition of (23) in met, (23) is also satisfied when having a variable resistance with the aforementioned frequency. Regarding the definition of the “fault-tolerant” terminology [54], the primary controller will automatically be reacting to any faults appearing on the ac side of other VSCs connected to dc energy pool, since it is able to regulate and stabilize the dc voltage during the existence of time-varying sinusoidal resistance with the double ac-side frequency. Consequently, it is not required that the controller of either dc-voltage power port VSC or other VSCs is augmented with any dual-sequence strategy or protocol to have FRT property during faults as reported and needed in [33]–[34]. Besides, as discussed in Subsubsection III-D-1, this structure is a fault-tolerant system by itself, so there will be no need for the separation of “Fault Diagnosis” and “Controller Redesign” blocks—they all are lumped into the “Controller” block.

IV. SIMULATION RESULTS

Fig. 5 has been simulated using the MATLAB/Simulink environment as a multi-infeed ac/dc modernized power system. The detailed switching model of the dc-voltage power port VSC, in Zone I, and the dc/dc converter, in Zone III, are used in the simulation for better accuracy. Thus, we can test the control performance of the dc-voltage power port VSC under typical high-frequency disturbances of switching-based loads, such as dc/dc converters. However, the average model of the VSC in Zone II is used to reduce the computational burden without loss of accuracy. Also, Zone II is simply controlled by PWM-based voltage-oriented controllers and works as a *Constant P/Q Active Load*, which takes care of constant power loads. Zone III mimics a *Battery Energy Storage System* which takes care of both charging and discharging modes forcing Zone I responds to its demands and thus changes its operating point and goes through the equilibrium-to-equilibrium maneuver. In Zone III we also have fixed impedance dc loads, so the system under test includes all of the important, key scenarios to test, evaluate, and examine the proposed controller. The system parameters are given in Appendix. Parameter k is selected based on the plant’s parameters to satisfy $-1 < u_{a,ave} < +1$, $-1 < u_{b,ave} < +1$, and $-1 < u_{c,ave} < +1$; accordingly, $k=0.1$ satisfies the aforementioned limits, and it also provides an acceptable convergence rate as verified by simulation results. The effect of k variation is also simulated at the end of this section. The switching frequency is selected to be 10 kHz for the simulation section. Several scenarios and events have been considered and simulated to assess the transient performance of the proposed voltage control scheme. The key results associated with

different fault-free and faulty events are reported as follows—for both proposed nonlinear controller and linearized model-based linear controls.

A. Event Category-A Using the Proposed Nonlinear Control

Category-A Event—first, we consider healthy, normal, fault-free operation of Fig. 5 in order to test the controller response to the newly added dynamics associated with the dc-side inductor. To this end, the dc energy pool is energized from its initial zero states by a ramp function which starts from zero at $t=0.00$ s to its final value (i.e., 1,500 V) at $t=0.50$ s—which is testing the dc-voltage power port VSC’s equilibrium-to-equilibrium maneuver capability. Then, Zone II is connected to the dc energy pool at $t=1.00$ s with zero active and reactive power. At $t=2.00$ s, in order to examine our controller’s performance, capabilities, and abilities to recover the dc voltage, Zone II is abruptly (i.e., *without* any slew rate, which is equivalent to about 20 MW/s) commanded to absorb 0.50 MW/0.00 var from its ac grid and to inject to the dc energy pool. This results in the rise time of 0.07 s associated with the actual active power. Thus, the dc-voltage power port VSC is working as an inverter and is therefore injecting active power to its ac grid. At $t=3.00$ s, Zone II is abruptly commanded to work in reverse, i.e., to absorb 0.50 MW/0.00 var from the dc energy pool and to inject to its ac grid. This results in the rise time of 0.14 s associated with the actual active power. Thus, the dc-voltage power port VSC is working as a rectifier and is therefore absorbing active power from its ac grid—it should be pointed out that the dynamics of VSC in the rectification more differs from those in inversion mode and that is why they look different [14]–[19]. Zone II is again abruptly commanded to absorb 0.50 MW/0.00 var from its ac grid and to inject to the dc energy pool at $t=4.00$ s, and within this period, it is commanded to inject 0.50 Mvar to its ac grid at $t=5.00$ s. This results in the rise time of 0.14 s associated with the actual active power. Hence, after $t=5.00$ s, Zone II is absorbing 0.5 MW from its ac grid and is injecting 0.50 Mvar to its ac grid. The transient performance of the dc-link voltage of the dc-voltage power port VSC is shown in Fig. 6-(a). At $t=6$ s, the interlocked switch shown in Fig. 2 changes its position, so Zone III is commanded to absorb 0.49 MW from the dc energy pool. Afterward, Zone III is commanded to inject 0.86 MW to the dc energy pool at $t=7.00$ s, and the battery energy storage system (BESS) will finally reach that amount of power at $t=7.58$ s, according to its dynamics.

Fig. 6-(a) shows the excellent tracking and disturbance rejection performances of the proposed controller where the recovery time is around 0.25 s, and dc-link voltage quality during variations in the power direction is very good from overvoltage and undervoltage perspectives. Fig. 6-(b) shows the active and reactive power responses of Zone II whereas Fig. 7-(a) shows the average control effort of the proposed controller. Fig. 7-(b) shows the power supplied to Zone III, i.e., the BESS. It should be pointed out that Fig. 6 and Fig. 7, during *Category-A Events*, also include the response of the dc energy pool to the connection of the VSCs directly tied to the dc link.

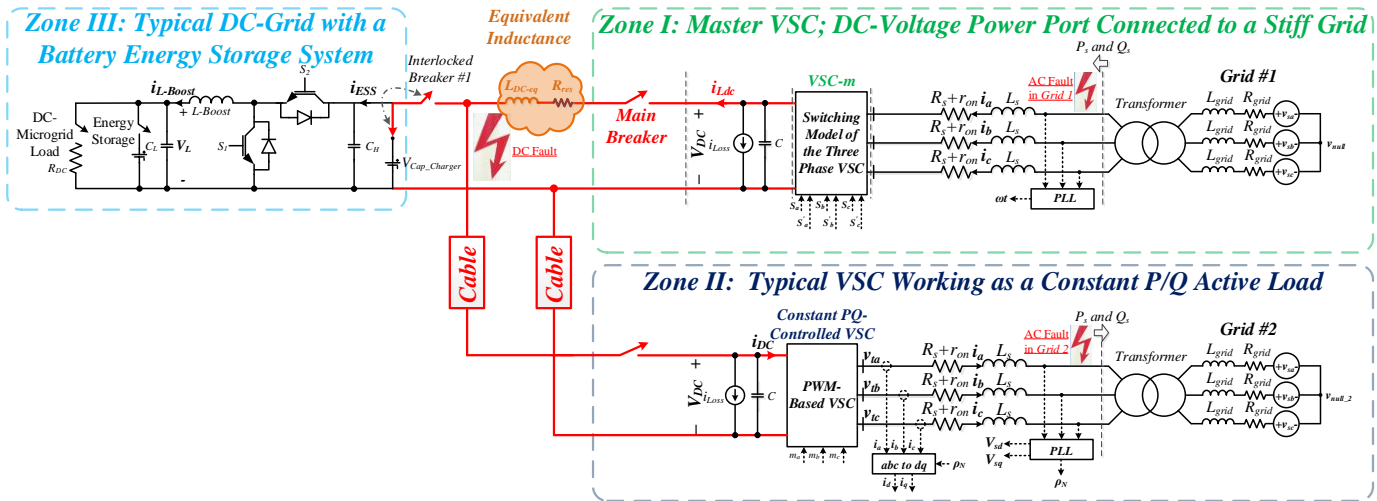


Fig. 5. The multi-feed ac/dc power system under test for simulation results.

Thus, this will also affect the effective dc-link capacitance of dc-voltage power port VSC. In other words, we have simulated a circuit which has uncertainties compared to the parameters employed in the controller proposed. To do so, the parameters used for setting up the controller proposed, (i.e., the parameters employed in (4), (8), and (14)—for the **Flatness-Based Reference Trajectory Generation**—and employed in (31)—for the **Passivity-Based Controller**—which are all shown in Fig. 2-(a)), are selected from Table I in Subsection D in Appendix; this leads to 36.50% uncertainty in the value of the dc-side filter’s parameters, e.g., C_{eq} . Although there exists high amount of uncertainties taken into consideration for simulating the response, the good outcome of this paper contribution is that the proposed controller still shows enough robust stability against this parametric uncertainty. The ringing shown in Fig. 6-(a) is because of so. In this regard, Fig. 8 has shown the effect of C_{eq} uncertainty on the dc voltage; Fig. 8 also reveals that the global stability of the closed-loop system with the proposed control is rigorously guaranteed. Moreover, as shown, there are significant active power exchange between ac and dc grid in order to test the effectiveness of the equilibrium-to-equilibrium maneuvering capability proposed.

The overshoot/undershoot seen in Fig. 6-(a) has been generated by the very large amount of active power demanded by the *Constant PQ Active Load* (therefore it is regarded as an extremely large unmodeled disturbance for which we don’t have observer here). The undershoot/overshoot has indeed caused by the active power changes of the *Constant PQ Active Load*, whose power is commanded to change from ± 0.5 MW to ± 0.5 MW—without any slew rate which is equivalent to 20 MW/s—which is not a practical case in the industry at all and just been applied here in order to reveal our controller’s performance, capabilities, and abilities to recover the dc voltage. As regards this, Fig. 9 has shown the output dc voltage for more real, practical cases, in which the active power changes by ramp functions and slew rate controls—the slew rate of 3.08 MW/s has been applied here just as an example. Fig. 9 reveals that the amount of undershoot/overshoot (as well as the ringing) is within a very acceptable range (and therefore is very negligible).

Parameter k affects the transient performance related to the time response of the states converging to their associated

nominal signals. As a result, k affects the transient performance of the dc-side voltage. The effect of variations on k has been simulated, and accordingly, Fig. 10 reveals the effect of changes in k on the entire previous designed event. As previously mentioned in *Remark 4*, the time response of the dynamic system from the standpoint of the transient performance is able to help the designer select the most appropriate k value—looking at the transient performance shown in Fig. 10, we have selected k value to be equal to 0.1.

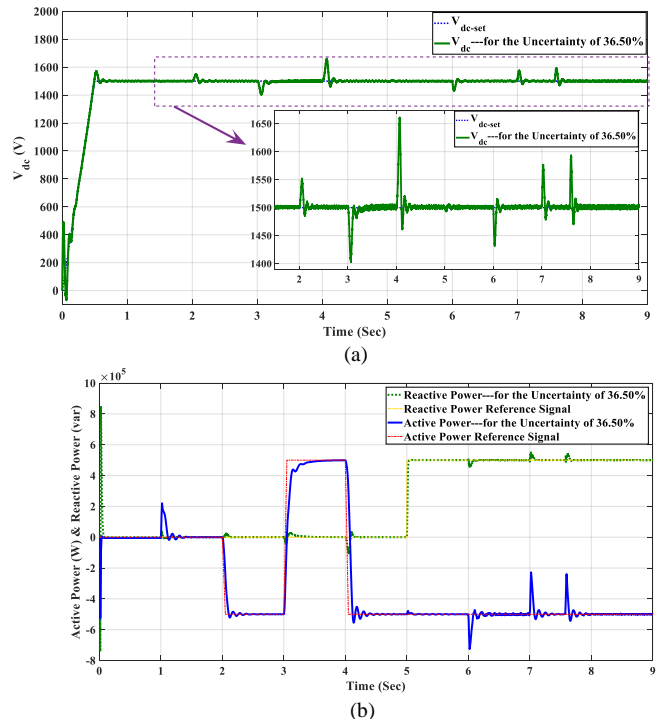


Fig. 6. The response of the dc-voltage power port VSC to *Category-A* Events with abrupt power changes to test the controller ability to recover the dc voltage and its performance: (a) output dc voltage, its reference signal, and its enlarged view; and (b) variations in the active and reactive power when Zone II is commanded to change its demand *without* any slew rate, which is equivalent to 20 MW/s here (and hence significant changes in the active power of the dc-voltage power port in order to examine the effectiveness of the equilibrium-to-equilibrium maneuvering capability proposed).

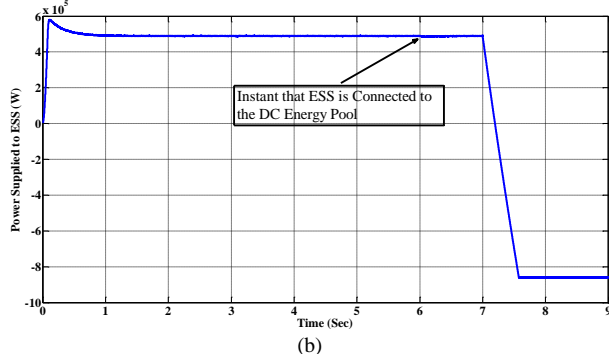
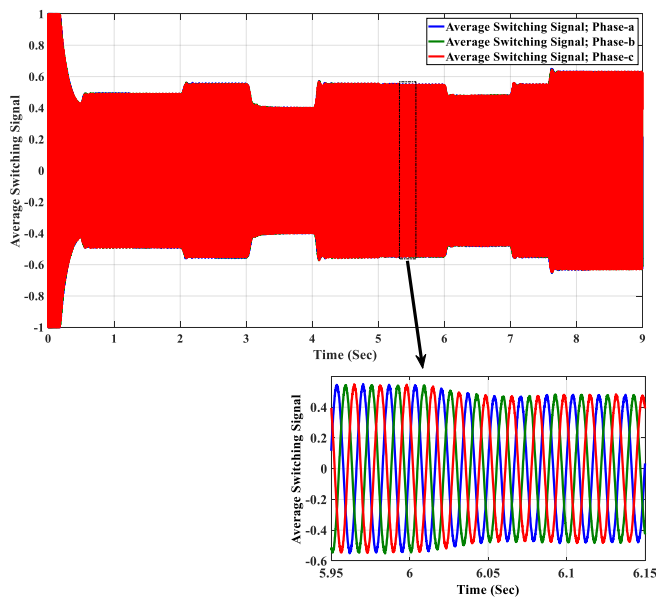


Fig. 7. The response of the dc-voltage power port VSC to *Category-A* Events shown in Fig. 6: (a) control inputs, i.e., average switching signals (control levers) including an enlarged view for the time window of $5.95 < t < 6.15$; and (b) power supplied to the battery energy storage system; it is connected to the battery energy storage system at $t=6$ s via an interlocked switch.

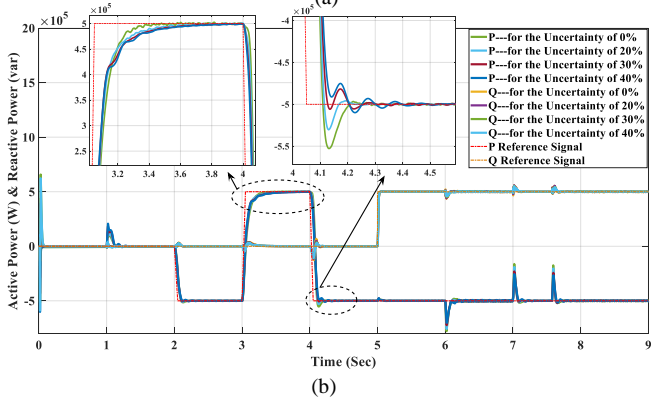
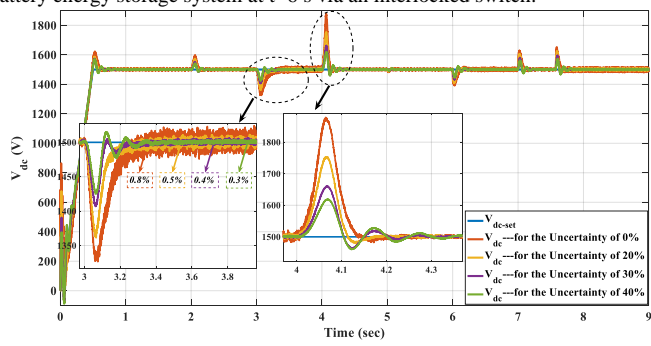


Fig. 8. The response of the dc-voltage power port VSC to *Category-A* Events with abrupt power changes to test the controller ability to recover the dc voltage and its performance—Zone II is commanded to change its demand *without* any slew rate, which is equivalent to 20 MW/s here—and with different percentage of uncertainties in C_{eq} : (a) output dc voltage, its reference signal and its enlarged views; and (b) variations in the active and reactive power when Zone II change its demand and its enlarged views.

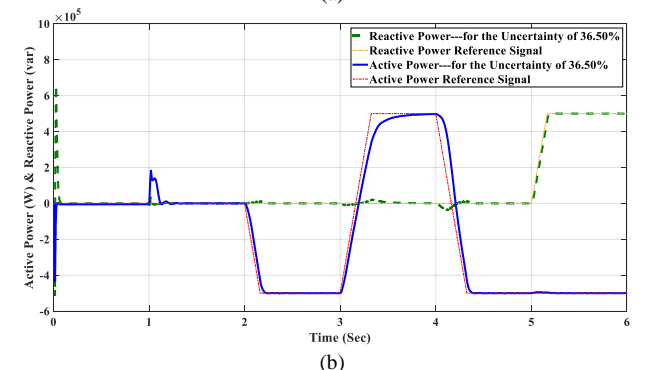
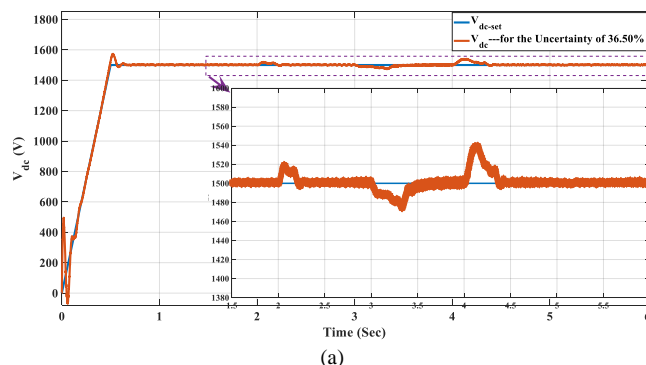


Fig. 9. The response of the dc-voltage power port VSC to *Category-A* Events (only related to the *Constant PQ Active Load*) with power changes in more real, practical cases: (a) output dc voltage, its reference signal, and its enlarged view; and (b) variations in the active and reactive power when Zone II is commanded to change its demand *with* the slew rate of 3.08 MW/s (and hence significant changes in the active power of the dc-voltage power port in order to examine the effectiveness of the equilibrium-to-equilibrium maneuvering capability proposed).

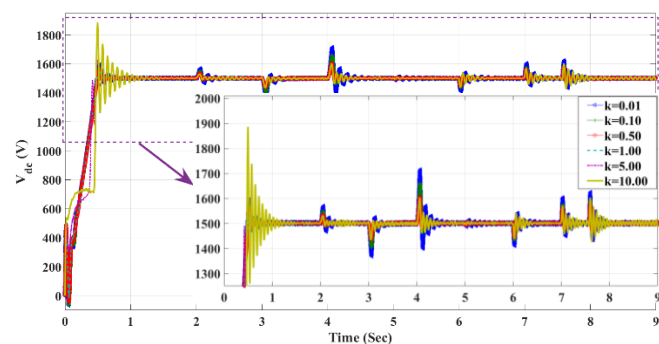


Fig. 10. The effect of changes in k on the dc-link voltage: dc voltage and its reference signal, in addition to its enlarged view— k varies from 0.01 to 10.00 as shown by the legend.

B. Comparison of Event *Category-A* Using Linearized Model-Based Linear Control

For comparison, the structure shown in Fig. 5 has been simulated with the PI-lead controller mentioned in [15] and [16]. Here, the transient performance of the dc voltage and the “signal spectrum” of the ac-side current have been simulated and compared with those of the proposed nonlinear

controller—Fig. 11 and Fig. 12 demonstrate the simulation results. Fig. 11 demonstrates that the linearized model-based linear controller is not able to successfully perform equilibrium-to-equilibrium maneuver since the controller has been designed for the “linearized model” with a current-controlled PWM-based VSC. Therefore, unmodeled dynamics show up and deteriorate the transient performance of the dc voltage. Contrary to the proposed controller, Fig. 11-b shows poor transient performance, especially for tracking the V_{dc-set} ramp and the transients; oscillations with the frequency of about $\frac{1}{0.064} = 15.63$ Hz; the overshoot of about 6.33%; the undershoot of about 9.07%; and the duration of about 0.356 s will take place because of the aforementioned shortcomings. Additionally—for the same ac-side filter—Fig. 12 has shown that the proposed nonlinear controller results in a much less total harmonic distortion (THD) of the ac-side current, i.e., 0.64% and 16.09% for the proposed controller and the linear one, respectively. This reveals that THD is almost 25 times less for the proposed controller. Consequently, if the same amount of THD is expected, we can achieve a much higher reduction in the size of the required passive filter for the proposed controller compared to that in the linear one.

C. Event Category-B Using the Proposed Nonlinear Control

Category-B Events—second, we consider the faulty operation of Fig. 5 to examine the controller response to different, possible faults associated with the ac-/dc-side grids formed in Fig. 5. To this end, the structure shown in Fig. 5 has been simulated with the fault-tolerant controller proposed in this paper. First of all, the impact of dc faults with different duration is investigated to check the capability of the controller for “riding through” dc faults with different time intervals or, equivalently, to check the dc-fault-tolerant property of the controller. Fig. 13 demonstrates the mentioned feature. Moreover, the structure shown in Fig. 5 has to be tested for ac-side faults in either ac *Grid 1* or ac *Grid 2* although the second one, i.e., ac faults in *Grid 2* discussed in Subsubsection III-D-4, has been simulated in [16] “without” any proof provided for the stability and FRT capability. To do so, the enhanced controller proposed and shown in Fig. 2 are again tested, and simulations are conducted for different cases of faults in either ac *Grid 1* or *Grid 2* in order to fully cover the discussions made in Subsubsections III-D-3–III-D-4.

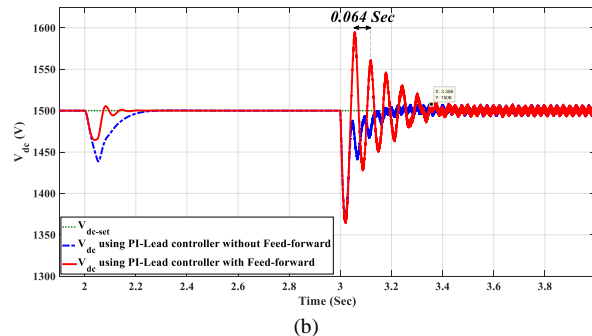
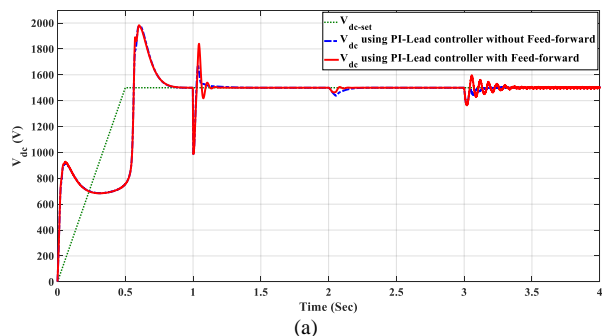


Fig. 11. The response of the dc-voltage power port VSC to *Category-A* Events for the period of 0–4.0 s (with the current-controlled PWM-based VSC using the linearized model-based linear controller): (a) output dc voltage; and (b) enlarged view.

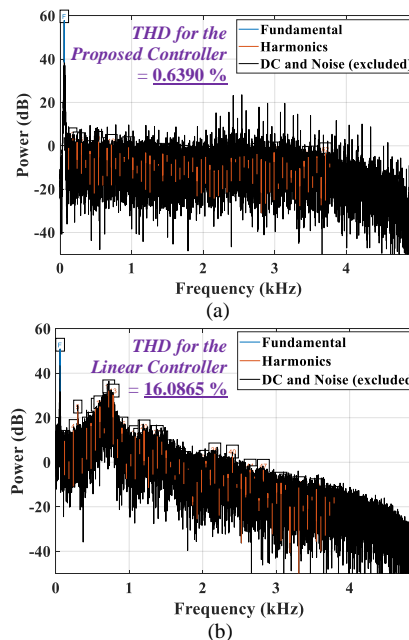


Fig. 12. AC-side current’s “signal spectrum,” including the total harmonic distortion (in %), as well as harmonics up to the 63rd one (in dB)—for the same ac-side filter—when (a) the proposed controller using the structure shown in Fig. 2; and (b) the current-controlled PWM-based VSC using the linearized model-based linear controller is employed.

Fig. 14 demonstrates the simulation results associated with a wide range of voltage drop in Phase-A and Phase-B for different loads fed by the dc-voltage power port VSC. To show the effectiveness of the enhanced controller, the simulation results have been repeated for two cases of $K_{Fault}=0$, i.e., equivalently without the FRT enhancement, and $K_{Fault}\neq 0$, i.e., equivalently with the FRT enhancement. Fig. 14-(a) reveals that the system is unstable as predicted by (28) since in hundred percent (100%) loading the dc voltage crashes for $K_{Fault}=0$. Also, the enhanced nonlinear controller is examined for the ac fault at the *Grid 2* side. As Fig. 14-(b) reveals. The closed-loop system controlled with the proposed regulator is very stable with very acceptable, satisfactory transient performance as discussed and proved in Subsection III-D-4.

D. Comparison of Event Category-B Using Robust, Multi-Objective and PI-lead Controllers

For the purpose of comparison, the structure shown in Fig. 5 has been simulated with PI-lead controller mentioned in [15] and [16], as well as a robust, multi-objective, controller

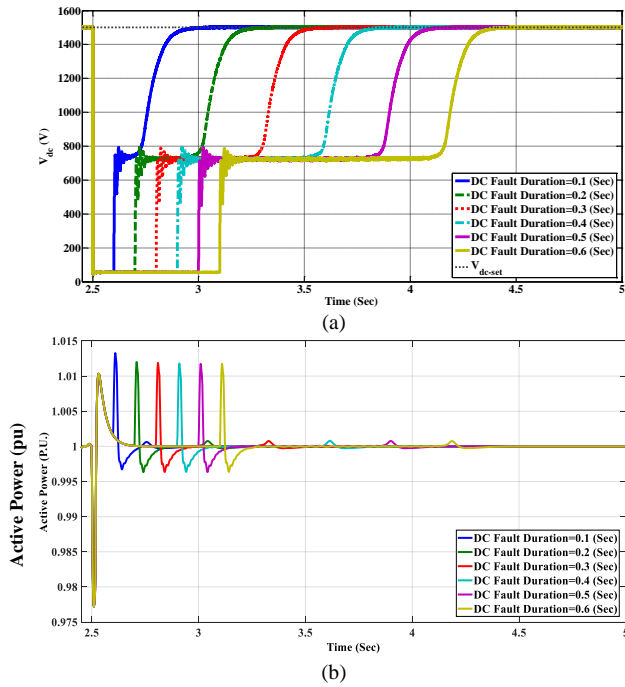


Fig. 13. The FRT capability of the proposed enhanced nonlinear controller for dc-side faults: (a) dc voltage; and (b) the power delivered to Zone II, i.e., *Constant PQ Active Load*.

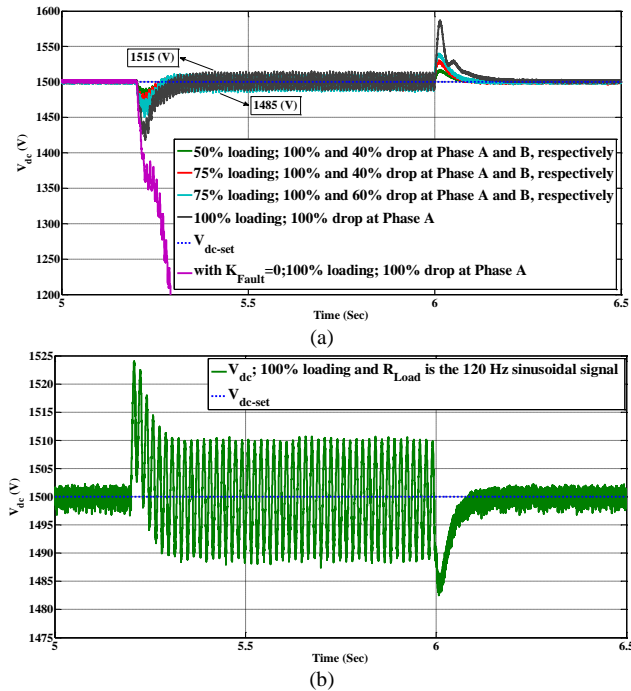


Fig. 14. Simulation results of V_{dc} when there is: (a) a fault on the ac side of dc-voltage power port VSC with different severity as mentioned on the figure above; and (b) a fault on the ac side of another PQ-controlled VSC connected to the dc energy pool in MI-AC/DC-MG configuration.

proposed in [14]. Again, the impact of a dc fault is investigated to check the capability of the controller for “riding through” the dc fault or, equivalently, to check the dc-fault-tolerant property of PI-lead controller, as well as a robust, multi-objective controller. Fig. 15 demonstrates the mentioned feature, and it is clear that the system does not have FRT capability for dc faults.

In addition, in order to have a comprehensive comparison with linear controllers, the system has been simulated with a

robust, multi-objective, dual-sequence controller—which has been mentioned in [14]—for both types of ac-side faults, i.e., the ac-side fault in *Grid 1* and the one in *Grid 2*. As detailed and discussed in [14], the inverse matrix calculation is a need for this type of robust, multi-objective, dual-sequence controllers. Furthermore, the oscillation of the dc voltage is more than that of the enhanced nonlinear controller with the same amount of loading; the burden of calculation is very much higher than that of the enhanced nonlinear controller, undoubtedly, because of inverse matrix calculations required in [14]. For the ac-side fault in *Grid 2*, Fig. 16-(b) shows a good transient performance of the whole system. However, the PQ-controlled VSC (i.e., PQ-VSC in [14]) converter connected to the dc side of the VSC in [14] has been equipped with a dual-sequence controller which increases the burden of computation, dramatically. Moreover, it imposes an extra, additional condition on connecting PQ-controlled VSCs, which is having dual-sequence controllers. As seen before, this condition is, however, not required for the case of enhanced nonlinear controller proposed here. Indeed, this enhanced nonlinear controller generally makes the MI-AC/DC-MGs’ flexibility stronger by omitting additional requirements for the controllers of other VSCs—as none of the VSCs (e.g., those are working as constant P/Q active loads, etc.) need have a specific controller in order to exchange power with the dc-voltage power port VSC.

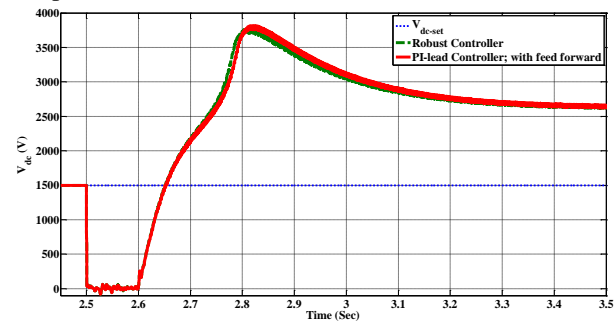
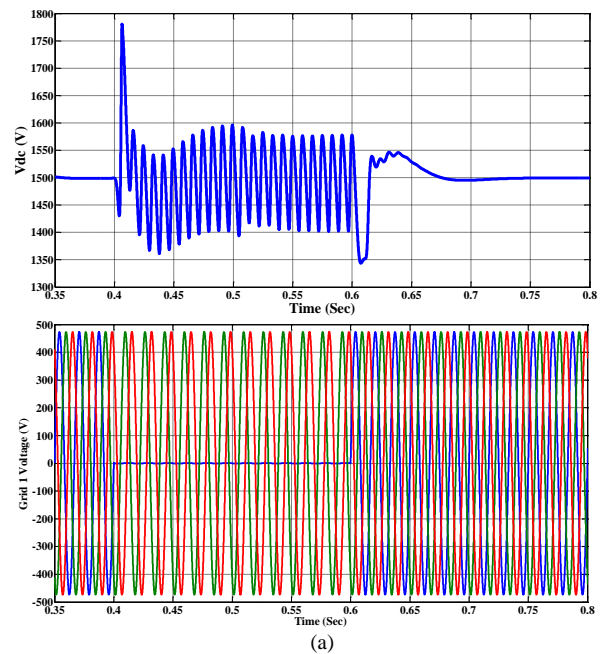


Fig. 15. The FRT capability of PI-lead controller mentioned in [16] for dc-side faults.



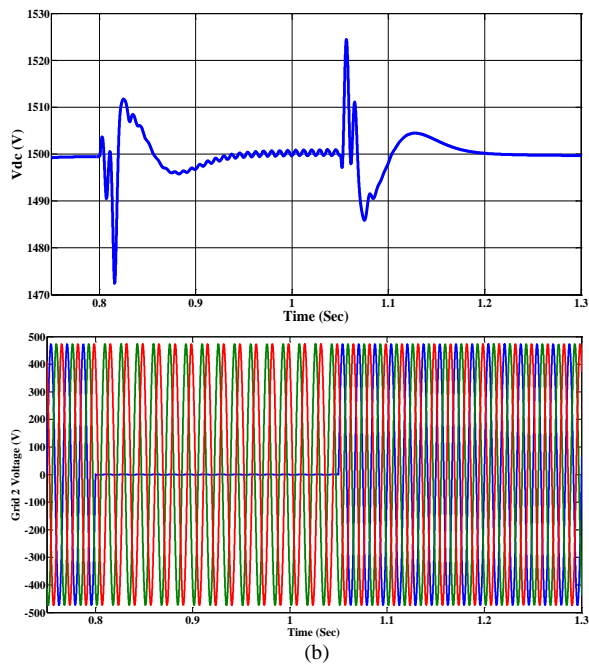


Fig. 16. The FRT capability of a robust, multi-objective, dual-sequence, linear controller for (a) ac fault in *Grid 1*; and (b) ac fault in *Grid 2* [14].

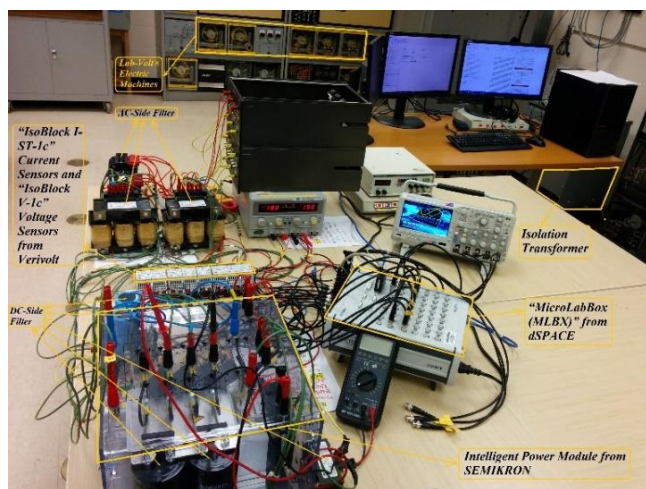


Fig. 17. The scaled-down test rig for conducting experiments.

V. EXPERIMENTAL RESULTS

For further evaluation of the proposed controller, an experimental test system is employed to emulate the performance of the stiff-grid-connected VSC equipped with an *LC*-filter at the dc side of a scaled-down, multi-infeed ac/dc modernized grid (or a hybrid ac/dc microgrid) as shown in Fig. 17. As regards this, the experiments conducted on a scaled-down test rig are provided in the first subsection, and in order to demonstrate a correlation between the simulation and experimental results, the same downgraded setup has been simulated by MATLAB since the test rig has been scaled down to be able to fulfill the tests.

A. Experimental Results of the Scaled-Down Test Rig

The experimental system consists of a grid-connected VSC, operating as a dc-voltage power port VSC, and dc-side both static and dynamic loads modeling a typical, scaled-down MI-AC/DC-MG. The VSC is controlled in the rectification mode, which yields the worst operating conditions with respect to the

dc-link voltage stability. An intelligent power module from SEMIKRON, which includes six insulated gate bipolar transistors (IGBTs) built by three “SKM 50 GB 123 D” modules, three “SKHI 21A (R)” gate drives, and protection circuit, is used to implement the dc-voltage power port VSC. The switching frequency is 5 kHz, which yields a control-period of 200 μ s. The ac-side filter inductance and resistance are 2.4 mH and 0.06 Ω , respectively. The dc-link capacitance and inductance are 2.04 mF and 1.50 mH, respectively. The three-phase VSC is nominally rated at 35 A and 208 V. However, to evaluate the effectiveness of the proposed enhanced controller, the VSC is not operated at the rated power to be able to emulate and excite the worst operating point from the perspective of non-minimum phase dynamics during conducting experiments. Consequently, the laboratory-scale converter is being utilized as a 0.7-kW, 20.0-V_{ac}, 20.0-A “de-rated” system in order to have sufficiently strong non-minimum dynamics caused by the stated operating point for controller’s performance validation purposes; see [14]–[18] for further details.

The VSC’s inductor currents are measured by “IsoBlock I-ST-1c” current sensors from Verivolt, and the voltages are measured by “IsoBlock V-1c” voltage sensors from Verivolt. The converter is interfaced with a “MicroLabBox (MLBX)” from dSPACE. The proposed control algorithm is exacted and run by a dual-core, 2 GHz “NXP (Freescale) QorIQ P5020” real-time processor. The PWM signals are generated by “Xilinx Kintex-7 XC7K325T” field programmable gate arrays (FPGAs) connected to digital inputs/outputs (I/Os). The MLBX interface board is equipped with eight 14-bit, 10 megasamples per second (MSPs), differential analogue-to-digital channels to interface the measured signals to the control system (with the functionality of free running mode). The software code is generated by the Real-Time-WorkShop in Simulink environment. The dc-side load is composed of an *LC*-filter connected to a resistive load-box and a dynamic load, which can be regarded as an effective way to model both static and dynamic loads of an MI-AC/DC-MG; the dynamic load is composed of a *Lab-Volt*® dc-motor loaded by a dynamometer.

The proposed controller has been examined under equilibrium-to-equilibrium maneuver tests by means of two main events. First, the voltage of the dc link has linearly been changed from 0.6 per-unit to 1.0 per-unit during 1.0 s while it is feeding 1.0 per-unit dynamic load, and the corresponding results are shown in Fig. 18. Second, to effectively test the control functionality and transient performance, a sudden, harsh change in both dynamic and static loads from 0.0 per-unit to 1.0 per-unit is applied—i.e., an intentionally created, long-lasting, harsh dc motor current (for testing the controls during operating point variations) along with a sudden static load change. The corresponding results are illustrated in Fig. 19 and Fig. 20. Also, the effective dc-link capacitance has been doubled in order to assess the robustness of the proposed controller against parametric uncertainties in the equivalent dc-link capacitance. To this end, Fig. 20 shows the control performance of the proposed controller under such parametric uncertainties, and the system is excited by an increase in the dc-side load. As depicted in Fig. 18–Fig. 20, in spite of the large, dynamic variations in the MI-AC/DC-MG’s equilibrium point with various natures, the proposed controller offers the robust

stability against operating point variations and also preserves the robust transient performance of the dc-link voltage. This is because of the equilibrium-to-equilibrium maneuver capability of the passivity-based controller, which has been discussed in Section III.

Moreover, to evaluate the performance of the proposed controller for FRT capability, it has been examined under the unbalanced condition appearing on the ac side of the grid. Fig. 21-(a) and Fig. 21-(b) reveal that the controller is able to stabilize the dc-side voltage with good performance under permanent 90% voltage dip in one phase when dc-side grid changes its operating point and feeds a load. Also, Fig. 21-(c) shows the dc-side voltage when there exists a load variation in the dc side of the VSC.

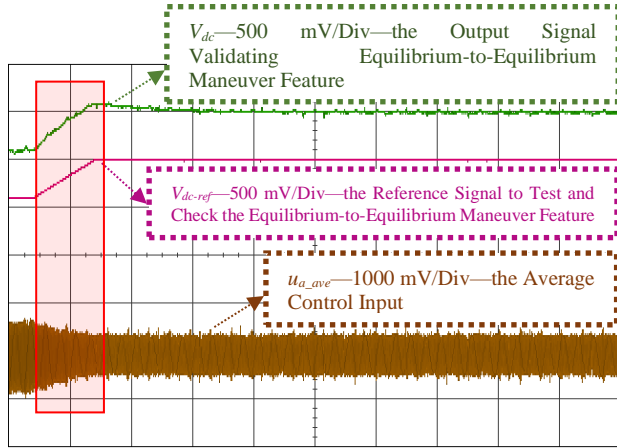


Fig. 18. Experimental results of the proposed controller for testing and validating equilibrium-to-equilibrium maneuver capability by the linear change in V_{dc-ref} —Channel 2 (top): V_{dc} output in per-unit, 500 mV/Div; Channel 4 (middle): V_{dc-ref} reference in per-unit, 500 mV/Div; Channel 1 (bottom): $u_{a,ave}$, average control signal, 1000 mV/Div; and time horizontal axis 1.0 s/Div.

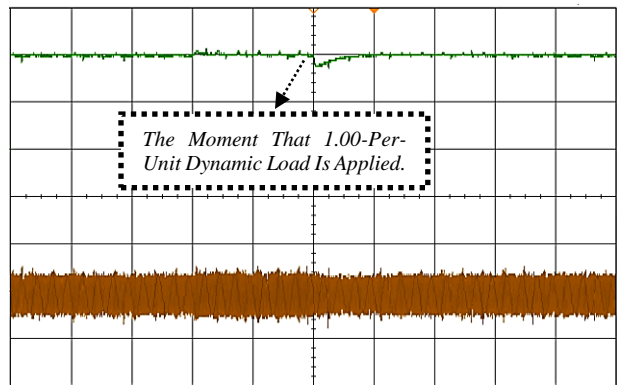


Fig. 19. Experimental results of the proposed controller for testing and validating equilibrium-to-equilibrium maneuver capability by a sudden, harsh change in the dynamic load (i.e., an intentionally created, harsh motor starting current) while V_{dc-ref} is 1.00 per-unit—Channel 2 (top): V_{dc} output in per-unit, 500 mV/Div; Channel 1 (bottom): $u_{a,ave}$, average control signal, 1000 mV/Div; and time horizontal axis 1.0 s/Div.

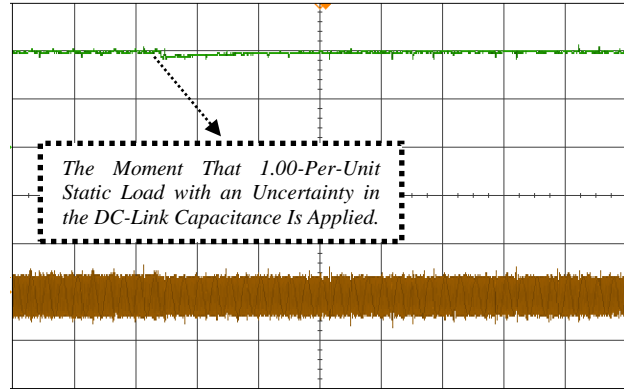


Fig. 20. Experimental results of the proposed controller during a variation in the static dc load, as well as existing uncertainty in the dc-link capacitance while V_{dc-ref} is 1.00 per-unit—Channel 2 (top): V_{dc} output in per-unit, 500 mV/Div; Channel 1 (bottom): $u_{a,ave}$, average control signal, 1000 mV/Div; and time horizontal axis 1.0 s/Div.

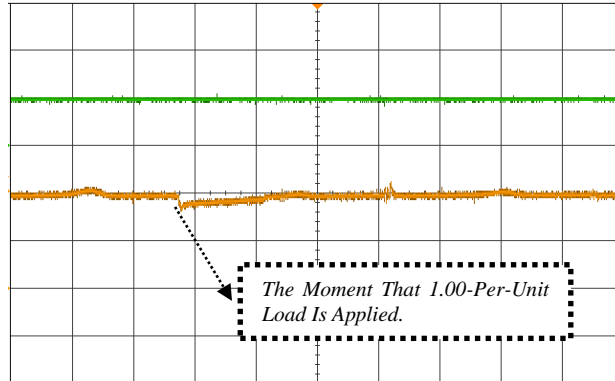
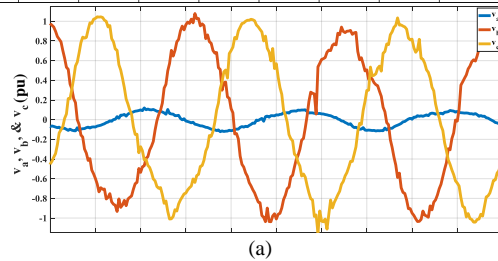
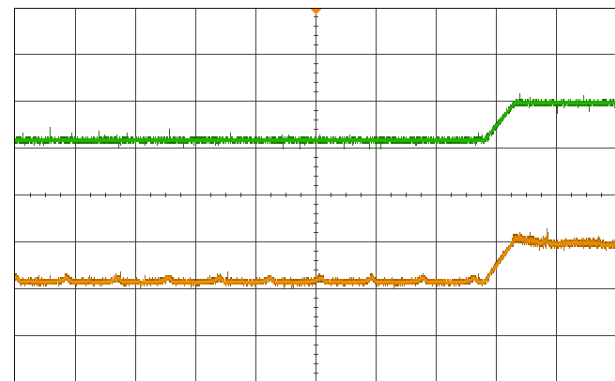


Fig. 21. Experimental results of the proposed fault-tolerant controller during existing severe unbalanced condition in the ac-side voltage: (a) an equilibrium, operating point variation by a linear change in V_{dc-ref} —Channel 2 (top): V_{dc-ref} reference in per-unit, 500 mV/Div; Channel 1 (bottom): V_{dc} , average control signal, 500 mV/Div; and time horizontal axis 2.0 s/Div; (b) equilibrium, operating point variation by a variation in the dc load—Channel 2 (top): V_{dc-ref} reference in per-unit, 1000 mV/Div; Channel 1 (bottom): V_{dc} , average control signal, 500 mV/Div; and time horizontal axis 500 ms/Div.

B. Simulation Results of the Downgraded Setup Generated by MATLAB

In order to demonstrate a correlation between the simulation and experimental results, the same downgraded setup which is tested under similar circumstances has been simulated by MATLAB. The aforementioned results have been provided in Figs. 22–25; Figs. 18–21 and Figs. 22–25 demonstrate that there is complete agreement between what has been experimentally generated by the test rig and what has been digitally simulated by MATLAB, respectively.

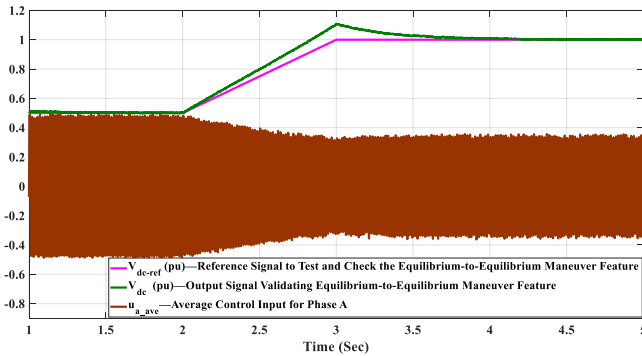


Fig. 22. MATLAB-generated simulation results for the experiment associated with the Fig. 18.

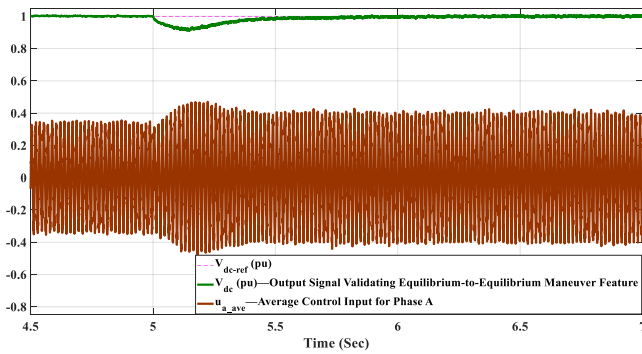


Fig. 23. MATLAB-generated simulation results for the experiment associated with the Fig. 19—we did our best to mimic the same scenario as that of Fig. 19 for the long-lasting, harsh dc motor current in this case—but, certainly, they cannot be the same exactly as that is a random variable depending on the mechanical systems.

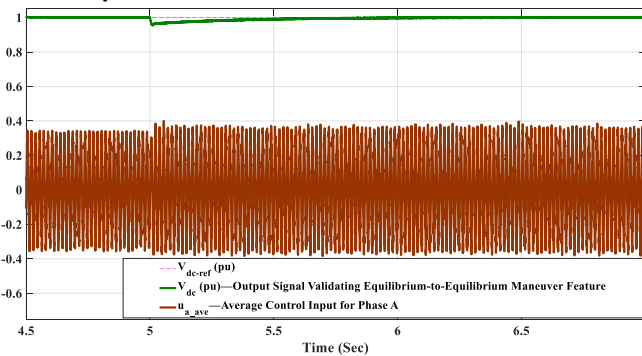


Fig. 24. MATLAB-generated simulation results for the experiment associated with the Fig. 20.

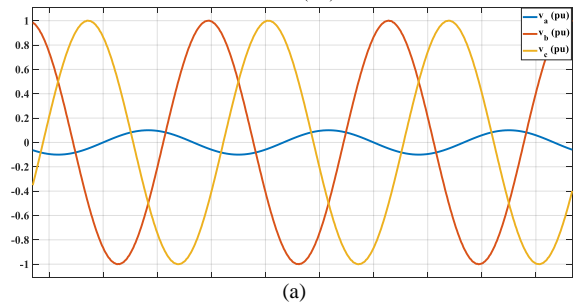
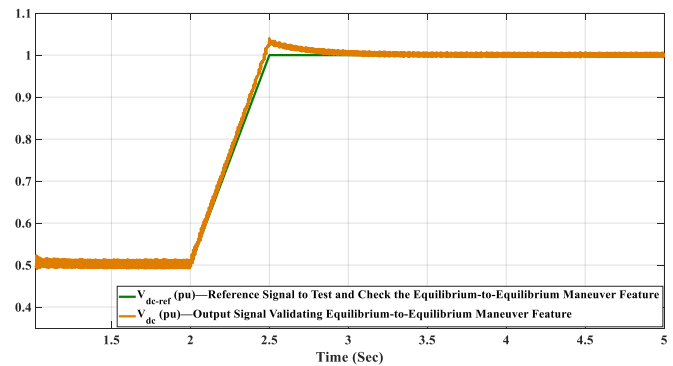


Fig. 25. MATLAB-generated simulation results for the experiment associated with the Fig. 21.

VI. CONCLUSION

In this article, multi-infeed ac/dc modernized grids (or hybrid ac/dc grids) have been considered, and an enhanced nonlinear controller has been proposed to improve the resiliency along with the power quality of the aforementioned type of microgrids in the smart grid paradigm. In this regard, improvements have been accomplished with respect to two integral directions. First, considering the linearized model of a dc energy pool based on the energy balance equation reveals that considering L_{DC-eq} adds additional zeros and poles to the dynamics of dc voltage; at different operating points and for different levels of uncertainties in system parameters, while the pole can be unstable, the zero can lead to non-minimum phase dynamics. To tackle this problem, we have proposed an enhanced variable-structure-based nonlinear controller for the dc-voltage power port VSC to take into account the nonlinear dynamics caused by L_{DC-eq} . Second, the proposed primary controller has been augmented with making use of fault-tolerant nonlinear control approaches for the dc-voltage power port VSC in MI-AC/DC-MGs considering the presence of any kinds of faults or harsh unbalanced conditions on the ac-side voltage of all VSCs forming a typical MI-AC/DC-MG. In fact, this feature generally strengthens the flexibility of MI-AC/DC-

MGs in the smart grid paradigm of the future. The proposed enhanced controller has taken into account comprehensive nonlinear closed-loop dynamics of the dc-voltage power port VSC with an equilibrium-to-equilibrium maneuver capability, without any cascaded control structures, so it “globally” and “fault-tolerantly” regulates all existing nonlinear dynamics by means of a passivity-based design approach. In other words, the large signal model of the dc-voltage power port VSC model, captured from Kirchhoff’s current law, has been employed in order to design the mentioned controller, which is not suffering from the cascaded controller structure employed in the conventional current-controlled PWM-based VSCs connected to the dc side via LC -filters. As a result, the proposed controller was able to respond with highly enhanced transient performance compared to linearized model-based linear controls. On top of the above-mentioned benefits, it resulted in the significant THD reduction and, as a consequence, the considerable reduction in the passive filter’s size required. Theoretic analyses, simulation results, and experimental tests have provided for revealing the effectiveness of the proposed enhanced nonlinear controller.

VII. APPENDIX

A. Subsection A

Equations (5)–(6) have been “re”expressed by (A-1)—just as a reference—in order to represent them in the general form of affine nonlinear dynamic systems using $f(x)$, $g(x)$, and $e(t_n)$ matrices, where $x = [i_{n_a} \ i_{n_b} \ i_{n_c} \ V_{n_dc} \ i_{n_Ldc}]^T = [x_{n1} \ x_{n2} \ x_{n3} \ x_{n4} \ x_{n5}]^T$, $e(t_n)$ is the disturbance vector, and $y = h(x) = x_{n4}$.

$$\frac{d}{dt_n} \begin{bmatrix} x_{n1} \\ x_{n2} \\ x_{n3} \\ x_{n4} \\ x_{n5} \end{bmatrix} = \underbrace{\begin{bmatrix} -qx_{n1} \\ -qx_{n2} \\ -qx_{n3} \\ -\frac{x_{n4}}{q_{dc_Load}} - x_{n5} \\ \frac{L_s}{L_{DC_eq}} x_{n4} - \frac{L_s}{L_{DC_eq}} q_{res} x_{n5} \end{bmatrix}}_{f(x_n)} + \underbrace{\begin{bmatrix} \cos(\omega_n t_n) \\ \cos(\omega_n t_n - \frac{2\pi}{3}) \\ \cos(\omega_n t_n + \frac{2\pi}{3}) \\ 0 \\ \frac{-L_s}{L_{DC_eq}} V_{n_dc_Load} \end{bmatrix}}_{e(t_n)} + \underbrace{\begin{bmatrix} -x_{n4} & 0 & 0 \\ 0 & -x_{n4} & 0 \\ 0 & 0 & -x_{n4} \\ x_{n1} & x_{n2} & x_{n3} \\ 0 & 0 & 0 \end{bmatrix}}_{g(x_n)} \underbrace{\begin{bmatrix} u_{a_ave} \\ u_{b_ave} \\ u_{c_ave} \end{bmatrix}}_u \quad (A-1)$$

B. Subsection B

The derivation of (17) has been provided below.

$$\begin{aligned} & \left\{ \begin{aligned} \frac{de}{dt_n} &= \frac{dx_n}{dt_n} - \frac{dx_n^*}{dt_n}, \\ \text{where } \frac{dx_n}{dt_n} &= (A_c(u_{ave}) + A_d)x_n + Bu_{ave} + v_n, \end{aligned} \right. \\ & \Rightarrow \frac{de}{dt_n} = (A_c(u_{ave}) + A_d)x_n + Bu_{ave} + v_n - \frac{dx_n^*}{dt_n} \Rightarrow \\ & \frac{de}{dt_n} = (A_c(u_{ave}) + A_d)(x_n + \underbrace{+x_n^* - x_n^*}_{\substack{\text{Add } x_n^* \text{ and Deduct } x_n^* \\ \text{in the Parentheses}}}) + \\ & B(u_{ave} + \underbrace{+u_{ave}^* - u_{ave}^*}_{\substack{\text{Add } u_{ave}^* \text{ and Deduct } u_{ave}^* \\ \text{in the Parentheses}}}) + v_n - \frac{dx_n^*}{dt_n} \Rightarrow \\ & \left\{ \begin{aligned} \frac{de}{dt_n} &= (A_c(u_{ave}) + A_d)(x_n - x_n^*) + B(u_{ave} - u_{ave}^*) + \\ v_n + \underbrace{(A_c(u_{ave}) + A_d)x_n^* + Bu_{ave}^*}_{\substack{\text{Derived from Adding and} \\ \text{Deducting } x_n^* \text{ \& } u_{ave}^*}} - \frac{dx_n^*}{dt_n}, \end{aligned} \right. \Rightarrow \\ & \text{where } \frac{dx_n^*}{dt_n} = (A_c(u_{ave}^*) + A_d)x_n^* + Bu_{ave}^* + v_n. \\ & \frac{de}{dt_n} = (A_c(u_{ave}) + A_d)e + \\ & B(u_{ave} - u_{ave}^*) + (A_c(u_{ave}) - A_c(u_{ave}^*))x_n^* \Rightarrow \\ & \frac{de}{dt_n} = \underbrace{(A_c + A_d)e + B(u_{ave} - u_{ave}^*) + (A_c(u_{ave}) - A_c(u_{ave}^*))x_n^*}_{\text{which is (17)}}, \end{aligned}$$

This concludes the derivation. \square

C. Subsection C

This subsection complements the proof of the *Theorem 1*. Regarding (23), considering (6), (30), and $K = \text{diag}[k, k, k]$ —with $k > 0$ —the left side of (23) is calculated as follows.

One can prove that (A-2) is positive definite using Sylvester’s criterion and (8) as follows. To do so, we have mentioned Sylvester’s criterion in mathematics for reference.

Sylvester’s Criterion [55]: It is a “necessary and sufficient” criterion to determine whether a Hermitian matrix is positive definite. Sylvester’s criterion states that an $n \times n$, Hermitian matrix M_H is positive definite “if and only if” all the following matrices have a positive determinant: (1) the upper left 1-by-1 corner of M_H ; (2) the upper left 2-by-2 corner of M_H ; (3) the upper left 3-by-3 corner of M_H ; ...; and (n) the M_H itself. In other words, all of the “leading principal minors” must be positive.

Based on Sylvester’s criterion, one can see that “all” of the leading principal minors are positive as expressed in (A-2). Based on Sylvester’s criterion, inequalities (A-3) conclude that (23) is true and met for the dynamics of our system model.

Regarding (29), considering (27) and (30), one can simply prove that

$$\begin{bmatrix} -1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \\ \frac{i_{n_a}^*}{V_{n_dc}^*} & \frac{i_{n_b}^*}{V_{n_dc}^*} & \frac{i_{n_c}^*}{V_{n_dc}^*} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{n_a_Fault} - v_{n_a} \\ v_{n_b_Fault} - v_{n_b} \\ v_{n_c_Fault} - v_{n_c} \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} v_{n_a_Fault} - v_{n_a} \\ v_{n_b_Fault} - v_{n_b} \\ v_{n_c_Fault} - v_{n_c} \\ -\frac{v_{n_a_Fault} - v_{n_a}}{V_{n_dc}^*} i_{n_a}^* - \frac{v_{n_b_Fault} - v_{n_b}}{V_{n_dc}^*} i_{n_b}^* - \frac{v_{n_c_Fault} - v_{n_c}}{V_{n_dc}^*} i_{n_c}^* \\ 0 \end{bmatrix} = 0.$$

Thus, this subsection concludes all of the derivations. \square

D. Subsection D

This subsection provides all of the parameters used in Fig. 5 in Section IV.

TABLE I
SIMULATION PARAMETERS OF ZONE I IN FIG. 5

Rated Power	0.50 MVA
Grid #1 Voltage (low-voltage side)	580 V at 60 Hz
SCR and X_{grid}/R_{grid} —where $X_{grid} \triangleq 2\pi f_{grid} L_{grid}$	12.62 and 1
R_f —associated with the ac-side filter	0.06 Ω
r_{on} —associated with the Zone I's VSC	2 m Ω
L_f —associated with the ac-side filter	300 μ H
i_{Loss} —associated with the VSC loss	1.5 A
C —associated with the dc-side capacitance of Zone I	25,000 μ F
L_{DC_eq} —associated with the dc-side equivalent inductance	300 μ H
Switching Frequency	10 kHz
k , positive constant parameter of the proposed controller	0.1
C_{eq} —associated with the dc-side equivalent capacitance required for the parameters of the proposed controller	25,000 μ F

$$[-A_d + B^* K (B^*)^T] = \begin{bmatrix} q + k(V_{n_dc}^*)^2 & 0 & 0 & -ki_{n_a}^* V_{n_dc}^* & 0 \\ * & q + k(V_{n_dc}^*)^2 & 0 & -ki_{n_b}^* V_{n_dc}^* & 0 \\ * & * & q + k(V_{n_dc}^*)^2 & -ki_{n_c}^* V_{n_dc}^* & 0 \\ * & * & * & \frac{1}{q_{dc-Load}} + k[(i_{n_a}^*)^2 + (i_{n_b}^*)^2 + (i_{n_c}^*)^2] & 0 \\ * & * & * & * & q_{res} \end{bmatrix}, \quad (A-2)$$

where symbol “*” is used to induce symmetric terms.

$$\det\left(\begin{bmatrix} q + k(V_{n_dc}^*)^2 \end{bmatrix}\right) = q + k(V_{n_dc}^*)^2 > 0,$$

$$\det\left(\begin{bmatrix} q + k(V_{n_dc}^*)^2 & 0 \\ * & q + k(V_{n_dc}^*)^2 \end{bmatrix}\right) = [q + k(V_{n_dc}^*)^2]^2 > 0,$$

$$\det\left(\begin{bmatrix} q + k(V_{n_dc}^*)^2 & 0 & 0 \\ * & q + k(V_{n_dc}^*)^2 & 0 \\ * & * & q + k(V_{n_dc}^*)^2 \end{bmatrix}\right) = [q + k(V_{n_dc}^*)^2]^3 > 0,$$

$$\det\left(\begin{bmatrix} q + k(V_{n_dc}^*)^2 & 0 & 0 & -ki_{n_a}^* V_{n_dc}^* \\ * & q + k(V_{n_dc}^*)^2 & 0 & -ki_{n_b}^* V_{n_dc}^* \\ * & * & q + k(V_{n_dc}^*)^2 & -ki_{n_c}^* V_{n_dc}^* \\ * & * & * & \frac{1}{q_{dc-Load}} + k[(i_{n_a}^*)^2 + (i_{n_b}^*)^2 + (i_{n_c}^*)^2] \end{bmatrix}\right) =$$

$$[q + k(V_{n_dc}^*)^2]^2 \left[[q + k(V_{n_dc}^*)^2] \left[\frac{1}{q_{dc-Load}} + k(1.5I^2) \right] - k^2(1.5I^2)(V_{n_dc}^*)^2 \right] =$$

$$\left[q + k(V_{n_dc}^*)^2 \right]^2 \left[\frac{q}{q_{dc-Load}} + qk(1.5I^2) + \frac{k(V_{n_dc}^*)^2}{q_{dc-Load}} \right] > 0, \text{ and}$$

$$\det\left([-A_d + B^* K(B^*)^T\right]) = \underbrace{\left[\underbrace{-q_{res}}_{\text{It is negative.}} \times \underbrace{\left[-\left[q + k(V_{n_dc}^*)^2 \right]^2 \left[\frac{1}{q_{dc-Load}} + k(1.5I^2) \right] - k^2(1.5I^2)(V_{n_dc}^*)^2 \right]}_{\text{Based on the expression above, it is also negative.}} \right]}_{\text{It is finally positive.}} > 0, \quad (\text{A-3})$$

where we have benefited from $k > 0$; (8); the fact that $(i_{n_a}^*)^2 + (i_{n_b}^*)^2 + (i_{n_c}^*)^2 = [I \cos(\omega t + \varphi)]^2 + [I \cos(\omega t + \varphi + \frac{2\pi}{3})]^2 + [I \cos(\omega t + \varphi + \frac{4\pi}{3})]^2 = 1.5I^2$ [17]; and the following formulas to calculate the determinant of associated matrices—where $v \triangleq q + k(V_{n_dc}^*)^2$, $\alpha \triangleq -ki_{n_a}^* V_{n_dc}^*$, $\beta \triangleq -ki_{n_b}^* V_{n_dc}^*$, and $\gamma \triangleq -ki_{n_c}^* V_{n_dc}^*$.

$$\det\left(\begin{bmatrix} v & 0 & 0 & \alpha \\ * & v & 0 & \beta \\ * & * & v & \gamma \\ * & * & * & \varepsilon \end{bmatrix}\right) = v^2(v\varepsilon - \alpha^2 - \beta^2 - \gamma^2), \text{ and } \det\left(\begin{bmatrix} v & 0 & 0 & \alpha & 0 \\ * & v & 0 & \beta & 0 \\ * & * & v & \gamma & 0 \\ * & * & * & \varepsilon & 0 \\ * & * & * & * & \kappa \end{bmatrix}\right) = -\kappa[-v^2(v\varepsilon - \alpha^2 - \beta^2 - \gamma^2)]. \quad (\text{A-4})$$

TABLE II
SIMULATION PARAMETERS OF
ZONE II IN FIG. 5

Rated Power	0.5 MVA
Grid #2 Voltage	580V at 60Hz
SCR and X_{grid}/R_{grid}	12.62 and 1
R_s	0.06 Ω
r_{on}	2 m Ω
L_s	300 μ H
C	3,125 μ F
i_{Loss}	1.5 A
K_p	0.40 Ω
(Current Controller)	
K_i	12 Ω /s
(Current Controller)	

TABLE III
SIMULATION PARAMETERS OF
DC ENERGY POOL IN FIG. 5

Rated voltage	1,500 V
dc-cable length	300 km
R_{cable}	0.820 m Ω /km
C_{cable}	0.014 μ F/km
L_{cable}	0.980 μ H/km

TABLE IV
SIMULATION PARAMETERS OF
ZONE III IN FIG. 5

Power Rating	0.90 MW
ESS and load voltage	500 V _{dc}
C_L	1,000 μ F
C_H	6,000 μ F
L_{Boost}	100 mH
R_{DC}	1 Ω
K_p and K_i (mode1)	0.40 and 4.00×10^{-4}
K_p and K_i (mode2)	0.0133 and 0.0533
V_{L_Ref}	500 V
i_{L_Ref}	1,800 A

TABLE V
PARAMETERS OF EXPERIMENTAL SETUP TO MIMIC THE SIMULATION OF A
HIGH-POWER CONVERTER

Rated Power	0.7 kVA
Adjusted Grid Voltage and Current	20 V and 20 A at 60 Hz
$R_{s,r_{on}}$	0.06 Ω
L_s	2.40 mH
C_{eq}	2.04 mF
$L_{DC,eq}$	1.50 mH
Switching Frequency	5 kHz
k , positive constant parameter of the proposed controller	0.1

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