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Power Losses Control for Modular Multilevel Converters Under Capacitor Deterioration

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***Abstract*--The modular multilevel converter (MMC) is attractive for medium/high-voltage and high-power applications because of the advantages of its high modularity, availability and high power quality. Due to chemical process, aging effect, etc., the capacitor in the submodule (SM) of the MMC would gradually deteriorate and the capacitance would drop, which would cause unbalanced SM power losses distribution in the same arm of the MMC and affect the reliability of the MMC. This paper proposed an equivalent-reference (ER) control method, which can effectively realize balanced SM power losses distribution in the same arm of the MMC through the voltage-balancing control for the virtual capacitor voltages in the MMC under the capacitor deterioration. The proposed ER control can effectively improve the reliability of the MMC with the balanced SM power losses distribution in the MMC under capacitor deterioration. The simulation studies with the time-domain professional tool PSCAD/EMTDC are conducted and a down-scale MMC prototype is also tested with the proposed control strategy. The study results confirm the effectiveness of the proposed control strategy.**

***Index Terms*— Capacitor deterioration, control strategy, modular multilevel converter, power losses.**

I. INTRODUCTION

MODULAR multilevel converters (MMCs) have becomes increasingly attractive for medium/high-voltage and high-power applications with the advantages such as the excellent output voltage waveforms and very high efficiency [1, 2]. A multilevel voltage can be produced with the flexible operation of the MMC while reducing average switching frequency without compromising the power quality [3, 4]. Recently, due to the easy construction, assembling, and flexibility in converter design, the MMC becomes promising for various applications such as machine drives [5], electric railway supplies [6] and microgrid [7].

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Reliability is one of the most important issues for the MMC, because the MMC is composed of a large number of devices such as switch, diode and capacitor, where each device can be considered as a potential failure point [8], [9]. The electrolytic capacitor is widely considered for the MMC in some applications such as motor drive and microgrid [5], [7], [10-13] because of its feature such as high capacitance per unit volume. Due to the chemical process, aging effect, etc., the capacitor in the MMC would gradually deteriorate, which is normally expressed by the capacitance drop [14, 15]. Normally, the deteriorated capacitor needs be replaced until its capacitance drops below the threshold value, such as 80% of the rated value [14].

Recently, several methods have been presented to monitor capacitance in the MMC. Reference [14] introduces a capacitor condition monitoring scheme for the MMC, where the capacitance in the MMC is estimated by a recursive least square algorithm based on the capacitor voltage, arm current and switching state. Reference [15] presents a capacitor condition monitoring scheme based on a Kalman filter algorithm, where the capacitance in the MMC is estimated based on the capacitor voltage and current. Reference [16] presents a simple capacitor monitoring algorithm based on the relationship between the reference SM capacitance and the monitoring SM capacitance. The above literature can effectively estimate the capacitance in the MMC with very high accuracy and the error is less than about 1%.

Owing to capacitor deterioration, the MMC would be operated with different capacitances in the different SMs. It would affect the performance of the MMC, especially the SM power losses in the arm of the MMC, which would affect aging of semiconductors and lifetime of SMs. Reference [17] presents an active power losses distribution method for the MMC based on circulating currents at fundamental frequency, second harmonic and dc voltage offset on the converter voltage waveform, which can change the balance of power losses between the top switch and bottom switch in each SM. However, it can not balance the power losses distribution among the SMs in the arm under capacitor deterioration. Reference [18] presents an SM level power loss balancing control for the MMC based on switching loss model, unbalance degree extractor, power level balancing control regulator and enable module. However, it only reduces the imbalance of the SM switching losses distribution in the arm. It also only considers the whole SM switching loss and it does not consider the switching losses balancing distribution for each type semiconductor among the SMs in the arm. In addition, the real-time calculation of each semiconductor

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switching losses and unbalance degree also increases the computation amount. Reference [19] presents the switching balancing (SB) algorithm and total losses balancing (TLB) algorithm to reduce the SM power losses imbalance in the arm. The SB algorithm reduces the SM switching power losses imbalance in the arm through equally distributing the number of transitions for the SMs in the arm, which can reduce the SM power losses imbalance in the arm. The TLB algorithm reduces the SM power losses imbalance in the arm based on the sum of the SM conduction losses deviation and switching losses deviation. However, the SB algorithm only considers the switching loss and omits the conducting loss. In addition, both SB and TLB algorithms only consider the power loss balancing for the whole SM, not for each type semiconductor, which can not realize power loss balancing for each type semiconductor among the SMs in the arm, which would result in different lifetimes for the same type of semiconductors in different SMs of the arm. In addition, the real-time monitoring of a large number of transitions for each SM and average number of transitions, real-time computation of conduction losses and switching losses of all semiconductors in each SM would increase the computation amount, which would require high processing capability for the controller.

In this paper, the power losses distribution of the MMC under capacitance deterioration is analyzed in detail, where the capacitor deterioration would cause different equivalent references (ERs) for the SMs in the same arm. It would result in unbalanced SM power losses distribution in the same arm of the MMC and cause different aging speed of semiconductors, and therefore affect the reliability of the MMC. In this paper, an ER control method is proposed for the MMC under capacitor deterioration, where the ERs for the SMs in the same arm can be kept close to each other through the voltage-balancing control for the virtual capacitor voltages. The proposed ER control method can effectively balance the SM power losses distribution in the same arm of the MMC based on the relationship between ER and semiconductor power losses in the arm. Therefore, the proposed power losses control strategy imposes the reliability of the MMC by improving the aging speed of the SMs. In comparison with [18] and [19], the primary contributions of this paper include: 1) this paper reveals the relationship between the capacitance and semiconductor power loss in the SM including conduction loss and switching loss; 2) this paper considers power loss balancing for both conduction loss and switching loss; 3) the proposed method not only can balance the power losses for the whole SM, but also can balance the power losses of the same type semiconductors in different SMs of the arm; 4) the proposed control algorithm is based on the SM capacitance, while the change of the SM capacitance is normally quite slow. It means that the capacitor value is not necessary to be updated in each control period, and accordingly simplifies the computation and reduces computation amount.

This paper is organized as follows. Section II presents the operation principle of the MMC. Section III analyses the relationship between the ER and the power losses of the MMC in detail under capacitor deterioration. Section IV proposes the ER control method for the MMC under capacitor deterioration. The system simulation and experimental tests are presented in Sections V and VI, respectively, to show the effectiveness of the proposed power losses control strategy for the MMC. Finally, the conclusions are presented in Section VII.

II. Operation Principle of MMCs

A three-phase MMC is shown in Fig. 1(a), which has six arms. Each arm consists of n SMs and an arm inductor L_s. The upper arm and the lower arm in the same phase comprise a phase unit. Fig. 1(b) shows the i-th SM (i=1, 2……n) in the upper arm of phase A, which contains the top switch/diode (T_t/D_t), the bottom switch/diode (T_b/D_b), the capacitor C_{aui} and the bypass switch [20]. Normally, each SM is controlled with a switching function S as

$$S=\begin{cases}1, & T_t \text{ is on and} T_b \text{ is off}\\ 0, & T_t \text{ is off and} T_b \text{ is on}\end{cases} \tag{1}$$

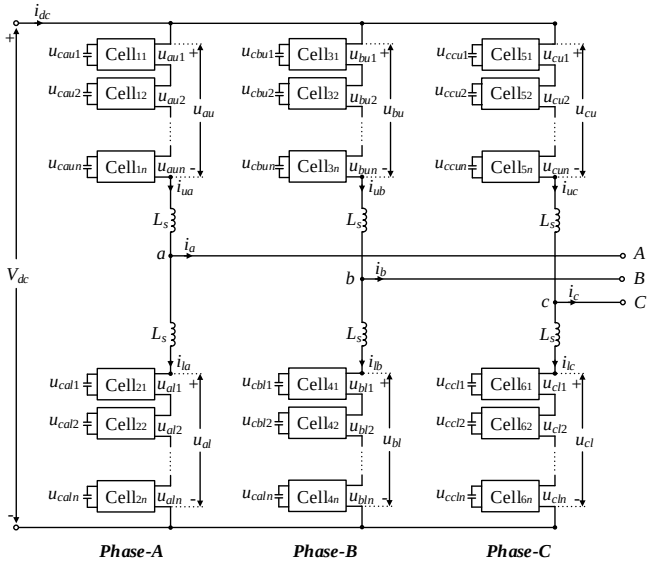

Fig. 1. (a) Block diagram of a three-phase MMC. (b) SM unit.

Table I shows the two states of the SM. One is “On” state, when S is 1. Here, the SM output voltage u_{aui} equals the capacitor voltage u_{caui}. The other one is “Off” state and u_{aui} equals 0, when S is 0. In the “On” state, the charge and discharge of the capacitor C_{aui} depends on the arm current flow direction. If the arm current i_{ua} is positive, as shown in Fig. 1(a), the capacitor in On-state SM would be charged and u_{caui} is increased. If i_{ua} is negative, the capacitor in On-state SM would be discharged and u_{caui} is decreased. In the “Off” state of the SM, the corresponding capacitor would be bypassed and u_{caui} is unchanged, irrespective of the arm current flow direction [21].

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TABLE I
TWO OPERATION STATES OF SMS

SM state	S	T_t	T_b	u_{aui}	i_{ua}	C_{aui}	u_{caui}
on	1	on	off	u_{caui}	≥0	Charge	Increased
					<0	Discharge	Decreased
off	0	off	on	0	≥0 or <0	Bypass	Unchanged

In Fig. 1(a), suppose that the circulating current is suppressed with the method [22], the upper and lower arm current i_{ua} and i_{la} in the phase A can be described as

$$\begin{cases} i_{ua} = \dfrac{I_m}{2}\sin(\omega t+\alpha)+\dfrac{i_{dc}}{3} \\ i_{la} = -\dfrac{I_m}{2}\sin(\omega t+\alpha)+\dfrac{i_{dc}}{3} \end{cases} \tag{2}$$

where I_m and α are the peak value and the phase angle of the phase current at the ac side of the MMC, respectively. ω is the fundamental angular frequency. i_{dc} is the current at the dc side, as shown in Fig. 1(a).

According to [23] and [24], the voltage u_{au} in Fig. 1, which is the sum of the n series-connected SMs' output voltage, can be expressed as

$$u_{au} = \sum_{i=1}^{n} u_{aui} \tag{3}$$

with

$$u_{aui} = u_{caui}\cdot\frac{1+x_{er\_aui}}{2} \tag{4}$$

$$u_{caui} = \frac{1}{C_{aui}}\int i_{caui}dt = \frac{1}{C_{aui}}\int i_{ua}\cdot\frac{1+x_{er\_aui}}{2}dt \tag{5}$$

where x_{er_aui} is the ER for the i-th SM. u_{aui}, u_{caui} and i_{caui} are the SM output voltage, capacitor voltage and capacitor current of the i-th SM, respectively, as shown in Fig. 1(b).

III. ANALYSIS OF MMCS UNDER CAPACITOR DETERIORATION

A. Analysis of ERs

Normally, the chemical process, aging, etc. would cause capacitor deterioration, which would result in capacitance drop. Here, the deteriorated capacitor needs to be replaced until its capacitance drops below the threshold value, such as 80% of the rated value [14]. Consequently, the MMC would work with the different capacitances in the different SMs.

Fig. 2 shows the upper arm of phase A, where the capacitance C_{au1}~C_{aun} are supposed to be uncertain. With the voltage-balancing control in [22], the capacitor voltages in the upper arm of phase A can be kept balanced as

$$u_{cau1} = u_{cau2} = \cdots\cdots = u_{caun} = u_{cau} \tag{6}$$

Under the modulation scheme in [22], the synthesized arm voltage u_{au} for the upper arm of phase A can be expressed as

$$u_{au} = n\cdot u_{cau}\cdot\frac{1+x_{au}}{2} \tag{7}$$

with

$$x_{au} = m\cdot\sin(\omega t+\beta) \tag{8}$$

where x_{au} is the reference for the upper arm of phase A. m is modulation index. β is the phase angle.

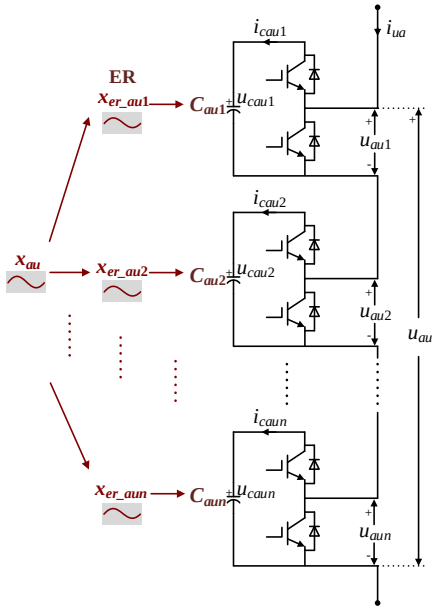

Fig. 2. n series-connected SMs in the upper arm of phase A.

Substituting (3), (4) and (6) into (7), the relationship between x_{au} and x_{er_au1}~ x_{er_aun} can be obtained as

$$x_{au} = \frac{1}{n}\sum_{i=1}^{n} x_{er\_aui} \tag{9}$$

Combining (2), (5), (6) and (8), the (10) can be obtained as

$$\frac{1+x_{er\_au1}}{C_{au1}} = \frac{1+x_{er\_au2}}{C_{au2}} = \cdots\cdots = \frac{1+x_{er\_aun}}{C_{aun}} = \frac{1+x_{au}}{C_{ave}} \tag{10}$$

with

$$C_{ave} = \frac{1}{n}\sum_{i=1}^{n} C_{aui} \tag{11}$$

where C_{ave} is the average capacitance in upper arm of phase A.

Based on (10) and (11), it can be observed that the ER x_{er_aui} for the i-th SM depends on the C_{aui}. Along with the drop of C_{aui}, the x_{er_aui} will be reduced, as shown in Table II. On the other hand, according to (8) and (10), it can be seen that a dc component would be caused in x_{er_aui}, as shown in Table III, as follows.

1) *Situation I*: if $C_{aui} > C_{ave}$, x_{er_aui} will be more than x_{au}. Here, a positive dc component would be caused in x_{er_aui}. If C_{aui} is far more than C_{ave}, the dc component in x_{er_aui} would be big.
2) *Situation II*: if $C_{aui} = C_{ave}$, the x_{er_aui} will be equal to x_{au} and there is no dc component in x_{er_aui}.
3) *Situation III*: if $C_{aui} < C_{ave}$, the x_{er_aui} will be less than x_{au}. Here, a negative dc component would be caused in x_{er_aui}. If C_{aui} is far less than C_{ave}, the dc component in x_{er_aui} would be small.

TABLE II
RELATIONSHIP BETWEEN C_{aui} AND x_{er_aui}

C_{aui}	ER x_{er_aui}
Drop	Reduced

TABLE III
DC COMPONENT IN ER

Situation	C_{aui}	ER x_{er_aui}	DC component in x_{er_aui}
I	> C_{ave}	> x_{au}	> 0
II	= C_{ave}	= x_{au}	= 0
III	< C_{ave}	< x_{au}	< 0

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Fig. 3 shows the performance of the SMs with various capacitances in the arm, which is derived from the simulation in Section V. Fig. 3(a) shows the capacitances C_{au1}~C_{au6}. The other capacitances are all 15 mF. The average capacitance C_{ave} in the arm is 14.775 mF. Among C_{au1}~C_{au6}, only C_{au1} is more than C_{ave} and the others are less than C_{ave}. Fig. 3(b) shows the dc component in x_{er_au1}~x_{er_au6}, where only the dc component in x_{er_au1} is positive and the dc components in x_{er_au2}~x_{er_au6} are all negative, which verifies the analysis in Table III. In addition, Fig. 3(c) shows the relationship among the fundamental components in x_{er_au1}~x_{er_au6}, which almost meets the (10) and verify the analysis in Table II.

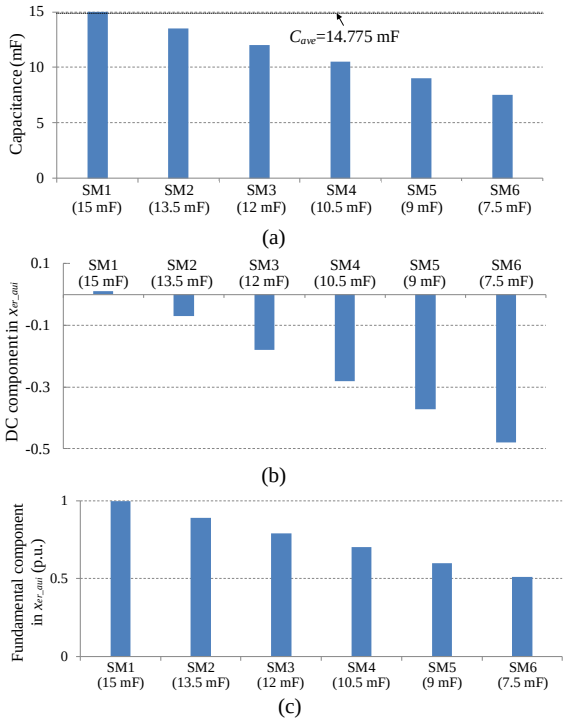

Fig. 3. (a) SM capacitance. (b) DC component in x_{er_aui}. (c) Fundamental component in x_{er_aui}.

B. SM Conduction Loss

The conduction situation of the top and bottom switch/diode (T_t/D_t and T_b/D_b) in each SM, as shown in Fig. 1(b), is listed in Table IV. The conduction losses of the switch/diode are analyzed in detail as follows.

TABLE IV
CONDUCTION SITUATIONS IN SM

i_{ua}	S	Semiconductor Current			
		T_t	D_t	T_b	D_b
≥0	1	0	i_{ua}	0	0
	0	0	0	i_{ua}	0
<0	1	i_{ua}	0	0	0
	0	0	0	0	i_{ua}

1) *Conduction losses P_{ctt} of T_t*: arm current i_{ua} flows through T_t when i_{ua}<0 and S_{aui}=1. The P_{ctt} can be expressed as [25]

$$P_{ctt\_i} = -i_{ua} \cdot S_{aui} \cdot [u_{ceo} + r_c \cdot (-i_{ua}) \cdot S_{aui}] \quad (12)$$

where u_{ceo} and r_c are switch on-state zero-current collector-emitter voltage and collector-emitter on-state resistance, respectively. S_{aui} is the switching function for the i-th SM, which can be expressed with the Fourier series expansion as $(1+x_{er\_aui})/2$ [24], [26]. Therefore, (12) can be rewritten as

$$P_{ctt\_i} = -i_{ua} \cdot \frac{1+x_{er\_aui}}{2} \cdot [u_{ceo} + r_c \cdot (-i_{ua}) \cdot \frac{1+x_{er\_aui}}{2}] \quad (13)$$

2) *Conduction losses P_{cdt_i} of D_t*: i_{ua} flows through D_t when i_{ua}≥0 and S_{aui}=1. With the Fourier series expansion of S_{aui}, the P_{cdt_i} can be expressed as

$$P_{cdt\_i} = i_{ua} \cdot \frac{1+x_{er\_aui}}{2} \cdot [u_{ceo} + r_c \cdot i_{ua} \cdot \frac{1+x_{er\_aui}}{2}] \quad (14)$$

3) *Conduction losses P_{ctb_i} of T_b*: i_{ua} flows through T_b when i_{ua}≥0 and S_{aui}=0. With the Fourier series expansion of S_{aui}, the P_{ctb_i} can be expressed as

$$P_{ctb\_i} = i_{ua} \cdot (1 - \frac{1+x_{er\_aui}}{2}) \cdot [u_{ceo} + r_c \cdot i_{ua} \cdot (1 - \frac{1+x_{er\_aui}}{2})] \quad (15)$$

4) *Conduction losses P_{cdb_i} of D_b*: i_{ua} flows through D_b when i_{ua}<0 and S_{aui}=0. With the Fourier series expansion of S_{aui}, the P_{cdb_i} can be expressed as

$$P_{cdb\_i} = i_{ua} \cdot (1 - \frac{1+x_{er\_aui}}{2}) \cdot [u_{ceo} + r_c \cdot (-i_{ua}) \cdot (1 - \frac{1+x_{er\_aui}}{2})] \quad (16)$$

From (13)~(16), it can be observed that the conduction loss of the T_t/D_t and T_b/D_b in the i-th SM is related to the ER x_{er_aui}, as shown in Table V. Combining (10) and (13)~(16), it can be seen that the capacitor C_{aui} drop causes reduced x_{er_aui}, which reduces P_{ctt_i}, P_{cdt_i} and increases P_{ctb_i}, P_{cdb_i} in the i-th SM.

TABLE V
CONDUCTION LOSSES OF SM

C_{aui}	ER x_{er_aui}	Top Switch/Diode		Bottom Switch/Diode	
		T_t	D_t	T_b	D_b
		P_{ctt_i}	P_{cdt_i}	P_{ctb_i}	P_{cdb_i}
Drop	Reduced	Reduced	Reduced	Increased	Increased

C. SM Switching Loss

Based on above analysis, although all capacitor voltage in the arm are kept balanced with the voltage-balancing control, the drop of the capacitance C_{aui} reduces ER x_{er_aui} for the SM, which would result in different switching frequencies and different switching losses for these SMs in the same arm. Under the voltage-balancing control method in [22], it is possibility that the SM with the dropped C_{aui} would reduce its switching time to reduce ER x_{er_aui}. Consequently, the capacitance drop would reduce SM switching frequency and decrease SM switching losses, as shown in Table VI.

TABLE VI
TREND OF SWITCHING LOSSES IN SMS

C_{aui}	ER x_{er_aui}	Trend of SM switching frequency	Switching losses
Drop	Reduced	Reduced	Reduced

Fig. 4 shows the SM losses with various capacitances in the same arm, which is derived from the simulation in Section V. The Infineon IGBT FZ1200R17HP4 is used in the MMC, where the losses are calculated based on the simulated current waveforms and the semiconductor specifications from the manufacturer. The junction temperature is considered to be 125°C. Along with the drop of the capacitance, as shown in Fig. 3(a), the conduction losses P_{ctt}, P_{cdt} in T_t, D_t is reduced and the conduction losses P_{ctb}, P_{cdb} in T_b, D_b is increased, as shown in Fig. 4(a), which verifies the conduction losses

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analysis in Table V. In addition, the drop of the capacitance causes the reduction of the SM switching frequency and the decrease of the switching losses P_{stt}, P_{sdt}, P_{stb}, P_{sdb} in T_t, D_t, T_b, D_b, respectively, as shown in Figs. 4(b) and (c), which verifies the switching losses analysis in Table VI. Fig. 4(d) shows the power losses of the top switch/diode T_t/D_t and bottom switch/diode T_d/D_d. It can be seen that, along with the capacitance drop, the power losses of the top switch/diode T_t/D_t is reduced and the power losses of the bottom switch/diode T_d/D_d is increased, which results in that the error between the power losses of the top switch/diode T_t/D_t and the power losses of the bottom switch/diode T_d/D_d is increased along with the capacitance drop.

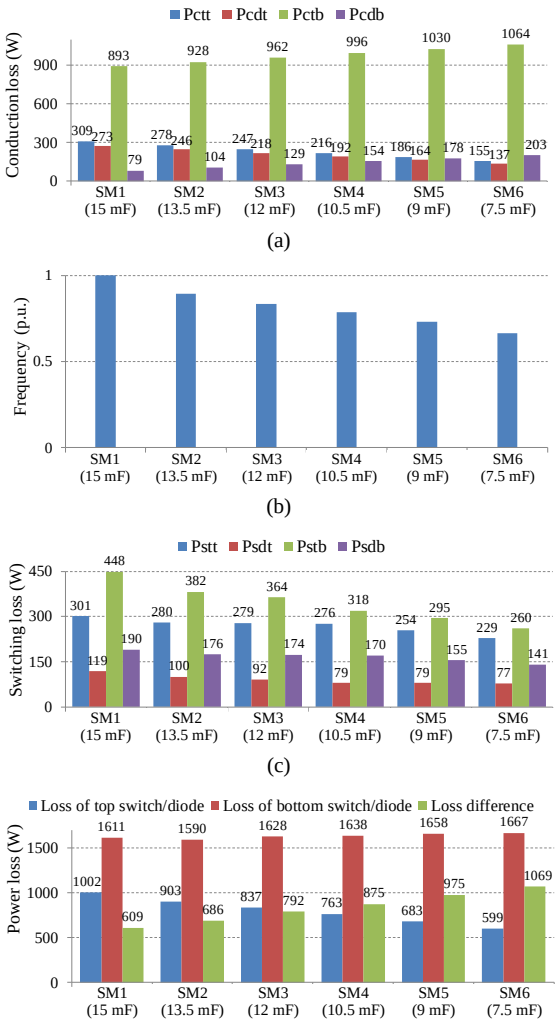

Fig. 4. Power losses of the SM1~SM6. (a) Conduction losses. (b) Switching frequency. (c) Switching losses. (d) Top and bottom switch/diode losses.

Based on above analysis, the different capacitance in the different SMs would cause different ERs for the SMs, which would cause different T_t loss, D_t loss, T_b loss and D_b loss in the different SMs, respectively. It would cause different aging speed of the T_t, D_t, T_b and D_b in the different SMs, respectively, which results in the different lifetime of the T_t, D_t, T_b and D_b in the different SMs, respectively, and therefore affects the reliability of the MMC.

IV. Proposed Power Losses Control For MMCs Under Capacitor Deterioration

A. Proposed Control Strategy

Based on aforementioned analysis, although the capacitor voltages are kept balanced, the capacitance drop causes different ERs x_{er_au1}~x_{er_aun} for the SMs in the same arm. The different ERs of the SMs would result in different SM losses in the same arm and affect the reliability of the MMC.

To improve the performance of the MMC, an ER control method is proposed for the MMC, as shown in Fig. 5, which can ensure that the ERs close to each other in the same arm. In Fig. 5, the capacitor voltage u_{caui} in the upper arm of phase A is monitored, which can be expressed as

$$u_{caui} = u_{dsm} + \Delta u_{caui} \tag{17}$$

where u_{dsm} is the dc component and Δu_{caui} is the ripple component. In the steady state situation, the arm current does not affect the dc component u_{dsm} but the ripple component Δu_{caui} [24]. In the proposed ER control, the virtual capacitor voltage (VCV) u'_{caui} is defined as

$$u'_{caui} = u_{dsm} + k_i \cdot \Delta u_{caui} \tag{18}$$

where k_i is the coefficient.

Based on the VCV u'_{cau1}~u'_{caun}, the voltage-balancing control [22] is implemented. The index list for the SMs in the arm is established through sorting VCV u'_{cau1}~u'_{caun} in ascending order. The required on-state SM number n_{on} is obtained by the arm reference x_{au}, which is calculated not only based on the MMC control such as the active power control, reactive power control and dc-link voltage control but also the circulating current control. According to the index list, required on-state SM number n_{on} and the arm current, appropriate SMs will be switched to the "On" state, and the ER x_{er_au1}~x_{er_aun} for the SMs in the same arm will be generated, which can ensure the VCV balancing as

$$u'_{cau1} = u'_{cau2} = \cdots\cdots = u'_{caun} \tag{19}$$

Combining (2), (5), (8), (17)~(19), (20) can be obtained as

$$k_1 \cdot \frac{1+x_{er\_au1}}{C_{au1}} = k_2 \cdot \frac{1+x_{er\_au2}}{C_{au2}} = \cdots\cdots = k_n \cdot \frac{1+x_{er\_aun}}{C_{aun}} \tag{20}$$

Based on (20), in order to keep the ERs x_{er_au1}~x_{er_aun} close to each other even if the capacitors C_{au1}~C_{aun} are not the same in Fig. 5, the (21) should be satisfied.

$$\frac{k_1}{C_{au1}} = \frac{k_2}{C_{au2}} = \cdots\cdots = \frac{k_n}{C_{aun}} \tag{21}$$

From (21), it can be seen that the coefficient k_1~k_n in Fig. 5 can be decided based on the SM capacitances in the arm. The capacitance in the MMC can be calculated based on the relationship among the capacitor's voltage, current and capacitance [14, 15], where the capacitor voltage is monitored and the capacitor current is obtained based on the monitored arm current and the switching function. The capacitance estimation can be achieved with the high accuracy, where the error is less than about 1%. As a result, the proposed control in Fig. 5 can achieve that the ERs x_{er_au1}~x_{er_aun} are close to each other in the same arm.

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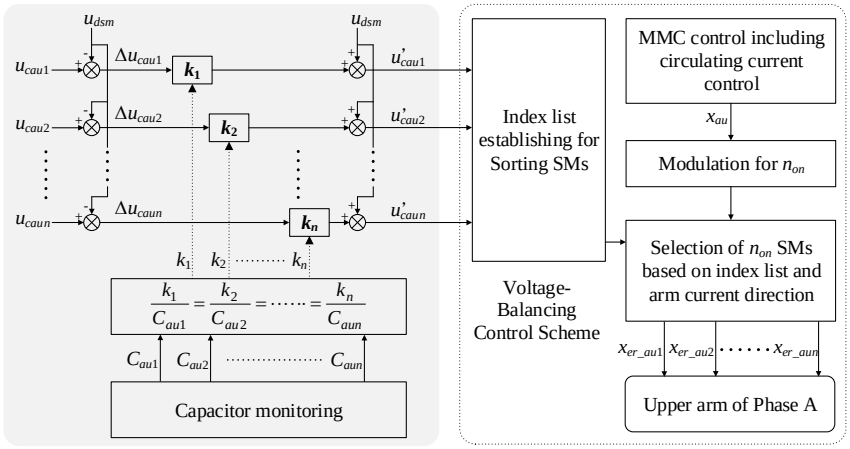

Fig. 5. Proposed ER control for the MMC under capacitor deterioration.

B. SM Power Loss Analysis Under Proposed Control Strategy

With the proposed control strategy, the VCV u'_{cau1}~u'_{caun} are kept balanced. According to (17) and (18), the dc components in u_{cau1}~u_{caun} are kept the same. The only difference is the ripple amplitude in u_{cau1}~u_{caun}, which are with the relationship as

$$k_1 \cdot \Delta u_{cau1} = k_2 \cdot \Delta u_{cau2} = \cdots\cdots = k_n \cdot \Delta u_{caun} \tag{22}$$

Suppose that the electrolytic capacitor is used in the MMC and the capacitor needs to be replaced when its capacitance drops to 80% of the rated value, according to (22), the capacitor voltage ripple amplitude would be increased by 0.25 p.u. at most. However, the capacitor voltage ripple amplitude is normally far less than the dc component u_{dsm} in the capacitor voltage [1-9]. Therefore, the impact of the different capacitor voltage ripple amplitudes on the MMC performance can be neglected, and the capacitor voltage u_{cau1}~u_{caun} can be almost regarded as close to each other. As a result, the proposed control not only keeps the ERs x_{er_au1}~x_{er_aun} close to each other, but also almost keeps the capacitor voltage balancing, which would improve the losses distribution of the SMs in the same arm, as follows.

1) *Conduction losses*: according to (13)~(16), the same x_{er_au1}~x_{er_aun} ensures that the conduction losses P_{ctt}, P_{cdt}, P_{ctb} and P_{cdb} in the SMs of the same arm would be close to each other, respectively.
2) *Switching losses*: according to the voltage-balancing method [22], it is large possibility that the SMs in the same arm would work with the close switching frequency to produce the same ERs x_{er_au1}~x_{er_aun}, which would improve the switching losses distribution of the SMs in comparison with that without the proposed control strategy.

Based on above analysis, it can be observed that the proposed control improves the conduction losses and switching losses of the semiconductors in the different SMs of the same arm, and therefore improves the reliability of the MMC. In comparison with [18] and [19], the proposed control considers both conduction losses balancing and switching losses balancing, where it not only can balance the power losses for the whole SM, but also can balance the power losses of the same type semiconductors in different SMs of the arm. In addition, owing to that the change of capacitance is normally slow, the coefficients k_1~k_n are not required to be updated in each control period, which simplifies the computation of virtual capacitor voltages and reduces the computation amount.

In the proposed control shown in Fig. 5, the coefficients k_1~k_n corresponding to the n SM capacitances C_{au1}~C_{aun} are used to regulate the n SM capacitor voltage ripples to balance the power losses distribution in the arm. If the fault occurs to the i-th SM such as switch fault, diode fault, capacitor fault and the faulty SM is detected by the fault detection methods [16], [27-29], the i-th SM would be immediately bypassed from the arm by the SM bypass switch shown in Fig. 1(b). In this situation, the coefficients k_1~k_{i-1} and k_{i+1}~k_n corresponding to the rest n-1 SM capacitances C_{au1}~$C_{au(i-1)}$ and $C_{au(i+1)}$~C_{aun} are used to produces the n-1 virtual capacitor voltages u'_{cau1}~$u'_{cau(i-1)}$ and $u'_{cau(i+1)}$~u'_{caun}, which are kept balanced by the voltage-balancing control and can ensure balancing SM power losses distribution for the rest n-1 SMs in the arm.

V. SIMULATION AND DISCUSSION

To verify the proposed control, a three-phase MMC system is built with the time-domain simulation tool PSCAD/EMTDC, as shown in Fig. 6. The circulating current is suppressed with the method in [22]. The system parameters are listed in the Table VII.

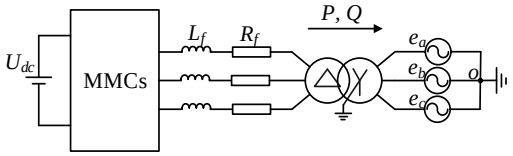

Fig. 6. Block diagram of the simulation system.

TABLE VII
SIMULATION SYSTEM PARAMETERS

Parameters	Value
DC-link voltage U_{dc} (kV)	100
Grid line-to-line voltage (kV)	220
Grid frequency (Hz)	50
Transformer voltage rating	50 kV/220 kV
Number of SMs per arm n	100
Nominal SM capacitance C (mF)	15
Inductance L_s (mH)	10
Load inductance L_f (mH)	2

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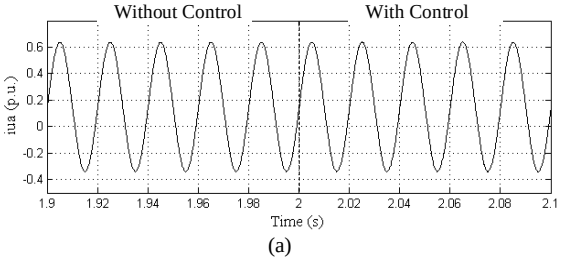
A. Enabling of Proposed Control

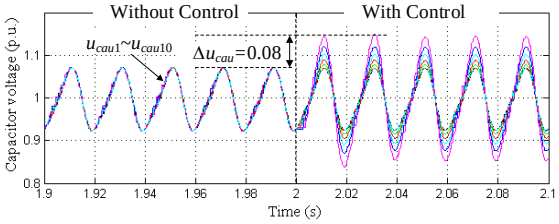
Figs. 7~10 shows the performance of the three-phase MMC, where the active power P and the reactive power Q is 100 MW and 0 MVar in the MMC system, respectively. Here, the capacitances C_{au2}~C_{au6} drop, where C_{au2}=13.5 mF, C_{au3}=12 mF, C_{au4}=10.5 mF, C_{au5}=9 mF, C_{au6}=7.5 mF, respectively, as shown in Fig. 3(a).

In Fig. 7, the proposed control is enabled since 2 s. Fig. 7(a) shows the arm current i_{ua}. Figs. 7(b) and (c) show the capacitor voltage u_{cau1}~u_{cau10}, where the peak values of the u_{cau2}~u_{cau6} are increased to 1.08, 1.09, 1.1, 1.12 and 1.15 p.u., respectively, under the proposed control so as to improve the SM power losses distribution, which meets (21) and (22) in the proposed control. Suppose that the capacitor needs to be replaced when its capacitance is less than 80% of the rated value, it can be seen that the voltage peak value of the replaced capacitor is only 1.09 p.u., which is only increased by 1.8%. The ripple amplitudes in u_{cau1}~u_{cau6} under the proposed control are shown in Fig. 7(d), which are far less than the capacitor voltages, as shown in Fig. 7(b). In addition, the THD of the arm current i_{ua} without and with the proposed control is shown in Fig. 7(e), respectively. The THD of the MMC's output voltage u_{ab} without and with the proposed control is shown in Fig. 7(f), respectively. The THD of the MMC's output current i_a without and with the proposed control is shown in Fig. 7(g), respectively. The THD of the i_{ua}, u_{ab} and i_a with the proposed control is almost the same to that without the proposed control, respectively, which shows that the proposed control has little impact on the performance of the MMC because the capacitor voltage ripple is quite small in comparison with the capacitor voltage.

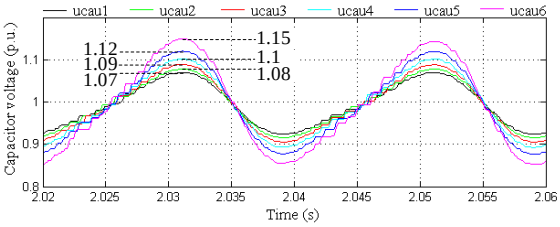
Figs. 8 and 9 show the performance of the MMC under the proposed control. Fig. 8(a) shows the dc component in x_{er_au1}~x_{er_au6}, which are quite small and can be negligible. Fig. 8(b) shows the amplitude of the fundamental component in x_{er_au1}~x_{er_au6}, which are almost the same with each other and nearly equal to that in x_{au}. As a result, the proposed control effectively improves the equivalent references in the MMC. With the proposed control, the conduction losses, switching losses and switching frequency in SM1~SM6 are nearly close to each other, respectively, as shown in Figs. 9(a)~(c). The losses of the top switch/diode and the losses of the bottom switch/diode in SM1~SM6 are nearly close to each other, respectively, as shown in Fig. 9(d). Therefore, the losses difference between the top switch/diode and the bottom switch/diode in SM1~SM6 are nearly close to each other, as shown in Fig. 9(d), which improves the power losses distribution in the arm in comparison with that without the proposed control shown in Fig. 4.



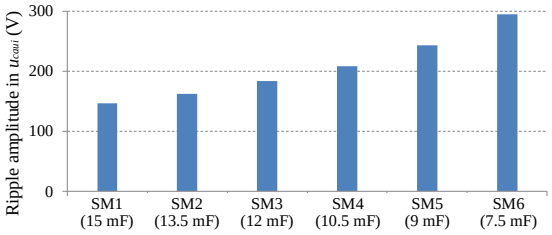
(a)



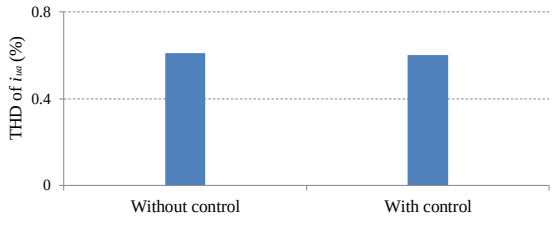
(b)



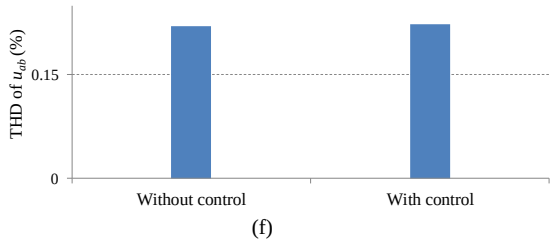
(c)



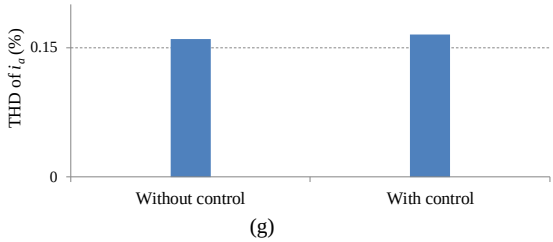
(d)



(e)

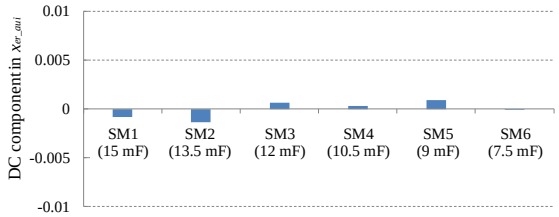


(f)



(g)

Fig. 7. (a) i_{ua}. (b) u_{cau1}~u_{cau10}. (c) u_{cau1}~u_{cau6}. (d) Ripple amplitudes in u_{cau1}~u_{cau6}. (e) THD analysis of i_{ua}. (f) THD analysis of u_{ab}. (g) THD analysis of i_a.



(a)

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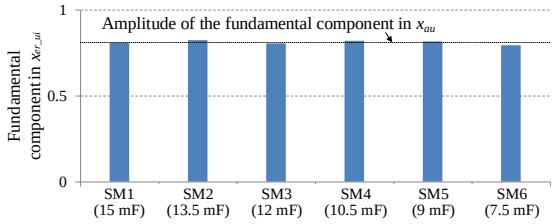

(b)

Fig. 8. (a) DC components in x_{er_au1}~x_{er_au6}. (b) Fundamental components in x_{er_au1}~x_{er_au6}.

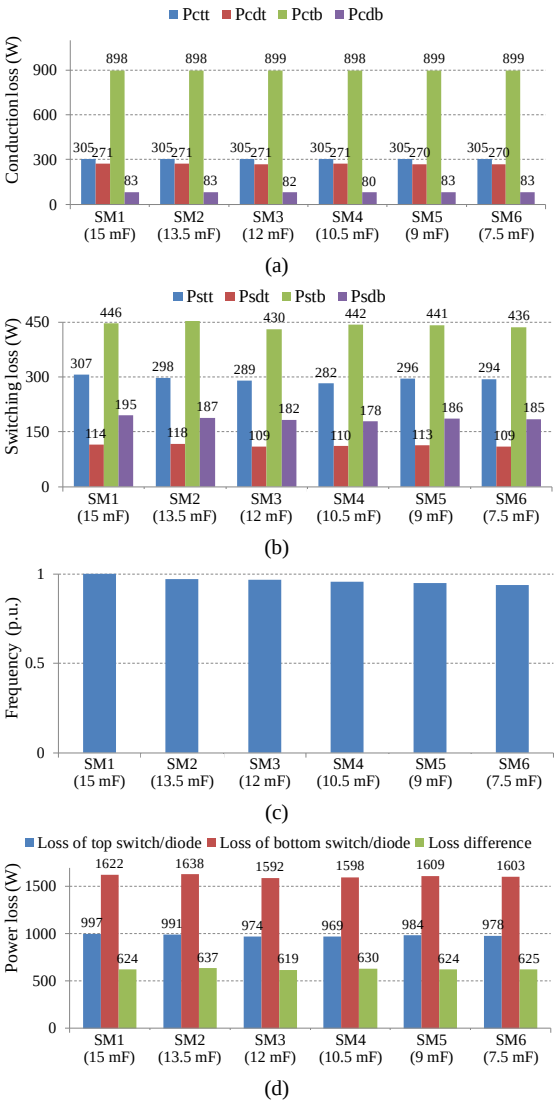

Fig. 9. Power losses in SM1~SM6. (a) Conduction losses. (b) Switching losses. (c) Switching frequency. (d) Top and bottom switch/diode losses.

Fig. 10 shows the efficiencies of the MMC without and with the proposed control, where the efficiency of the MMC without and with proposed control is quite close to each other.

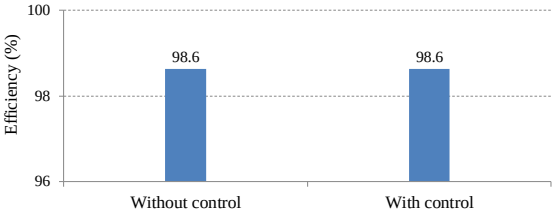

Fig. 10. Efficiency of MMCs without and with proposed control.

B. Analysis of Capacitor Voltage Ripple

In the proposed control, the different capacitor voltage ripples may be cause because of the different SM capacitances according to (21) and (22), where the SM capacitor voltage ripple would increase more if the SM capacitance drops more. Normally, the deteriorated capacitor needs be replaced until its capacitance drops below the threshold value, such as 80% of the rated value [14]. Fig. 11 shows the voltage ripple of the SM capacitor whose value drops to 80% of the rated value. In the MMC system, the rated SM capacitance is 15 mH and the corresponding equivalent capacity discharging time constant is 45 KJ/MVA, which is in the reasonable design range of the MMC [30]. From Fig. 11, it can be observed that the capacitor voltage ripple is increased along with the increase of the active power and reactive power. Even if the MMC works at the maximum power, the capacitor voltage ripple is still less than 20% and in the allowable range [18], [31].

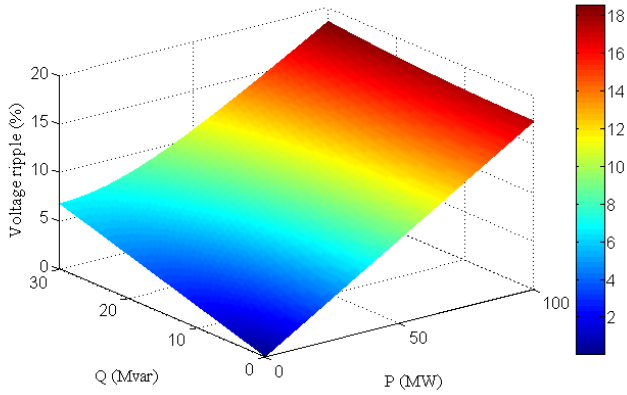

Fig. 11. Capacitor voltage ripple under various power.

C. Impact of Capacitor Monitoring Accuracy

The proposed control is based on the coefficients k_1~k_n, which are decided by the capacitor monitoring. As a result, the accuracy of the capacitor monitoring would affect the proposed control. Normally, the capacitance estimation can be achieved with high accuracy and the error is less than about 1%.

Figs. 12~15 show the semiconductor power loss errors ΔP_{ctt}, ΔP_{cdt}, ΔP_{ctb}, ΔP_{cdb}, ΔP_{stt}, ΔP_{sdt}, ΔP_{stb}, ΔP_{sdb} between SM 2 and SM 1, between SM 3 and SM 1, between SM 4 and SM 1, between SM 5 and SM 1, between SM 6 and SM 1, respectively. Fig. 12 shows the performance of the MMC without the proposed control. Figs. 13~15 show the performance of the MMC with the proposed control, where the different capacitor monitoring errors are considered for the MMC including 0, 0.5% and 1%. It can be observed that the semiconductor power loss errors would be increased along with the increase of the capacitor monitoring error. However, even the capacitor monitoring error reaches the maximum value, 1%, the semiconductor power loss errors are still quite smaller than those without proposed control. As a result, the proposed control effectively reduces the SM power losses unbalance in the arm of the MMC and improves the system reliability.

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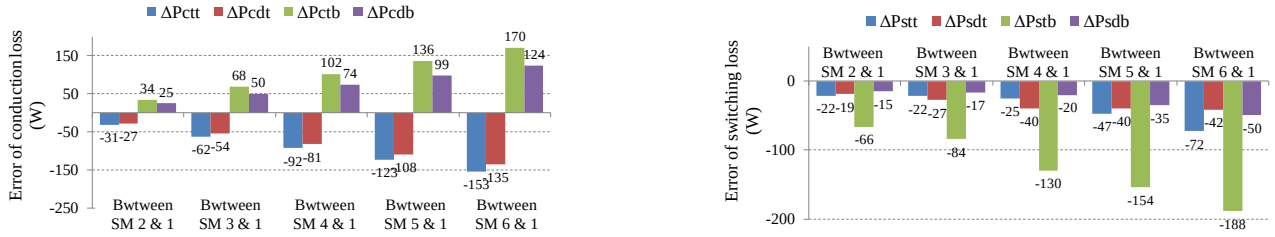
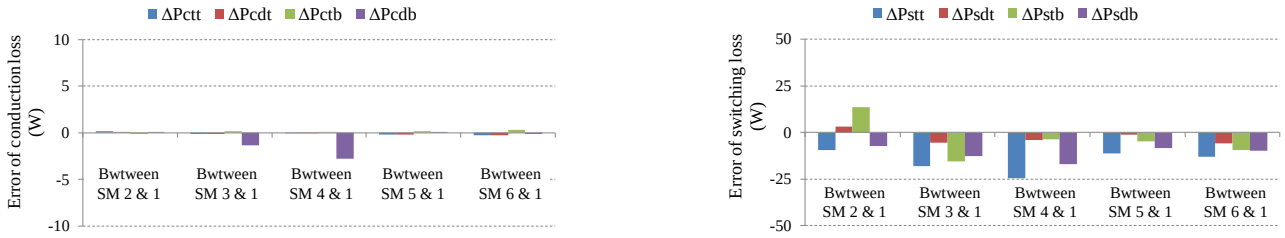


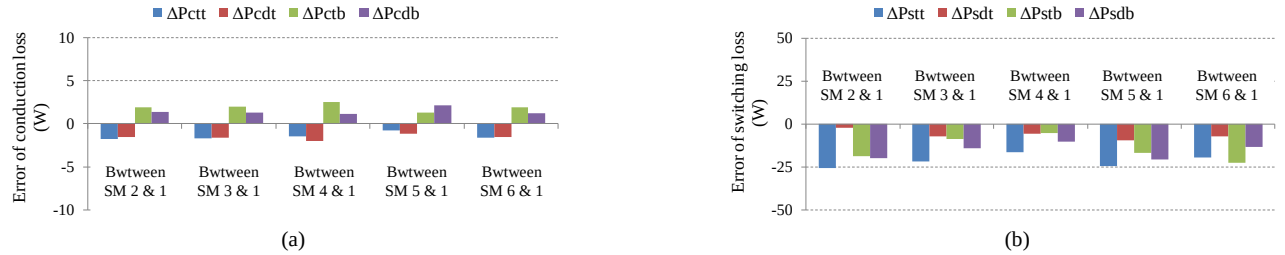
(a) (b)

Fig. 12. Semiconductor power losses errors without proposed control. (a) ΔP_{ctt}, ΔP_{cdt}, ΔP_{ctb}, ΔP_{cdb}, (b) ΔP_{stt}, ΔP_{sdt}, ΔP_{stb}, ΔP_{sdb}.



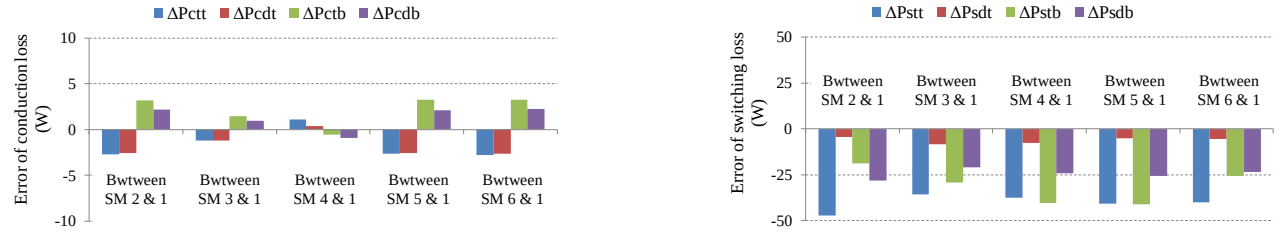
(a) (b)

Fig. 13. Semiconductor power losses errors with proposed control and 0 capacitor monitoring error. (a) ΔP_{ctt}, ΔP_{cdt}, ΔP_{ctb}, ΔP_{cdb}, (b) ΔP_{stt}, ΔP_{sdt}, ΔP_{stb}, ΔP_{sdb}.



(a) (b)

Fig. 14. Semiconductor power losses errors with proposed control and 0.5% capacitor monitoring error. (a) ΔP_{ctt}, ΔP_{cdt}, ΔP_{ctb}, ΔP_{cdb}, (b) ΔP_{stt}, ΔP_{sdt}, ΔP_{stb}, ΔP_{sdb}.

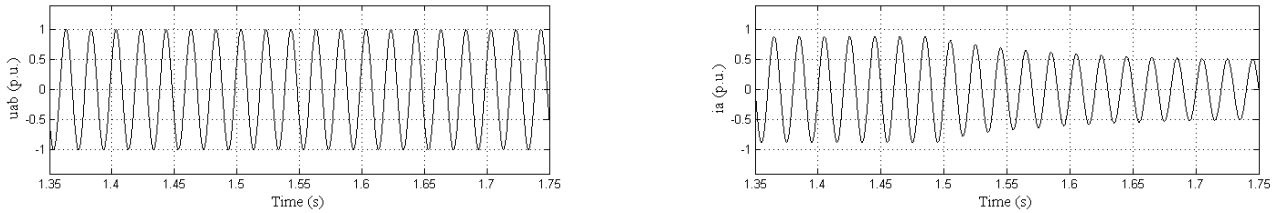


(a) (b)

Fig. 15. Semiconductor power losses errors with proposed control and 1% capacitor monitoring error. (a) ΔP_{ctt}, ΔP_{cdt}, ΔP_{ctb}, ΔP_{cdb}, (b) ΔP_{stt}, ΔP_{sdt}, ΔP_{stb}, ΔP_{sdb}.

D. Change of Power

The dynamic performance of the MMC under the proposed control is shown in Fig. 16, where the reference of the active power is step changed from 90 MW to 50 MW. Figs. 16(a)~(c) show grid voltage u_{ab}, grid current i_a and upper arm current i_{ua} in phase A. Fig. 16(d) shows the upper arm capacitor voltage u_{cau1}~u_{cau10} in phase A, where the ripple amplitudes of the u_{cau1}~u_{cau10} are reduced along with the reduction of the active power. Figs. 16(e) and (f) show the conduction losses and switching losses of the semiconductors in SM 1~6, where the MMC works at 90 MW active power; Figs. 16(g) and (h) show the conduction losses and switching losses of the semiconductors in SM 1~6, where the MMC works at 50 MW active power. It can be observed that the conduction losses and switching losses of each type semiconductor in SM 1~6 are kept balanced, respectively, with the proposed control.



(a) (b)

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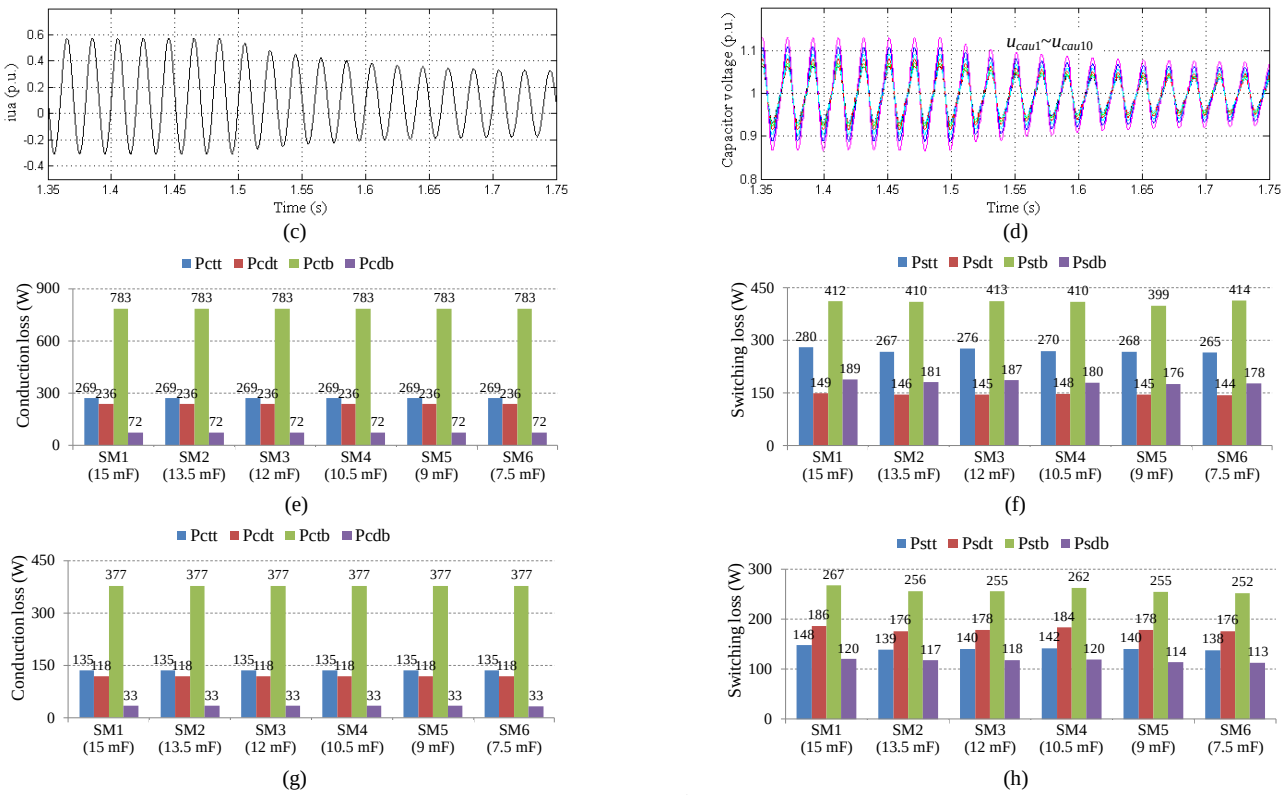


Fig. 16. (a) u_{ab}. (b) i_a. (c) i_{ua}. (d) u_{cau1}~u_{cau10}. (e) SM conduction losses at 90 MW. (f) SM switching losses at 90 MW. (g) SM conduction losses at 50 MW. (h) SM switching losses at 50 MW.

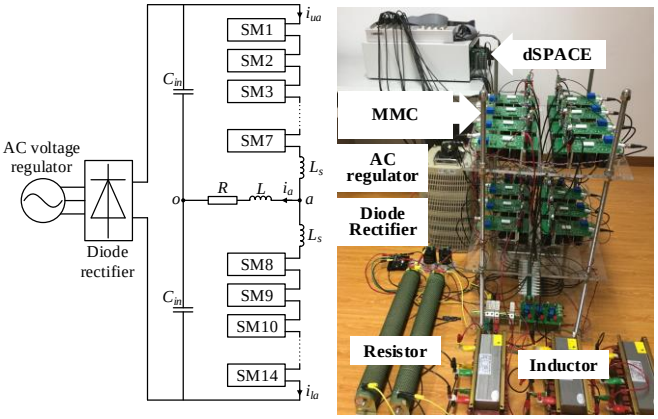
VI. EXPERIMENTAL STUDIES

A single-phase MMC with 7 SMs per arm, as shown in Fig. 17(a), is built in the laboratory. Fig. 17(b) shows the photo of the experimental circuit, where the IXFK48N60P is adopted as the switch/diode. An uncontrolled rectifier with electrolytic capacitors constitutes the dc bus voltage. The system control algorithm is implemented in the dSPACE1005 and the drive signals from the dSPACE1005 are sent to the driving panel in each SM by the optical fiber. The circulating current is suppressed with the method in [22]. The system parameters are shown in the Table VIII. To verify the proposed control, the small capacitance C_{au2}=1.761 mF and C_{au3}=1.345 are used in the experimental circuit, which are measured with the UNI-T UT612 LCR meter at 100 Hz and 25ºC.

TABLE VIII
EXPERIMENTAL SYSTEM PARAMETERS

Parameters	Value
DC-link voltage V_{dc} (V)	300
Rated frequency (Hz)	50
Capacitor C_{in} (mF)	2.2
Nominal capacitor C_{sm} (mF)	2.35
Inductor L_s (mH)	3
Load inductor L (mH)	1.8
Load resistor R (Ω)	10
Switching frequency (kHz)	5

Fig. 18 shows the performance of the MMC, where the proposed control is enabled since 0.1 s. Fig. 18(a) shows the arm current i_{ua}. Fig. 18(b) shows the capacitor voltage u_{cau1}, u_{cau2} and u_{cau3} in SM1, SM2 and SM3, respectively. Before 0.1 s, all capacitor voltages are kept balanced and the ripple amplitudes of all capacitor voltages are nearly the same with



(a) (b)

Fig. 17. (a) Experimental circuit. (b) Photo of the experimental system.

each other. After 0.1 s, the ripple amplitudes of the capacitor voltage u_{cau2} and u_{cau3} are increased under the proposed control so as to improve the SM power losses distribution, where the maximum peak value of the capacitor voltage is increased by 0.03 p.u. (1.7 V). Fig. 18(c) shows u_{cau1}, u_{cau2} and u_{cau3} under the proposed control, where the ripple amplitude of the u_{cau1}, u_{cau2} and u_{cau3} are 5.6 V, 7 V and 9.2 V, respectively, which meets the (21) and (22) in the proposed control. The ripple amplitudes of the capacitor voltages are far less than the capacitor voltages, as shown in Figs. 18(b) and (c). In addition, Fig. 18(d) shows that the THD of the upper arm current i_{ua} with the proposed control is almost the same to the THD of the i_{ua} without the proposed control, which shows that the proposed control has little impact on the performance of the MMC.

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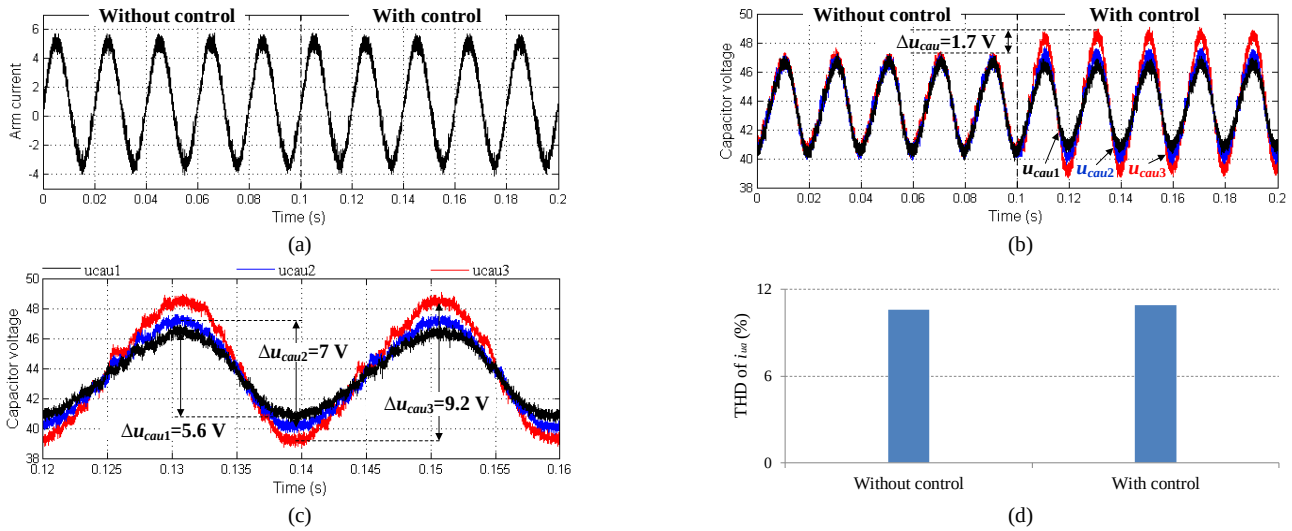
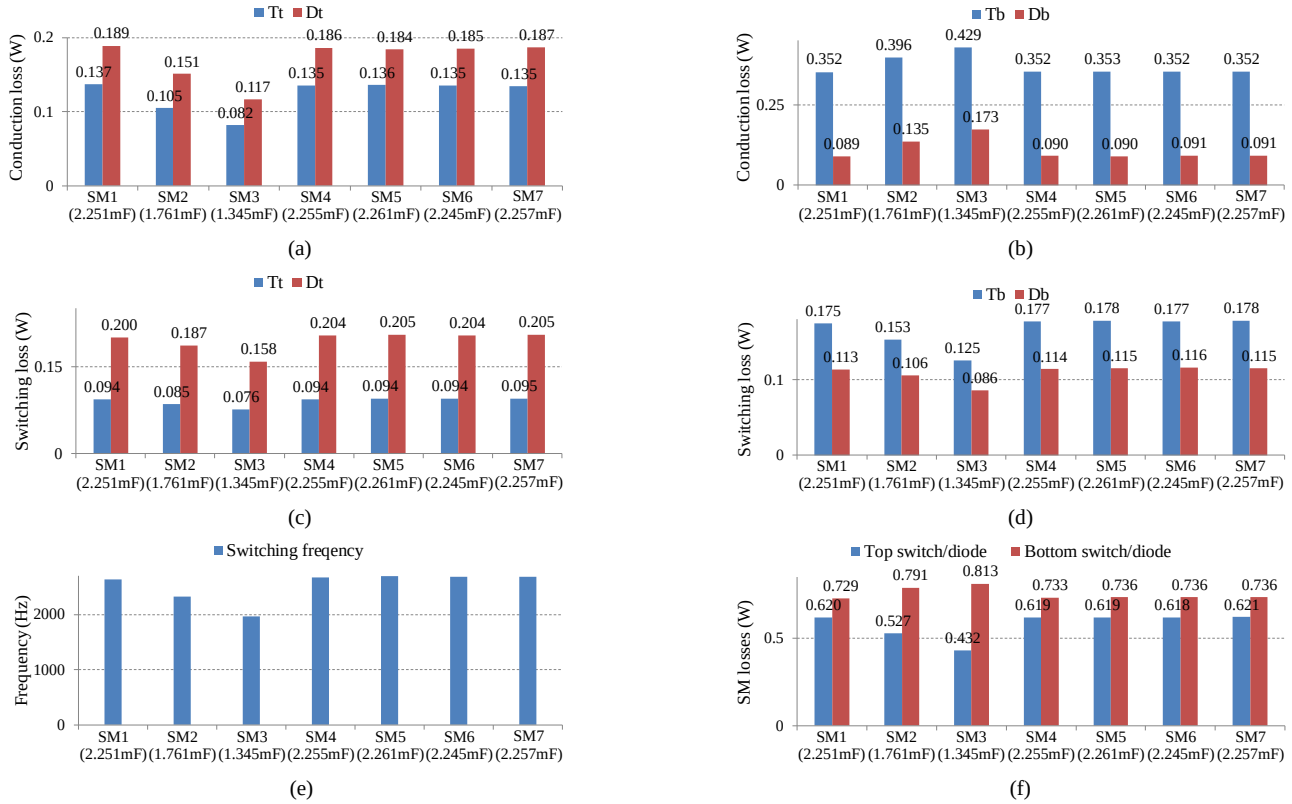


Fig. 18. Performance of MMCs. (a) i_{ua}. (b) u_{cau1}~u_{cau3}. (c) u_{cau1}~u_{cau3}. (d) THD analysis of i_{ua}.

Figs. 19 and 20 show the losses of the MMC with and without the proposed control, respectively, which includes the losses in SM1~SM7. The losses are calculated based on the experimental current and the semiconductor specifications from the manufacturer.

If the proposed control is not adopted, as shown in Fig. 19, along with the drop of the capacitance C_{au2} in SM2 and the capacitance C_{au3} in SM3, the conduction losses of T_t, D_t are gradually reduced from SM2 to SM3, respectively; the conduction losses of T_b, D_b are gradually increased from SM2 to SM3, respectively; the switching frequency is gradually reduced from SM2 to SM3; the switching losses are gradually reduced from SM2 to SM3. Consequently, the loss difference between the top switch/diode and the bottom switch/diode is gradually increased from SM2 to SM3, which would affect the reliability of the MMC. However, if the proposed control is used, as shown in Fig. 20, the conduction losses of T_t, D_t are nearly kept the same in SM1~7, respectively; the conduction losses of T_b, D_b are nearly kept the same in SM1~7, respectively; the difference of the switching frequency is reduced among SM1~7; the switching losses in SM1~7 are quite close to each other. As a result, the losses differences between the top switch/diode and the bottom switch/diode in SM1~7 are quite close to each other, which effectively improves the reliability of the MMC under capacitor deterioration.



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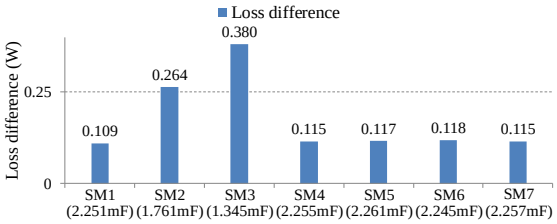
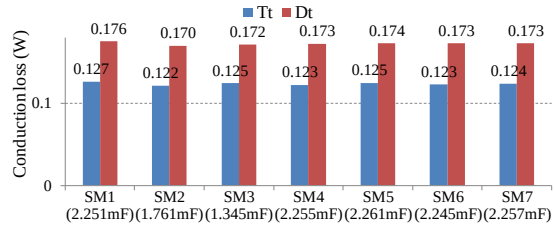
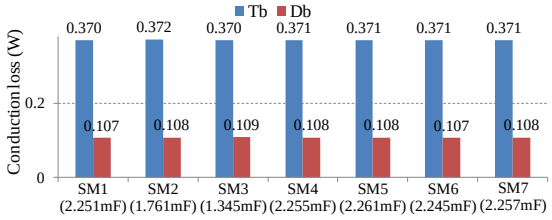


(g)

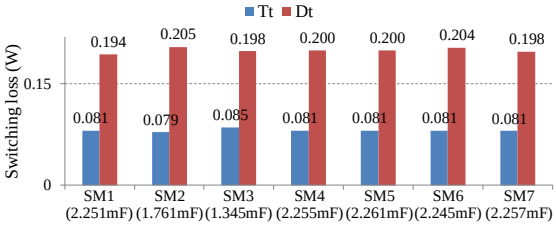
Fig. 19. Performance of MMCs without proposed control including (a) Conduction losses of T_t and D_t. (b) Conduction losses of T_b and D_b. (c) Switching losses of T_t and D_t. (d) Switching losses of T_b and D_b. (e) SM switching frequency. (f) Top and bottom switch/diode losses. (g) Loss difference.



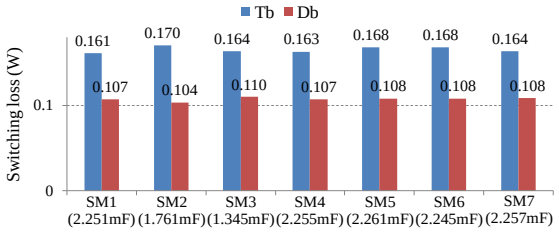
(a)



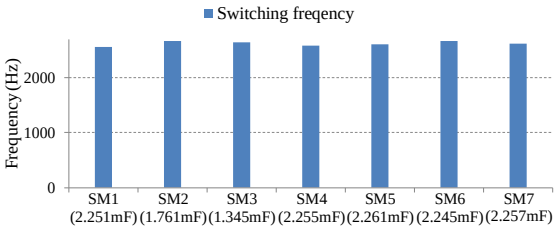
(b)



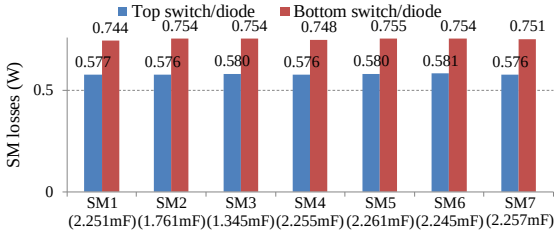
(c)



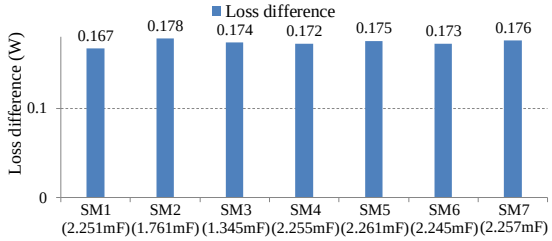
(d)



(e)



(f)



(g)

Fig. 20. Performance of MMCs with proposed control including (a) Conduction losses of T_t and D_t. (b) Conduction losses of T_b and D_b. (c) Switching losses of T_t and D_t. (d) Switching losses of T_b and D_b. (e) SM switching frequency. (f) Top and bottom switch/diode losses. (g) Loss difference.

Fig. 21 shows the efficiency of the MMC without and with the proposed control. It can be observed that the efficiencies of the MMC without and with the proposed control are quite close to each other.

Fig. 22 shows the dynamic performance of the MMC with the proposed control, where the modulation index is reduced to half. Figs. 22(a) and (b) show that the arm current i_a and the ripples of capacitor voltages u_{cau1}~u_{cau3} are reduced. With the

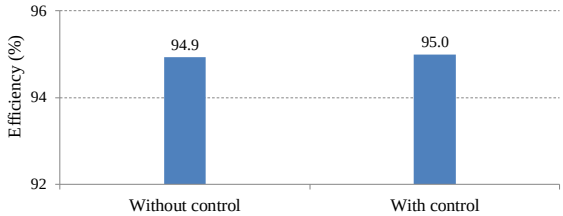


Fig. 21. Efficiency of MMCs without and with proposed control.

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proposed control, the conduction losses of T_t, D_t, T_b, D_b and the switching losses of T_t, D_t, T_b, D_b in different SMs of the arm are still kept balanced, respectively, when the modulation index is reduced to half, as shown in Figs. 22(c)~(f).

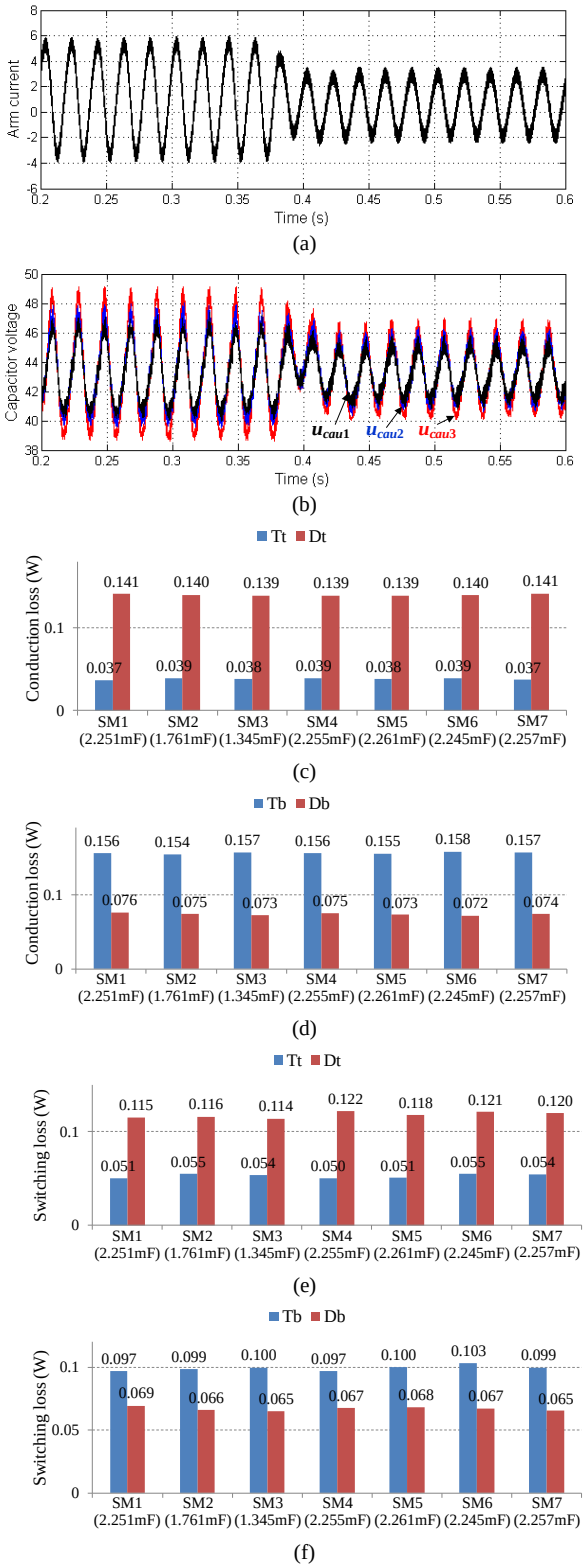

Fig. 22. Dynamic performance of MMCs with proposed control including (a) i_{ua}. (b) u_{cau1}~u_{cau3}. (c) Conduction losses of T_t and D_t. (d) Conduction losses of T_b and D_b. (e) Switching losses of T_t and D_t. (f) Switching losses of T_b and D_b.

VII. CONCLUSIONS

In this paper, the SM power losses distribution in the arm of the MMC under capacitor deterioration is analyzed in detail. The capacitor drop results in the different ERs for the SMs in the same arm and causes unbalanced SM power losses distribution in the same arm, where the losses of the switch T_t, diode D_t, switch T_b and diode D_b would be different in the SMs with different capacitances, respectively, and therefore affects the MMC reliability. An ER control method is proposed for improving the reliability of the MMC under capacitor deterioration. Through the voltage-balancing control for the virtual capacitor voltages, the ERs for the SMs in the same arm can be kept close to each other. It improves the unbalanced SM power losses distribution in the same arm, where the losses of the switch T_t, diode D_t, switch T_b and diode D_b would be close to each other in the SMs with different capacitances, respectively, and therefore improves the reliability of the MMC under capacitor deterioration. The simulation and experiment results show the effectiveness of the proposed control strategy.

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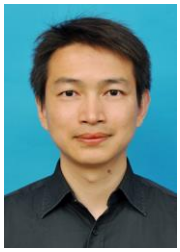

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