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Published in:
IEEE Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2019.2897061

Publication date:
2019

Document Version
Accepted author manuscript, peer reviewed version

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2897061, IEEE Transactions on Power Electronics

A Novel Seven-Level Active Neutral Point Clamped Converter with Reduced Active Switching Devices and DC-link Voltage

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Abstract— This paper presents a novel seven-level inverter topology for medium-voltage high-power applications. It consists of eight active switches and two inner flying-capacitor units forming a similar structure as in a conventional Active Neutral Point Clamped (ANPC) inverter. This unique arrangement reduces the number of active and passive components. A simple modulation technique reduces cost and complexity in the control system design without compromising reactive power capability. In addition, compared to major conventional 7-level inverter topologies such as the Neutral Point Clamped (NPC), Flying Capacitor (FC), Cascaded H-bridge (CHB) and Active NPC (ANPC) topologies, the new topology reduces the dc-link voltage requirement by 50%. This recued dc-link voltage makes the new topology appealing for various industrial applications. Experimental results from a 2.2 kVA prototype are presented to support the theoretical analysis presented in this paper. The prototype demonstrates a conversion efficiency of around 97.2% ± 1% for a wide load range.

Keywords—Multilevel Inverter, 7-level inverter, Active Neutral Point Clamped (ANPC) inverter, Flying Capacitor, Voltage Source Converter.

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I. INTRODUCTION

In recent years, multilevel converters have received increasing attention from both academia and industry for applications ranging from medium to high voltage/power conversion (e.g., >3 kV and >100 kW). This is because multilevel converters exhibit some significant advantages compared to two-level VSIs, such as improved output waveforms with lower harmonic distortion, lower electromagnetic interference, reduced stress across the semiconductor devices, and fault-tolerant operation. They are also potentially attractive for low voltage/power applications (e.g., 380 V and <100 kW) due to reduced filter size, lower switching loss and better power quality [1]. In addition, they exhibit a favorable behavior for grid-connected renewable systems, especially for solar Photovoltaic (PV) because the solid connection between the PV module and the grid via neutral point of NPC or ANPC topologies helps to keep the Common Mode Voltage (CMV) constant, which reduces the leakage current in the system. This behavior is equally appealing for motor drives and marine power supply [2].

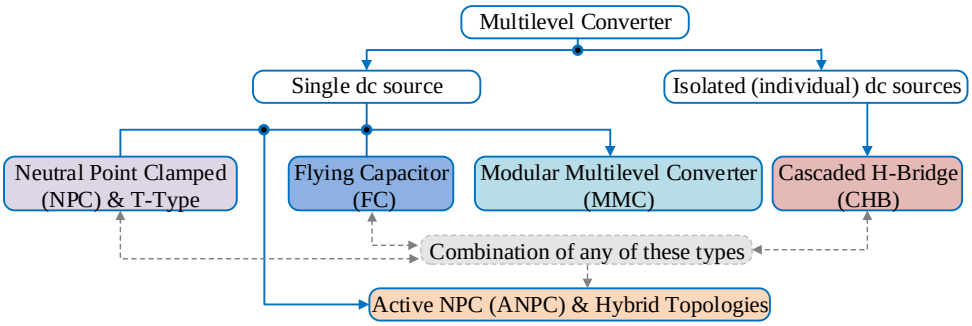

Fig. 1. A broad categorization of multilevel converter topologies.

Multilevel converter topologies have been reported in the literature since the 1970s, yet there are still new topologies being investigated and finding applications in emerging areas [3]-[8]. A broad categorization of the multilevel converters is illustrated in Fig. 1. Some of the popular multilevel topologies include the Neutral Point Clamped (NPC) converter [4], [6], [10], [12]; Flying-Capacitor (FC) converter [8], [11], [13]; Cascaded H-bridge (CHB) converter [3], [4], [5], [20]; T-Type converter [1], [5]; Modular Multilevel converter (MMC) [5], [16]; and hybrid multilevel NPC converter [8], [9], [12], [14]. A Single-phase circuit of some of the common topologies generating a seven-level output are shown in Fig. 2. The NPC converter is easy to control with simple PWM techniques; however, in many cases the unsymmetrical loading of power devices causes underutilization [19], [21]. In addition, as the number of output voltage levels increases, the dc-link capacitor voltage balancing becomes difficult, often demanding complex control strategies [5], [15]. The FC converter is controlled by multi-carrier phase shifted PWM and shows symmetrical loading of power devices and spreads losses equally across the power devices [11], [18], [20]. However, the increased number of capacitors in FC-type topologies with a large number of levels leads to more complex control scheme [4], [11], [13]. In contrast, the CHB can achieve a large number of levels by a straightforward cascaded structure of H-bridges, and loss equalization can be achieved even with simple phase

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shifted PWM technique. However, the CHB requires isolated dc sources for each H-bridges, potentially making the system bulky and expensive [1], [3]-[5], [16]. The T-Type converter uses similar PWM strategies as the NPC topology, differing only in that one power device generates the positive or negative half of the output voltage. The power devices are loaded symmetrically in pairs but the outer power devices has to block the entire dc-link voltage during operation [1], [5]. Likewise, the increased number of capacitors in higher-level FC- and MMC-type topologies lead to more complex control scheme [5], [8], [11], [13], [16].

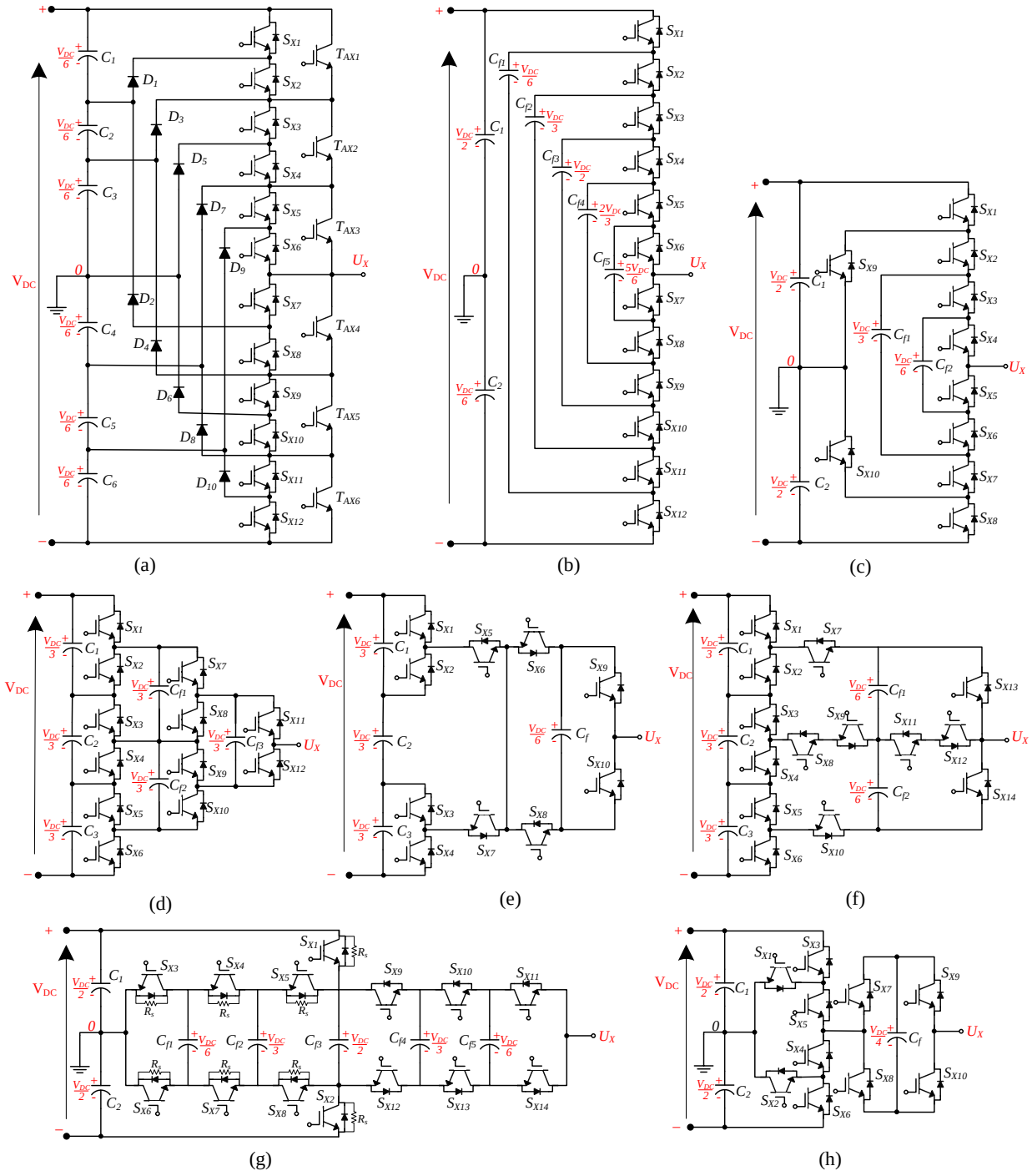

Fig. 2. Phase leg of some of the conventional seven-level inverter topologies: (a) 7L-NPC [10], [19], (b) 7L-Flying Capacitor [11], (c) 7L-ANPC [12], (d) generalized 7L-Peng model [13], (e) Hybrid Clamped 7L-ANPC [2] , (f) Hybrid 7L-ANPC-I [14], (g) Hybrid 7L-ANPC-II [12], and (h) Hybrid 7L-ANPC-III [15]. Here X ∈ (R, Y, B) phases.

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Typically, multilevel inverters requires a higher dc-link voltage which is up to two times the peak of the ac voltage output. Fig. 3 and Table I summarizes the magnitude and level of the output voltage in p.u. of some of the topologies of Fig. 2 for a given dc-link voltage ($V_{DC} = 1\,p.u.$). It shows that dc-link voltage utilization is increased by moving from mid-point clamped topologies (≤50% in Fig. 2 (a, b, c, g, and h)) to hybrid clamped topologies (≤75% in Fig. 2 (f)). For many applications (e.g. a grid-connected PV system), these circuits may require an additional front-end boost dc-dc converter, or string of series-connected PV modules to raise the dc-link voltage (e.g. up to 800 V for connection to a 400 V grid). Examples of the front-end dc-link supply for some of the common multilevel converters are given in Fig. 4. In general, these multi-stage power conversion approaches reduce system efficiency and reliability, whilst increasing the size and cost of the system. In the case of a PV system, the additional boost stage can be eliminated by connecting PV modules in series strings to produce a higher dc-link voltage, however this potentially reduces energy yield due to mismatch between the modules (e.g. as a result of shading) which will tend to offset the improved converter efficiency. Therefore, a single-stage dc-ac power converter with boost capabilities offers an interesting alternative compared to two-stage approach [13].

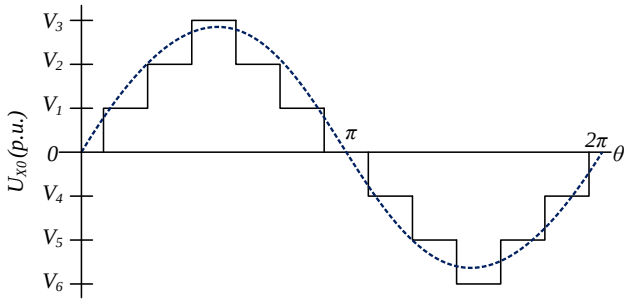
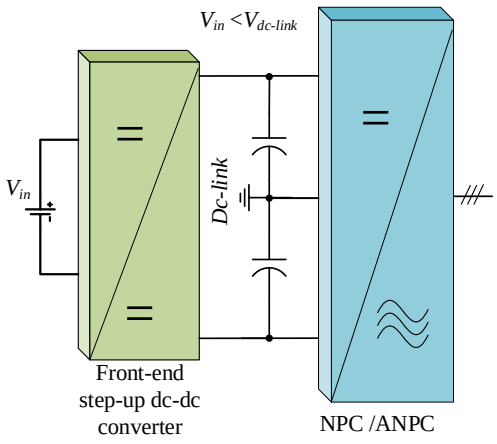


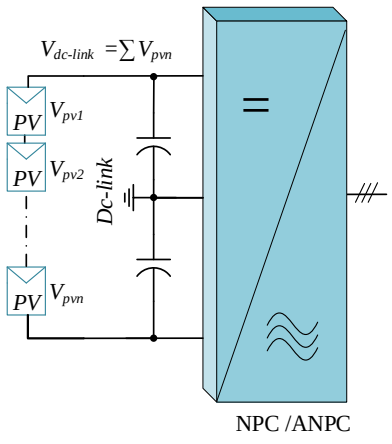
TABLE I
DIFFERENT 7-LEVEL INVERTERS AND ITS OUTPUT VOLTAGE LEVELS (P.U.).

Level	Conventional				Proposed
	Mid-point clamped	Hybrid active-clamped			
	(Fig. 2 (a, b, c, g, h))	(Fig. 2 (d))	(Fig. 2 (e))	(Fig. 2 (f))	(Fig. 4 (a))
V_1	+1/6	+1/4	+1/6	+1/4	+1/4
V_2	+1/3	+1/2	+1/3	+1/2	+1/2
V_3	+1/2	+1	+1/2	+3/4	+1
V_4	-1/6	-1/4	-1/6	-1/4	-1/4
V_5	-1/3	-1/2	-1/3	-1/2	-1/2
V_6	-1/2	-1	-1/2	-3/4	-1

Fig. 3. Output voltage levels of different seven-level inverter topologies (for $V_{dc-link} = V_{DC} = 1\,p.u.$).



(a)



(b)

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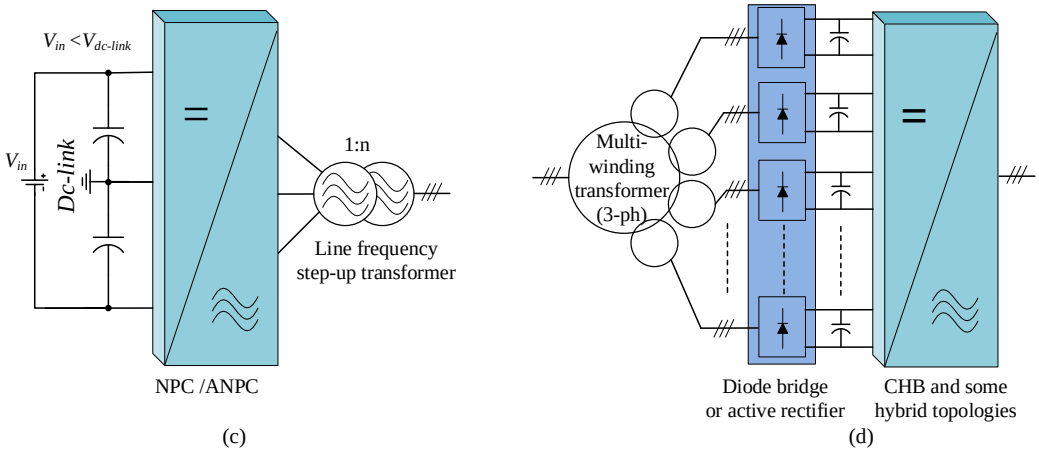

Fig. 4. Examples of front end dc-link supply for some of the common multilevel converters: (a) using a front-end step-up dc-dc converter, when $V_{in} < V_{dc-link}$, (b) connecting PV modules in series (string), where, $V_{dc-link} = \sum V_{PVn}$, (c) using a line frequency step-up transformer at the output, when $V_{in} < V_{dc-link}$, (d) using a multi-winding transformer and diode-bridge (multi-pulse) or active-rectifier for CHB (isolated) and some hybrid topologies (isolated or non-isolated).

The ANPC and some hybrid topologies, which combine the concept of NPC, FC and/or CHB have received more attention in recent times for medium power applications as they retain most of the advantages of the parent topologies [8]-[9], [12], [14] and [22]-[23]. However, they still require a large number of active and passive components and a higher dc-link voltage as shown in Fig. 3 and Fig. 4. These disadvantages present a challenge in terms of developing a new power circuit which is more attractive than the classical topologies in terms of the number of components and dc-link voltage requirements. Considering this aspect, a novel eight-switch seven-level boost-ANPC inverter (7L-Boost-ANPC) is investigated in this paper and discussed for general-purpose applications (e.g. rolling mills, fans, pumps, marine appliances, mining, traction, and a grid-connected renewable energy, etc.), which reduces the dc-link voltage requirement to half of the conventional multilevel inverter family, whilst reducing both active and passive components.

The paper is organized as follows: Section II presents the concept and analysis of the 7L-ABNPC followed by its principle of operation in Section III. A comprehensive comparison with design rules and components selection are presented in Section IV. Simulations and experimental results of the 2.2 kVA single-phase prototype are finally provided in Section V for verification, and the paper is concluded in Section VI.

II. CIRCUIT DESCRIPTION

The phase leg of the new seven-level boost-ANPC inverter consists of eight power switches and four capacitors. A schematic of the phase-leg of the inverter is shown in Fig. 5(a), where S_{X1}, S_{X2}, …, S_{X8} (X ∈ (R, Y, B) phases) are the switching devices. The corresponding modulating and switching signals are shown in Fig. 5 (b). Among the eight switches, two switches (S_{X3} & S_{X8}) are devices with a bipolar voltage blocking capability and unipolar controllability, e.g. a reverse blocking IGBT (RB-IGBT) or an IGBT/MOSFET with a series diode, and the other six (S_{X1}, S_{X2}, S_{X4}, S_{X5}, S_{X6} and S_{X7}) are standard reverse-conducting unipolar voltage devices, such as a MOSFET/IGBT. Similar to the conventional 7L-NPC, 7L-ANPC and 7L-FC topologies, the dc-link consists of two series-connected capacitors C_1 and C_2, whose rated voltages is

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half the dc-link voltage. The combination of switches S_{X1}, S_{X4} and S_{X5} or S_{X2}, S_{X6}, S_{X7} form bidirectional current carrying paths, which connects the AC terminal to the dc-link mid-point "0" (DC neutral point). The flying capacitor C_{F1} charges to V_{dc} through S_{X3} and S_{X8} in every switching cycle from the input supply V_{dc} to create a full virtual dc-bus for the 3rd level ($0.5V_{dc}$ to V_{dc} or $-0.5V_{dc}$ to $-V_{dc}$) in the output voltage waveform before the filter. Similarly, the flying capacitor C_{F2} charges to $0.25V_{dc}$ through S_{X3}, S_{X4} and S_{X6} in positive cycle and through S_{X5}, S_{X7} and S_{X8} in the negative cycle to create the 1st and 2nd levels (0 to $0.25V_{dc}$ or 0 to $-0.25V_{dc}$ and $0.25V_{dc}$ to $0.5V_{dc}$ or $-0.25V_{dc}$ to $-0.5V_{dc}$). Under ideal operation, the proposed inverter has seven output voltage levels: $\pm V_{dc}$, $\pm V_{dc}/2$, $\pm V_{dc}/4$, and 0. The corresponding phase and line voltages in a three-phase configuration are illustrated in Fig. 6(a) & (b). To make further analysis and comparison, V_{dc} is defined as the dc-link voltage of the proposed 7L ABNPC, and V_{DC} is the dc-link voltage of the conventional 7L-NPC, 7L-ANPC and 7L-FC topologies, where $V_{dc} = V_{DC}/2$.

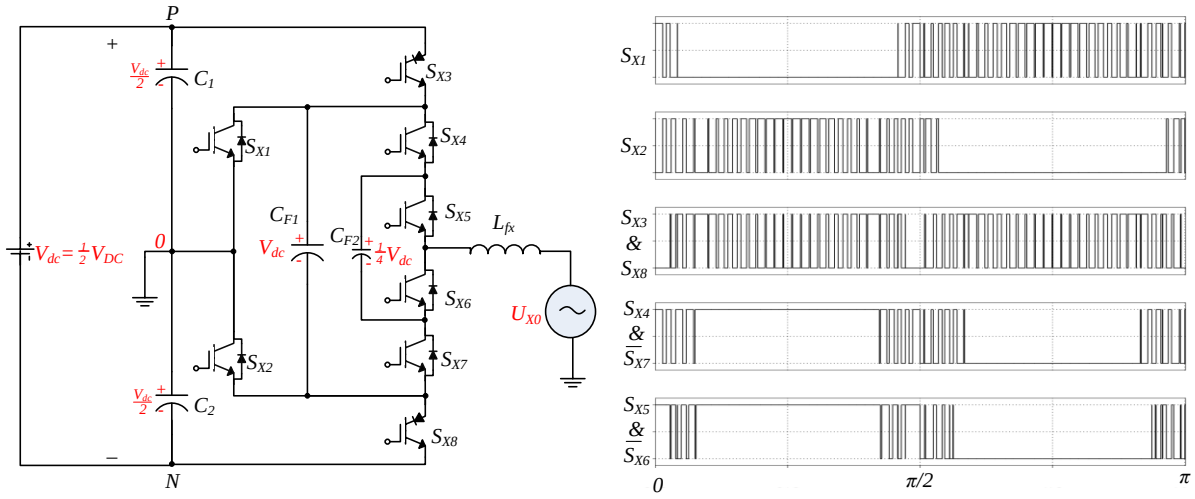

Fig. 5. A phase leg of the proposed 7L-Boost-ANPC inverter with gate signal for four switches. Here X ∈ (R, Y, B) phases.

Some of the prominent features of the new eight-switch seven-level ANPC inverter includes:

1) A reduction in the number of components (both active and passive) compared to equivalent circuits. Only eight active switches are used per-phase.
2) Full utilization of the dc-link voltage of the dc-link voltage compared to the traditional NPC, ANPC and FC inverter families.
3) The voltage stress on switches are the same as the conventional NPC, ANPC and FC inverter families, i.e. the maximum voltage stress on each switch is $V_{dc} = V_{DC}/2$.
4) The voltage stress on the dc-link capacitor is halved, which reduces the size and Equivalent Series Resistance (ESR) of the capacitor.
5) The inverter can operate at any power factor (leading/lagging), which in grid applications can be used to provide reactive power support, for example.

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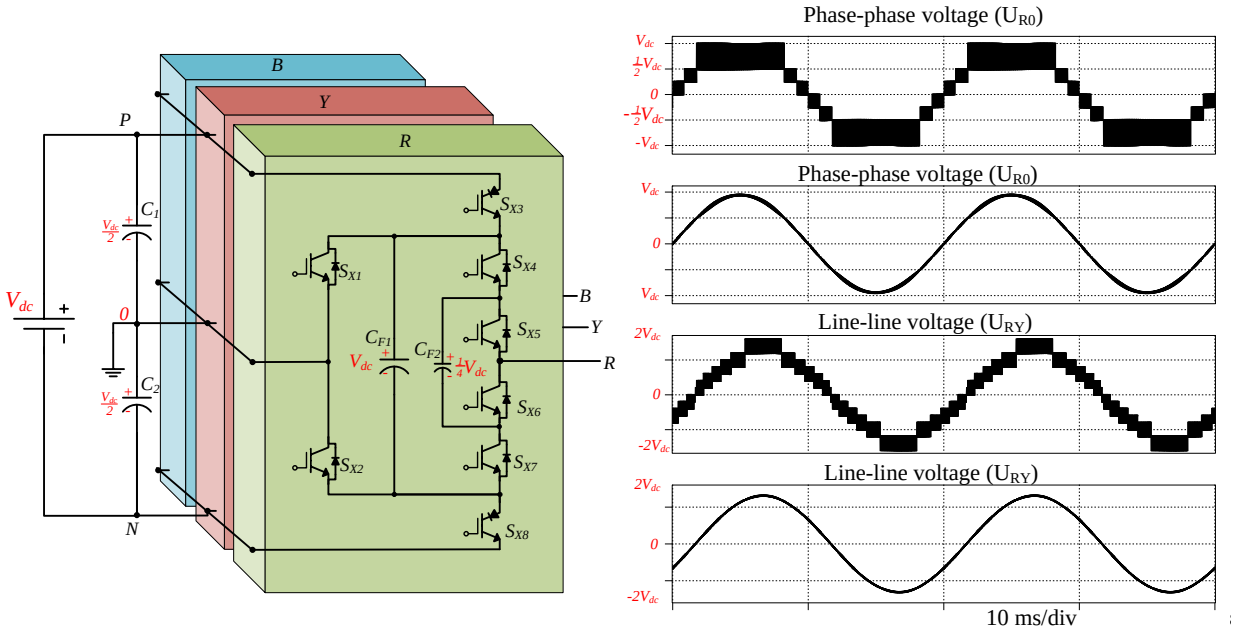

Fig. 6. Proposed seven-level three-phase inverter circuit illustrating its output phase voltage (U_{R0}) and line voltage (U_{RY}).

III. OPERATING MODES AND MODULATION STRATEGY

A. *Unity power factor operation*

The operation of the inverter for positive real power flow (DC to AC) consists of ten switching states which generate the seven-level voltage at the output using the capacitor voltages. Considering a dc-link voltage of V_{dc}, each dc-link capacitor voltage is maintained at an average of $0.5\,V_{dc}$, the voltage of the capacitor C_{F1} is maintained at V_{dc} and C_{F2} is maintained at $0.25\,V_{dc}$. The active switches (S_{X1} and S_{X2}) of the converter clamp to the neutral point to ensure the equal voltage sharing between the main switches ($S_{X3} - S_{X6}$) and create additional zero-voltage switching states. The converter switching states are shown in Fig. 7 (state A to J) and are accompanied by the corresponding current paths. The output voltage level, corresponding switching states and current through C_{F1} & C_{F2} are listed in Table II. The output current is defined as i_x, and U_{xo} represents the output voltage with reference to the neutral point. Fig. 8 shows a PWM modulation scheme for the proposed inverter in unity power factor operation with six carriers and one reference signal that are used to generate the appropriate gating signals (Level Shifted-PWM) for one phase of the inverter. The capacitor C_{F1} charges through the dc-link voltage in states A, D, F, and I, and discharges to the load in the remaining states. These charging and discharging states are uniformly distributed over the power cycle and can be switched at every switching cycles to maintain the capacitor C_{F1} voltage at V_{dc} [24]. Similarly, there are two pairs of redundant switching states in the ±1 & ±2 levels (States A and B in +1 & +2) and (States F and G in -1 & -2) which have an equal and opposite impact on C_{FC2} voltage. The effect of redundant switching states in both ±1 & ±2 levels on the C_{F2} voltage is opposite. As a result, regulation of C_{F2} voltage in both levels can be achieved by proper selection of redundant switching states. To keep the

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voltage of C_{F2} balanced, the sign of the output current i_x and the actual value of C_{F2} voltage can be used to decide which redundant switching state to select.

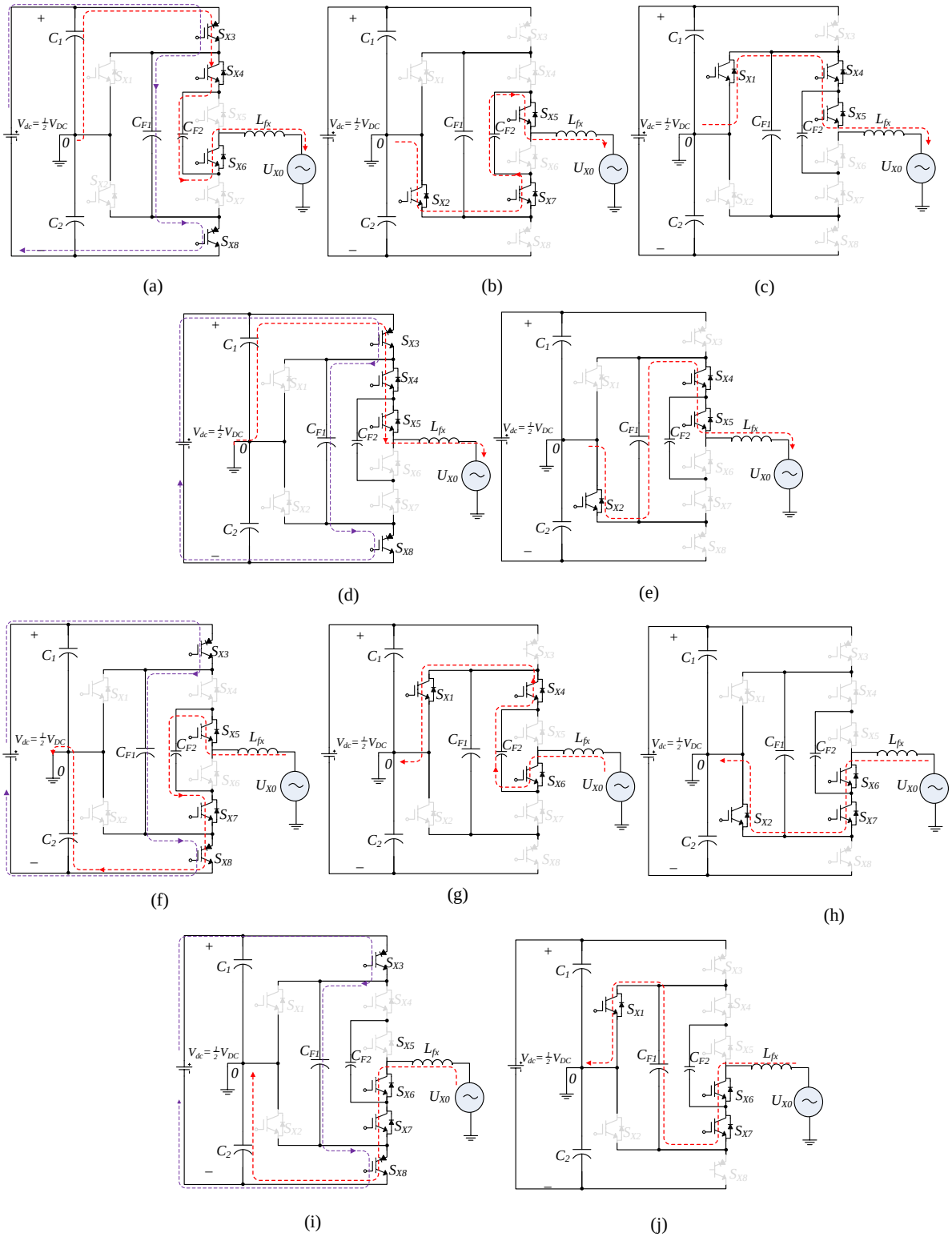

Fig. 7. Ten switching states for the 7L-ABNPC inverter: (a) State A: +1, (b) State B: +1, (c) State C: 0, (d) State D: +2, (e) State E: +3, (f) State F: -1, (g) State G: -1, (h) State H: 0, (i) State I: -2, (j) State J: -3 (red dotted-line represents the active current path, and violet dotted-line represents C_{F1} charging current path).

TABLE II
SWITCHING STATES OF THE PROPOSED 7-LEVEL INVERTER.

Switching		**Output Voltage**										***Impact to***	***Impact to***

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States	Level	(U_{x0})	S_{X1}	S_{X2}	S_{X3}	S_{X4}	S_{X5}	S_{X6}	S_{X7}	S_{X8}	i_{CF1}	i_{CF2}	V_{CF1}	V_{CF2}
A	2	$+¼V_{dc}$	0	0	1	1	0	1	0	1	i_{cf}	i_x	↑	↑
B		$+¼V_{dc}$	0	1	0	0	1	0	1	0	0	$-i_x$	—	↓
C	1	0	1	0	0	1	1	0	0	0	*0*	*0*	—	—
D	3	$+½V_{dc}$	0	0	1	1	1	0	0	0	i_{cf}	*0*	↑	—
E	4	$+V_{dc}$	0	1	0	1	1	0	0	0	i_x	0	↓	—
F	5	$-¼V_{dc}$	0	0	1	0	1	0	1	1	i_{cf}	i_x	↑	↑
G		$-¼V_{dc}$	1	0	0	1	0	1	0	0	*0*	$-i_x$	—	↓
H	1	0	0	1	0	0	0	1	1	0	*0*	*0*	—	—
I	6	$-½V_{dc}$	0	0	1	0	0	1	1	1	i_{cf}	*0*	↑	—
J	7	$-V_{dc}$	1	0	0	0	0	1	1	0	$-i_x$	*0*	↓	—

Note: "—" means no impact; "↓" means decrease; "↑" means increase.

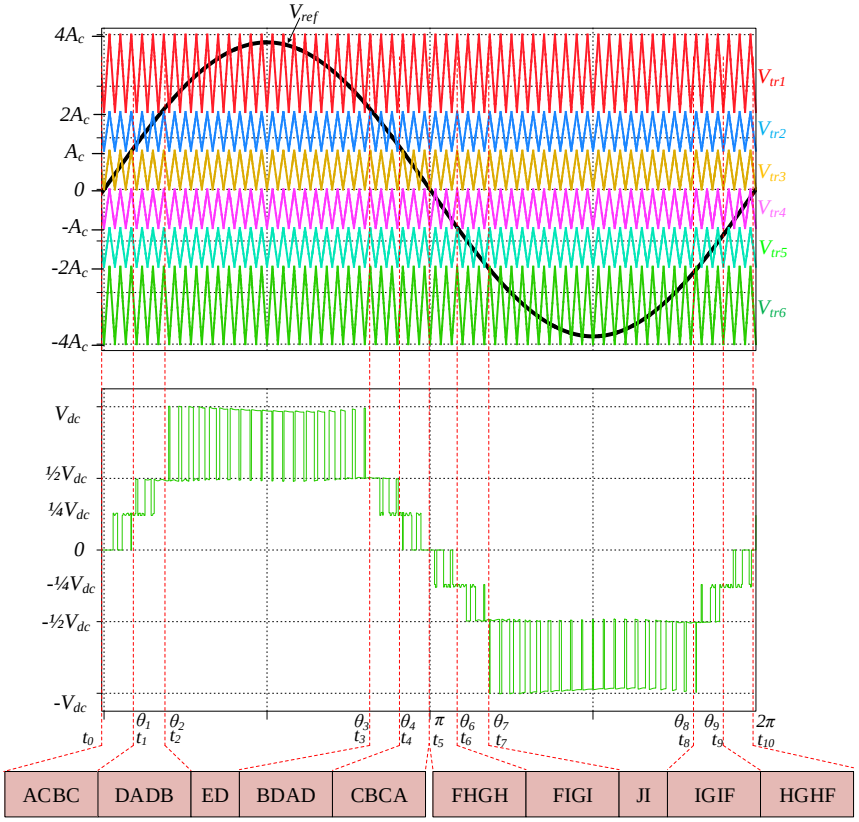

Fig. 8. Level Shifted PWM (LS-PWM) of the 7L-ABNPC inverter showing voltage level and corresponding switching states.

From Fig. 8, the modulation index M is defined as:

$$\mathrm{M} = \frac{V_{ref,max}}{4A_c} \tag{1}$$

where, $V_{ref,max}$ is the maximum amplitude value of the reference waveform $V_{ref} = 4A_c \sin(2\pi f_{ref} t)$ and A_c is the amplitude of the carrier waveform. At $t = t_1$, $V_{ref} = A_c$ and $t = t_2$, $V_{ref} = 2A_c$. Using this, the time t_1 and t_2 and corresponding angle $\theta_1$and θ_2 can be calculated as:

$$t_1 = \frac{sin^{-1}\left(\frac{1}{4}\right)}{2\pi f_{ref}} \iff \theta_1 = sin^{-1}\left(\frac{1}{4}\right) \tag{2}$$

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$$t_2 = \frac{sin^{-1}\left(\frac{1}{2}\right)}{2\pi f_{ref}} \Leftrightarrow \theta_2 = \frac{\pi}{6} \tag{3}$$

where f_{ref} is the frequency of the reference waveform.

Using (2) and (3), θ_3, θ_4, …, θ_9 can also be calculated, as $\theta_3 = \pi - \theta_2$, $\theta_4 = \pi - \theta_1$, $\theta_6 = \pi + \theta_1$, $\theta_7 = \pi + \theta_2$, $\theta_8 = 2\pi - \theta_2$, $\theta_9 = 2\pi - \theta_1$ from which t_3, t_4, …, t_{10} can be calculated as and when necessary.

Using the above conduction time and angle, switching pattern for each voltage level are discussed in details as below:

i) Level $+V_{dc}/4$ $[t_0 \le t \le t_1$ and $t_4 \le t \le t_5$ or $0 \le \theta \le \theta_1$ and $\theta_4 \le \theta \le \pi]$: To keep the voltage of C_{F2} at $+V_{dc}/4$ in the +1 level, switching states ACBC… from $t_0 \le t \le t_1$, and switching states CBCA… from $t_4 \le t \le t_5$ are used. When the output current is positive and the measured voltage of C_{F2} is lower than its reference value, then states B and F are chosen to charge C_{F2}. In this way, the C_{F2} voltage can be balanced at the reference value. The redundant switching states helps to balance the C_{F2}, whilst clamping the C_{F2} to V_{dc} for the next higher voltage level (Level +2).

In level +1, the constituent of the phase voltage (U_{X0}) can be expressed as:

$$U_{X0} = \begin{cases} V_{C1} - V_{CF2} = \frac{1}{2}V_{dc} - \frac{1}{4}V_{dc} = +\frac{1}{4}V_{dc}, & \text{State A} \\ 0, & \text{State C} \\ V_{CF2} = +\frac{1}{4}V_{dc}, & \text{State B} \end{cases} \tag{4}$$

ii) Level $+V_{dc}/2$ $[t_1 \le t \le t_2$ and $t_3 \le t \le t_4$ or $\theta_1 \le \theta \le \theta_2$ and $\theta_3 \le \theta \le \theta_4]$: Similarly in level $+V_{dc}/2$ from $t_1 \le t \le t_2$ and $t_3 \le t \le t_4$, the voltage across C_{F2} is maintained constant by appropriately choosing the redundant states A and B in combination with switching state D. Hence, switching states DADB… and BDAD… maintains the voltage of C_{F2} at $+V_{dc}/4$, whilst producing the +2 level at the output. The continuation of State A in every alternate switching cycle also helps to clamp the capacitor C_{F1} to V_{dc} for the next higher voltage level (Level +3).

In level +2, the constituent of the phase voltage (U_{X0}) can be expressed as:

$$U_{X0} = \begin{cases} V_{C1} - V_{CF2} = \frac{1}{2}V_{dc} - \frac{1}{4}V_{dc} = +\frac{1}{4}V_{dc}, & \text{State A} \\ V_{C1} = +\frac{1}{2}V_{dc}, & \text{State D} \\ V_{CF2} = +\frac{1}{4}V_{dc}, & \text{State B} \end{cases} \tag{5}$$

iii) Level $+V_{dc}$ $[t_2 \le t \le t_3$ or $\theta_2 \le \theta \le \theta_3]$: Voltage level +3 ($+V_{dc}$) from $t_2 \le t \le t_3$ can be generated by appropriately switching States E and D. In every switching cycle the C_{F1} is clamped to the dc-link voltage, which keeps the phase voltage $U_{X0} = U_{X0,max} = +V_{dc}$. The range of the voltage fluctuation in C_{F1} in level ± 3, is determined by its capacitance, charging/discharging period, and load (magnitude and type of the load). Considering these factors in design (Section IV(B)), the voltage ripples on the capacitor should be limited to $\le 10\%$ of the V_{CF1}.

In level +3, the constituent of the phase voltage (U_{X0}) can be expressed as:

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$$U_{X0} = \begin{cases} V_{C1} = +\frac{1}{2}V_{dc}, & \text{State D} \\ V_{CF1} = +V_{dc}, & \text{State E} \end{cases} \quad (6)$$

iv) Level $-V_{dc}/4$ $[t_5 \le t \le t_6$ and $t_9 \le t \le t_{10}$ or $\pi \le \theta \le \theta_6$ and $\theta_9 \le \theta \le 2\pi]$: Similar to level +1, the voltage across C_{F2} is maintained at $+V_{dc}/4$ in -1 level using the redundant switching states F and G. Hence, switching states FHGH… from $t_5 \le t \le t_6$, and switching states HGHF… from $t_9 \le t \le t_{10}$ appropriately balance the voltage of C_{F2} at the reference level.

In level -1, the constituent of the phase voltage (U_{X0}) can be expressed as:

$$U_{X0} = \begin{cases} -V_{C2} + V_{CF2} = -\frac{1}{2}V_{dc} + \frac{1}{4}V_{dc} = -\frac{1}{4}V_{dc}, & \text{State F} \\ 0 = +\frac{1}{2}V_{dc}, & \text{State H} \\ -V_{CF2} = -\frac{1}{4}V_{dc}, & \text{State G} \end{cases} \quad (7)$$

v) Level $-V_{dc}/2$ $[t_6 \le t \le t_7$ and $t_8 \le t \le t_9$ or $\theta_6 \le \theta \le \theta_7$ and $\theta_8 \le \theta \le \theta_9]$: The switching states FIGI… from $t_6 \le t \le t_7$ and IGIF… from $t_8 \le t \le t_9$ maintains C_{F2} voltage at $+V_{dc}/4$, whilst producing -2 level at the output. The continuation of State I in every alternate switching cycle also helps to clamp C_{F1} to V_{dc} for the next lower voltage level (Level -3).

In level -2, the constituent of the phase voltage (U_{X0}) can be expressed as:

$$U_{X0} = \begin{cases} -V_{C2} + V_{CF2} = -\frac{1}{2}V_{dc} + \frac{1}{4}V_{dc} = -\frac{1}{4}V_{dc}, & \text{State F} \\ -V_{C2} = -\frac{1}{2}V_{dc} = +\frac{1}{2}V_{dc}, & \text{State I} \\ -V_{CF2} = -\frac{1}{4}V_{dc}, & \text{State G} \end{cases} \quad (8)$$

vi) Level $-V_{dc}$ $[t_7 \le t \le t_8$ or $\theta_7 \le \theta \le \theta_8]$: Switching States J and I from $t_7 \le t \le t_8$ are alternately switched to generate -3 level, whilst clamping the voltage of C_{F1} to V_{dc}.

In level -3, the constituent of the phase voltage (U_{X0}) can be expressed as:

$$U_{X0} = \begin{cases} -V_{C2} = -\frac{1}{2}V_{dc}, & \text{State J} \\ -V_{CF1} = -V_{dc}, & \text{State I} \end{cases} \quad (9)$$

B. Non-unity power factor operation

The operation of the inverter in the reactive mode is shown in Fig. 9, where the polarity of the output voltage and current (v_g, i_{ac}) are opposite for $\varphi > \arcsin(1/2)$. Regions II and IV belong to the positive power regions (v_g and i_{ac} have same polarity), while Regions I and III are negative power regions (v_g and i_{ac} have opposite polarity). The commutation of switches in the negative power region are illustrated in Fig. 10. These are not special or additional switching states on the top of the ten switching states as discussed in unity power factor condition (Fig. 7), but they are natural commutation states created by the polarity and direction of the output voltage and current respectively. A pink coloured

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switching device indicates it is the principal current carrying device, grey coloured device indicates that the device is off ($v_{gs} = 0$) and blue color indicates the device is naturally turned-off ($v_{gs} = 1$).

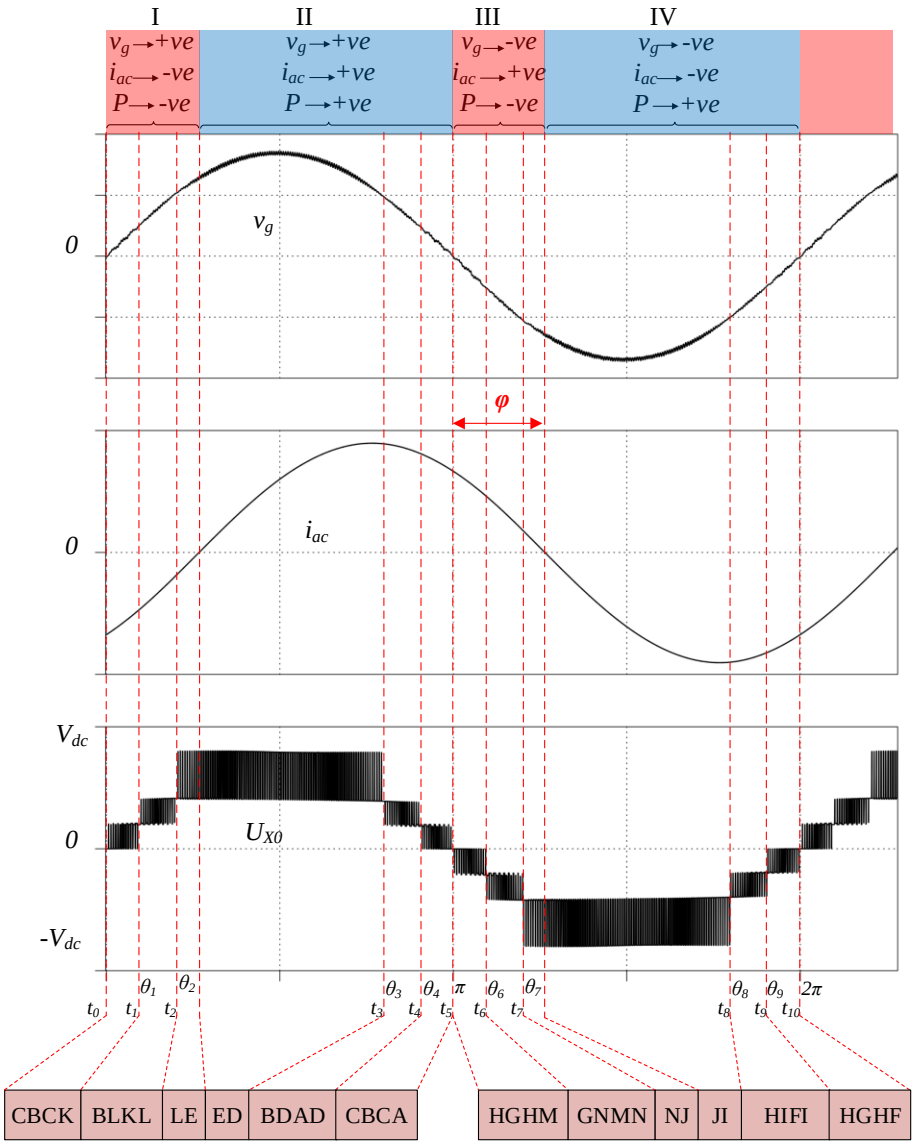

Fig. 9. Non-unity power factor operation of the inverter illustrating its waveforms and switching pattern.

Here S_{X3} and S_{X8} are unidirectional switches with bipolar voltage capability, but this does not limit the reactive power capability of the inverter. When v_g is positive and i_{ac} is negative, the current freewheels through anti-parallel diode of S_{X4} turning State A (+1 in Fig. 7) to State K (+1 in Fig. 10), where S_{X3} is naturally turned off by the direction of load current. The current free wheels through anti-parallel diode of S_{X4} and of S_{X5} in State L (+2 in Fig. 10), which previously flowed through the main switches (S_{X4} and S_{X5}) in State D (+2 in Fig. 7). Similarly, State F and State I transform to State M and State N respectively when v_g is negative and i_{ac} is positive. Irrespective of polarity of v_g and i_{ac}, switches S_{X1}, S_{X4} and S_{X5} or S_{X2}, S_{X6} and S_{X7} forms a bidirectional current path during the zero voltage state, which is common in both unity power factor and non-unity power factor modes of operation.

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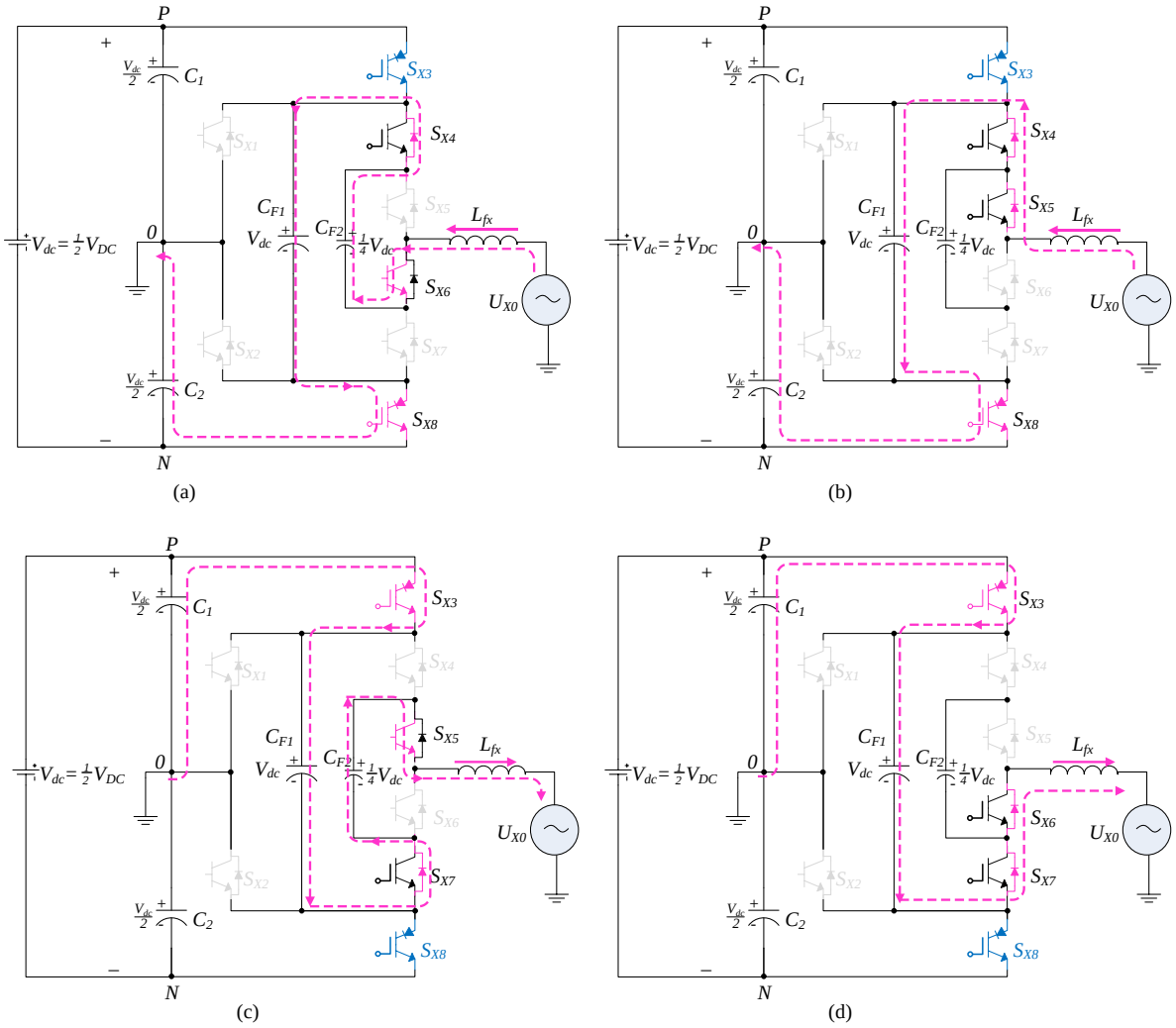

Fig. 10. Commutating states of inverter in non-unity power factor operation (a) State K, and (b) State L, (c) State M, and (d) State N.

During non-unity power factor operation, the redundant commutation states with respective phase voltage (U_{X0}) can be expressed as:

$$U_{X0}=\begin{cases}-V_{C2}+V_{CF1}-V_{CF2}=-\frac{1}{2}V_{dc}+V_{dc}-\frac{1}{4}V_{dc}=+\frac{1}{4}V_{dc}, & \text{State K}\\ -V_{C2}+V_{CF1}=-\frac{1}{2}V_{dc}+V_{dc}=+\frac{1}{2}V_{dc}, & \text{State L}\\ V_{C1}-V_{CF1}+V_{CF2}=\frac{1}{2}V_{dc}-V_{dc}+\frac{1}{4}V_{dc}=-\frac{1}{4}V_{dc}, & \text{State M}\\ V_{C1}-V_{CF1}=\frac{1}{2}V_{dc}-V_{dc}=-\frac{1}{2}V_{dc}, & \text{State N}\end{cases} \tag{10}$$

The overall operation of the inverter in both unity and non-unity power factor conditions is illustrated in Fig. 11. From this, it can be concluded that the inverter has a full reactive power capability without any special considerations, such as special modulation techniques or switch arrangements for non-unity power factor operation.

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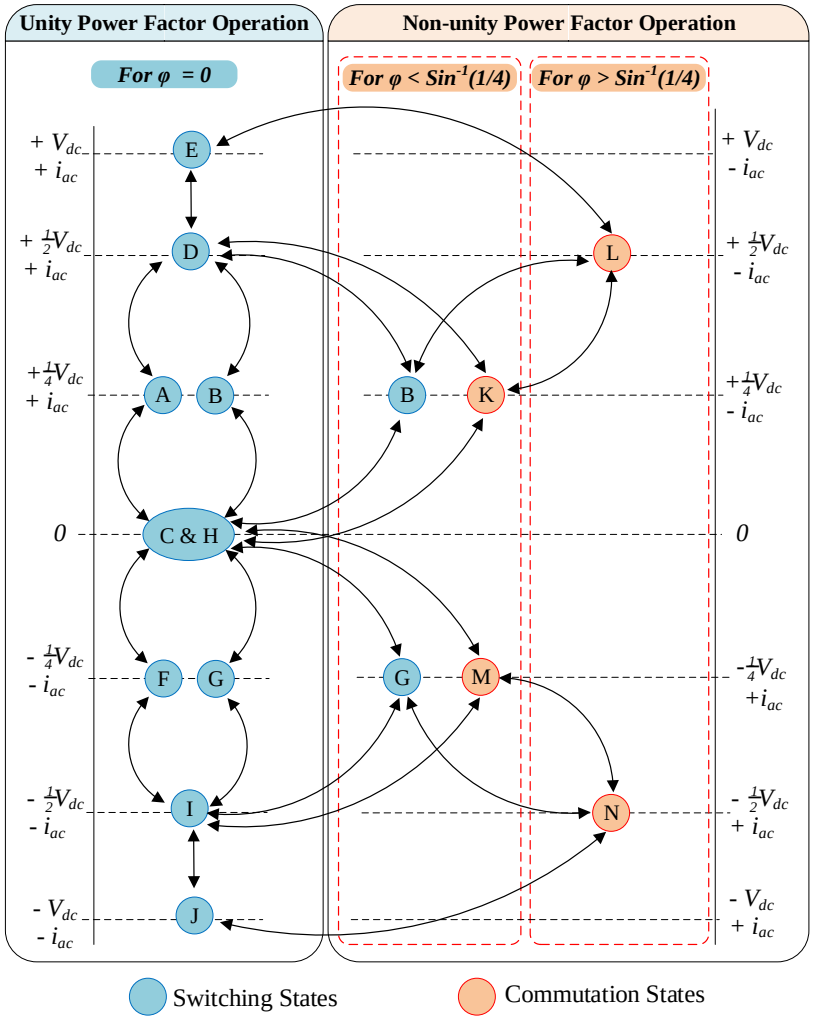

Fig. 11. Overall operation of the inverter illustrating its switching and commutation states during different power factor angles ($\varphi = 0$, $\varphi < \arcsin(1/4)$, and $\varphi > \arcsin(1/4)$).

IV. COMPARATIVE SUMMARY AND DESIGN GUIDELINES

A. *Comparison with different conventional topologies*

A comparative summary of the some of the key features of the proposed 7L inverter with the conventional 7L topologies is presented in Table III. The parameters and numbers of components included are for one phase leg only. The total semiconductor count includes all diodes (antiparallel and/or series), MOSFETs and IGBTs in the topology. For example, the total semiconductor count in the proposed topology is 18, which includes 2 RB-IGBTs or 2 MOSFETs with series diode (2 IGBTs + 2 body diodes or 2 MOSFETs + 2 series diodes and 2 body diodes) + 6 MOSFETs (6 MOSFETs + 6 anti-parallel diodes). The reduction in number of active switches to eight and the dc-link voltage requirement by 50% in the proposed 7L-ABNPC is the notable contribution compared to traditional NPC, ANPC and FC inverter family. In addition, it does not require any additional power circuitry, i.e., transformers, rectifiers, and/or isolated dc sources for the dc-link capacitors as used in CHB [3], [5], [7], [8], [20] and some hybrid topologies [2], [20]. Table IV presents a comparative summary of the proposed 7L inverter with the conventional 7L-inverter topologies in terms of voltage stress

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across major components. Here, V_{dc} is the dc-link voltage of the proposed 7L ANPC, and V_{DC} is the dc-link voltage of the conventional 7L-converter topologies, where $V_{dc} = V_{DC}/2$. It is evident that the voltage stress on the switch in the proposed topology is same or less than the conventional topologies. Further, the voltage stress on the dc-link capacitor is reduced by 50% compared to conventional topologies with mid-point grounding. Hence, considering the number of components and device stress, the proposed converter uses least number of components with low voltage stress, which comparatively reduce the overall system design cost.

TABLE III
COMPARATIVE SUMMARY OF THE PROPOSED 7L-BOOST ANPC WITH THE CONVENTIONAL 7L-INVERTER TOPOLOGIES (PER PHASE) IN TERMS OF NUMBER OF COMPONENTS AND DC-LINK VOLTAGE REQUIREMENTS.

Parameters	Proposed	Fig. 1(a)	Fig. 1(b)	Fig. 1(c)	Fig. 1(d)	Fig. 1(e)	Fig. 1(f)	Fig. 1(g)	Fig. 1(h)
No. of Active Switches	8	18	12	10	12	10	14	14	10
No. of Capacitors	4	6	7	4	6	4	5	7	3
DC- link voltage required for the same output voltage (3-ph out)	V_{dc} =½ V_{DC}	V_{DC}	V_{DC}	V_{DC}	½ V_{DC}	V_{DC}	¾V_{DC}	V_{DC}	V_{DC}

TABLE IV
SUMMARY OF VOLTAGE STRESS ON MAJOR COMPONENTS OF THE PROPOSED 7L-BOOST ANPC WITH THE CONVENTIONAL 7L-INVERTER TOPOLOGIES.

Device	Fig. 1(b)	Fig. 1(c)	Fig. 1(d)	Fig. 1(e)	Fig. 1(f)	Fig. 1(g)	Fig. 1(h)	Proposed (Fig. 5(a)
S_{X1}	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$
S_{X2}	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$
S_{X3}	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\pm\frac{1}{4}V_{DC}$
S_{X4}	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{3}{8}V_{DC}$
S_{X5}	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{8}V_{DC}$
S_{X6}	$\frac{5}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{8}V_{DC}$
S_{X7}	$\frac{5}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	$\frac{3}{8}V_{DC}$
S_{X8}	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	$\pm\frac{1}{4}V_{DC}$
S_{X9}	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	–
S_{X10}	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	–
S_{X11}	$\frac{1}{6}V_{DC}$	–	$\frac{1}{3}V_{DC}$	–	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	–	–
S_{X12}	$\frac{1}{2}V_{DC}$	–	$\frac{1}{3}V_{DC}$	–	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	–	–
S_{X13}	–	–	–	–	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	–	–
S_{X14}	–	–	–	–	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	–	–
C_1	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{4}V_{DC}$
C_2	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{4}V_{DC}$
C_3	–	–	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	–	–	–
C_{f1}	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	$\frac{1}{2}V_{DC}$
C_{f2}	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	–	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	–	$\frac{1}{8}V_{DC}$
C_{f3}	$\frac{1}{2}V_{DC}$	–	$\frac{1}{3}V_{DC}$	–	–	$\frac{1}{2}V_{DC}$	–	–
C_{f4}	$\frac{2}{3}V_{DC}$	–	–	–	–	$\frac{1}{3}V_{DC}$	–	–
C_{f5}	$\frac{5}{6}V_{DC}$	–	–	–	–	$\frac{1}{6}V_{DC}$	–	–

B. Design Guidelines

The voltage and current ratings of the active switches and diodes can be deduced from Table IV. However, to retain a comfortable safety margin, voltage and current ratings of the selected power devices should therefore be set at 150% of their theoretically calculated values.

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It should also be noted that the switches in the capacitor-charging path (S_{X3} and S_{X8}) are burdened by the charging current and the load current. The charging current depends on the duty cycle $d(t)$ of the referred switch in the current path, load current $i_{ac}(t)$ and δ, where

$$d(t) = M \sin(\omega t)\,, \tag{11}$$

$$\text{and } i_{ac}(t) = I_{ac,max}\sin(\omega t)\,, \tag{12}$$

$$\text{and } \delta = C_{FC1}/C_{DC}\,. \tag{13}$$

Here, $C_{DC} = C_1 = C_2$ is the dc-link capacitance of the circuit and is calculated considering the permissible voltage ripple across the dc-link (ΔV_{dc}) as

$$C_{DC,min} \geq \frac{I_{dc}}{2f_s \Delta V_{dc,max}}\,. \tag{14}$$

From (13) and (14), the minimum required C_{FC1} can be calculated as

$$C_{FC1,min} \geq \frac{\delta V_{dc}}{2f_s R_o\, \Delta V_{dc,max}}\,, \tag{15}$$

where, f_s is the switching frequency, R_o is the load resistance and $\Delta V_{dc,max}$ is the allowable voltage ripple into consideration.

TABLE IV
SUMMARY OF VOLTAGE AND CURRENT STRESS OF THE PROPOSED TOPOLOGY.

Switches	Voltage Stress	Current Stress
S_{X1}	$+V_{dc}$	$\approx (I_{ac,max} + \Delta i_{ac})$
S_{X2}	$+V_{dc}$	$\approx (I_{ac,max} + \Delta i_{ac})$
S_{X3}	$\pm 0.5\ V_{dc}$	$\approx \left[\frac{M}{1-M}\frac{1+\delta}{1+2\delta}+1\right] I_{ac,max}$
S_{X4}	$+0.75V_{dc}$	$\approx (I_{ac,max} + \Delta i_{ac})$
S_{X5}	$+0.25V_{dc}$	$\approx (I_{ac,max} + \Delta i_{ac})$
S_{X6}	$+0.25V_{dc}$	$\approx (I_{ac,max} + \Delta i_{ac})$
S_{X7}	$+0.75V_{dc}$	$\approx (I_{ac,max} + \Delta i_{ac})$
S_{X8}	$\pm 0.5\ V_{dc}$	$\approx \left[\frac{M}{1-M}\frac{1+\delta}{1+2\delta}+1\right] I_{ac,max}$

The current stress on C_{FC1} can be calculated as

$$i_{FC,max} \approx \frac{M}{1-M}\frac{1+\delta}{1+2\delta} I_{ac,max}\,. \tag{16}$$

where $I_{ac,max}$ is the maximum amplitude of the load current. The charging current through S_{X3} and S_{X8} not only depends on the load, but also on M and δ. The current stress reduces with lower M and higher C_{FC} values. However, small M ($M < 0.8$) reduces the dc-link voltage utilization factor and large C_{FC} ($\delta > 4$) increases the cost and size of the capacitor. As a result, a compromise should be made between minimizing current stress in S_{X3} and S_{X8} and maximizing dc-link voltage utilization (which will reduce the cost and size of the flying capacitor in the circuit).

Since, the flying capacitor C_{F1} charges in both positive and negative cycle and also in both +1 and +2 levels or -1 and -2 levels. This helps to distribute the charging current throughout the power cycle. A small inductor L_s in the range of 10

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nH - 1 µH (such as Coilcraft SER2000 Series High Current Shielded Power Inductors) may also be inserted in the circuit in order to limit the current due to instantaneous voltage difference with the dc-link [16]. Hence, with appropriately chosen M, δ and L_s ($0.8 \leq \mathrm{M} \leq 0.95, 1 \leq \delta \leq 4,$ and $10\ \mathrm{nH} \leq L_s \leq 1\ \mu\mathrm{H}$), the current on the relevant switches in the charging current path is approximately estimated to be between $2.5I_{ac,max}$ to $4I_{ac,max}$. This is generally the case for most boost type converters.

Fig. 12 illustrates the detailed switching pattern of the inverter in +1 and +2 levels showing the charging and discharging of C_{F2}. The redundant switching states A (+1) & B (+1) and F (-1) and G (-1) helps to balance the voltage of C_{F2} to $V_{dc}/4$. The charging time (t_c) of C_{F2} can be written as:

$$t_c = \begin{cases} = \frac{M\ Sin(\theta)}{f_s/2}, & M\ Sin(\theta) \leq \frac{1}{4} \\ = \frac{1-M\ Sin(\theta)}{f_s/2}, & M\ Sin(\theta) \geq \frac{1}{4} \end{cases} \tag{17}$$

From (17), the voltage ripple of C_{F2} can be calculated as:

$$\Delta V_{CF2} = \frac{\Delta Q_{F1}}{C_{F2}} = \frac{I_{ac,max}\ Sin(\theta) t_c}{C_{F1}} \tag{18}$$

Using (17) and (18), this voltage ripple can be calculated in terms of $I_{ac,max}$, f_s, and M as:

$$\Delta V_{CF2} = \begin{cases} = \frac{I_{ac,max}\ M\ Sin^2(\theta)}{C_{F2} f_s/2}, & M\ Sin(\theta) \leq \frac{1}{4} \\ = \frac{I_{ac,max}[Sin(\theta) - M\ Sin^2(\theta)]}{C_{F2} f_s/2}, & M\ Sin(\theta) \geq \frac{1}{4} \end{cases} \tag{19}$$

The charging time (t_c) and the capacitor voltage ripple (ΔV_{CF1}) functions are increasing from $0 \leq \theta \leq \arcsin(1/4)$ and is decreasing from $\arcsin(1/4) \leq \theta \leq \arcsin(1/2)$. The magnitude of ΔV_{CF2} reaches its maximum when $\sin(\theta) = 1/4M$. Using this condition, the minimum value of C_{F2} can be calculated as:

$$C_{F2,min} \geq \frac{3I_{ac,max}}{8 f_s M \Delta V_{CF2}} \tag{20}$$

It is worth noting that the maximum voltage ripple occurs when the load is purely resistive. Once the capacitance is determined under purely resistive conditions, the voltage ripple and hence the required capacitance will be smaller for a reactive load.

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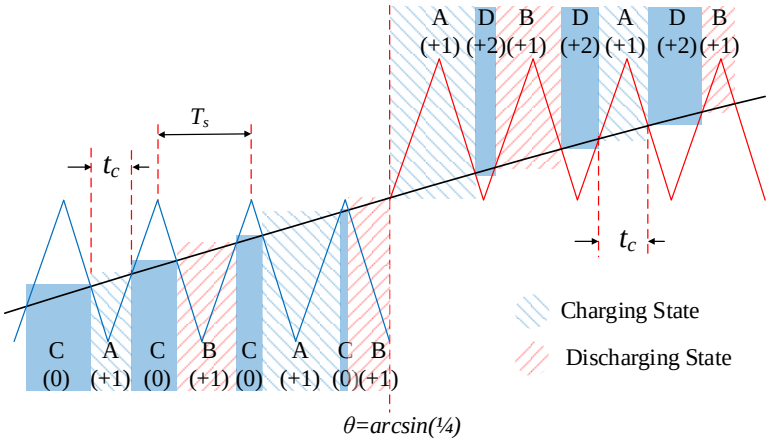

Fig. 12. Illustration of charging/discharging and control of the capacitor C_{F2} voltage.

TABLE V
PARAMETERS AND COMPONENTS USED FOR SIMULATION AND EXPERIMENT.

Description	Value/Parameter Used
Input Voltage (V_{dc})	400 V
Output voltage (v_{ac})	230 V
Power Rating (P_O)	2.2 kVA
Carrier frequency (f_s)	15 kHz
Line frequency (f)	50 Hz
dc-link capacitor (C_1 & C_2)	470 µF, 250 V
Flying capacitor (C_{FC1})	470 µF, 450 V
Flying capacitor (C_{FC2})	100 µF, 150 V
Filter inductor (L_f) & capacitor (C_f)	0.3 mH and 2.2 µF
Switches ($S_{X1} - S_{X6}$)	SCT3022AL
Diode (D_3 & D_6)	C5D50065D
Load (resistor and inductor)	2.2 kVA (30-60 Ω, 200 mH)

V. SIMULATION AND EXPERIMENTAL RESULTS

To verify the concept of the proposed inverter circuit and the theoretical analysis, several simulations using PLECS have been carried out. The parameters and component values used for both simulations and the experimental prototype are listed in Table V. Fig. 13 shows the steady state output voltage, load current, voltage across the flying capacitor and the dc-link capacitors, as well as the voltage and currents occurring across/through the switches. The fifth trace in Fig. 13(a) shows an unfiltered 7-level voltage, which is filtered to leave a pure fundamental frequency sinusoidal at the load. The inverter produces an RMS voltage of about 230 V for a 400 V dc-link voltage. Under unity power factor, the current and voltage are in phase. Also, it is evident that there is a natural balance in the voltage across the dc-link capacitors around its reference value $V_{C1} = V_{C2} = V_{dc}/2 = 200$ V (Fig. 13(a)). This natural balance is maintained under different loads, modulation indexes, power factor, with different initial capacitor voltages. As shown in Fig. 13(b) & (c), the voltage and current stress are in agreement with the analysis presented in section IV. Fig. 13(d) shows a frequency domain representation of the output voltage when using Level Shifted-PWM at a carrier frequency of 15 kHz. As evident, the THD of the output voltage and current are $<$ 2.2 %.

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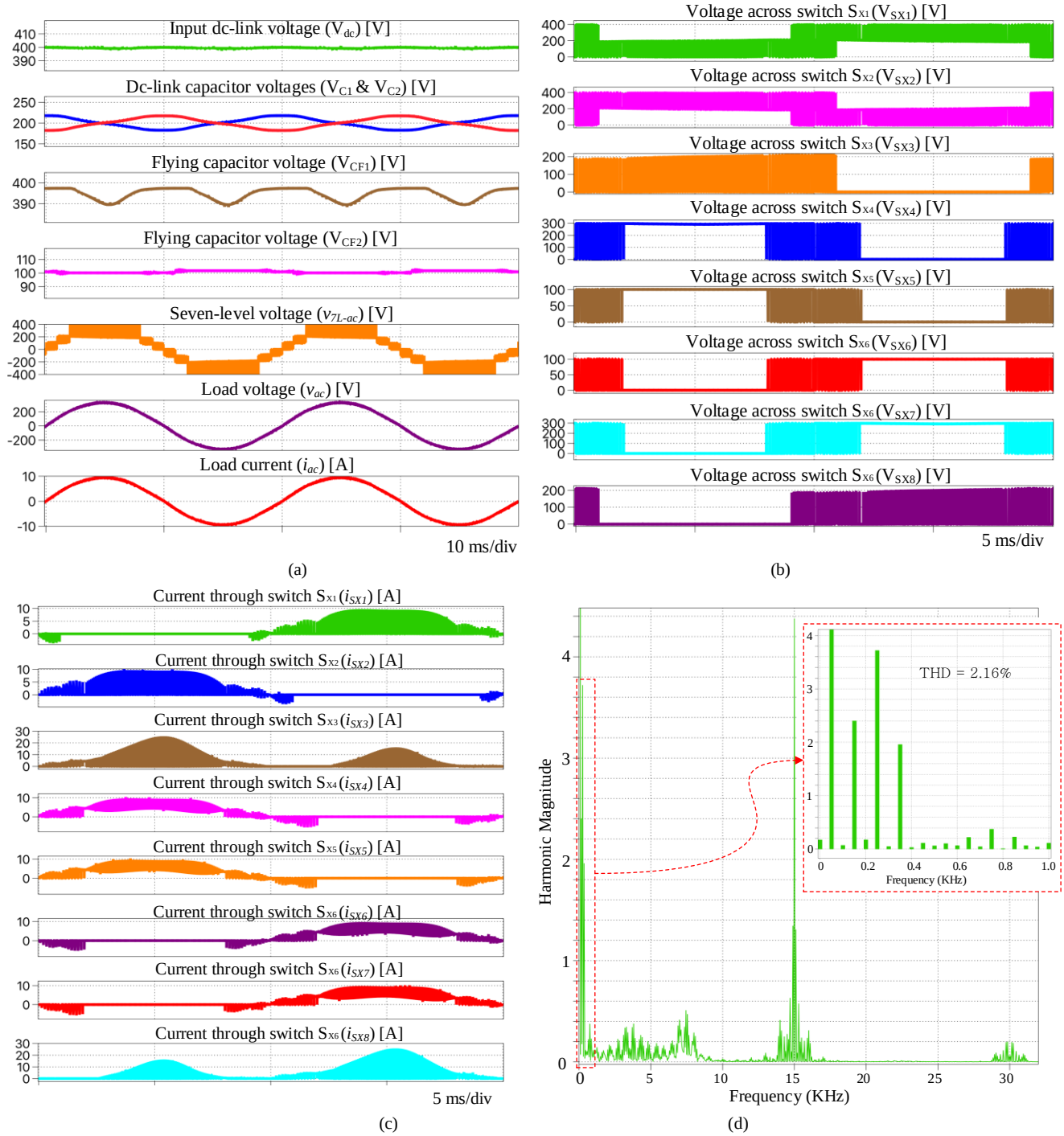

Fig. 13. Some key simulated waveforms of the proposed seven-level inverter: (a) input voltage, flying capacitors voltages, phase voltage (with and without filter), and (b) voltage stress on switches, (c) current stress on switches, and (d) harmonic spectrum of the output voltage.

The capacity of delivering reactive power has also been successfully tested for both lagging and leading power factor. Fig. 14 (a) shows the operation of the inverter in lagging power factor $\varphi_{pf} = -45^0$, and Fig. 14(b) shows the operation of the inverter in leading power factor of $\varphi_{pf} = +45^0$. Hence, without considering any special consideration (additional switching devices or switching sequence) or modulation technique, the inverter is capable of generating 7-level output voltage; which when filtered out to get pure sinusoidal voltage and current. This verify the seamless operation of the inverter as illustrated in Fig. 11 for any power factor angle.

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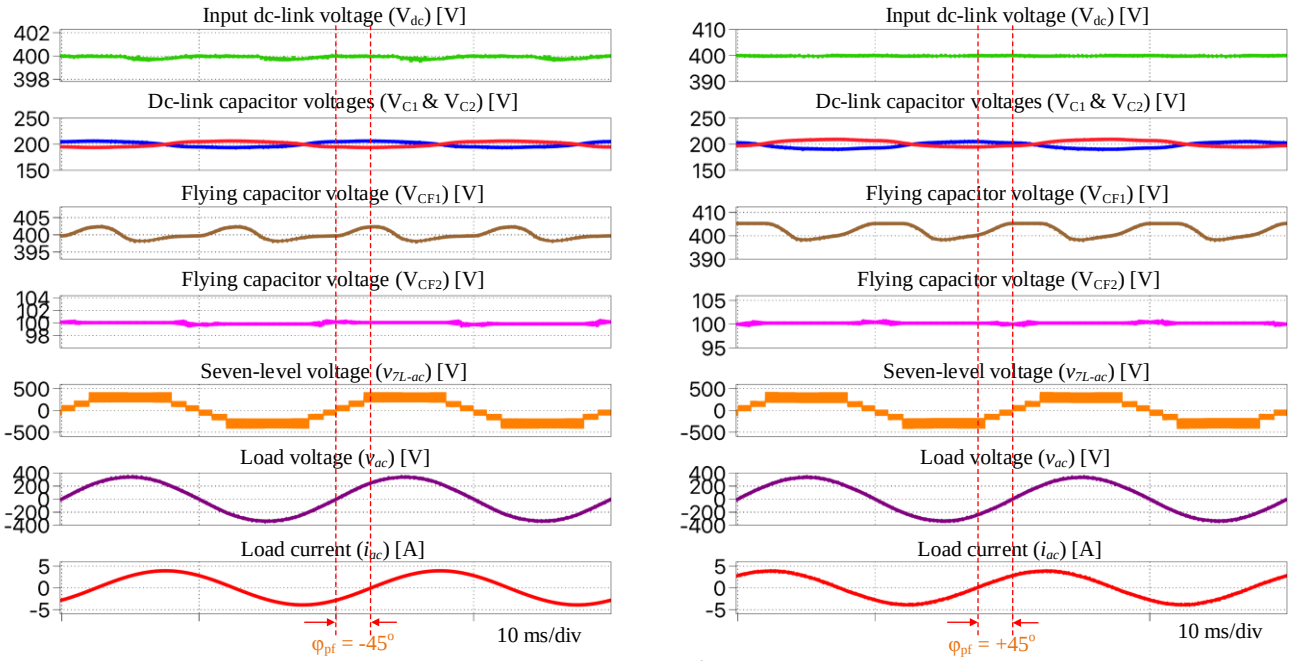

Fig. 14. Operation of the inverter during: (a) lagging power factor of $\varphi_{pf} = -45^0$ (RL load of 60 Ω + 200 mH), and (b) leading power factor of $\varphi_{pf} = +45^0$ (RC load of 60 Ω + 50 µF).

The dynamic performance of the converter under several changes in the active power is shown in Fig. 15. The converter is simulated under sudden change (step) in the load. As it can be seen, the converter track their reference voltages very well under any load changes and confirms its good performance in both transient and steady state operations.

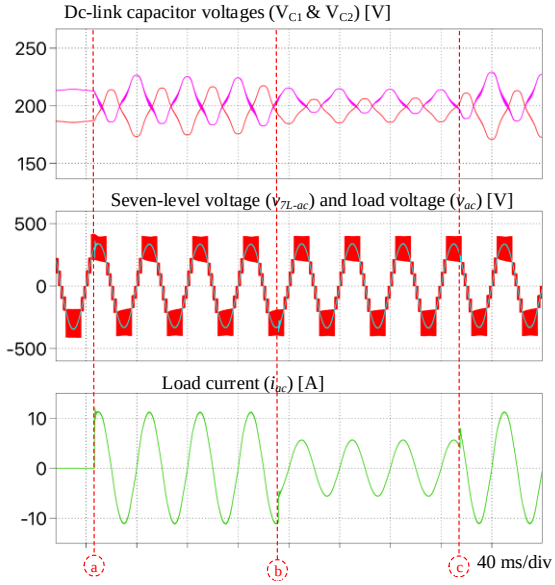

Fig. 15. Dynamic performance of the converter under several changes in the active power (a→ step change in load from no load to full load (30 Ω), b→ step change in load from full load (30 Ω) to half load (60 Ω), and c→ step change in load from half load (60 Ω) to full load (30 Ω)).

A conventional two-stage boost plus 7L-ANPC topology (Fig. 2(c)) in a system similar to Fig. 4 (a) and a single-stage system using 7L-ABNPC are simulated in PLECS in order to make a direct performance comparison. Parameters such as the input voltage (V_{in} = 400 V), load (2.2 kVA), power factor ($\cos\varphi$ = 1), switching frequency (15 kHz), modulation index (M = 0.85), and output voltage ($v_{ac} = 230\ V$) are identical for both systems. The single-stage 7L-

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ABNPC demonstrates a 2-3% higher efficiency over a wide range of loads. Using LS-PWM with feedforward control, the THD and DC-link capacitor voltage ripple is same for both topologies.

As a follow-up, based on the satisfactory simulation results and to verify and validate the practicality of the proposed 7L inverter, a compact 2.2 kVA prototype was developed as shown in Fig. 16. All switches are 650 V SiC devices (SCT3022AL) from ROHM Semiconductor. Experimental results under unity power-factor condition are shown from Fig. 17 to Fig. 21. Fig. 22 demonstrates the behaviour of the inverter when operating in a reactive power mode. It can be seen that the inverter is capable of generating a seven-level output voltage with a clean sinusoidal voltage and current.

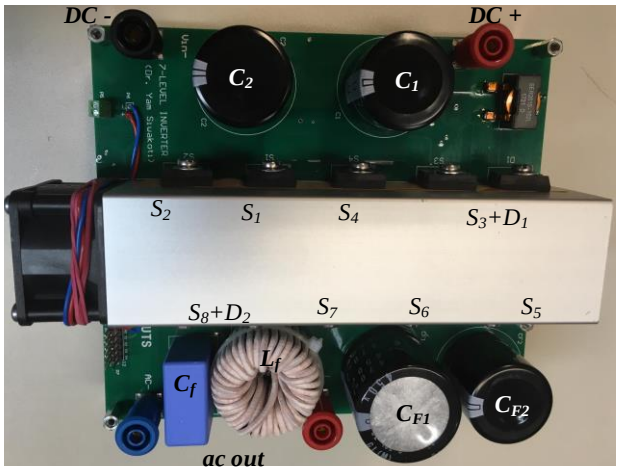

Fig. 16. Picture showing the prototype of a 2.2 kVA (single-phase) seven level inverter.

Fig. 17(a) shows the inverter input/output voltage and current waveforms with clear seven levels in the output voltage with a clear sinusoidal output voltage and current. Fig. 17(b) shows the input current of the inverter, which is continuous with a peak amplitude of around 5.5 A. Note that, a dc-link voltage of 380 V (Ch. 1) magnitude is sufficient to achieve a line-neutral output voltage of 230 V_{RMS}. This is in contrast to conventional 7L topologies which would require a nominal dc-link of close to 800 V. As shown in Fig. 18, the voltage stress on devices respectively corroborates the earlier analysis and simulation results. The peak current through S_{X3} and S_{X8} is ≈26 A as shown in Fig 19(b), which validates Fig. 13 (c) and Table IV. Fig. 20 also shows the voltages of two dc-link capacitors and two flying capacitors: Ch 1 is the upper dc-link capacitor voltage, Ch. 2 is lower dc-link capacitor voltage, Ch. 3 is C_{F1} voltage and Ch. 4 is C_{F2} voltage. The measured peak-to-peak C_{F1} and C_{F2} voltage ripple is 10 V (= 10 V/400 V = 2.5%) and 2 V (= 2 V/100 V = 2%) respectively, and dc-link capacitor half-line-frequency voltage ripple is 22 V (= 22 V/200 V = 11%). The balanced FC and dc-link capacitor voltages verify the modulation method and confirm the advantage of the self-balancing in the proposed circuit. In addition, as shown in Fig. 21, the small LC output filter provides good high-frequency attenuation and a maximum peak-to-peak current ripple amplitude of 4.35 A.

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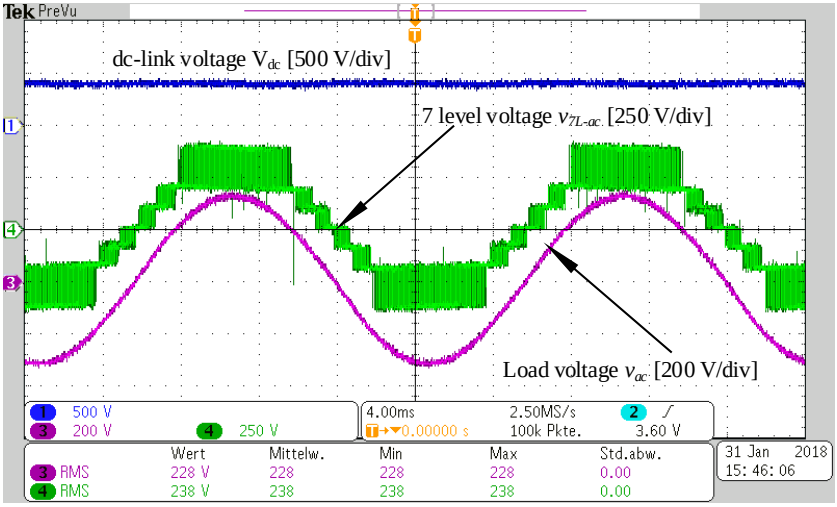
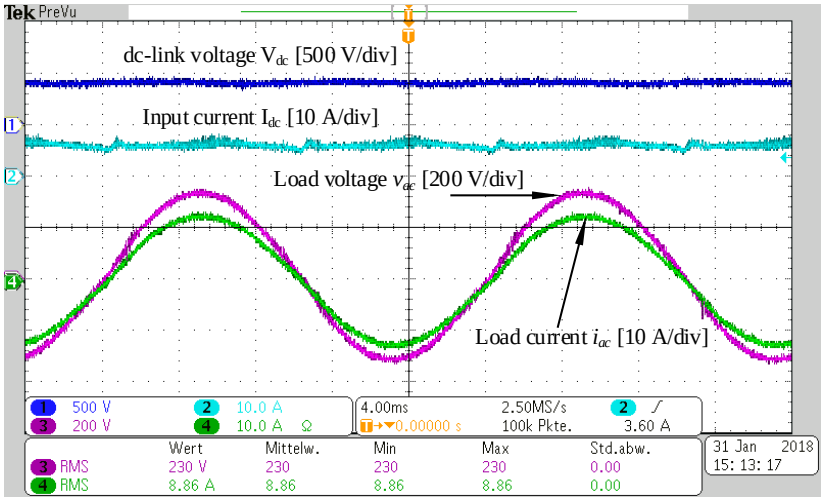
The reactive power operation mode is also tested as shown in Fig. 22 with power factor of 0.93 (inductive). The inverter still produces a good quality voltage and current waveform without high distortion (THD < 1.8 %).

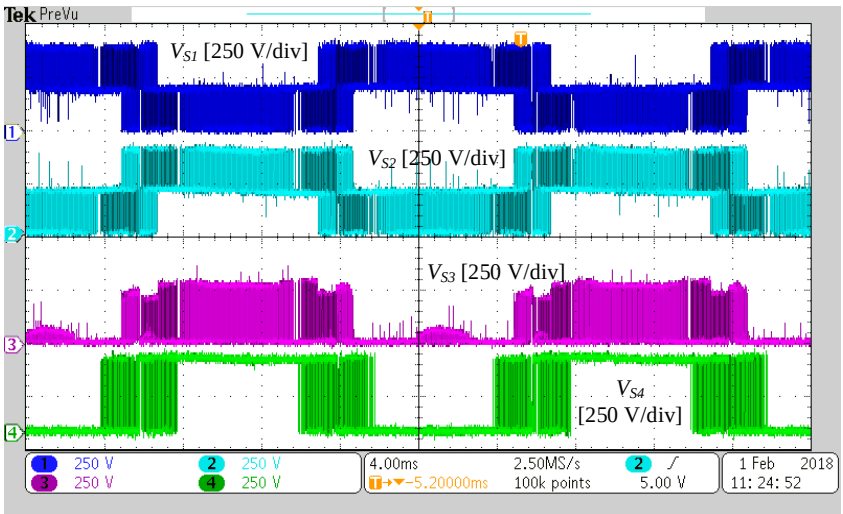


(a)



(b)

Fig. 17. Measured waveforms under unity power factor condition showing inverter input/output voltage/current waveforms. The measured output current THD is 2.15%.



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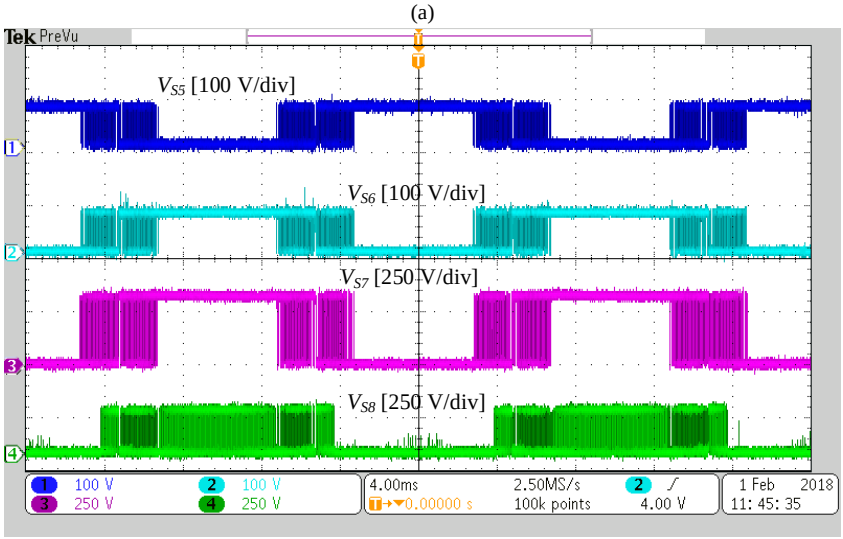
(a)



(b)

Fig. 18. Measured waveforms showing the voltage stress on the semiconductor devices.

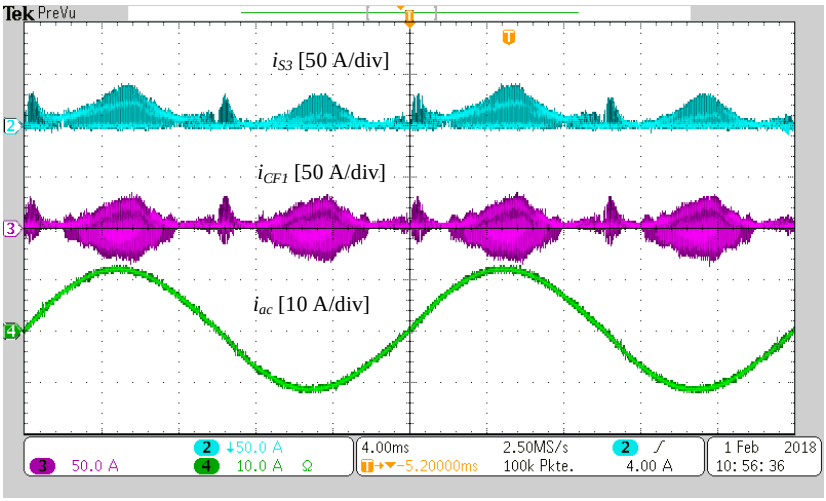


Fig. 19. Measured waveforms showing the current stress on C_{F1} and S_3 at full load current.

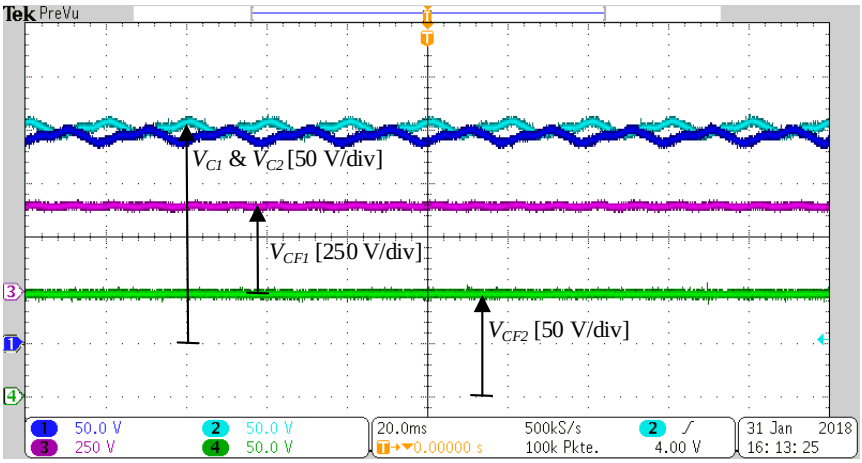


Fig. 20. Measured waveforms showing the input voltage, flying capacitor voltage, and upper and lower dc-link capacitor voltage.

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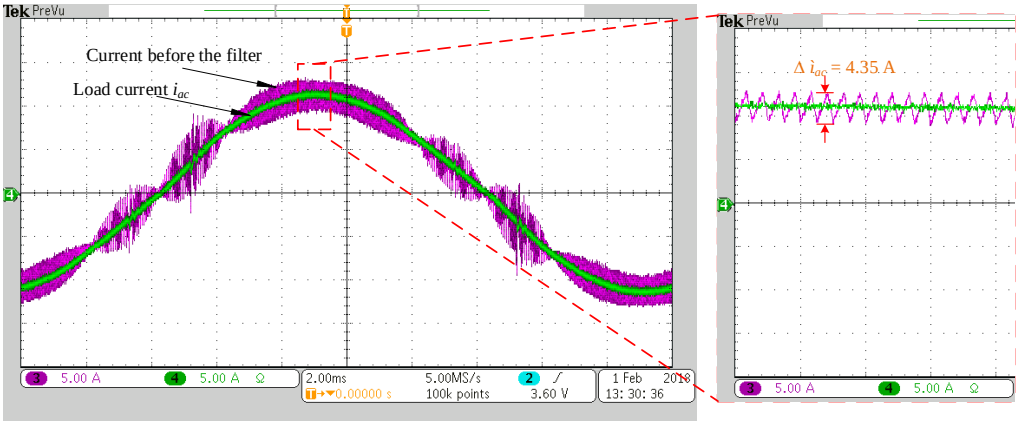


Fig. 21. Measured waveforms showing the inverter output currents (before and after the filter).

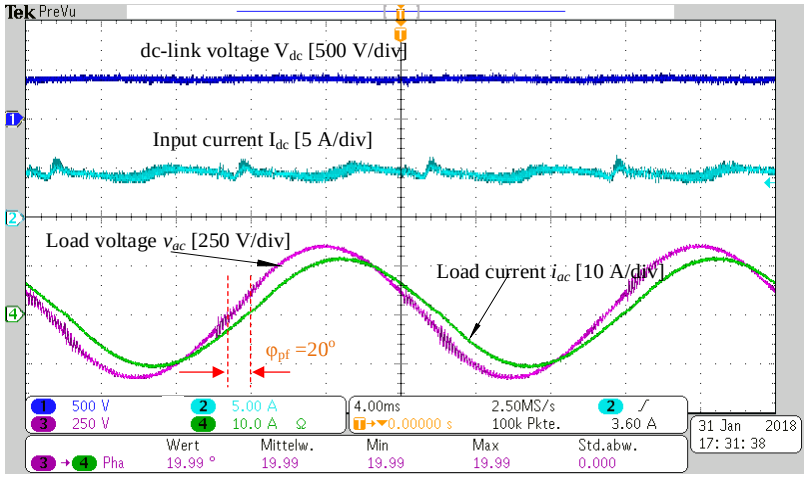
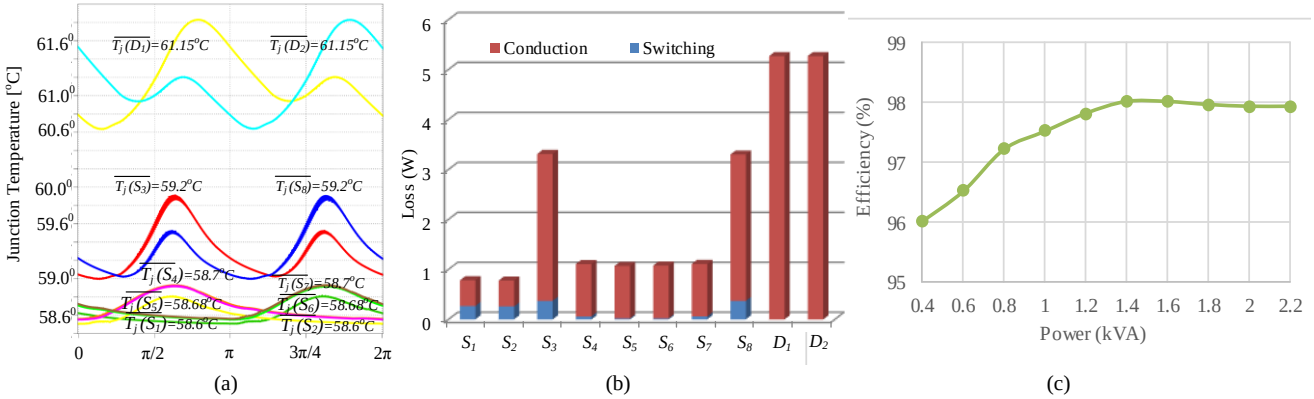


Fig. 22. Measured waveforms under reactive power condition (cos φ = 0.93) showing inverter input/output voltage and current waveforms.

The simulated averaged power loss distribution and the operating junction temperature (T_j) of the individual switching elements are presented in Fig. 23(a). A constant ambient temperature, T_A, of 40ºC is assumed in this analysis with uniform temperature distribution across the heat sink. As expected, the diodes and switches in the capacitor-charging path have higher loss (conduction) and hence relatively higher temperature ($\Delta\hat{T}_j \approx 3$℃) then the other switches. Fig. 23(b) show similar findings and the loss distribution across the switching components. Fig. 23(c) shows the measured efficiency of the prototype inverter across a range of output power levels. The peak efficiency of the inverter is 98.2%.



(a) (b) (c)

Fig. 23. (a) Steady state operating junction temperature of the semiconductor, (b) loss distribution, and (c) measured efficiency of the inverter.

VI. CONCLUSION

In this paper, a novel eight-switch seven-level Active Neutral Point Clamped inverter is proposed. Modulation techniques are explored and operation under both active and reactive power factor conditions are systematically analyzed. A comparative analysis and a set of design guidelines are presented and followed by simulation and experimental verification.

Compared to conventional seven-level inverter topologies, the ANPC inverter topology requires only eight power devices for a single-phase design and halves the dc-link voltage required to produce a given ac voltage output magnitude when compared to similar circuits. For applications such as for a grid-connected PV system, this may help eliminate additional power conversion stages (boost converters) and therefore increase the efficiency and reliability of the system. Further, this reduces the voltage stress on the dc-link capacitor, which reduces the cost and size of the system design. The inverter can operate at any power factor (leading or lagging) without requiring any changes to the modulation scheme.

Compared with other seven-level configurations, the performance demonstrated by the new inverter is highly competitive, potentially making it an appropriate topology choice for a wide-range of power conversion applications, e.g. variable-speed drives, electric vehicles (V2G/G2V technologies), grid-connected renewable energy systems.

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